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RTL8152B-VB-CG

INTEGRATED 10/100M ETHERNET CONTROLLER FOR USB APPLICATIONS

DATASHEET
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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2013/03/21	First release.
1.1	2013/07/15	Indicated Protocol Offload (ARP & NS) is supported at all speeds.

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1. General Description

The Realtek RTL8152B-VB-CG 10/100M Ethernet controller combines an IEEE 802.3u compliant Media Access Controller (MAC), USB bus controller, and embedded memory. A linear regulator (LDO) is incorporated for reduced BOM cost.

With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8152B-VB offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capabilities. The RTL8152B-VB features embedded One-Time-Programmable (OTP) memory.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments.

The RTL8152B-VB supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

The RTL8152B-VB supports 'RealWoW!' technology that enables remote wake-up of a sleeping PC through the Internet. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Note: The 'RealWoW!' service requires registration on first time use.

The RTL8152B-VB is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8152B-VB supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The RTL8152B-VB can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8152B-VB supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8152B-VB supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The device also features USB 2.0 technology. It provides higher bandwidth and improved protocols for data exchange between the host and the device. In addition, USB 2.0 offers a more aggressive power management feature that enables selective suspend to save energy.

The RTL8152B-VB is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, docking station, and embedded applications.

2. Features

Hardware

- Integrated 10/100M transceiver

- Auto-Negotiation with Next Page capability

- Supports USB 2.0 and 1.1

- Supports pair swap/polarity/skew correction

- Crossover Detection & Auto-Correction

- Supports Wake-On-LAN and 'RealWoW!' (Wake-On-WAN) Technology (see note 1)

- Supports ECMA-393 ECMA ProxZzzy Standard for sleeping hosts (see note 1)

- XTAL-Less Wake-On-LAN

- Supports 25MHz or 48MHz external clock (from oscillator or system clock source)

- Supports power down/link down power saving

- Transmit/Receive on-chip buffer support

- Embedded OTP memory

- Built-in linear regulator (LDO)

- Supports Customizable LEDs

- Controllable LED Blinking Frequency and Duty Cycle

- Supports hardware CRC (Cyclic Redundancy Check) function

- LAN disable with GPIO pin

- Supports LPM (Link Power Management)

- SPI Flash Interface

- Supports CDC-ECM

- 24-pin QFN 'Green' package

Software Offload

- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support

IEEE

- Supports Full Duplex flow control (IEEE 802.3x)

- Fully compliant with IEEE 802.3, IEEE 802.3u

- Supports IEEE 802.1P Layer 2 Priority Encoding

- Supports IEEE 802.1Q VLAN tagging

- Supports IEEE 802.3az-2010 (EEE)

Microsoft AOAC (Always On Always Connected)

- Supports 16-set 128-byte Wake-Up Frame pattern exact matching

- Supports link change wake up

- Supports Microsoft WPD (Wake Packet Detection)

- Supports Protocol Offload (ARP & NS) at all speeds

Intel CPPM (Converged Platform Power Management)

- Supports L1 with 3ms BESL

- Supports selective suspend

Note 1. Select between RealWoW! or ECMA, only one feature can be active at a time.

3. System Applications

■ USB 10/100M Ethernet on Motherboard, Dongle, Notebook, Docking station, or Embedded system

4. Pin Assignments
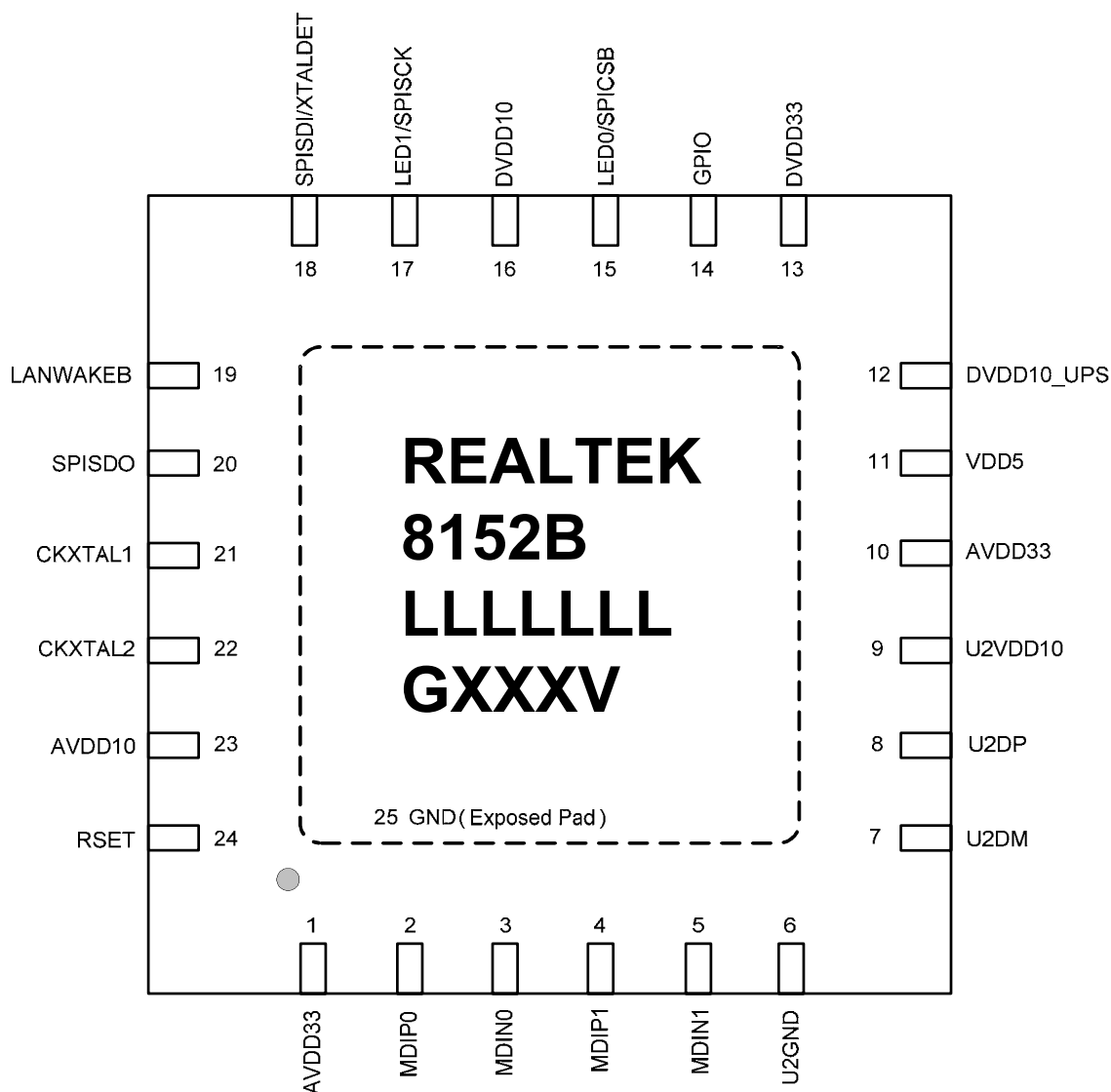
Figure 1.   Pin Assignments

4.1. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 1). The version number is shown in the location marked 'V'.

5. Pin Descriptions

The signal type codes below are used in the following tables:

    I: Input   O: Output

    P: Power

5.1. Power Management Pin

Table 1.   Power Management Pin

Symbol	Type	Pin No	Description
LANWAKEB	O	19	Power Management Event Output Pin (Active Low), minimum 7ms, maximum 9ms.

5.2. USB Interface Pins

Table 2.   USB Interface Pins

Symbol	Type	Pin No	Description
U2DP	IO	8	USB 2.0/USB 1.1 Differential Signal Pair.
U2DM	IO	7	

5.3. Transceiver Interface Pins

Table 3.   Transceiver Interface Pins

Symbol	Type	Pin No	Description
MDIP0	IO	2	In MDI mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	3	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	4	In MDI mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	5	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.

5.4. Clock Pins

Table 4.   Clock Pins

Symbol	Type	Pin No	Description
CKXTAL1	I	21	Input of 25MHz Clock Reference.
CKXTAL2	IO	22	Output of 25MHz Clock Reference. Input of 25MHz or 48MHz External Clock Source.
XTALDET/SPISDI	I	18	Power-Up Strapping Pin. Pull High: 25MHz clock source Pull Low: 48MHz clock source

Note: When a 25MHz clock is used the XTALDET pin must be pulled high by a resistor during power-up. When a 48MHz clock is used the XTALDET pin must be pulled low by a resistor during power-up.

5.5.   LDO Regulator and Reference Pins

Table 5.   LDO Regulator and Reference Pins

Symbol	Type	Pin No	Description
AVDD33	P	10	Linear Regulator (LDO) 3.3V Output. *Note: The embedded LDO is designed for RTL8152B-VB internal use only. Do not provide this power source to other devices.*
AVDD10	P	23	Linear Regulator (LDO) 1.05V Output. *Note: The embedded LDO is designed for RTL8152B-VB internal use only. Do not provide this power source to other devices.*
DVDD10_UPS	P	12	Linear Regulator (LDO) 1.05V Output. *Note: The embedded LDO is designed for RTL8152B-VB internal use only. Do not provide this power source to other devices.*
RSET	I	24	Reference. External resistor reference.

5.6.   SPI Flash Pins

Table 6.   SPI Flash Pins

Symbol	Type	Pin No	Description
SPICSB	O	15	SPI Flash Chip Select.
SPISDO	I	20	Input from SPI Flash Serial Data Output Pin.
SPISDI/XTALDET	O	18	Output to SPI Flash Serial Data Input Pin.
SPISCK	O	17	SPI Flash Serial Data Clock.

5.7. LED Pins

Table 7.   LED Pins

Symbol	Type	Pin No	Description
LED0	O	15	See section 6.2 Customizable LED Configuration, page 8 for details.
LED1	O	17	

Note: During power down mode, the LED signals are logic high.

5.8. Power and Ground Pins

Table 8.   Power and Ground Pins

Symbol	Type	Pin No	Description
VDD5	P	11	Analog 5.0V Power Supply.
AVDD33	P	1, 10	Analog 3.3V Power Supply.
DVDD33	P	13	Digital 3.3V Power Supply.
AVDD10	P	23	Analog 1.05V Power Supply.
DVDD10	P	16	Digital 1.05V Power Supply.
DVDD10_UPS	P	12	Digital 1.05V Uninterruptible Power Supply.
U2VDD10	P	9	USB 2.0/USB 1.1 Digital 1.05V Power Supply.
U2GND	P	6	USB 2.0/USB 1.1 Ground.
GND	P	25	Ground (Exposed Pad).

Note: Refer to the latest schematic circuit for correct configuration.

5.9. GPIO Pin

Table 9.   GPIO Pin

Symbol	Type	Pin No	Description
GPIO	IO	14	General Purpose Input/Output Pin. Link OK Feature: Output Pin (Active High) Power Saving Feature: Output Pin (Active Low) LAN Disable Mode: Input Pin (Active Low)

6.   Functional Description

6.1.   USB Interface

The SIE (Serial Interface Engine) employs a robust hardwired USB protocol implementation so that the entire USB interface operation can be done without firmware intervention. For all three types of End Points (Bulk-IN, Bulk-OUT, and Interrupt-IN), appropriate responses and handshake signals are generated by the SIE. The SIE analog transceiver complies fully with driver and receiver characteristics defined in USB Specification Rev. 2.0

6.1.1.   USB Configurations

The RTL8152B-VB supports two networking configurations, ECM (Ethernet Networking Control Model) configuration, and in-house configuration. The ECM configuration complies with CDC-ECM, and is a general Ethernet networking model that enables network communication without installing additional vendor specific drivers. The in-house configuration requires a vendor specific driver to support enhanced features and optimized performance.

6.1.2.   Endpoint 0

All USB devices support a common access mechanism for accessing information through this control pipe. Associated with the control pipe at endpoint 0 is the information required to completely describe the USB device. This pipe also provides the register read and write to the RTL8152B-VB.

6.1.3.   Endpoint 1 Bulk-IN

The maximum Bulk-IN packet size is 512 bytes. Each Ethernet packet is transferred to the HOST by this Endpoint. If the Ethernet packet is larger than 512 bytes, the RTL8152B-VB splits the Ethernet packet into multiples of 512 bytes. The HOST treats USB packets that are less than 512 bytes or are equal to zero as End of Ethernet packets.

6.1.4.   Endpoint 2 Bulk-OUT

The HOST sends the USB packet to Ethernet. If the Ethernet packet is larger than 512 bytes, the Host will send the Ethernet packet in multiples of 512 bytes. A USB packet that is less than 512 bytes or is equal to zero is treated as an End of Ethernet packet.

The Ethernet packet (containing multiple USB packets) will be queued in the TX FIFO and transmitted when possible. If the Ethernet packet is transmitted without error, the TX FIFO space that was occupied by the transmitted Ethernet packet will be released. If the 2K TX FIFO is full, the RTL8152B-VB will respond with a NYET when the host tries to Bulk-OUT more USB packets.

It is possible to have multiple Ethernet packets in the TX FIFO simultaneously. If an Ethernet packet is to be transmitted but experiences collisions more than 16 times (default), this is called a transmit abort and the packet will be skipped for transmission by the RTL8152B-VB.

6.1.5.   Endpoint 3 Interrupt-IN

The Interrupt Endpoint (EP3) can be used to poll the current link speed and link ok status of the RTL8152B-VB.

6.2. *Customizable LED Configuration*

The RTL8152B-VB supports customizable LED operation modes via OCP register offset 0xDD90h. Table 10 describes the different LED actions.

Table 10. LED Select

Bit	Symbol	RW	Description
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

Configure OCP register offset 0xDD90h to support your own LED signals. For example, if the value in the OCP offset 0xDD90 is 0xA1h (10100001b), the LED actions are:

- LED 0: On only in 10M mode, with no blinking during TX/RX

- LED 1: On only in 100M mode, with TX/RX blinking

Table 11. Customized LEDs

	LINK		ACT
Speed	Link 10M	Link 100M	-
LED 0	Bit 0	Bit 1	Bit 3
LED 1	Bit 4	Bit 5	Bit 7

Table 12. LED Feature Control-1

Feature Control	Bit12	Bit13	Bit14	Bit15
0	LED0 Low Active	LED1 Low Active	RSVD	Indicates Option 1 of Table 14 is selected
1	LED0 High Active	LED1 High Active	RSVD	Indicates Option 2 of Table 14 is selected

Table 13. LED Feature Control-2

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Table 14): Selected Speed LINK+ Selected Speed ACT Option 2 (see Table 14): Selected Speed LINK+ All Speed ACT

Note 1: ACT means blinking TX and RX. LINK indicates Link 10M and Link 100M.
Note 2: There is a special mode: LED OFF Mode → Set all bits to 0.

Table 14.   LED Option 1 & Option 2 Settings

Link Bit		Active Bit	Description		
10	100		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	LED Off		
0	0	1	-	$Act_{10}+Act_{100}$	$Act_{10}+Act_{100}$
0	1	0	$Link_{100}$	-	-
0	1	1	$Link_{100}$	Act_{100}	$Act_{10}+Act_{100}$
1	0	0	$Link_{10}$	-	-
1	0	1	$Link_{10}$	Act_{10}	$Act_{10}+Act_{100}$
1	1	0	$Link_{10}+Link_{100}$	-	-
1	1	1	$Link_{10}+Link_{100}$	$Act_{10}+Act_{100}$	$Act_{10}+Act_{100}$

Note:
Act_{10} = LED blinking when Ethernet packets transmitted/received at 10Mbps.
Act_{100} = LED blinking when Ethernet packets transmitted/received at 100Mbps.
$Link_{10}$ = LED lit when Ethernet connection established at 10Mbps.
$Link_{100}$ = LED lit when Ethernet connection established at 100Mbps.

6.2.1.   LED Blinking Frequency Control

The RTL8152B-VB also supports LED blinking frequency and duty cycle control via OCP register offset DD92h to control user's LED blinking frequency and duty cycle (see Table 15). For example, if the OCP register offset 0xDD92 is 0x0B (00001011b), the LED blinking frequency is 80ms and duty cycle is 75%. The LED state is shown in Figure 2 (assumes the LED is low active).

Table 15.   LED Blinking Frequency Control

Bit	RW	Description
3:2	RW	LED Blinking Frequency 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
1:0	RW	LED Blinking Duty Cycle 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%
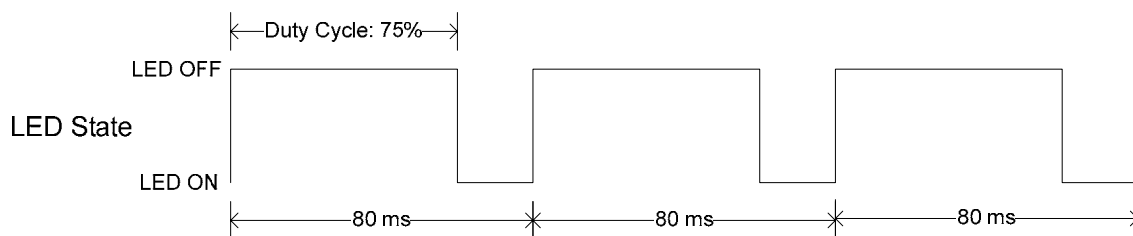
Note: Assumes the LED is low active.

Figure 2.   LED Blinking Frequency and Duty Cycle

6.3. PHY Transceiver

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8152B-VB operates at 10/100Mbps over standard CAT.5 UTP cable (100Mbps), and CAT.3 UTP cable (10Mbps).

6.3.1.   PHY Transmitter

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2.   PHY Receiver

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.3.3.   Link Down Power Saving Mode

The RTL8152B-VB implements link-down power saving mode, greatly improving power consumption when the network cable is disconnected. The RTL8152B-VB automatically enters link down power saving mode within three seconds after the cable is disconnected from it. Once it enters link down power saving mode, it transmits normal link pulses on its TX pins and continues to monitor the RX pins to detect incoming signals. After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

6.4. SPI Flash

SPI (Serial Peripheral Interface) Flash is enabled by the RTL8152B-VB through the Chip Select pin, and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). The SPI flash utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Table 16.   SPI Flash Interface

SPI Flash	Description
SO	Input Data Bus.
SI	Output Data Bus.
SCK	SPI Flash Serial Data Clock.
CS	SPI Flash Chip Select.

6.5. Energy Efficient Ethernet (EEE)

The RTL8152B-VB supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps and 100Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

6.6. Link Power Management (LPM)

The RTL8152B-VB supports Link Power Management (LPM). It provides an efficient way to manage bus and system power via hosts and hubs. It implements a power sleep state that reduces power consumption by providing faster suspend and resume times. The four power management states for USB are L0 (On), L1 (Sleep), L2 (Suspend) and L3 (Off). To reduce power consumption when the system is in Low Power State, some of the circuits are disabled.

Refer to http://www.usb.org/developers/docs/.

6.7. LAN Disable Mode

The RTL8152B-VB supports 'LAN Disable Mode', which uses an external signal to control whether the NIC is enabled or disabled.

6.8. Power Management

The RTL8152B-VB complies with ACPI (Rev 1.0, 1.0b, 2.0), Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8152B-VB can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the USB interface when such a packet or event occurs. The system is then restored to a normal state to process incoming jobs.

When the RTL8152B-VB is in power down mode:

- The RX state machine is stopped. The RTL8152B-VB monitors the network for wake-up events such as a Magic Packet and Wake-Up Frame in order to wake up the system. When in power down mode, the RTL8152B-VB will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the RX on-chip buffer.

- The on-chip buffer status and packets that have already been received into the RX on-chip buffer before entering power down mode are held by the RTL8152B-VB.

- Transmission is stopped. USB transactions are stopped. The TX on-chip buffer is held.

- After being restored to D0 state, the RTL8152B-VB transmits data that was not moved into the TX on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8152B-VB, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8152B-VB adapter.

- The received Magic Packet does not contain a CRC error.

- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8152B-VB, e.g., a broadcast, multicast, or unicast address to the current RTL8152B-VB adapter.

- The received Wake-Up Frame does not contain a CRC error.

- The 16-bit CRC of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8152B-VB is configured to allow direct packet wake-up, e.g., a broadcast, multicast, or unicast network packet.

- The 128-byte of the received Wake-Up Frame matches the 128-byte of the sample Wake-Up Frame pattern given by the local machine's OS.

Note 1: 16-bit CRC: The RTL8152B-VB supports 16-set 16-bit CRC wake-up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^5+1$.

Note 2: 128-byte Wake-Up Frame: The RTL8152B-VB supports 16-set 128-byte wake-up frames. If enabled, the 16-bit CRC wake-up match will be disabled.

6.9. Protocol Offload

Protocol offload is a task offload supported by Microsoft Windows 7. It maintains a network presence for a sleeping higher power host. Protocol offload prevents spurious wake-up and further reduces power consumption. It maintains connectivity while hosts are asleep, including receiving requests from other nodes on the network, ignoring packets, generating packets while in the sleep state (e.g., the Ethernet Controller will generate ARP responses if the same MAC and IPv4 address are provided in the configuration data), and intelligently wake-up host systems. The RTL8152B-VB supports the ECMA (European Computer Manufacturers Association) specification including proxy configuration and management, IPv4 ARP, IPv6 NDP, and wake-up packets. The RTL8152B-VB also supports optional ECMA items such as QoS tagged packets and duplicate address detection.

6.10. XTAL-Less Wake-On-LAN

The RTL8152B-VB supports board level design with an external 25MHz or 48MHz clock source instead of the crystal.

The external clock source may stop generating the clock when in suspend mode (S3/S4/S5). To support the Wake-On-LAN function without the external clock source, the RTL8152B-VB will automatically change its source clock from the external clock to an internal self-oscillating auxiliary clock when it enters suspend mode. Note that when in suspend mode, the auxiliary clock can establish only a 10Mbps link and does not support ARP/NS offload and ECMA ProxZzzy.

6.11. *Wake Packet Detection (WPD)*

The RTL8152B-VB supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

Refer to the Microsoft Wake Packet Detection (WPD) Interface Specification for details (http://msdn.microsoft.com/en-us/library/hh440160(v=vs.85).aspx).

6.12. *'RealWoW!' (Wake-On-WAN) Technology*

The RTL8152B-VB supports Realtek 'RealWoW!' technology that allows the RTL8152B-VB to send keep alive packets to the Wake Server when the PC is in sleeping mode. Realtek 'RealWoW!' can pass wake-up packets through a NAT (Network Address Translation) device. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Users can login into the Wake Server via the Internet to wake the selected sleeping PC. Registration of Account information to the Wake Server is required on first time use.

6.13. *Always On Always Connected*

The RTL8152B-VB supports Microsoft's AOAC (Always On Always Connected) model. The AOAC platform can enter the system state 'Connected Standby' and allow the RTL8152B-VB to enter a low-power state. The RTL8152B-VB will maintain Layer 2 connectivity and generate a wake signal when one of the following conditions is satisfied:

- Link status becomes 'connected'
- Link status becomes 'disconnected'
- Receives a WOL pattern
- Receives a wildcard pattern

7. LDO Regulator

The RTL8152B-VB incorporates three linear Low-Dropout (LDO) regulators that feature high power supply ripple rejection and low output noise. The RTL8152B-VB embedded LDO regulators do not require power inductors on the PCB; only an output capacitor between its output and analog ground for phase compensation, which saves cost and PCB real estate.

The output capacitors (and bypass capacitors) should be placed as close as possible to the power pins for adequate filtering.

Note 1: The embedded LDO is designed for RTL8152B-VB internal use only. Do not provide this power source to other devices.

Note 2: The LDO 1.05V output pin (DVDD10_UPS) must be separated from the other LDO 1.05V output pin (AVDD10).

8.   Characteristics

8.1.   Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 17.   Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD5IN	Supply Voltage 5.0V	-0.3	5.5	V
VDD33OUT, AVDD33, DVDD33	Supply Voltage 3.3V	-0.3	3.63	V
AVDD10, DVDD10, DVDD10_UPS	Supply Voltage 1.05V	-0.3	1.32	V
Dcinput	Input Voltage	-0.3	Corresponding Supply Voltage + 10%	V
Dcoutput	Output Voltage	-0.3	Corresponding Supply Voltage + 10%	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the latest schematic circuit for correct configuration.

8.2.   Recommended Operating Conditions

Table 18.   Recommended Operating Conditions

Description	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD5	4.75	5.0	5.25	V
	AVDD33, DVDD33	3.14	3.3	3.46	V
	AVDD10, DVDD10, DVDD10_UPS	1.0	1.05	1.1	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the latest schematic circuit for correct configuration.

8.3. Crystal Requirements

Table 19. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type.	-	25/48	-	MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. $T_a = 0°C \sim +70°C$.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. $T_a = 25°C$.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	70	Ω
CL	Load Capacitance.	16	-	20	pF
DL	Drive Level.	-	-	0.5	mW

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.
Note 3: The ESR maximum value of 70ohm is based on shunt capacitance (Co) less than 7pF.
Note 4: The accuracy of the crystal resonance frequency can be achieved by matching the load capacitance correctly to the designed-in circuit. The latest schematic circuit recommends two external capacitors of 27pF connected between the crystal and ground. To match this use the load capacitance specified by the crystal manufacturer of 16~20pF.

8.4. Oscillator Requirements

Table 20. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25/48	-	MHz
Frequency Stability	$T_a = 0°C \sim +70°C$	-30	-	+30	ppm
Frequency Tolerance	$T_a = 25°C$	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter	-	-	-	200	ps
Vp-p	-	3.15	3.3	3.45	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

8.5. Environmental Characteristics

Table 21. Environmental Characteristics

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C

8.6. DC Characteristics

Table 22.   DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD5	5.0V Supply Voltage	-	4.75	5.00	5.25	V
AVDD33, DVDD33	3.3V Supply Voltage	-	3.14	3.30	3.46	V
AVDD10, DVDD10, DVDD10_UPS	1.05V Supply Voltage	-	1.00	1.05	1.10	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9*VDD33	-	VDD33	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 4mA	0	-	0.1*VDD33	V
V_{ih}	Minimum High Level Input Voltage	-	2.0	-	-	V
V_{il}	Maximum Low Level Input Voltage	-	-	-	0.8	V
I_{in}	Input Current	Vin = VDD33 or GND	0	-	0.5	µA
Icc5	Average Operating Supply Current from 5.0V	At 100Mbps with heavy network traffic	-	0.4	-	mA
Icc33	Average Operating Supply Current from 3.3V	At 100Mbps with heavy network traffic	-	24	-	mA
Icc10	Average Operating Supply Current from 1.05V	At 100Mbps with heavy network traffic	-	60	-	mA

Note: Refer to the latest schematic circuit for correct configuration.

8.7. Reflow Profile Recommendations

Table 23.   Reflow Profile Recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Minimum Preheat Temperature (T_{smin})	100°C	150°C
Maximum Preheat Temperature (T_{smax})	150°C	200°C
Preheat Time (t_S) from T_{smin} to T_{smax}	60~120 seconds	60~120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second max.	3°C/second max.
Liquidus Temperature (T_L)	183°C	217°C
Time (t_L) Maintained above T_L	60~150 seconds	60~150 seconds
Peak Package Body Temperature (T_p)	235°C	260°C
Time (t_p)^2 within 5°C of Peak T_P	20 seconds	20 seconds
Ramp-Down Rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature (T_p)	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the topside of the package, measured on the package body surface.
Note 2: Tolerance for Tp is defined as a supplier's minimum and a user's maximum.
Note 3: Reference document: IPC/JEDEC J-STD-020D.1.

8.8. AC Characteristics

8.8.1. SPI Flash Commands

Table 24. SPI Flash Commands

Command	Operation Code	Action
WREN	06h	Write Enable.
WRDI	04h	Write Disable.
RDID	9Fh	Read Manufacturer and Product ID.
RDSR	05h	Read Status Register.
WRSR	01h	Write Status Register.
Read	03h	Read.
Page Program	02h	Page Program.
Sector Erase (4K)	20h	Erase The Selected Sector.
Block Erase (64K)	D8h	Erase The Selected Block.
Chip Erase	60h or C7h	Erase Whole Chip.

8.8.2. SPI Flash Interface Timing Sequences
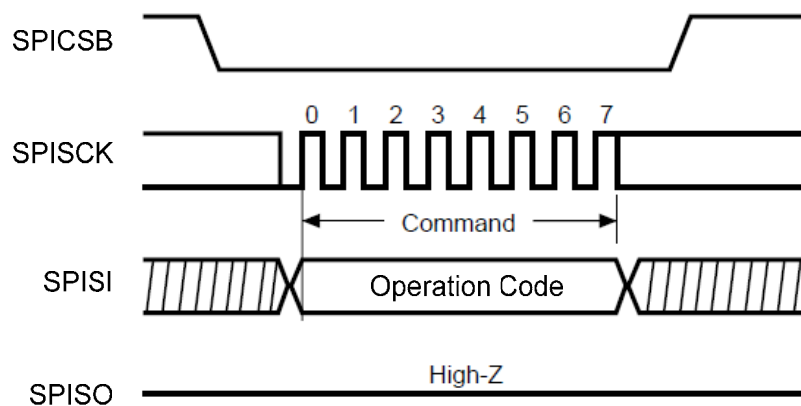
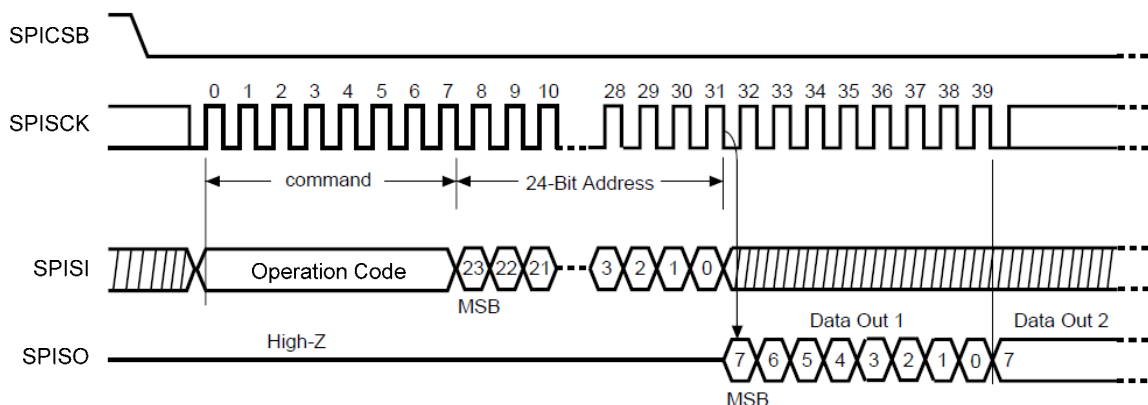**Figure 3. WREN/WRDI Timing Sequence**

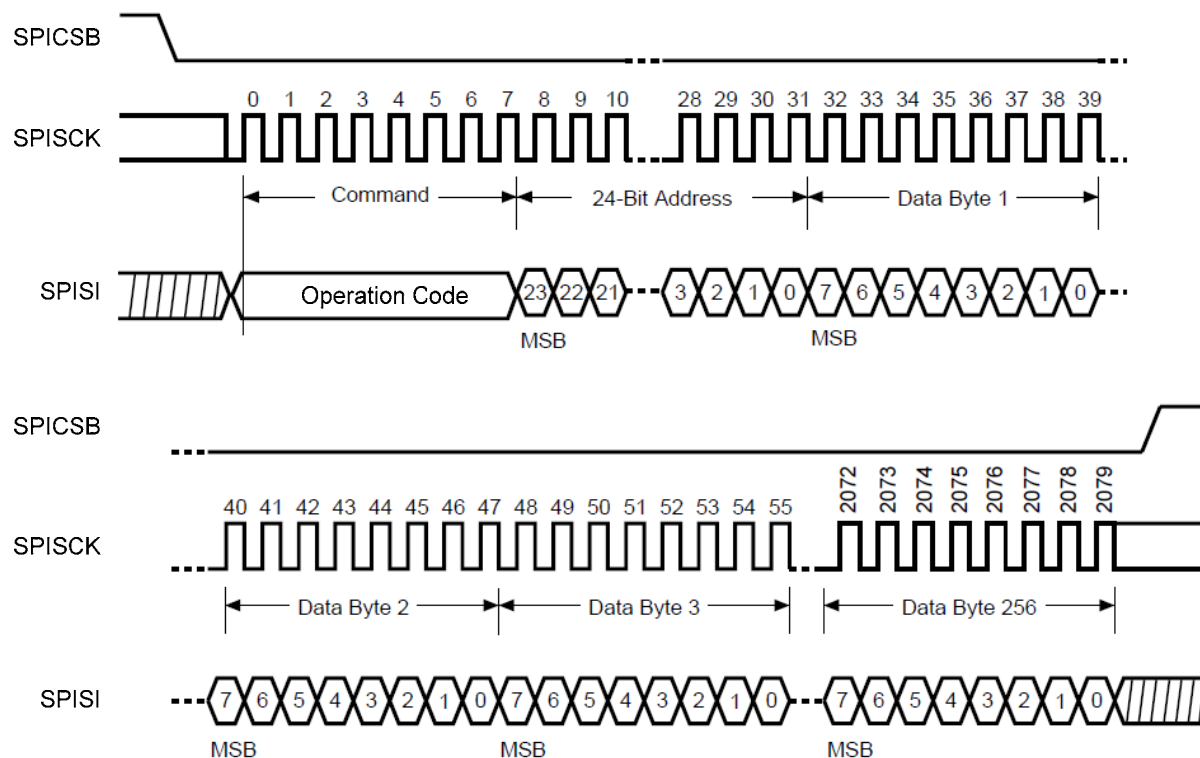

Figure 4. Read Timing Sequence

Figure 5.   Page Program Timing Sequence
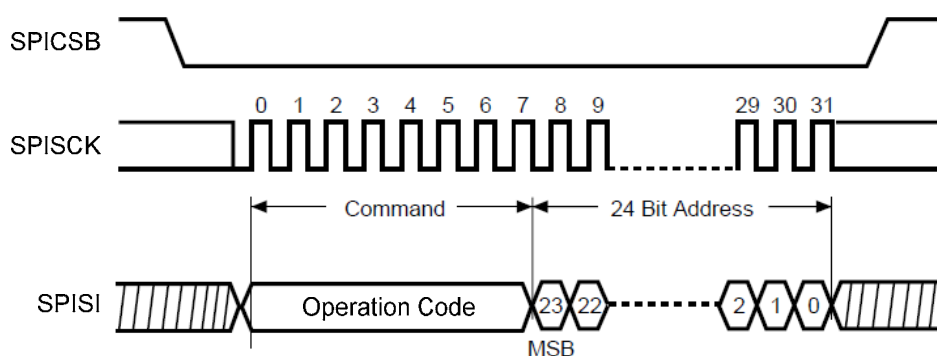

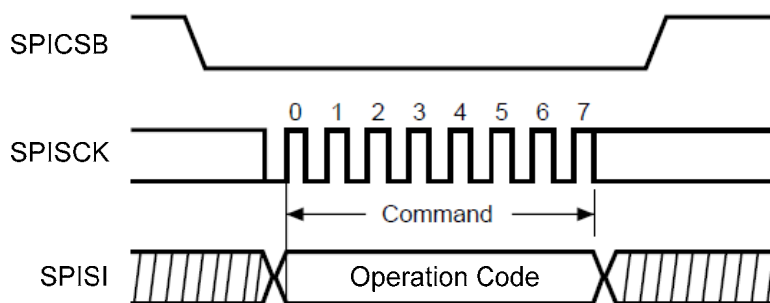Figure 6.   Sector/Block Erase Timing Sequence

Figure 7.   Chip Erase Timing Sequence

8.8.3.   SPI Flash Type Supported

Table 25.   SPI Flash Type Supported

Manufacturer	Flash Part No.	Density (Mb)	Maximum Freq. (MHz)
MXIC	MX25L4006E	4	86
	MX25L8006E	8	86
	MX25L1606E	16	86
Winbond	W25X40CV	4	80
	W25Q40BV	4	80
	W25Q80BV	8	80
	W25Q16CV	16	80
Micron	M25P40	4	75
	M25PX80	8	75
	M25PX16	16	75

Note 1: The Flash clock frequency should be 33MHz or higher.

Note 2: Flash density should be 4Mb or more. 4Mb is only for single OS driver. For feature extensions, 8Mb is recommended.

9. Mechanical Dimensions
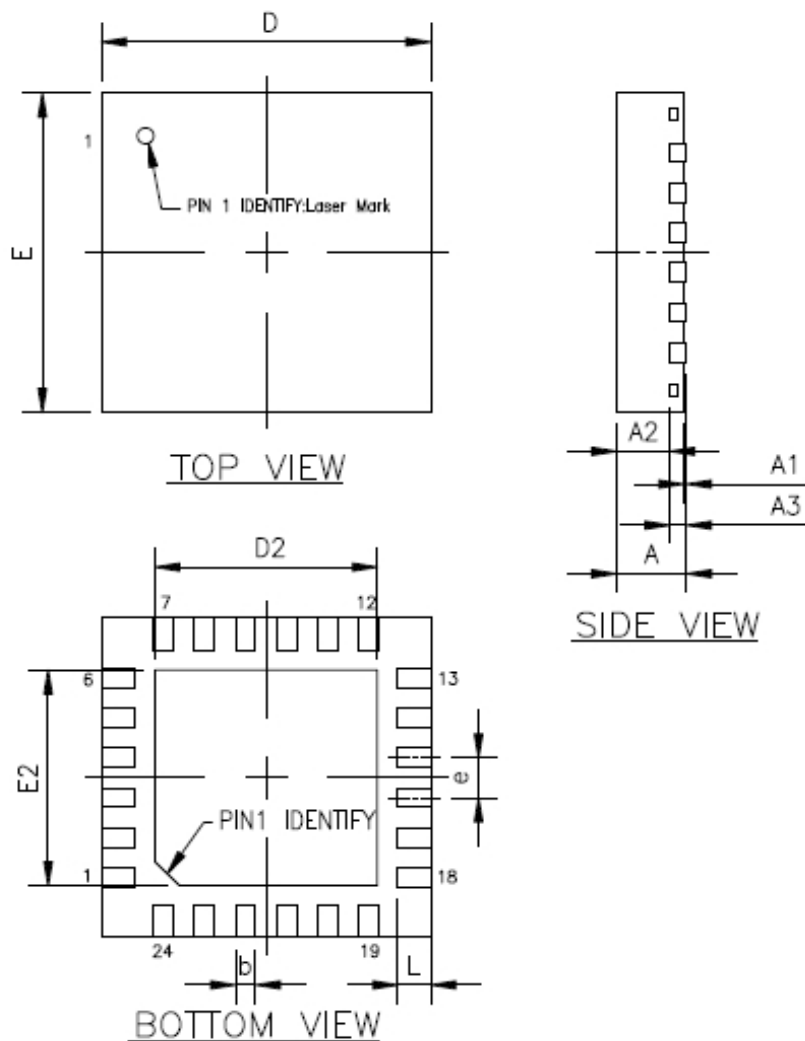
Symbol	Dimension in mm			Dimension in inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	-	0.65	0.70	-	0.026	0.028
A_3	0.20REF			0.008REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	4.00BSC			0.158BSC		
D2/E2	2.45	2.70	2.95	0.096	0.106	0.116
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

10. Ordering Information

Table 26.   Ordering Information

Part Number	Package	Status
RTL8152B-VB-CG	24-Pin QFN 'Green' Package	-

Note: See page 3 for package ID information.