

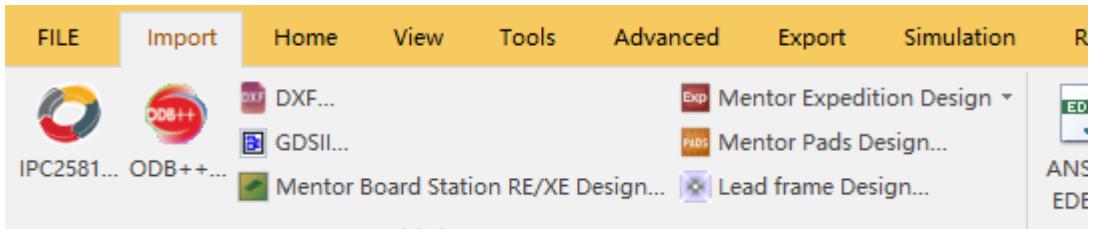
SI WAVE 使用教程

作者: 向仔州

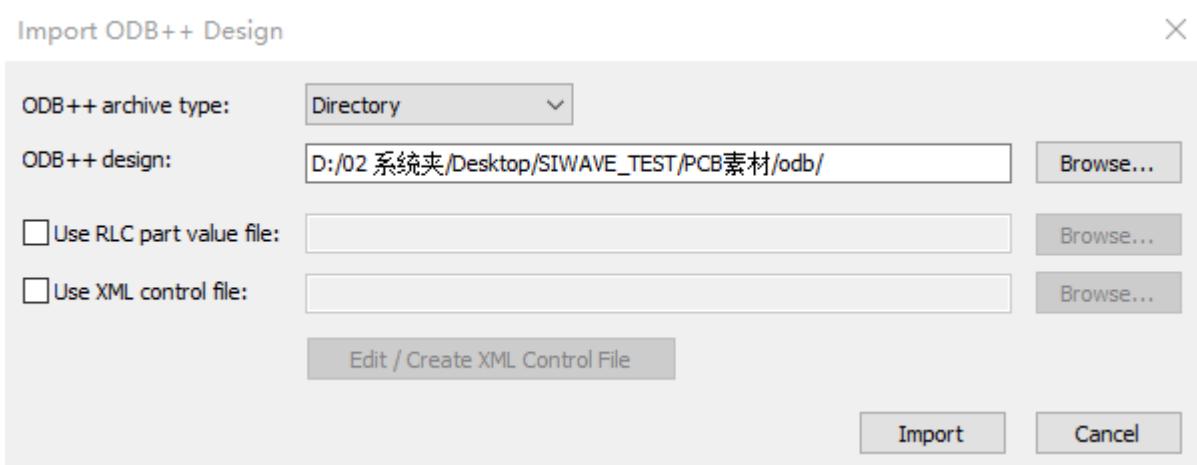
确保在安装 maxwell 中安装好了 siwave 软件, 至于安装教程请查阅《maxwell 使用教程》。

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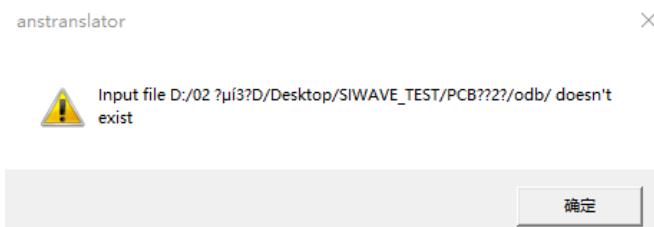
导入 Altium designer 制作的 ODB++ PCB 文件



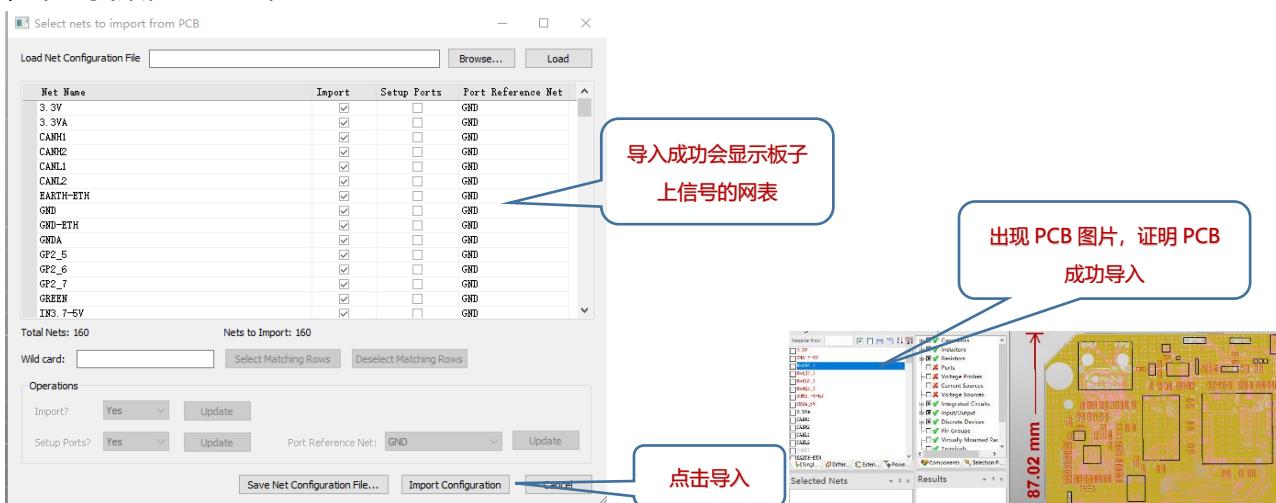
odb
这就是 AD 生成的 odb 目录，全部导入。

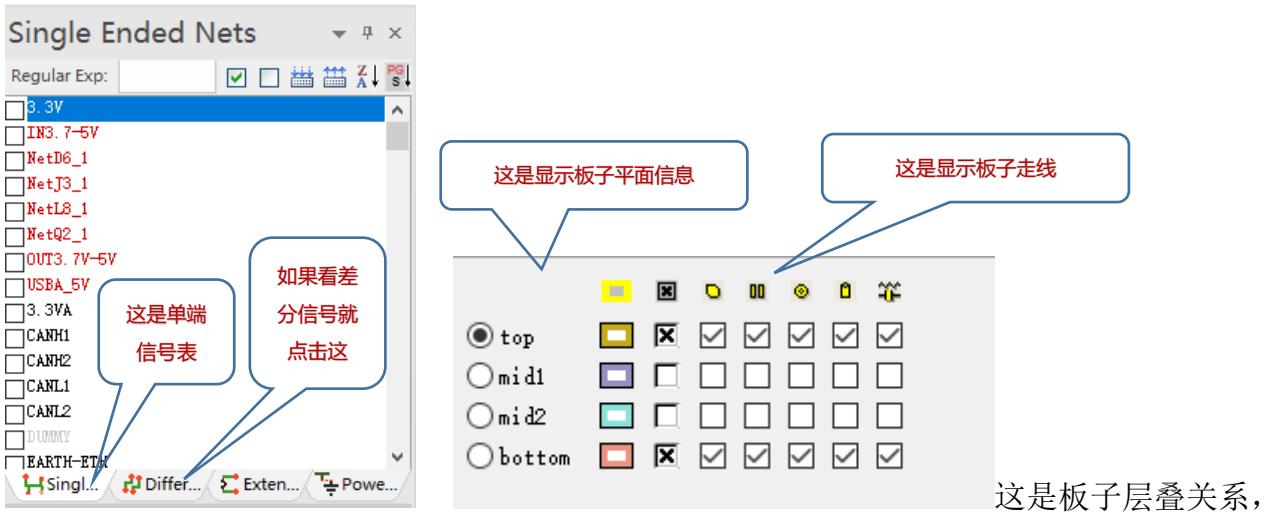


input file doesn't exist 错误

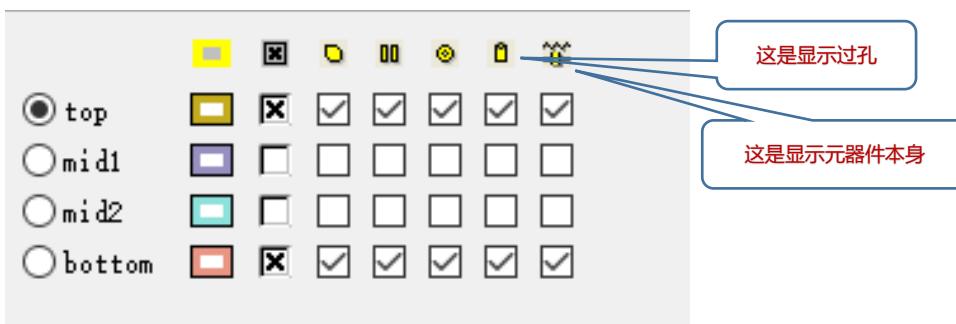


这是因为你的目录有中文路径，就是放在桌面，但是“桌面”也是中文，也不得行。必须放在全英文路径下。我放在了 E 盘下。





因为我是四层板，我这里只显示顶层和底层。



PCB 板层叠设置



每层名字

类型选择，每层是绝缘材质还是金属材质

每层厚度

本层导电用什么材料选的 EDB 铜

有了材料自动显示，自动显示导电材料的电导率

本层不导电的区域，比如绿油位置，采用什么材料填充这里选的空气

PCB 加工蚀刻时，导线不完全是矩形的，所以这里设置

如果以上铜箔材料和绝缘材料没有想要的，就在这儿添加自定义的材

空气材料的相对介电常数

对本层铜进行粗糙度设置

Select all DIELECTRIC layers Scheme-1 Save Current Color Scheme Color scheme As Is Set as Default Default Scheme for new projects: SIwave

Thickness change affects die elevations Edit Material Properties Invert Stackup Conformal Coat Units mm Copper Weight

OK Cancel

现在设置顶层铜导体，绝缘层用 FR4

第2层是填充绝缘层，所以直接 FR4 填充

点击 OK 设置完成

第3层是铜，电源层，所以设置铜导体和 FR4 填充绝缘层

叠层设置完成后，相对显示绿色

修改焊盘

Verify Padstacks...

点击进入

Padstack Editor

Cross-Sectional View

Padstack(s)

Pad_Simple_X50.0000Y50.0000H30.00

Add Delete Copy

Padstack Properties

Name: Pad_Simple_X50.000

Via Plating

Ratio 100% Absolute 0 mm

Via Material

copper EDB cooper

Layer Pad Antipad Thermal Relief Pad

top	Circle (R: 0.381)	None	None
Dielectric_1	Circle (R: 0.381)	None	None
mid1	Circle (R: 0.381)	None	None
Dielectric_2	Circle (R: 0.381)	None	None
mid2	Circle (R: 0.381)	None	None
Dielectric_3	Circle (R: 0.381)	None	None
bottom	Circle (R: 0.381)	None	None

Top-Down View

Polygonal Pad Edit

OK Cancel

Select All Metal Layers Select All Dielectric Layers

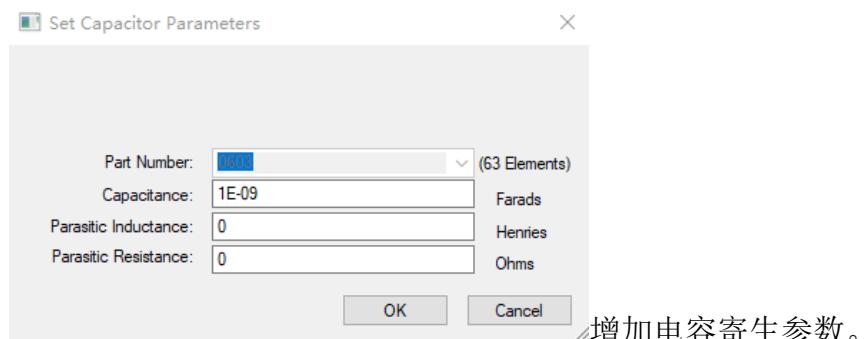
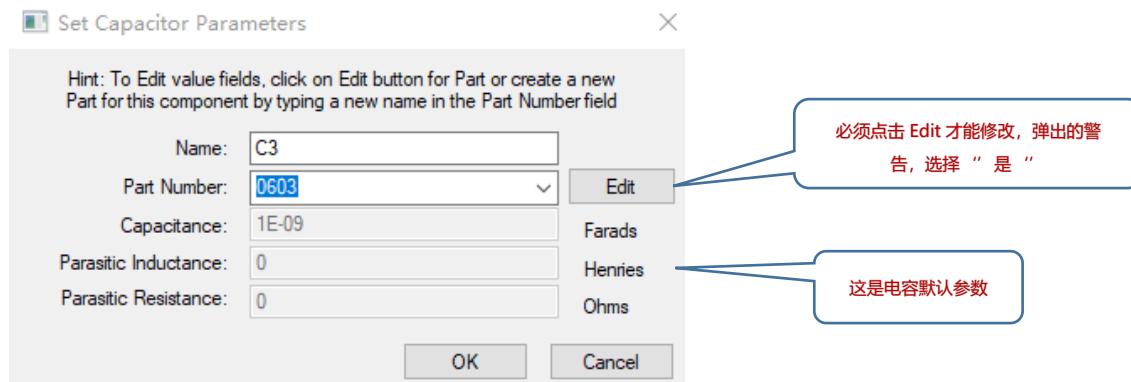
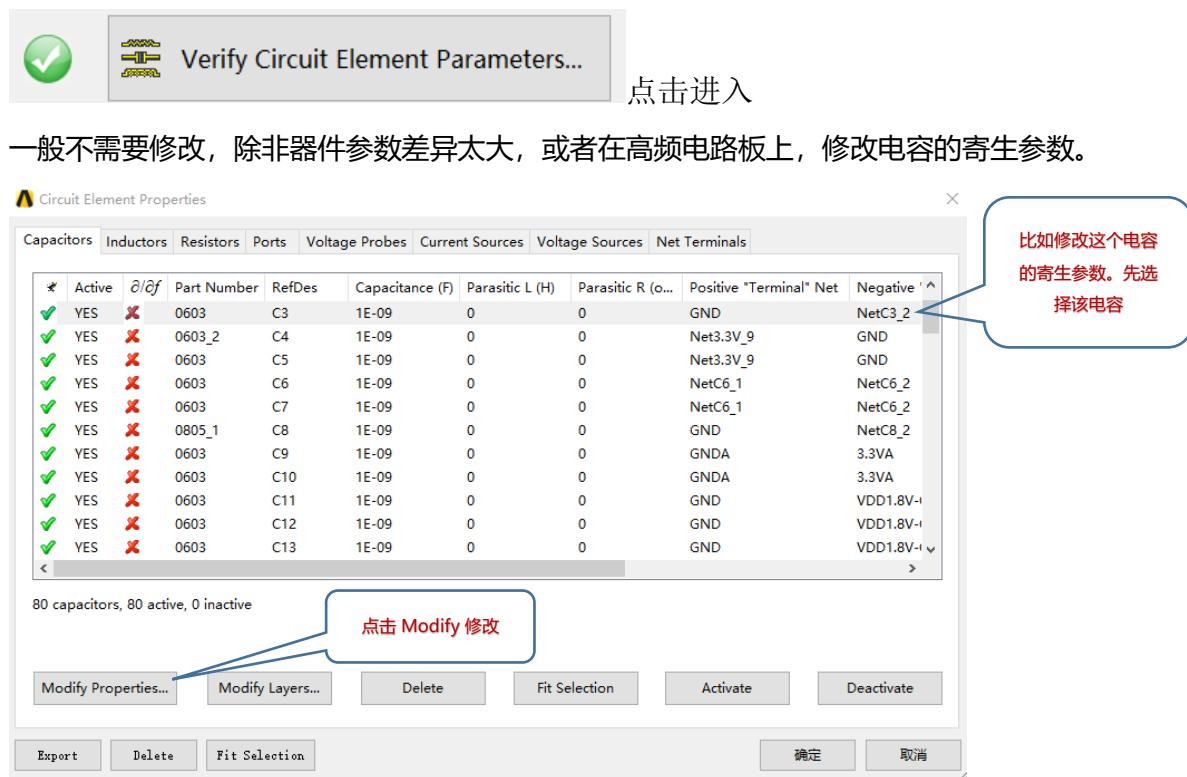
Pad Properties Shape: Circle Radius: 0.381 mm Height: 0.381 mm Update

Antipad Properties Shape: -None- Width: 0 mm Height: 0 mm Update

Thermal Relief Pad Properties Shape: -None- Width: 0 mm Height: 0 mm Update

一般 ODB++都已经把焊盘设置好了，所以我们一般不需要修改，点击 OK 就可以了。

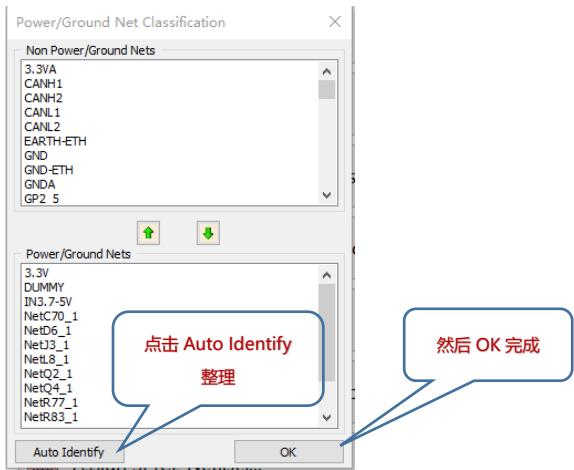
电路器件参数修改



设置识别电源与 GND 网络

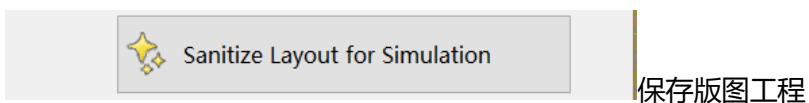


点击进入

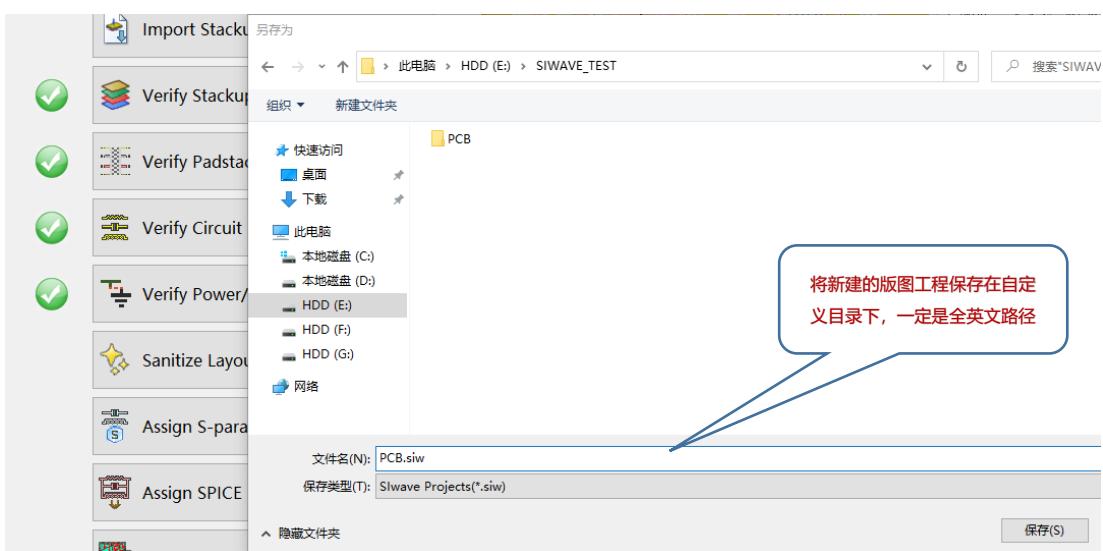


点击 Auto Identify
整理

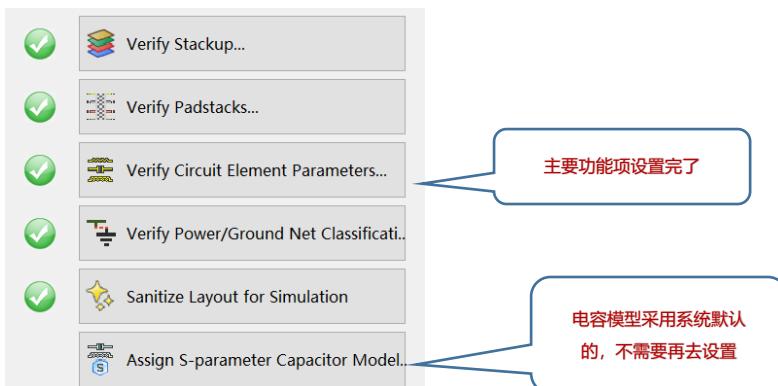
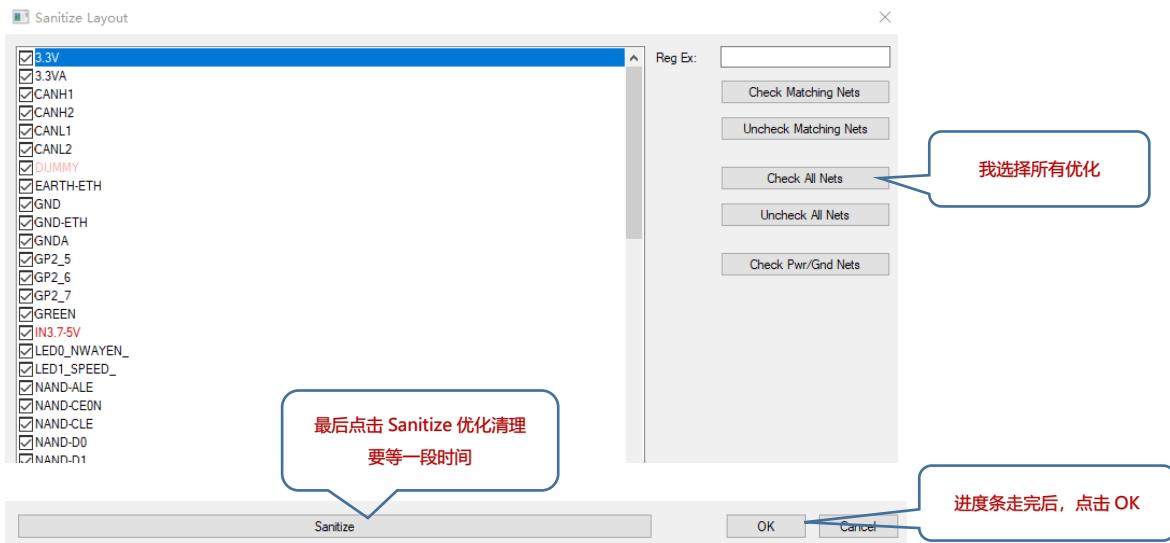
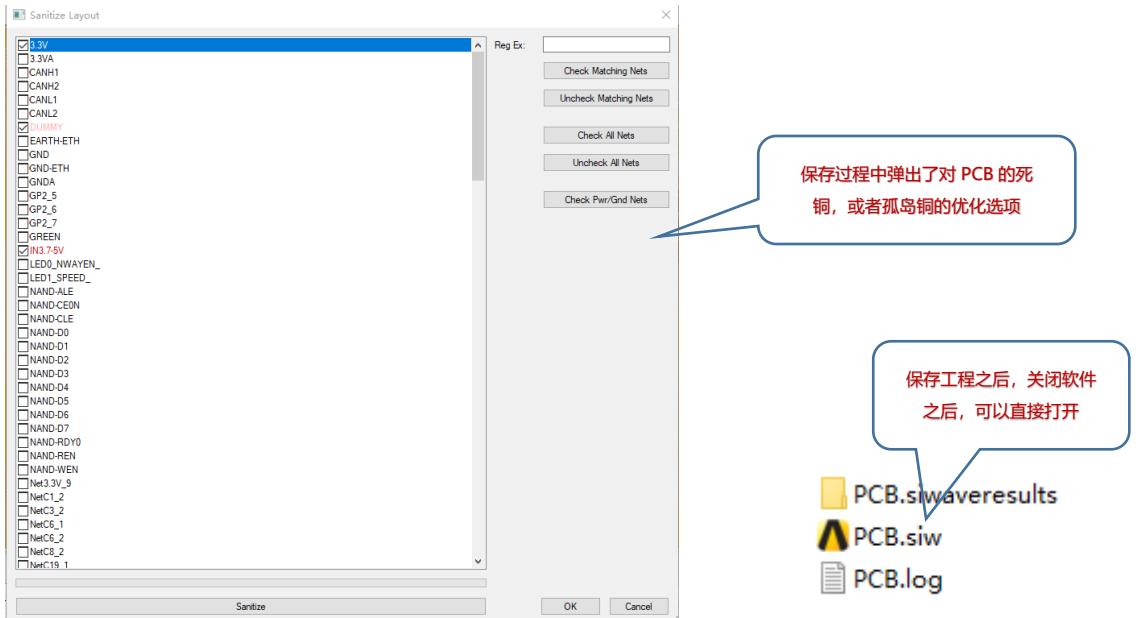
然后 OK 完成



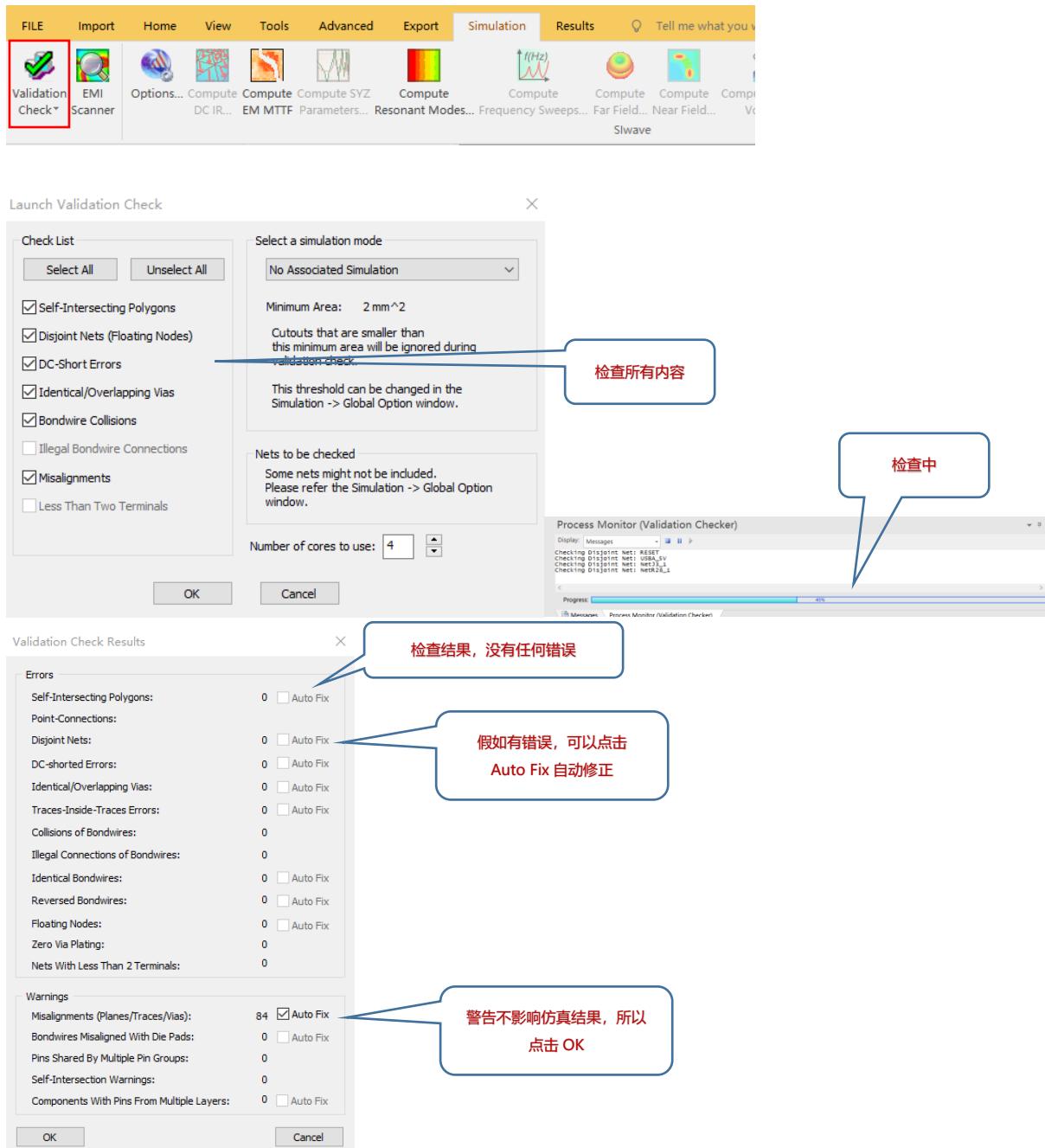
保存版图工程



将新建的版图工程保存在自定
义目录下，一定是全英文路径

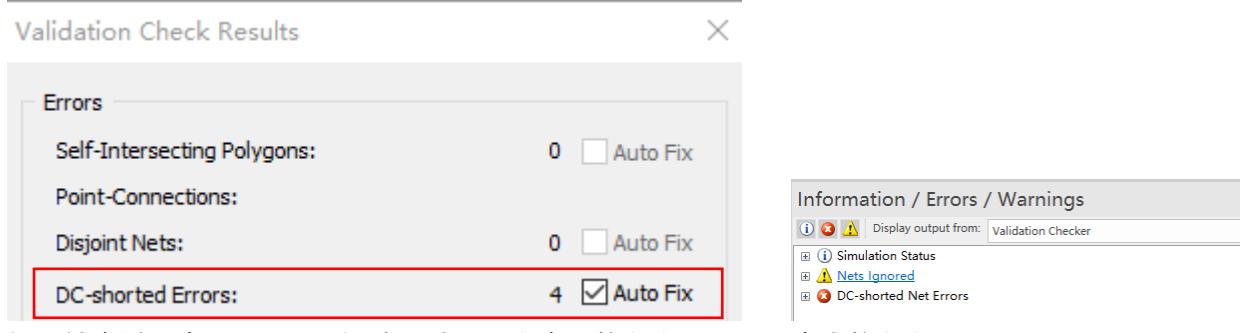


仿真前检查



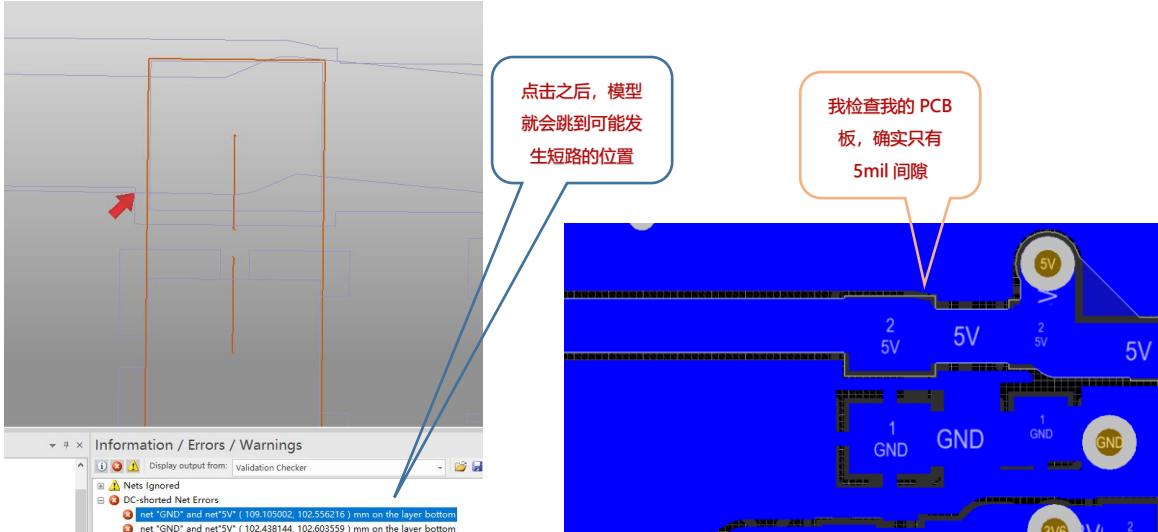
现在模型设置完成。

仿真前检查结果, 短路风险 (DC-shorted Errors)



如果检查过程中出现了 DC 短路风险, 那么查看信息窗口 DC 项

点击信息窗口 DC 项



这个就要看是自己调整还是板厂调整了。只能说模型给的形状不是黑规整。

现在将敷铜与电源的间距加宽到 10mil



敷铜问题解决了。

仿真前检查结果，分隔的敷铜问题(Self-Intersecting Polygons)

Validation Check Results

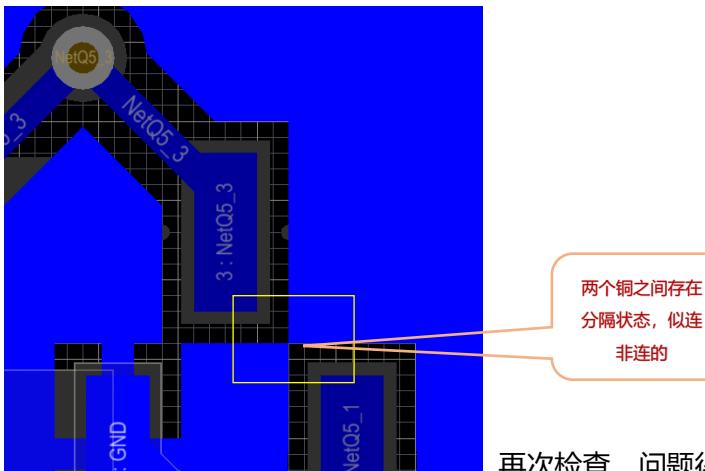
Information / Errors / Warnings

Errors

Self-Intersecting Polygons: 1 Auto Fix

Display output from: Validation Checker

- Simulation Status
- Nets Ignored
 - All geometry on net "DUMMY" will be ignored
- Misalignment Warnings
- Self Intersection Errors
 - net "GND" (119.634000, 103.632000) mm on layer bottom

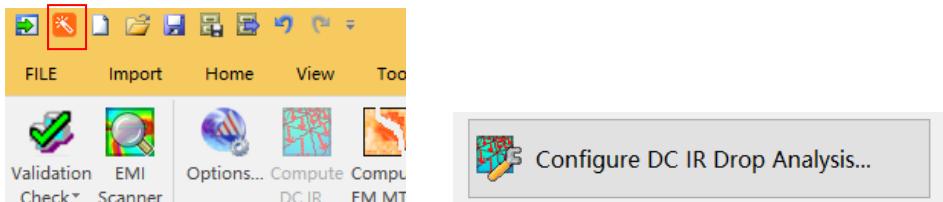


再次检查，问题得到解决。

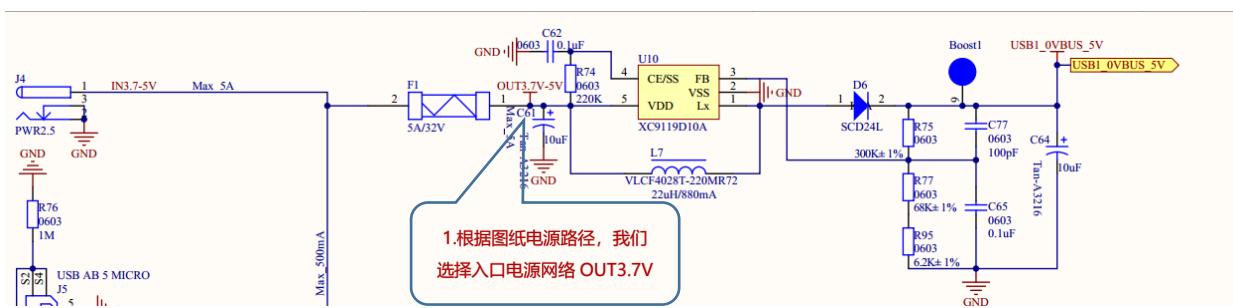
DC 直流压降和电流密度仿真

确保前面 PCB 板层叠设置完成。

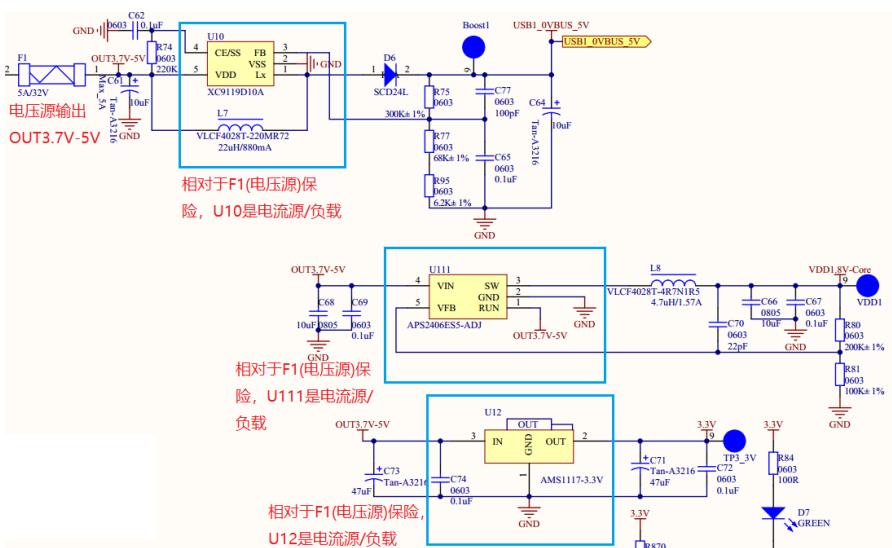
直流仿真主要是仿真每个芯片的电压降，和电流在 PCB 板区域大小。



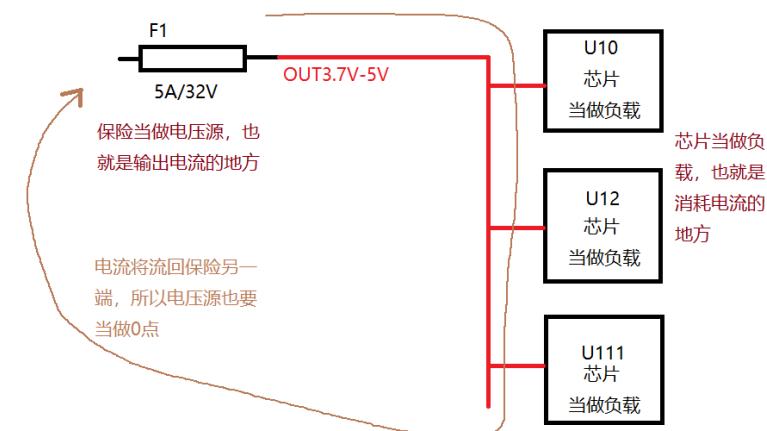
打开向导，选择 DC IR



1.根据图纸电源路径，我们
选择入口电源网络 OUT3.7V



简化图如下



DC IR Configuration

Ref. . .	Part Number	Positive Net	Reference Net	Source/Probe	Type	Magni...
D4	1N4001	OUT3.7V-5V	NetD4_2	None		
F1	5A/32V	OUT3.7V-5V	IN3.7-5V	None		
J100	HY-PH-2.0-4P	OUT3.7V-5V	GND	None		
J101	HY-PH-2.0-6P	OUT3.7V-5V	GND	None		
Q1	PMOS-IRLML6401	OUT3.7V-5V	NetQ1_1	None		
Q300	2SJ661	OUT3.7V-5V	NetJ3_1	None		
U8	TJA1050	OUT3.7V-5V	GND	None		
U10	XC9119D10A	OUT3.7V-5V	GND	None		
U12	AMS1117-3.3V	OUT3.7V-5V	GND	None		
U11	AFS2406ES5-ADJ	OUT3.7V-5V	GND	None		

Positive Net: Reference Net: Source/Probe: Type: Magnitude:

Load... Save... Source/Probe Naming Convention... Hide RLC component...

Configure Simulation → Validate... → Simulate...

2.选择 OUT3.7V-5V 入口电源

3.得到 OUT3.7V-5V 连接的电流消耗单元，一般是以芯片当做负载，所以这里把连接的芯片列出来也就是哪些器件会消耗我们的 OUT3.7V-5V 出来的电流

DC IR Configuration

Ref. . .	Part Number	Positive Net	Reference Net	Source/Probe	Type	Magni...
D4	1N4001	OUT3.7V-5V	NetD4_2	None		
F1	5A/32V	OUT3.7V-5V	IN3.7-5V	None		
J100	HY-PH-2.0-4P	OUT3.7V-5V	GND	None		
J101	HY-PH-2.0-6P	OUT3.7V-5V	GND	None		
Q1	PMOS-IRLML6401	OUT3.7V-5V	NetQ1_1	None		
Q300	2SJ661	OUT3.7V-5V	NetJ3_1	None		
U8	TJA1050	OUT3.7V-5V	GND	None		
U10	XC9119D10A	OUT3.7V-5V	GND	Current Source	Constant Vol...	1.0A
U12	AMS1117-3.3V	OUT3.7V-5V	GND	Current Source	Constant Vol...	1.0A
U11	AFS2406ES5-ADJ	OUT3.7V-5V	GND	Current Source	Constant Vol...	1.0A

Positive Net: Reference Net: Source/Probe: Type: Magnitude:

Load... Save... Source/Probe Naming Convention... Hide RLC component...

Configure Simulation → Validate... → Simulate...

设置 U10,U12,U11 为 5V 电源的负载，每个芯片消耗电流 1A

4.除了设置芯片为负载电流消耗点以外，还必须设置电压源，也就是输出端。

DC IR Configuration

Ref. . .	Part Number	Positive Net	Reference Net	Source/Probe	Type	Magni...
D4	1N4001	OUT3.7V-5V	NetD4_2	None		
F1	5A/32V	OUT3.7V-5V	IN3.7-5V	Voltage Source	5V	
J100	HY-PH-2.0-4P	OUT3.7V-5V	GND	None		
J101	HY-PH-2.0-6P	OUT3.7V-5V	GND	None		
Q1	PMOS-IRLML6401	OUT3.7V-5V	NetQ1_1	None		
Q300	2SJ661	OUT3.7V-5V	NetJ3_1	None		
U8	TJA1050	OUT3.7V-5V	GND	None		
U10	XC9119D10A	OUT3.7V-5V	GND	Current Source	Constant Vol...	1A
U12	AMS1117-3.3V	OUT3.7V-5V	GND	Current Source	Constant Vol...	1A
U11	AFS2406ES5-ADJ	OUT3.7V-5V	GND	Current Source	Constant Vol...	1A

Positive Net: Reference Net: Source/Probe: Type: Magnitude:

Load... Save... Source/Probe Naming Convention... Hide RLC component...

Configure Simulation → Validate... → Simulate...

5.设置保险为电压源，也就是输出电流端，电源也为 0 点输出 5V 电压

DC IR Configuration

Ref. . .	Part Number	Positive Net	Reference Net	Source/Probe	Type	Magni...
D4	1N4001	OUT3.7V-5V	NetD4_2	None		
F1	5A/32V	OUT3.7V-5V	IN3.7-5V	Voltage Source	5V	
J100	HY-PH-2.0-4P	OUT3.7V-5V	GND	None		
J101	HY-PH-2.0-6P	OUT3.7V-5V	GND	None		
Q1	PMOS-IRLML6401	OUT3.7V-5V	NetQ1_1	None		
Q300	2SJ661	OUT3.7V-5V	NetJ3_1	None		
U8	TJA1050	OUT3.7V-5V	GND	None		
U10	XC9119D10A	OUT3.7V-5V	GND	Current Source	Constant Vol...	1A
U12	AMS1117-3.3V	OUT3.7V-5V	GND	Current Source	Constant Vol...	1A
U11	AFS2406ES5-ADJ	OUT3.7V-5V	GND	Current Source	Constant Vol...	1A

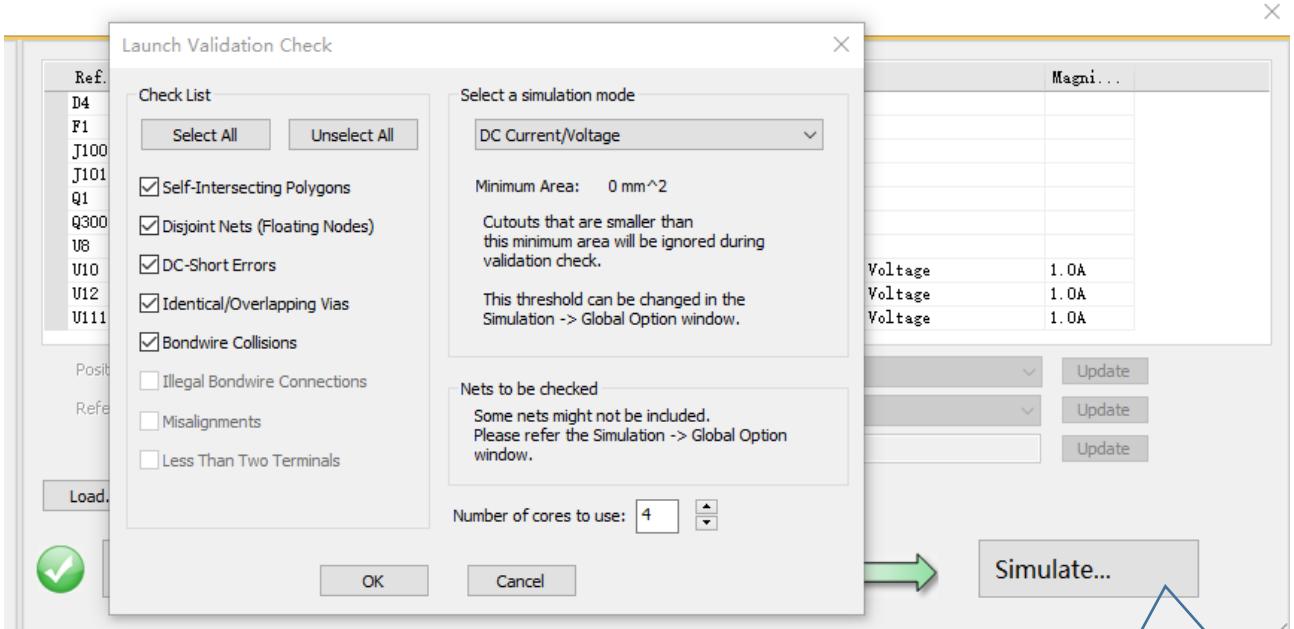
Positive Net: Reference Net: Source/Probe: Type: Magnitude:

Load... Save... Source/Probe Naming Convention... Hide RLC component...

Configure Simulation → Validate... → Simulate...

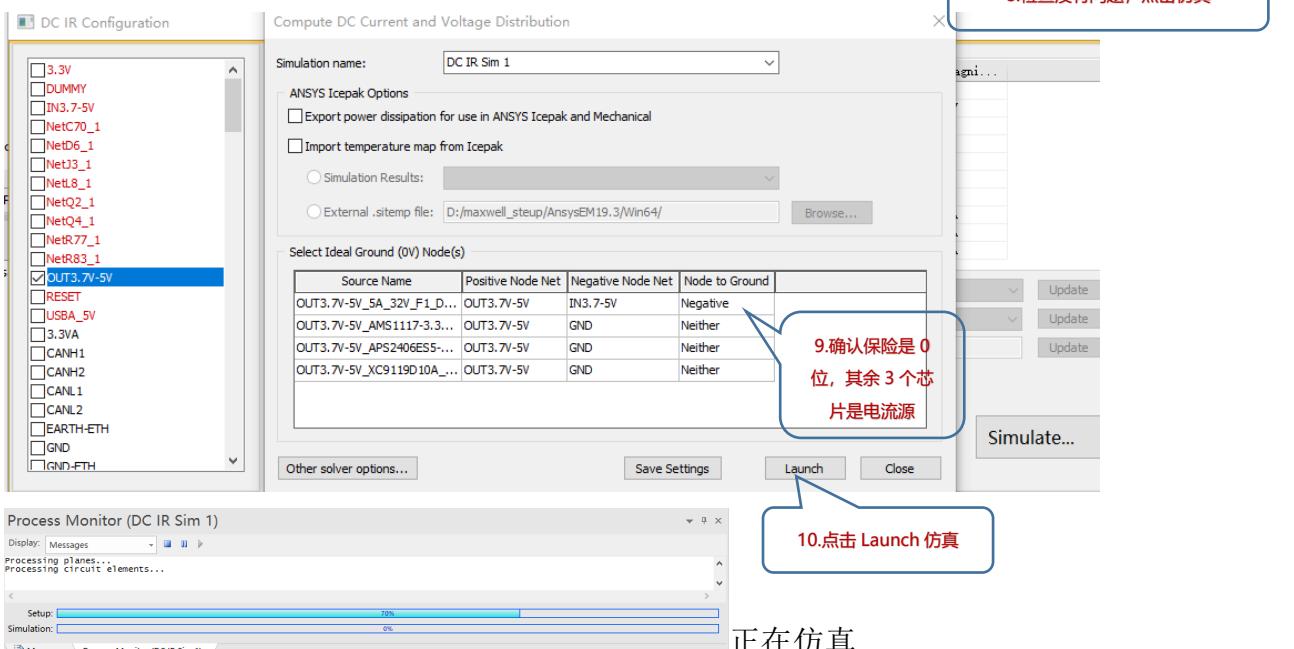
6.点击配置

7.点击检查，再检查一遍



Simulate...

8. 检查没有问题，点击仿真



Simulate...

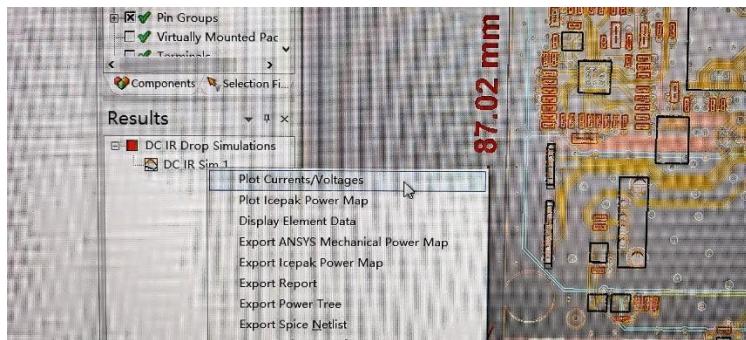
10. 点击 Launch 仿真

正在仿真

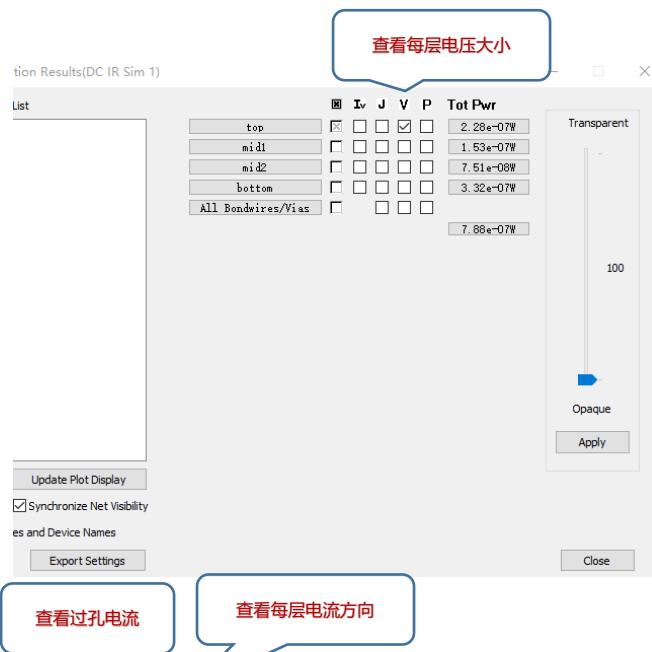


如果想在主界面看见 Results 框框，记住 Results 在 View->WorkSpaces->Results 打开

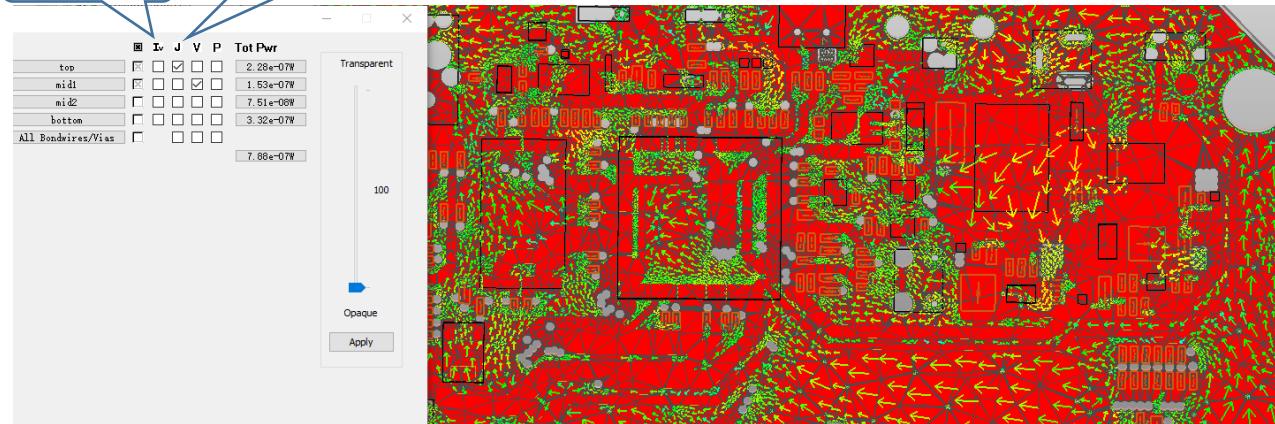
查看直流电压电流分布图(云图)



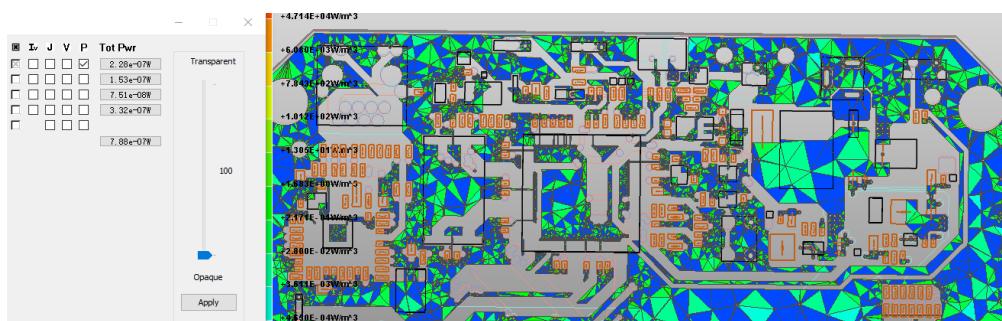
生成报告



查看每层电压大小

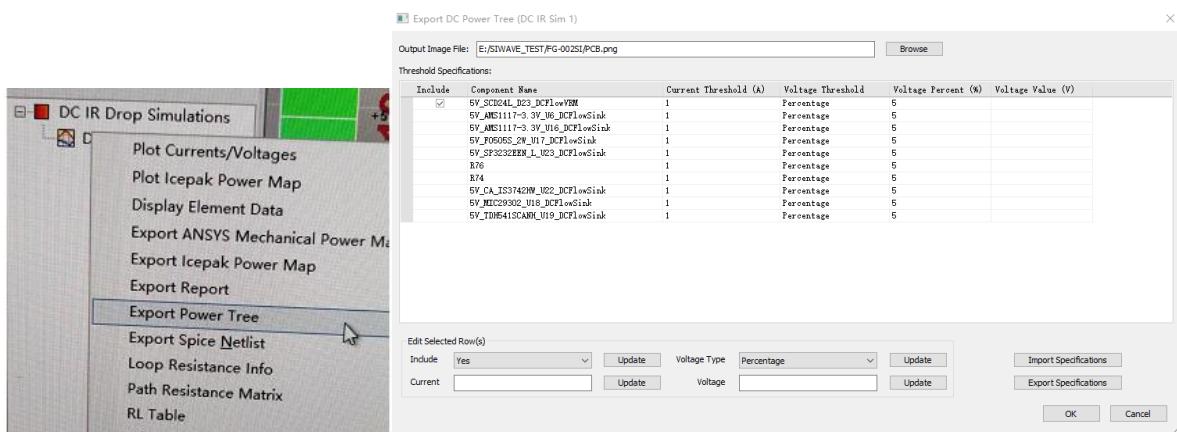


查看每层电流方向



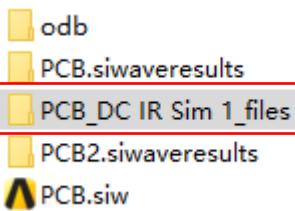
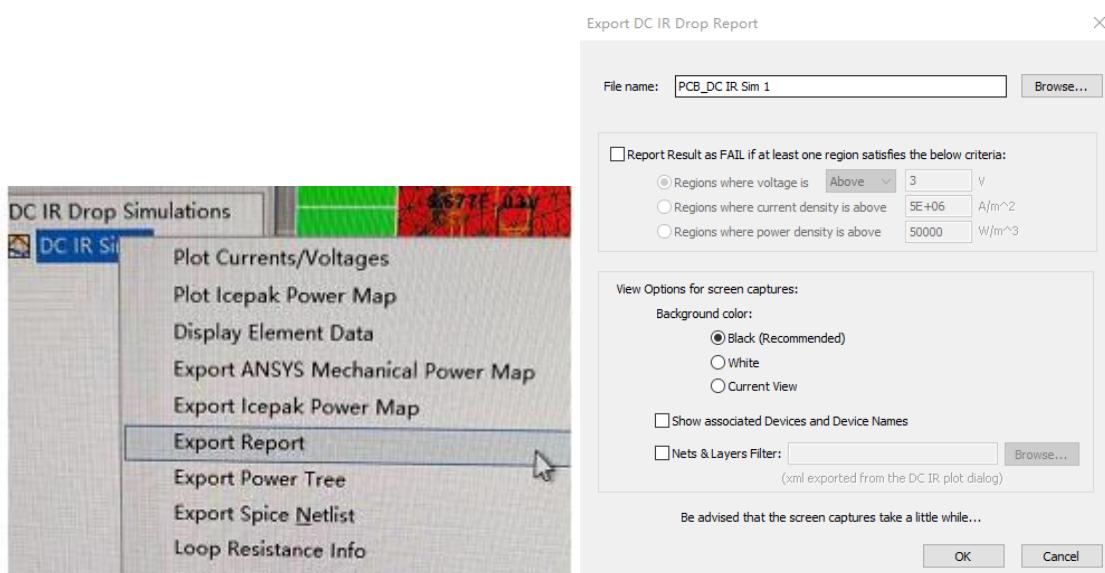
查看每层功耗

生成电流流向框图

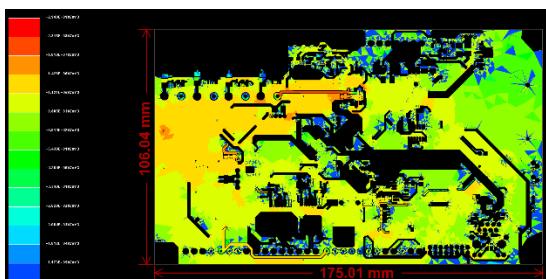


这是要生成的框图元件，点击 OK 就会生成框图和图片，图片存放在当前目录下。

生成报告，包含所有的电压电流云图，和数据表

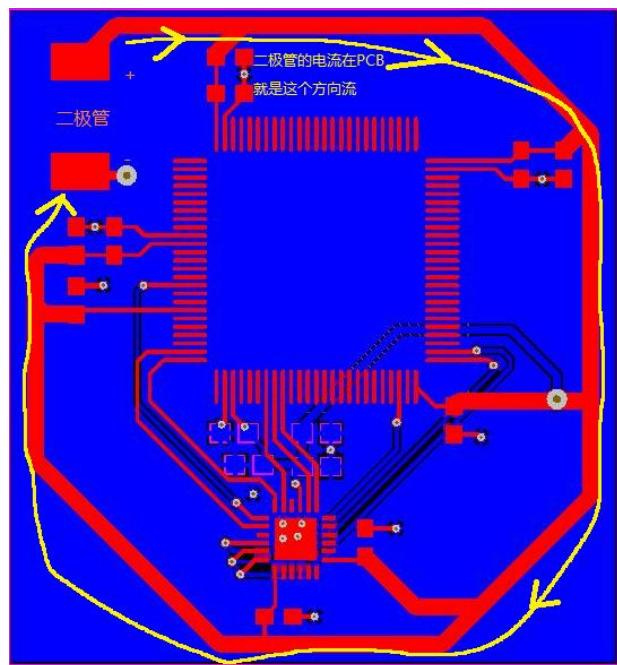
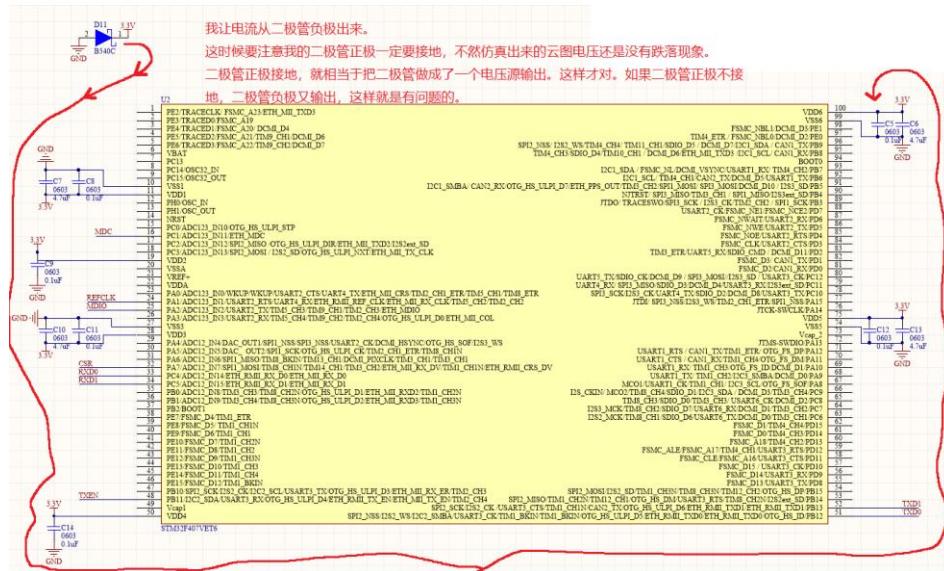


生成的报告是图片格式的，存放在你自己取名字的目录下。



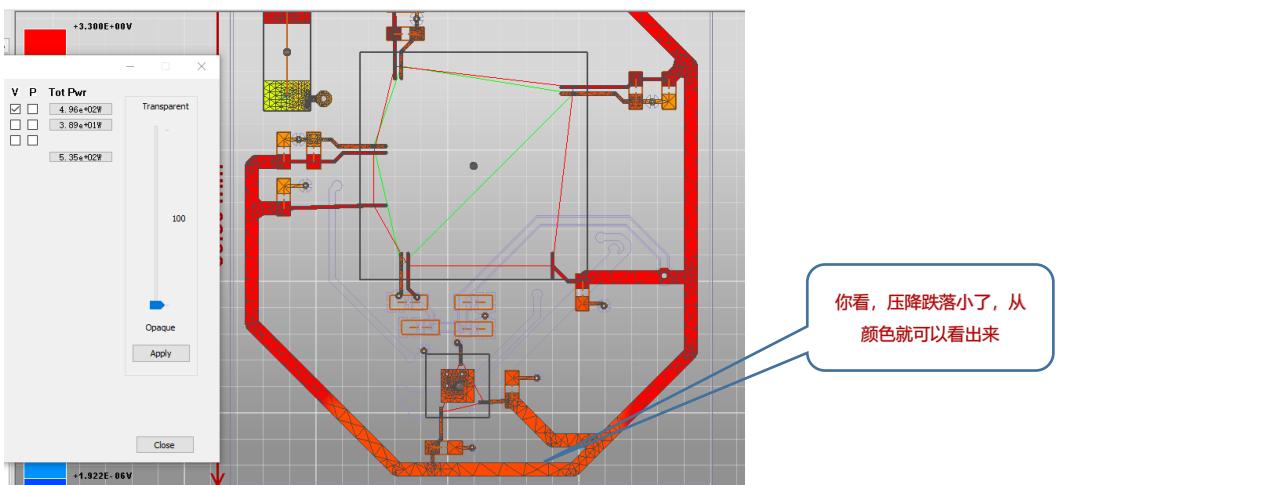
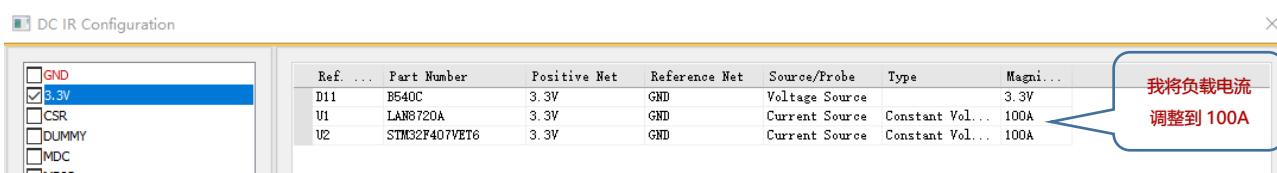
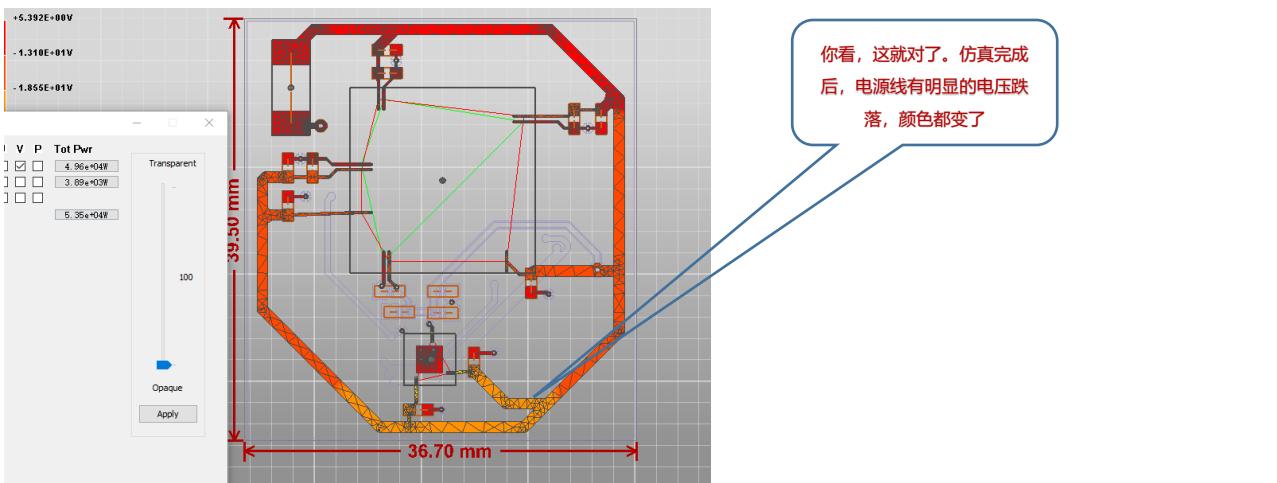
更详细的云图也是在报告里面。

在直流压降分析的环节，我们发现双面板不管是顶层还是底层，云图的电压选项都没有电压跌落的情况。所以我准备用一个简单的电路来做下仿真。



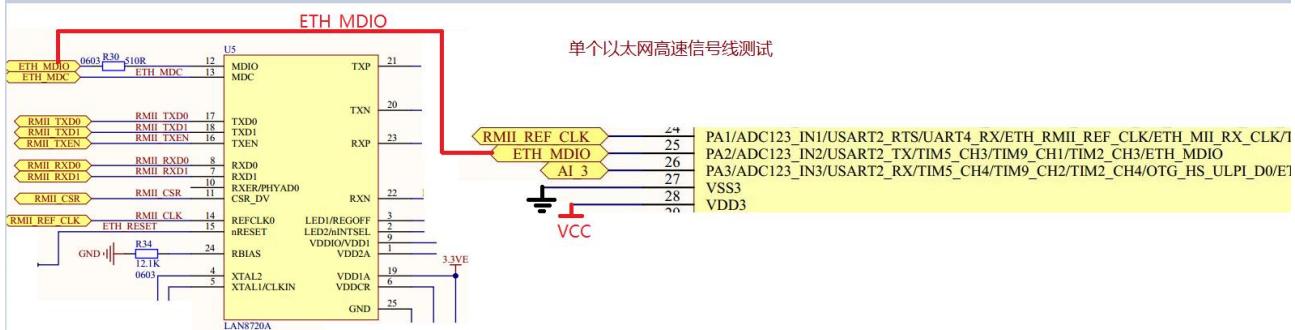
我们按照前面的仿真步骤仿真，只是有几步要注意



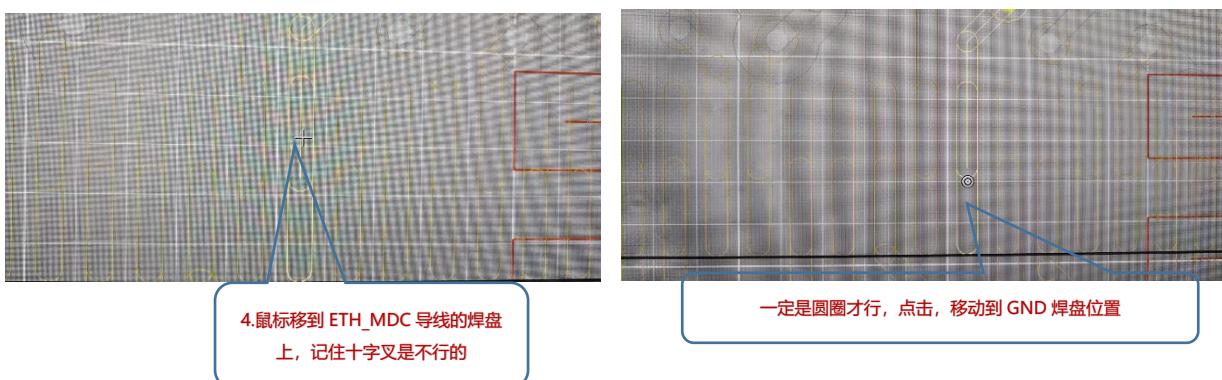
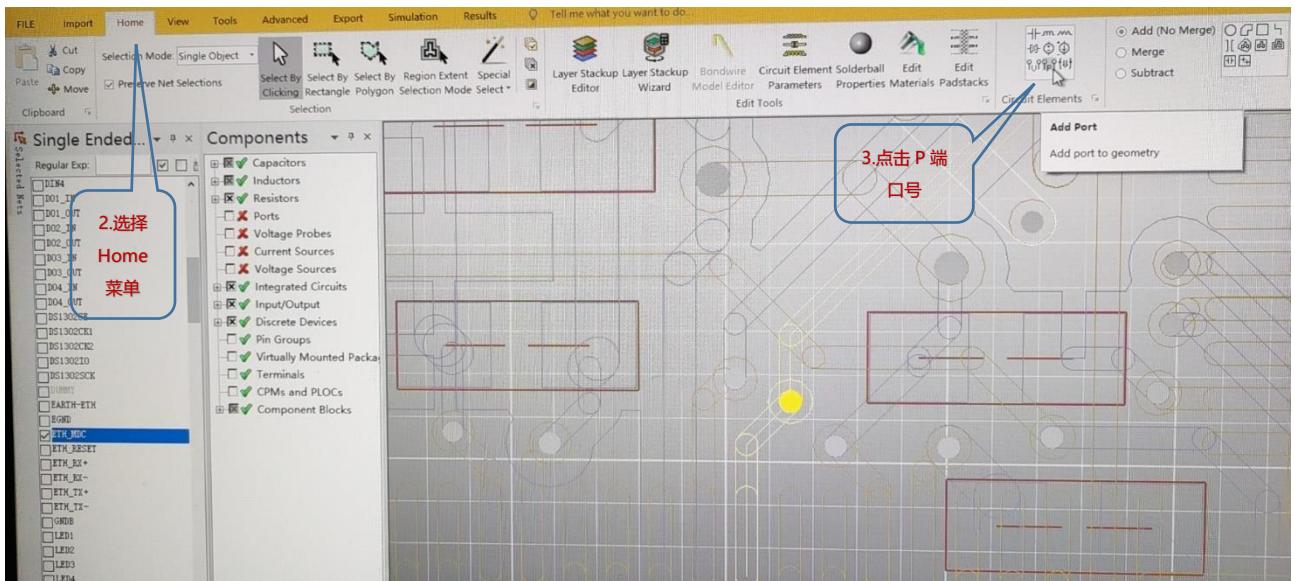
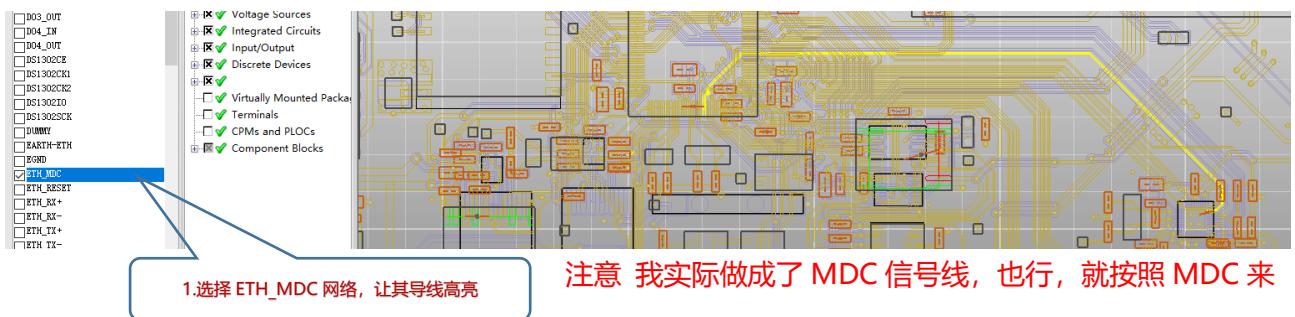


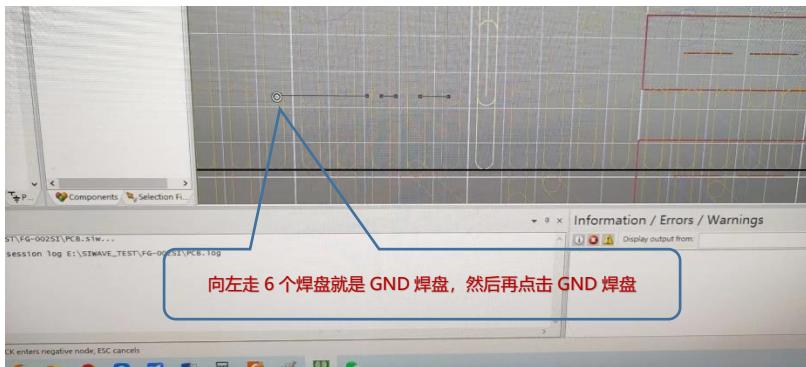
这才是 DC IR Drop 正确的仿真方式，设置输出电压源的时候一定要有接地端。

PCB 的 SYZ 参数提取



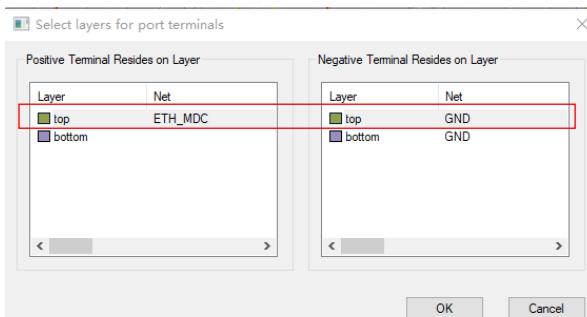
我们用以太网传输线为案例，来做 phy 桥连接信号测试，现在测单根线。



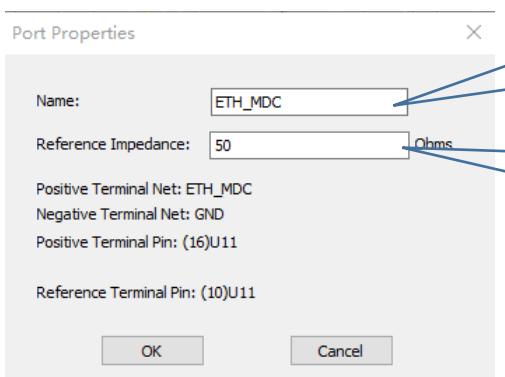
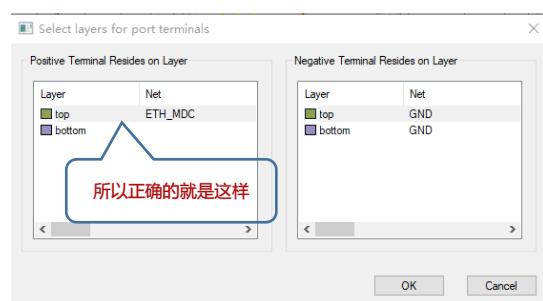
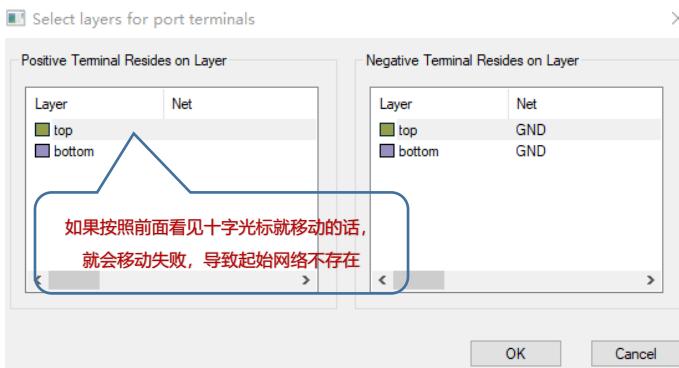


有些 GND 焊盘不在这个方向，看自己

实际情况而决定移到方向。

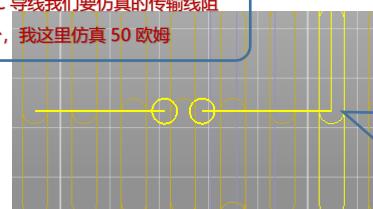


反正点击成功后会显示起始网络 ETH_MDC 和 GND

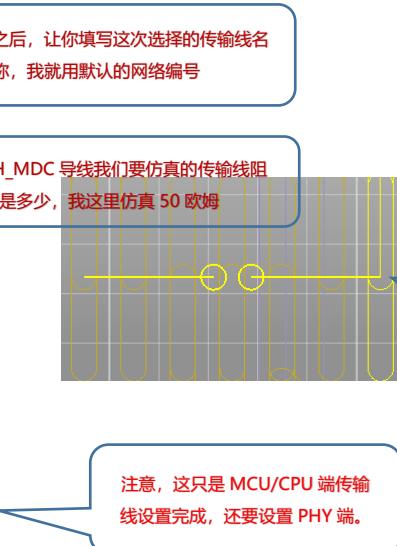
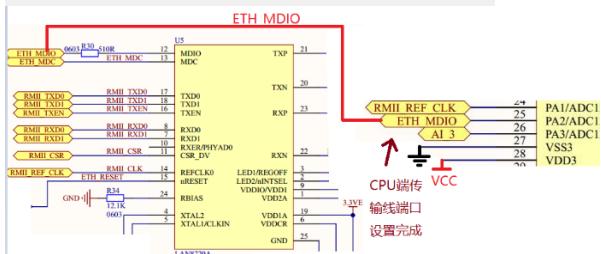


点击 OK 之后, 让你填写这次选择的传输线名称, 我就用默认的网络编号

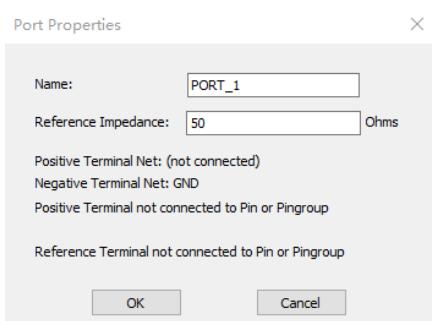
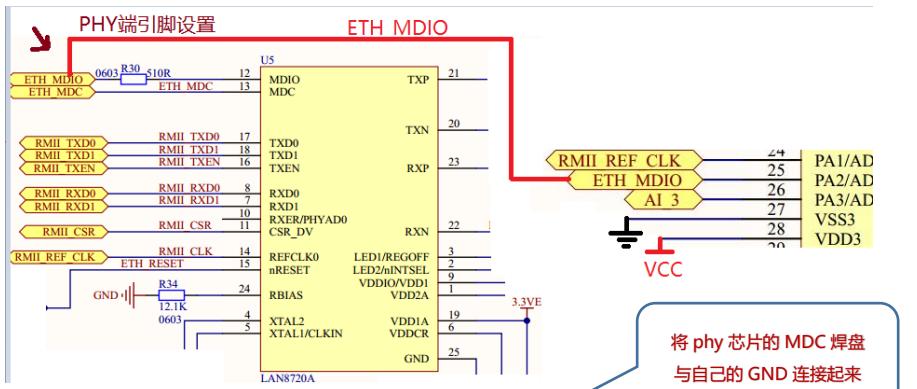
这条 ETH_MDC 导线我们要仿真的传输线阻抗是多少, 我这里仿真 50 欧姆



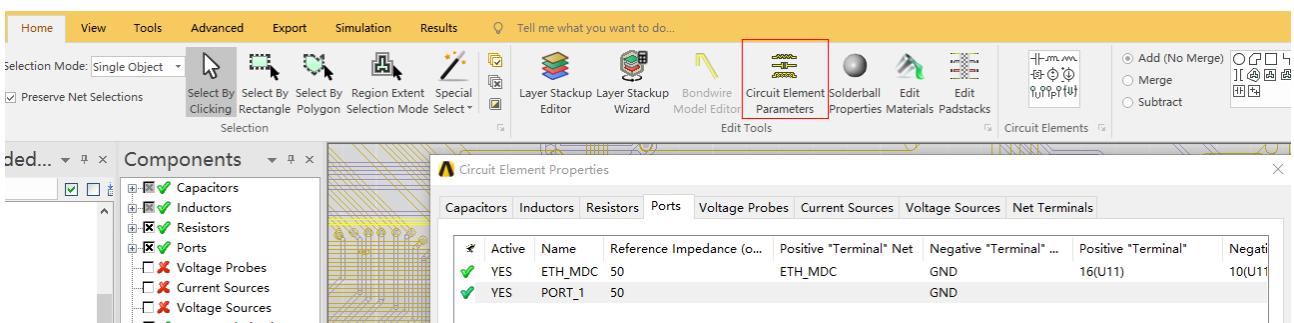
端口选择成功后,
会出现这种图形,
表示 MDC 线和
GND 焊盘的间距



注意, 这只是 MCU/CPU 端传输
线设置完成, 还要设置 PHY 端。

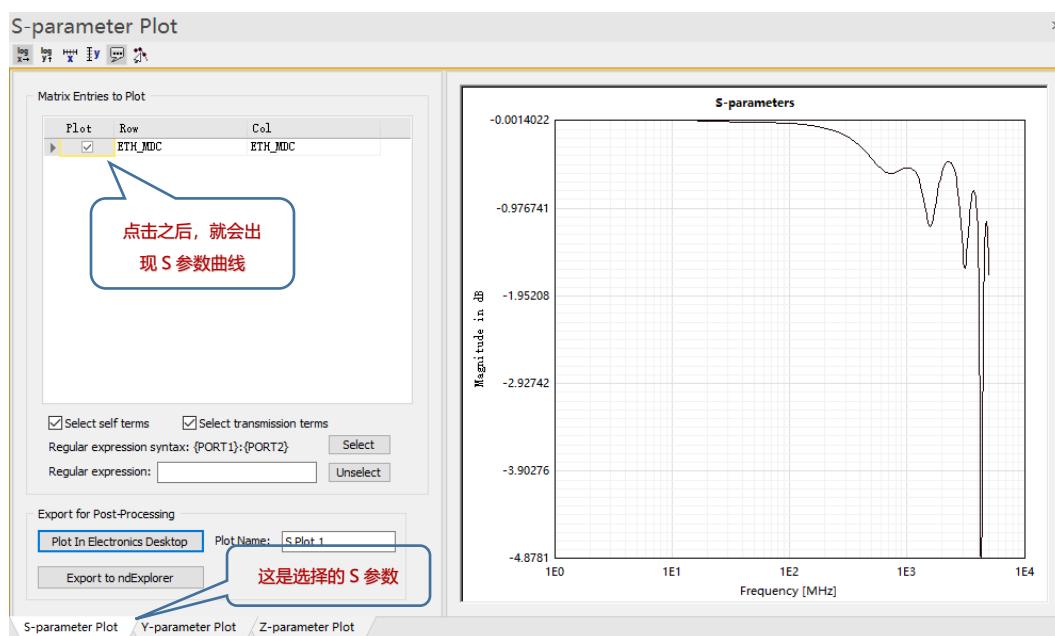
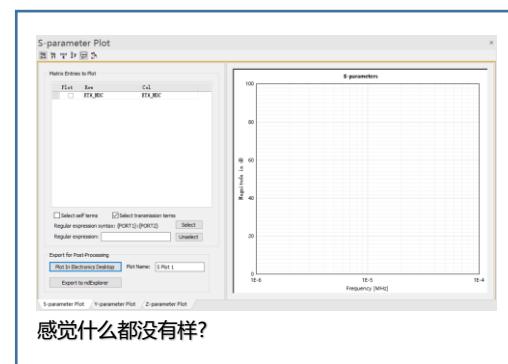
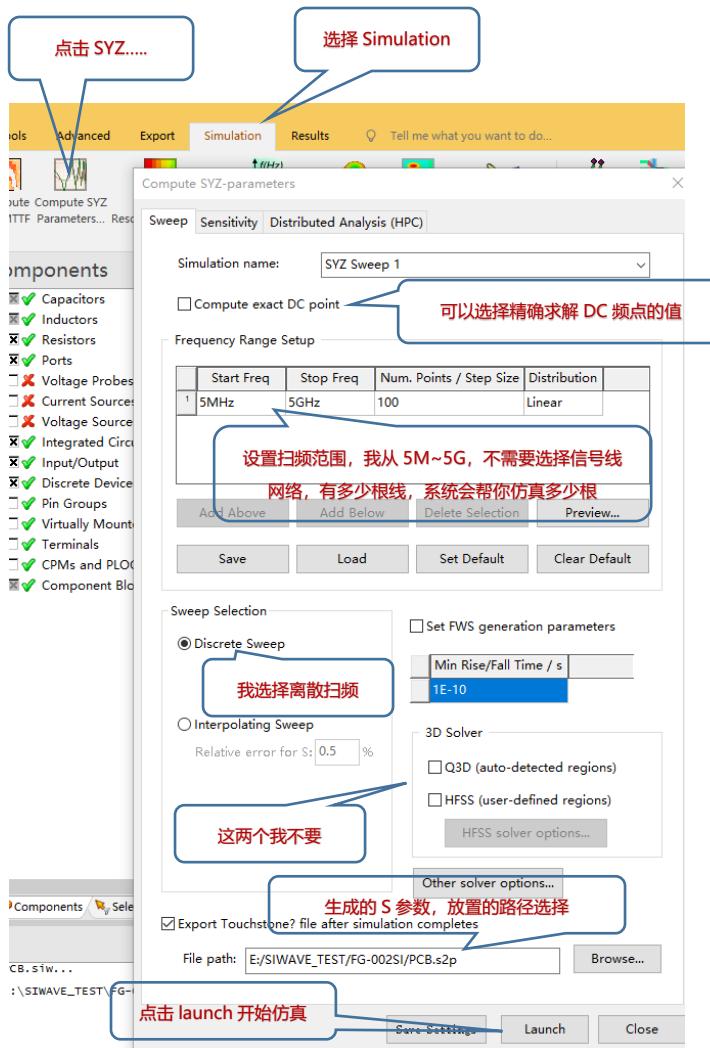


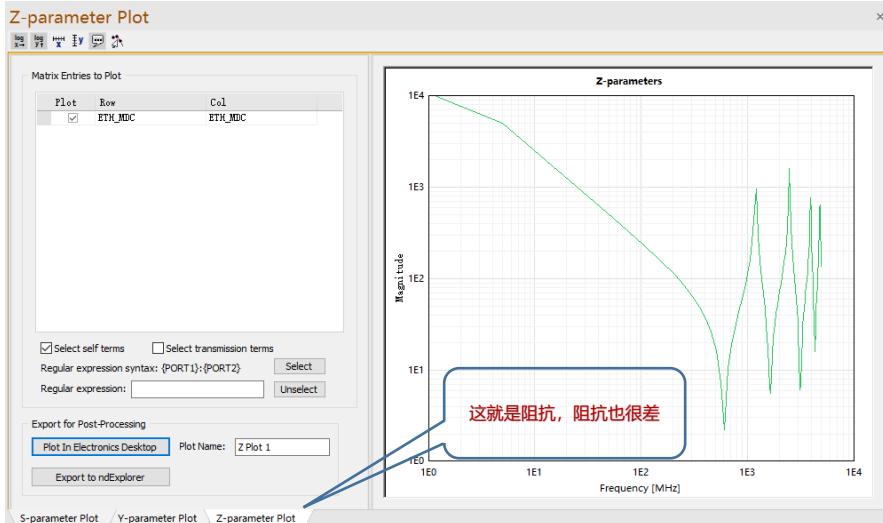
一样的选择 50 欧姆。现在这条 ETH_MDC 网络设置完成了。



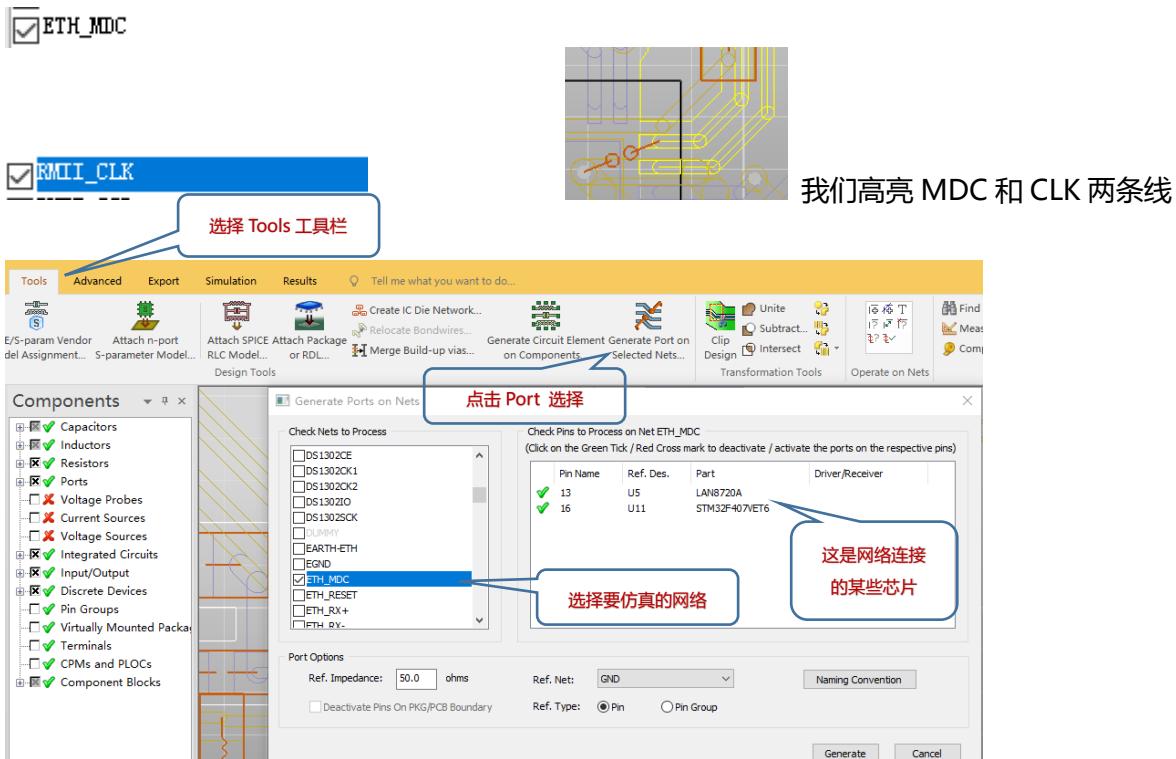
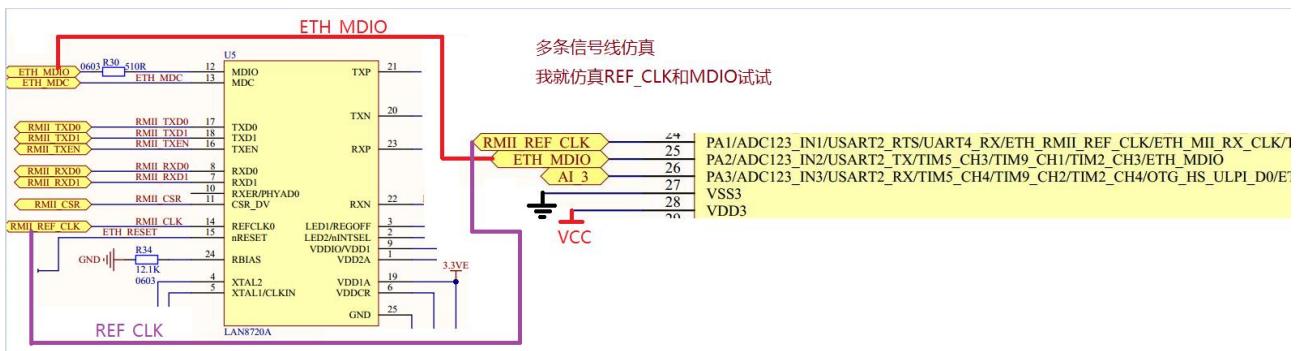
在 Home->下的 Circuit Element Parameters 里面可以看到你添加的传输线。

SYZ 参数仿真(主要看插入损耗，回波损耗曲线)





多条信号线 SYZ 参数仿真



Generate Ports on Nets

Check Nets to Process

- PE14
- PE15
- RMII_CLK
- RMII_CSR
- RMII_RXD0
- RMII_RXD1
- RMII_TXD0
- RMII_TXD1
- RMII_TXEN

Check Pins to Process on Net ETH_MDC
(Click on the Green Tick / Red Cross mark to deactivate / activate the port)

Pin Name	Ref. Des.	Part	Driver/Receiver
13	U5	LAN8720A	
16	U11	STM32F407VET6	

绿色的勾表示自动帮我们在引脚上建立端口

Generate Ports on Nets

Check Nets to Process

- PE14
- PE15
- RMII_CLK
- RMII_CSR
- RMII_RXD0
- RMII_RXD1
- RMII_TXD0
- RMII_TXD1
- RMII_TXEN

Check Pins to Process on Net ETH_MDC
(Click on the Green Tick / Red Cross mark to deactivate / activate the ports on the respective pins)

Pin Name	Ref. Des.	Part	Driver/Receiver
13	U5	LAN8720A	
16	U11	STM32F407VET6	

加入你不想要建立某个引脚的端口，在勾上点击，变成 x
就可以了

Generate Ports on Nets

Check Nets to Process

- NetU11_86
- NetU11_87
- NetU11_88
- PB0
- PB1
- PC13_KEY1
- PE13_KEY2
- PE5
- PE6
- PE14
- PE15
- RMII_CLK

Port Options

Ref. Impedance: 50.0 ohms Ref. Net: GND Naming Convention

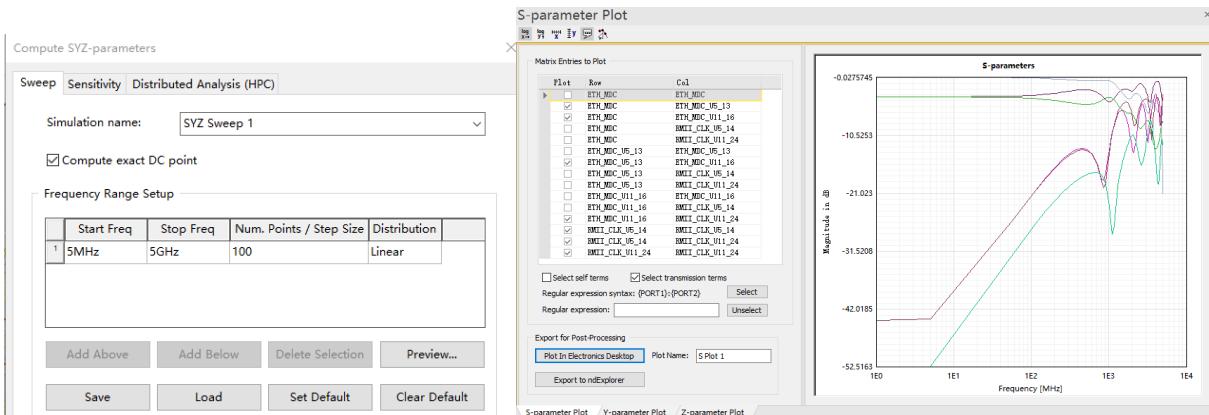
Ref. Type: Pin Pin Group

Deactivate Pins On PKG/PCB Boundary

设置端口阻抗 设置端口参考的网络 点击，创建端口

自动创建两个端口，有个端口是以前手动创建的，所以没有消除，就成了三个端口

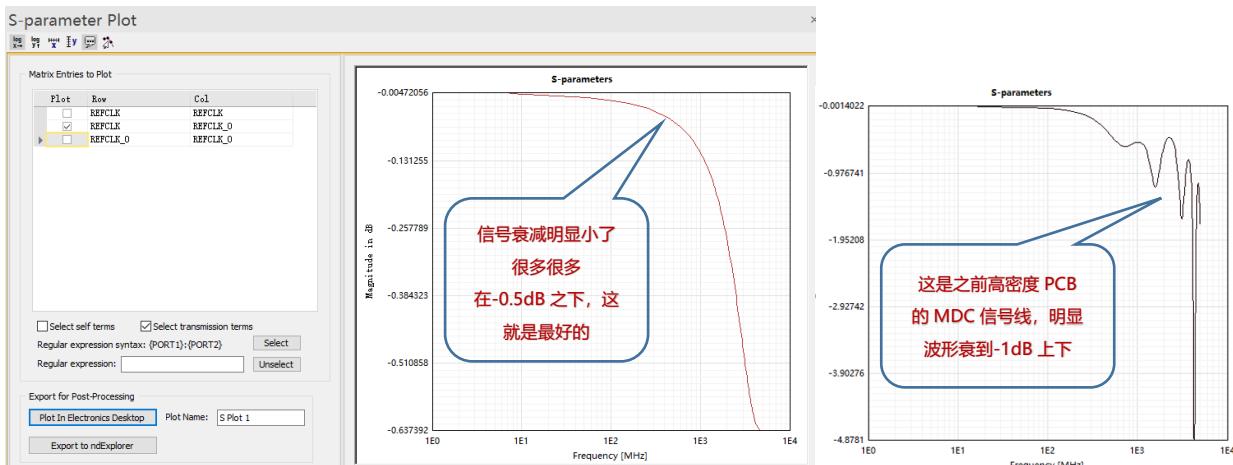
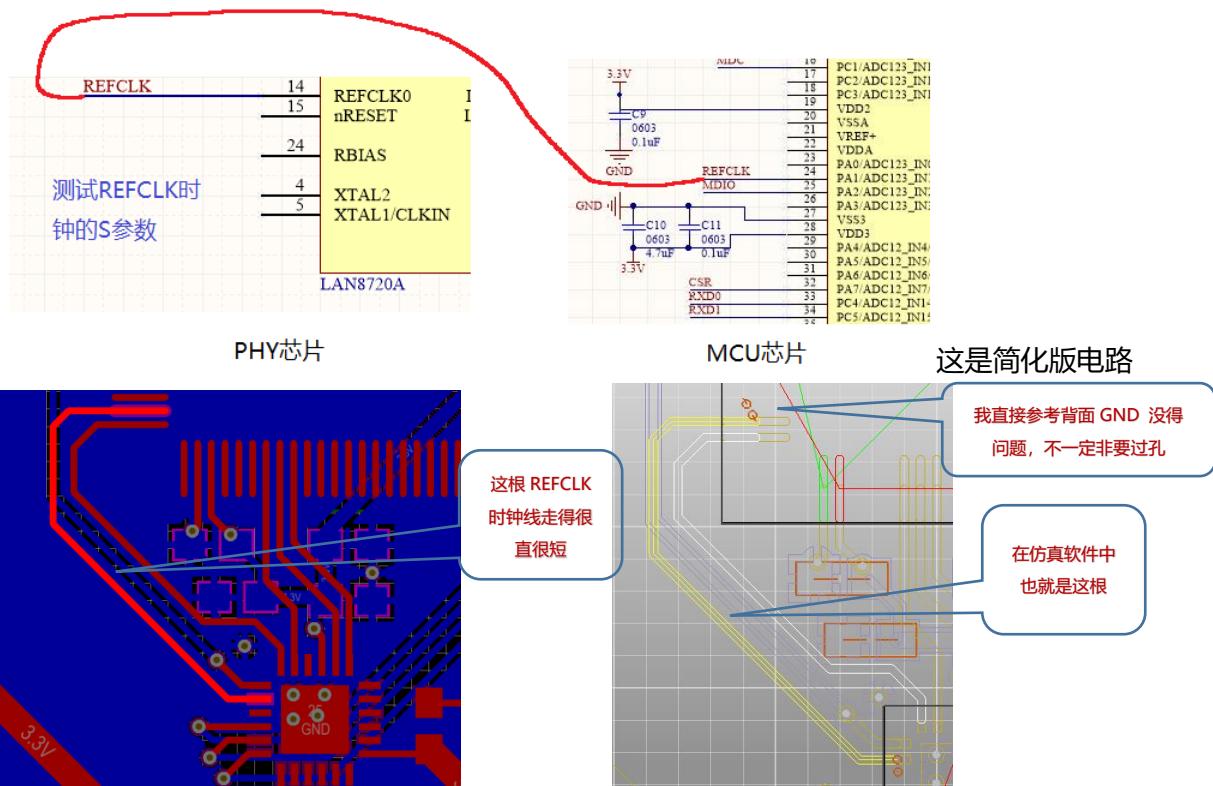
选择 SYZ 参数，按照之前的步骤，直接仿真。



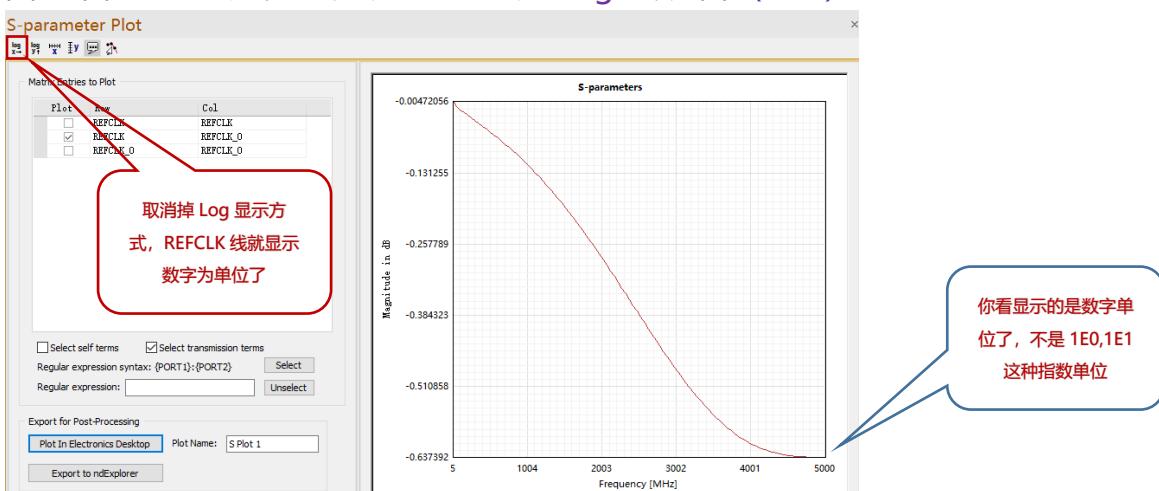
这就是多个网络的仿真结果。

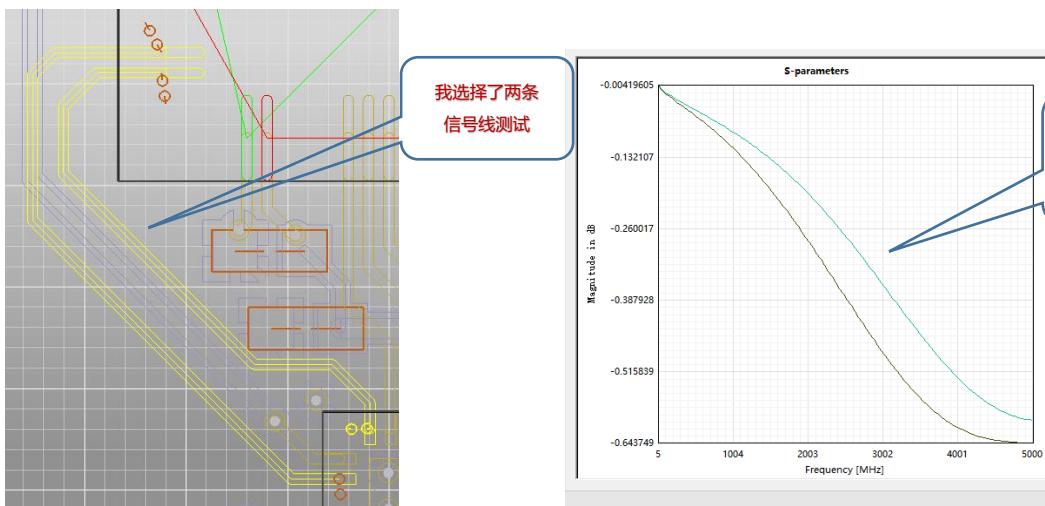
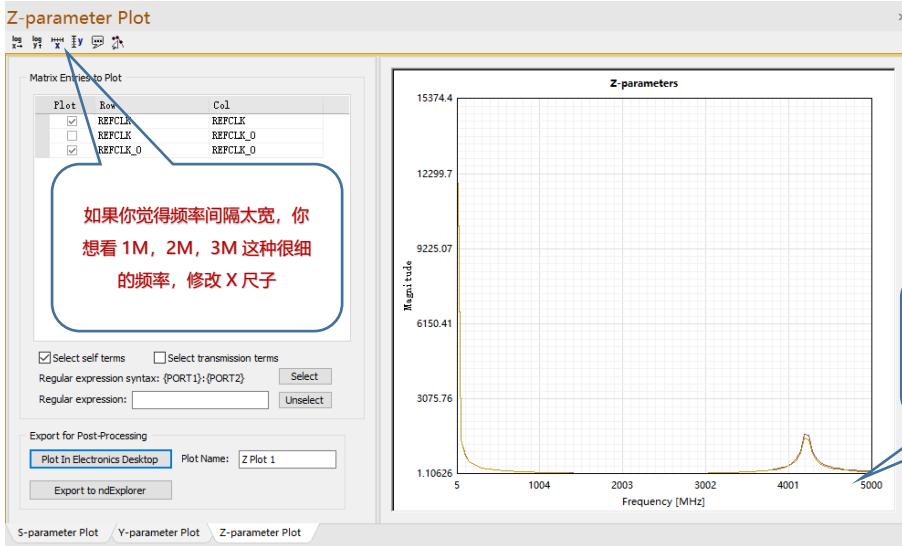
从以上仿真的结果来看，信号线的 S 参数和 Z 参数都不是很理想。S 参数和 Z 参数的定义，请查阅我的《HIG_SPEED_EE_Designer》文档 S 参数章节。

下面用简化版的 PCB 来测试下仿真，看看能否优化。



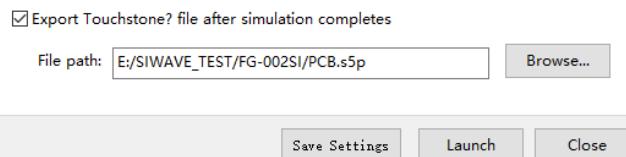
曲线单位显示问题，系统默认显示的是 Log 指数单位(重点)





S 参数和 Z 参数的定义, 请查阅我的《HIG_SPEED_EE_Designer》文档 S 参数章节。

SI 信号完整性仿真

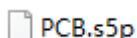


Save Settings

Launch

Close

确认我在前面章节提取 SYZ 参数时，生成的参数模型位置。



在当前工程目录下确实有这个模型。这个模型可以给其它软件用。至于我后面要用的 SIWAVE，是不需要手动导入 s5p 文件的，软件会自动导入。

选择 Siwizard....

PCB.siw - Slwave

Simulation Results Tell me what you want to do...

Mode... Frequency Sweeps... Far Field... Near Field... Compute Induced Voltage...

Slwave

Signal Net Analyzer Scan... NEXT/NEXT Crosstalk Scan... TDRwizard...

Compute RLGC... CPA Options... Compute AC Currents... Par PSI

Slwizard Step 1: Select Nets to Analyze

Single-Ended Differential Extended Extended Differential

Nets in Design:

- DO4_OUT
- DS1302CE
- DS1302CK1
- DS1302CK2
- DS1302IO
- DS1302SCK
- EARTH-ETH
- EGND
- ETH_MDC**
- ETH_RESET
- ETH_RX+
- ETH_RX-
- ETU_TV_1

Nets to Analyze:

Add >>

PE6

- RMII_CLK**
- RMII_CSR
- RMII_RXD0
- RMII_RXD1

< < Remove

然后点击 Next

Slwizard Step 2: Assign Driver and Receiver Models

Port	Pin	Expose	Part Number	Ref. . . .	Type	Corner	IBIS Component	Model Selector	IBIS Model	Excitation Source	PKG IC's
ETH_MDC	13	<input checked="" type="checkbox"/>	LANS720A	05	Receiver	Typical	-None-	-None-	-None-	<input checked="" type="checkbox"/>	
RMII_CLK	14	<input checked="" type="checkbox"/>	LANS720A	05	Receiver	Typical	-None-	-None-	-None-	<input checked="" type="checkbox"/>	
ETH_MDC	16	<input checked="" type="checkbox"/>	STM32F407VET6	U11	Receiver	Typical	-None-	-None-	-None-	<input checked="" type="checkbox"/>	
RMII_CLK	24	<input checked="" type="checkbox"/>	STM32F407VET6	U11	Receiver	Typical	-None-	-None-	-None-	<input checked="" type="checkbox"/>	

Operations

Expose pins in schematic? No Update

Change pin type to Driver (Active) Update

Change pin buffer corner to Typical Update

Include PKG RLCs for pins? No Update

Buffer Assignment

IBIS Component: -None- Update

IBIS Model Selector: -None- Manage Sources

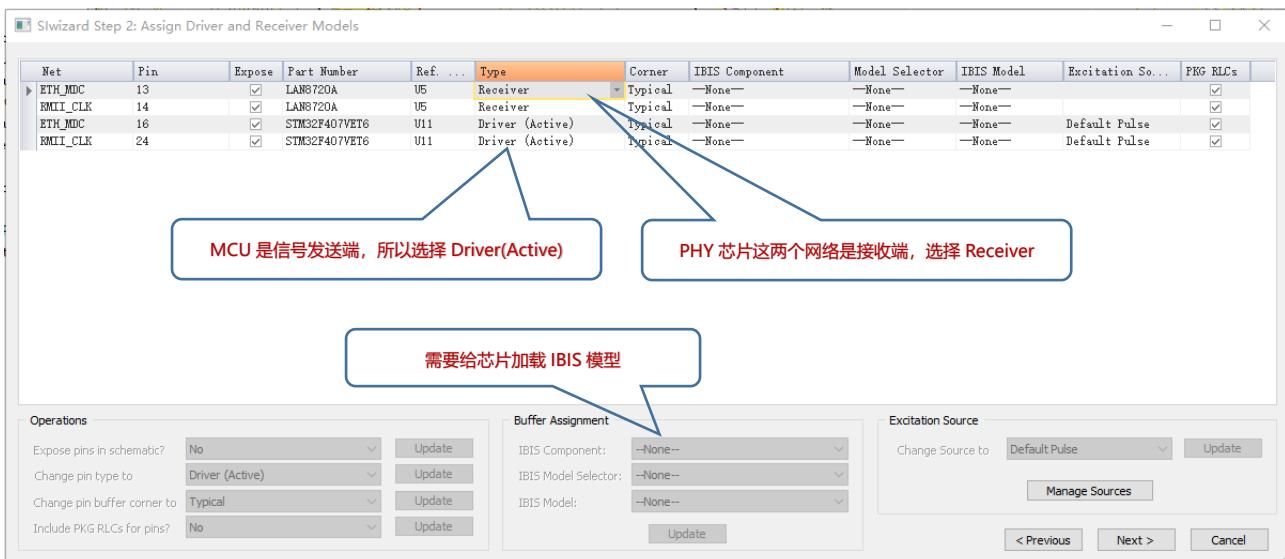
IBIS Model: -None- Update

Excitation Source

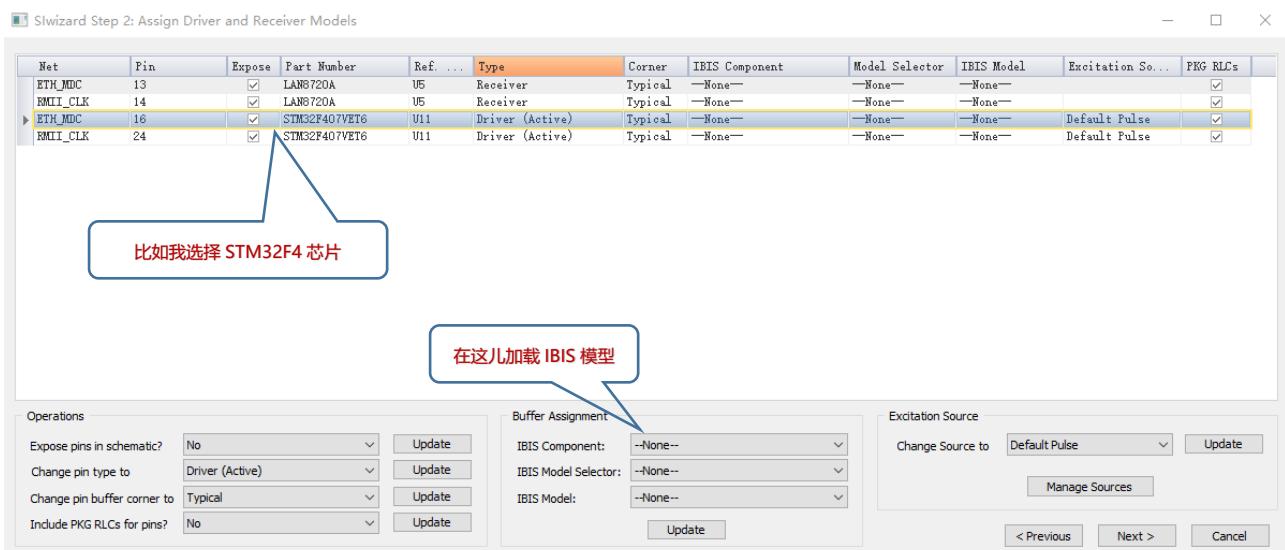
Change Source to Default Pulse Update

Manage Sources

< Previous Next > Cancel



IBIS 模型加载方式



IBIS 模型去 ST 官网下载

IBIS models (1)

STM32F405/415 and STM32F407/417 IBIS models



PHY 芯片官网 microchip

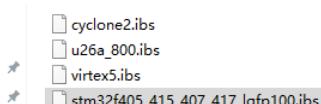


lan8720c.ibs

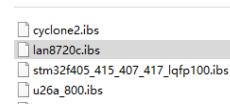
phy 芯片 IBIS

解压 IBIS 文件到 ANSYS 安装路径下的 IBIS 目录中

本地磁盘 (D:) > maxwell_stewp > AnsysEM19.3 > Win64 > buflib > IBIS



xwell_stewp > AnsysEM19.3 > Win64 > buflib > IBIS



重启 SIWAVE 软件，这样系统自动就会找到对应的 IBIS 模型。

Slwizard Step 2: Assign Driver and Receiver Models

Net	Pin	Expose	Part Number	Ref. . .	Type	Corner	IBIS Component	Model Selector	IBIS Model	Excitation So...	PKG RLCs
ETH_MDC	13	<input checked="" type="checkbox"/>	LAN8720A	U5	Receiver	Typical	lan8720e	diosh8_pupd...	diosh8_pupd...	<input checked="" type="checkbox"/>	
EMII_CLK	14	<input checked="" type="checkbox"/>	LAN8720A	U5	Receiver	Typical	lan8720e	diosh8_pupd...	diosh8_pupd...	<input checked="" type="checkbox"/>	
ETH_MDC	16	<input checked="" type="checkbox"/>	STM32F407VET6	U11	Driver (Active)	Typical	stm32f405_415_407_41...	iobp00_ar3ws...	iobp00_ar3ws...	Default Pulse	<input checked="" type="checkbox"/>
EMII_CLK	24	<input checked="" type="checkbox"/>	STM32F407VET6	U11	Driver (Active)	Typical	stm32f405_415_407_41...	iobp00_ar3ws...	iobp00_ar3ws...	Default Pulse	<input checked="" type="checkbox"/>

IO 口输出方式
MCU 输出方式要选择
也可以单独给芯片加入 IBIS 模型
可以通过 Manage 查看输出方式

Manage Sources

Name	Vol...	Type	Bit List	Seed	Period	Duty Cycle	Bit Rate	Delay	Rise Time	Fall Time	Internal Impedance
Default Pulse	1.0V	Pulse Starting High	N/A	N/A	10ns	0.5	N/A	1ns	35ps	35ps	50ohms
Default PRBS	1.0V	PRBS	N/A	1	N/A	N/A	500Mbps	1ns	35ps	35ps	50ohms
Default CustomB...	1.0V	Custom Bit Sequence	11010	N/A	N/A	N/A	500Mbps	1ns	35ps	35ps	50ohms
Default Clock	1.0V	Custom Bit Sequence	1010	N/A	N/A	N/A	500Mbps	1ns	35ps	35ps	50ohms

输出电压跳变 1V
电压周期 10ns
占空比 0.5
上升沿, 下降沿时间
PRBS 是伪随机码, 测试数
据速率可以用这个
如果是测试时钟信号线就选
择时钟输出
PHY 是接收端, 不需要设置

Slwizard Step 2: Assign Driver and Receiver Models

Net	Pin	Expose	Part Number	Ref. . .	Type	Corner	IBIS Component	Model Selector	IBIS Model	Excitation So...	PKG RLCs
ETH_MDC	13	<input checked="" type="checkbox"/>	LAN8720A	U5	Receiver	Typical	lan8720e	diosh8_pupd...	diosh8_pupd...	<input checked="" type="checkbox"/>	
EMII_CLK	14	<input checked="" type="checkbox"/>	LAN8720A	U5	Receiver	Typical	lan8720e	diosh8_pupd...	diosh8_pupd...	<input checked="" type="checkbox"/>	
ETH_MDC	16	<input checked="" type="checkbox"/>	STM32F407VET6	U11	Driver (Active)	Typical	stm32f405_415_407_41...	iobp00_ar3ws...	iobp00_ar3ws...	Default PRBS	<input checked="" type="checkbox"/>
EMII_CLK	24	<input checked="" type="checkbox"/>	STM32F407VET6	U11	Driver (Active)	Typical	stm32f405_415_407_41...	iobp00_ar3ws...	iobp00_ar3ws...	Default PRBS	<input checked="" type="checkbox"/>

选择随机码输出
点击下一步

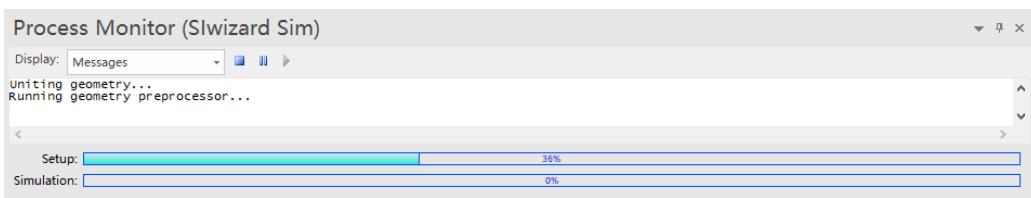
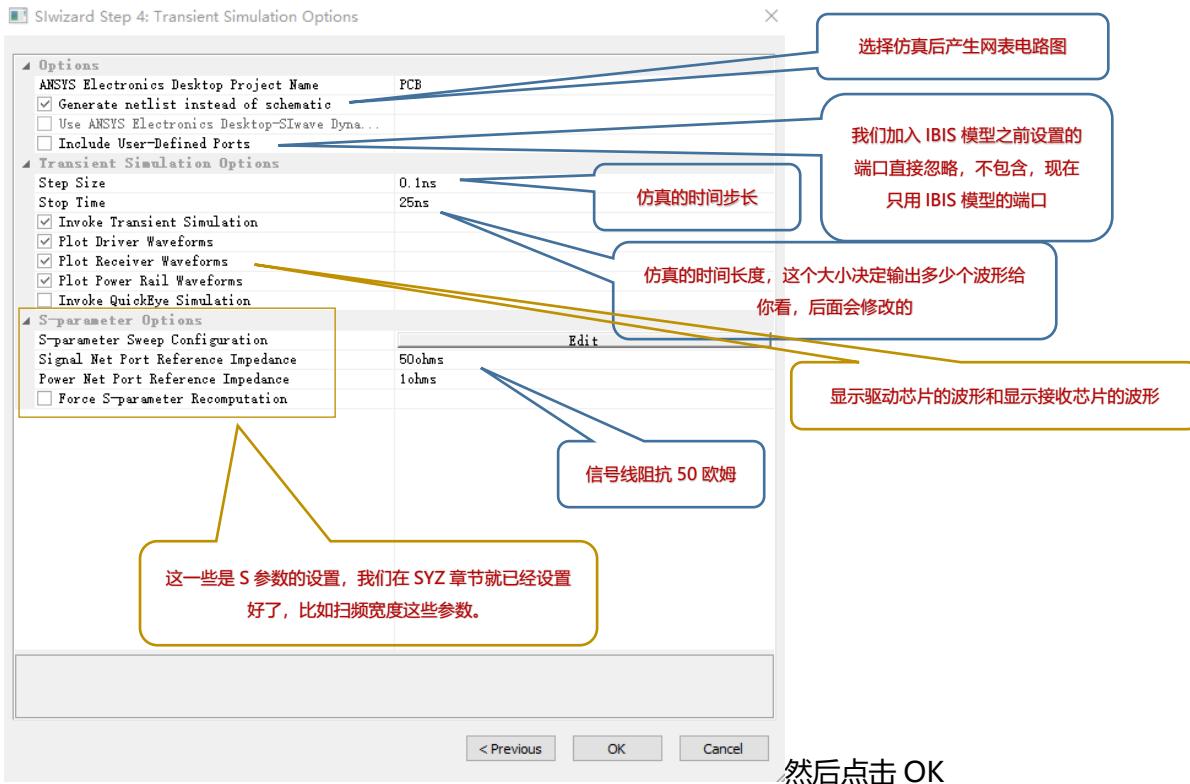
Slwizard Step 3: Component Power and Ground Nets

Part Name	Ref. Des.	Supply	Power Net	Ground Net	Power Pin Grouping	Ground Pin Group...
LAN8720A	U5	Buffer Internal Voltage	VDDEXT_1V8	GND	Group All	Group All
STM32F407VET6	U11	Buffer Internal Voltage	VDDEXT_1V8	GND	Group All	Group All

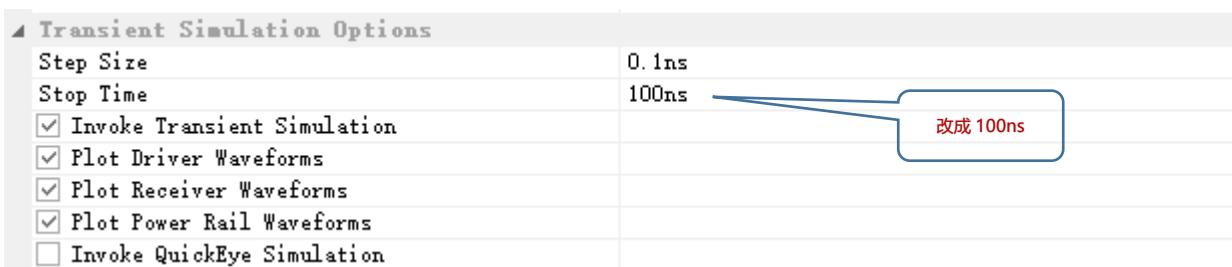
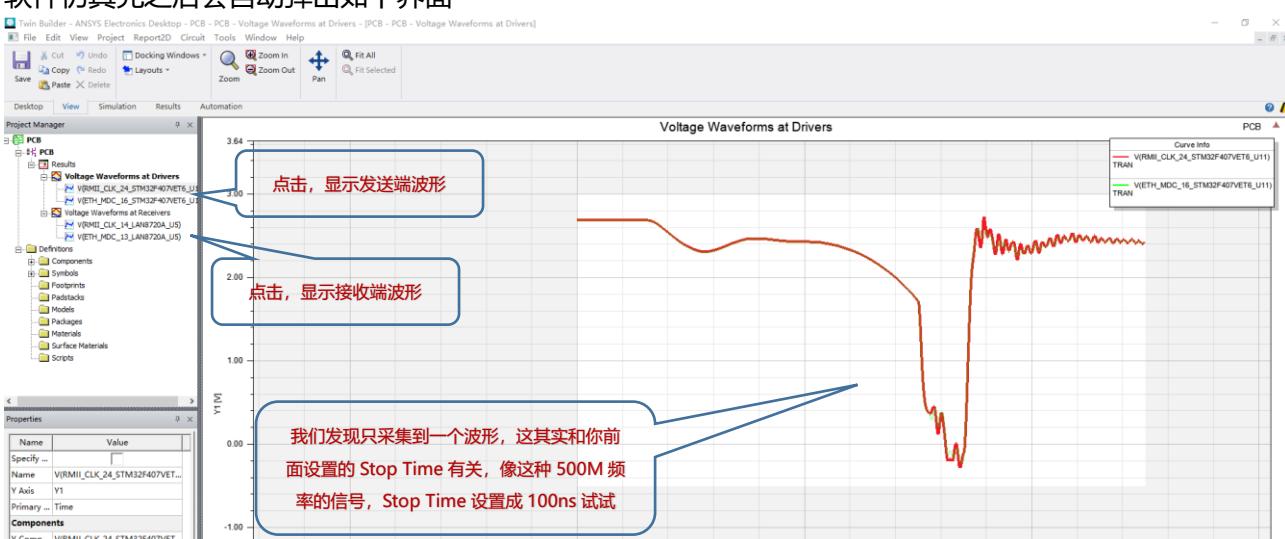
Operations
Supply: Buffer Internal Voltage
Power Net: VDDEXT_1V8
Ground Net: GND

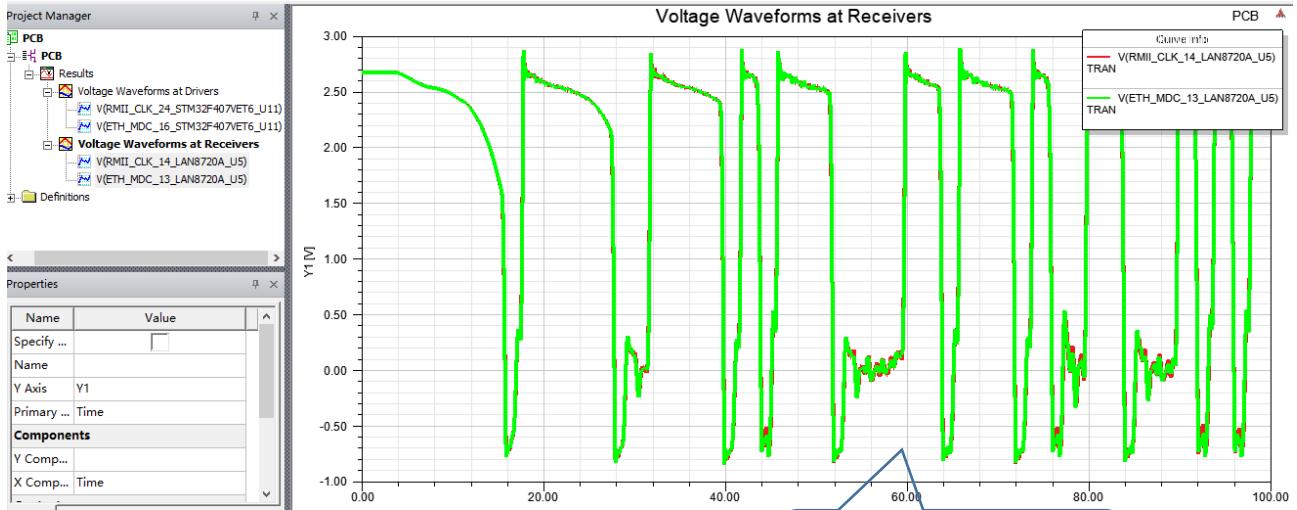
设置器件电源的影响, 如果不考虑用电情况, 选择 Buffer Internal Voltage 就可以了。如果考虑电源影响, 选择 VRM

我们不考虑电源影响, 点击 Next

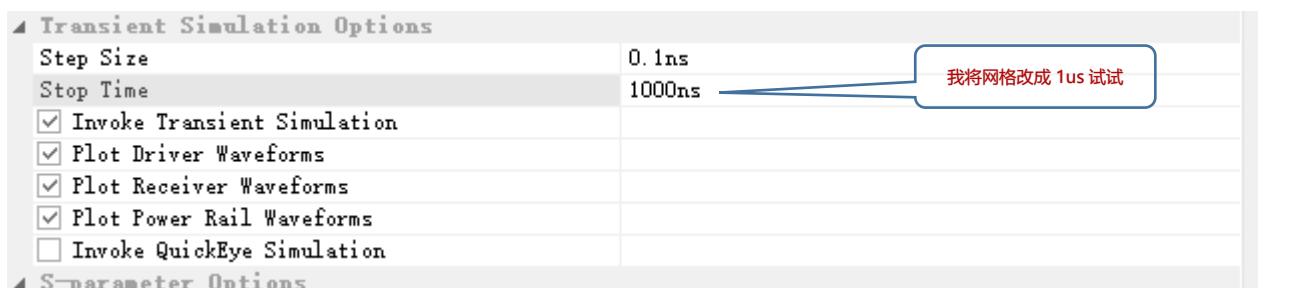
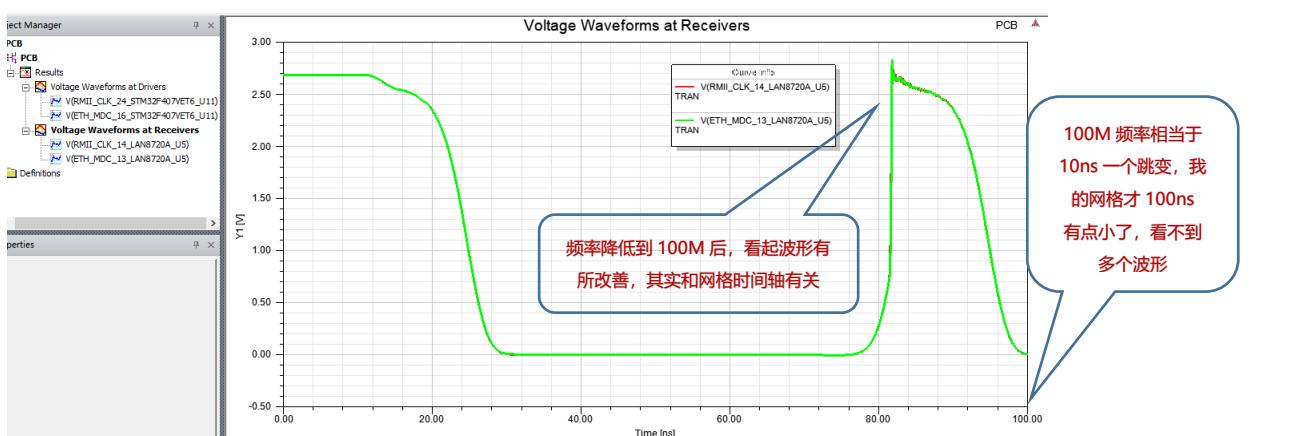
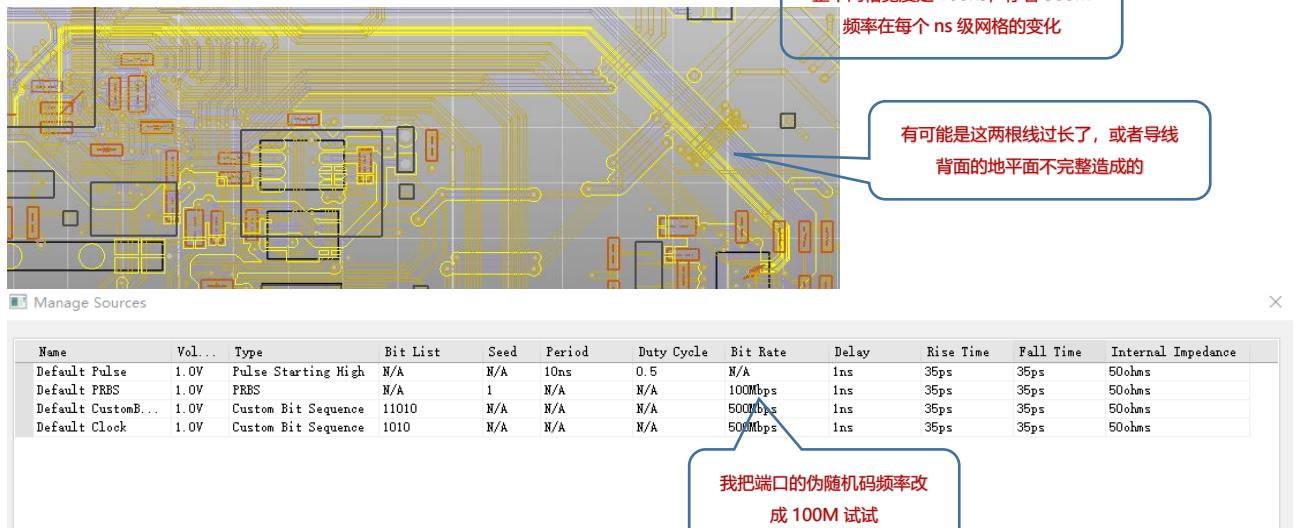


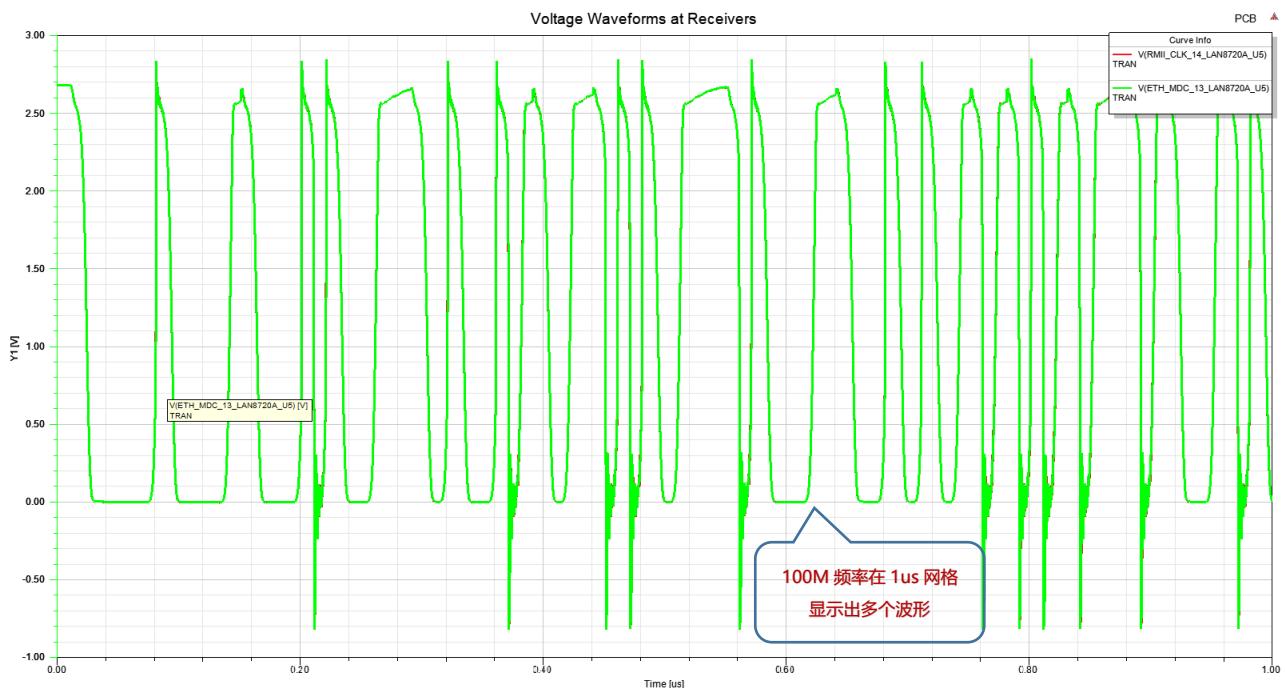
软件仿真完之后会自动弹出如下界面





500M 频率接收端波形效果不是很好。



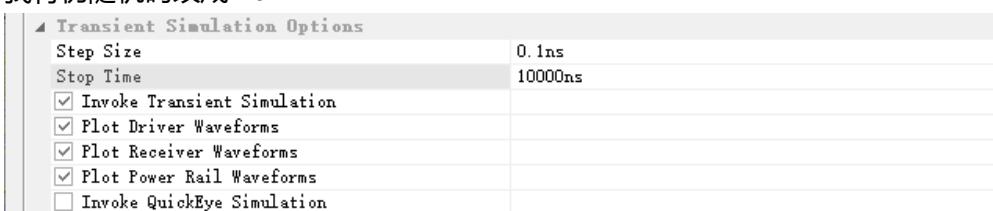


但是感觉波形过冲还是比较严重

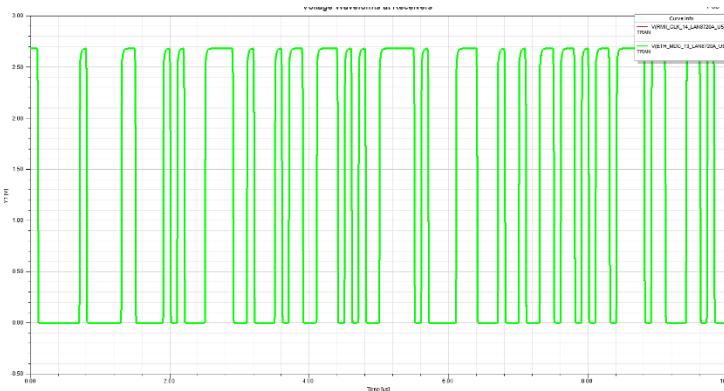
Manage Sources

Name	Vol...	Type	Bit List	Seed	Period	Duty Cycle	Bit Rate	Delay	Rise Time	Fall Time	Internal Impedance
Default Pulse	1.0V	Pulse Starting High	N/A	N/A	10ns	0.5	N/A	1ns	35ps	35ps	50ohms
Default PRBS	1.0V	PRBS	N/A	1	N/A	N/A	10Mbps	1ns	35ps	35ps	50ohms
Default CustomB...	1.0V	Custom Bit Sequence	11010	N/A	N/A	N/A	500Mbps	1ns	35ps	35ps	50ohms
Default Clock	1.0V	Custom Bit Sequence	1010	N/A	N/A	N/A	500Mbps	1ns	35ps	35ps	50ohms

我将伪随机码改成 10M



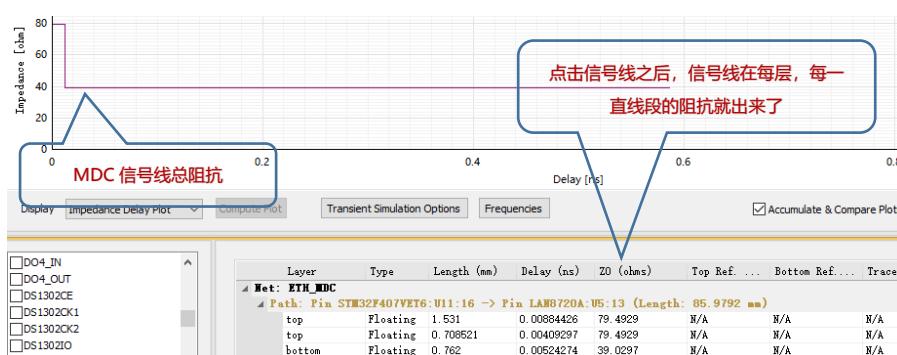
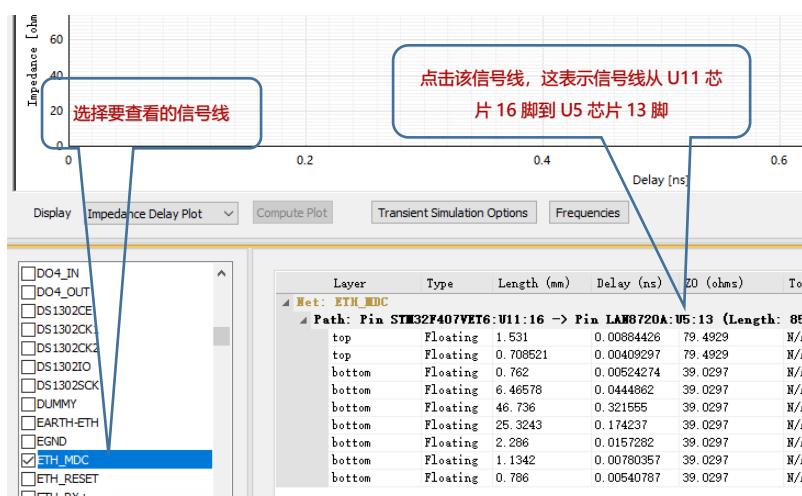
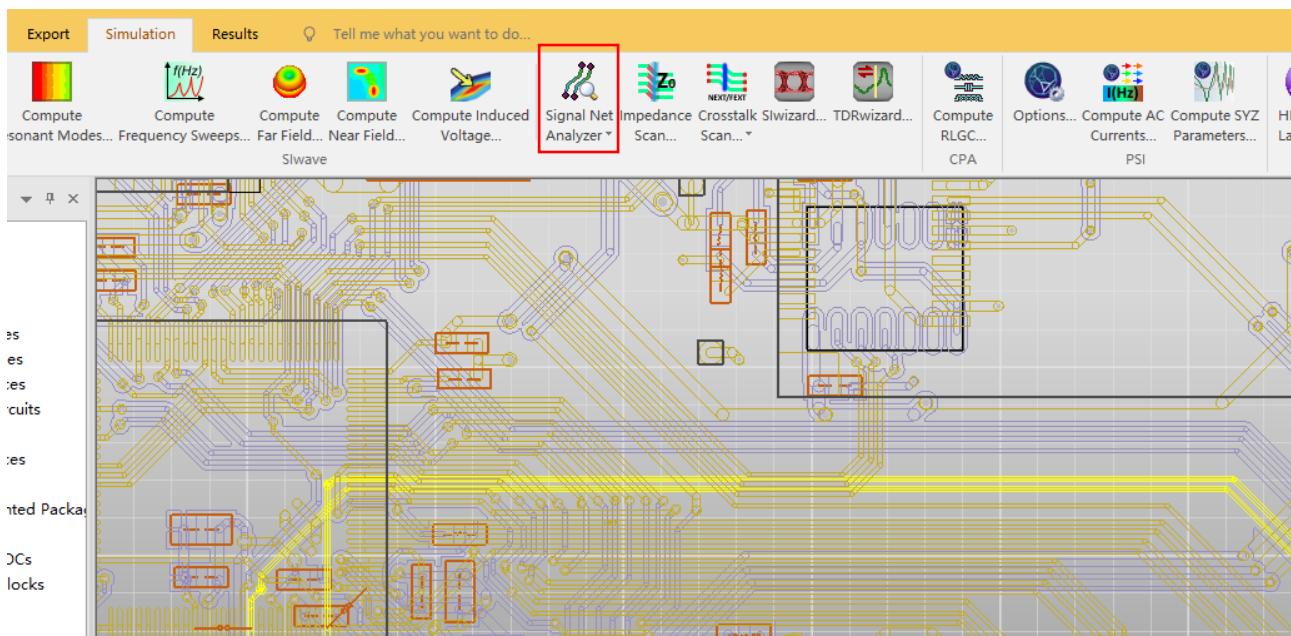
网格改成 10us



你看，波形正常了。所以高速信号还是和

PCB 排版走线有关

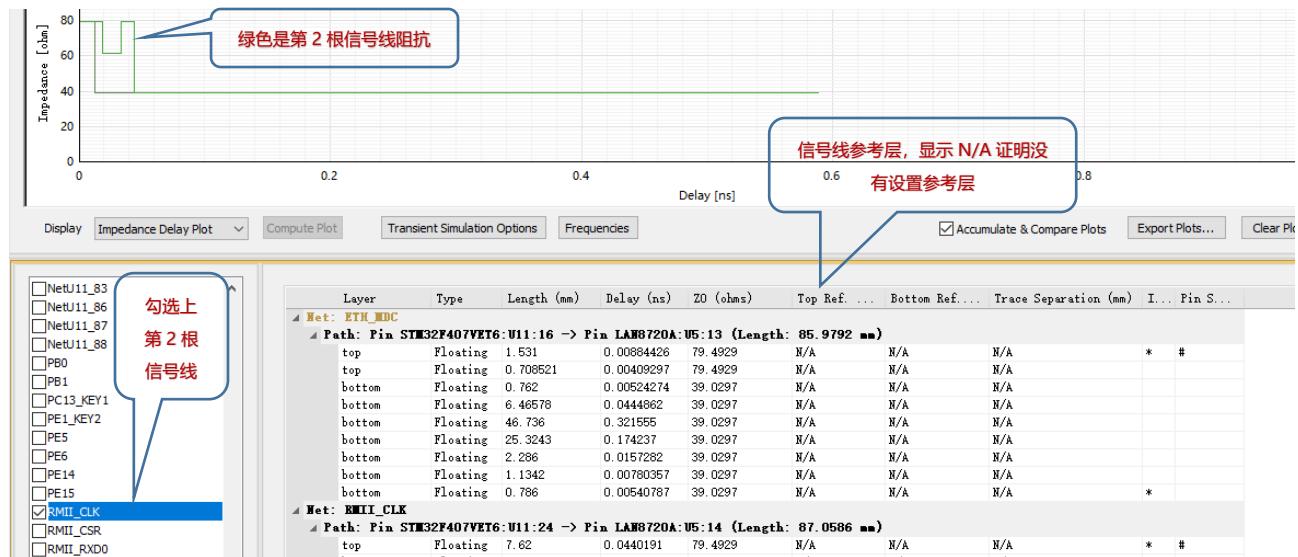
单根信号线长度和阻抗查看



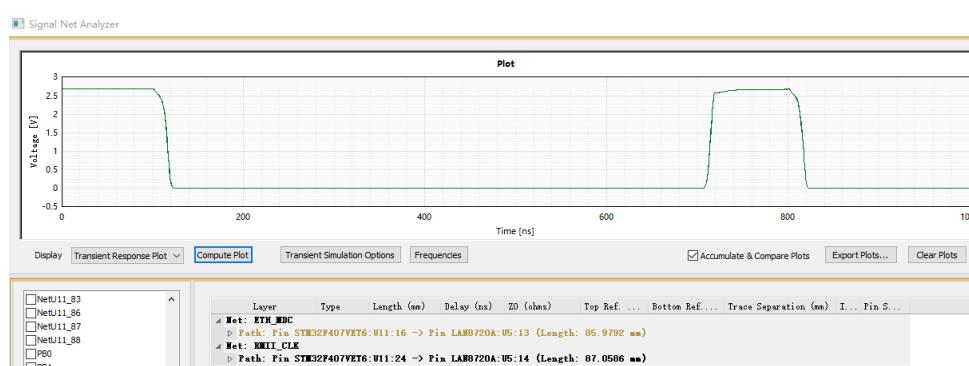
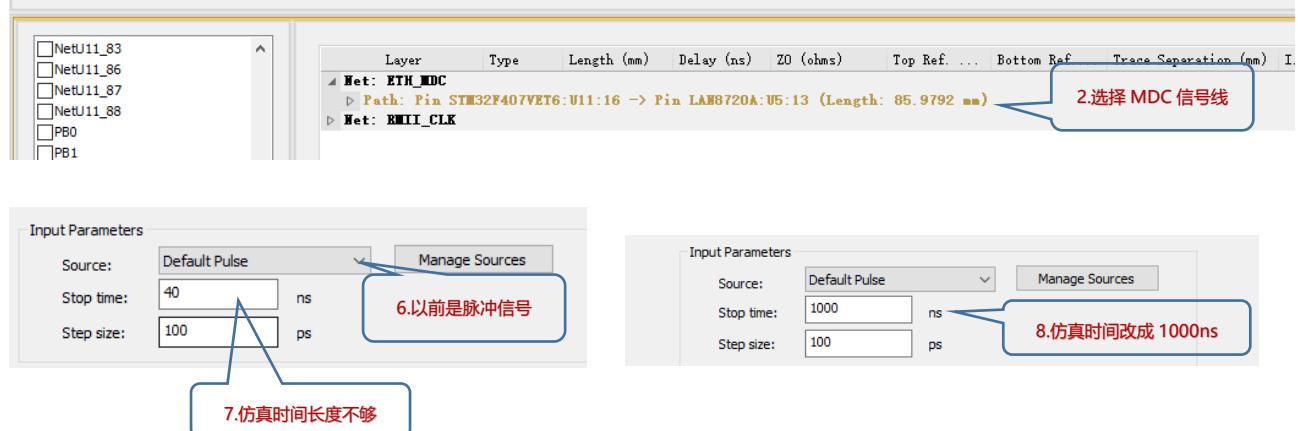
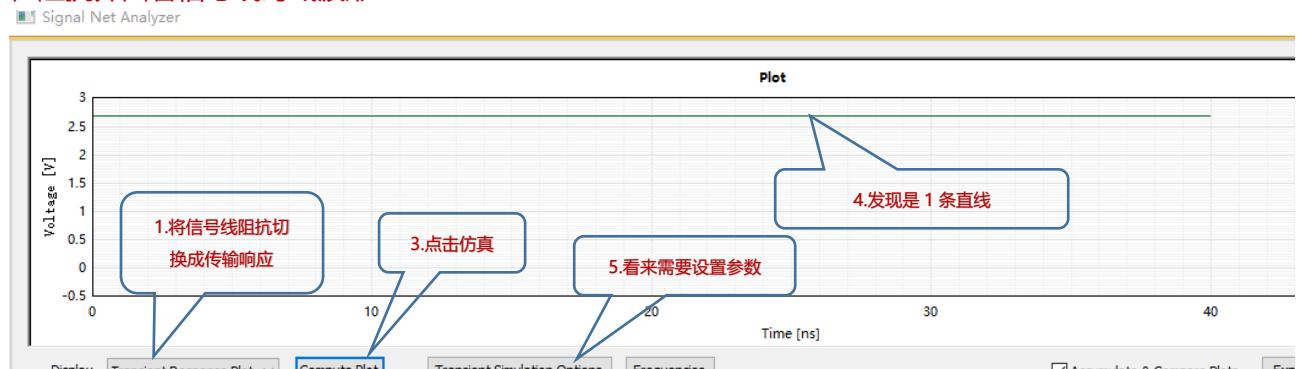
MDC 信号线总长度

Layer	Type	Length (mm)	Delay (ns)	Z0 (ohms)	Top Ref.	Bottom Ref.	Trace Separation (mm)	I... Fin S...
Net: ETH_MDC								
Path: Pin STM32F407VET6:U11:16 → Pin LAM8720A:U5:13 (Length: 85.9792 mm)								
top	Floating	1.531	0.00884426	79.4929	N/A	N/A	*	#
top	Floating	0.708521	0.00409297	79.4929	N/A	N/A		
bottom	Floating	0.762	0.00524274	39.0297	N/A	N/A		
bottom	Floating	6.46578	0.0444862	39.0297	N/A	N/A		
bottom	Floating	46.736	0.321555	39.0297	N/A	N/A		
bottom	Floating	25.3243	0.174237	39.0297	N/A	N/A		
bottom	Floating	2.286	0.0157282	39.0297	N/A	N/A		
bottom	Floating	1.1342	0.00780357	39.0297	N/A	N/A		
bottom	Floating	0.786	0.00540787	39.0297	N/A	N/A	*	

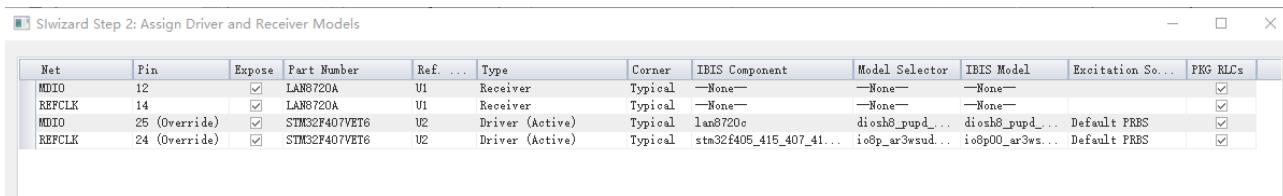
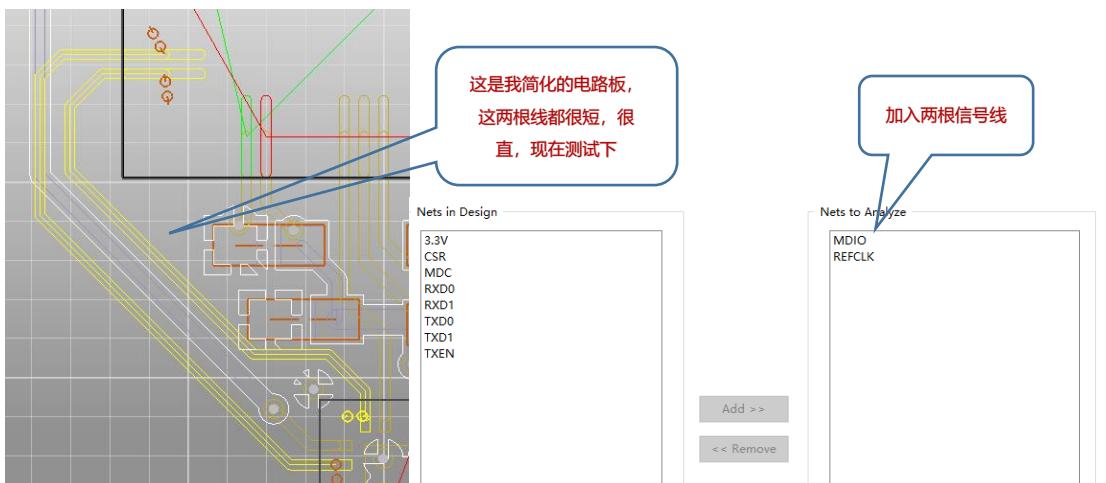
查看多根信号线的阻抗。以两根信号线为例



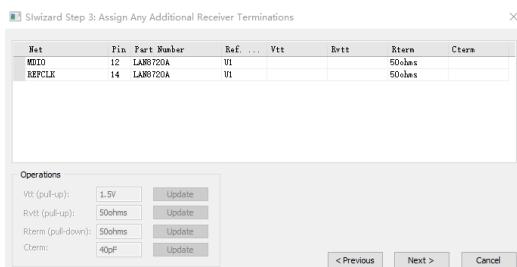
在阻抗界面看信号线时域波形



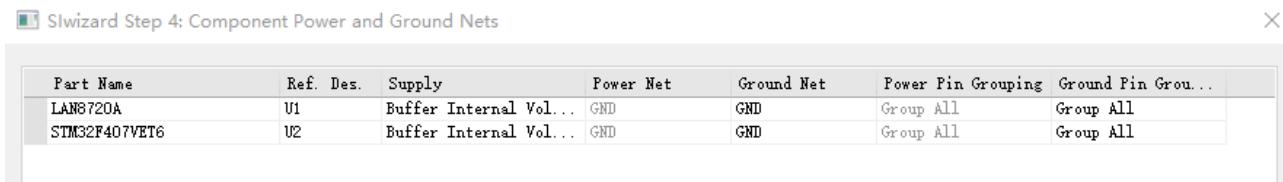
用简化版的 PCB，再来测试次 SI



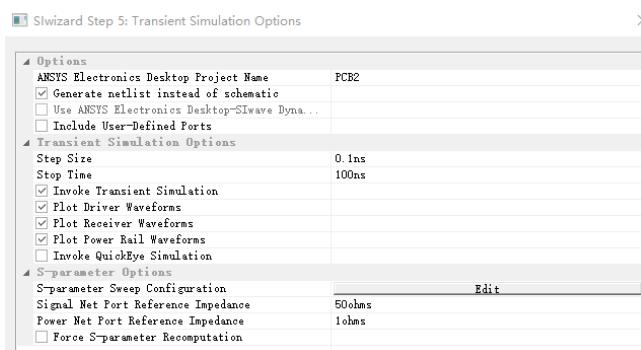
加入 IBIS 模型，伪随机码输出



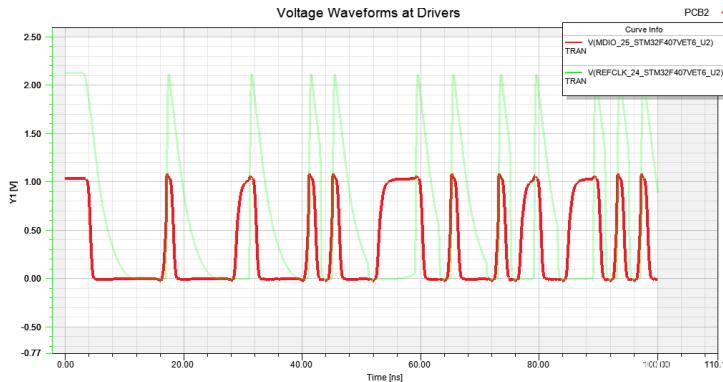
确认，继续下一步



无需电源影响，直接 Buffer 输出。



仿真长度 100ns，多看几个波形，直接 OK 仿真

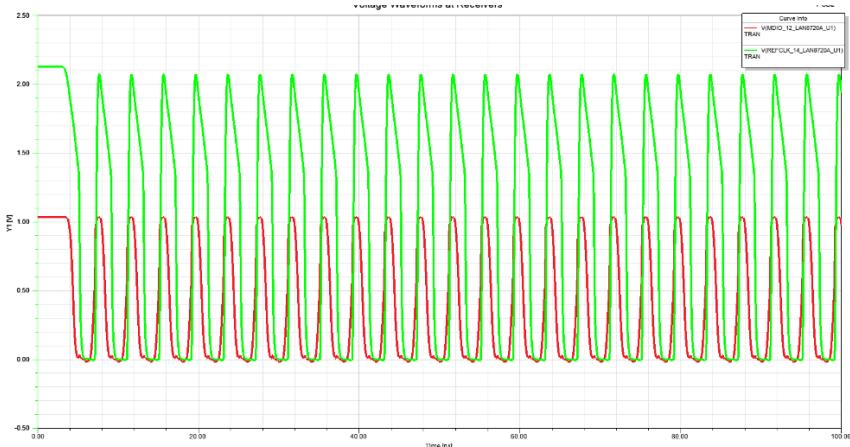


这就是仿真结果，比之前高密度板子好得多。

这是 500M 随机码的信号，还是有点不完美。

Net	Pin	Expose	Part Number	Ref. . .	Type	Corner	IBIS Component	Model Selector	IBIS Model	Excitation So... PKG RLCs
MDIO	12	✓	LAN8720A	U1	Receiver	Typical	—None—	—None—	—None—	✓
REFCLK	14	✓	LAN8720A	U1	Receiver	Typical	—None—	—None—	—None—	✓
MDIO	25 (Override)	✓	STM32F407VET6	U2	Driver (Active)	Typical	lan8720c	diosh8_pupd...	diosh8_pupd...	Default Clock
REFCLK	24 (Override)	✓	STM32F407VET6	U2	Driver (Active)	Typical	stm32f405_415_407_41...	iop0_ar3wsud...	iop0_ar3ws...	Default Clock ✓

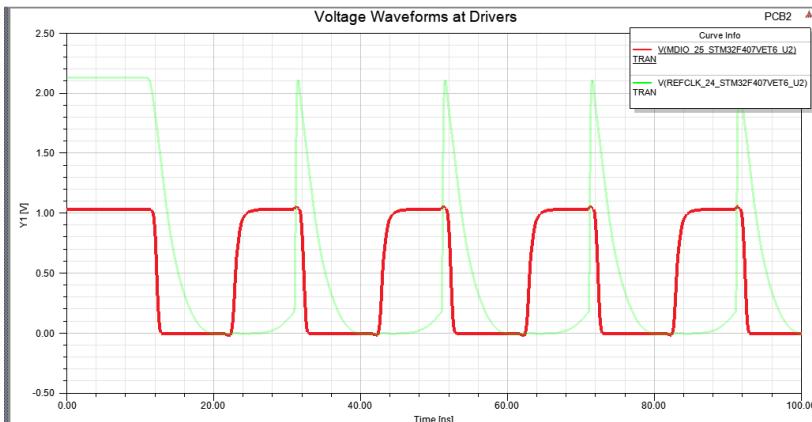
我改成时钟输出试试。



这是时钟输出，波形比较规整，但波形不是很方。最好是理想方波效果。

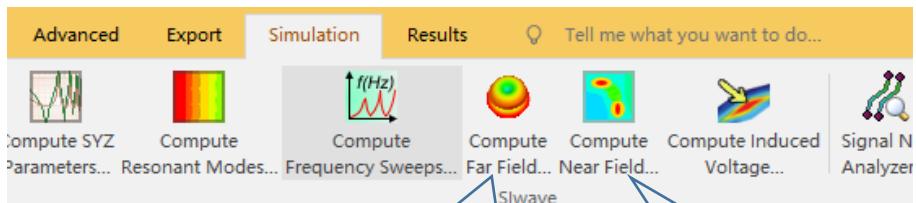
Name	Vol ...	Type	Bit List	Seed	Period	Duty Cycle	Bit Rate	Delay	Rise Time	Fall Time	Internal Impedance
Default Pulse	1.0V	Pulse Starting High	N/A	N/A	10ns	0.5	N/A	1ns	35ps	35ps	50ohms
Default PRBS	1.0V	PRBS	N/A	1	N/A	N/A	500Mbps	1ns	35ps	35ps	50ohms
Default CustomB...	1.0V	Custom Bit Sequence	11010	N/A	N/A	N/A	500Mbps	1ns	35ps	35ps	50ohms
Default Clock	1.0V	Custom Bit Sequence	1010	N/A	N/A	N/A	100Mbps	1ns	35ps	35ps	50ohms

我把时钟输出从 500M 降低到 100M 试试



MDIO 红色信号线很理想了，但是 REFCLK 绿色时钟信号线不是很理想。

PCB 电路板电磁辐射仿真



我们现在讲解近场仿真

什么是近场仿真？其实就是拿起频谱仪的探棒在电路板上面扫。



Compute Near Field

Near Field Distributed Analysis (HPC)

Simulation Near Field Sim 1

Excitations

(Use sources defined in project)
(Use sources defined in external file)
 Interpolate spectrum at missing frequency point

Configure sweep for EMI analysis...

Frequency Range Setup

Start Freq	Stop Freq	Num. Points	Distribution
1 5MHz	5GHz	100	Linear

Add Above Add Below Delete Selection Preview...
Save Load Set Default Clear Default

Meshing Frequencies for the Observation Mesh

(Default: Max. Frequency from the Sweep: 5GHz)
(Points:
(Range:

Cuboid Surface Positions (Offset values in mm)

+x: 3 -x: 3 +y: 3 -y: 3 +z: 3 -z: 3

Near Field Solver Options

Min. Adapt: 1 Triangles to Add / 20 % Maximum Edge Length: Automatically determined
Max. Adapt Passes: 10 Global Error: 3 % (input type="radio") 2.54952 mm (input type="radio")

Export near field data to .and/.nfd file:

Other solver options...

Save Settings Launch Close

第 1 种就是在 PCB 上自己画一个噪声源进行测试

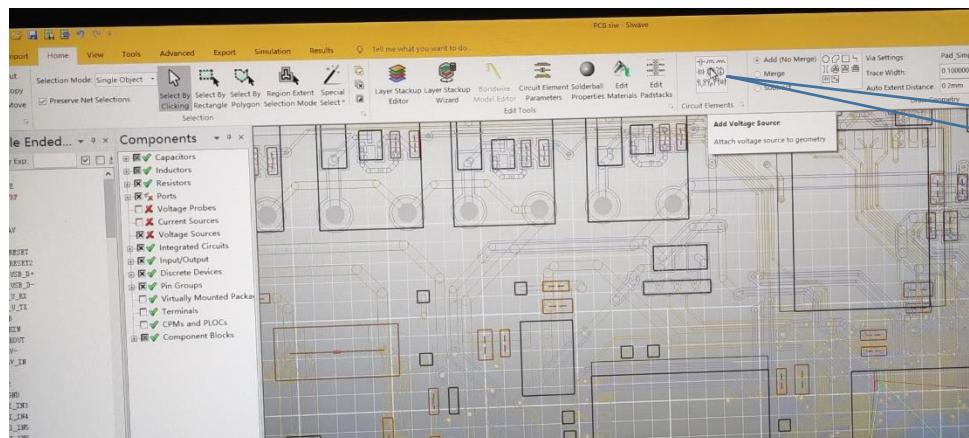
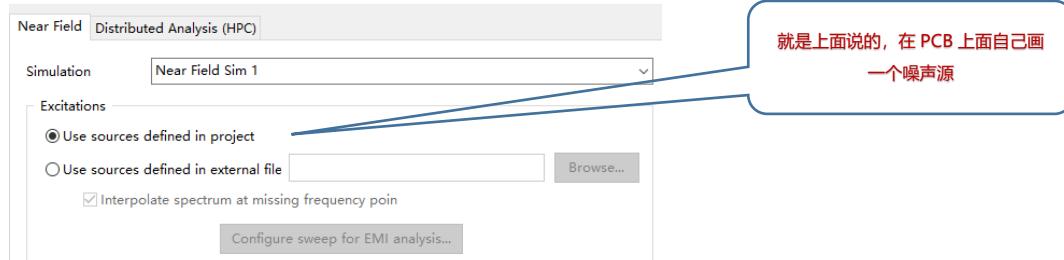
第 2 种就是 SYZ 参数提取后，生成模型文件加载进行测试，这种比较麻烦

设置 PCB 噪声的频率扫描范围，也就是你要 PCB 向外辐射多少 MHz 的噪声范围，建议不要用 5GHz，频点太宽了，仿真时间太长

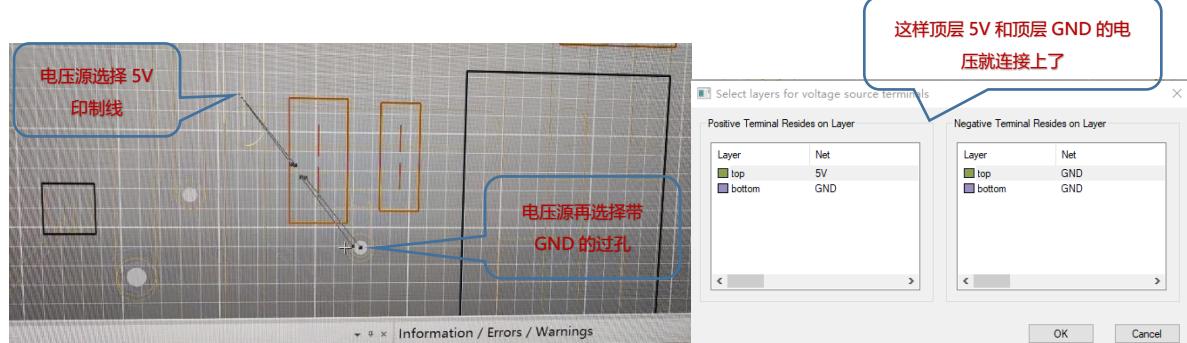
设置 PCB 场强范围，什么意思呢？

第1种方式，用自定义的噪声源进行仿真

Compute Near Field



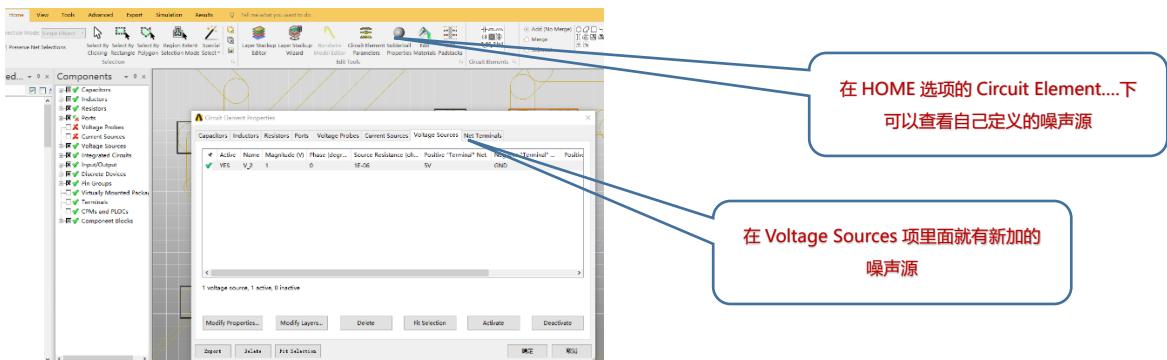
如果我要测量 5V 到 GND 网络的辐射，我就将电压源放在 5V 和 GND 的印制导线上



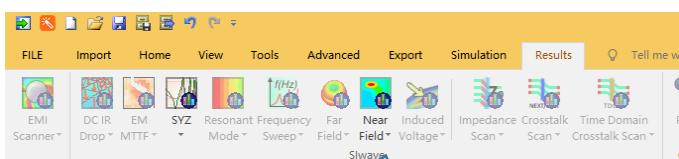
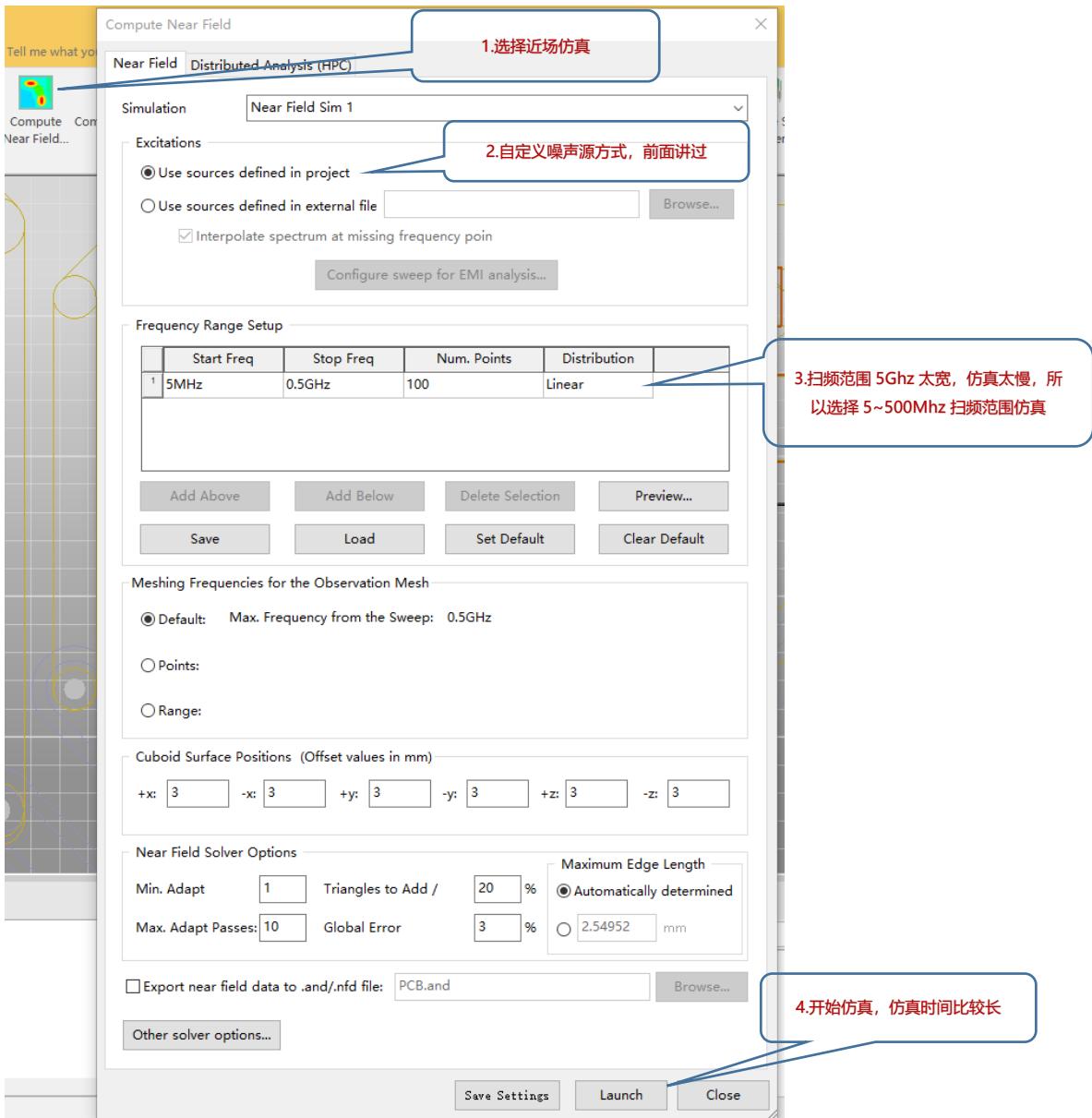
点击 OK 之后，要求你设置电压强度

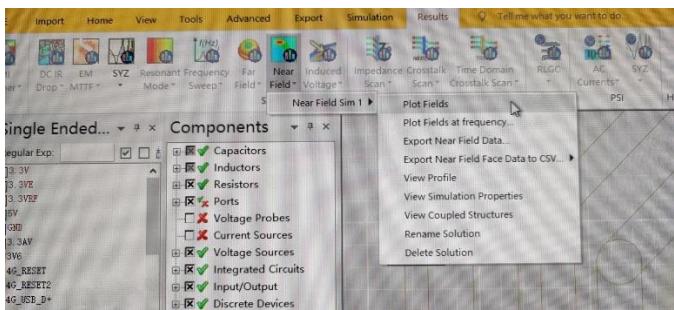


实际上噪声在每个频点的幅值(电压值)是不一样的，所有我们选择的(与频率无关电压源)测试就比较局限，现在只是仿真，可以这样做。要精准计算辐射强度还是要选择与频率相关的电压源。

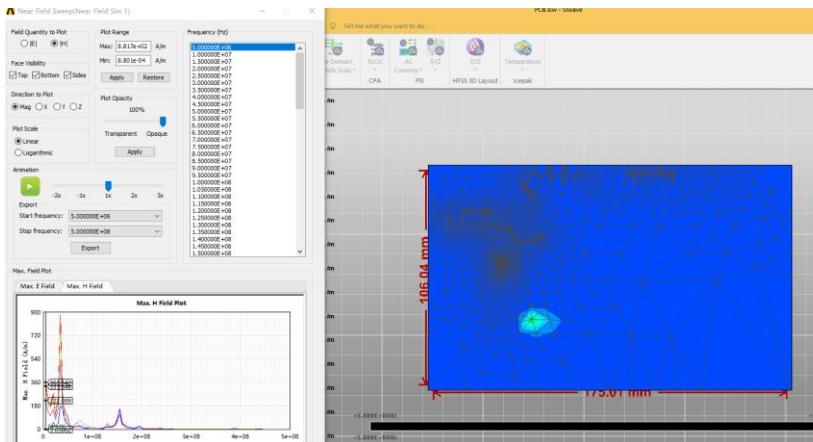


下面开始进行仿真



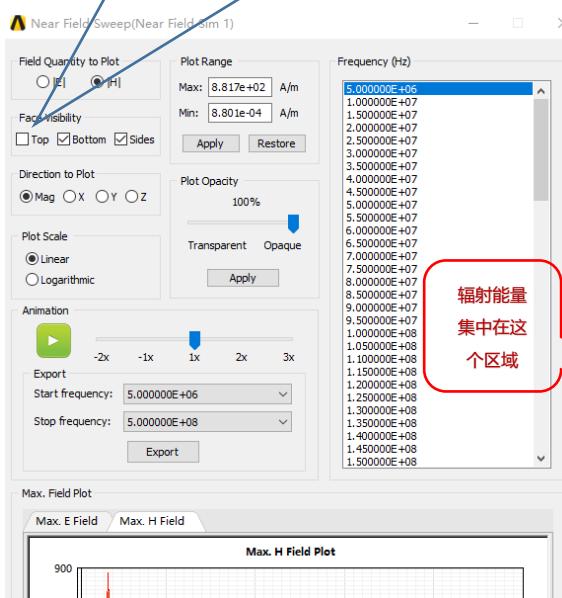


选择 Plot Fields 看结果

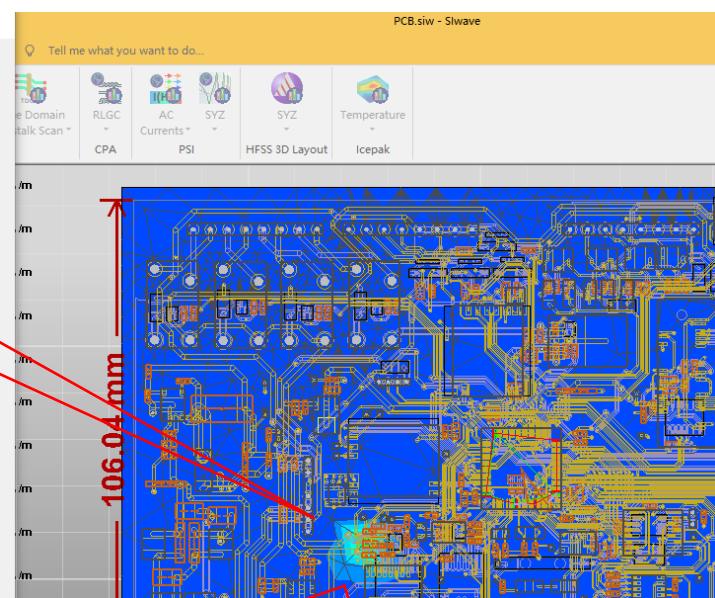


这就是仿真结果

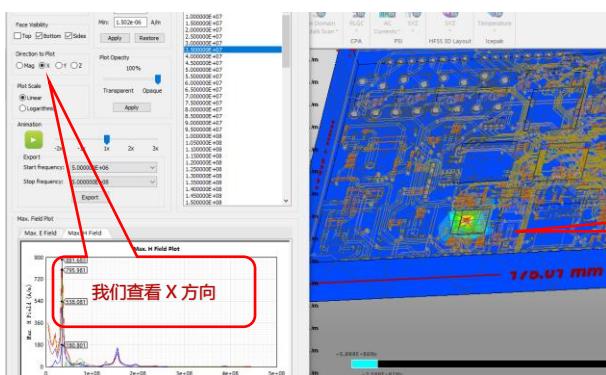
取消勾选，关闭掉 Top 层的隐藏，这样 Top 层就显示出来了



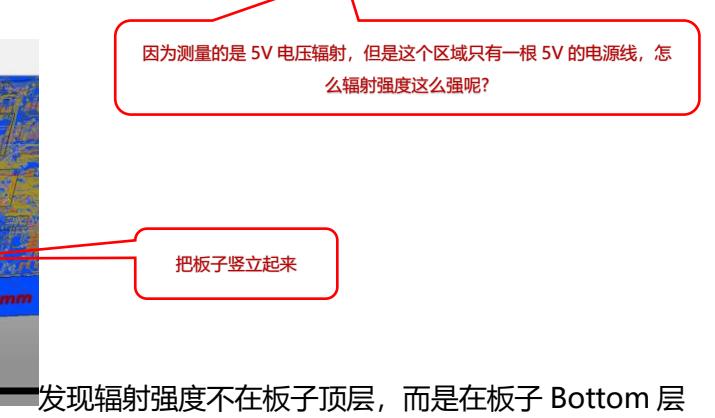
辐射能量
集中在这
个区域



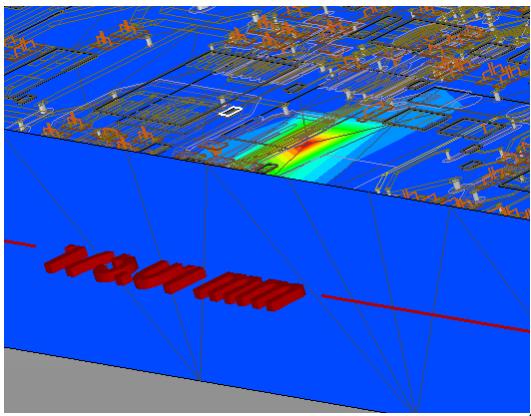
因为测量的是 5V 电压辐射，但是这个区域只有一根 5V 的电源线，怎
么辐射强度这么强呢？



我们查看 X 方向

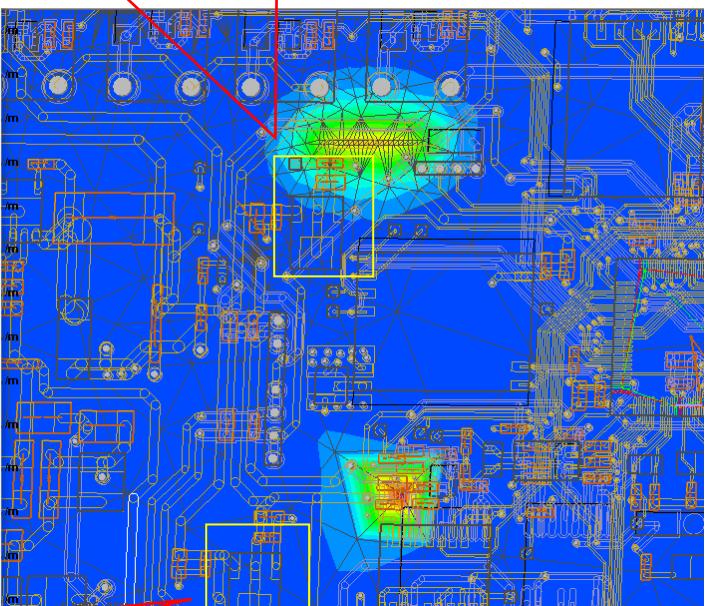
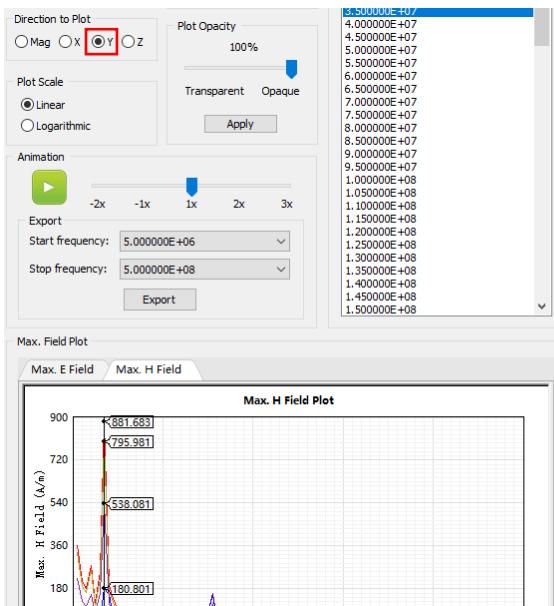


发现辐射强度不在板子顶层，而是在板子 Bottom 层



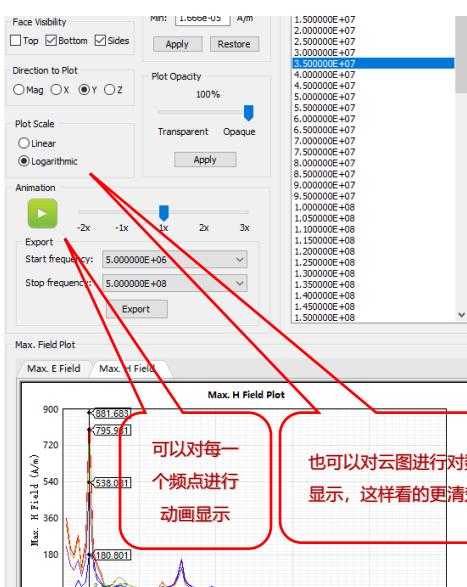
从这个方向看，辐射强度在板子背面。

我们看看 Y 方向是什么变化

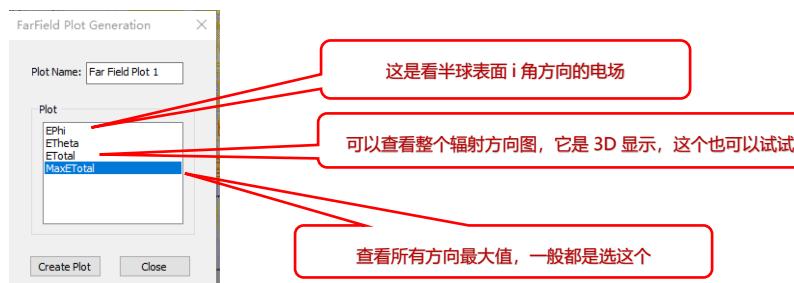
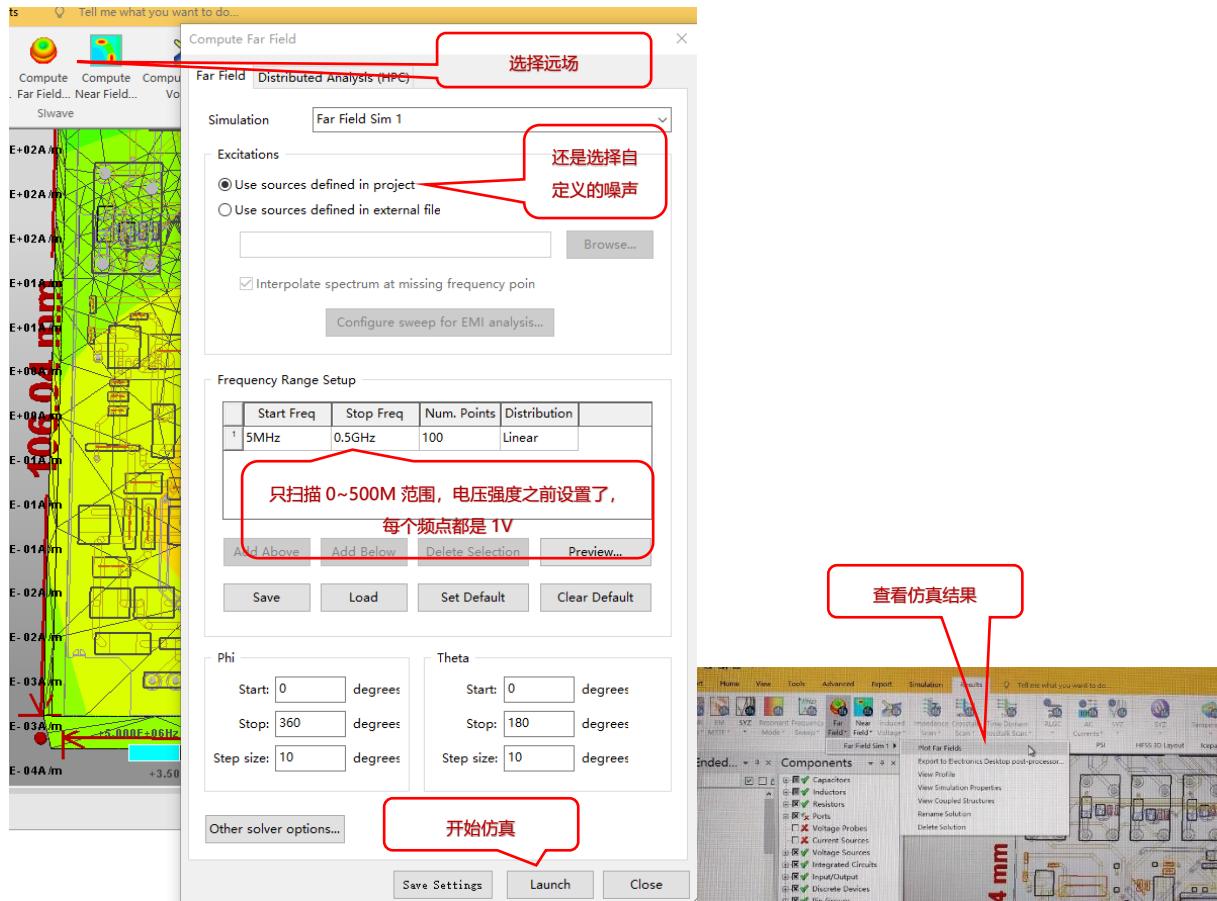


从 y 方向看，这儿也有一个 5V 降压 3.3V 的 LDO

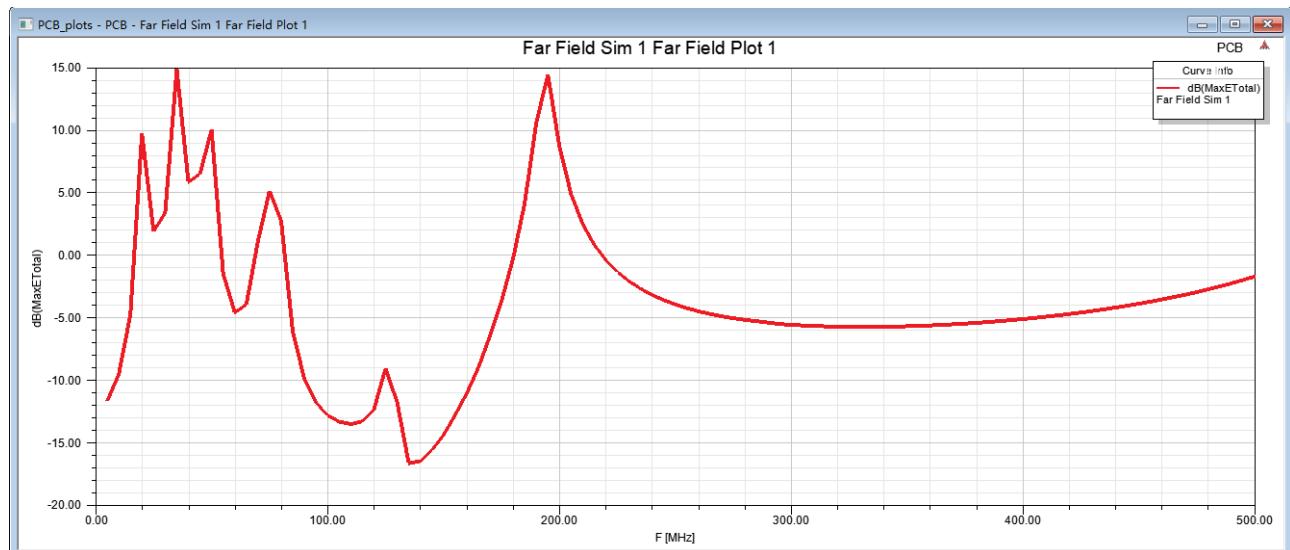
这下就能说明为什么 5V 在这两个区域辐射这么大了。

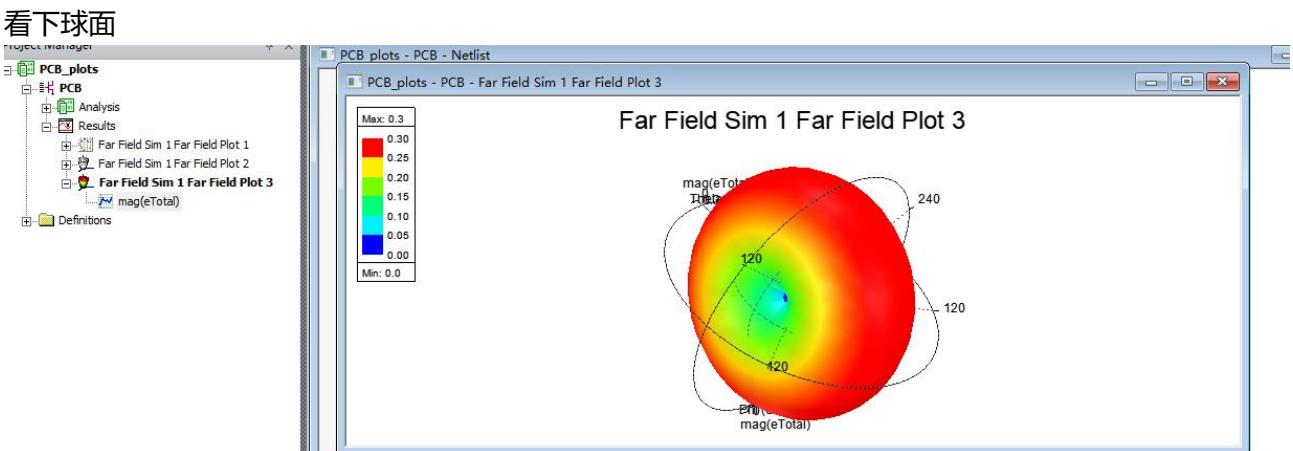


远场仿真

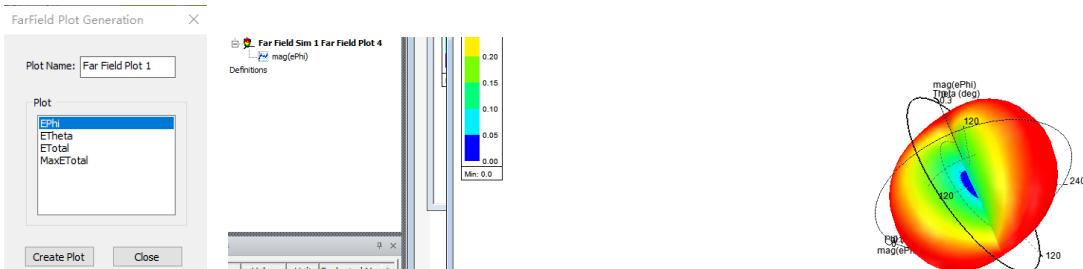


自动弹出 Electronics 软件，得到辐射强度曲线。可以将这个结果拿去和做 EMI 的标准对比下。



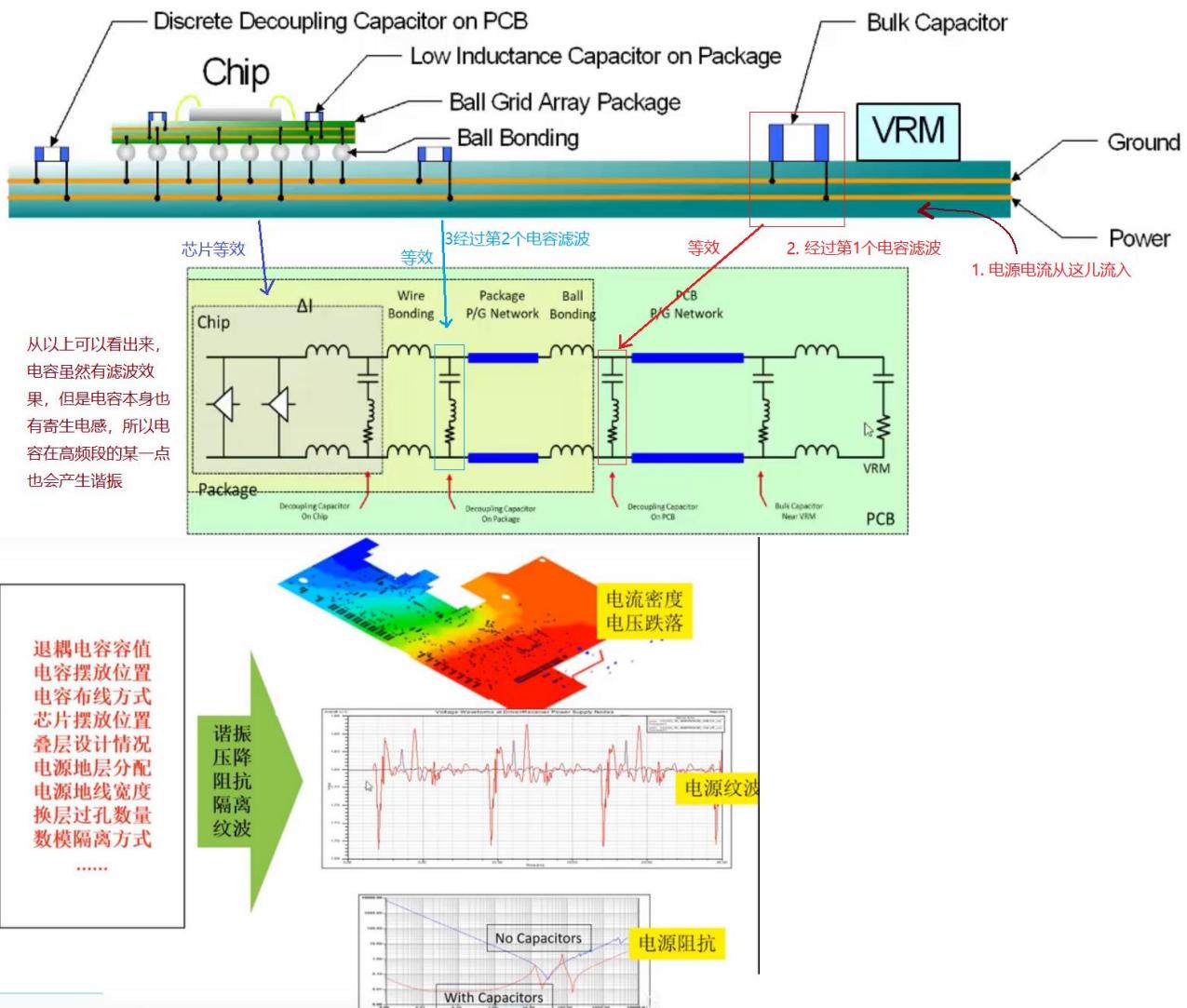


查看 i 方向



电源完整性分析

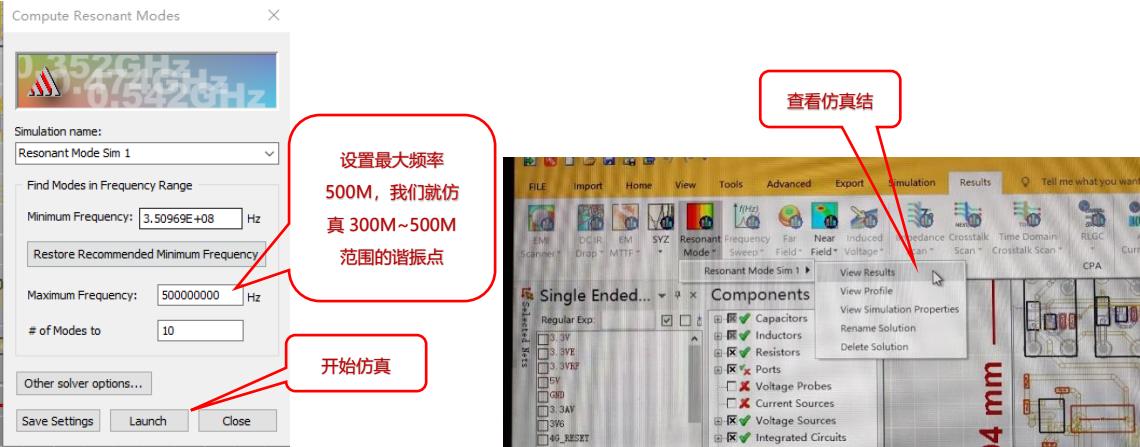
基本理论介绍



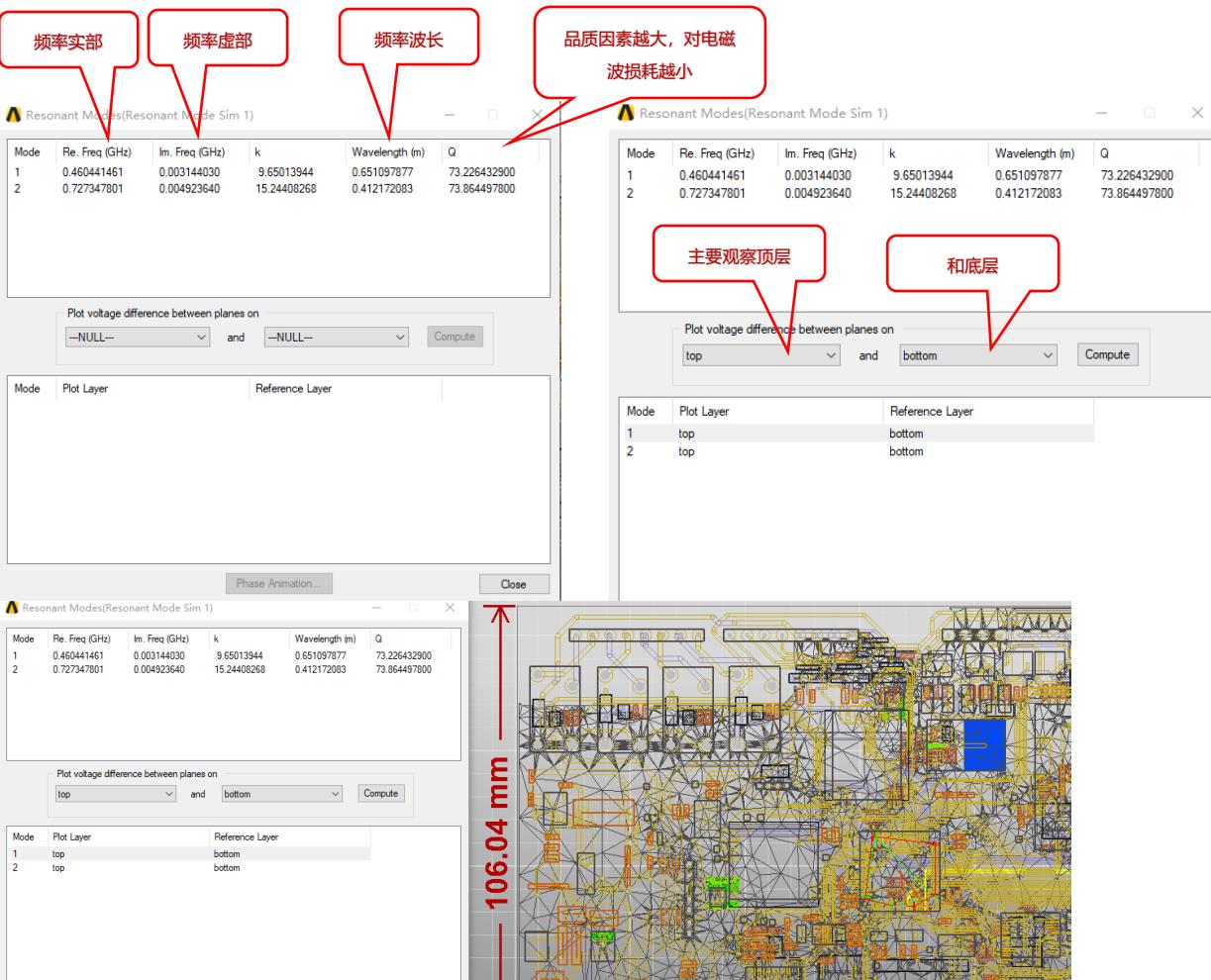
板级电源完整性仿真

采用谐振分析法来分析电源，谐振分析是经过 PCB 物理尺寸来分析 PCB 谐振状态。

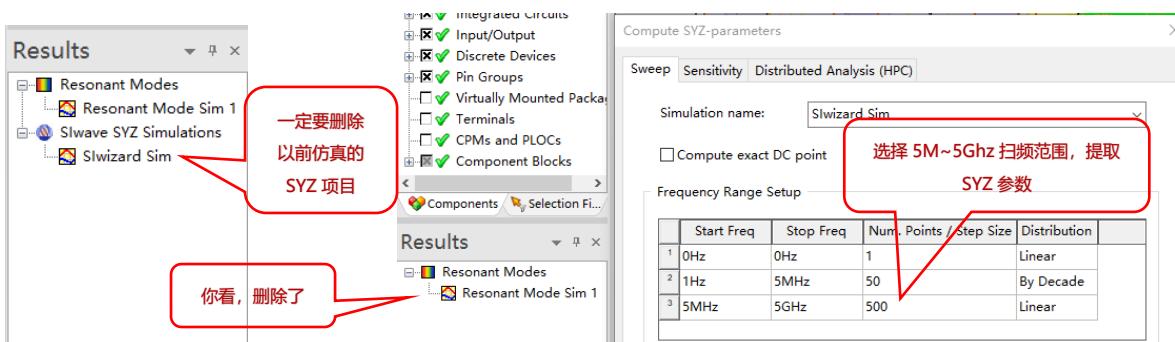
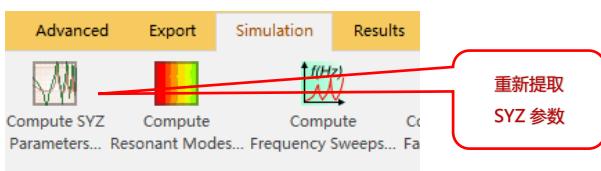
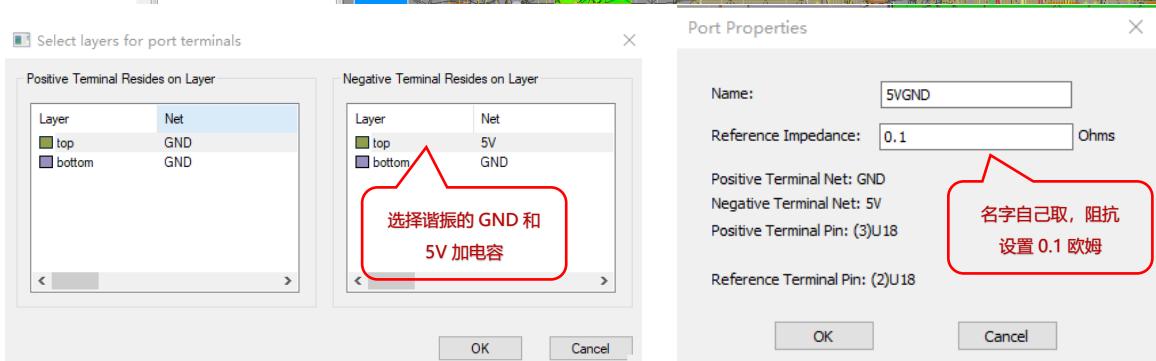
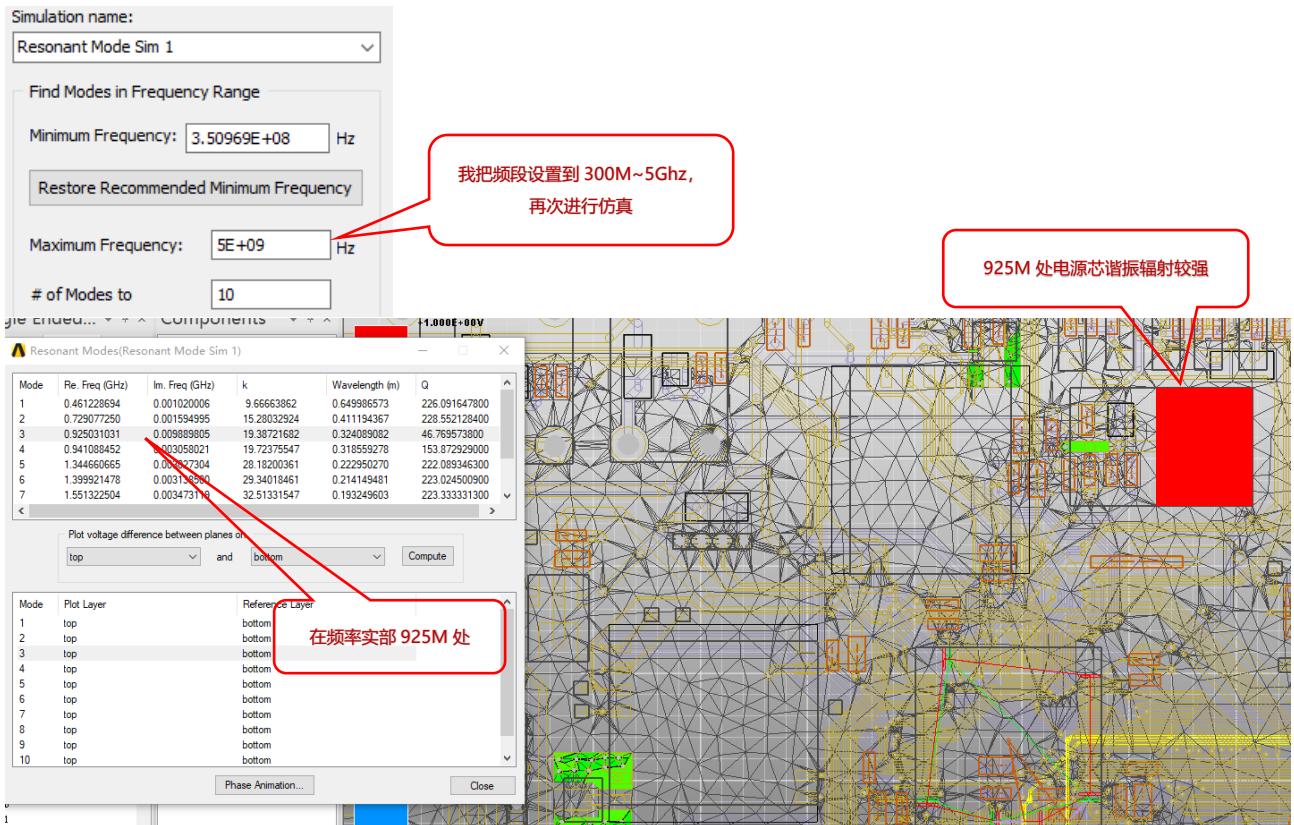




报告显示频率是以实部和虚部展示，所以频率并不是完整的 300M~500M，而是在 300M~500M 上下

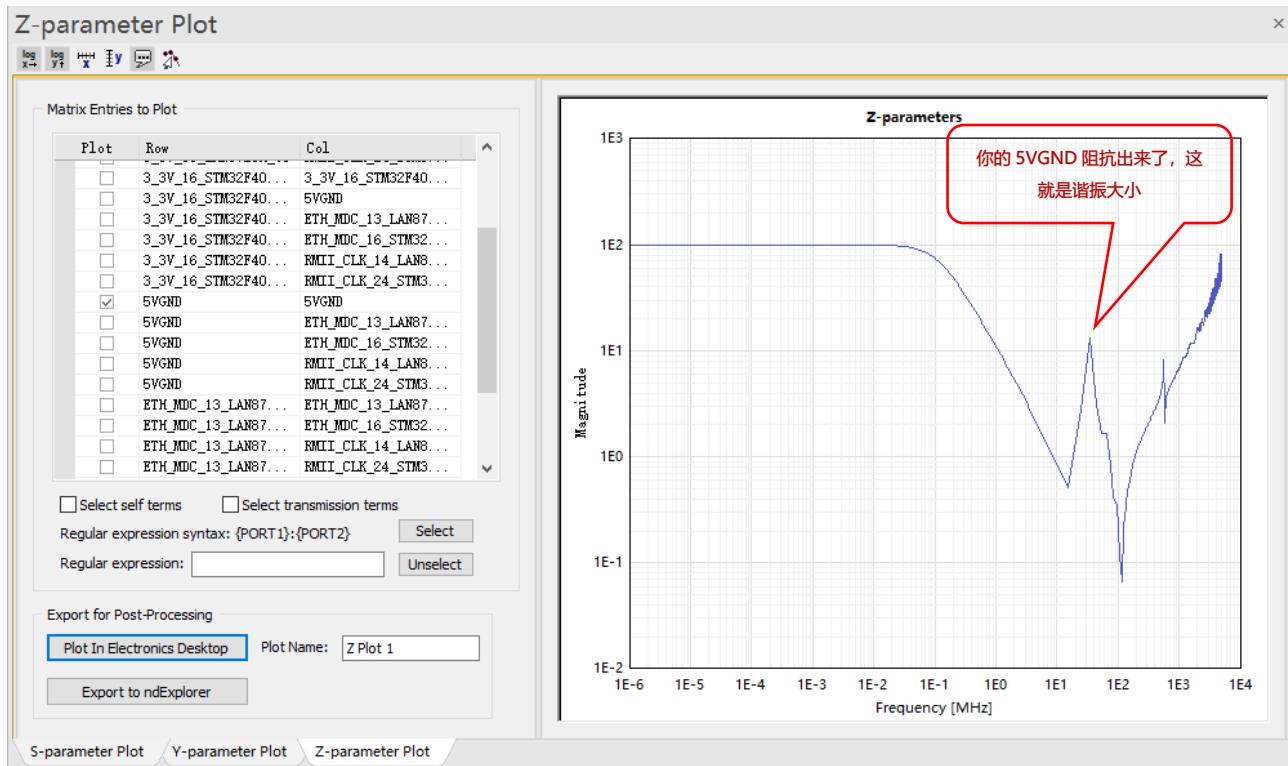


蓝色和绿色谐振强度区域就出来了。

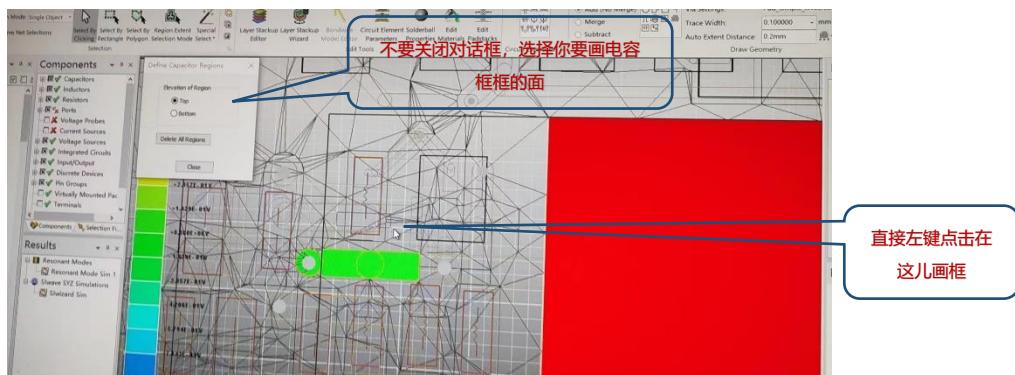
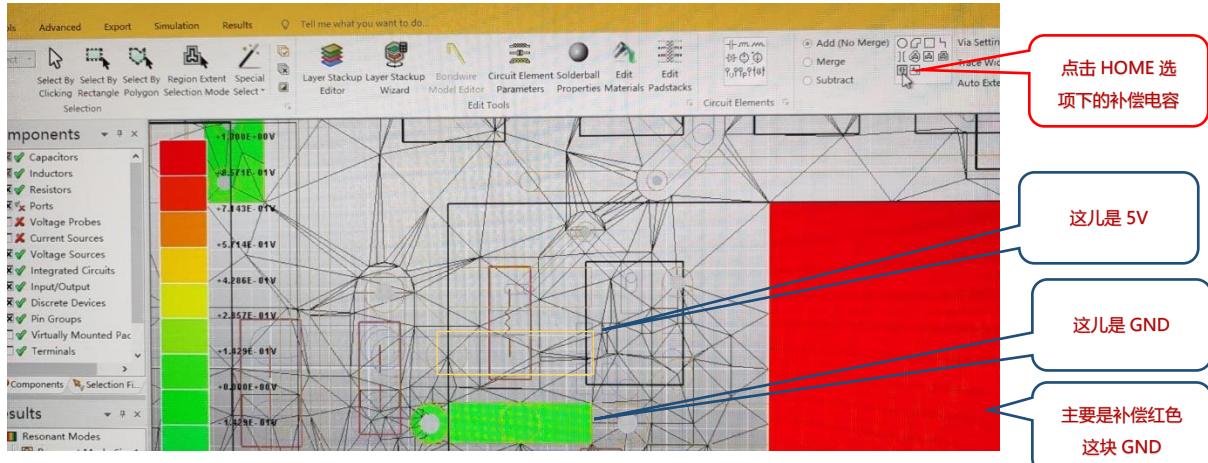


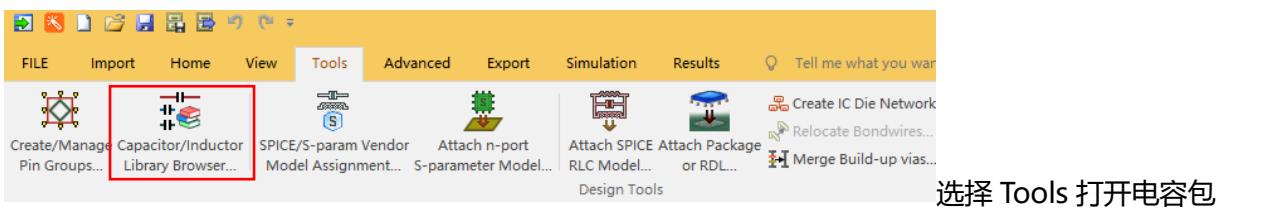
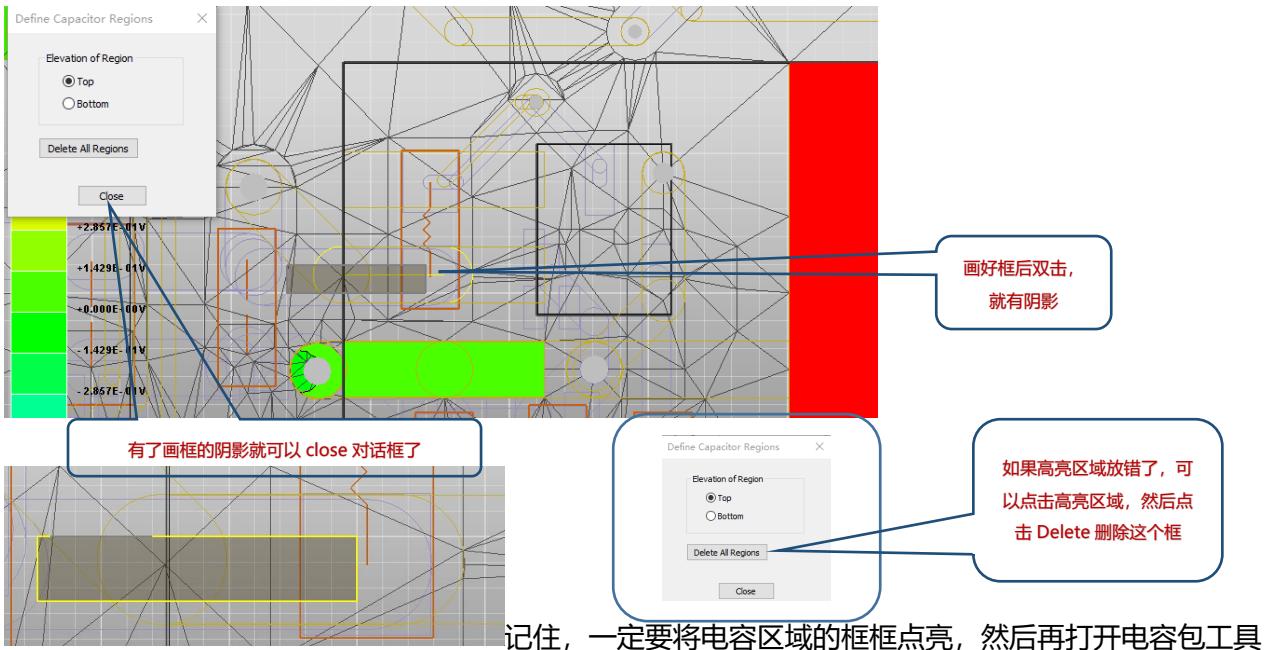
查看 Results 的 SYZ 报告

Z-parameter Plot

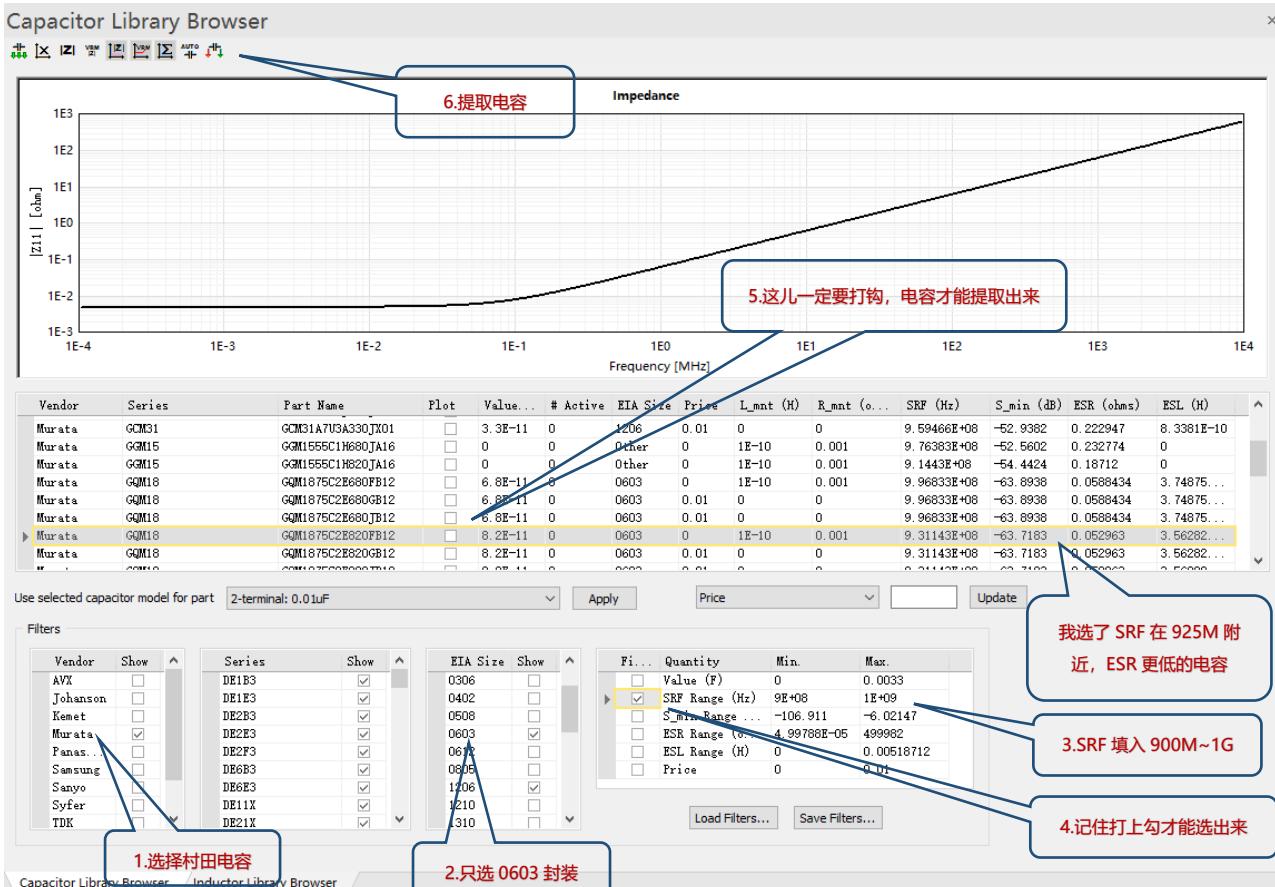


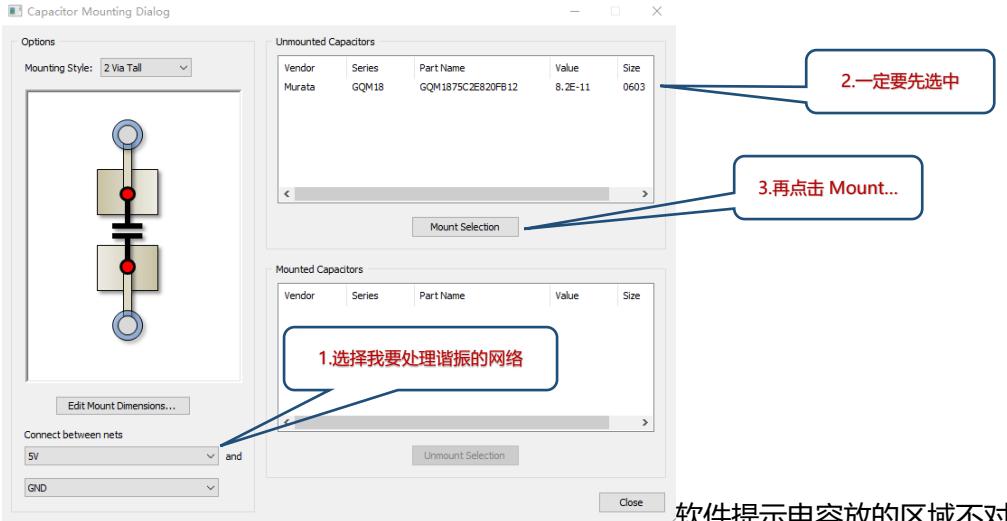
知道了频率谐振点，我们就要给该区域的焊盘放补偿电容





因为我要消除的是 925Mhz 的谐振，所以我要选择一个 SRF 自谐振频率在 925M 附近的电容





软件提示电容放的区域不对

主要是我现在手上这个板子布线布满了，没有区域可以放电容了。

PCB 电源阻抗自动优化

选择我要仿真的电源

这些电源需要给哪些负载供电，我就在供电的负载上面
选择 Port，我现在仿真 phy mcu 和 1117 芯片

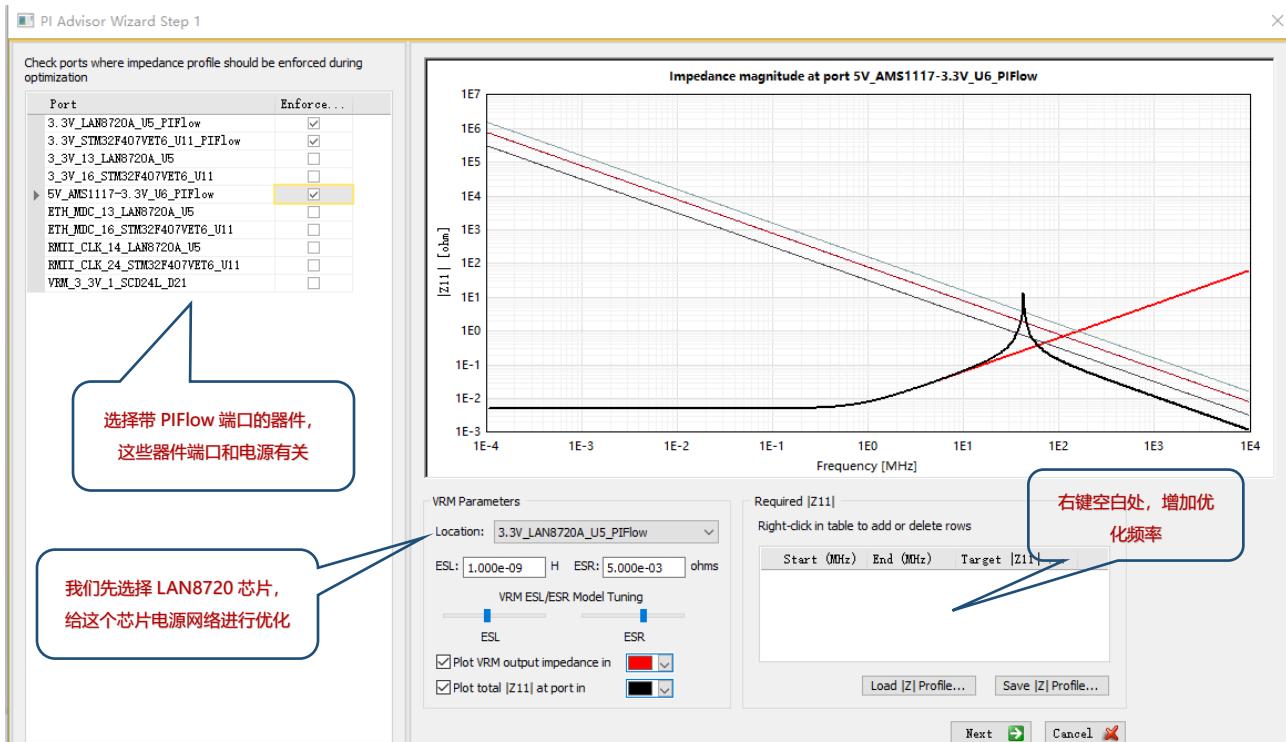
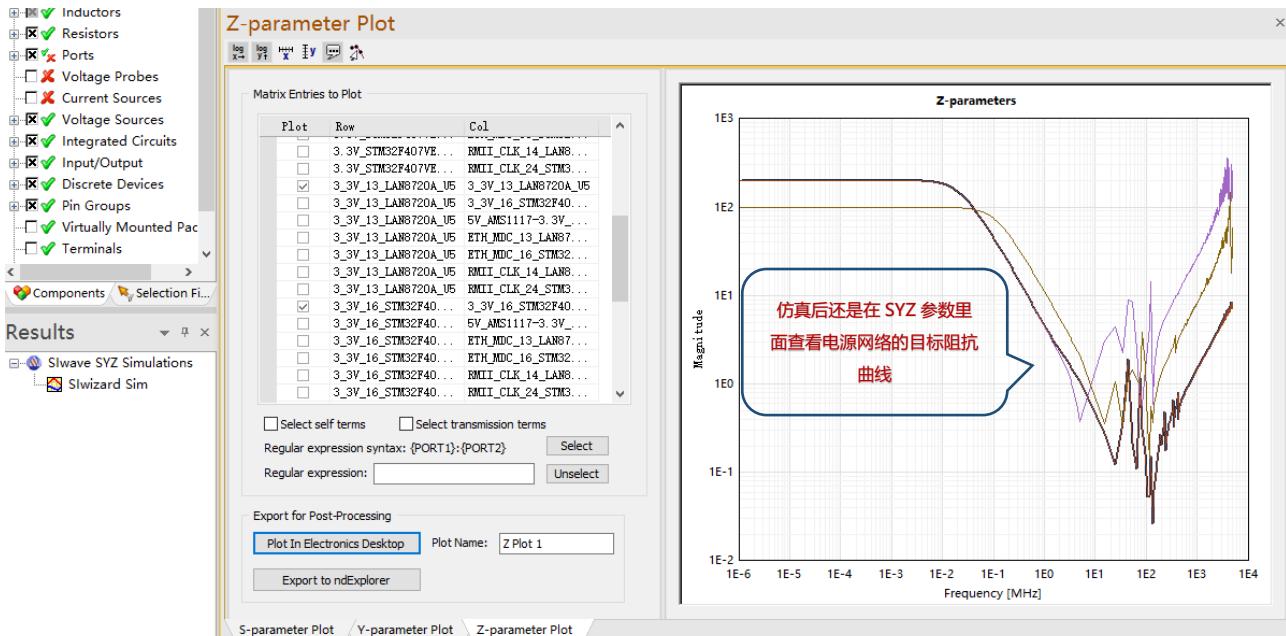
这三个选项依次点击一遍

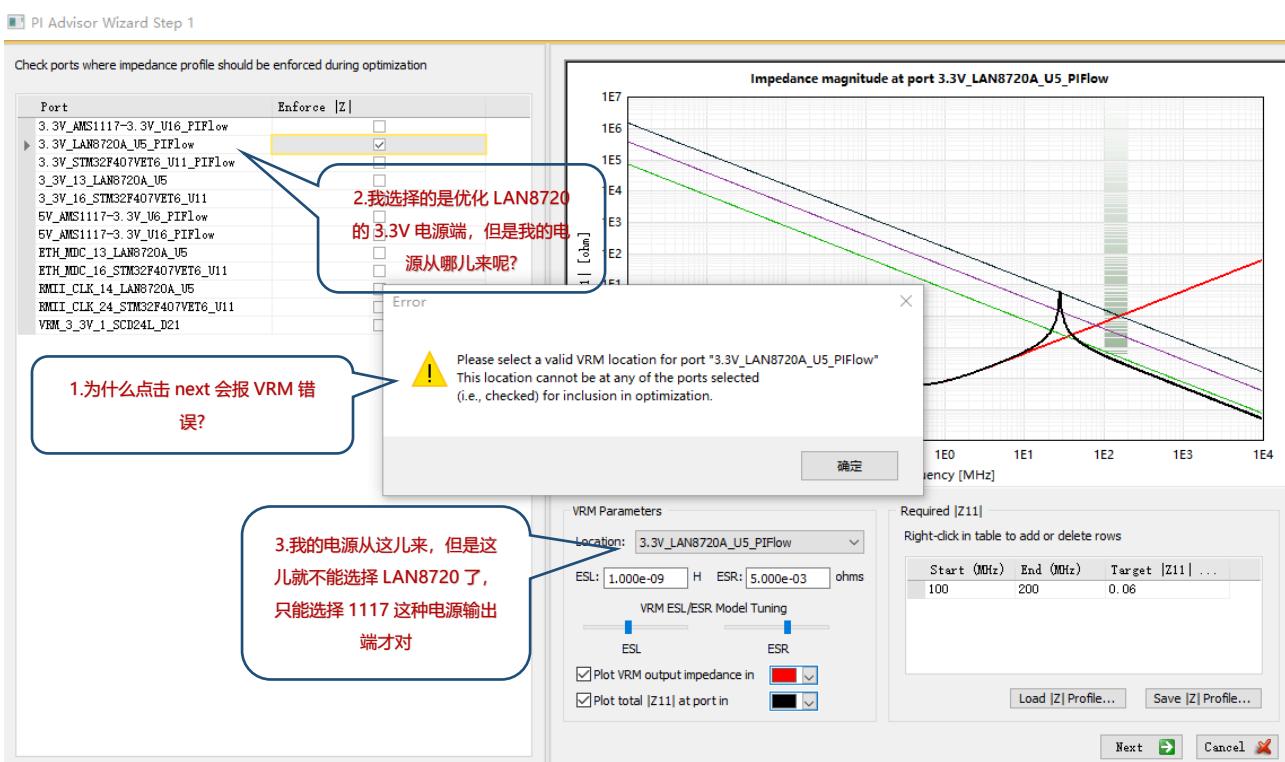
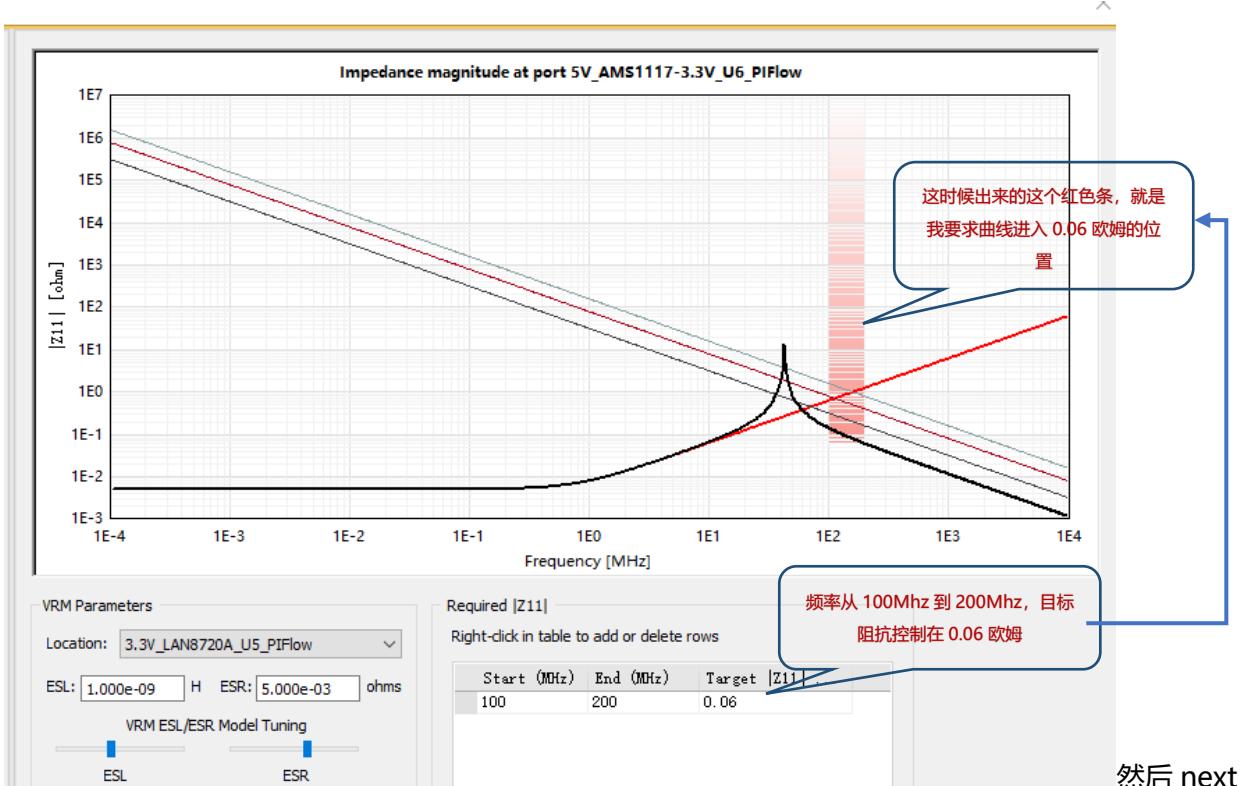
Ref. . .	Part Number	Positive Net	Reference Net	Port	Ref. . .
3.3V	1K4001	5V	NetD9_1	None	
5V	1K4001	5V	NetD10_1	None	
GND	1K4001	5V	NetD11_1	None	
3.3AV	1K4001	5V	NetD12_1	None	
3V	1K4001	5V	NetD13_1	None	
I2C_RESET	1K4001	3.3V	NetD17_1	None	
I2C_SCK	1K4001	3.3V	NetD18_1	None	
I2C_SDIO_D+	1K4001	3.3V	NetD19_1	None	
I2C_SDIO_D-	1K4001	3.3V	NetD20_1	None	
I2C_U_RX	1K4001	3.3V	NetD21_1	None	
I2C_U_TX	1K4001	3.3V	NetD22_1	None	
3V	1K4001	5V	NetD23_1	VBUS	None
32GN	1K4001	5V	NetD24_1	VBUS	None
32OUT	1K4001	5V	NetD25_1	VBUS	None
36V	1K4001	5V	NetD26_1	VBUS	None
36V_IN	1K4001	5V	NetD27_1	VBUS	None
A1	1K4001	5V	NetD28_1	VBUS	None
A2	1K4001	5V	NetD29_1	VBUS	None
AGND	1K4001	5V	NetD30_1	VBUS	None
AT_IN3	1K4001	5V	NetD31_1	VBUS	None

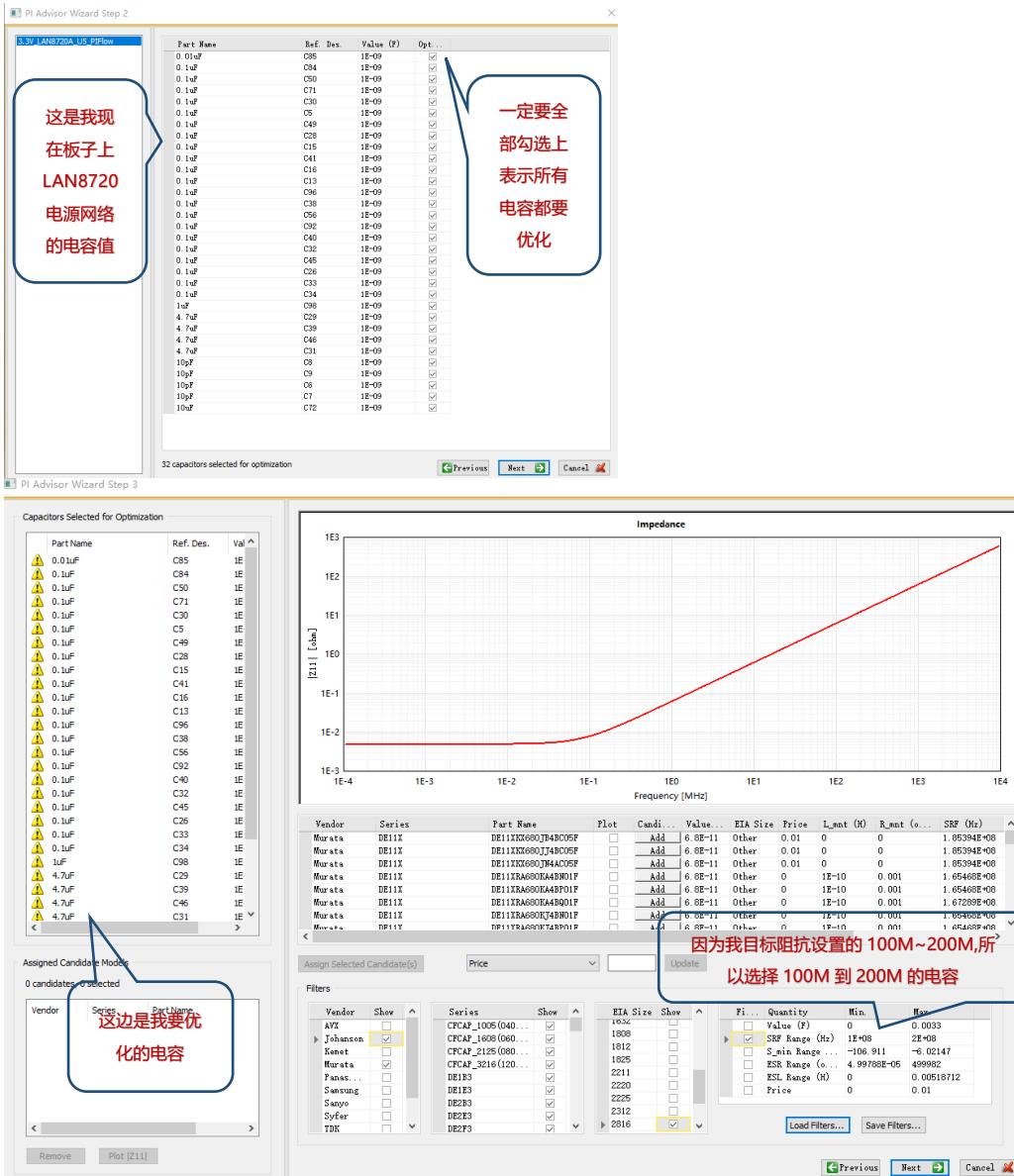
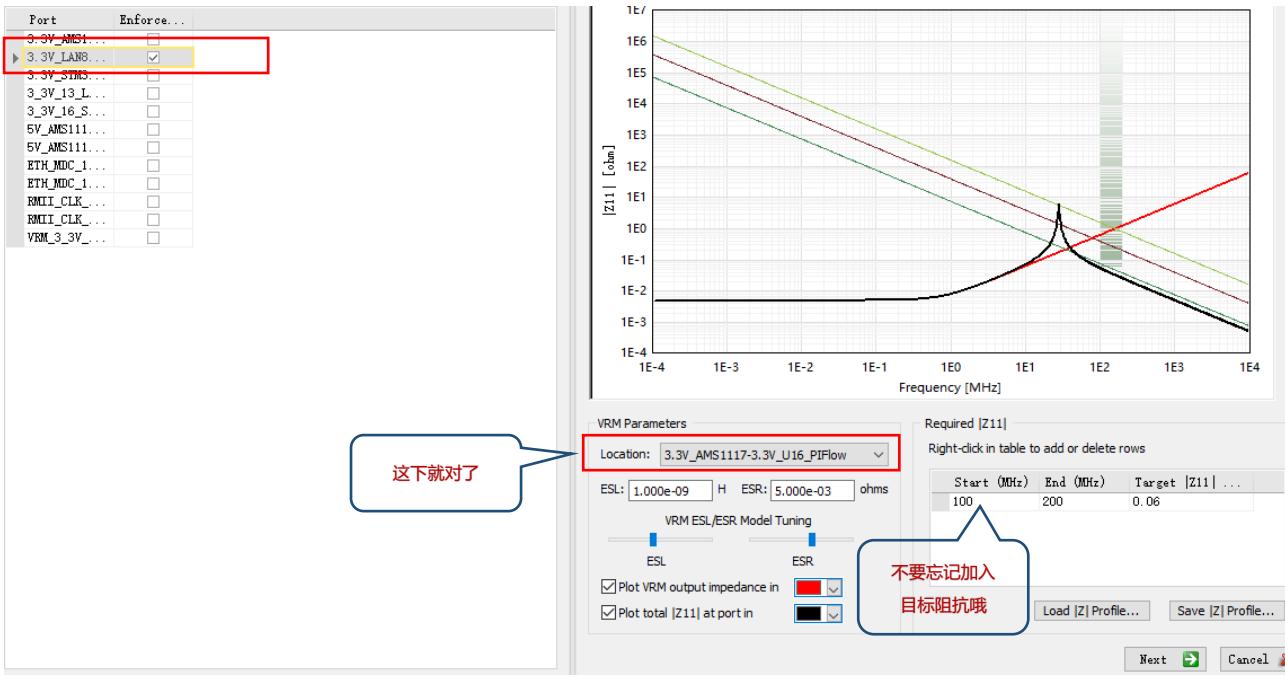
Frequency Range Setup					
	Start Freq	Stop Freq	Num. Points / Step Size	Distribution	
1	0Hz	0Hz	1	Linear	
2	1Hz	5MHz	50	By Decade	
3	5MHz	5GHz	500	Linear	

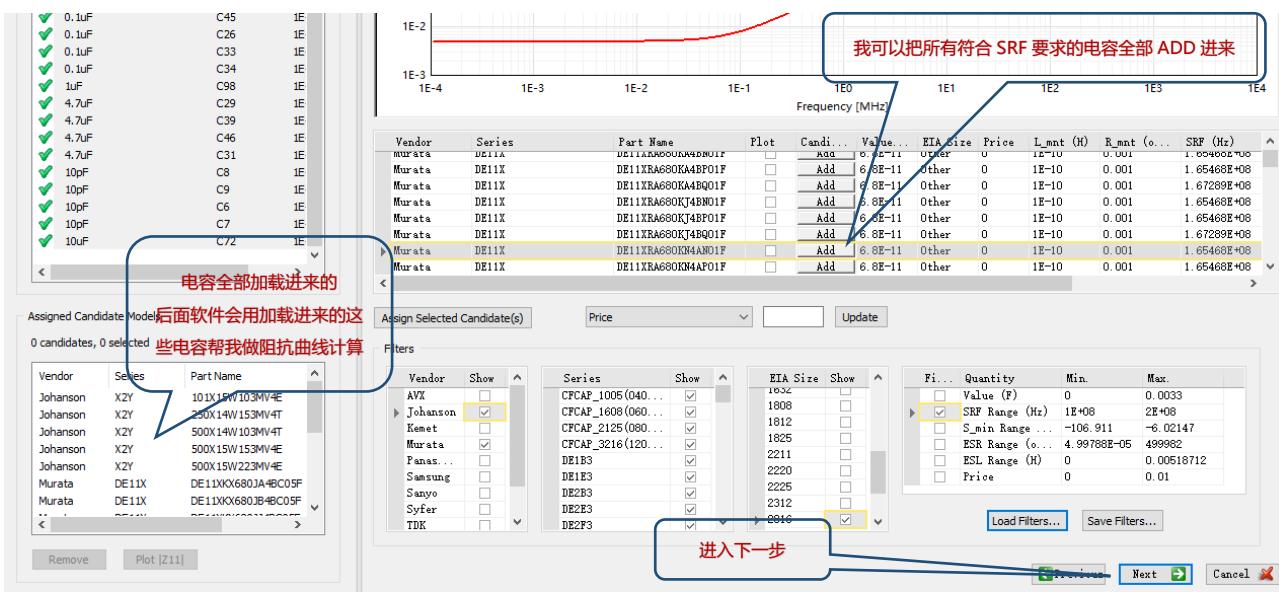
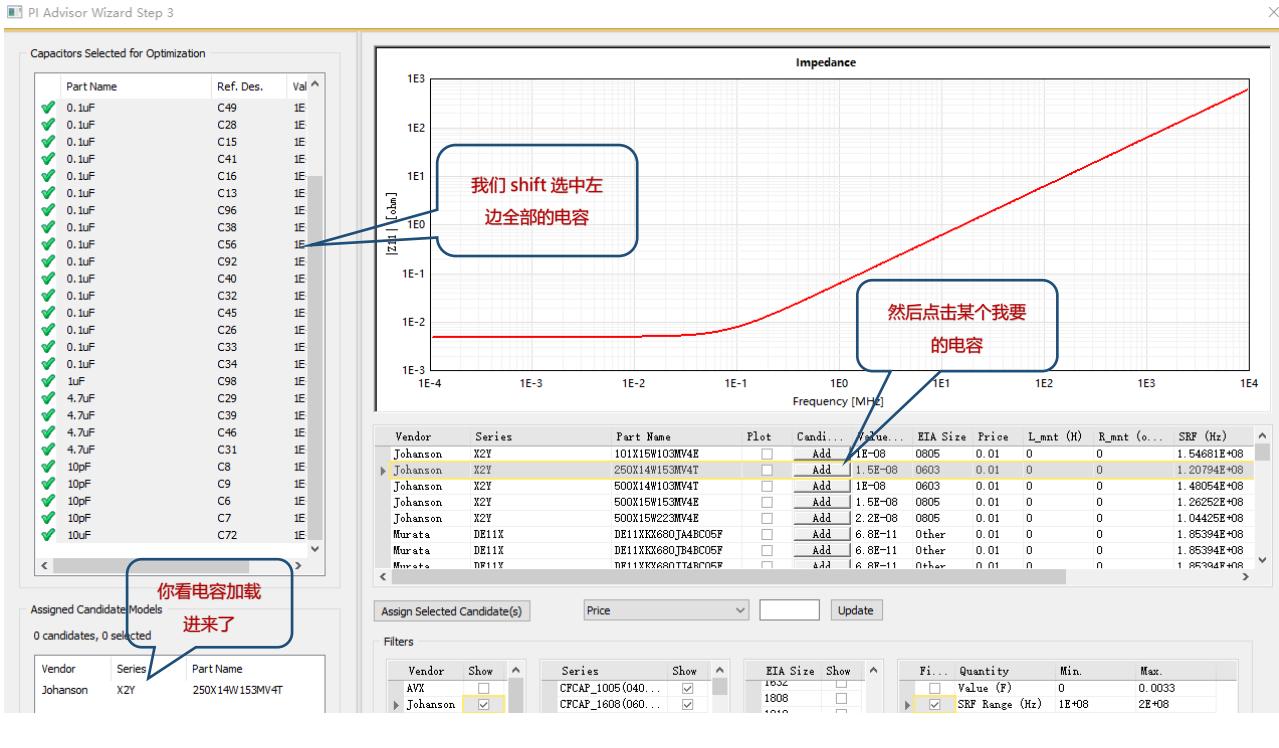
Add Above Add Below Delete Selection Preview...

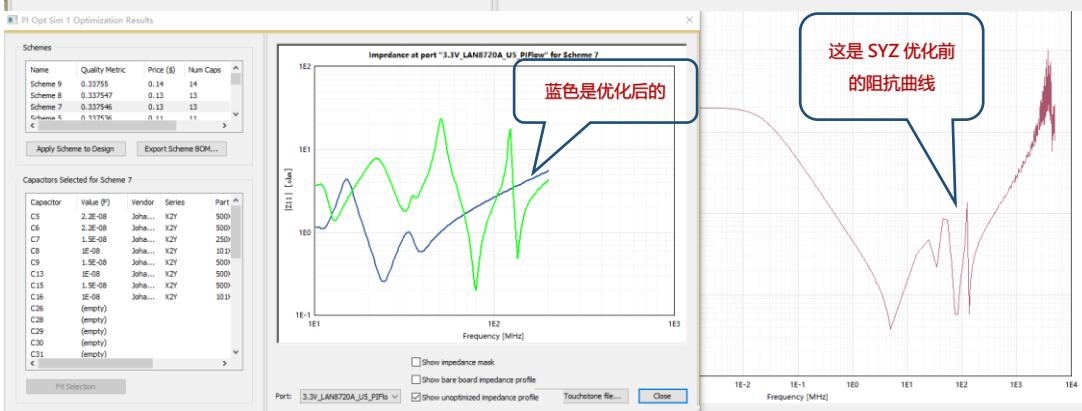
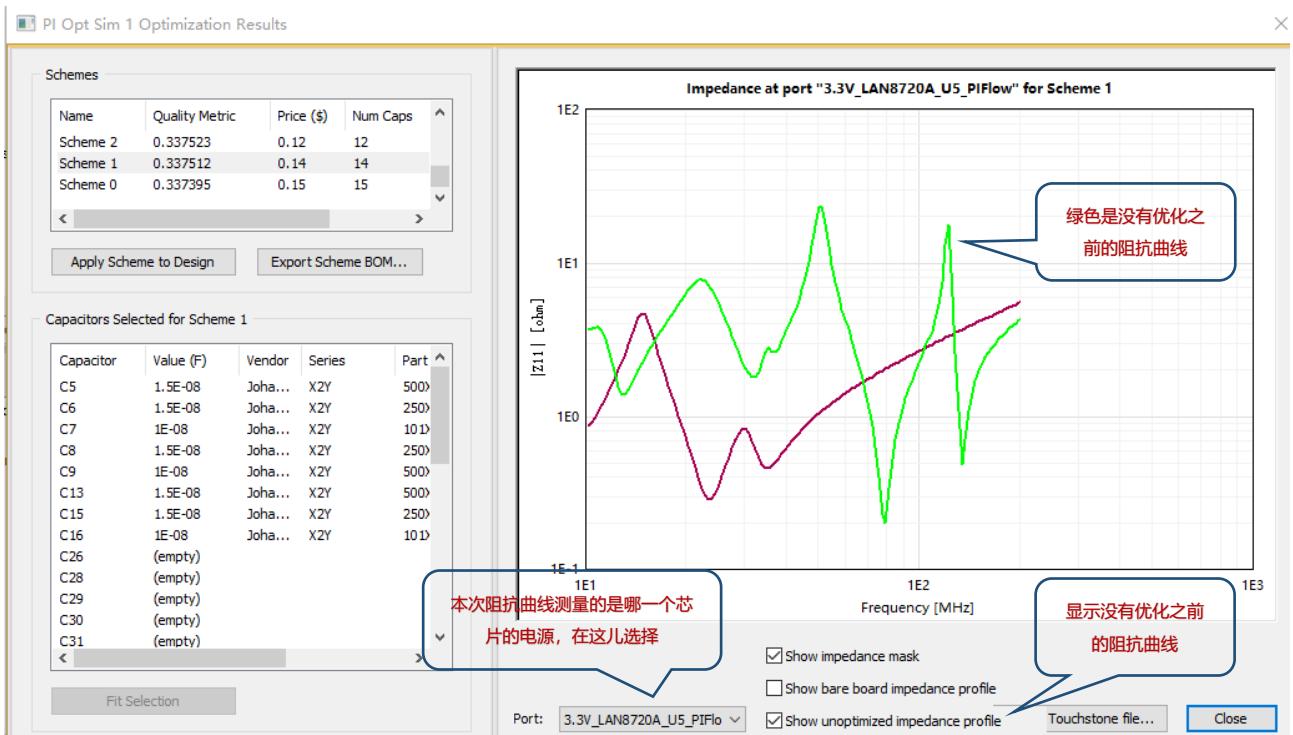
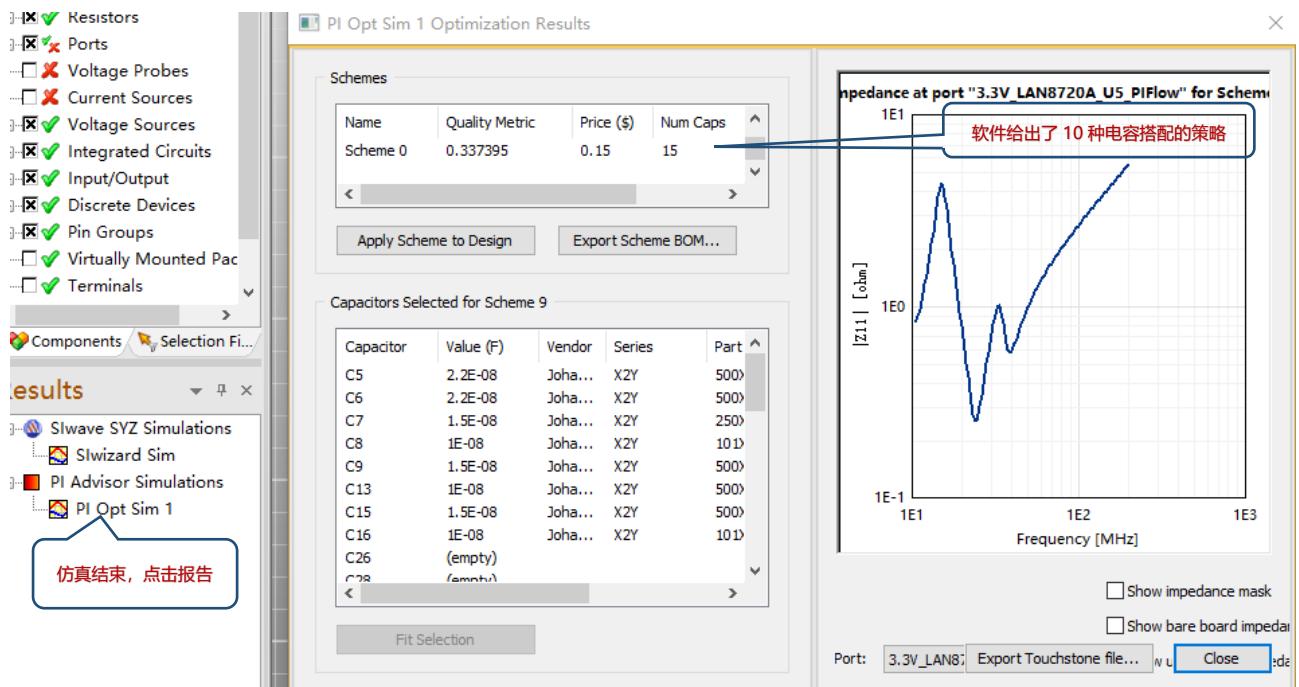
我就仿真 5M~5Ghz，点击 Launch







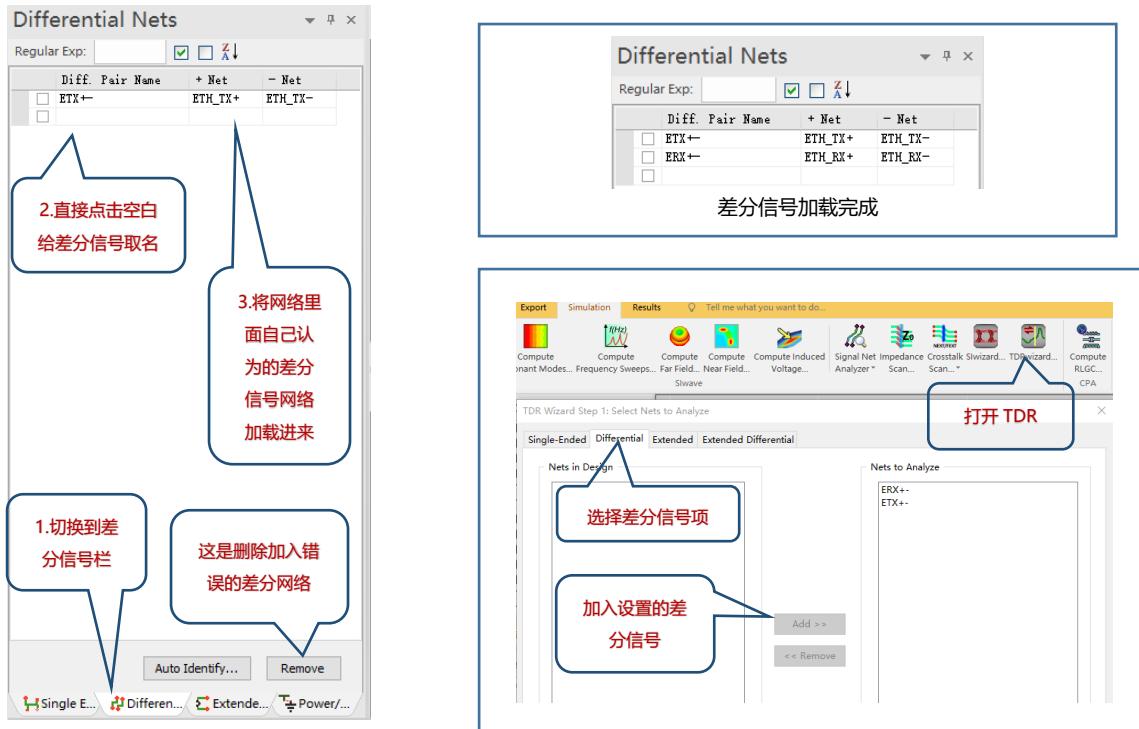




一对比就看出了明显的优化效果。

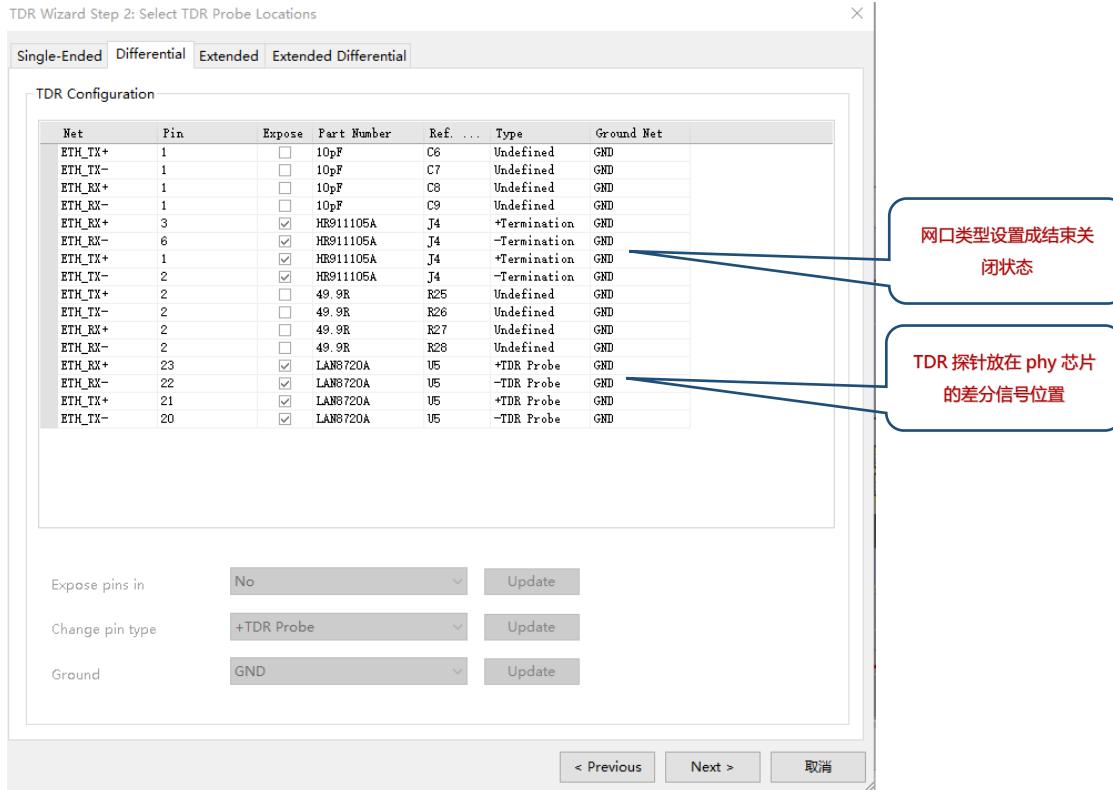
PCB 信号完整性 TDR 和 Crosstalk 仿真(测量串扰和阻抗)

如果导入的 PCB 差分信号没有自动生成，自己添加差分信号网络



TDR 测试，分析信号线的阻抗。

点击 TDR next 之后会出现警告，叫你设置差分信号类型



TDR Wizard Step 3: TDR Probe and Termination Configuration

TDR Probe Parameters

Net	Pin	Part Number	Ref. . .	Rise Time	Pulse Width	Pulse Pe... Z0	Time Delay
ETH_RX+, ETH_RX-	23, 22	LAN8720A	U5	35ps	10us	20us	100ohms 0.5ns
ETH_TX+, ETH_TX-	21, 20	LAN8720A	U5	35ps	10us	20us	100ohms 0.5ns

Red callouts:

- TDR 探针发送阶跃信号的上升沿时间是多少
- TDR 探针发送阶跃信号的脉宽是多少
- TDR 探针发送阶跃信号的周期是多少
- 差分阻抗设置多少

Rise Time: [] Update Z0: [] Update Time Delay: [] Update Pulse Period: [] Update

Termination Configuration

Net	Pin	Part Number	Ref. . .	Termination . . .	Termination Value
ETH_RX+, ETH_RX-	3, 6	HR911105A	J4	Resistor	100ohms
ETH_TX+, ETH_TX-	1, 2	HR911105A	J4	Resistor	100ohms

Type: Resistor Value: [] Update

Red callout: 网口接收端这边可以是阻性负载, 容性负载, 感性负载, 我选的阻性

< Previous Next > Cancel

TDR Wizard Step 4: Transient Simulation Options

Options

ANSYS Electronics Desktop Project Name: PCB_tdr
 Generate netlist instead of schematic

Transient Simulation Options

Step Size: 0.1ns
Stop Time: 25ns

S-parameter Options

S-parameter Sweep Configuration
Signal Net Port Reference Impedance: 50ohms
 Force S-parameter Recomputation

TDR wizard Frequency Range

Sweep

Compute exact DC point:

Frequency Range Setup

Start Freq	Stop Freq	Num. Points / Step Size	Distribution
0Hz	0Hz	1	Linear
1Hz	5MHz	50	By Decade
5MHz	14.2857GHz	500	Linear

Add Above Add Below Delete Selection Preview... Save Load Set Default Clear Default

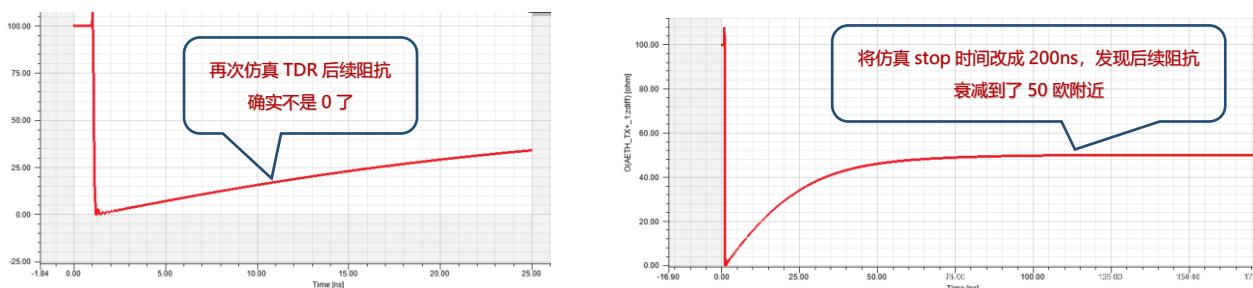
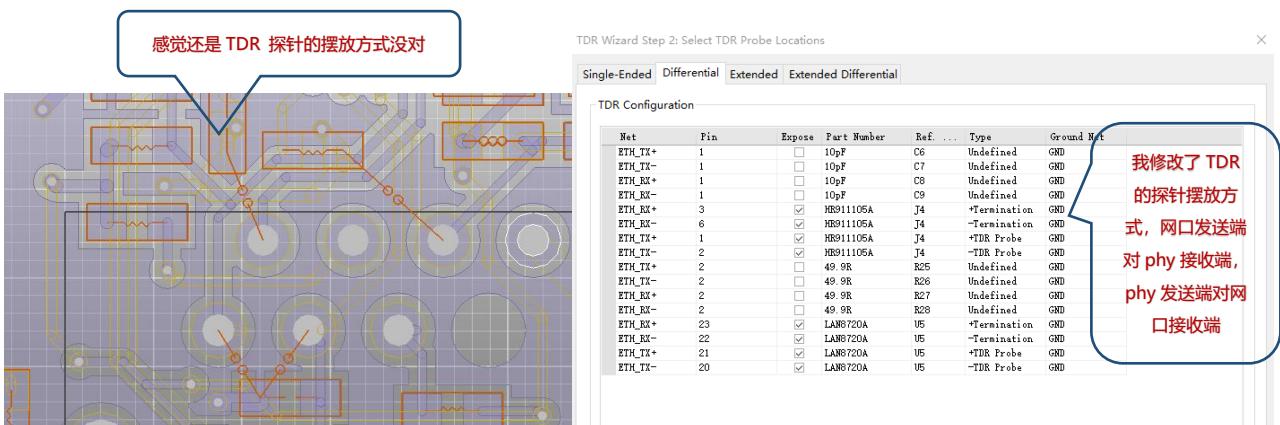
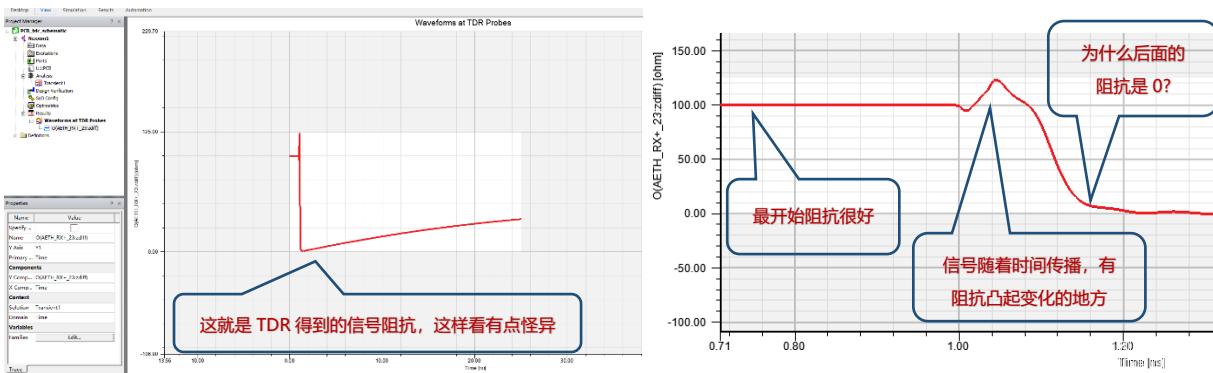
Sweep Selection

Discrete Sweep
Restore Default Sweep
Min Rise/Fall Time / s: 35E-12

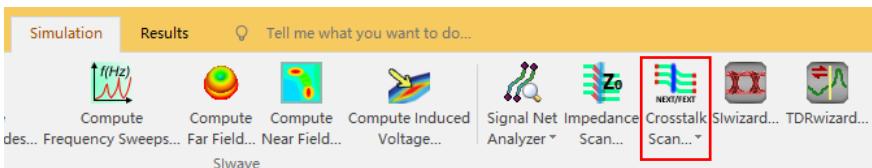
Red callouts:

- 仿真不需要生成网表
- 仿真时长一般是信号延时时间的几倍就够了, 不需要太长时间
- 这个扫频周期是根据我们 TDR 的上升/下降沿时间来得到的
- 如果我 TDR 上升/下降沿设置成 35ps, 那么系统自动就算出扫频宽度为 14.2G

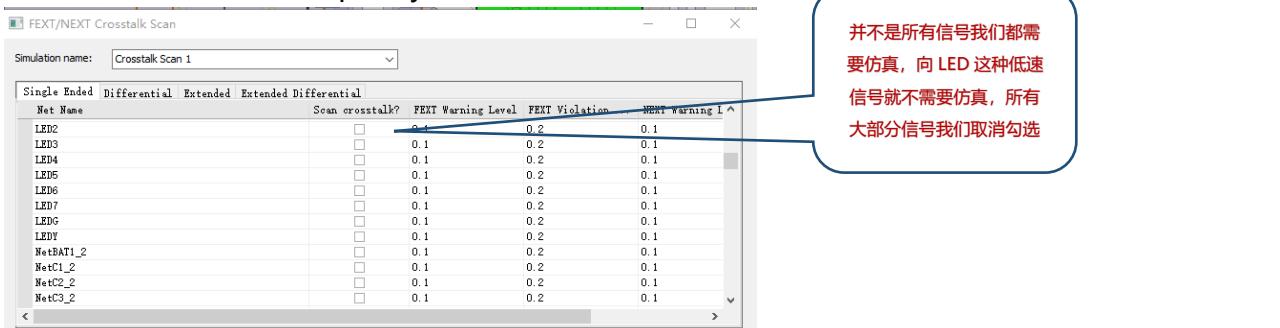
点击 OK 后就会自动仿真, 仿真完成会生成电子桌面, 情况如下

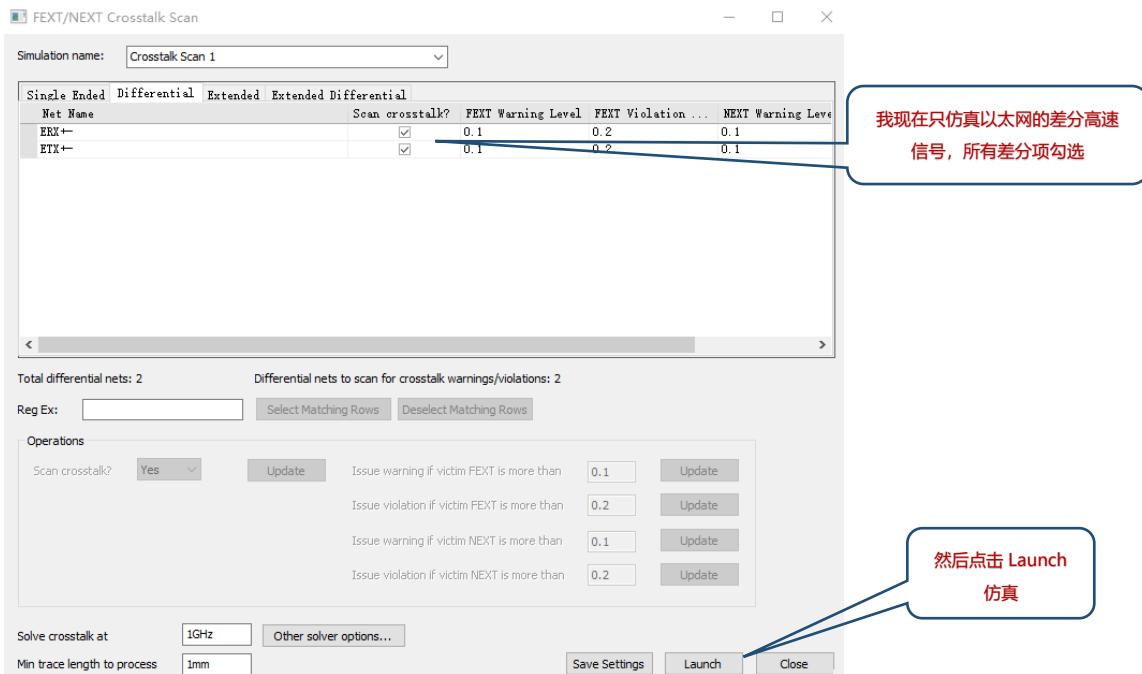


Crosstalk 仿真测试

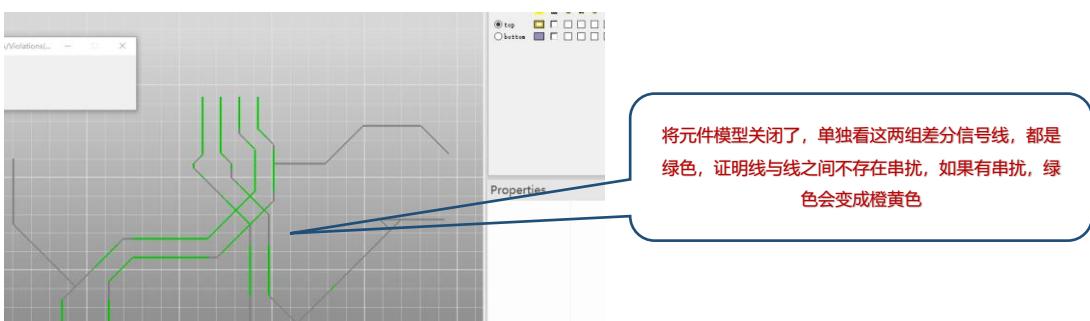
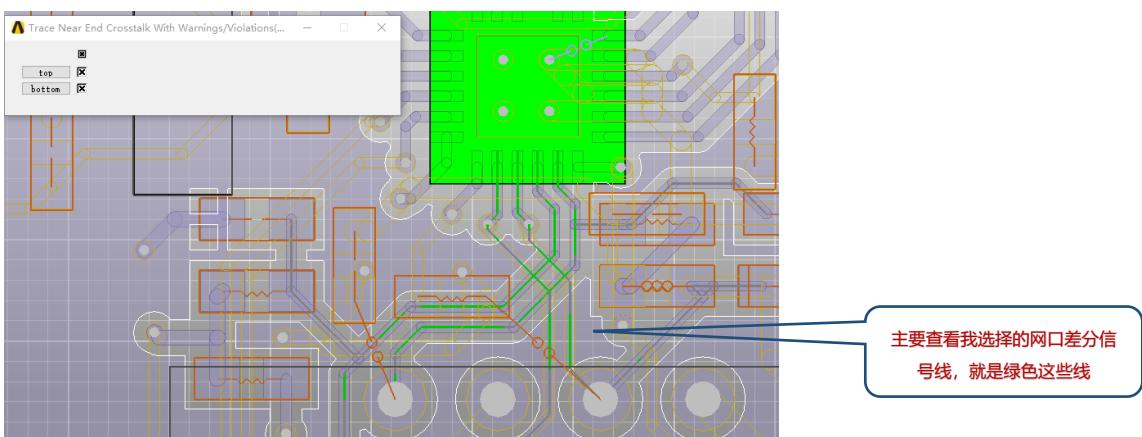
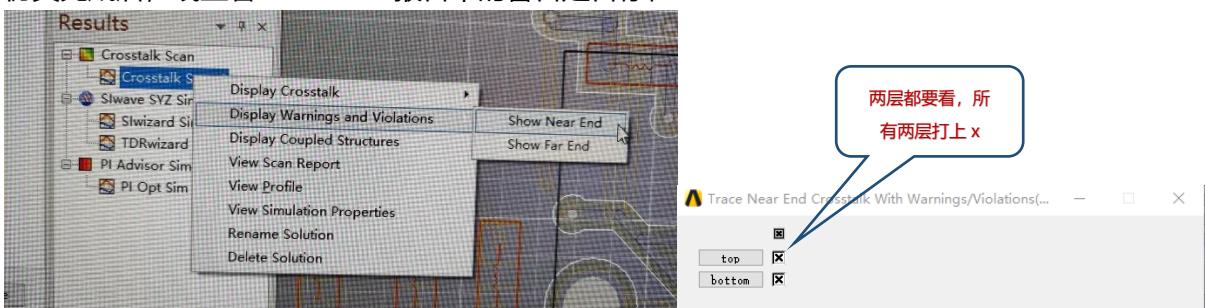


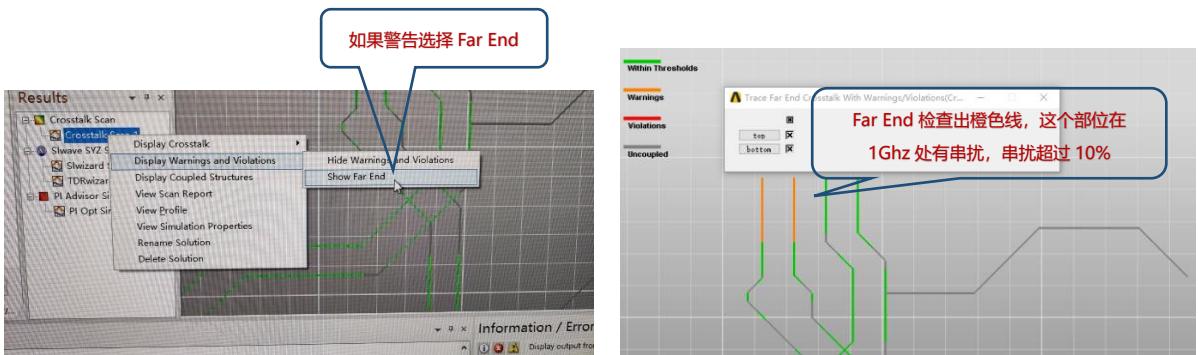
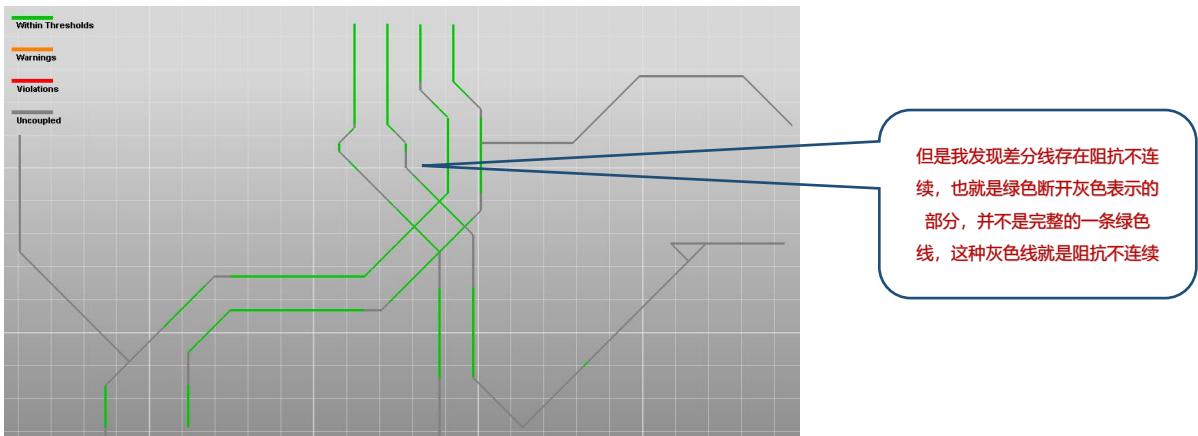
选择 CrossTalkScan->Frequency Domain 频域仿真功能





仿真完成后，线查看 CrossTalk 报告中的警告是否存在

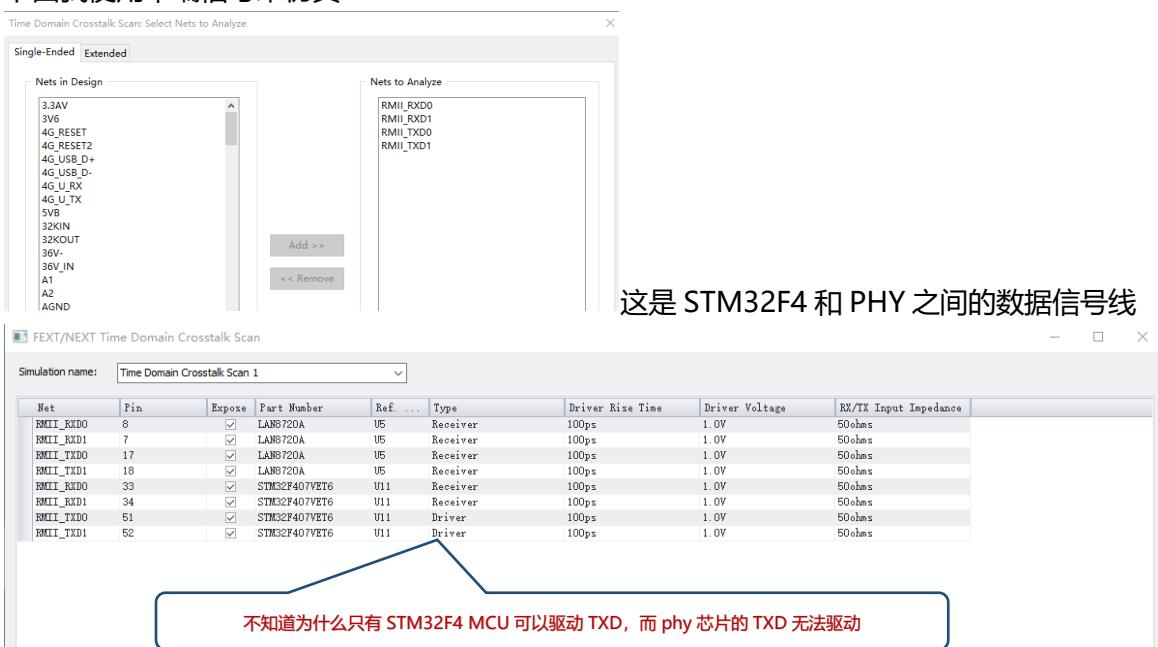




选择 CrossTalkScan->Time Domain 时域仿真,信号线之间串扰分析。

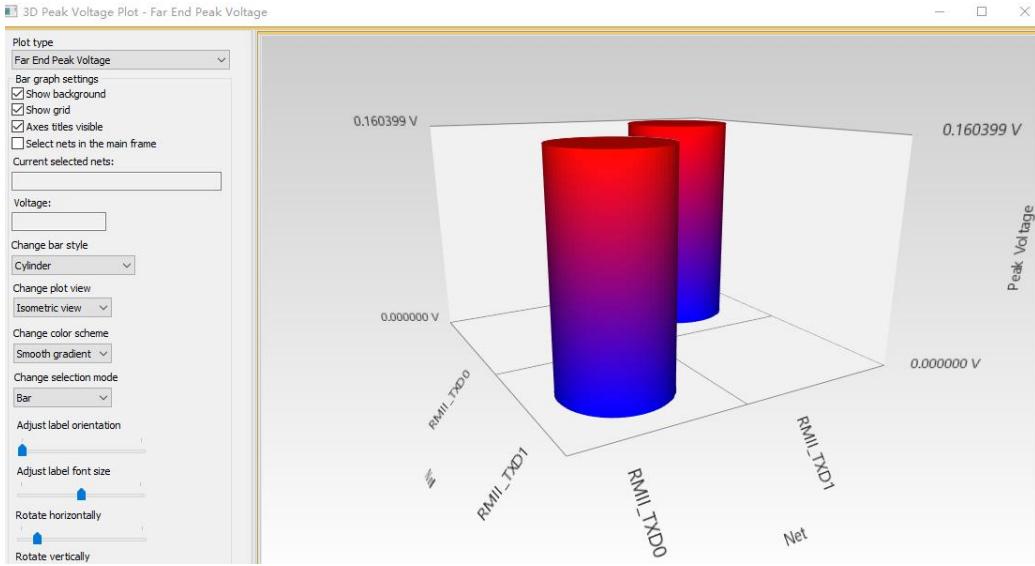


下面我使用单端信号来仿真

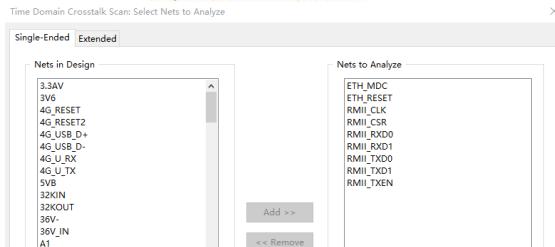
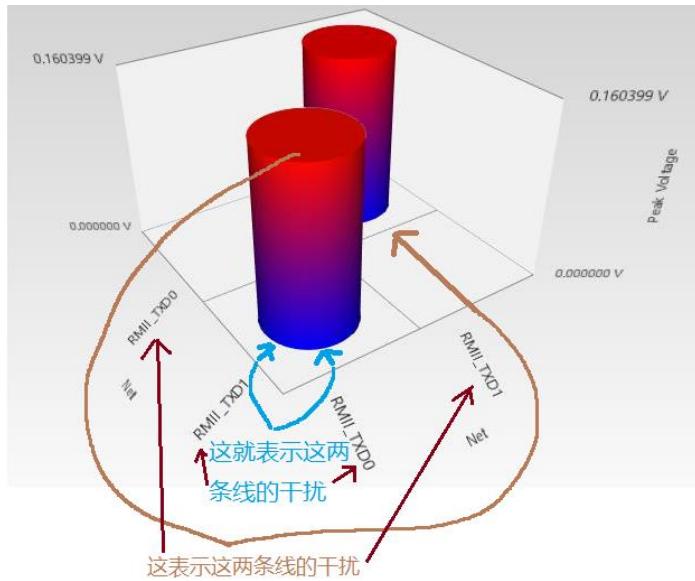




仿真完成后查看 Peak 数据



这就是表示 TXD1 和 TXD0 两条线之间的信号耦合度达到 0.1V，柱状体红色就是最大的耦合电压。怎么理解上面这种图形？看下面解释

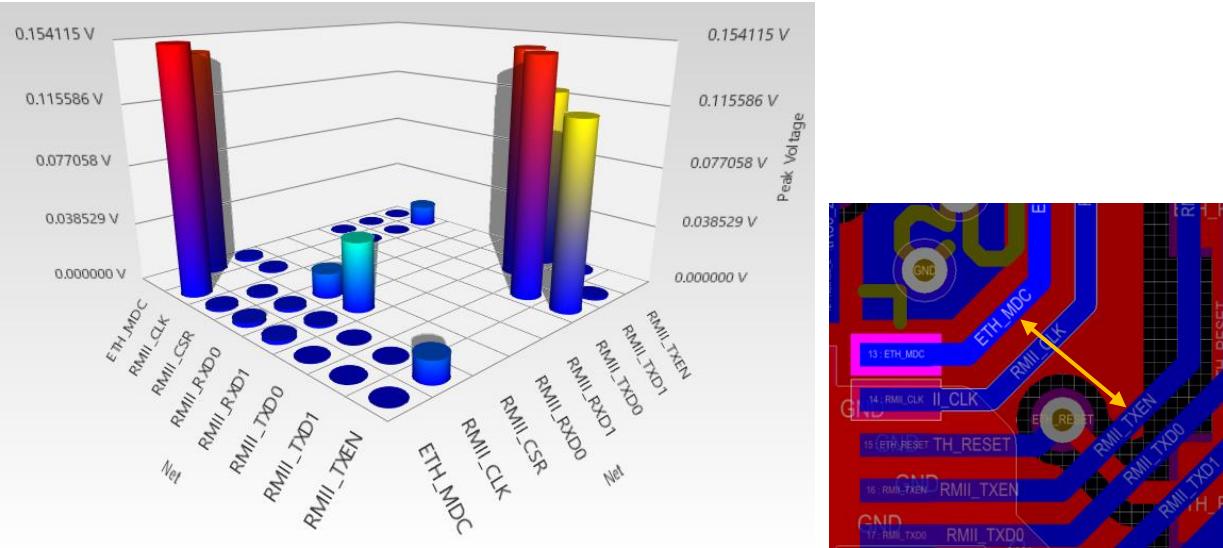


我多加几组信号线进行测试

Net	Pin	Expose	Part Number	Ref. . .	Type	Driver Rise Time	Driver Voltage	RX/TX Input Impedance
ETH_RESET	15	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
RMII_CLK	14	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
RMII_CSR	11	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
RMII_RXDO	8	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
RMII_RXD1	7	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
RMII_TXDO	17	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
RMII_TXD1	18	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
RMII_TXEN	16	✓	LAM8720A	U5	Receiver	100ps	1.0V	50ohms
ETH_MDC	16	✓	STM32F407VET6	U11	Driver	100ps	1.0V	50ohms
RMII_CLK	24	✓	STM32F407VET6	U11	Driver	100ps	1.0V	50ohms
RMII_CSR	32	✓	STM32F407VET6	U11	Driver	100ps	1.0V	50ohms
RMII_RXDO	33	✓	STM32F407VET6	U11	Receiver	100ps	1.0V	50ohms
RMII_RXD1	34	✓	STM32F407VET6	U11	Receiver	100ps	1.0V	50ohms
RMII_TXDO	51	✓	STM32F407VET6	U11	Driver	100ps	1.0V	50ohms
RMII_TXD1	52	✓	STM32F407VET6	U11	Driver	100ps	1.0V	50ohms
RMII_TXEN	48	✓	STM32F407VET6	U11	Driver	100ps	1.0V	50ohms

STM32 MCU
的信号线做成
驱动端

仿真后得到的串扰如下：



比如 RMII_TXEN 信号线与 ETH_MDC 信号线串扰最低,这两根线间距很大。其余网络自行分析。