The Status of Chiplets under Heterogeneous Integration Technology

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***Abstract*— With the development of technology in the semiconductor industry, Chiplets have been proposed and become increasingly important, aiming to solve the problem of rising costs and design difficulties caused by technological processes. This technology is a heterogeneous integration technology that combines chips manufactured at different process nodes and reuses them in different projects. In this review, we reviewed the current situation, key technologies needed in practical applications, and challenges faced in the small chip industry, and made prospects.**

***Index Terms*—Chiplets, *Heterogeneous Integration*, Interface, Packaging**

I. Introduction

In recent years, the development of semiconductor fields has seen a slowdown in Moore' law and the nodes technology. The reason is that no longer applicable due to the limitation of the production technology and its cost. As the semiconductor manufacturers, control final cost is the necessary. As transistors continue to shrink and reach physical limits, it becomes challenging to improve single-chip performance. Chiplets allow for specialized components like CPU cores, GPU cores, memory, and accelerators to be combined in a modular fashion, enabling better performance scaling.

To meet the requirements of advanced devices, chip level and substrate level scaling have been used [1], so chiplets have emerged as a result.

The application of chip level heterogeneous integration, also known as chiplets technology, is a promising solution to address this node size limitation. Chiplets are small integrated circuit chips with special functions, designed to be combined to form larger integrated circuits in accordance with the trend of heterogeneous integration in the semiconductor industry [2].

Chip makers would want to cut any corners they can find and then chiplets could help them achieve goals which is the first advantage with Chiplets. The reason is that Chiplets are smaller than monolithic design chip, so that when cutting on the silicon wafer, the loss of the wafer can be minimized as much as possible. With the continuous upgrading of technology, the cost of a single wafer is also significantly increasing [3].

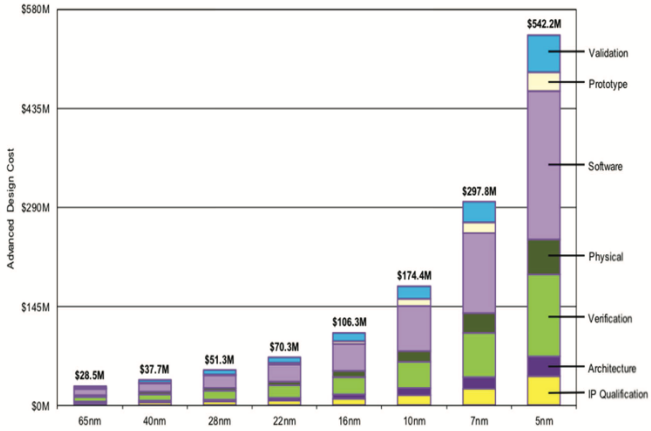

Fig. 1. Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS [3]

In such a scenario, Multi-Chip Package (MCP) packing technology is very important in the process of packaging for Chiplets which proposed in 1980s [3]. MCP technology combine multiple chips on substrate, however it focuses on the underlying packaging technology and does not figure out the problems on heterogeneous integration of chip such as interfaces and tools.

For achieve the problems on heterogeneous integration of chip, the Open Compute Project (OCP) mainly promoted by Facebook. The die integrated in Chips could interoperate to support the flexible combination from different vendors.

II. Interface

Choosing the appropriate interface technology is a crucial challenge to connect many small chips together. If the performance and type of the interface cannot match well, it will cause a loss of overall chip performance.

A. Serial

There are currently many interface methods, such as LR/MR, which are commonly used for long-distance communication, such as Ethernet and PCIE. Unlike the previous few, USR Serdes focus on die-to-die transmission through 2.5D/3D packaging technology which provide fast speed. It is also due to the difference in packaging technology, which has a short communication distance, resulting in good performance and energy consumption of this technology.

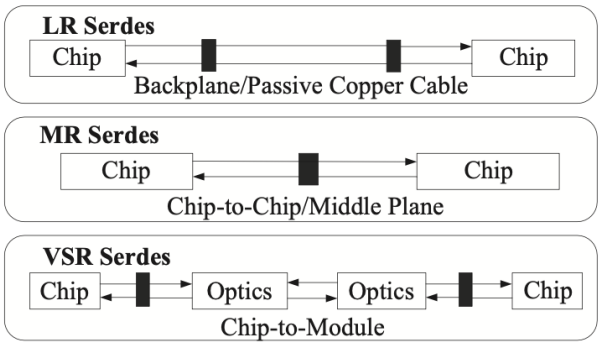

Fig. 2. Classification of Serial Interfaces [3].

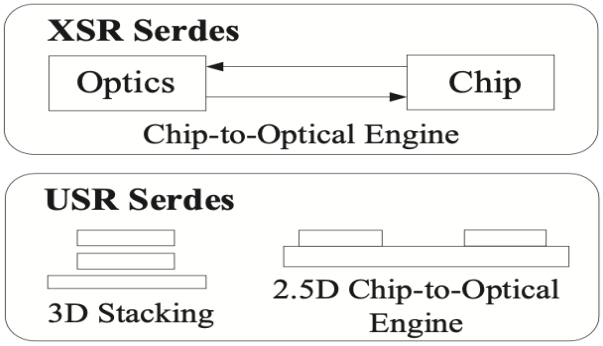

Fig. 3. Application of Serial Interfaces [3].

Based on 56 G Serdes interface specification, Table 2 shown the performance, advantages, and disadvantages between the currently type [3].

TABLE I
COMPARISONS AMONG DIFFERENT TYPES OF OIF 56 G SERDES [3].

SerDes Type	MR/LR SerDes	VSR SerDes	XSR SerDes	USR SerDes
Application Fields	Inter-chip	Chip-to-Module	Die-to-Die and Die-to Optical Engine	Die-to-Die
Transmission Medium	PCB	PCB	Substrate	Substrate or Silicon Interposer
Coding Scheme	PAM4, ENRZ	PAM4	PAM, NNRZ	NRZ
Bir Error rate	1E-4 1E-6	1E-6	1E-10 1E-15	1E-10 1E-15
Transmission Distance	500-1000 mm	125 mm/25 mm	50 mm	10mm
Power Consumption per bit	-	-	5 pJ/bit	3 pJ/pit

According to Table 1, USR SerDes obviously in not an optimal method but it is suitable method as interface technology to build the interaction between the dies since low BER and power consumption and fast speed.

B. Parallel

In the field of Chiplets, there is a distinct contrast between parallel interfaces and serial interfaces. Parallel interfaces refer to a method of connecting and communicating between Chiplets or integrated circuits, including multiple data lines that transmit data simultaneously.

In parallel interfaces, data is typically grouped into "parallel" data buses, where each bus carries a set of bits simultaneously (for example, 8 bits, 16 bits, or 32 bits). These parallel buses can be used for various purposes, including transmitting data, instructions, or control signals between components on small or larger chips [3].

The choice of parallel and serial interfaces depends on factors such as data transmission speed, power efficiency, and specific application requirements. Parallel interfaces can provide high-speed data transmission over short distances, but compared to serial interfaces, they may require more physical pins and consume more power. Serial interfaces are usually suitable for long-distance communication and can be more energy efficient.

There are four common parallel interfaces, namely AIB, MDI O, LIPINCON, and Bow Interface. The above all, all interfaces achieve a low power consumption and per-bit transmission, some characteristic same as serial interface.

None of the above interfaces can adapt to all situations, and the best communication solution for small chips depends on the actual situation. In addition, serial and parallel also have their own advantages and characteristics. Parallel interfaces can provide high bandwidth based on advanced serial interfaces, but also require more resources. In summary, when designing chips, it is necessary to be flexible and flexible, and Chiplets design manufacturers should also combine actual needs to achieve maximum benefits.

III. PACKAGING

The performance, cost, and maturity of Multi-Chip Packaging (MCP) technology have a significant impact on the application of chiplets. According to different processes, the packaging technologies that Chiplets can use are mainly divided into three types: substrate-based packaging technologies, silicon interposers-based packaging technologies and RDL-based (Redistribution Layer) fan-out packaging technology [3].

At present, due to cost and other factors, organic substrates are widely used. Like traditional PCBs, organic substrate materials complete wiring connections through etching processes, which do not depend on the silicon process used in semiconductor devices. Multiple tube cores can be high-density connected to the substrate through wire bonding or flip chip technology. But most of the pins of the chip are occupied by the power supply, which limits the transmission bandwidth of the die-to-die connection and affects the development of smaller chips with higher performance.

The 2.5D/3D packaging technologies are mainly in the form of silicon interposer-based packaging technology, but this technology bring the higher cost in materials.

To improve the cost control problem of the silicon interposer-based packaging method, substrate-less fan-out packaging technology packaging technology has been proposed, which based on the redistribution layer (RDL) deposits metal and dielectric layers on the surface of the wafer. Since in fanout packaging technology, RDL can improve signal quality by shortening circuit length and improve the integration of small chips by reducing chip area.

TABLE II
COMPARISONS AMONG DIFFERENT TYPES OF OIF 56 G SERDES [3].

Packaging Technology	Packaging Technology	Silicon Interposer-Based	RDL-Based Fan-Out
Integration density	Low	High	Middle
Integration density Performance	Low	High	High
Routing Dispersion	Highest	Higher	Middle
Heat Dispersion	Middle	Middle	High
Cost	Low	High	Middle
3D Extensibility	Low	Middle	High
Provider	Chip Packing Test Factory	Chip Foundry	Packaging Test Factory/Foundry/Integrated Device Manufacturer

IV. APPLICATION

Chips provide flexibility, scalability, and performance advantages in various applications, making them a universal solution for modern semiconductor design and integration. Their modular characteristics allow for the combination of different small chips to meet the specific requirements of different industries and use cases.

In practical application, AMD chips are a good example. Not all constituent departments require high performance, so maker can save money by making it a separate chip which is AMD did for example the Ryzen 7000 processor chips are based on a new 5 nanometers process node whereas the IO chip in them is based on a cheaper 6 nanometers node.

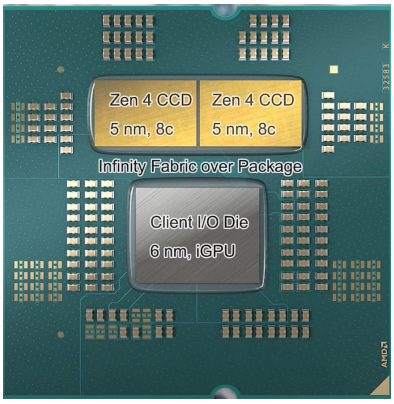

Fig. 3. AMD Ryzen 7000 processor chip

V. CONCLUSION

This article briefly introduces the concept and development of Chiplets technology, as well as why small chips can be given special attention.

With the development of technology, the price of advanced technology wafers is becoming increasingly expensive. Analyzing the cost reasons for the development of Chiplets from the perspective of manufacturers. Chiplets also have many advantages, improving system flexibility and accelerating design speed while controlling costs. However, there are still some choices and challenges in interface and packaging, and more research should be conducted on related technologies, such as interconnection and packaging, to simplify the complexity of system integration and achieve higher performance, lower power consumption, and higher regional efficiency. At present, AMD and other companies have truly applied Chiplets to actual production and sales, which is a trend. With the development, more and more companies will start to apply Chiplets technology. The prospects of this field are very broad, so corresponding supporting facilities must be upgraded.

REFERENCES

[1] S. P. Lim, M. D. Rotaru, W. Seit and H. H. Yao, "Assembly Challenges and Approaches for 2.5D Chiplet Based System," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 132-138, doi: 10.1109/ECTC51909.2023.00031.

[2] G. L. Gao *et al.,* "Die to Wafer Hybrid Bonding for Chiplet and Heterogeneous Integration: Die Size Effects Evaluation-Small Die Applications", 72nd ed., San Diego, USA, 1981, pp. 1975, 1981.

[3] T. Li *et al.,* "Chiplet heterogeneous integration technology—Status and challenges," *Electronics.*, vol. 9, no. 4, 2020