EECS151/251A
Introduction to Digital Design and ICs

Lecture 9:
RISC-V Datapath and Control II

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AMD Acquires Xilinx

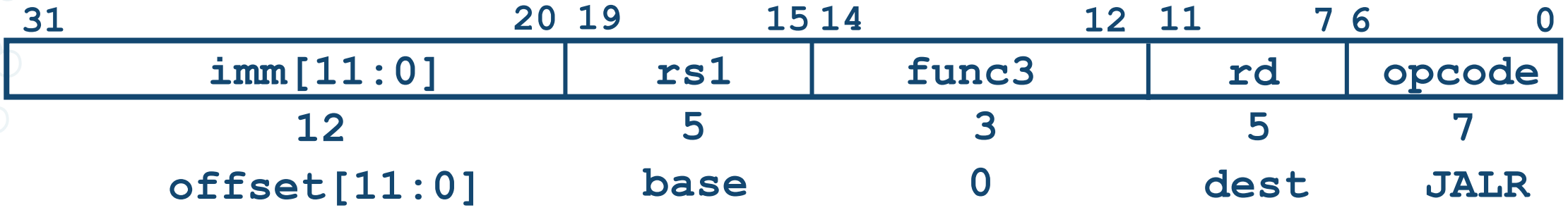
Over the next decade, high-performance computing will be at the center of nearly every major trend shaping the future. Whether in the cloud, at the edge or across the growing number of intelligent end devices — there is an increasing need to push the envelope to enable new experiences and services. While CPUs and GPUs will remain critical engines for those devices, in a world where algorithms are always advancing and new standards are continually emerging, we see demand growing for adaptive computing capabilities that will be critical to accelerate these emerging and evolving workloads.

AMD's acquisition of Xilinx creates the industry's high-performance and adaptive computing leader, combining a highly complementary set of products, customers and markets with differentiated IP and world-class talent. As we bring AMD and Xilinx together, there are considerable product, technology, market and financial benefits.

https://www.amd.com/en/corporate/xilinx-acquisition

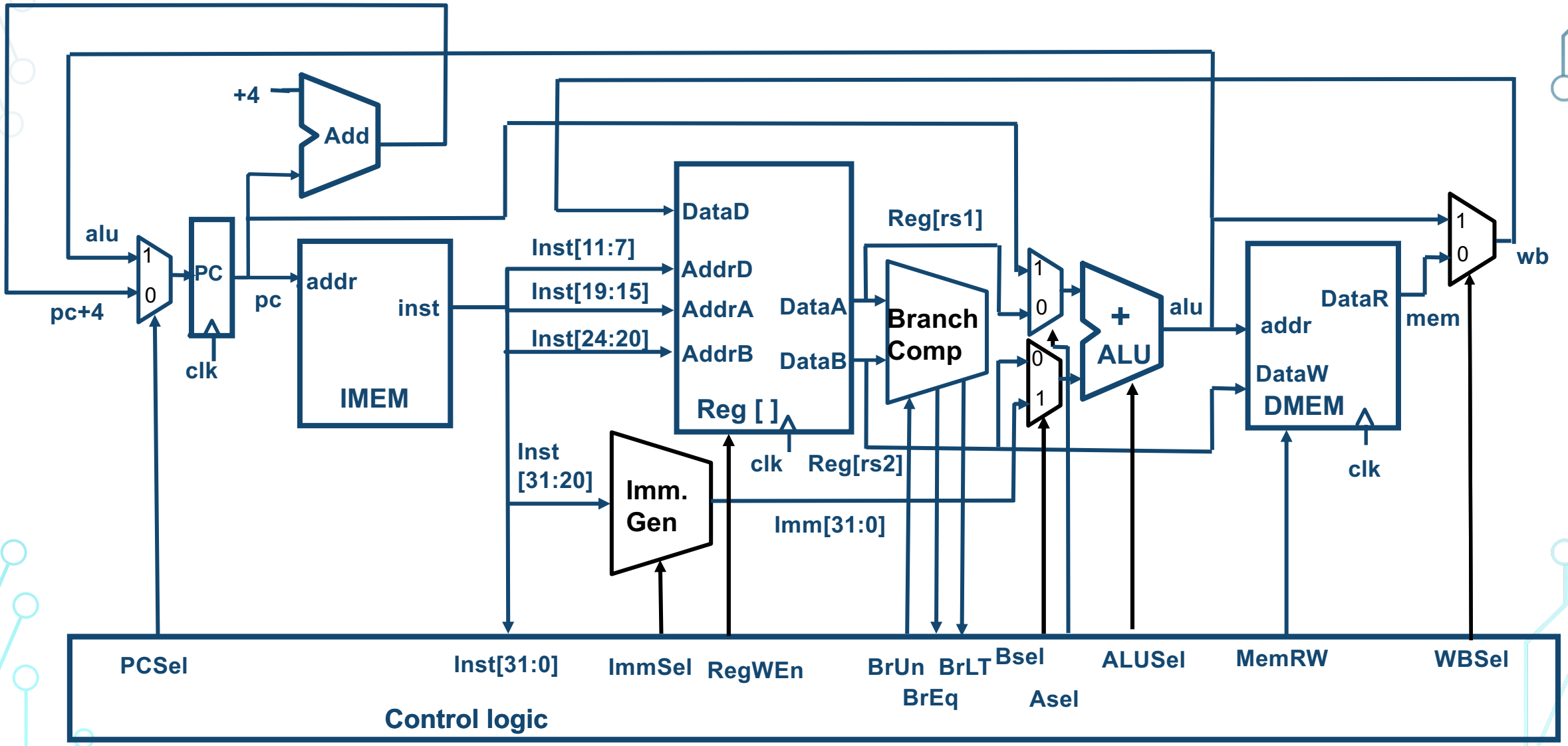
- RISC-V Datapath & Control
  - R-type
  - I-type
  - S-type
  - B-type
  - J-type
  - U-type
  - Control Logic
- RISC-V 5-stage Pipeline

JALR Instruction (I-Format)

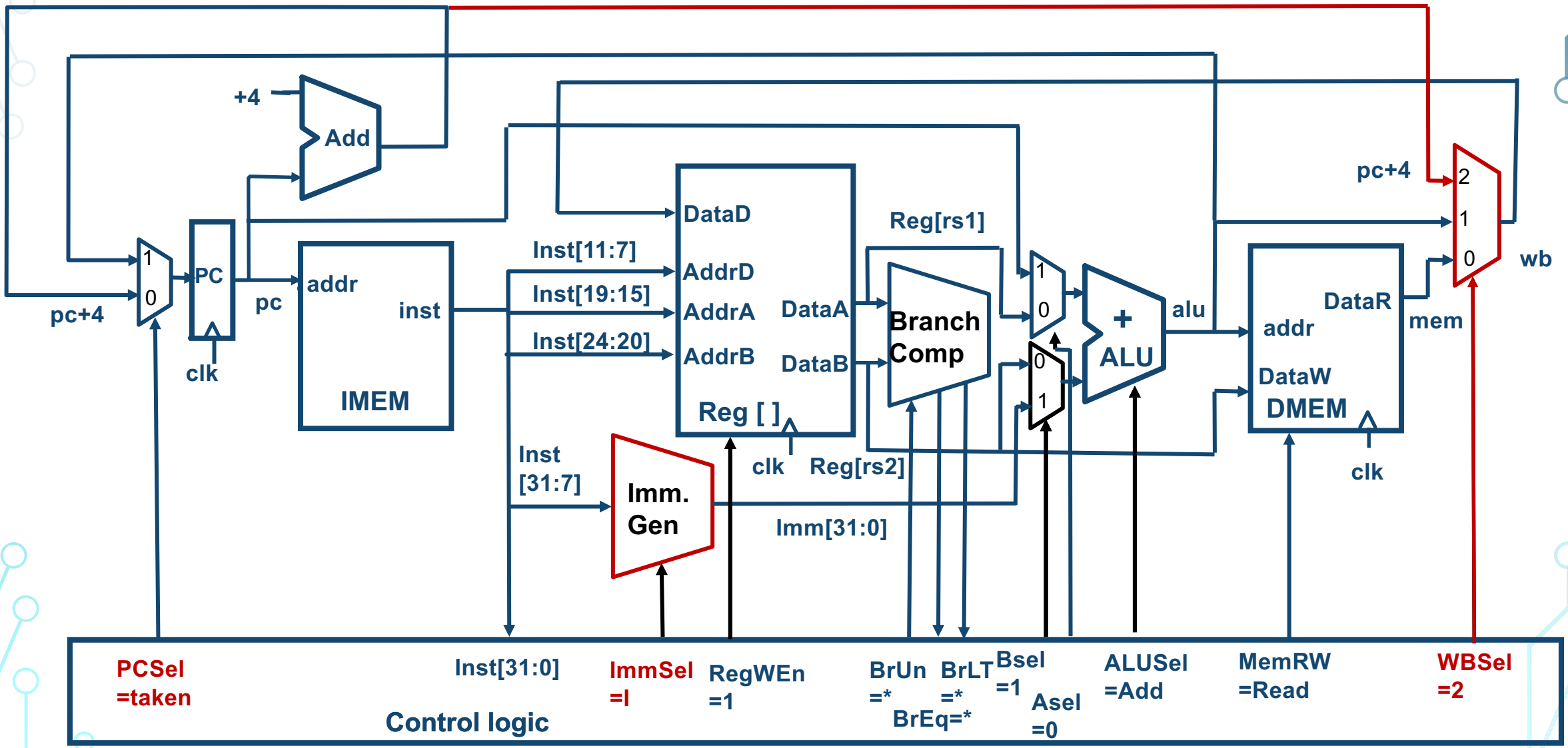


- JALR rd, rs, immediate
  - R[rd] = PC + 4; PC = Reg[rs1] + imm;
    - Writes PC+4 to rd (return address)
    - Sets PC = rs1 + immediate (and sets the LSB to 0)
  - Uses same immediates as arithmetic and loads
    - ***no*** multiplication by 2 bytes
    - In contrast to branches and JAL

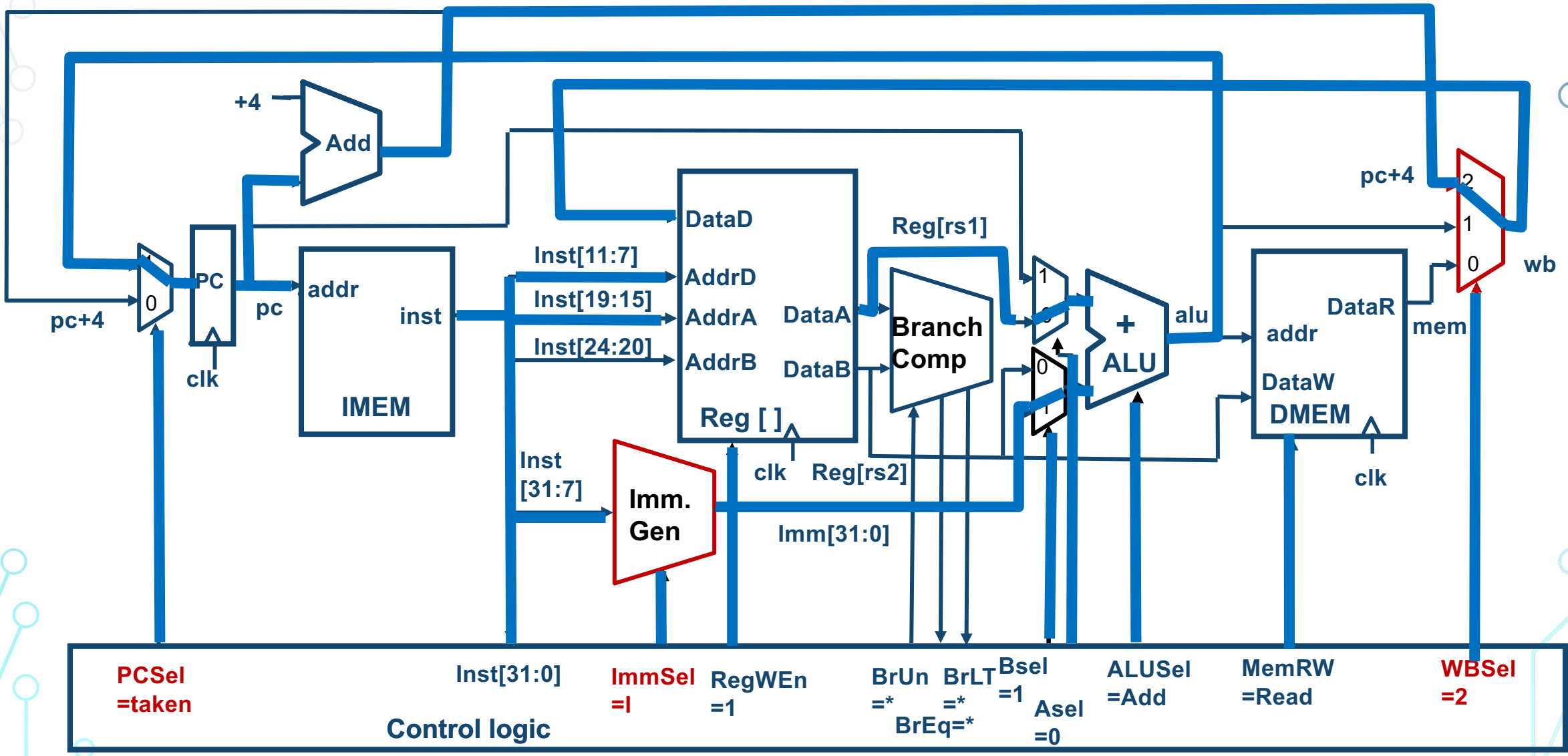
Datapath So Far, with Branches



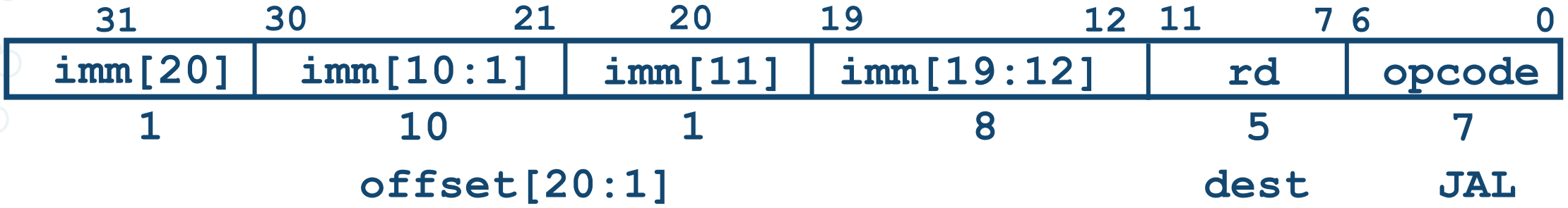
Adding JALR



Adding JALR

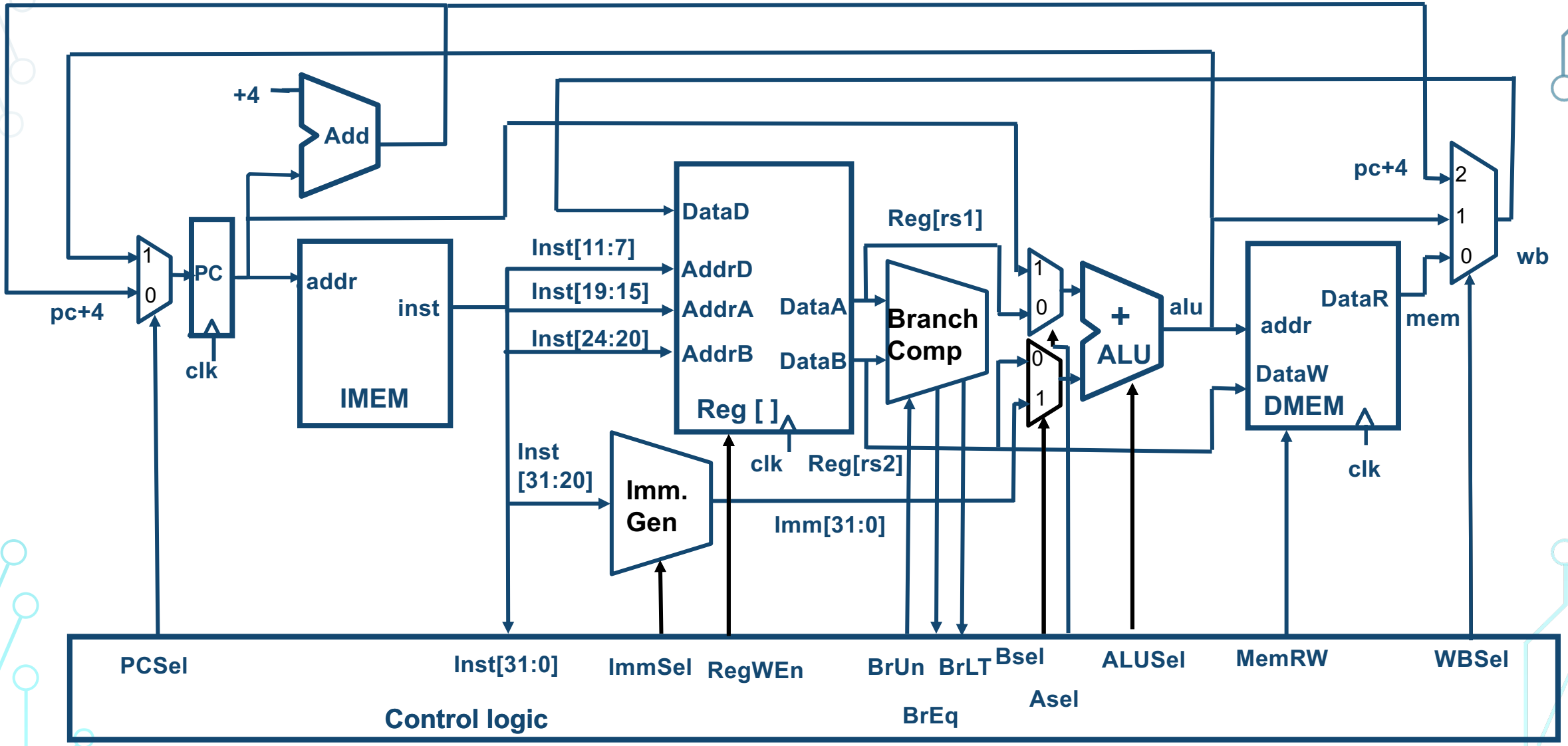

+4
Add
pc+4
0
PC
clk
pc
addr
inst
IMEM
Inst[11:7]
Inst[19:15]
Inst[24:20]
DataD
AddrD
AddrA
AddrB
DataA
DataB
Reg [ ]
clk
Reg[rs1]
Reg[rs2]
Branch Comp
1
0
+
ALU
alu
pc+4
2
1
0
wb
addr
DataR
DataW
DMEM
clk
mem
Inst [31:7]
Imm. Gen
Imm[31:0]
PCSel =taken
Inst[31:0]
Control logic
ImmSel =I
RegWEn =1
BrUn =*
BrLT =*
BrEq=*
Bsel =1
Asel =0
ALUSel =Add
MemRW =Read
WBSel =2

J-Format for Jump Instructions

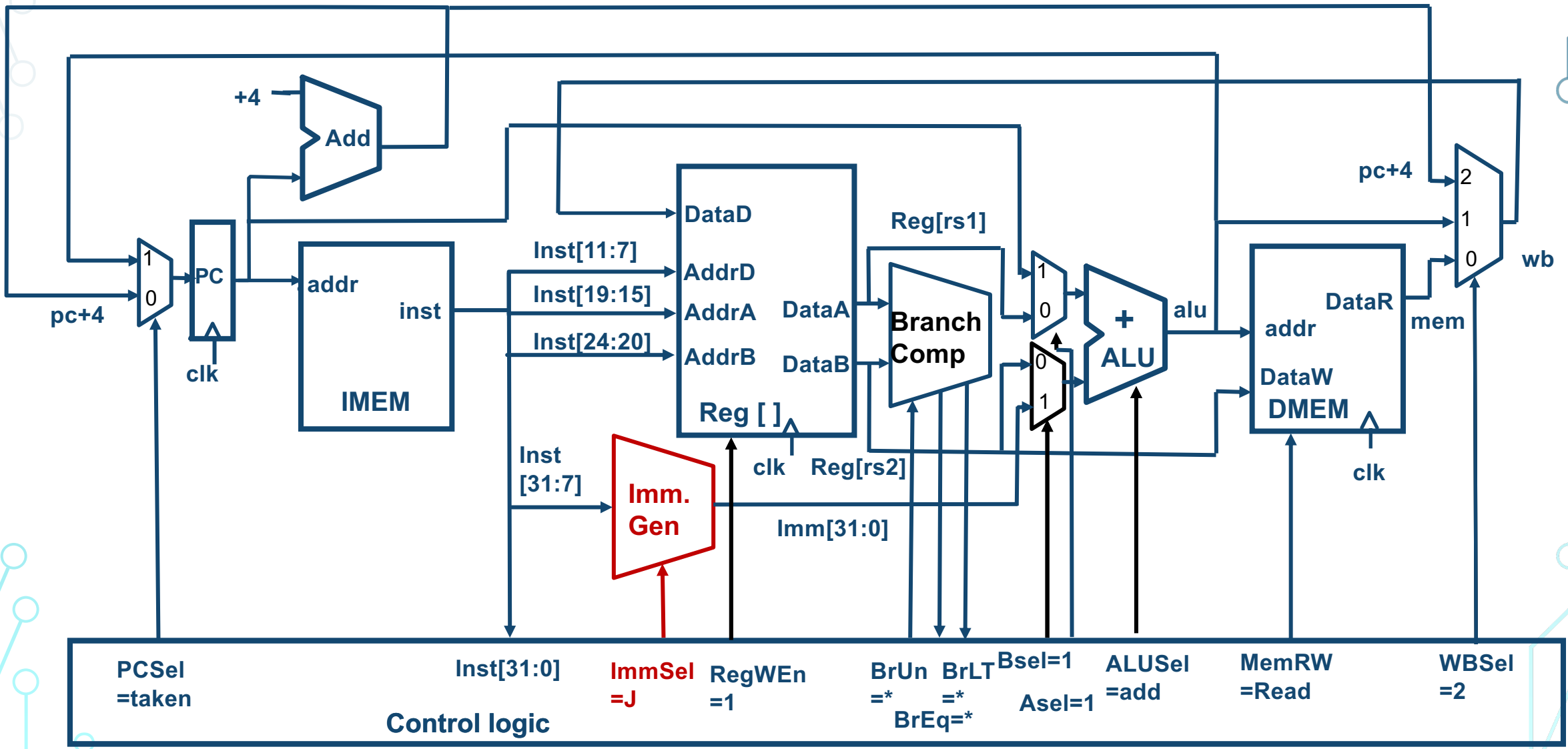


- JAL:
  - R[rd] = PC + 4; PC = PC + imm;
  - saves PC+4 in register rd (the return address)
    - Assembler "`j`" jump is pseudo-instruction, uses JAL but sets `rd=x0` to discard return address
  - Set PC = PC + offset (PC-relative jump)
- Target somewhere within $\pm 2^{19}$ locations, 2 bytes apart
  - $\pm 2^{18}$ 32-bit instructions
- Immediate encoding optimized similarly to branch instruction to reduce hardware cost

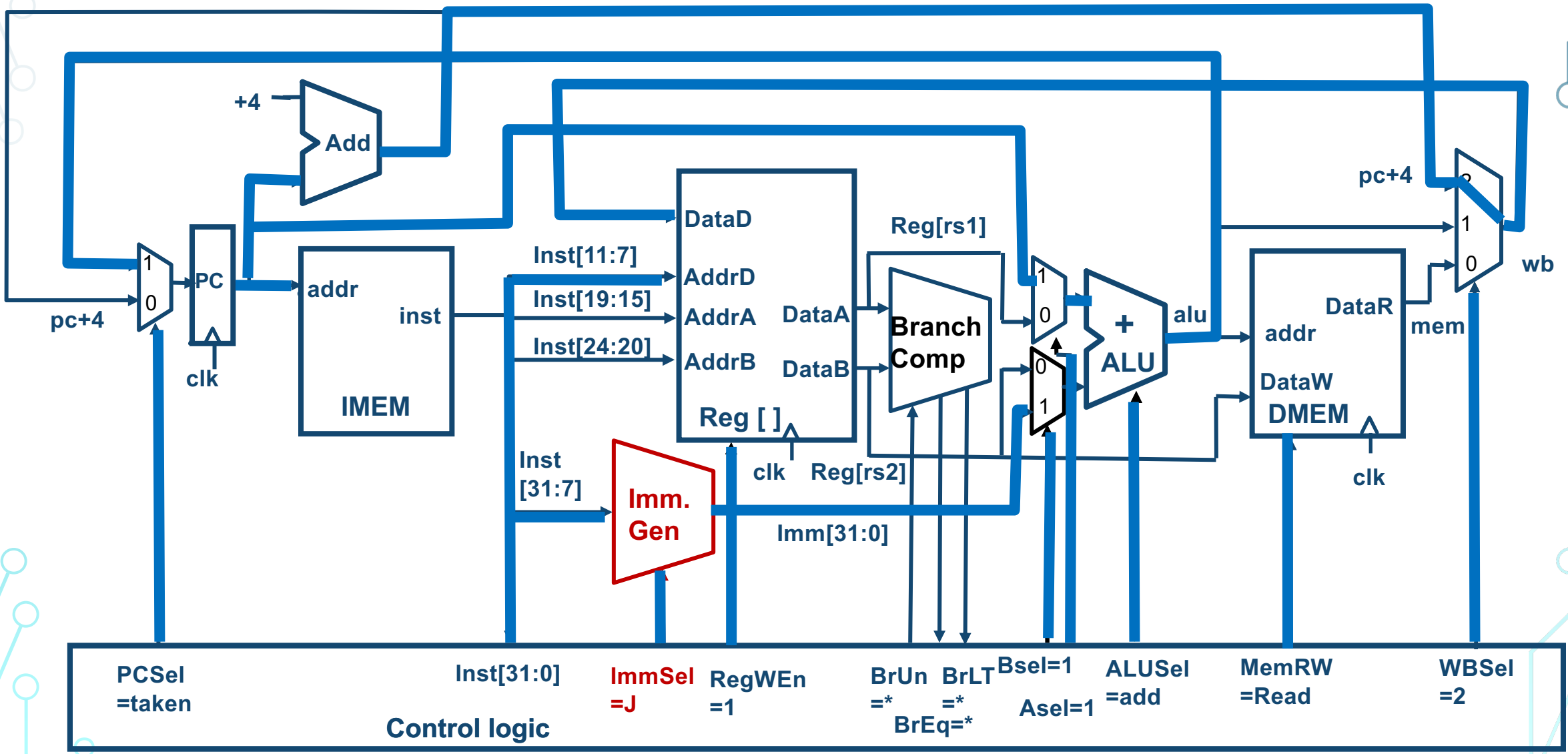
Datapath with JALR



Adding JAL


+4
Add
1
0
PC
clk
pc+4
addr
inst
IMEM
Inst[11:7]
Inst[19:15]
Inst[24:20]
DataD
AddrD
AddrA
AddrB
DataA
DataB
Reg [ ]
clk
Reg[rs1]
Reg[rs2]
Branch Comp
1
0
0
1
+
ALU
alu
pc+4
2
1
0
wb
addr
DataR
DataW
DMEM
clk
mem
Inst [31:7]
Imm. Gen
Imm[31:0]
PCSel =taken
Inst[31:0]
ImmSel =J
RegWEn =1
BrUn =*
BrLT =*
BrEq=*
Bsel=1
Asel=1
ALUSel =add
MemRW =Read
WBSel =2
Control logic

Adding JAL


+4
Add
pc+4
1
0
PC
clk
addr
inst
IMEM
Inst[11:7]
Inst[19:15]
Inst[24:20]
DataD
AddrD
AddrA
AddrB
DataA
DataB
Reg [ ]
clk
Reg[rs1]
Reg[rs2]
Branch Comp
Inst [31:7]
Imm. Gen
Imm[31:0]
1
0
0
1
+
ALU
alu
addr
DataR
DataW
DMEM
clk
mem
pc+4
1
0
wb
PCSel =taken
Inst[31:0]
Control logic
ImmSel =J
RegWEn =1
BrUn =*
BrLT =*
BrEq=*
Bsel=1
Asel=1
ALUSel =add
MemRW =Read
WBSel =2

- RISC-V Datapath & Control
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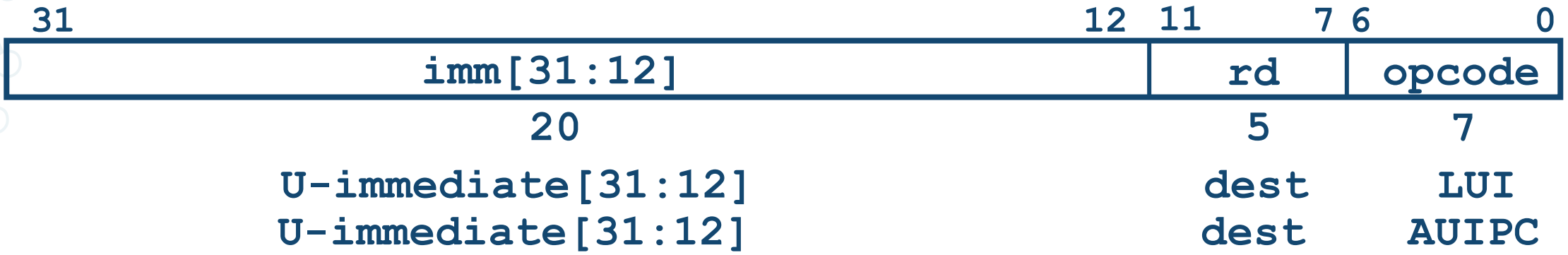
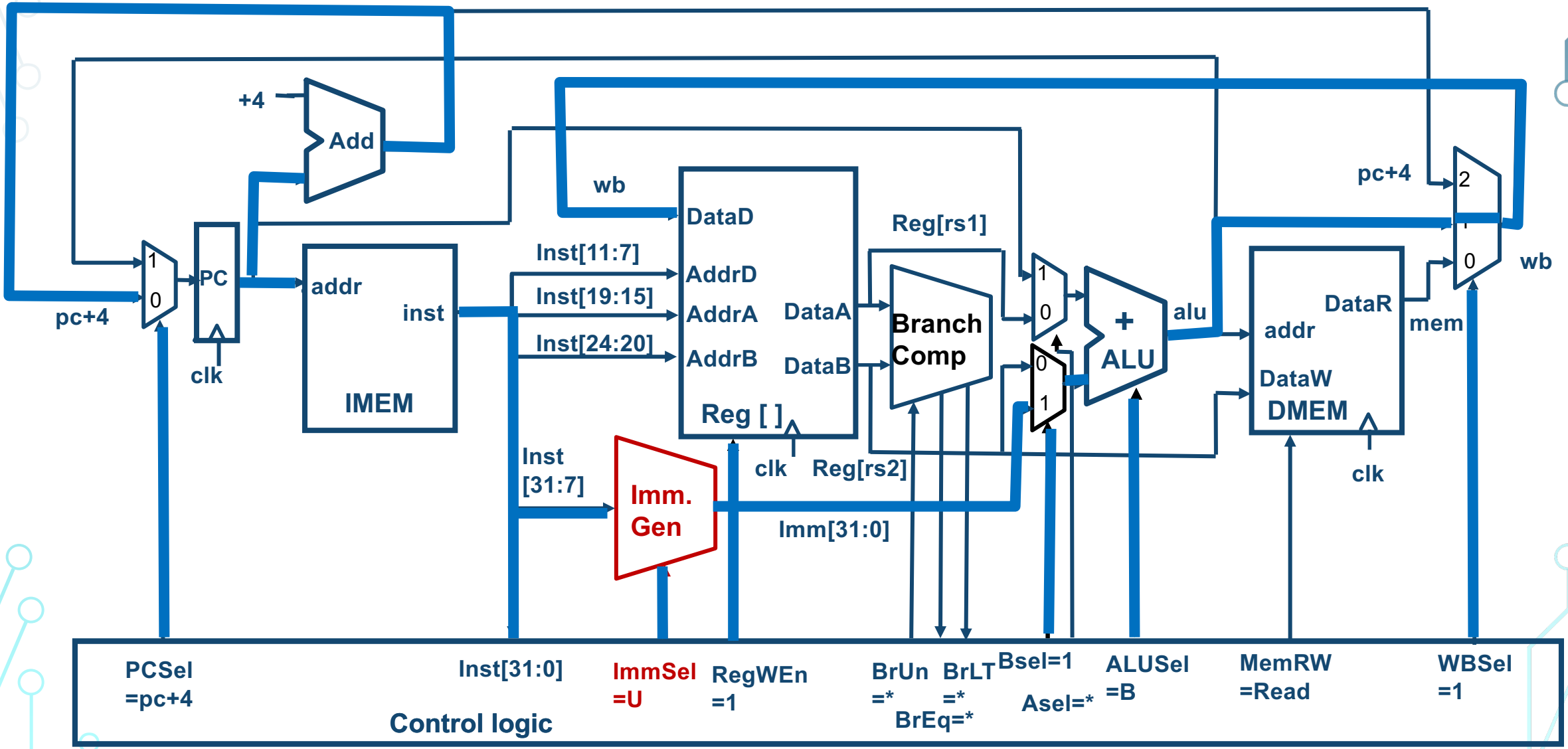
U-Format for “Upper Immediate” Instructions

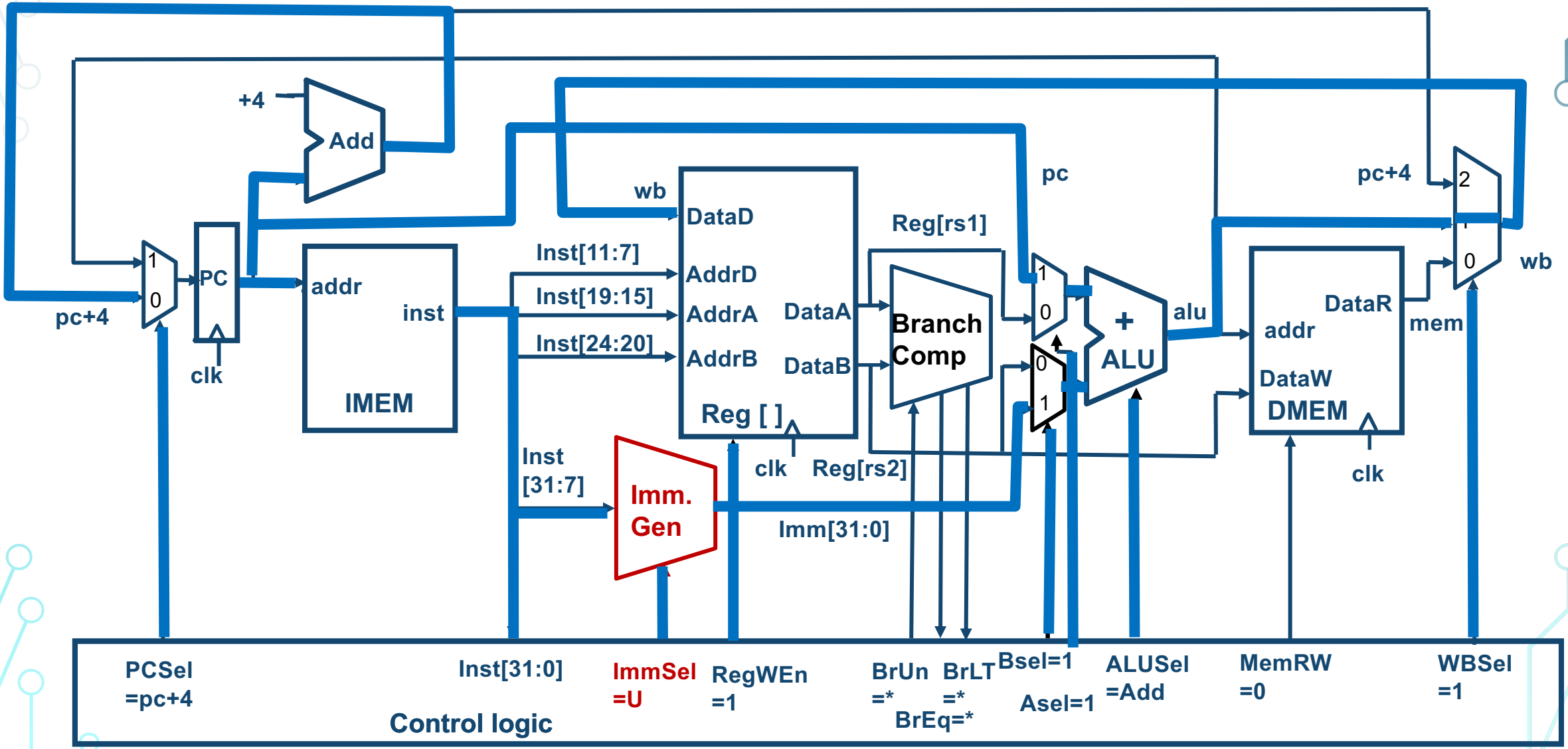


- Has 20-bit immediate in upper 20 bits of 32-bit instruction word
- One destination register, rd
- Used for two instructions
  - LUI – Load Upper Immediate
    - Reg[rd] = {imm, 12b’0}
  - AUIPC – Add Upper Immediate to PC
    - Reg[rd] = PC + {imm, 12’b0}

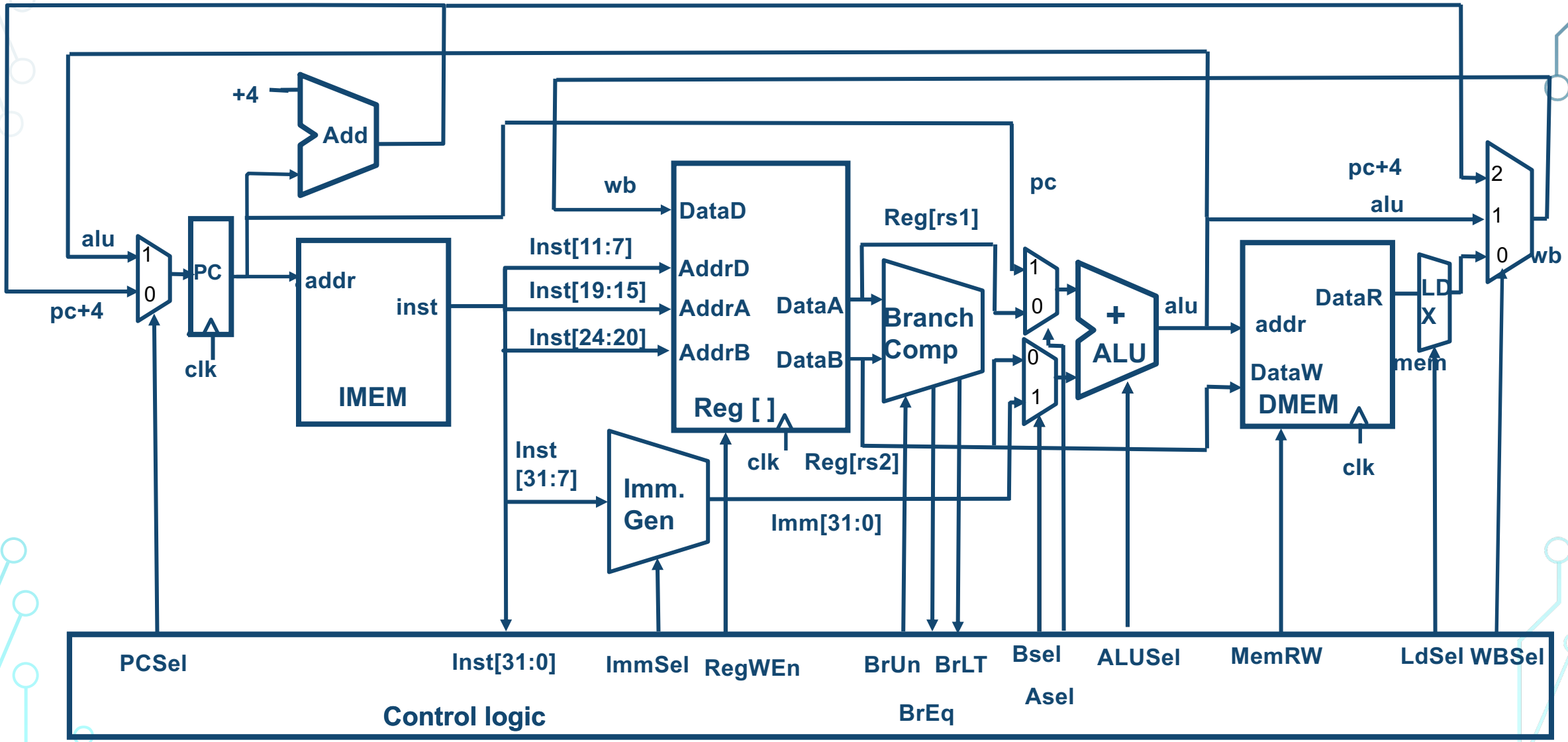
Implementing LUI



Implementing AUIPC



Complete RV32I Datapath!



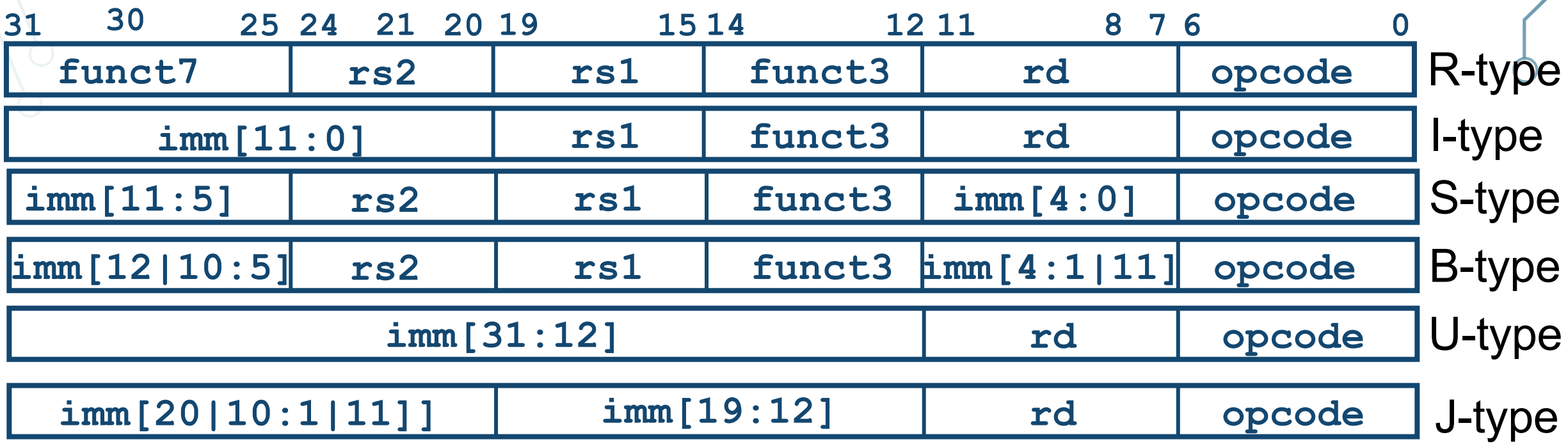
Recap: Complete RV32I ISA

imm[31:12]				rd	0110111	LUI
imm[31:12]				rd	0010111	AUIPC
imm[20|10:1|11|19:12]				rd	1101111	JAL
imm[11:0]		rs1	000	rd	1100111	JALR
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU
imm[11:0]		rs1	000	rd	0000011	LB
imm[11:0]		rs1	001	rd	0000011	LH
imm[11:0]		rs1	010	rd	0000011	LW
imm[11:0]		rs1	100	rd	0000011	LBU
imm[11:0]		rs1	101	rd	0000011	LHU
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	SB
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW
imm[11:0]		rs1	000	rd	0010011	ADDI
imm[11:0]		rs1	010	rd	0010011	SLTI
imm[11:0]		rs1	011	rd	0010011	SLTIU
imm[11:0]		rs1	100	rd	0010011	XORI
imm[11:0]		rs1	110	rd	0010011	ORI
imm[11:0]		rs1	111	rd	0010011	ANDI

0000000	shamt	rs1	001	rd	0010011	SLLI
0000000	shamt	rs1	101	rd	0010011	SRLI
0100000	shamt	rs1	101	rd	0010011	SRAI
0000000	rs2	rs1	000	rd	0110011	ADD
0100000	rs2	rs1	000	rd	0110011	SUB
0000000	rs2	rs1	001	rd	0110011	SLL
0000000	rs2	rs1	010	rd	0110011	SLT
0000000	rs2	rs1	011	rd	0110011	SLTU
0000000	rs2	rs1	100	rd	0110011	XOR
0000000	rs2	rs1	101	rd	0110011	SRL
0100000	rs2	rs1	101	rd	0110011	SRA
0000000	rs2	rs1	110	rd	0110011	OR
0000000	rs2	rs1	111	rd	0110011	AND
0000	pred	succ	00000	000	00000	0001111	FENCE
0000	0000	0000	00000	001	00000	0001111	FENCE.I
000000000000			00000	000	00000	1110011	ECALL
000000000001			00000	000	00000	1110011	EBREAK
csr			rs1	001	rd	1110011	CSRRW
csr			rs1	010	rd	1110011	CSRRS
csr			rs1	011	rd	1110011	CSRRC
csr			zimm	101	rd	1110011	CSRRWI
csr			zimm	110	rd	1110011	CSRRSI
csr			zimm	111	rd	1110011	CSRRCI

- RV32I has 47 instructions
- 37 instructions are enough to run any C program

Summary of RISC-V Instruction Formats



Administrivia

- No new lab this week.
- HW 3 due this week.
  - HW 4 out (last HW before midterm)
- Midterm 3/1 Tuesday
  - In class.
  - Cover up to pipelining (this week's lecture)
- Guest lecture on FPGA use cases next Thursday

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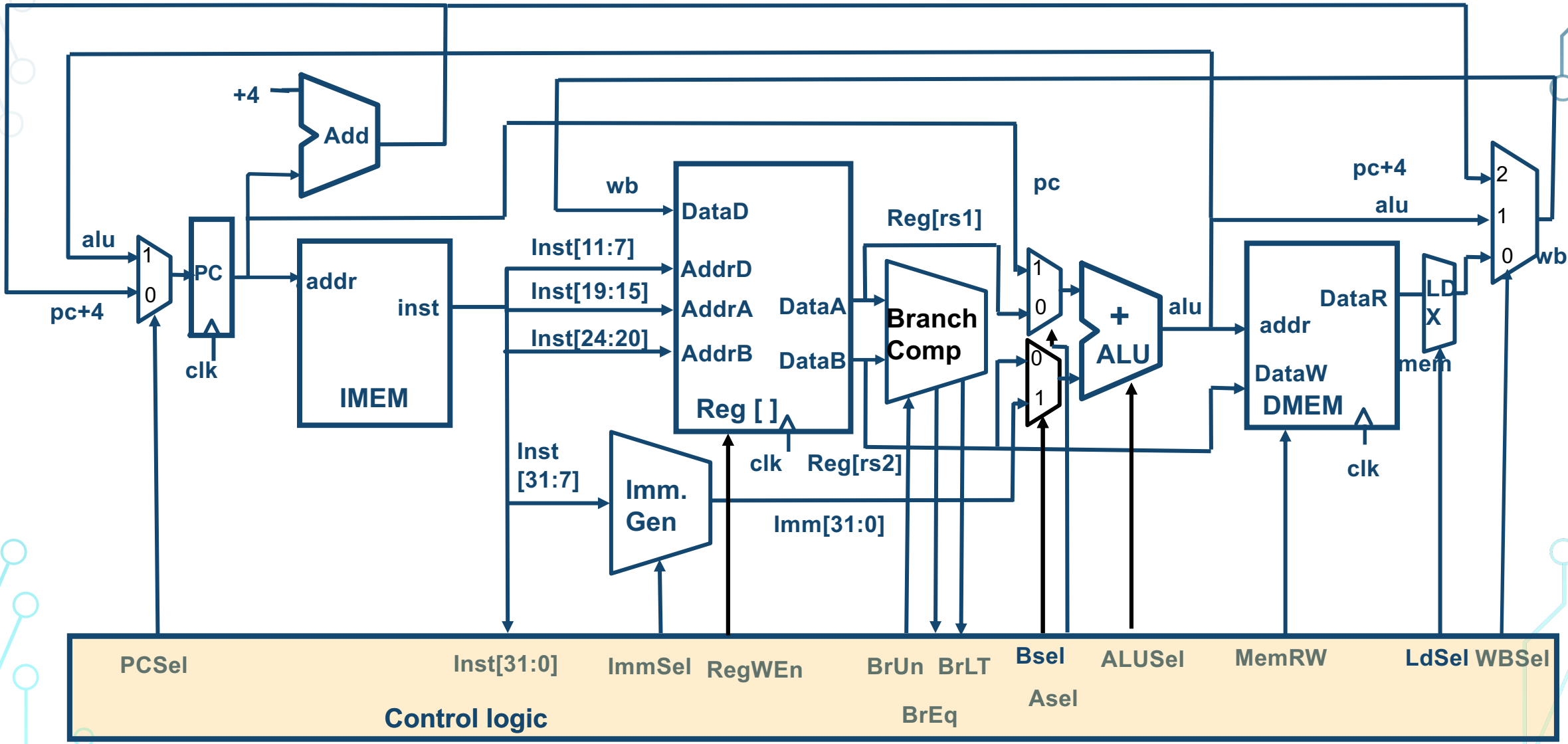
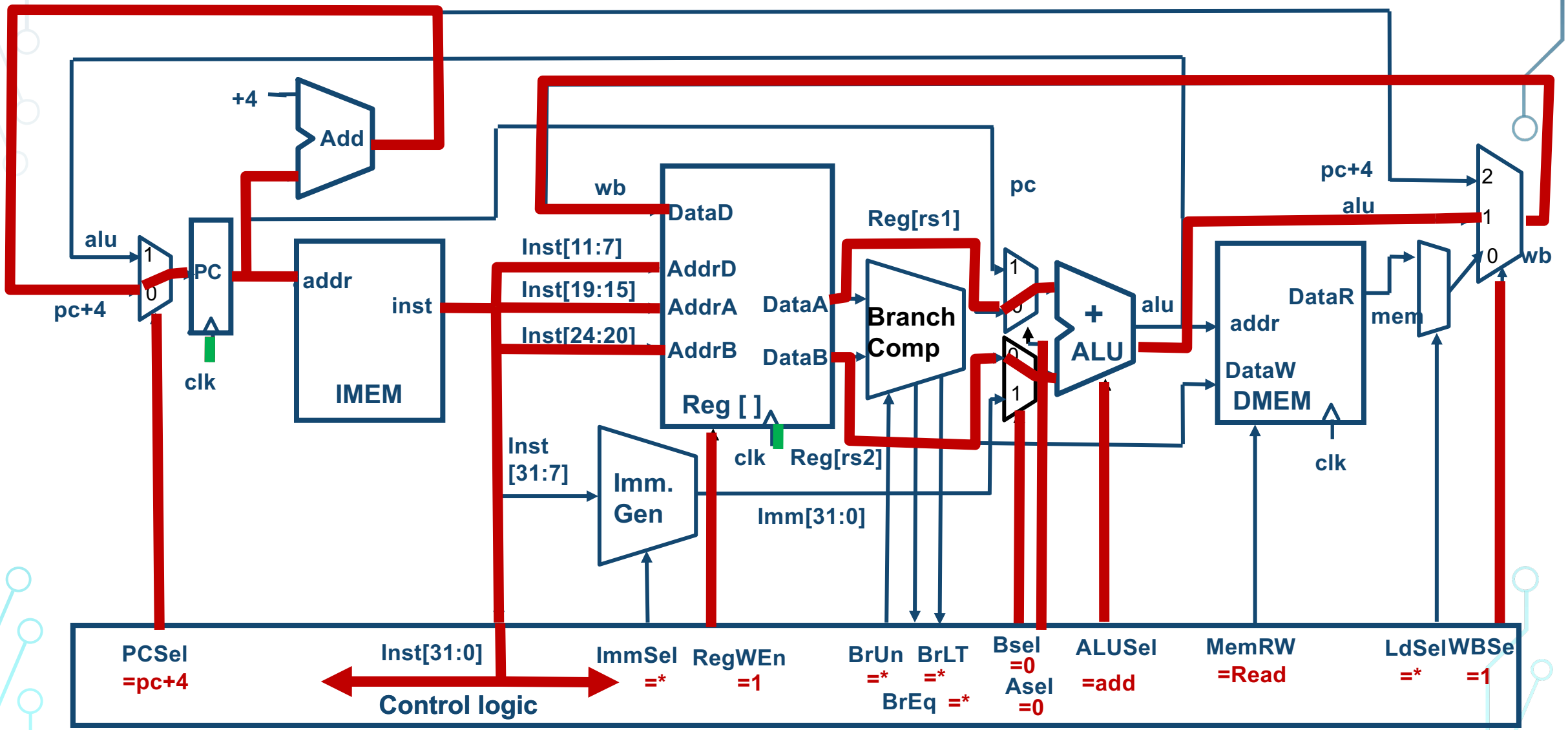
Complete RV32I Datapath with Control

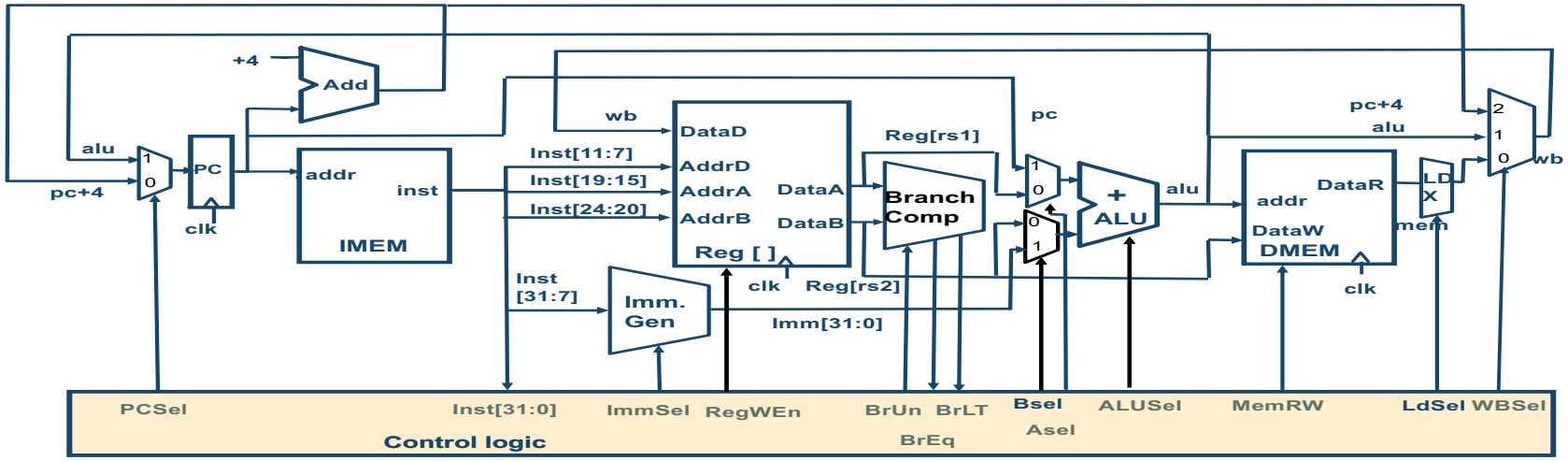


Example: add


+4
Add
alu
pc+4
PC
clk
addr
inst
IMEM
wb
DataD
AddrD
AddrA
AddrB
Reg [ ]
clk
DataA
DataB
Inst[11:7]
Inst[19:15]
Inst[24:20]
Inst
[31:7]
Imm.
Gen
Imm[31:0]
Reg[rs1]
Reg[rs2]
pc
Branch
Comp
+
ALU
alu
addr
DataW
DMEM
DataR
clk
mem
pc+4
alu
wb
PCSel
=pc+4
Inst[31:0]
Control logic
ImmSel
=*
RegWEn
=1
BrUn
=*
BrLT
=*
BrEq
=*
Bsel
=0
Asel
=0
ALUSel
=add
MemRW
=Read
LdSel
=*
WBSel
=1


31
25
24
20
19
15
14
12
11
7
6
0
funct7
rs2
rs1
funct3
rd
opcode
7
5
5
3
5
7

add Execution



Clock			
PC	1000	1004	
PC+4	1004	1008	
inst[31:0]	add x1,x2,x3	add x6,x7,x9	
Control logic	add control	add control	
Reg[rs1]	Reg[2]	Reg[7]	
Reg[rs2]	Reg[3]	Reg[9]	
alu	Reg[2]+Reg[3]	Reg[7]+Reg[9]	
wb	Reg[2]+Reg[3]	Reg[7]+Reg[9]	
Reg[1]	???	Reg[2]+Reg[3]	

Control Logic Truth Table

Inst[31:0]	BrEq	BrLT	PCSel	ImmSel	BrUn	ASel	BSel	ALUSel	MemRW	RegWEn	WBSel
`add`	*	*	+4	*	*	Reg	Reg	Add	Read	1	ALU
`sub`	*	*	+4	*	*	Reg	Reg	Sub	Read	1	ALU
(R-R Op)	*	*	+4	*	*	Reg	Reg	*(Op)*	Read	1	ALU
`addi`	*	*	+4	I	*	Reg	Imm	Add	Read	1	ALU
`lw`	*	*	+4	I	*	Reg	Imm	Add	Read	1	Mem
`sw`	*	*	+4	S	*	Reg	Imm	Add	Write	0	*
`beq`	0	*	+4	B	*	PC	Imm	Add	Read	0	*
`beq`	1	*	ALU	B	*	PC	Imm	Add	Read	0	*
`bne`	0	*	ALU	B	*	PC	Imm	Add	Read	0	*
`bne`	1	*	+4	B	*	PC	Imm	Add	Read	0	*
`blt`	*	1	ALU	B	0	PC	Imm	Add	Read	0	*
`bltu`	*	1	ALU	B	1	PC	Imm	Add	Read	0	*
`jalr`	*	*	ALU	I	*	Reg	Imm	Add	Read	1	PC+4
`jal`	*	*	ALU	J	*	PC	Imm	Add	Read	1	PC+4
`auipc`	*	*	+4	U	*	PC	Imm	Add	Read	1	ALU

RV32I, a nine-bit ISA!

imm[31:12]				rd	0110111	LUI
imm[31:12]				rd	0010111	AUIPC
imm[20|10:1|11|19:12]				rd	1101111	JAL
imm[11:0]		rs1	000	rd	1100111	JALR
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU
imm[11:0]		rs1	000	rd	0000011	LB
imm[11:0]		rs1	001	rd	0000011	LH
imm[11:0]		rs1	010	rd	0000011	LW
imm[11:0]		rs1	100	rd	0000011	LBU
imm[11:0]		rs1	101	rd	0000011	LHU
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	SB
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW
imm[11:0]		rs1	000	rd	0010011	ADDI
imm[11:0]		rs1	010	rd	0010011	SLTI
imm[11:0]		rs1	011	rd	0010011	SLTIU
imm[11:0]		rs1	100	rd	0010011	XORI
imm[11:0]		rs1	110	rd	0010011	ORI
imm[11:0]		rs1	111	rd	0010011	ANDI
0000000	shamt	rs1	001	rd	0010011	SLLI
0000000	shamt	rs1	101	rd	0010011	SRLI
0100000	shamt	rs1	101	rd	0010011	SRAI
0000000	rs2	rs1	000	rd	0110011	ADD
0100000	rs2	rs1	000	rd	0110011	SUB
0000000	rs2	rs1	001	rd	0110011	SLL
0000000	rs2	rs1	010	rd	0110011	SLT
0000000	rs2	rs1	011	rd	0110011	SLTU
0000000	rs2	rs1	100	rd	0110011	XOR
0000000	rs2	rs1	101	rd	0110011	SRL
0100000	rs2	rs1	101	rd	0110011	SRA
0000000	rs2	rs1	110	rd	0110011	OR
0000000	rs2	rs1	111	rd	0110011	AND

inst[30]

inst[14:12]

inst[6:2]

Instruction type encoded using only 9 bits inst[30],inst[14:12], inst[6:2]

Control Realization Options

- ROM
  - “Read-Only Memory”
  - Regular structure
  - Can be easily reprogrammed
    - fix errors
    - add instructions
- Combinatorial Logic
  - Decoder is typically hierarchical
    - First decode opcode, and figure out instruction type
    - E.g. branches are Inst[6:2] = 11000
    - Then determine the actual instruction
    - Inst[30] + Inst[14:12]
  - Modularity helps simplify and speed up logic
    - Narrow problem space for logic synthesis

Combinational Logic Control

- Simplest example: BrUn

inst[14:12] inst[6:2]

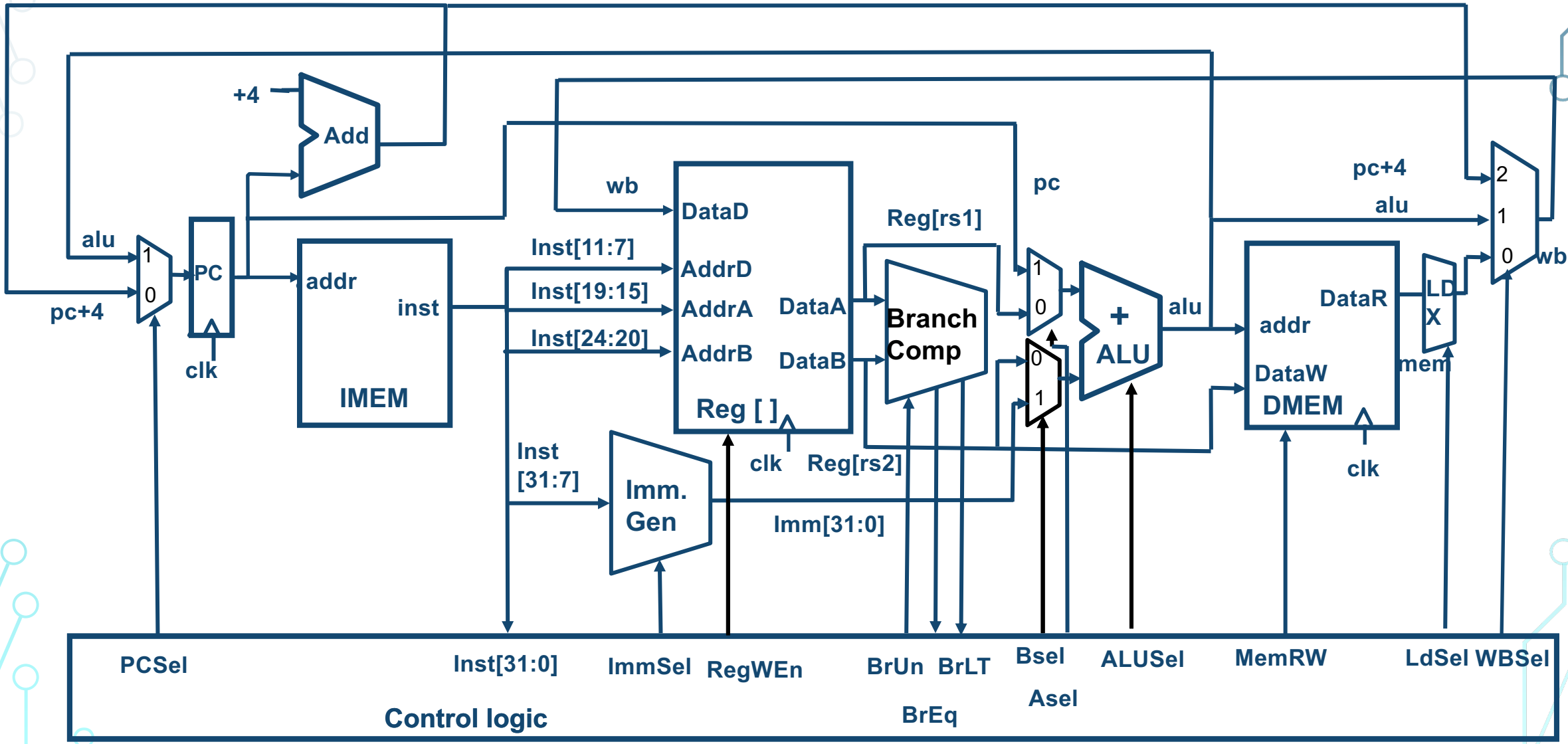
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU

inst[14:13]

inst[12]	00	01	11	10
0				
1				

- **How to decode whether BrUn is 1?**
  - **Branch = Inst[6] • Inst[5] • !Inst[4] • !Inst[3] • !Inst[2]**
  - **BrUn = Inst [13] • Branch**

Complete RV32I Datapath with Control



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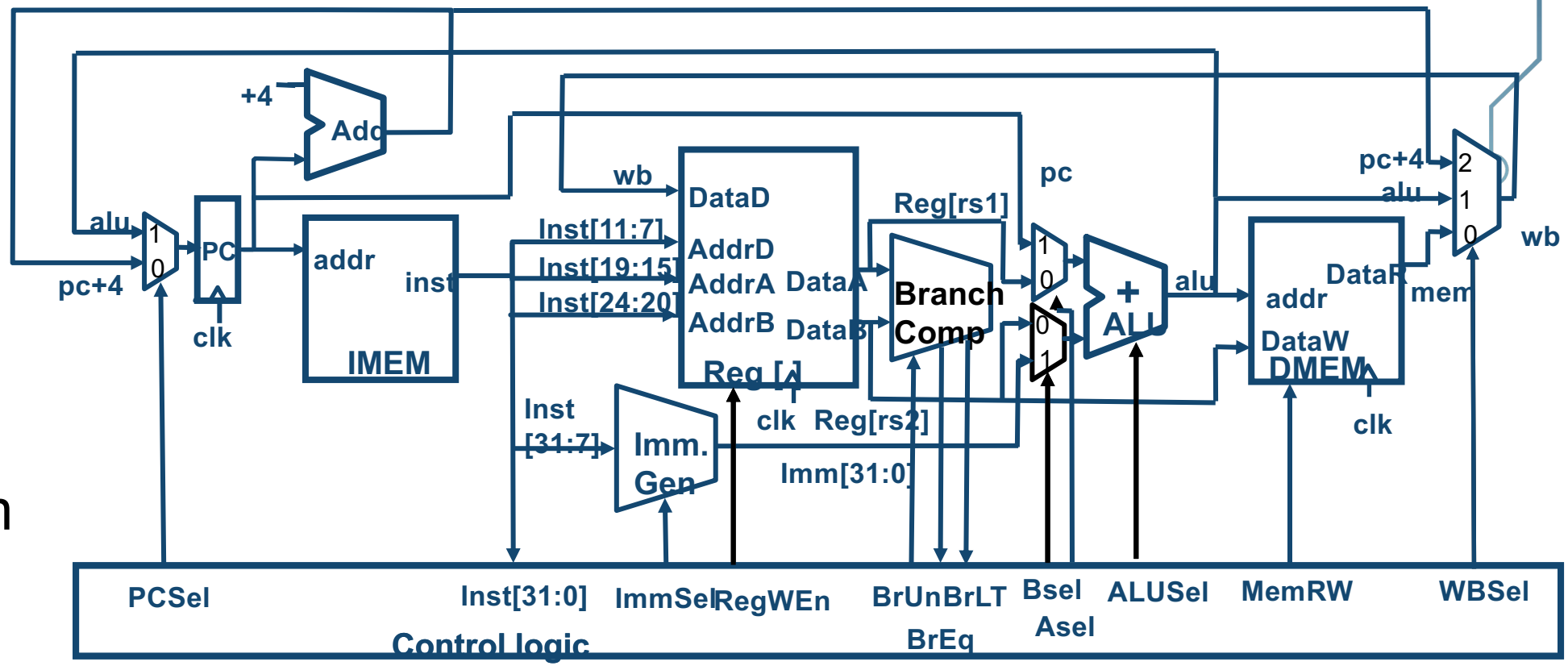
Critical Path

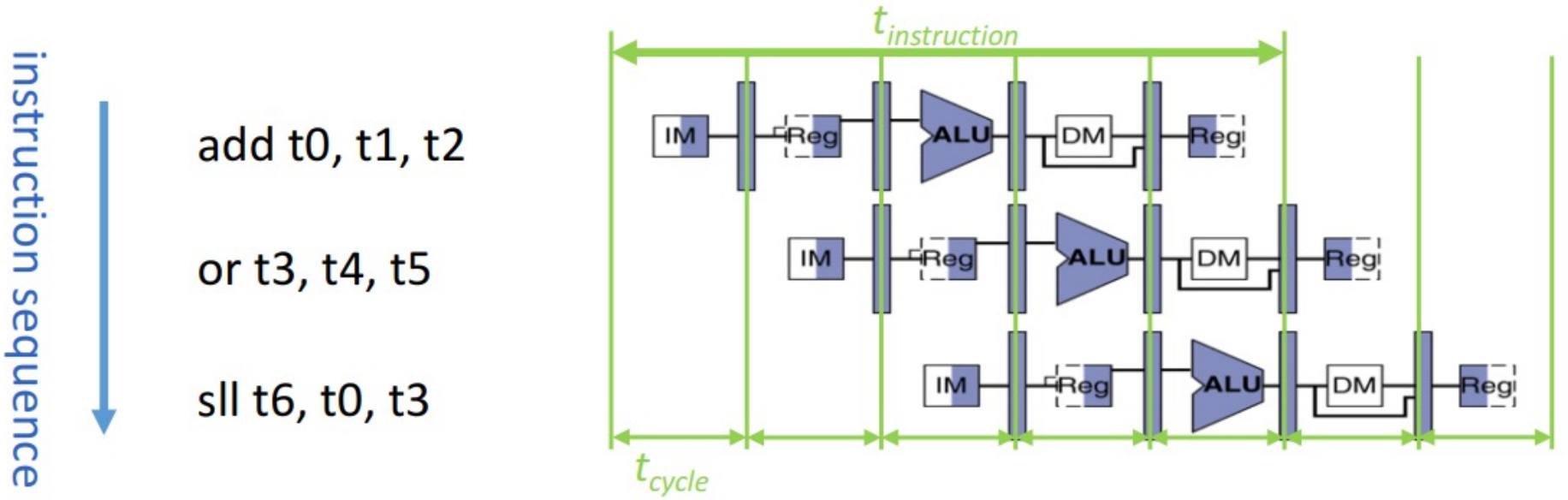
Critical
path for an addi

R[rd] = R[rs1]+imm



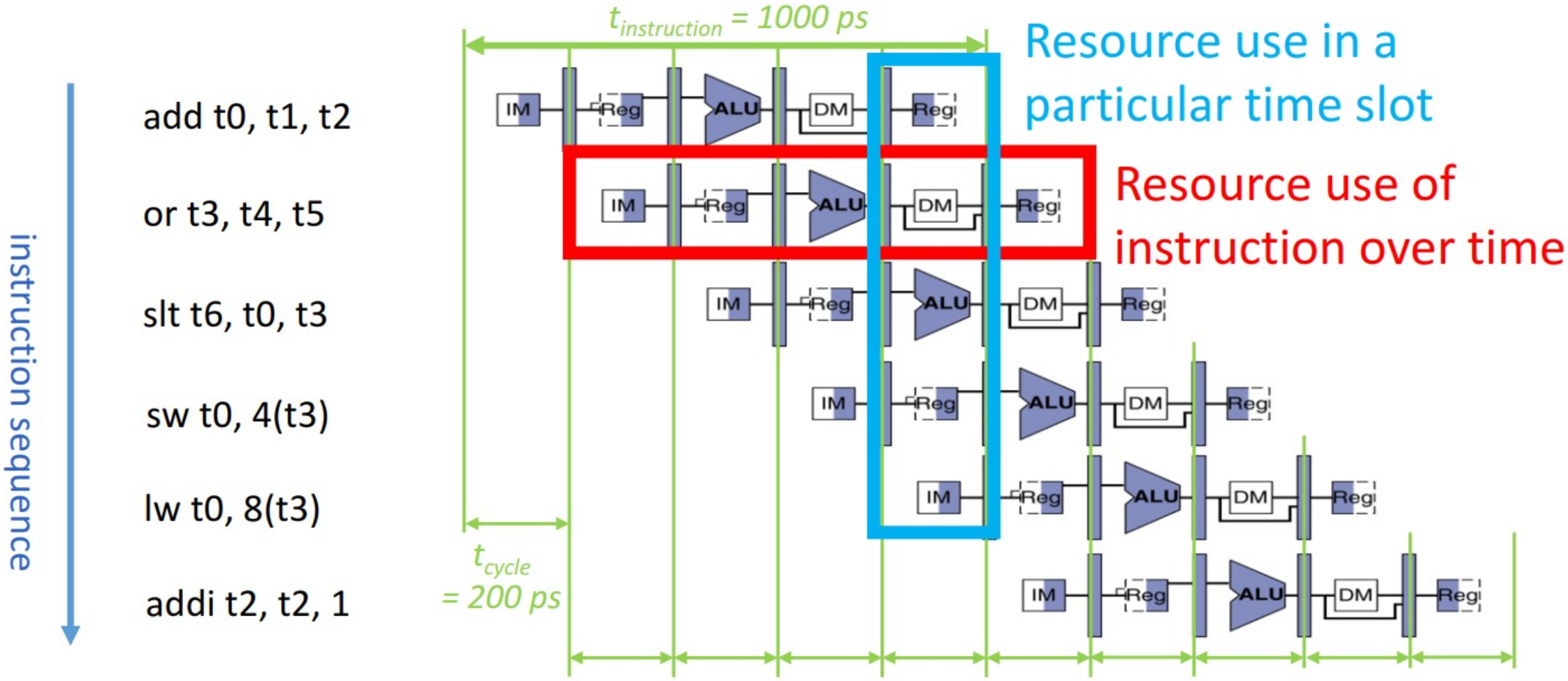
1) $t_{clk\text{-}q} + t_{Add} + t_{IMEM} + t_{Reg} + t_{BComp} + t_{ALU} + t_{DMEM} + t_{mux} + t_{Setup}$
2) $t_{clk\text{-}q} + t_{IMEM} + \max\{t_{Reg}, t_{Imm}\} + t_{ALU} + 2t_{mux} + t_{Setup}$
3) $t_{clk\text{-}q} + t_{IMEM} + \max\{t_{Reg}, t_{Imm}\} + t_{ALU} + 3t_{mux} + t_{DMEM} + t_{Setup}$
4) None of the above

Pipelining with RISC-V

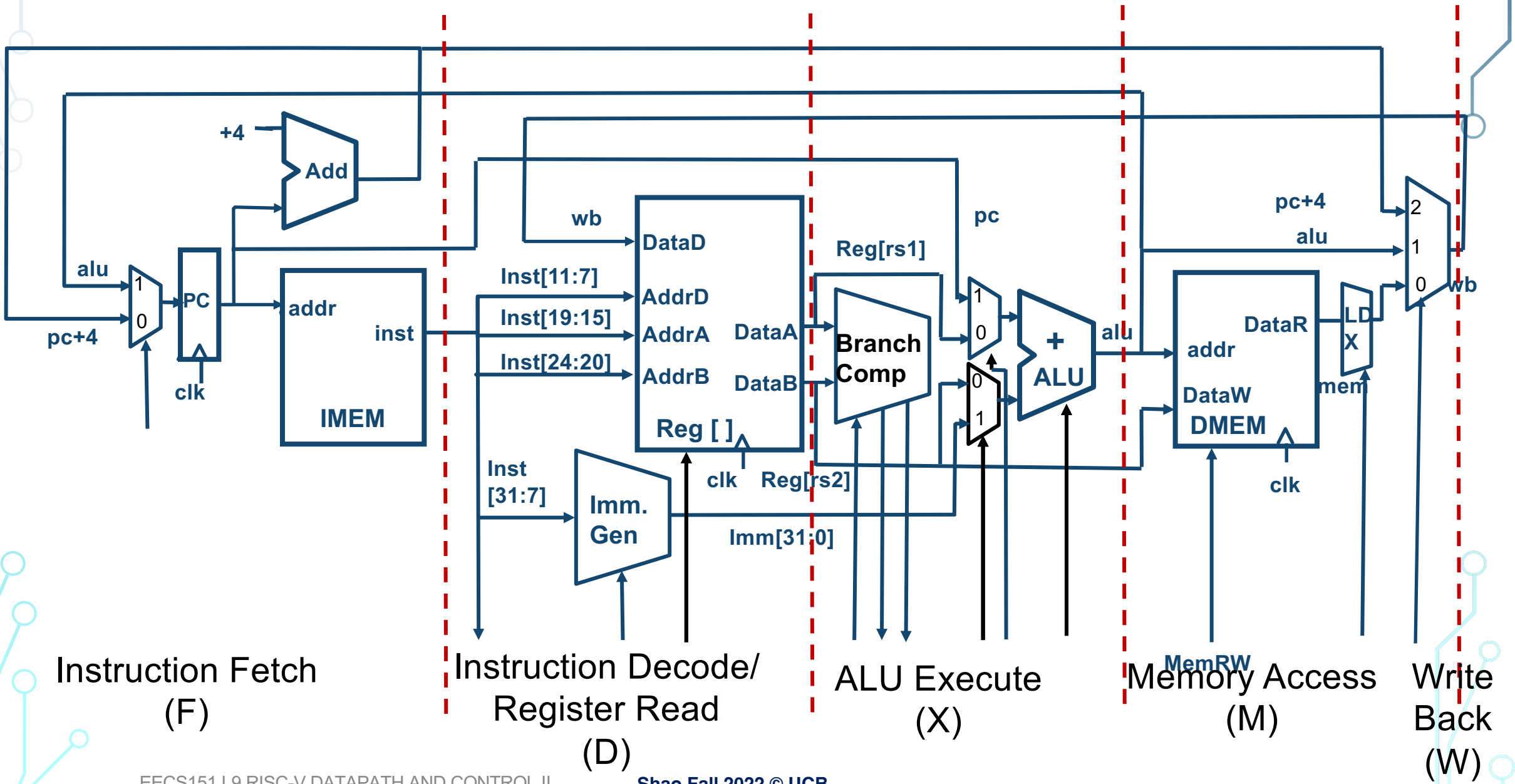


	Single Cycle	Pipelining
Timing	t_{step} = 100 … 200 ps	t_{cycle} = 200 ps
	Register access only 100 ps	All cycles same length
Instruction time, $t_{instruction}$	= t_{cycle} = 800 ps	1000 ps
Clock rate, f_s	1/800 ps = 1.25 GHz	1/200 ps = 5 GHz
Relative speed	1 x	4 x

Pipelining with RISC-V



Complete RV32I Datapath with Control



Instruction Fetch (F)

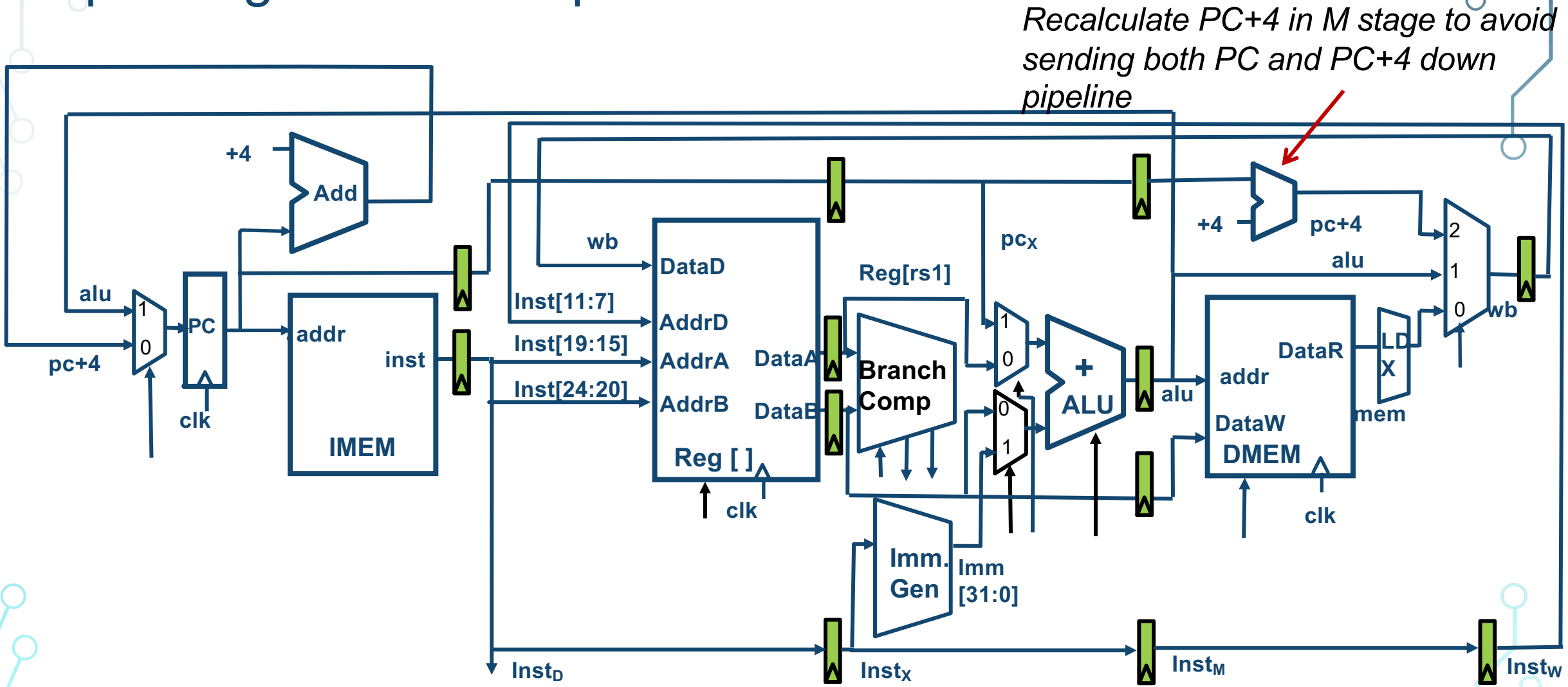
Instruction Decode/ Register Read (D)

ALU Execute (X)

Memory Access (M)

Write Back (W)

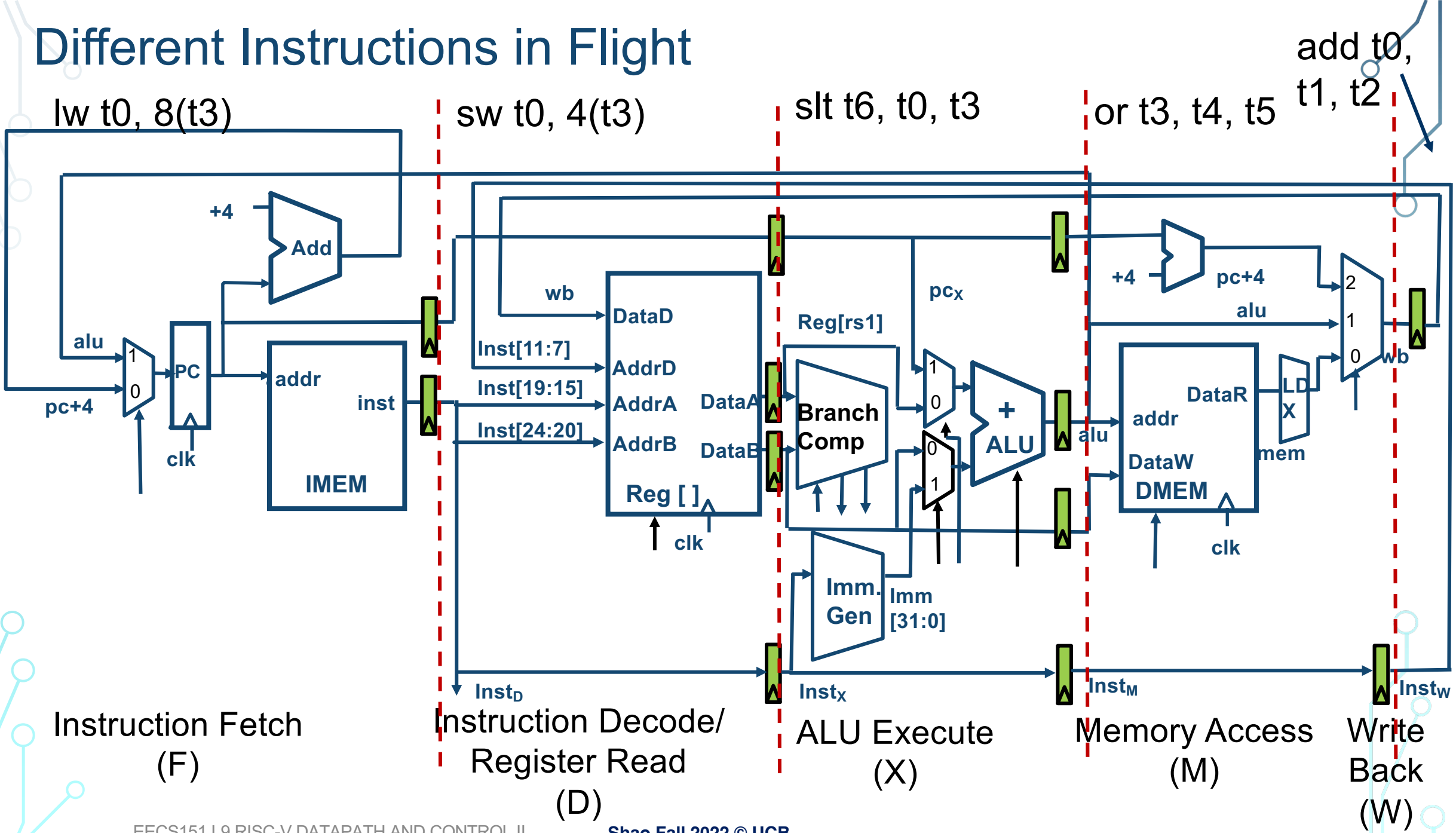
Pipelining RV32I Datapath



Instruction Fetch (F) | Instruction Decode/ Register Read (D) | ALU Execute (X) | Memory Access (M) | Write Back (W)

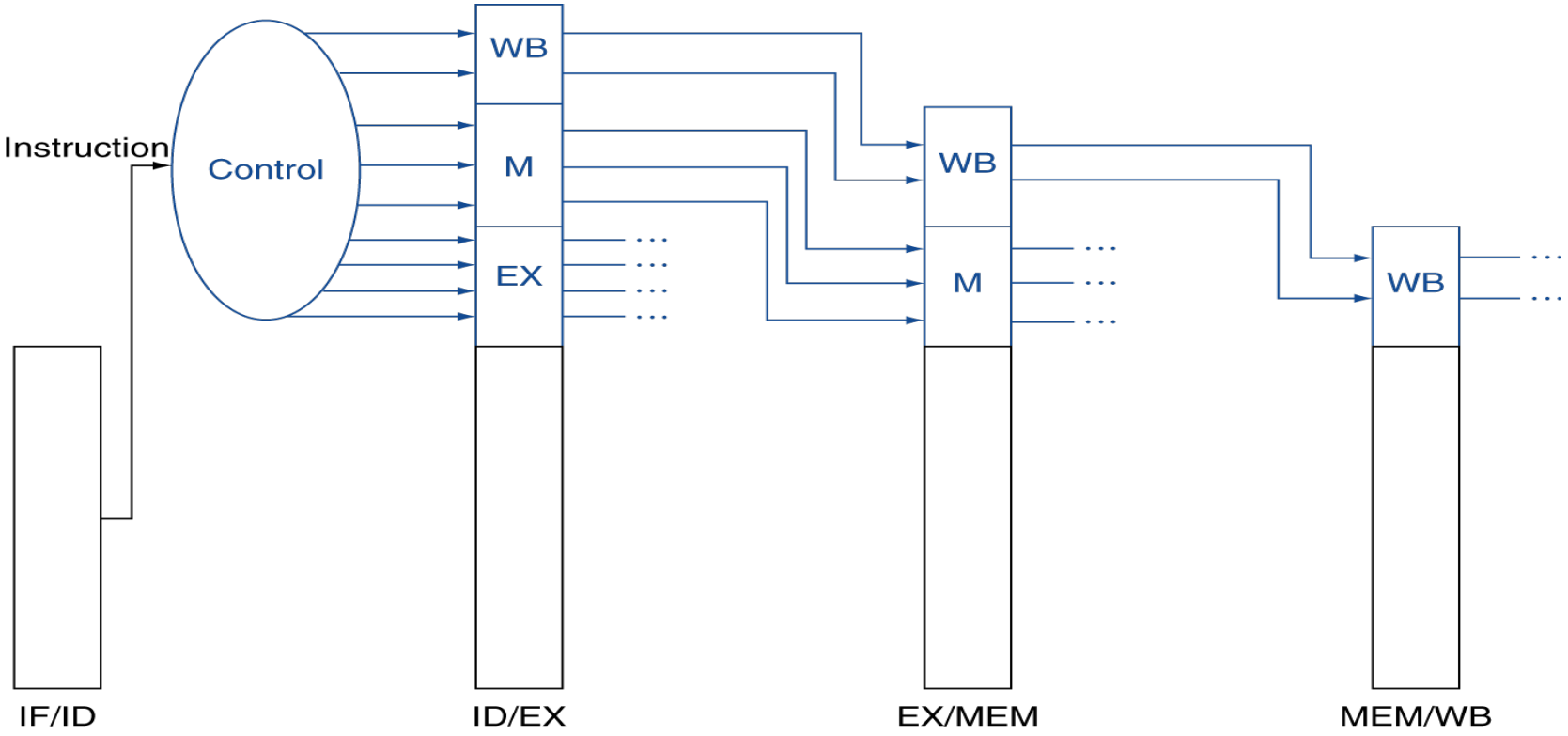
Must pipeline instruction along with data, so control operates correctly in each stage

Different Instructions in Flight



Pipelined Control

- Control signals derived from instruction
  - As in single-cycle implementation
  - Information is stored in pipeline registers for use by later stages



Summary

- We have covered the implementation of the base ISA for RV32I!!!
  - Get yourself familiar with the ISA Spec.
- Instruction type:
  - R-type
  - I-type
  - S-type
  - B-type
  - J-type
  - U-type
- Implementation suggested is straightforward, yet there are modalities in how to implement it well at gate level.
- Single-cycle datapath is slow – need to pipeline it