

Part A. Code Correctness and Design

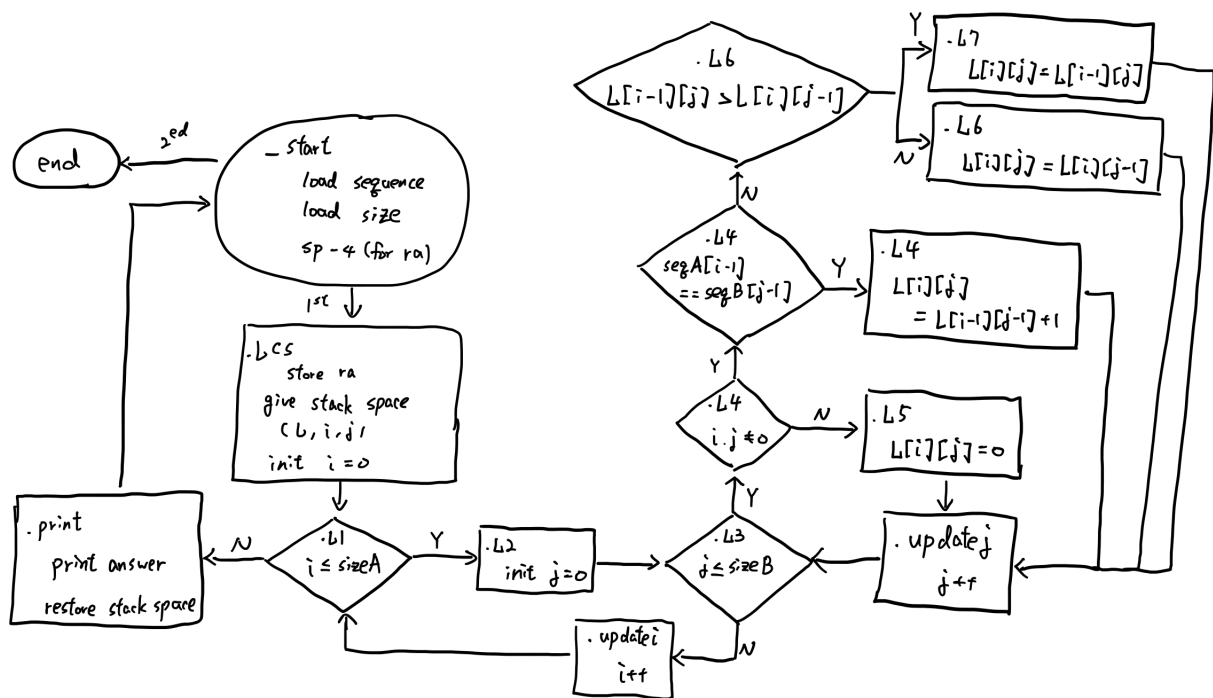
1. Correct Screenshot

Console

Found LCS length : 8

Found LCS length : 13

2. Flow Chart

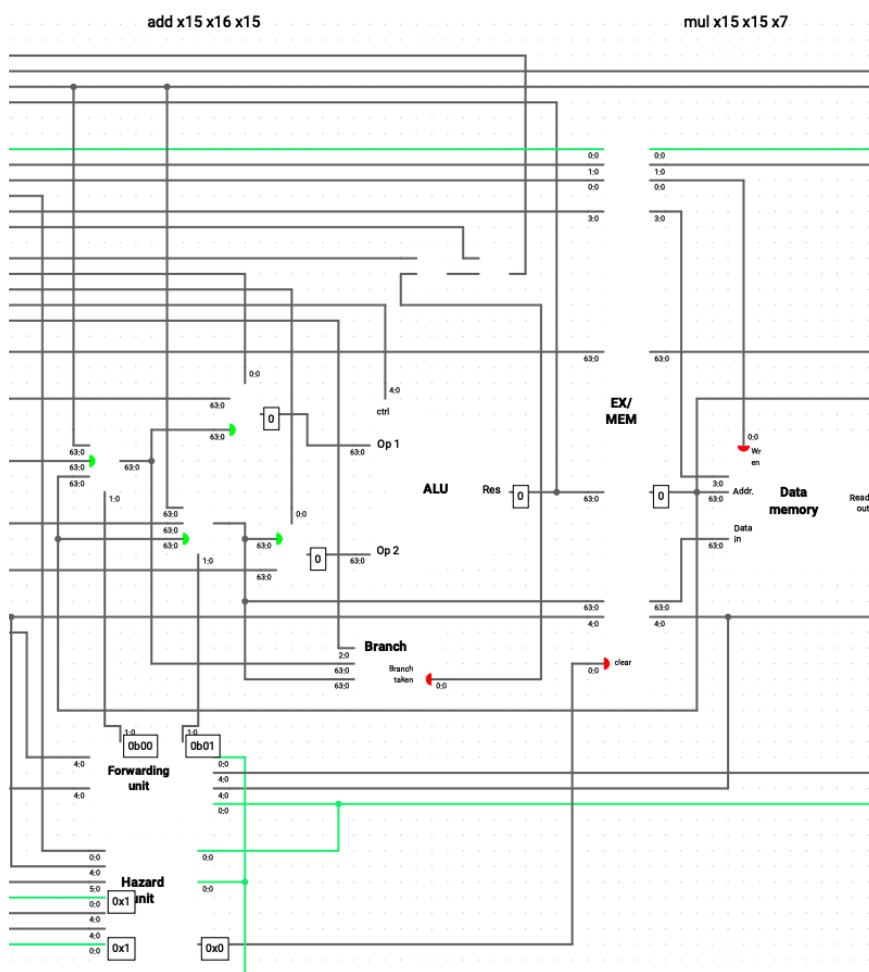


Part B. Hazard in Code

1. Type 1: R-type RAW at following 1st instruction.

92	<code>mul a5, a5, t2 # (sizeB+1)</code>
93	<code>add a5, a6, a5 # i*sizeB+j</code>

Line 92, mul is a R-type instruction, then t0 is set as rd(write) in this instruction, and it would be used as rs2(read) in next instruction.



Forwarding unit port : ldStage=0b00, MemStage=0b01

EX/MEM output = ALU op2 input

2. Type 2: R-type RAW at following 2nd instruction.

There is not any this type hazard happened in my code. I will give a simple example.

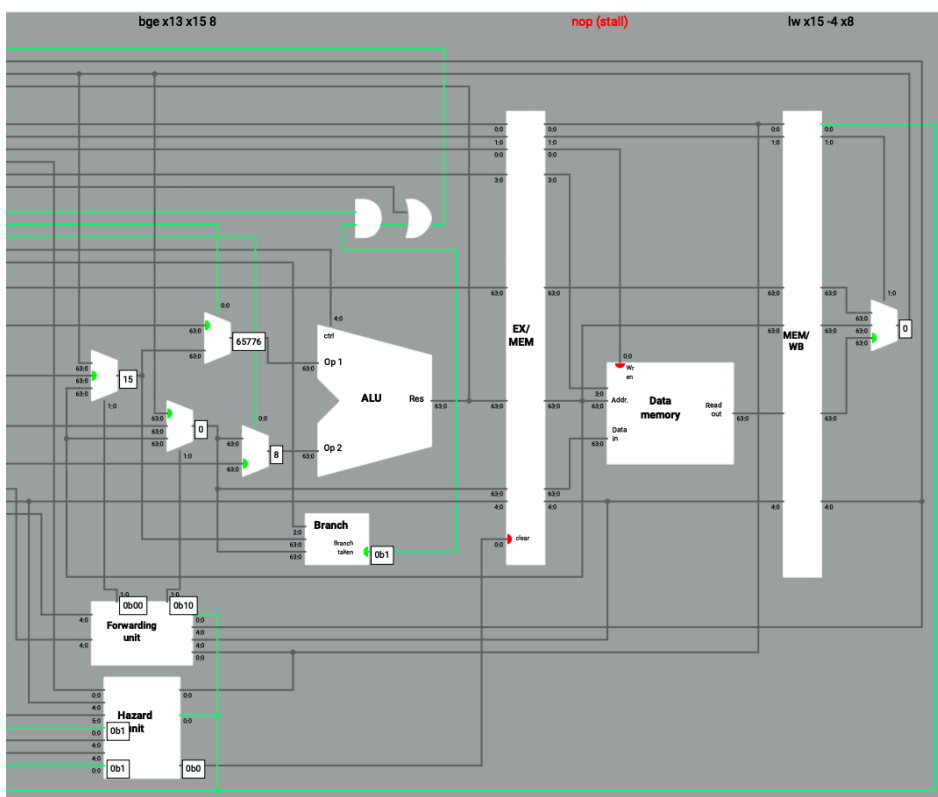
```
add a5, a5, a4
add a6, a6, a3
addi a5, a5, -1
```

Line 1, add is a R-type instruction, then a5 is rd (write), and the following 2nd instruction use a5 as r1(read) that means type 2 hazard happen. This example may happen when we have if-condition $\text{seqA}[i-1] == \text{seq}[j-1]$ to judge.

3. Type 3 : Load RAW at the following 1st instruction.

```
47      lw a5, -4(s0)
48      ble a5, a3, .L2 # go to loopj
```

Line 47, a5 is the load target(write), and it is used in next instruction as rs2(read) that is type 3 hazard.



Forwarding unit port: ldStage=0b00, MemStage=0b10

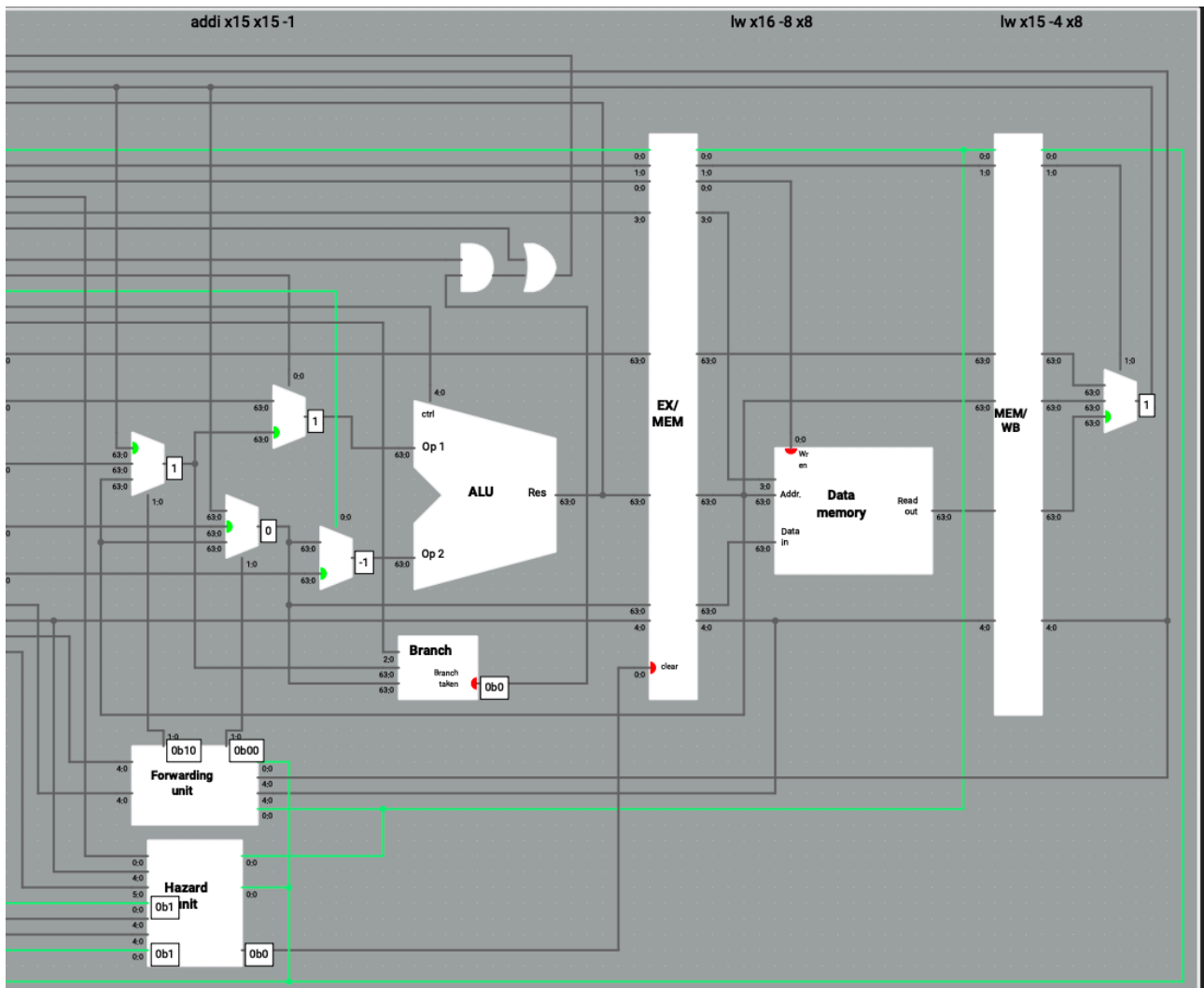
Because value haven't been stored complete, it insert nop between 2 instruction.

Forward value from MEM/WB to EX stage

4. Type 4 : Load RAW at the following 2nd instruction.

```
67      lw a5, -4(s0)
68      lw a6, -8(s0)
69      addi a5, a5, -1 # a5 = i-1
```

Line 67, a5 is the load target, and it is rs1 in line 69.



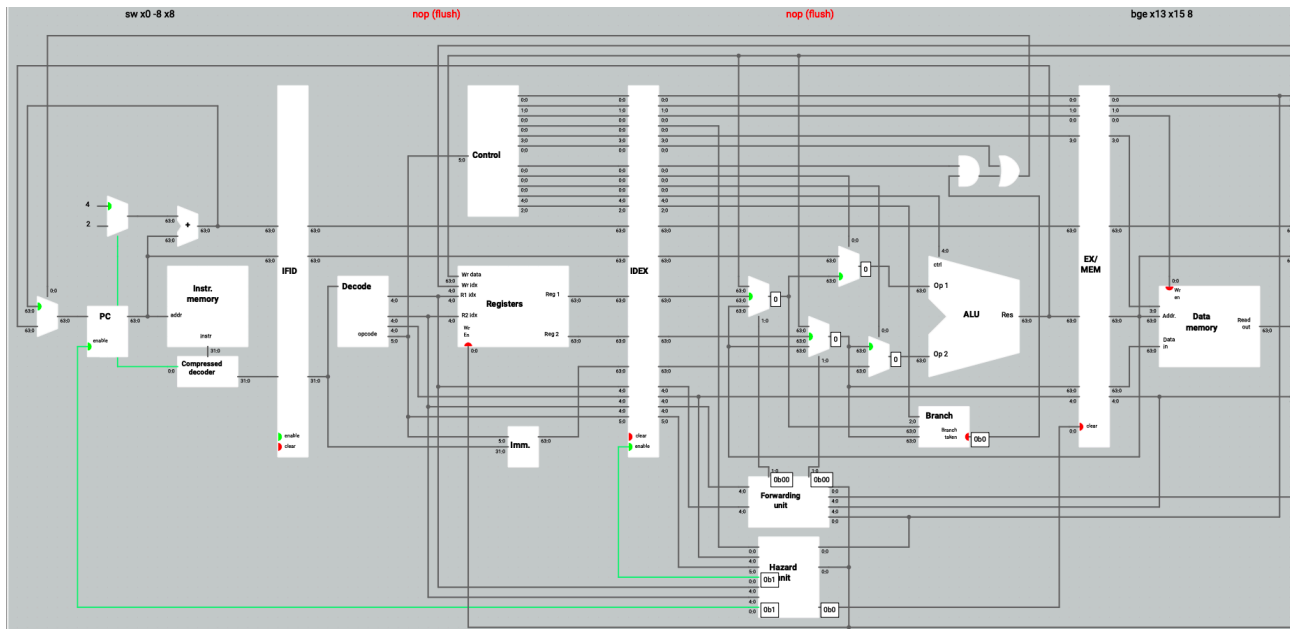
Forwarding unit port: ldStage=0b10, MemStage=0b00

Using Forwarding forward a5 value from MEM/WB to EX stage

5. Type 5 : Branch instruction (control hazard).

48 `ble a5, a3, .L2 # go to loopj`

Line 48, if $a5 < a3$, because of branch instruction, it would jump to .L2



Insert 2 nop after branch instruction.

Don't need to use forwarding, so forwarding port is 0.

All control ports are set as 0.