HW6

1. (20%) Draw the logic diagram of a four-bit register with four D flip-flops and four 4x1 multiplexers with mode selection S1 and S0. The register operates according to the following function table.

S1	S0	Register Operation
0	0	Load parallel data
0	1	Complement the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	No change

2. (20%) Ring counter vs Johnson counter: for a 6-bit ring counter
   (a) Design a 6-bit ring counter using shift registers.
   (b) List the 6 states produced with three flip-flops and the Boolean terms of each of the 6 AND gate outputs.

3. (20%) Use D flip-flops and gates to design a binary counter with each of the following repeated binary sequences:
   (a) 2, 3, 6
   (b) 1, 3, 5, 7

4. (20%) Use the serial adder (A+B) in the textbook as an example to design a serial subtractor (A-B).

5. (20%) Frequency divider:
   (a) Design a frequency divider to provide the output signal with frequency as 1/3 of the that of the original signal.
   (b) Design a frequency divider to provide the output signal with frequency as 1/6 of the that of the original signal.

