1. A common defect in silicon chips is for one signal wire to always get a constant logic value 0 (1, respectively); it is called a stuck-at-0 (stuck-at-1, respectively) fault. Consider the single-cycle processor for the following instructions: ld, sd, add, sub and beq.

a). Which instruction(s) could fail to operate correctly if the ALUSrc wire is stuck at 0?
ld and sd would fail.

b). Which instruction(s) could fail to operate correctly if the MemtoReg wire is stuck at 1?
add and sub which belong to R-type instruction would fail.

c). Which instruction(s) could fail to operate correctly if the ALUop0 wire is stuck at 0?
beq would fail.

2. Consider the execution of the machine instruction 00*CE*3623h*ex* on the single-cycle processor.

a). What are the values of the signals: Branch, MemRead, MemtoReg, ALUOp, MemWrite, ALUSrc and RegWrite?
0x00CE3623 = 0000 0000 1100 1110 0011 0110 0010 0011
opcode = 0100011 is S-type
funct3 = 011 is sd
Hence, the answer would be Branch is 0, MemRead is 0, MemtoReg is 1/0(don’t care), ALUOp is 00, MemWrite is 1, ALUSrc is 1, and RegWrite is 0.

b). What are the input values of the ALU? You can use Reg[x] to denote the value of register x.
Input of ALU in sd instruction are rs1 and imm.
rs1 is 11100 = Reg[28]
imm is 0000 0000 1100 = 12.

3. Assume that the positive edge-triggered clocking methodology is adopted and the logic blocks used to implement the single-cycle processor have the following delay values:

I-Mem/ D-Mem	Register File	Mux	ALU	Adder	Single Gate	PC Read	Register Setup	Sign Extend	Control
230 ps	130 ps	20 ps	180 ps	130 ps	5 ps	20 ps	10 ps	30 ps	30 ps

a). What is the latency of an add instruction (i.e., what is the minimum clock period to ensure that this instruction works correctly)?

Instruction add need PC read(20ps), I-Mem(230ps), Register File(130ps), mux(20ps), Adder(130ps), mux(20ps), and Register Setup(10ps). Totally, it takes 560ps.

b). What is the latency of an ld instruction (i.e., what is the minimum clock period to ensure that this instruction works correctly)?

Instruction ld need PC read(20ps), I-Mem(230ps), Register File(130ps), Adder(130ps), D-Mem(230ps), mux(20ps), and Register Setup(10ps). Totally, it takes 770ps.

c). What is the latency of an sd instruction (i.e., what is the minimum clock period to ensure that this instruction works correctly)?

Instruction sd need PC read(20ps), I-Mem(230ps), Register File(130ps), Adder(130ps), D-Mem(230ps). Totally, it takes 740ps.

4. Recall that the ALU introduced in Chapter 3 can support the set-less-than (slt) operation by setting the ALU operation to 0111. Now consider how to modify the single-cycle processor such that it can also execute the R-type instruction: slt rd, rs1, rs2.

a). Are additional logic blocks or wires needed? Justify your answer.

No. Instruction slt is similar to other R-type instructions, the only thing different between add and slt is ALUctrl signal, so the whole logic blocks and wires should be same.

b). Does the “Control” unit need any change? Justify your answer.

No. Control unit is used to decode opcode. The opcode of slt is same to other R-type instructions which means using same control unit can execute “slt” successfully with R-type datapath.

c). Does the “ALU control” unit need any change? Justify your answer.

Yes. Refer to the 4-1 pp.44, I need add a new line whose {funct7, funct3}={0000000 010}, ALU function is slt, ALUctr is 0111 in R-type

5. Assume that individual stages of a datapath have the following latencies:

IF	ID	EX	MEM	WB
300 ps	400 ps	450 ps	350 ps	250 ps

a). What are the clock periods in a five-stage pipelined processor and a single-cycle processor, respectively?
Pipeline: 450ps, single-cycle: 1750ps

b). What are the latencies of an sd instruction in a five-stage pipelined processor and a single-cycle processor, respectively?
Pipeline: 2250ps, single-cycle: 1750ps

c). If you can split one stage of the five-stage pipelined processor into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock period? Note that the new clock period must be minimum among all possible ways of splitting.
I will split EX stage into two part. New clock period become 400ps, and new latency become 2000ps.

6. Answer the following questions by assuming the clock rate is 500 MHz and no pipeline stalls occur.

a). If a 4-stage pipelined processor takes 50 ns to execute S instructions, how long will it take to execute 4S instructions?
Clock rate 500MHz -> clock period 2ns.
50-4*2=42(ns)/2=21. S=21+1=22 instructions. 4S=88 instructions.
It takes 8+87*2=182ns

b). Consider a pipelined processor which has N stages. If it takes 100 ns to execute S instructions and 340 ns to execute 4S instructions. What are N and S, respectively?
N*2+(S-1)*2=100 -> N+S=51
N*2+(4S-1)*2=340 -> N+4S=171
S=40, N=11.

7. Consider the following sequence of instructions executed on the five-stage pipelined processor. Assume that the execution starts in clock cycle 1.

and x28, x11, x29
ld x14, 8(x28)
ld x11, 4(x12)
ld x28, 0(x11)
sub x14, x28, x14
sd x11, 4(x14)

a). Assume both forwarding unit and hazard detection unit are not present in the processor. Insert a minimum number of NOP (no operation) instructions to ensure correct execution.

```
1    and x28, x11, x29
2    nop
3    nop
4    ld x14, 8(x28)
5    ld x11, 4(x12)
6    nop
7    nop
8    ld x28, 0(x11)
9    nop
10   nop
11   sub x14, x28, x14
12   nop
13   nop
14   sd x11, 4(x14)
```

b). Assume the processor has the forwarding unit and hazard detection unit. For each of the following three conditions, indicate in which clock cycle, it is true for the processor.

With forwarding unit and hazard detection unit, I get following instructions.

```
1    and x28, x11, x29
2    ld x14, 8(x28)
3    ld x11, 4(x12)
4    nop
5    ld x28, 0(x11)
6    nop
7    sub x14, x28, x14
8    sd x11, 4(x14)
```

i). All control signals to be stored in the ID/EX register are set to 0.

It means do nop. It's true in cycle 5 and cycle 7.

ii). The correct data is forwarded from the EX/MEM register to one ALU input.

Instruction 1 forward to Instruction 2 at cycle 4. Moreover, Instruction 7 forward to Instruction 8 at cycle 10.

iii). The correct data is forwarded from the MEM/WB register to one ALU input.

Instruction 3 forward to Instruction 5 at cycle 7. Moreover, Instruction 5 forward to Instruction 7 at cycle 9.

c). Assume the processor has the forwarding unit and hazard detection unit. How many clock cycles does the processor take to complete the execution of the code?

It takes 5+(8-1)=12 cycles.

8. Consider the sequence of branch outcomes: T, T, T, NT, NT, NT, NT, for a branch instruction that has been executed 7 times in a program, where T denotes taken and NT denotes not-taken.

a). What are the accuracy rates of the always-taken and always-not-taken predictors for this sequence of branch outcomes, respectively?

Accuracy of always-taken is 3/7

Accuracy of always-not-taken is 4/7

b). Consider a 1-bit dynamic predictor which starts at the NT state. What is the accuracy rate of the predictor for this sequence of branch outcomes?

Prediction will be: NT, T, T, T, NT, NT, NT

Accuracy is 5/7

c). Consider a 2-bit dynamic predictor which starts at the "strongly predict taken" state. What is the accuracy rate of the predictor for this sequence of branch outcomes?

Prediction will be: T, T, T, T, T, NT, NT

Accuracy is 5/7

9. Consider the execution of the following sequence of instructions on the five-stage pipelined processor:

add x10, x28, x29
sub x6, x31, x28
beq x28, x29, LABEL
sd x28, 0(x29)

Suppose the third instruction is detected to have an invalid target address and cause an exception in the ID stage (i.e., in clock cycle 4). What instructions will appear in the IF, ID, EX, MEM, and WB stages, respectively, in clock cycle 5? Note that each instruction in your answer should be one chosen from the given instructions, the NOP instruction (or bubble), and the first instruction of the exception handler.

Clock cycle 5:

IF	ID	EX	MEM	WB
sd x26, 1000(x0)	nop	nop	sub x6, x31, x28	add x10, x28, x29