Introduction to VLSI-Homework 4

1. Please design an unit inverter (shown as figure 1) with a V_{dd}=1.8V, I_d=10nA when V_i and V_o are 0.9V. Then, find the capacitance of the unit inverter using the following command in your Hspice file. Finally, based on the unit inverter, you have to design the different inverter buffer chain (shown as figure 2) with size of x,y,z to drve a load capacitance of 16 times of the capacitance of the designed unit inverter, respectively.

   Example for measure capacitance:

   .option captab=1

   .option dccap=1

   .meas dc cp find cap(Vi) at=0.9***Vi is the input of the unit inverter

2. Based on the problem 1, please run a Hspice transient simulation to check the output V_{o1}, V_{o2}, V_{o3} and V_{o4}, respectively. And estimate the tf and tr based on your simulation results. Where the input V_i is a square wave with a frequency of 25M Hz.

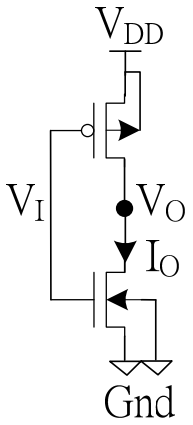

Fig. 1

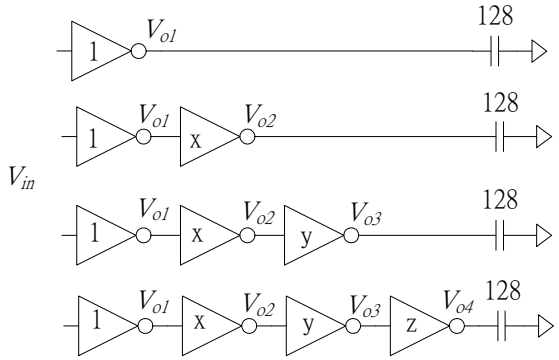

Fig.2

3. Midterm project:

(1) Please using the designed unit invert to design a register with function of CMOS positive-triger D latch shown as figure 1.31(b). Where the size of CMOS pass

transister are 1(NMOS):2(PMOS) same as the unit inverter. Showing your Hspice simulation results. Where the clock frequency is 25M Hz.Input data sequence is 1,1,0,1,0,0,1,0,1,1,1,0,0,1,0. Data rate is 25M bps.

(2) Based on the unit inverter shown as problem 1, please design a 2 input decoder shown as the figure 3 by using the footed and unfooted dynamic gate shown as the figure 9.23~25 of the text book, respectively. The load capacitance is 64 times of the capacitance of the unit inverter of the problem 1.

For each path, you have to show the results of your hand caculation. Including:

a. Number of stage N.

b. Average logic effort g_a.

c. The gate size for each path.

d. The average parasitic capacitance p_a .

Where B is 1.

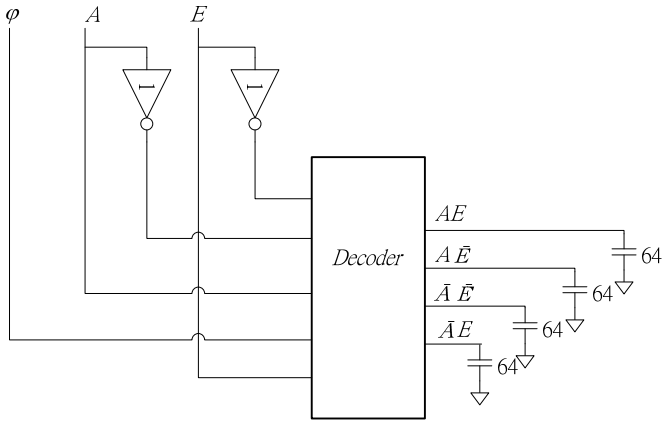

Fig.3