Introduction toVLSI- Home wrok 2

Tool:Hspice

Tecnology file: cic018.l

1. Please design the (W/L)n and (W/L)p of a nmos and a pmos transistor (showen in figure 1) for the following condition:
   V_D=0.9V,V_G=0.9V,V_{DD}=1.8V,I_{DS}=10uA and Gnd=0V.
   (1) Show the designed (W/L)n and (W/L)p.
   (2) For the designed NMOS and PMOS transistor, please show the I_{DS} vsus V_{DS} (0~1.8v) figure with the different V_G=0.7V,0.8V, 0.9V,1V, and 1.1V in the one figure.

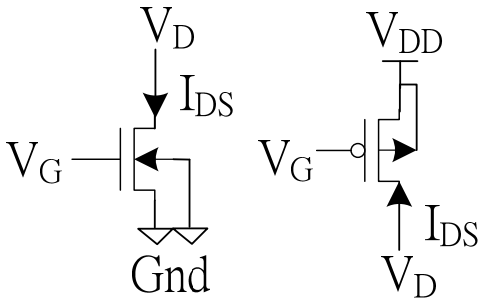

Fig. 1

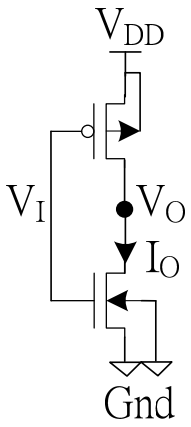

Fig. 2

2. Please design the (W/L)n and (W/L)p of a CMOS inverter(shown in figure 2) with the following different condition:
   (1) Where the V_{DD}=1.8V, V_I=0.9V, V_O=0.9V and Gnd=0V for the different I_O=10uA,20uA,30uA, respectively.
      a. Showing the designed (W/L)n and (W/L)p coresponds to the different I_O.
      b. Showing the V_O vsus V_I (0V~1.8V) figure.
      c. Showing your design steps and Hspice file.
   (2) Where the V_{DD}=1.8V, V_O=0.9V, I_O=20uA and Gnd=0V for the different V_I=0.7V,0.8V,0.9V,1V, and 1.1V.
      a. Showing the designed (W/L)n and (W/L)p coresponds to the different V_I.
      b. Showing the V_O vsus V_I (0V~1.8V) figure.
      c. Showing your design steps and Hspice file.