Exploring Alternative Device Structures To Bulk MOSFET for Low Power VLSI Systems

A project work submitted in the partial fulfilment of the requirements for award of the degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

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CERTIFICATE

This is to certify that the Project work entitled "**EXPLORING ALTERNATIVE DEVICE STRUCTURES TO BULK MOSFET FOR LOW POWER VLSI SYSTEMS"** is a certified record of work done by **AshaNali (1210413937), UdayKiran (1210413962), VivekRaju (1210413956),** submitted for the partial fulfillment of the requirements for the award of the degree of **Bachelor of Technology in Electronics and Communication Engineering**, GITAM University, Visakhapatnam during the academic year 2016-2017. This work is not submitted to any university for the award of any Degree/Diploma.

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We hereby declare that the project entitled **"EXPLORING ALTERNATIVE DEVICE STRUCTURES TO BULK MOSFET FOR LOW POWER VLSI SYSTEMS"** submitted in partial fulfilment of the requirements for the award of degree of **Bachelor of Technology** in **Electronics and Communication Engineering**. This dissertation is our original work and the project has not formed the basis for the award of any degree, associate ship, fellowship or any other similar titles and no part of it has been published or sent for the publication at the time of submission.

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ABSTRACT

As planar Bulk MOSFETs are scaled down, it is more and more difficult to achieve the scaled transistors with high performance. So there is a need for alternative device structures to meet the demands of low power VLSI systems. Significant research was done on Ultra-thin body devices namely, UTBB-SOI (Ultra-Thin Body with Back gate oxide- Silicon on Insulator), Tunnel FET and Multi gate (MG) structures.

In this major project, we focus on characterizing Tunnel FETs(TFET) so as to explore their performance trends, which are suitable for low power VLSI systems, such as high On-current to Off-current ratio (I_{ON}/I_{OFF}), Sub-60 mV/decade sub threshold slope, lower threshold roll-off and DIBL. As part of our research, we characterized TFETs (Homo and Hetero junction) based on III-V materials and simulate their performance by using Cadence tools.

Software Required:

1. Cadence Tools for circuit simulation
2. Verilog-A Simulator for analytical simulation (of Model)

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CHAPTER 1

INTRODUCTION

1. INTRODUCTION

Computing power has increased dramatically over the decades, enabled by significant advances in silicon integrated circuit (IC) technology led by the continued miniaturization of the MOS transistor. The rapid progress in the semiconductor industry has been driven by improved circuit performance and functionality together with reduced manufacturing costs. Since the 1960s, MOS transistor dimensions have been shrinking 30% every 3 years, as predicted by Moore's law depicted in Figure and scaling has in fact accelerated recently. While Moore's Law only describes the rate of increase in transistor density, reduction of the physical MOS device dimensions has improved both circuit speed and density in the following ways:

a) Circuit operational frequency increases with a reduction in gate length, LG, as ~1/LG; allowing for faster circuits

b) Chip area decreases ~ LG 2; enabling higher transistor density and cheaper ICs.

c) Switching power density ~ constant; allows lower power per function or more circuits at the same power.

Device scaling has been a relatively straightforward affair thus far, but physical limits are fast being approached, and new materials and device structures are needed to continue scaling trends.

The number of transistors on a chip has been increasing exponentially.

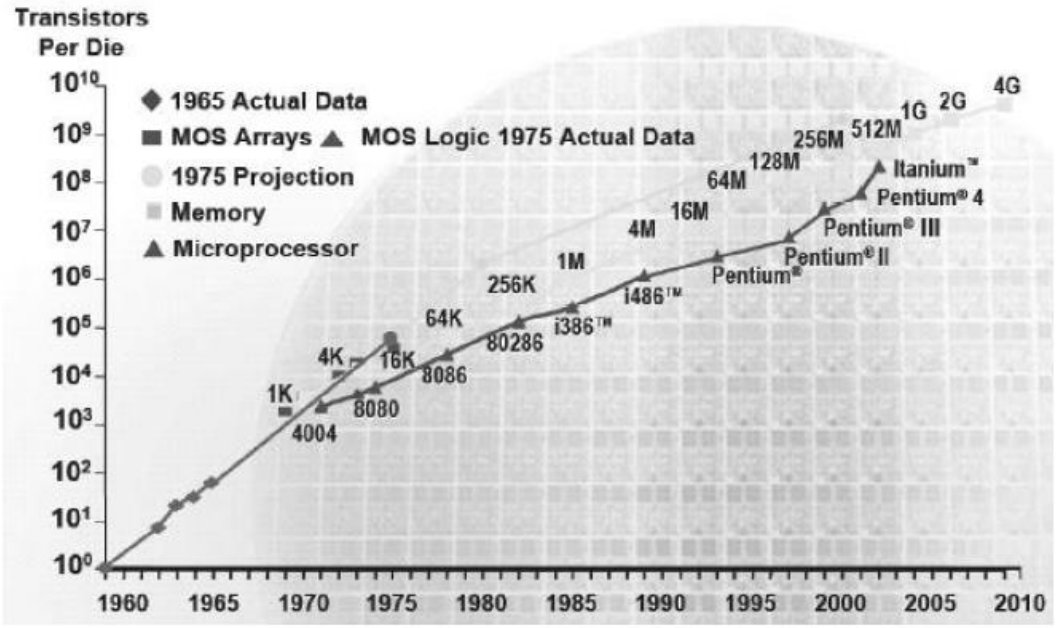

Fig 1.1 Moore's law

In this project, we are going to develop an alternative device structure for bulk MOSFETs since, they cannot be scaled beyond 50 nm node. Although we go for a 45 nm node, we come across some limitations like short channel effects, leakage currents, Subthreshold slope and low On and Off currents (I_{on} and I_{off}). In this thesis, we discuss about the development of Tunnel FET in three stages, where first stage tells us about the Bulk MOSFET and its limitations and need for alternative device structure. Second stage tells us about Tunnel FET device structure, working principle and its physical operation. In the third stage, we go for Model development of TFET, its implementation using Verilog-A and its schematic applications using Cadence tools. Finally, we present the results chapter and its analysis, also including the comparisons with the bulk MOSFETs.

CHAPTER 2

BULK MOSFET

2. BULK MOSFET

2.1. Device Description

MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor. It is capable of voltage gain and signal power gain.

- The MOSFET is the core of integrated circuit designed as thousands of these can be fabricated in a single chip because of its very small size.
- Every modern electronic system consists of VLSI technology and without MOSFET, large scale integration is impossible.
- The MOSFET is a four terminal device with source(S), gate (G), drain (D) and body (B) terminals.
- The body of the MOSFET is frequently connected to the source terminal so making it a three terminal device like field effect transistor.
- The MOSFET is very far the most common transistor and can be used in both analog and digital circuits.
- The structure of a bulk MOSFET is shown below.

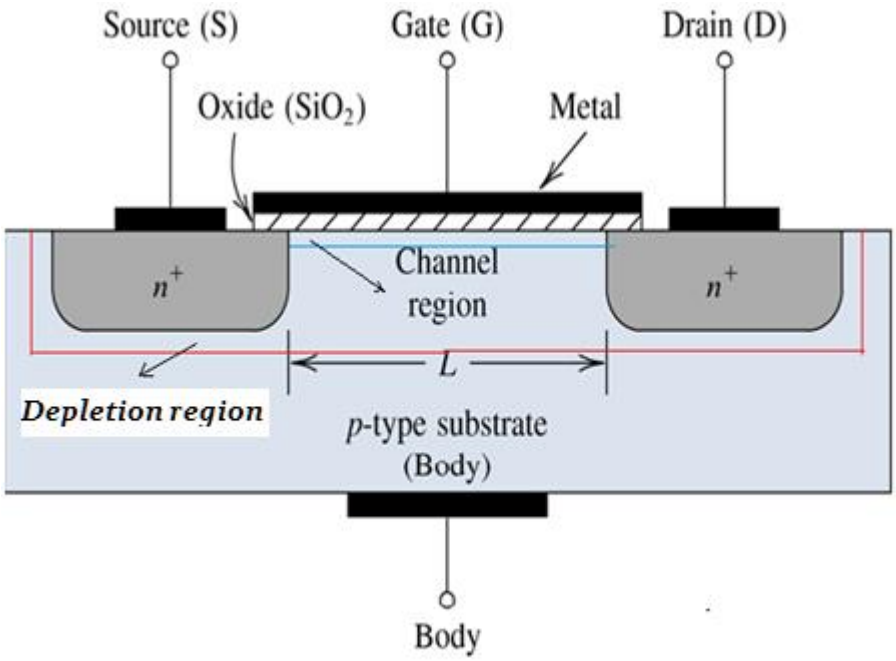

Fig 2.1 Structure of bulk MOSFET

- The MOSFET works by electronically varying the width of a channel along which charge carriers flow (electrons or holes).
- The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide.
- The MOSFET can be function in two ways:
    1. Depletion Mode
    2. Enhancement Mode

2.2. Physical Operation

The aim of the MOSFET is to be able to control the voltage and current flow between the source and drain. It works almost as a switch. The working of MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer which is located between source and drain terminal. It can be inverted from p-type to n-type by applying a positive or negative gate voltages respectively. When we apply the positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward with the substrate. The depletion region populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage, a hole channel will be formed under the oxide layer.

2.3. Threshold voltage

- The threshold voltage $V = VT$, corresponding to the onset of the strong inversion, is one of the most important parameters characterizing metal-insulator-semiconductor devices.
- Strong inversion occurs when the Vgs > V_t and the electron density becomes larger than the hole density in the channel.

- For this surface potential, the charge of the free carriers induced at the insulator–semiconductor interface is still small compared to the charge in the depletion layer.
- Various limitations of this Bulk MOSFET can be overcome by varying this Threshold Voltage and the corresponding equations are given.
- Threshold voltage is given by

$$V_T = V_{FB} + 2\emptyset_F + \frac{\sqrt{2\varepsilon_s q N_a (2\emptyset_F + V_{SB})}}{C_{OX}}$$

Where $\boldsymbol{V_{FB}}$ is flat band potential, $\boldsymbol{C_{OX}}$ is oxide capacitance, $\boldsymbol{\varepsilon_s}$ is permittivity of the substrate material, $\boldsymbol{q}$ is the electron charge, $\boldsymbol{N_a}$ is Doping concentration, $\boldsymbol{2\emptyset_F}$ is the surface potential, $\boldsymbol{V_{SB}}$ is the source-bulk voltage.

- The threshold difference due to an applied source-bulk voltage can therefore be expressed by

$$\Delta V_T = \gamma(\sqrt{(2\emptyset_F + V_{SB})} - \sqrt{2\emptyset_F})$$

Where $\boldsymbol{\gamma}$ is the body effect parameter given by

$$\gamma = \frac{\sqrt{2\varepsilon_S q N_a}}{C_{OX}}$$

2.4. Bottleneck to optimize the performance of MOSFET-Short Channel Effects

1. Subthreshold leakage
2. Gate Tunneling Current
3. Hot Carrier Effects (HCE)
4. Drain Induced Barrier Lowering (DIBL)
5. Threshold Roll-off

2.4.1. Subthreshold leakage:

- Subthreshold conduction or subthreshold leakage or subthreshold drain current is the current between the source and drain of a MOSFET.
- When the transistor is in subthreshold region, or weak-inversion region, that is, for gate to source voltages below the threshold voltage. Below figure shows the subthreshold leakage in an NMOSFET.

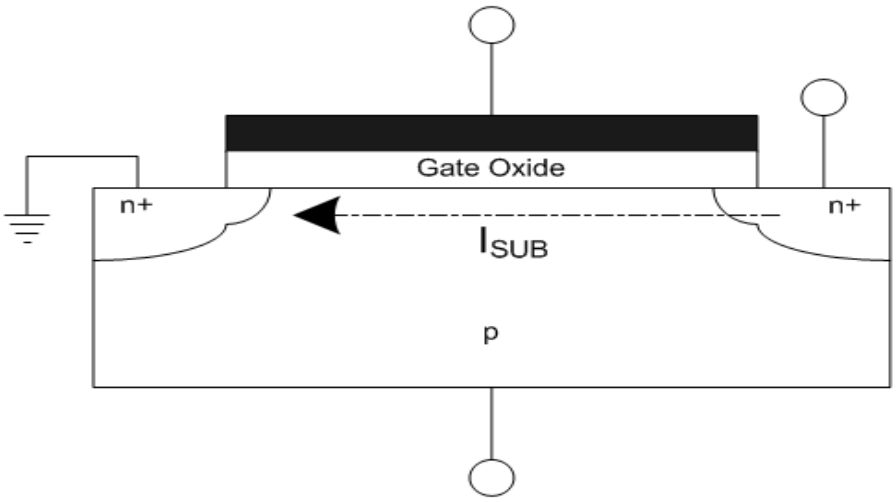

Fig 2.2 Sub threshold leakage in an NMOSFET

- In the past, the subthreshold conduction of transistors has usually been very small in the *off* state, as gate voltage could be significantly below threshold; but as voltages have been scaled down with transistor size, subthreshold conduction has become a bigger factor.
- Indeed, leakage from all sources has increased: for a technology generation with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption

2.4.2. Gate Tunneling Current:

These are actually Oxide tunneling currents. Bandgap of silicon dioxide is so large, that it can accommodate any number of electrons.

2.4.3. Hot Carrier Effects (HCE):

- As feature size decreases, Electric field in channel region increases which leads to gain high kinetic energy by holes & electron (Hot carrier).
- High kinetic energy helps them to inject inside gate oxide and form interface states, which in turns causes degradation of circuit performance. This effect is called Hot Carrier Effect.
- Cause of Hot Carrier Effect:
  1. In submicron device, channel doping is increased to reduce the channel depletion region (DIBL effect).

2. High doping increases threshold voltage.
3. Gate oxide thickness reduces to control the threshold voltage.
4. Due to channeling doping concentration, decreased channel length & reduced gate oxide thickness , hot carrier generated & injected to gate oxide.

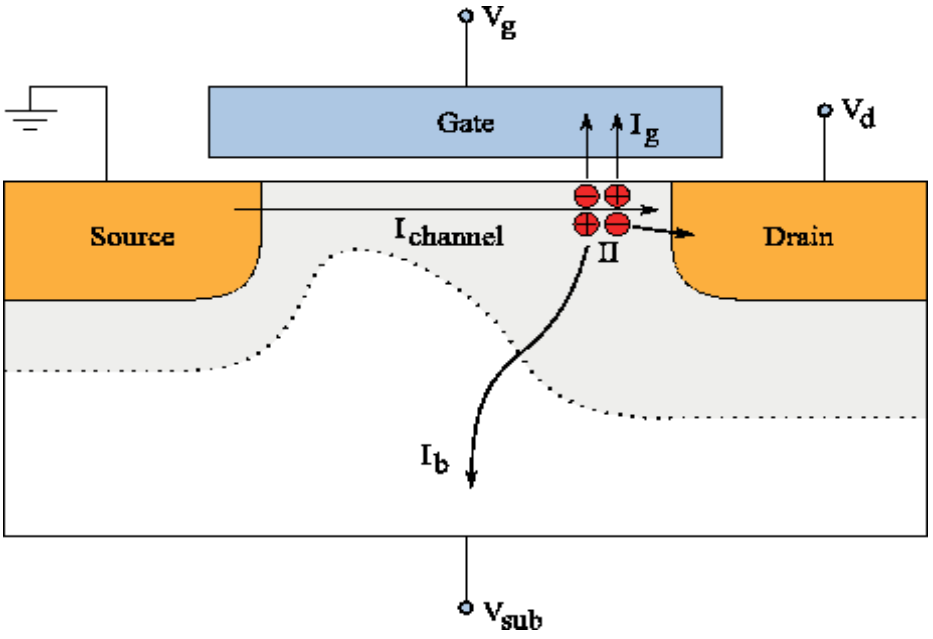

Fig 2.3 Hot Carrier Effect

2.4.4. Drain Induced Barrier Lowering (DIBL):

When the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge, punch through occurs. Punch through can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels. The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the surface (*VGS<VT0*), the carriers (electrons) in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage VGS and the drain-to-source voltage *VDS*. If the drain voltage is increased, the potential barrier in the channel decreases, leading to *drain-induced barrier lowering* (DIBL).

2.4.5. Threshold Roll-off:

Threshold voltage decreases rapidly with an increase in the Off current (Ioff), also threshold voltage decreases with decrease in channel length, which is called as Threshold voltage roll-off. If the off current goes on increasing, the channel length is not acceptable and hence scaling cannot be done, which is an effect of threshold roll-off.

2.5. Leakage Currents

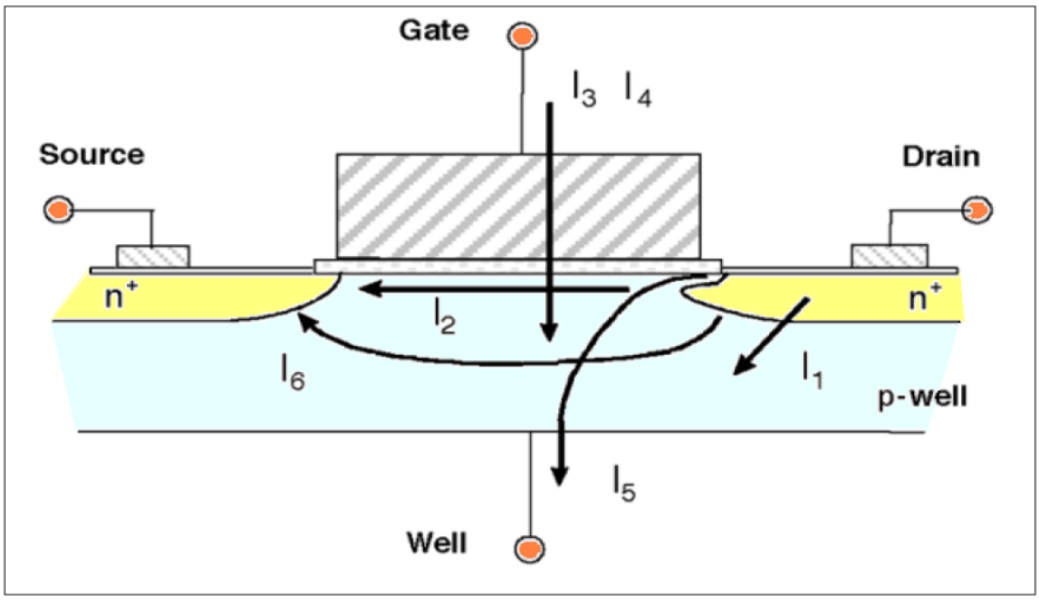

Fig 2.4 Leakage currents in a bulk MOSFET

❖ **Description of leakage currents:**

1. **Reverse bias pn Junction Leakage current (I1)**: It is due to the pn junction formed between the p type substrate and n type semiconductor material.
2. **Sub threshold Leakage current (I2)**: It is due to diffusion mechanism, which is because of a change in the concentration of the current. This leakage is the drain – source current of a transistor.
3. **Gate Direct Tunneling Leakage current (I3)**: These are actually Oxide tunneling currents. Bandgap of silicon dioxide is so large, that it can accommodate any number of electrons

4. **Leakage current (I4):** It occurs due to Hot carrier effect, where the electrons from the channel enter into oxide layer and get trapped and gradually degrade the device performance by accumulation over there.
5. **Gate Induced Drain Leakage current (I5**) : This is caused by high field effect in the drain junction of MOS transistors.
6. **Sub surface leakage path (I6):** This happens because of the large drain gap, and also called as Punch through.

2.6. Summary

- The Bulk MOSFETs, cannot scale be scaled down beyond 50 nm.
- The performance of Bulk MOSFET can be improved on by optimizing the device structure.
- Other way, an alternative device structure can be used for better performance.
- So, we go for two alternative device structures namely Multi gate FET and Tunnel FET.

CHAPTER 3

TUNNEL FET

3. TUNNEL FET

3.1. Device description

- In the quest for transistors that can replace CMOS as the power horse of the semiconductor industry, steep slope devices such as tunnel field-effect transistors (TFETs) have emerged as the leading contender because of their capability to keep scaling the supply voltage and lowering the power consumption.
- TFETs utilize interband tunneling as the current conduction mechanism, thus avoiding the Boltzmann-limited subthreshold swing of 60 mV/decade.
- To gain more insights into the benefits of tunnel FETs in low power circuit applications and make performance projections, a universal analytical TFET SPICE model that captures the essential features of the tunneling process has been developed.
- A simple analytic capacitance model of the gate drain capacitance has been developed and validated on two different TFET structures: a planar InAs double-gate TFET and an AlGaSb/InAs in-line TFET.
- Basic structure of TFET is shown in the below figure.

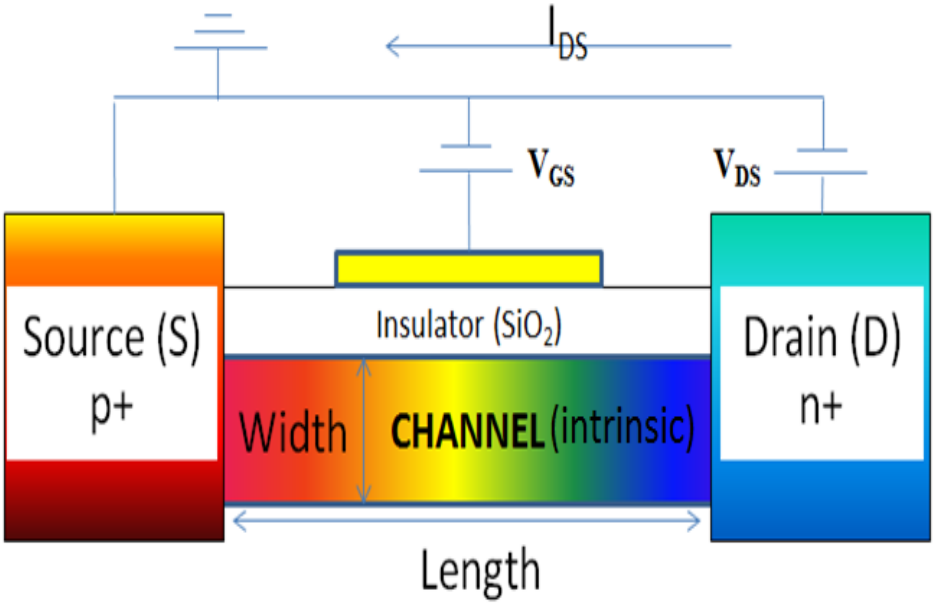

Fig 3.1 Tunnel FET structure(NTFET)

3.2. Working principle

Tunnel FETs utilize a MOS gate to control the band-to-band tunneling across a degenerate *p*-*n* junction. The schematic cross-section and energy band diagrams of *n*channel TFET in OFF and ON states are shown in Figure 3.2 a and b. The device is normally off. When zero bias is applied to the gate, the conduction band minimum of the channel is above the valence band maximum of the source, so band-to-band tunneling is suppressed. A tunneling window, *qVtw*, opens up as the conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel and the transistor is ON.

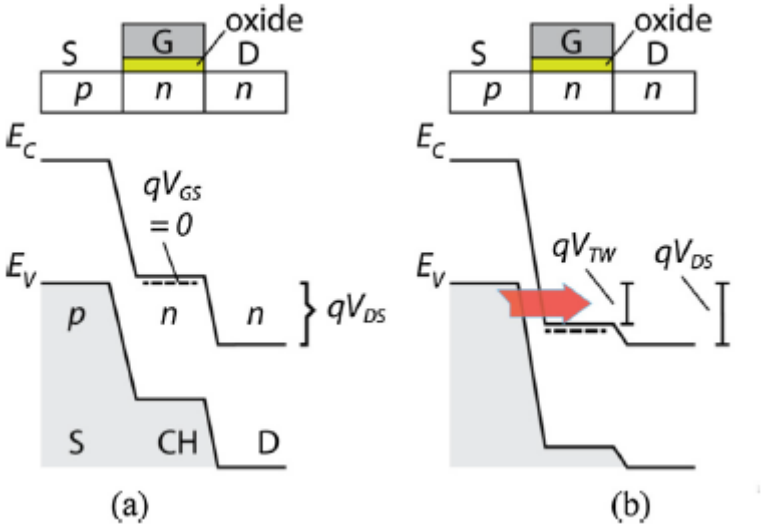

Fig 3.2 Band to band tunneling in N-channel enhancement mode TFET (a) OFF state (b) ON state

The principle of operation is the same for the *p*-channel TFET with source, channel and drain conductivity types switched. In the conventional mode of operation, the *n*-channel TFET tunnel current is suppressed when *Vgs* is low and the tunnel window at the source junction is opened with positive *Vgs*. However the TFET can turn on at the channel drain junction when the gate bias is sufficiently negative. As shown in Figure 1c when the gate bias is negative, the valence band maximum of the channel can be shifted above the conduction band minimum of the drain leading to electron tunneling from the channel into the drain. Therefore, the tunneling window opens up again, with the tunnel junction shifted from the sourcechannel junction to the drain-channel junction. When this happens the channel conduction changes from one carrier type to another and the transfer characteristic is said to be ambipolar. This behavior is generally universal across TFET

geometries. When the gate bias is still positive and the drain bias becomes negative, TFET behaves like an Esaki diode, with the signature NDR behavior appearing in the output characteristics.

3.3. Physical Operation

- The device is operated by applying gate bias so that electron accumulation occurs in the intrinsic region.
- At sufficient gate bias, band-to-band tunneling (BTBT) occurs when the conduction band of the intrinsic region aligns with the valence band of the P region.
- Electrons from the valence band of the p-type region tunnel into the conduction band of the intrinsic region and current can flow across the device.
- As the gate bias is reduced, the bands becomes misaligned and current can no longer flow.

3.4. Advantages of TFET

- Ultra-low power and ultra-low voltage.
- Short Channel Effects.
- Reduction in the leakage currents.
- Exceeding the Speed requirements due to tunneling effects.
- Similarity in fabrication process as compared with MOSFET.
- Higher ION/ IOFF current ratio
- The sub-threshold slope can be less than 60 mV/decade, such that potentially lower supply voltages can be used.

3.5. TFET as good switch

- Power dissipation is a fundamental problem for nanoelectronic circuits. Scaling the supply voltage reduces the energy needed for switching, but the field-effect transistors (FET's) in today's integrated circuits require at least 60mV of gate voltage to increase the current by one order of magnitude at room temperature.
- Tunnel FET's avoid this limit by using quantum mechanical band-to-band tunneling, rather than thermal injection (Bulk MOSFETs), to inject charge carriers into the device channel.

- Tunnel FETs based on ultrathin semiconducting films or nanowires could achieve a 100-fold power reduction over complementary metal-oxide-semiconductor (CMOS) transistors, so integrating tunnel FETs with CMOS technology could improve low power integrated circuits.
- Switching characteristics of TFET are good because of high ION/IOFF ratio and steeper sub threshold swing. In the past, the tunnel effect was known to disrupt the operation of transistors.
- As the bandgap, a large ON-current is difficult to achieve using a homo junction at the tunneling interface.
- Highly staggered heterojunctions exhibit suitable characteristics for these applications but require the development of a technological process in order to fully use these properties. Therefore, various architectures have been proposed to set up a n-TFET based on the (near) broken gap arsenide/antimonide heterojunctions.
- A vertical configuration with lateral drain contacts on an InAs/AlGaSb tunneling interface in line with the gate (named "T-shape" configuration in the following) was first proposed by Lu et al and realized by Li et al, demonstrating a large ON-current exceeding other TFET devices. Zhou et al further improved this result using a pure GaSb source.

3.6. Device Models of TFET

To gain more insights into the benefits of tunnel FETs in low power circuit applications and make performance projections, the TFET was developed in the following models.

1. Physics based model (Universal Tunnel FET model)
2. Look Up table based model (III – V Tunnel FET model)

3.6.1. Universal Tunnel FET model:

The model is valid in all four operating quadrants of the TFET. Based on the Kane-Sze formula for tunneling, the model captures the distinctive features of TFETs such as bias-dependent subthreshold swing, superlinear drain current onset, ambipolar conduction, and

negative differential resistance (NDR). A simple analytic capacitance model of the gate drain capacitance has also been developed and validated on two different TFET structures: a planar InAs double-gate TFET and an AlGaSb/InAs in-line TFET, and

good agreement is observed between the model and published simulations. The model is implemented in SPICE simulators using Verilog-A and in native AIM-Spice.

- **Kane-Sze model:**

  The TFET model is built on the expression for the current in a p+n+ tunnel junction described by the Kane–Sze tunneling formula, which is evaluated by integrating the product of charge flux and the tunneling probability in the tunneling window, where the tunneling probability is calculated by applying the Wentzel–Kramers– Brillouin (WKB) approximation.

3.6.2. III – V Tunnel FET model:

TFETs have asymmetrical source/drain doping which operates as reverse-biased, gated p-i-n tunnel diodes. In TFETs, the on-off switching is enabled by the gate-voltage induced band-to-band tunneling (BTBT) at the source-channel tunnel junction.

High on-state current (Ion), high on-off ratio and steep SS are critical aspects in TFET design, which allow the further scaling of the supply voltage (VDD) for power consumption reduction without jeopardizing the performance. Tremendous progress has been made in TFET prototype demonstration with significant improvement of the tunneling limited Ion and reduction of SS. The design of TFET involves the tunneling barrier reduction (e.g. low bandgap materials, hetero-band-alignment), gate electrostatics improvement (e.g. multi-gate or gate-all-around, ultra-thin body, effective oxide thickness (EOT) reduction), and low interface states to suppress the trap-assisted tunneling (TAT). III-V semiconductors are attractive for TFET fabrication due to their direct band-gaps and wide range of compositionally tunable band-alignment for tunnel barrier reduction.

- **InAs Homojunction TFET model:**

  The double-gate InAs homo junction TFET schematic is shown in below Figure corresponding to the simulation structure, which has a gate length (L_G) of 20nm, ultra-thin body thickness (T_{Ch}) of 5nm, high-k dielectric thickness (HfO_2) of 5nm at E_{OT} of 1nm with the source/drain doping of $4x1019cm^{-3}$(p+) and $6x1017cm^{-3}$(n+), respectively.

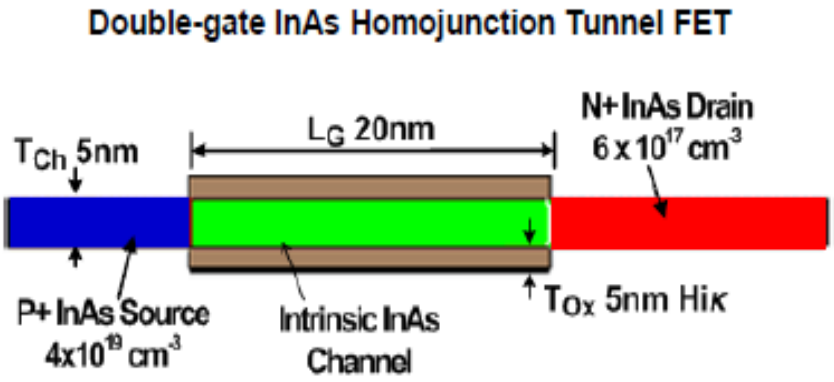

Fig 3.3 Structure of InAs Homojunction Tunnel FET

- **AlGaSb/InAs Heterojunction TFET model:**

  Below Figure shows the GaSb-InAs heterojunction FET schematic, which is calibrated with simulated structure, with a gate length (L_G) of 40nm, ultra-thin body (T_{Ch}) of 5nm, high-k dielectric thickness (HfO_2) of 5nm at E_{OT} of 1nm with the source/drain doping of 4x1019 cm^{-3} (p+) and 2x1017 cm^{-3} (n+) respectively.

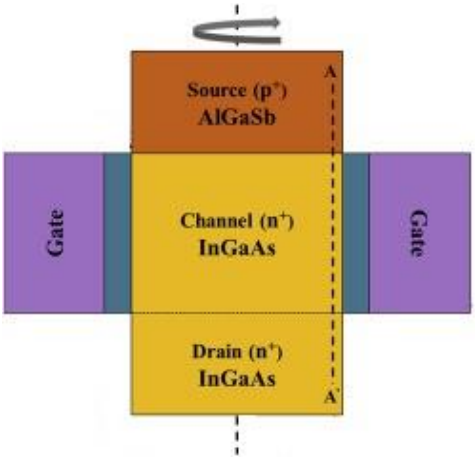

Fig 3.4 Structure of AlGaSb/InAs heterojunction Tunnel FET

Above figure shows the calibration of DC characteristics obtained from TCAD simulation with OMEN simulation results. The current at 0.5 V Vds shows good match at sub-threshold region and super-threshold region. Note that leakage current from TCAD simulation was 1 order lower. The Verilog-A model of GaSb-InAs HTFET uses 20 nm gate-length derived from this calibrated model.

CHAPTER 4

MODEL DEVELOPMENT OF TFET

4. MODEL DEVELOPMENT OF TFET

Tunnel FETs utilize an MOS-gate to control the band-to-band tunneling across a degenerate p–n junction. A tunneling window, qV_{TW}, opens up as the conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel and the transistor is ON. The principle of operation is the same for a p–i–n TFET, except that the n-channel TFET is an enhancement-mode device while the p–i–n TFET is inversion-mode.

The two-terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias-dependent tunneling window and a dimensionless factor which accounts for the superlinear current onset in the output characteristic.

The signature feature of the TFET is the decrease in subthreshold swing with decreasing drain current, which is well established in both simulations and experiments. The model assumes that this behavior is caused by the exponential band tails that arise from imperfections and lattice disorder due to impuri-ties, dopants, and phonons and extend into the band gap. This band tail, also known as the Urbach tail, represents a funda-mental limit to the steepness that can be practically achieved and thus becomes an adjustable element in the model.

- **Kane-Sze model:**

  The TFET model is built on the expression for the current in a p^+n^+ tunnel junction described by the Kane–Sze tunneling formula,which is evaluated by integrating the product of charge flux and the tunneling probability in the tunneling window, where the tunneling probability is calculated by applying the Wentzel–Kramers–Brillouin (WKB) approximation.

$$J_D = aV_R\varepsilon \exp\left(-\frac{b}{\varepsilon}\right)$$

$$a = \frac{q^3}{8\pi^2 h^2}\sqrt{\frac{2m_g^*}{E_g}} \qquad\qquad b = \frac{4\sqrt{2m_R^*}E_G^{3/2}}{3qh}$$

  where V_R is the reverse bias on the tunnel junction and physically accounts for the energy range, qV_R, over which the tunneling occurs, n is the maximum electric field in the reverse biased junction, and a and b are coefficients determined by the material

properties of the junction, m_R is reduced effective mass. E_G is the semiconductor band gap, h is the reduced Planck's constant.

The kane-Sze expression is adapted to the form

$$J_D = afV_{TW}\varepsilon \exp\left(-\frac{b}{\varepsilon}\right)$$

Where f is a dimensionless factor controlling both the cur-rent onset and saturation versus V_{DS}, which is based on the Fermi occupancy probability of filled states in the valence band and unfilled states in the conduction band.V_{TW} is the tunneling window related to crossing and uncrossing of energy bands.

- **Electric Field:**

  The maximum electric field in is taken to be linearly dependent on gate–source bias, V_{GS}, and drain–source bias, V_{DS},

  $$\varepsilon = \varepsilon_0(1 + \gamma_1 V_{DS} + \gamma_2 V_{GS})$$

  The electric field, ε_0 , is the built-in electric field at the source– channel tunnel junction when zero bias is applied to both gate and drain terminals. Parameters, Υ_1, Υ_2 are linear coefficients with unit of inverse volts. Increasing gate bias enhances the elec-tric field at the source–channel junction by both enlarging the volt-age drop (compared to the built-in voltage) and narrowing the tunneling barrier region. Increasing the drain bias has the same effect, but to a lesser degree because the drain field is screened by the gate electrode.

- **Subthreshold region:**

  In the subthreshold region, the drain current of a tunnel FET depends exponentially on the gate bias, which is dominated by the exponential decrease of the tunneling window with VGS below the threshold voltage. Accordingly, the tunneling window in the subthreshold region can be expressed by

  $$V_{TW} \approx U\, exp\left(\frac{V_{GS} - V_{TH}}{U}\right)$$

  Here, the factor, U, called the Urbach factor, is given by

  $$U = \gamma_0 U_0 + (1 - \gamma_0)U_0\left(\frac{V_{GS} - V_{OFF}}{V_{TH} - V_{OFF}}\right)$$

  $$U_0 = nk_BT/q$$

Where γ_0 is a parameter that controls how quickly the tunneling window closes with gate bias, n is the subthreshold ideality factor, V_{OFF} is the minimum V_{GS} voltage for which is valid. The threshold voltage V_{TH} is defined as the gate–source bias at which the source valence-band-maximum equals the channel conduction-band-min-imum (for an n-channel TFET). The expression causes the sub-threshold swing to decrease linearly with gate bias. When V_{GS} equals V_{OFF}, U is $\gamma_0 U_0$ and $\gamma_0$is a factor less than or equal to 1. When the gate bias is equal to the threshold voltage then U equals U_O.

- **Above-Threshold region:**

  According to Kane-Sze adapted expression, the drain current in the above-threshold region should be directly controlled by the tunneling window. Above-threshold the tunneling window should be given by

$$V_{TW} \approx V_{GS} - V_{TH}$$

  Which can be called the overdrive voltage.

- **Bridging the Subthreshold and above-threshold regions:**

  The following expression allows a contin-uous transition between the subthreshold and above-threshold regions,

$$V_{TW} = U\ ln\left[1 + exp\left(\frac{V_{GS} - V_{TH}}{U}\right)\right]$$

  When in the subthreshold region, the tunneling window grows exponentially with gate bias, but in the above-threshold region, it tends to a linear dependence on the gate bias. Whereas the mathematical expression in is able to describe both expo-nential and linear regions in a single equation, there is no physical basis to justify its accuracy in the transition region, 3nkT.

- **Super linear current onset:**

  The super linear onset of the output characteristic is another sig-nature behavior of the TFETs. Initially the following simple function f, was used to describe both the super linear onset and the saturation of drain current with drain–source bias.

$$f = \frac{1 - exp\left(-\frac{V_{DS}}{\Gamma}\right)}{1 + exp\left(\frac{V_{THDS} - V_{DS}}{\Gamma}\right)}$$

  Where Γ is a constant and V_{THDS} is the drain threshold voltage which corresponds to the minimum drain voltage needed to initiate the tunneling current. When V_{DS} equals zero, then and the tunneling current are zero. When V_{DS} becomes large, the function f

tends to one. In the low V_{DS} region the nonlinear turn-on of the drain current is well captured by *f*. The superlinear onset degrades drastically as V_{THDS} becomes bigger than 0.1V. At large V_{DS}, the function f saturates to 1, as desired.

The drain threshold voltage has been found to increase line-arly with gate voltage and then saturate at large V_{GS}. To account for this dependence, the drain threshold voltage was modified to,

$$V_{THDS} = \lambda \, tanh(V_{GS} - V_{OFF})$$

Where λ is a constant with the unit of volts and the voltage inside the tanh function is normalised to 1V.

4.1. DC models of TFETs

A tunnel FET is essentially a gated p–i–n tunnel diode. The asymmetrical source/drain junction causes tunnel FETs to have asymmetrical characteristics when the drain–source bias is reversed. When forwardly biased ($V_{DS} < 0$), the band-to-band tunneling current gradually gives way to the diffu-sion current as V_{DS} is decreased, resulting in NDR in the I_D–V_{DS}. Also due to the asymmetrical doping, the tunnel junction shifts from the source–channel junction to drain–channel junction when the gate bias reverses, resulting in ambipolar conduction. To fully make use of these features in circuit design, our model is extended into all four quadrants of operation:

1. $I_D[V_{GS} > V_{OFF}, V_{DS} > 0]$
2. $I_D[V_{GS} < V_{OFF}, V_{DS} > 0]$
3. $I_D[V_{GS} < V_{OFF}, V_{DS} < 0]$
4. $I_D[V_{GS} > V_{OFF}, V_{DS} < 0]$

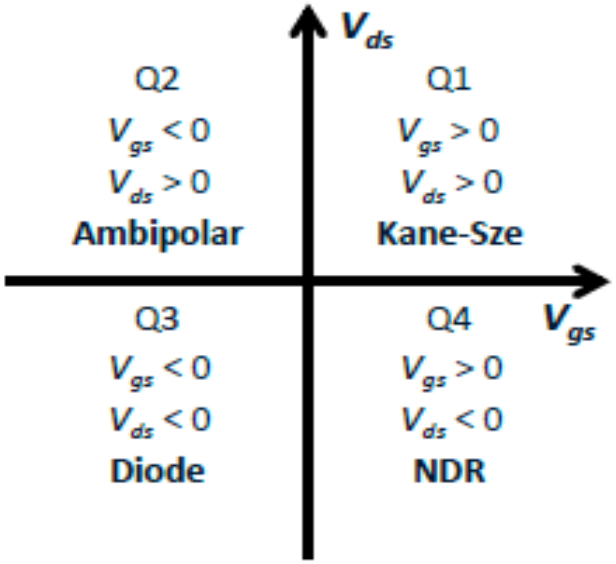

Fig 4.1 Operating regions in different quadrants

- **First Quadrant:** $I_D[V_{GS} > V_{OFF}, V_{DS} > 0]$

$$J_D = afV_{TW}\varepsilon \exp\left(-\frac{\mathrm{b}}{\varepsilon}\right)$$

- **Second Quadrant:** The ambipolar current: $I_D[V_{GS} < V_{OFF}, V_{DS} > 0]$

  Ambipolar current is not limited to p–i–n TFETs. At negative gate bias, a parasitic junction can form near the drain contacts even in an n-channel TFET.

  The ambipolar current is added to the model by copying the current for $V_{GS} > V_{OFF}$ to $V_{GS} < V_{OFF}$ and multiplying the current by a smoothing function, f_S.

$$I_D(V_{GS} < V_{OFF}) = I_D(V_{GS} > V_{OFF})f_s$$
$$f_s = \left(1 - (1 - s)tanh\left(-\frac{V_{GS} - V_{OFF}}{s}\right)\right)$$

  where s is an attenuation factor that sets the ratio of I_D ($V_{GS} < V_{OFF}$) to I_D ($V_{GS} > V_{OFF}$). In cases where the ambipolar current is sup-pressed, s can be set to a small number.

- **Third Quadrant:** $I_D[V_{GS} < V_{OFF}, V_{DS} < 0]$

  The third quadrant is the least used region. In this region, the current is defined using the universal diode current equation,

$$J_D = -J_0\left(exp\left(-\frac{V_{DS}}{nkT/q}\right) - 1\right)$$

- **Fourth Quadrant – the negative differential resistance region:**

$$I_D[V_{GS} > V_{OFF}, V_{DS} < 0]$$

When the drain–source bias, V_{DS}, is negative, the source–chan-nel junction is forward biased and behaves like a forward-biased tunnel diode. The NDR is included by modifying a model for the tunnel diode from Sze and Ng,

$$J = J_p \frac{V}{V_p} e^{1-\frac{V}{V_p}} + J_0\left(e^{\frac{V}{nkT/q}} - 1\right)$$

The parameters JP, J0, VP, n are fitting parameters. Parameter n is the diode ideality factor and shares the same value as n in subthreshold region.

4.2. Capacitance Model

The partitioning of gate capacitances between the source and drain in TFETs is significantly different from CMOS, primarily due to the difference in the distribution of inversion charge. Under positive bias, while the channel of an n-channel TFET is accumulated with electrons, the channel of a p–i–n TFET is inverted, which means that the inversion layer is formed at a higher V_{GS} for p–i–n TFETs. Because C_{GS} is much smaller compared to C_{GD} and will be dominated by interconnect capacitance, it is set as a constant. Noticing the similarity between the f function and the behavior of C_{GD} with increasing V_{GS} and V_{DS}, the f function is modified to model the behavior of C_{GD}.

$$C_{GD} = C_{GD,MIN} + \left(C_{GD,MAX} - C_{GD,MIN}\right)\frac{(1+\beta V_{GS}^m) - exp\left(-\frac{V_{GS}-V_{OFF}}{\Gamma'}\right)}{1 + exp\left(\frac{(V_{TH}+\alpha V_{DS}) - (V_{GS}-V_{OFF})}{\Gamma'}\right)}$$

- $C_{GD,MIN}$ and $C_{GD,MAX}$ are the approximate minimum and maximum values of C_{GD}, which is gate to drain capacitance.
- Parameters α, β, Γ', and m are fitting parameters, in which α and m are dimensionless, β has unit of $1/V_m$, and Γ' has unit of volts.

- VGS and VDS are the gate to source and drain to source capacitances respectively, VTH is the threshold voltage.
- C_{GD} is set to $C_{GD,MIN}$ in the other three quadrants.

4.3. TFET Model implementation

4.3.1. Cadence Tools

Cadence is an Electronic Design Automation (EDA) environment that allows integrating in a single framework different applications and tools (both proprietary and from other vendors), allowing to support all the stages of IC design and verification from a single environment. These tools are completely general, supporting different fabrication technologies. When a particular technology is selected, a set of configuration and technology-related files are employed for customizing the Cadence environment. This set of files is commonly referred as a *design kit*.

4.3.2. Verilog-A Model

The Verilog-A language is a high-level language that uses modules to describe the structure and behavior of analog systems and their components. With the analog statements of Verilog-A, you can describe a wide range of conservative systems and signal-flow systems, such as electrical, mechanical, fluid dynamic, and thermodynamic systems.

The model described above has been implemented in Verilog-A. Simple circuit level simulations were carried out using Cadence Virtuoso. A p-type device was emulated from the n-type device for this study. To ensure continuity and smoothness of the model in all bias conditions, a basic diode model was added to take into account negative V_{DS}. This results in the typical uni-directional conduction feature of a TFET.

These are the symbols for P-TFET and N-TFET, designed with the Verilog-A implementation.

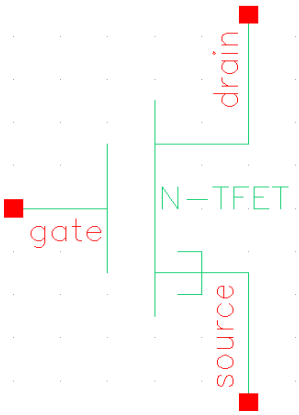

Fig 4.2 Symbol for P-TFET

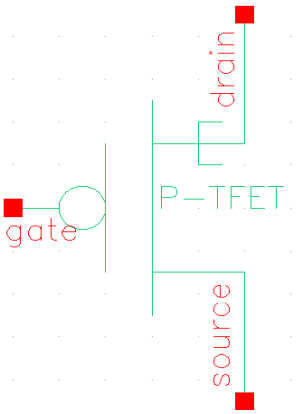

Fig 4.3 Symbol for N-TFET

4.4. Schematic Applications

- **TFET Inverter:**

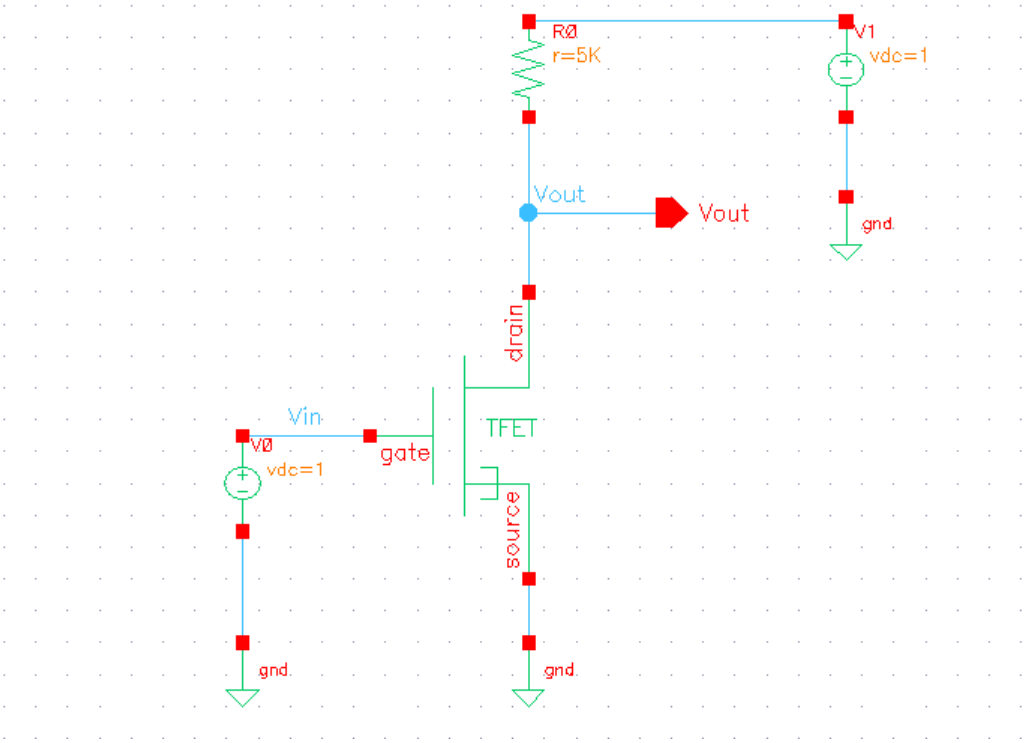

Fig 4.4 Schematic of TFET inverter

CHAPTER 5

RESULTS AND ANALYSIS

5. RESULTS AND ANALYSIS

The model for a III-V TUNNEL FET based on look up table model is created using Verilog A tool and the procedure is as follows.

5.1. Simulation steps

- The model of III-V Tunnel FET, both NTFET (homojunction InAs) and HNTFET (heterojunction AlGaSb/InAs) is developed using Verilog A and that is used for circuit simulation.
- Run Cadence applications by opening an xterm window and type login details and then create a directory and launch the virtuoso environment.
- Now create a new library (to contain circuits) so go to File -> New -> Library from the File menu of the Library Manager. Then fill in the name of the new library (e.g. Tutorial) in the dialog window, and leave the Path empty (this will create the library in the directory where you started icfb, you could also choose to set a path if you wanted another directory). Click on “Do not add any existing technology”.
- Start by clicking on the created library in the Library Manager window once, then go to File -> New -> Cell View and fill in with the cell name, Verilog A as the view name, and Composer - Schematic as the tool, then press OK.
- Verilog A editor window will open, write the code of the TFET module and type "esc"->":"->"wq"->"Enter" on the keyboard to save the module.
- Once the syntax is correct a dialog box will appear and ask you if you want to create a new symbol, click "Yes". The TFET model thus created can be used in the schematic for circuit simulation and analysis.

5.2. Analytical simulations results for NTET (Homojunction InAs):

The Look up table based TFET model is developed in Verilog A. For Homojunction (InAs) TFET, required parameters are mentioned in the below table and applying a bias voltages of 1v to drain then Ids versus characteristics is shown.

Table 1 Parameters for NTFET (Homojunction InAs):

Channel thickness (Tch)	5 nm
Oxide thickness(Tox)	2 nm
Width(w)	1 um
Length (l)	20 nm
Doping level concentration(Na)	1e15cm-3

5.2.1. Transfer characteristics :

- **Linear graph :**

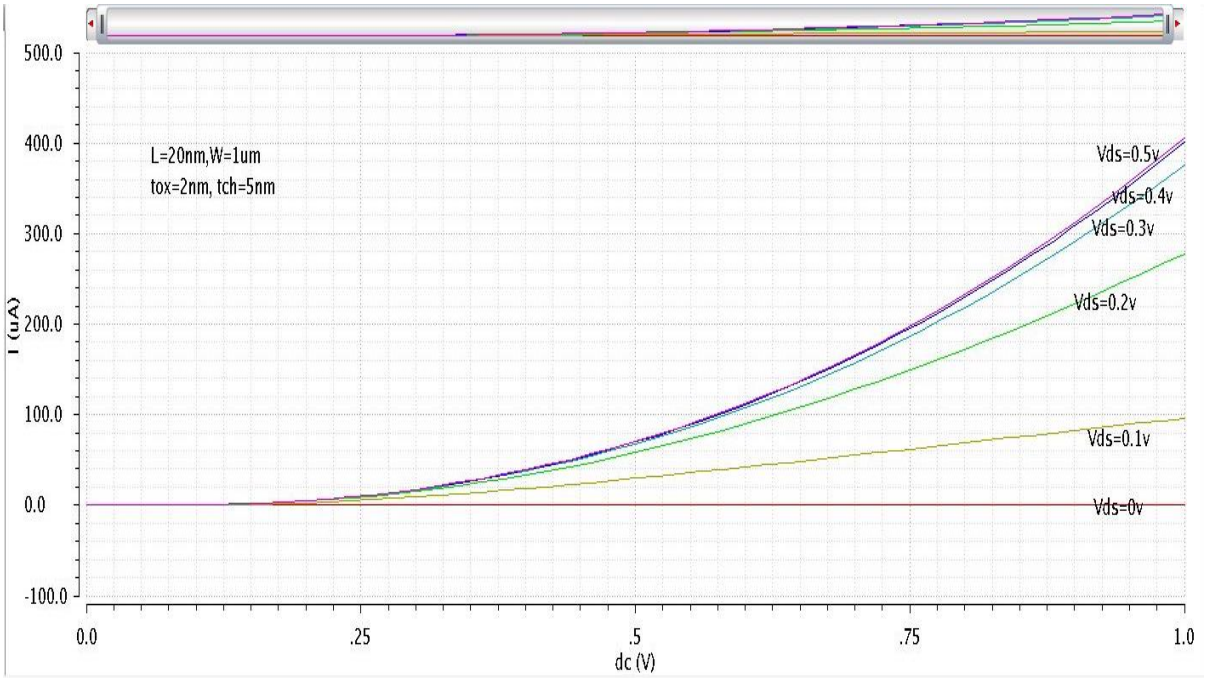

Fig 5.1 Simulation result for NTFET Id versus Vgs characteristics

The above graph shows the plot between drain current (Id) and gate to source voltage (Vgs), we can observe that an On current of 400 uA is observed for a drain to source voltage (Vds) of 0.5v and for an applied input voltage of 1v.The sweep rage for gate to source voltage (Vgs) is 0 to 1v.

- **logarithmic graph:**

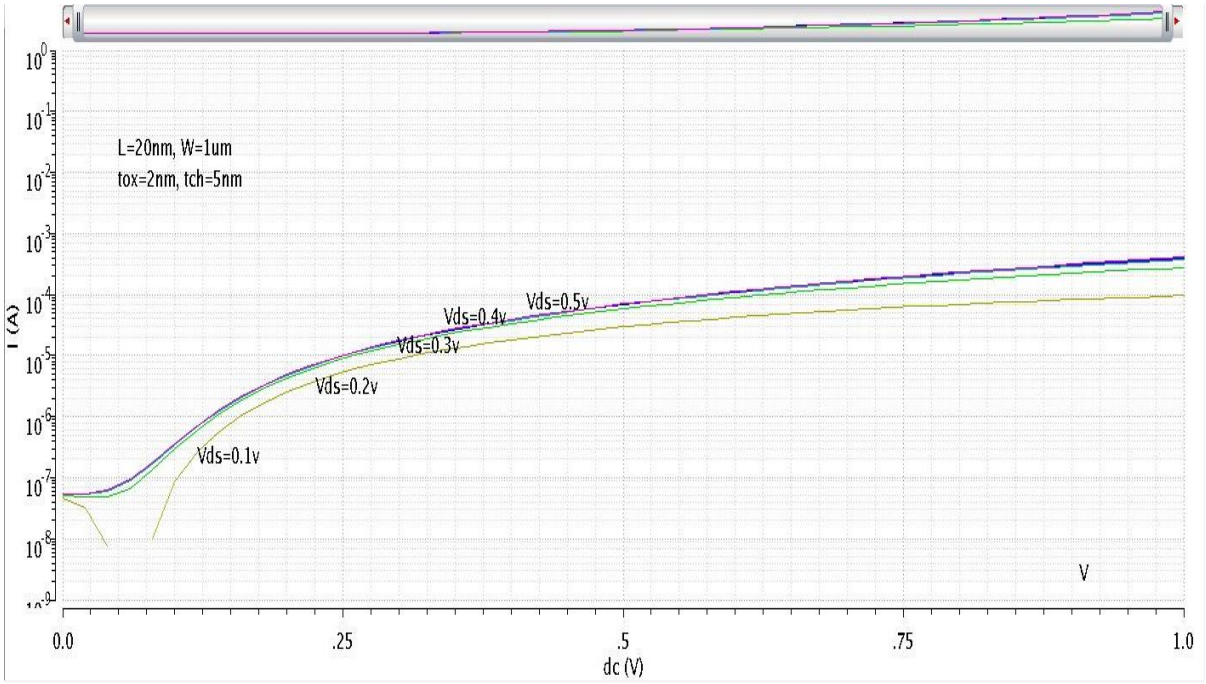

Fig 5.2 Simulation result for NTFET log Id versus Vgs characteristics

The above graph shows the plot between logarithmic values of Id (drain current) and Vgs (gate to source voltage). We can observe that On current is achieved for low value of Vgs as compared to bulk MOS.

5.2.2. Drain characteristics :

- **.linear graph:**

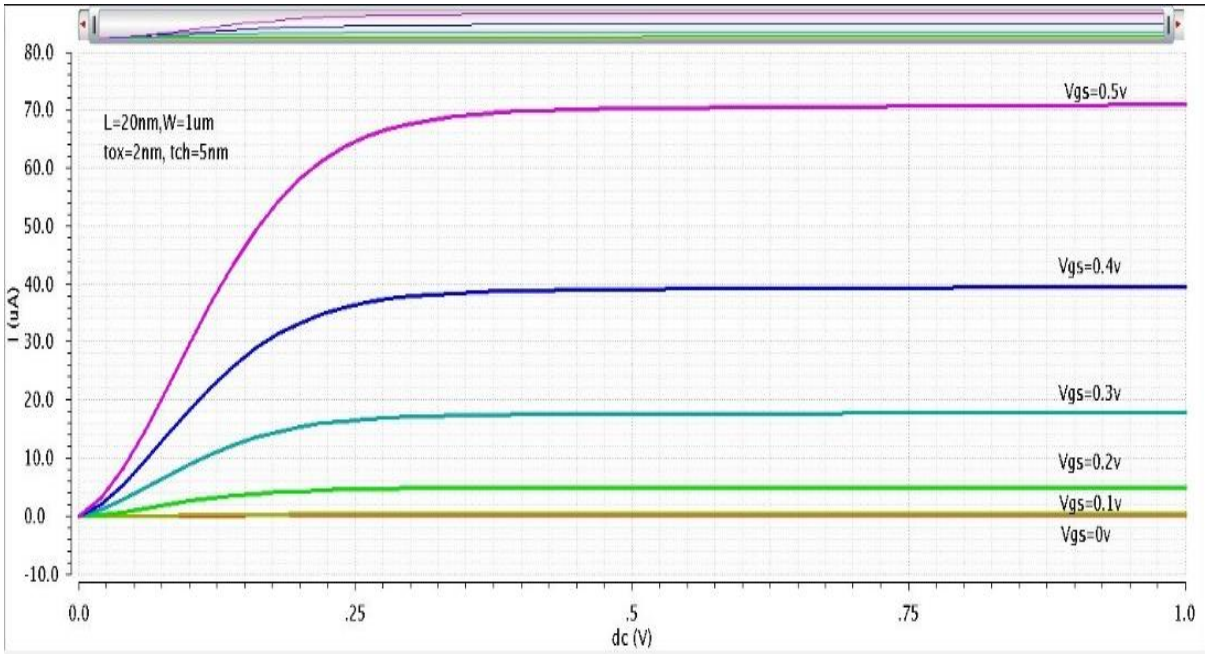

Fig 5.3 Simulation result for NTFET Id versus Vds characteristics

The above graph shows the plot between drain current (Id) and drain to source voltage (Vds), we can observe that an On current of 70 uA is observed for a drain to source voltage (Vgs) of 0.5v and for an applied input voltage of 1v. The sweep rage for drain to source voltage (Vds) is 0 to 1v. High On current is achieved for low Vds (drain to source voltage), as compared to MOSFET, also less overdrive is observed in MOS, compared to TFET.

5.2.3. Graph showing Ambipolar nature(symmetric) of NTFET :

- **Ambipolar nature at high Vds:**

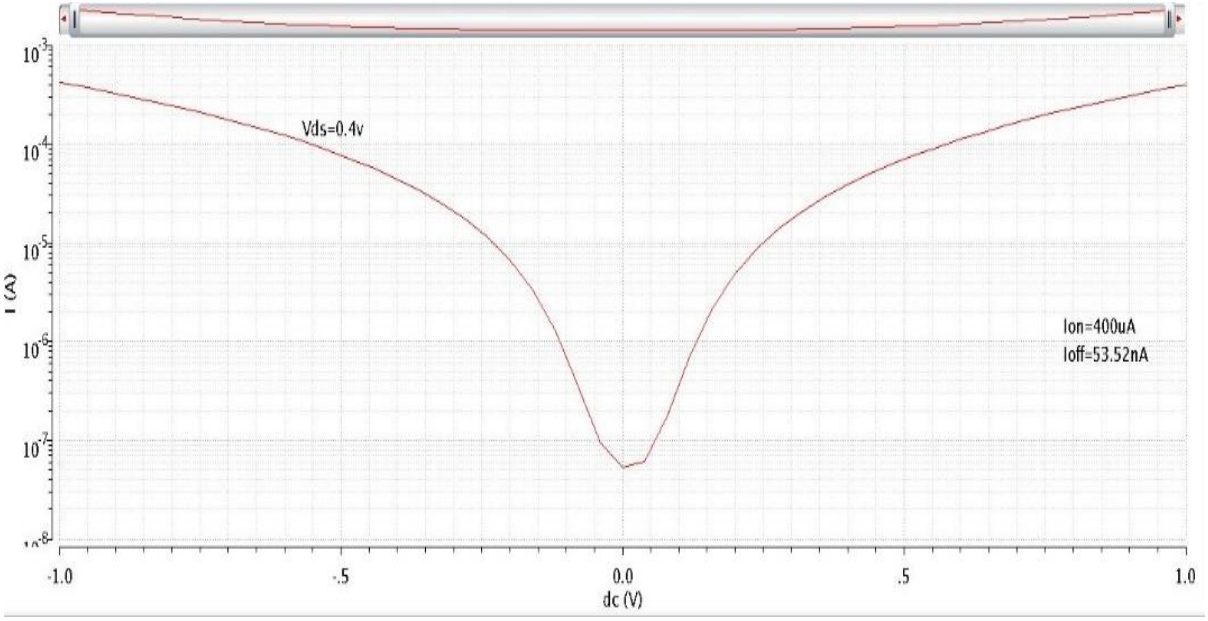

Fig 5.4 Simulation result for NTFET log Id-Vgs at Vds=0.4V

The above graph shows the plot between logarithmic values of Id Vs Vgs and at high Vds where we applied Vds=0.4 v, ambipolarity of NTFET can be observed, where it shows the symmetric nature for both positive and negative Vgs sweep range. Here we can observe an On current of 400 uA and Off current of 53.52 nA.

- **Ambipolar nature(asymmetric) at low Vds :**

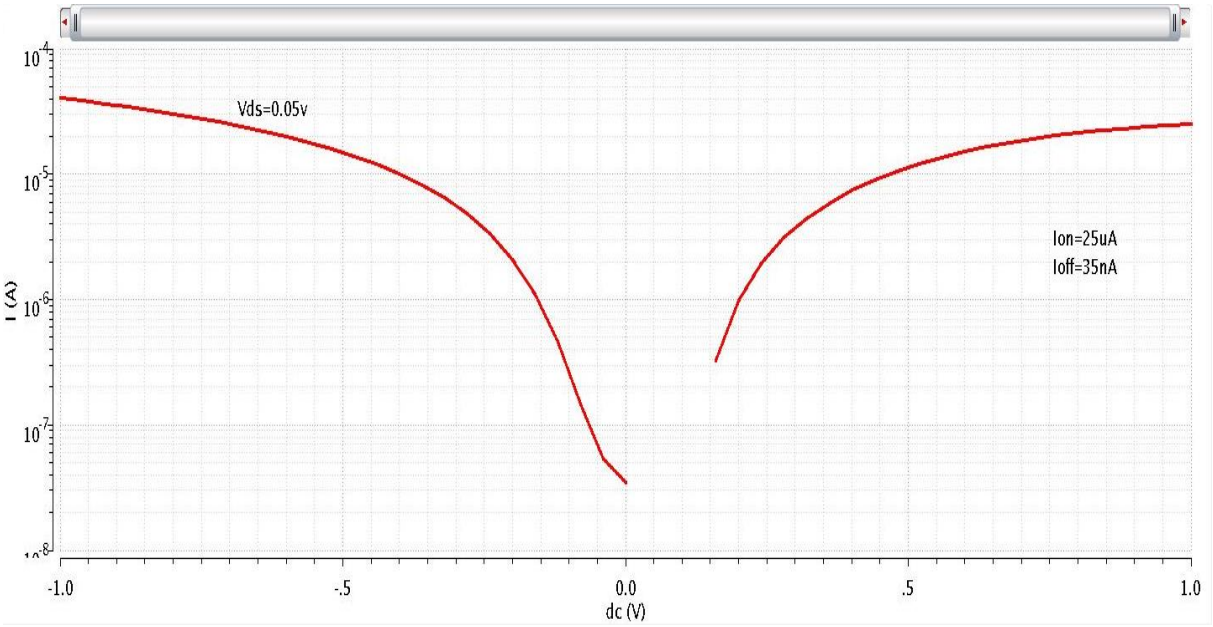

Fig 5.5 Simulation result for NTFET log Id_Vgs at Vds=0.05V

The above graph shows the plot between logarithmic values of Id Vs Vgs and at low Vds where we applied Vds=0.05 v, ambipolarity is not observed here since it does not show the symmetric nature and there is a slight difference in the on and off currents for both positive and negative Vgs sweep range. Here we can observe an On current of 25 uA and Off current of 35 nA for positive Vgs.

5.2.4. Inverter characteristics(dc) for NTFET:

- **DC Response:**

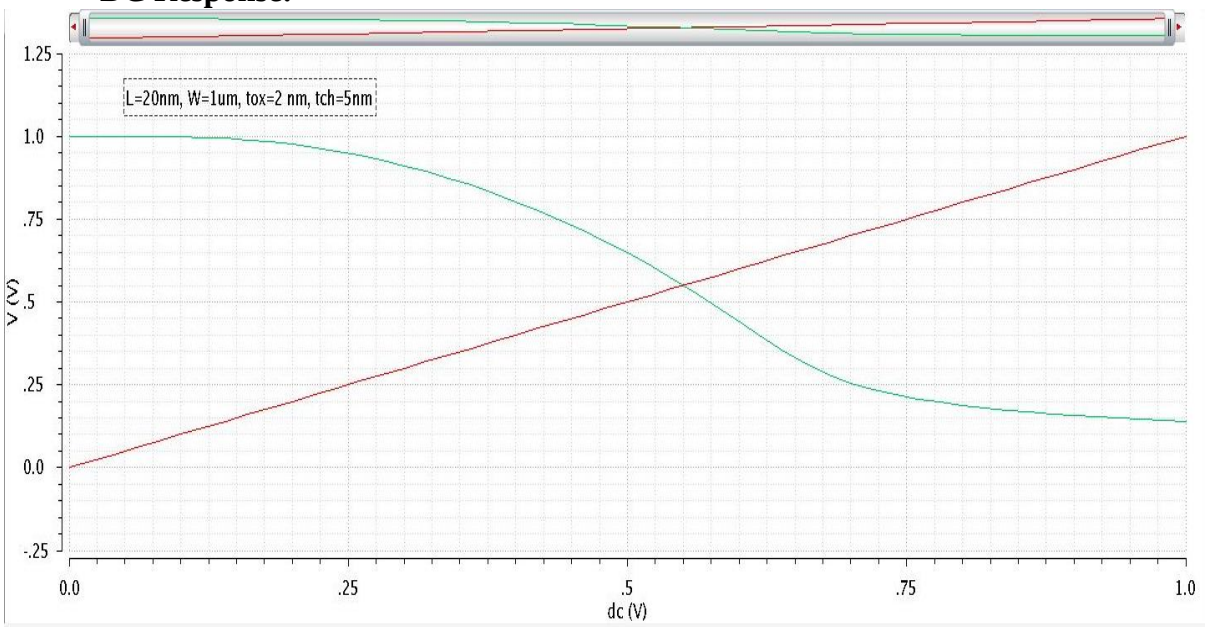

Fig 5.6 Simulation result for NTFET Inverter characteristics

- **Transient response :**

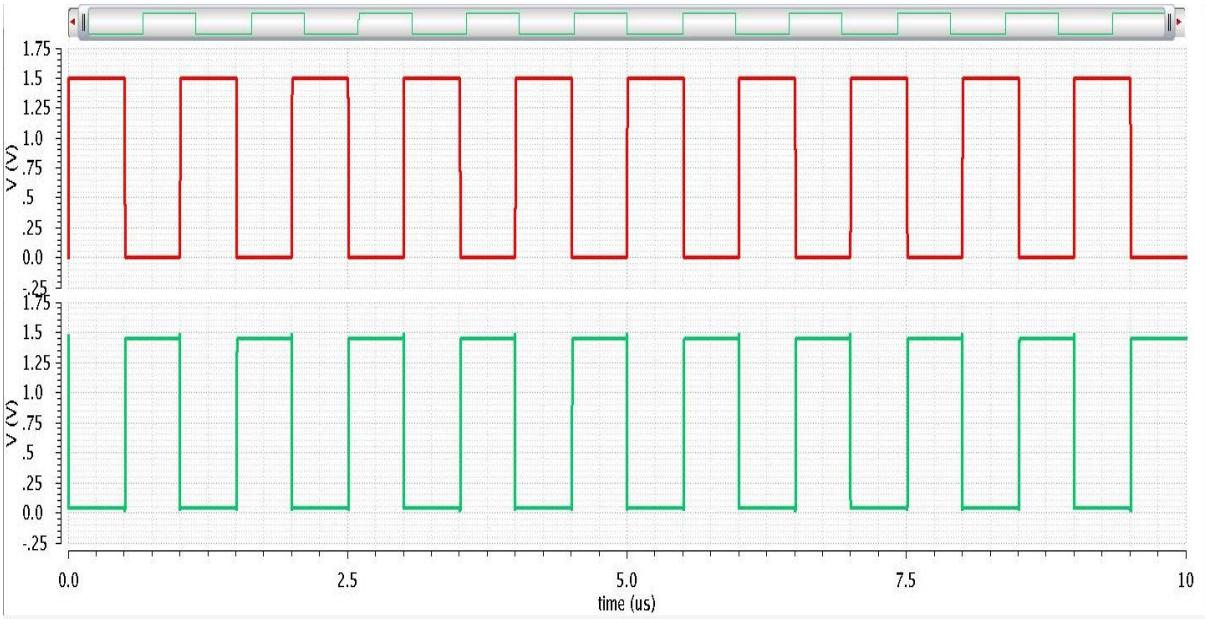

Fig 5.7 Simulation result for transient response of NTFET Inverter

The above two graphs depict the Inverter characteristics in both DC and Transient analysis respectively. For an inverter, if the noise margin obtained is low, it is not good fot the TFET operating, we need to get a high noise margin.

5.3. Analytical simulations results for HNTFET(AlGaSb/InAs):

The Look up table based TFET model is developed in Verilog A. For Heterojunction (AlGaSb/InAs) TFET, required parameters are mentioned in the below table and applying a bias voltages of 1v to drain then Ids versus characteristics is shown.

Table 2 Parameters for HNTFET (AlGaSb/InAs)

Channel thickness (Tch)	5 nm
Oxide thickness(Tox)	2 nm
Width(w)	1 um
Length (l)	20 nm
Doping level concentration(Na)	1e15 cm-3

5.3.1. Transfer characteristics :

- **linear graph:**

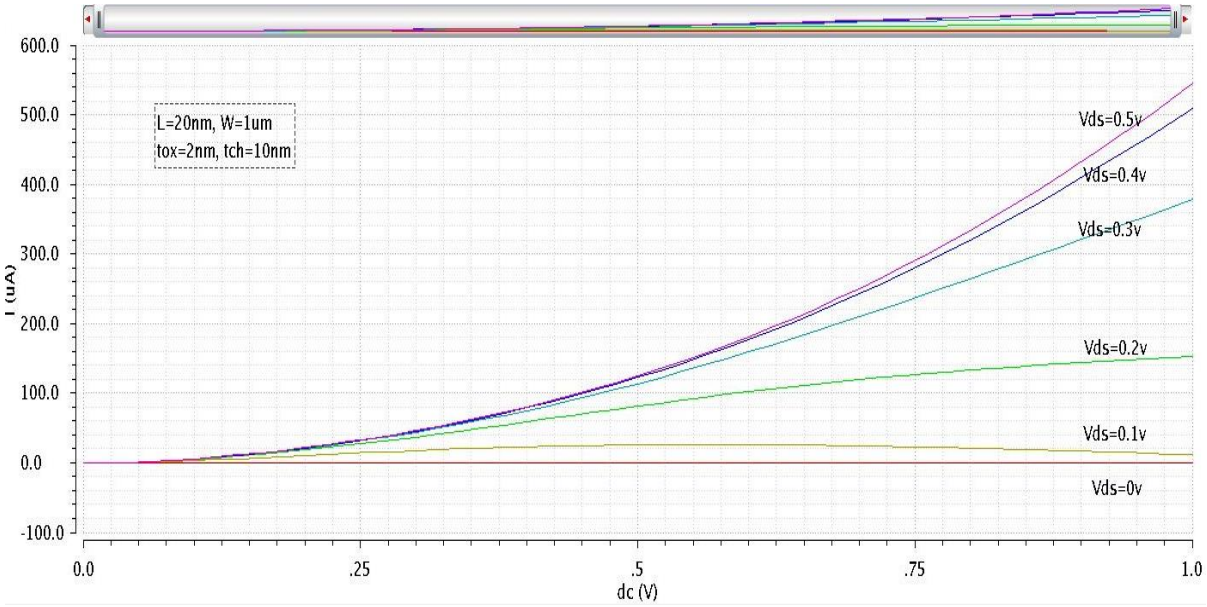

Fig 5.8 Simulation result for HNTFET Id versus Vgs characteristics

The above graph shows the plot between drain current (Id) and gate to source voltage (Vgs)for a HNTFET , we can observe that an On current of 550 uA is observed for drain to source voltage (Vds) of 0.5v and for an applied input voltage of 1v.The sweep rage for gate to source voltage (Vgs) is 0 to 1v.

- **logarithmic graph:**

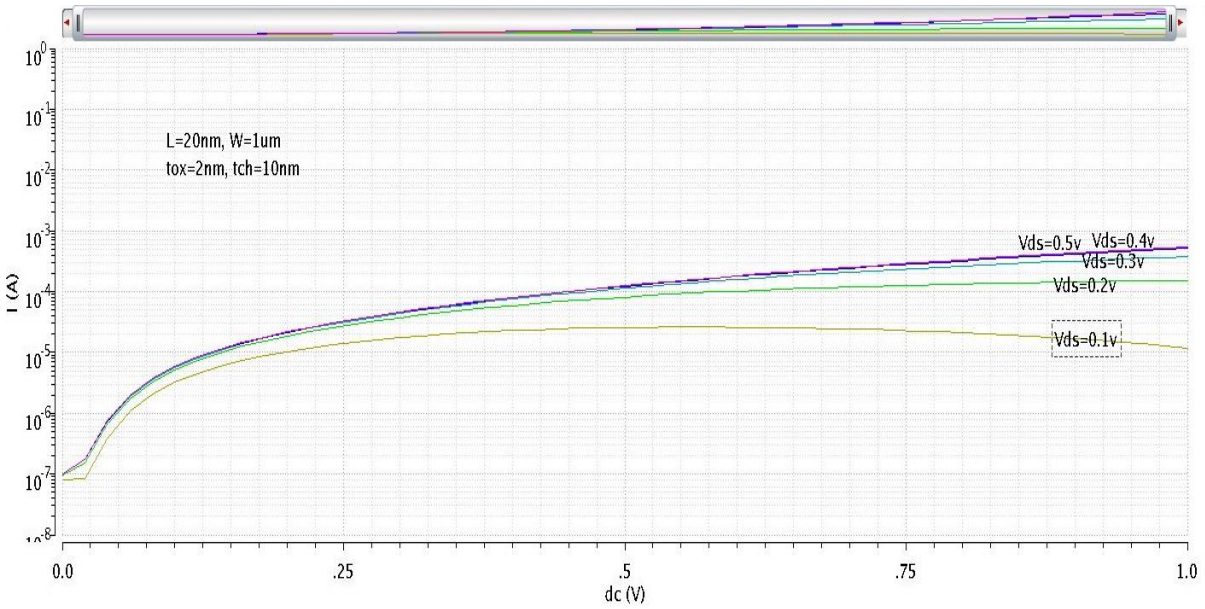

Fig 5.9 Simulation result for HNTFET log Id versus Vgs characteristics

The above graph shows the plot between logarithmic values of Id (drain current) and Vgs (gate to source voltage). We can observe that high On current is achieved for HNTFET as compared to NTFET for same value of Vds.

5.3.2. Drain characteristics :

- **linear graph**

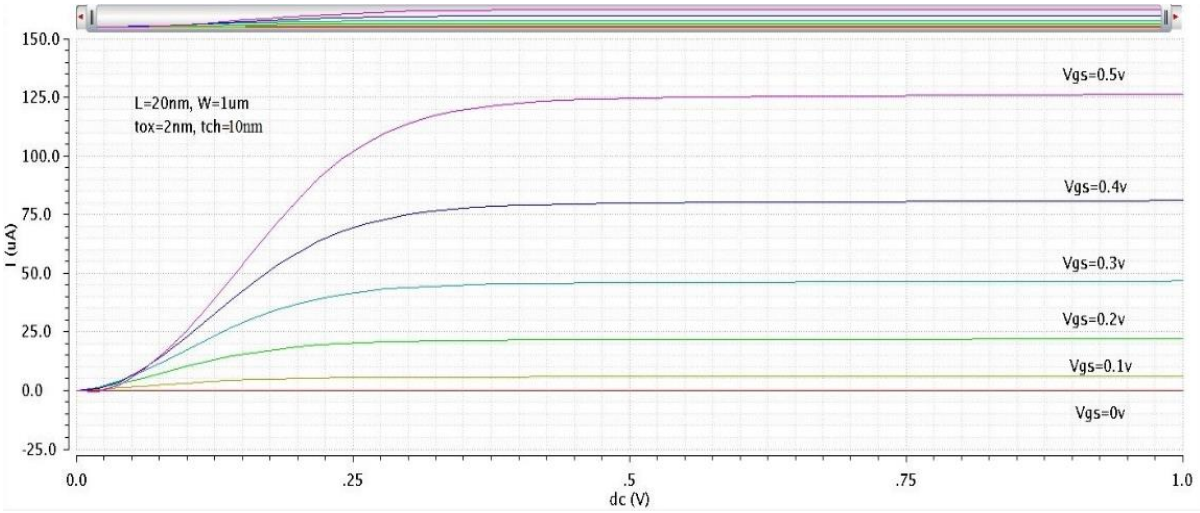

Fig 5.10 Simulation result for HNTFET Id versus Vds characteristics

The above graph shows the plot between drain current (Id) and drain to source voltage (Vds), we can observe that an On current of 125 uA is observed for a drain to source voltage (Vgs) of 0.5v and for an applied input voltage of 1v. The sweep rage for drain to

source voltage (Vds) is 0 to 1v. High On current is achieved for low Vds (drain to source voltage), as compared to NTFET.

5.3.3. Graph showing Ambipolar nature(symmetric) of HNTFET :

- **Ambipolar nature(symmetric) at high Vds:**

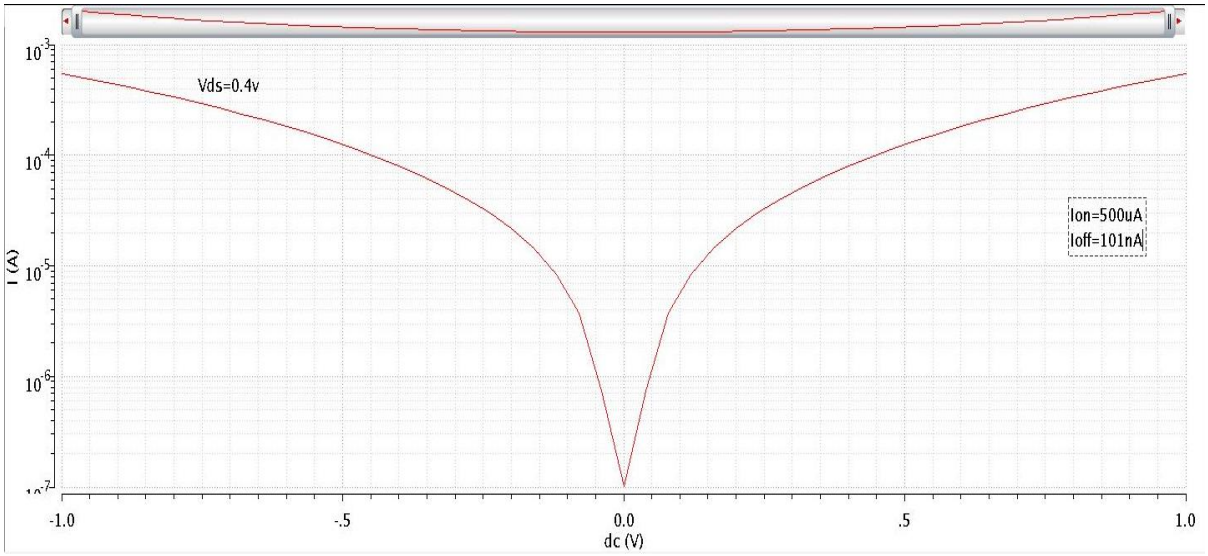

Fig 5.11 Simulation result for HNTFET log Id-Vgs at Vds=0.4V

The above graph shows the plot between logarithmic values of Id Vs Vgs and at high Vds where we applied Vds=0.4 v, ambipolarity of HNTFET can be observed, where it shows the symmetric nature for both positive and negative Vgs sweep range. Here we can observe an On current of 500 uA and Off current of 101 nA, which is higher as compared to NTFET.

- **Ambipolar nature(symmetric) at low Vds:**

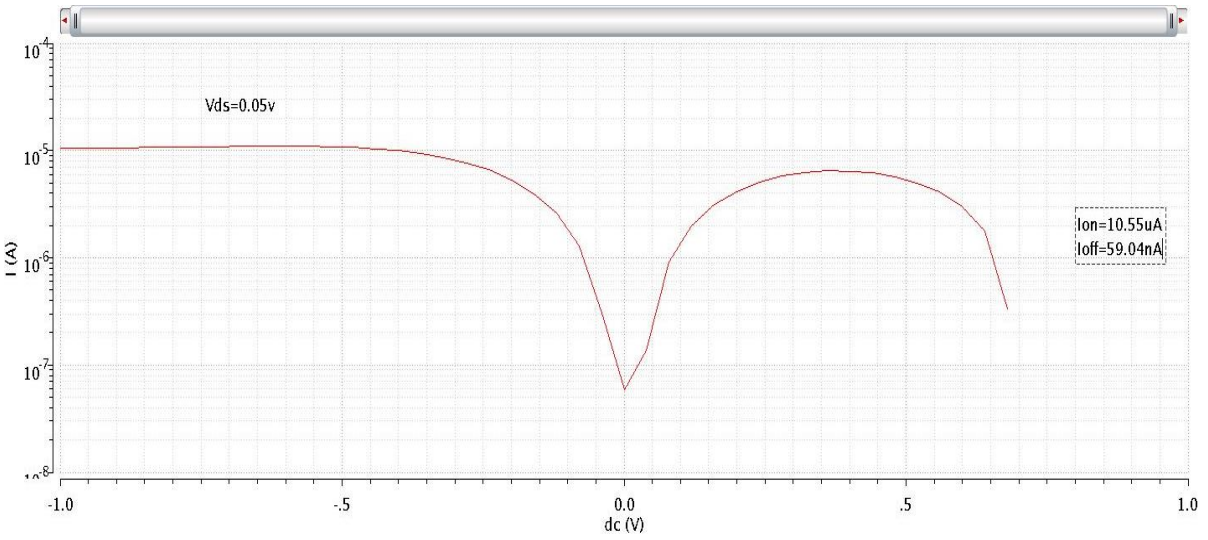

Fig 5.12 Simulation result for HNTFET log Id Vgs at Vds=0.05V

The above graph shows the plot between logarithmic values of Id Vs Vgs and at low Vds where we applied Vds=0.05 v, ambipolarity IS maintained but a slight difference in the on and off currents for both positive and negative Vgs sweep range. Here we can observe an On current of 10.55 uA and Off current of 59.04 nA for positive Vgs. Here Off current is maintained for both high and low Vds and doesn't go low for low Vds, as in the case of NTFET.

5.3.4. Inverter characteristics(dc) for Heterojunction TFET:

- **DC Response**

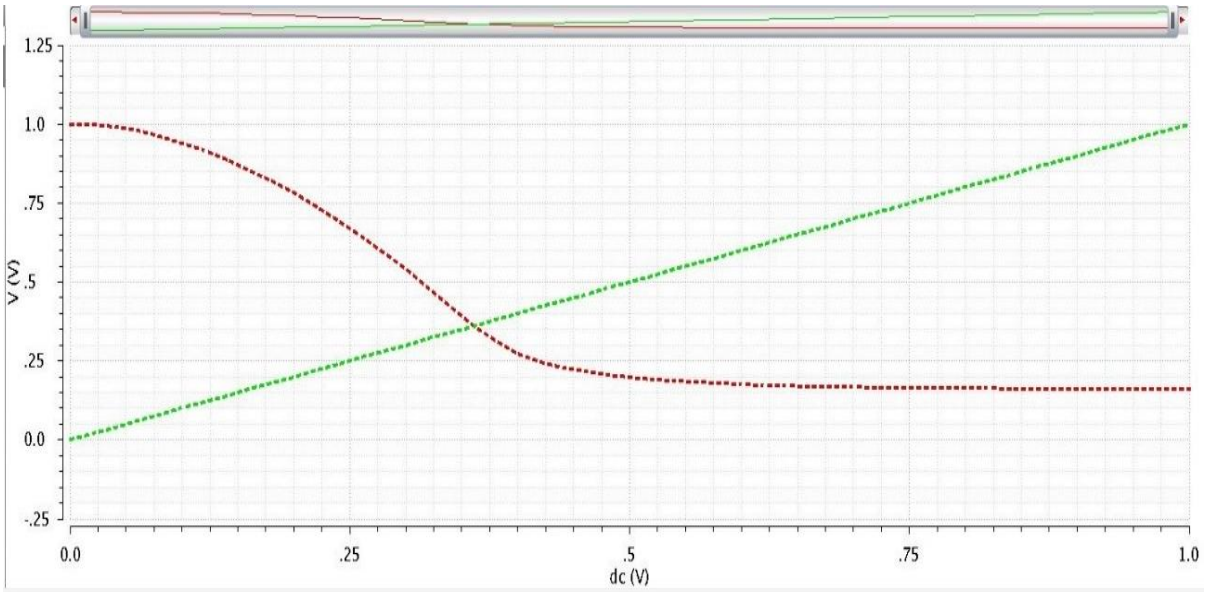

Fig 5.13 Simulation result for HNTFET Inverter characteristics

- **Transient response:**

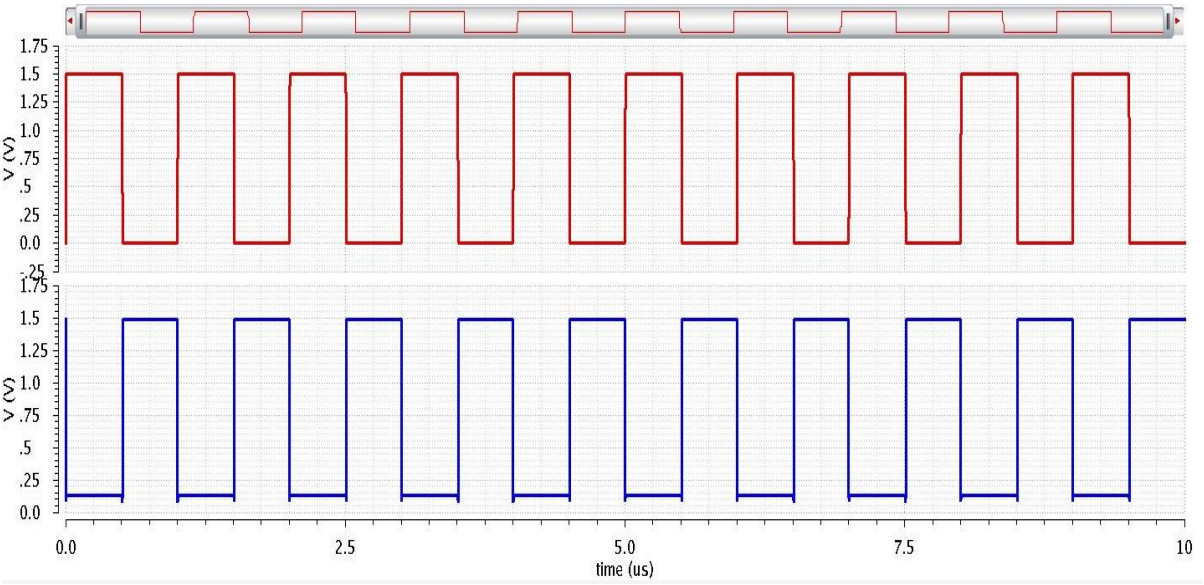

Fig 5.14 Simulation result for HNTFET Inverter (pulse input)

The above two graphs depict the Inverter characteristics in both DC and Transient analysis respectively. For an inverter, if the noise margin obtained is low, it is not good fot the TFET operating, we need to get a high noise margin.

5.4. Comparison results between NTFET, HNTFET and NMOS:

From the below comparisions between NMOS, NTFET & HNTFET, the drain characteristics are observed. The NMOS cannot be operated effectively under Vgs <=1v for Transfer characteristics, Vds<=1v for Drain characteristics. Where the TFET reaches the high current with low Vgs. In the TFET devices Heterojunction NTFET gives more performance and accuracy compared to Homojunction NTFET. The comparisions and results are shown below.

5.4.1. Linear Transfer characteristics:

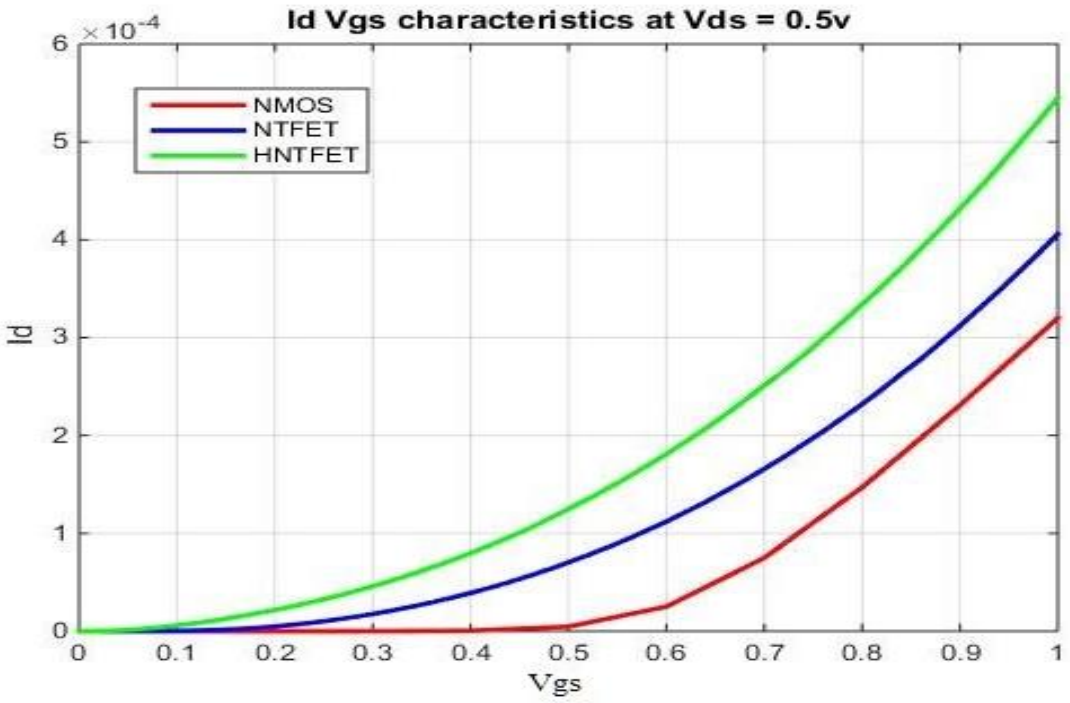

Fig 5.15 Comparision of Id Vgs characteristics

5.4.2. Linear drain characteristics:

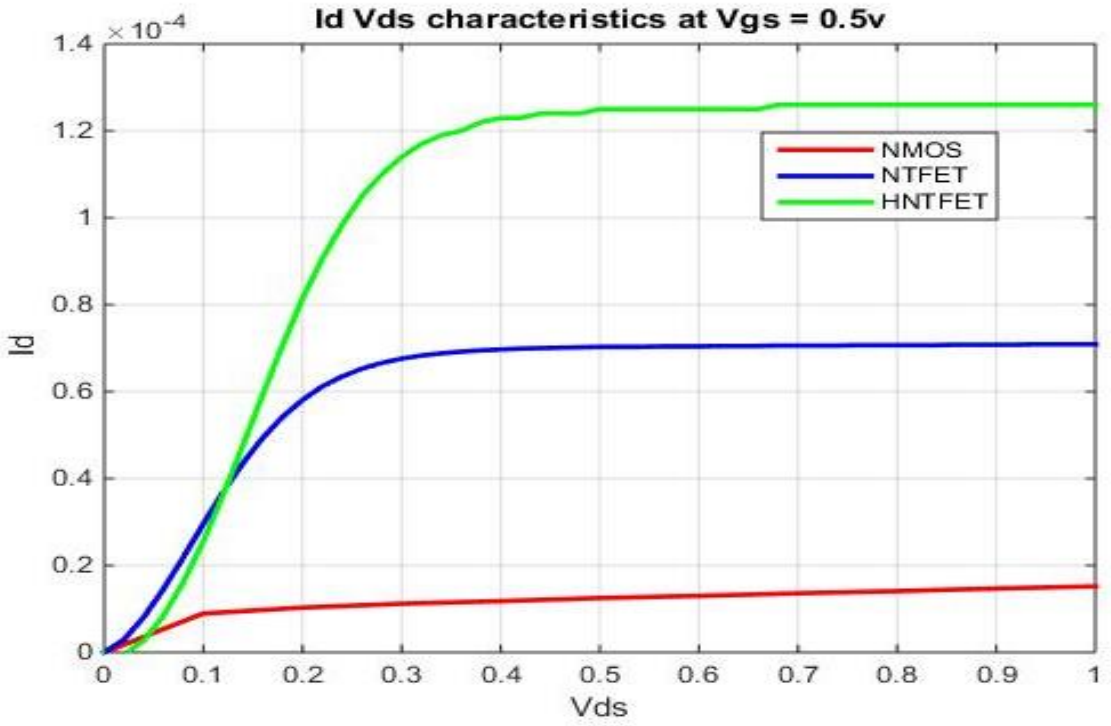

Fig 5.16 Comparision of Id Vds characteristics

5.4.3. Inverter characteristics:

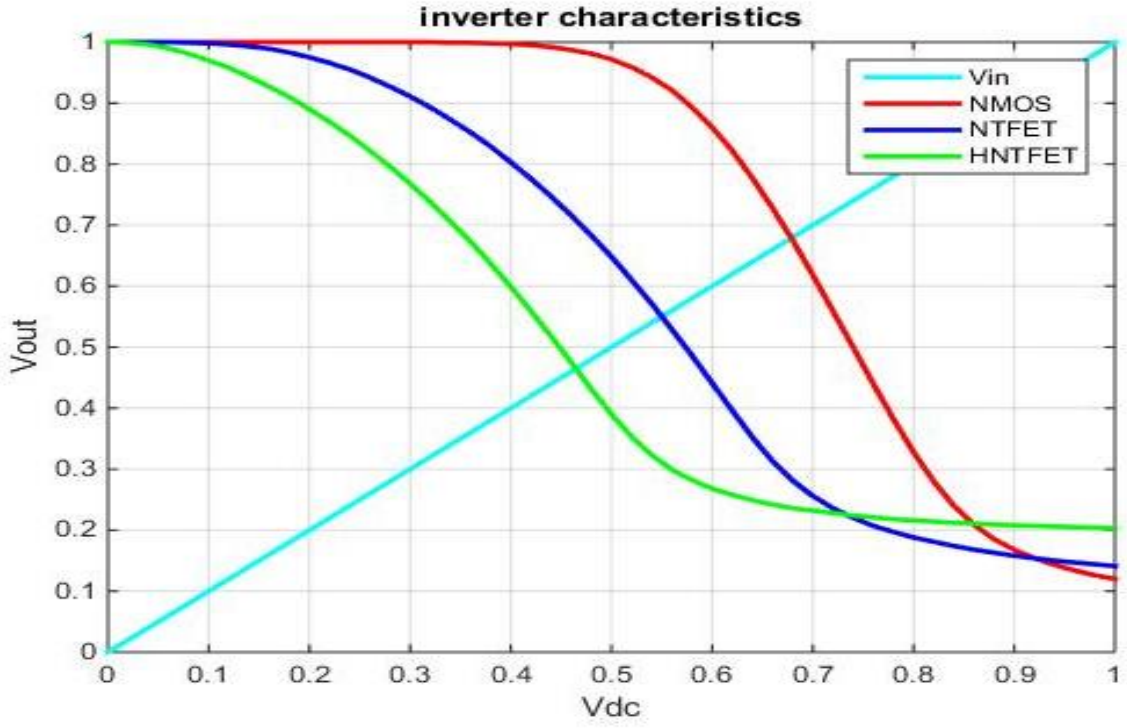

Fig 5.17 Comparision of inverter characterisitcs

5.5. Observations :

From the above results, we can have some of the following observations

- We can observe the ambipolar nature using the graph "Log Id-Vgs" of both homojunction and heterojunction TFETs.
- For Homojunction (InAs) TFET, if we observe ambipolarity is maintained when high Vds is applied i.e; graph is symmetric, but when low Vds is applied, it losts its ambipolarity, since the graph becomes asymmetric.
- For Heterojunction (AlGaSb/InAs) TFET, if we observe ambipolarity is maintained at both high and low Vds. So, when high Vds is applied i.e; graph is symmetric, and when low Vds is applied, it doesn't lose its ambipolarity.
- In the case of ambipolarity, Heterojunction TFET is preferred over Homojunction TFET, because Higher On Current is maintained in heterojunction TFETs.
- Also from the graph, we can observe that Ion (On current) is 120uA and 80uA for InAs and AlGaSb/InAs TFETs respectively.
- Higher on and off currents can be observed in hetero TFETs compared to homo TFETs.
- Also NDR (Negative differential region) can be observed from the graph of Id-Vds of both homo and hetero TFETs in 3rd quadrant.

CONCLUSION

TFET can replace in the future the CMOS for low power applications and it presents low I_{OFF} and low I_{ON} and SS (Sub threshold Slope) below 60mV/dec. TFET can be used in many applications for operation of dc voltage less than or equal to 1v thereby offering significant power dissipation savings, which is not possible in the case of Bulk MOSFET. Because of their low off currents, they are ideally suited for low power and low standby power logic applications operating at moderate frequencies. In comparison to a MOSFET, high I_{on}/I_{off} ratio and steep SS (Sub threshold Slope) over several decades indicate TFET's superiority for ultra-low-voltage applications. Among a few candidates for the steep subthreshold FETs, tunneling FET is a most promising one due to its simple structure and its capability of the drain voltage reduction. Other promising applications of TFETs include ultralow power specialized analog integrated circuits with improved temperature stability and low power SRAM. To justify the versatility of the model, the model is applied to two TFETs with distinctly different geometries, a planar double-gate InAs TFET and a broken-gap AlGaSb/InAs inline TFET, and good agreement is demonstrated between the model and both simulations.

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APPENDIX

Parameters and Constants

The following Constant parameters are included in the Verilog-A model.

- Physical Constants:
  - Elementary Charge q = 1.602 X 10^{-19} C
  - Electron rest mass m_0 = 9.109 X 10^{-31} Kg
  - Planck's constant h = 6.626 X 10^{-34} J-s
  - Boltzmann's constant k_B = 1.381 X 10^{-23} J/K
  - Permittivity of vacuum ε_0 = 8.854 X 10^{-12} F/m
- Drain Current Parameters
  - Transition width parameter = 5
  - Built-in electric field ξ_0 = 5.27E7 V/m
  - Semiconductor band gap E_G = 0.35 eV
  - NDR drain-source voltage sensitivity parameter η = 0.1
  - Saturation shape parameter Γ = 0.06 V
  - p-n junction saturation current density J_0 = 1E7 A/m^2
  - NDR current density parameter J_P = 2E8 A/m^2
  - NDR current scale factor = 2/v
  - Saturation voltage parameter λ = 0.19 V
  - Reduced effective mass m_R^* = 0.012
  - Sub-threshold ideality factor n = 1.8
  - Tunnel junction ideality factor n = 1.1
  - Tunneling window parameter γ_0 = 0.5
  - Electric field parameter γ_1 = 0.011/m
  - Electric field parameter γ_2 = 1.3 1/m
  - Drain access resistance per unit width = 0 Ωμm
  - Gate access resistance per gate square = 0 Ω
  - Drain access resistance perunit width = 0 Ωμm
  - Ambipolar current attenuation S= 1.0
  - Channel thickness t_{CH} = 5E-9 m
  - Tunnel junction peak voltage V_P = 0.05 V

- Threshold voltage $\boldsymbol{V_{TH}}$ = 0.17 V

❖ Capacitance Parameters:

- Gate-drain capacitance parameter $\boldsymbol{\alpha}$ = 1.14
- Gate-drain capacitance parameter $\boldsymbol{\beta}$ = 0.02 /V^{MC}
- Gate-source capacitance per unit width = 6.9E-11 F/m
- Equivalent oxide thickness $\boldsymbol{\varepsilon_{OT}}$ = 0.2E-9 m
- Gate insulator dielectric constant $\boldsymbol{\varepsilon_{SI}}$ = 1.0
- Capacitance parameter $\boldsymbol{\Gamma'}$ = 0.18 V
- Cgd knee-shape parameter $\boldsymbol{m}$ = 2

Table 3 Range of parameters in the model

Parameters	Range	InAs(DG)	AlGaSb/InAs SG
E_G (eV)	-	0.354	0.354
m_R^*	-	0.0218	0.0218
t_{CH} (nm)	-	5	10
Γ (V)	0 - 1	0.056	0.044
γ_0	0 - 1	0.64	0.17
γ_1 (m-1)	0 - 1	0.01	0.01
γ_2 (m-1)	0 - 2	1.89	0.83
ξ_0 (MV/cm)	0.5 - 5	0.507	0.839
λ (V)	0 - 1	0.19	0.33
n	>1	1.49	1.39
V_{OFF} (V)	0 - V_{DD}	0	0
V_{TH} (V)	0 - V_{DD}	0.145	0.076

Verilog-A Code for TFET

```
// VerilogA for tfet, ndtfet, veriloga

`include "discipline.h"
`define n_type          1
`define p_type          -1
`define CHARGE      1.6021918e-19
`define M0      9.1095e-31
`define H               6.62606957e-34
`define HBAR            1.05458e-34
`define KB      1.3806488E-23
`define PI      3.141592653
`define EPS0    8.85418782e-12
`define VDSMIN      1e-12
`define DELTA           5
`define VMIN 0.001
`define AMIN 1u

module ndtfet(drain, gate, source);
  inout drain, gate, source;
  electrical drain, gate, source;
  electrical drainprime, gateprime, sourceprime;

 // instance parameters
  parameter real w = 1e-6;
  parameter real l = 2e-8;

//drain-source current parameters
  parameter real e0 = 0.527e8;
  parameter real eg = 0.35;
  parameter real eta = 0.1;
  parameter real gamma0 = 0.06;
  parameter real gammac = 0.18;
  parameter real j0 = 1e7;
```

```
  parameter real jp = 2e8;
  parameter real k = 2;
  parameter real lambda = 0.19;
  parameter real mr = 0.012;
  parameter real n1 = 1.8;
  parameter real n2 = 1.1;
  parameter real r0 = 0.5;
  parameter real r1 = 0.01;
  parameter real r2 = 1.3;
  parameter real rdw = 0;
  parameter real rgwl = 0;
  parameter real rsw = 0;
  parameter real s = 1;
  parameter real tch = 5e-9;
  parameter real voff = 0.01;
  parameter real vp = 0.05;
  parameter real vth = 0.17;

 //fixed capacitances parameters
  parameter real alpha = 1.14;
  parameter real beta = 0.02;
  parameter real cgs0 = 6.9e-11;
  parameter real cgdew = 0;
  parameter real cgsew = 0;
  parameter real eot = 0.2n;
  parameter real gamma1 = 0;
  parameter real k0 = 0;
  parameter real k1 = 1;
  parameter real mc = 2;
  parameter real epsi = 3.9;
  parameter integer type = `n_type;

  real vds, vsd, vdse, vsde, vgs, vgd, mrvalue, egvalue, u0, a, b, ag, bg, eps, ru, gamma, vthds,
vthdsa, gi, r0p, deltas;
```

```
real vgt, vgo, vgoe, vgoen, f, u, e, id;
real vgta, vgoa, vgoea, vgoena, fa, ua, ea, ida, idr;
real rd, rg, rs, gd, gg, gs;
real cgde, cgse;
real ci, cgs, cgd, cgdmax, cgdmin, ac, ace, vgse;

analog
  begin
    @(initial_step or initial_step("static"))
      begin
        u0 = n1*$vt;
        mrvalue = mr*`M0;
        egvalue = eg*`CHARGE;
        ru = r0*u0;
        r0p = 1-r0;
        deltas = `DELTA*`DELTA;
        a =
w*tch*`CHARGE*`CHARGE*`CHARGE/(8*`PI*`PI*`HBAR*`HBAR)*sqrt(2*mrvalue/eg
value);
        b = 4*egvalue*sqrt(2*mrvalue*egvalue)/(3*`CHARGE*`HBAR);
        eps = epsi*`EPS0;
        cgde = cgdew*w*1e6;
        cgse = cgsew*w*1e6;
        ci = `EPS0*epsi*w*l/eot;
        cgdmax = 0.9*ci;
        cgdmin = 0.13*ci;
        rd = rdw/(w*1e6);
        rg = rgwl*w/l;
        rs = rsw/(w*1e6);
        if(rd > 0)
          gd = 1/rd;
        else
          gd = 0;
        if(rg > 0)
```

```
        gg = 1/rg;
      else
        gg = 0;
      if(rs > 0)
        gs = 1/rs;
      else
        gs = 0;
    end
  vds = type*V(drainprime,sourceprime);
  vgd = type*V(gateprime,drainprime);
  vgs = type*V(gateprime,sourceprime);
  vgt  = vgs-vth;
  vdse = `VDSMIN*(0.5*vds/`VDSMIN+sqrt(deltas+(0.5*vds/`VDSMIN-
1)*(0.5*vds/`VDSMIN-1))-sqrt(deltas+1));

// main drain-source tunneling current
  vgo  = vgs-voff;
  vgoe = `VMIN*(1+0.5*vgo/`VMIN+sqrt(deltas+(0.5*vgo/`VMIN-1)*(0.5*vgo/`VMIN-
1)));
  vgoen = vgoe/(vth-voff);
  gamma = gamma0 + gamma1*vgoe;
  gi = 1/gamma;
  vthds = lambda*tanh(k0+k1*vgo);
  f = (1-limexp(-vds*gi))/(1+limexp((vthds-vds)*gi));
  u = ru+r0p*u0*vgoen;
  e = e0*(1+r1*vds+r2*vgoe);
  id = a*f*u*ln(1+limexp((vgt)/u))*e*limexp(-b/e);

 // ambipolar drain-source current
  vgta = -vgs+2*voff-vth;
  vgoa  = -vgo;
  vthdsa = lambda*tanh(k0+k1*vgoa);
  vgoea = `VMIN*(1+0.5*vgoa/`VMIN+sqrt(deltas+(0.5*vgoa/`VMIN-
1)*(0.5*vgoa/`VMIN-1)));
```

```
    vgoena = vgoea/(vth-voff);
    fa = (1-limexp(-vdse*gi))/(1+limexp((vthdsa-vdse)*gi));
    ua = ru+r0p*u0*vgoena;
    ea = e0*(1+r1*vdse+r2*vgoea);
    ida = s*a*fa*ua*ln(1+limexp((vgta)/ua))*ea*limexp(-b/ea);

// NDR drain-source current
    vsd = -vds;
    vsde = vdse;
    idr = -w*tch*(jp*(vsde/vp)*k*vgoe*limexp(1+(-vsde+eta*vgs)/vp) +
j0*(limexp(vsd/n2/$vt)-1));
    id = id + ida + idr;

 //capacitance calculations
    vgse = `VMIN*(1+0.5*vgs/`VMIN+sqrt(deltas+(0.5*vgs/`VMIN-1)*(0.5*vgs/`VMIN-
1)));
    ac = ((1+beta*pow(vgse,mc))-limexp(-vgoe/gammac))/(1+limexp((vth+alpha*vdse-
vgoe)/gammac));
    ace = `AMIN*(1+0.5*ac/`AMIN+sqrt(deltas+(0.5*ac/`AMIN-1)*(0.5*ac/`AMIN-1)));
    cgs = cgs0*w;
    cgd = cgdmin + (cgdmax - cgdmin)*ace;

 // Augment the matrix
    I(gateprime,sourceprime) <+ type*cgs*ddt(vgs);
    I(gateprime,drainprime) <+ type*cgd*ddt(vgd);
    I(drainprime,sourceprime) <+ type*id;
    I(gate,drain) <+ type*(ddt(cgde*V(gate,drain)));
    I(gate,source) <+ type*ddt(cgse*V(gate,source));
    if(rd > 0)
      begin
        I(drain,drainprime) <+ gd*V(drain,drainprime);
      end
    else
      V(drain,drainprime) <+ 0.0;
```

```
    if(rs > 0)
      begin
        I(source,sourceprime) <+ gs*V(source,sourceprime);
      end
    else
      V(source,sourceprime) <+ 0.0;
    if(rg > 0)
      begin
        I(gate,gateprime) <+ gg*V(gate,gateprime);
      end
    else
      V(gate,gateprime) <+ 0.0;
  end
endmodule
```