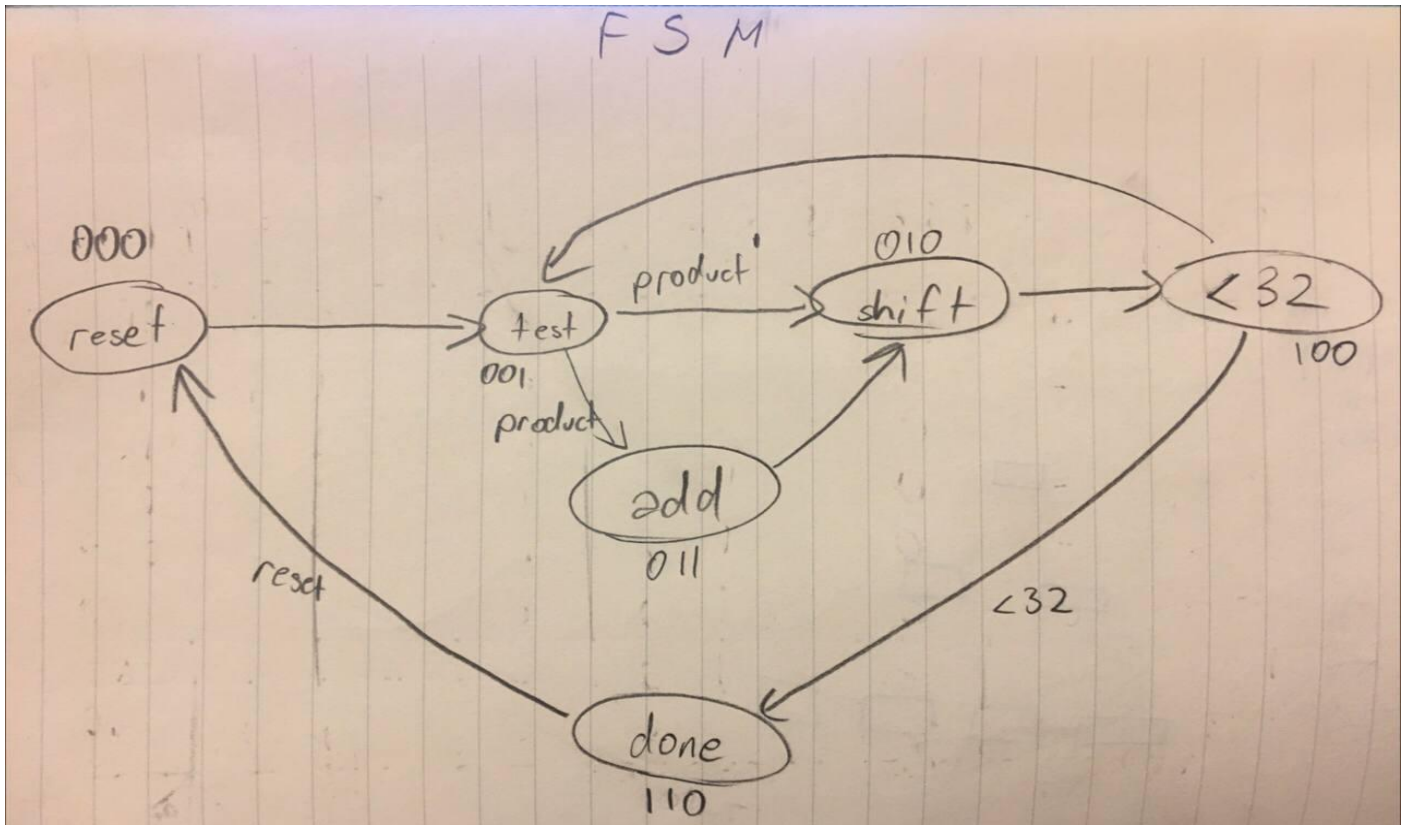


CSE 331/503
Computer Organization
Homework 3 – ALU with Multiplication Design

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product <32 reset	$s_2 s_1 s_0$	000	001	011	010	100	101	111	110
000		1	0	0	0	1	0	0	0
001		1	0	0	0	1	0	0	0
011		1	0	0	0	0	0	0	0
010		1	0	0	0	0	0	0	0
100		1	1	0	0	1	0	0	0
101		1	1	0	0	1	0	0	0
111		1	1	0	0	0	0	0	0
110		1	1	0	0	0	0	0	0

$$N_0 = s_2' s_1' (\text{product}) + s_1' s_0' (<32) + s_2' s_1' s_0'$$

$\begin{matrix} S_2 S_1 S_0 \\ \text{product} \\ < 32 \\ \text{reset} \end{matrix}$	000	001	011	010	100	101	111	110
000	0	1	1	0	0	0	0	1
001	0	1	1	0	0	0	0	0
011	0	1	1	0	1	0	0	0
010	0	1	1	0	1	0	0	1
100	0	1	1	0	0	0	0	1
101	0	1	1	0	0	0	0	0
111	0	1	1	0	1	0	0	0
110	0	1	1	0	1	0	0	1

$$N_1 = S_2' S_0 + S_2 S_1' S_0' (< 32) + S_2 S_1 S_0' (\text{reset})'$$

	000	001	011	010	100	101	111	110
000	0	0	0	1	0	0	0	1
001	0	0	0	1	0	0	0	0
011	0	0	0	1	1	0	0	0
010	0	0	0	1	1	0	0	1
100	0	0	0	1	0	0	0	1
101	0	0	0	1	0	0	0	0
111	0	0	0	1	1	0	0	0
110	0	0	0	1	1	0	0	1

$$N_2 = S_2 S_1' S_0' (< 32) + S_1 S_0' (\text{reset})' + S_2' S_1 S_0'$$

Truth table										
S_2	S_1	S_0	product	<32	reset	N_2	N_1	N_0	shift Right	write
0	0	0	x	x	x	0	0	1	0	0
0	0	1	0	x	x	0	1	0	0	0
0	0	1	1	x	x	0	1	1	0	0
0	1	0	x	x	x	1	0	0	1	0
0	1	1	x	x	x	0	1	0	1	1
1	0	0	x	0	x	0	0	1	0	0
1	0	0	x	1	x	1	1	0	0	0
1	1	0	x	x	0	1	1	0	0	0
1	1	0	x	x	1	0	0	0	0	0

$$N_0 = S_2' S_1' S_0' + S_2' S_1' S_0 (\text{product}) + S_2 S_1' S_0' (<32)'$$

$$N_1 = S_2' S_1' S_0 (\text{product})' + S_2' S_1' S_0 (\text{product}) + S_2' S_1 S_0' (<32) + S_2 S_1 S_0' (\text{reset})'$$

$$N_2 = S_2' S_1 S_0' + S_2 S_1' S_0' (<32) + S_2 S_1 S_0' (\text{reset})'$$

$$\text{shift right} = S_2' S_1 S_0' + S_2' S_1 S_0 = S_2' S_1$$

$$\text{write} = S_2' S_1 S_0$$

I couldn't understand how to implement par1 in verilog, thus my alu32 does not have mult32.v.

half_adder_testbench

Objects

Name	Value	Kind	Mode
a	St1	Net	In
b	St1	Net	In
sum	St0	Net	Out
carry_out	St1	Net	Out

Transcript

```

add wave -position end sim:/half_adder_testbench/sum
add wave -position end sim:/half_adder_testbench/carry_out
VSIM 37> step -current
# time = 0, a =0, b=0, sum=0, carry_out=0
# time = 20, a =1, b=0, sum=1, carry_out=0
# time = 40, a =0, b=1, sum=1, carry_out=0
# time = 60, a =1, b=1, sum=0, carry_out=1
VSIM 38>

```

full_adder_testbench

Objects

Name	Value	Kind	Mode
a	St0	Net	In
b	St1	Net	In
carry_out	St0	Net	Out
sum	St1	Net	Out

Transcript

```

add wave -position end sim:/full_adder_testbench/sum
VSIM 44> step -current
# time = 0, a =0, b=0, carry_in=0, sum=0, carry_out=0
# time = 20, a =0, b=0, carry_in=1, sum=1, carry_out=0
# time = 40, a =0, b=1, carry_in=0, sum=1, carry_out=0
# time = 60, a =0, b=1, carry_in=1, sum=0, carry_out=1
# time = 80, a =1, b=0, carry_in=0, sum=1, carry_out=0
# time = 100, a =1, b=0, carry_in=1, sum=0, carry_out=1
# time = 120, a =1, b=1, carry_in=0, sum=0, carry_out=1
# time = 140, a =1, b=1, carry_in=1, sum=1, carry_out=1
VSIM 45>

```

adder32_testbench

Objects

Name	Value	Kind	Mode
sum	St1	Net	Out
carry_out	St0	Net	Out
b	St1	Net	In
a	St0	Net	In

Transcript

```

add wave -position end sim:/adder32_testbench/a
VSIM 57> step -current
# time = 0, a =00000000000000001010000010100000, b=00000000000010100000101001000000, carry_in=0, sum=000000000000101010101011100000, carry_out=0
# time = 20, a =0000000000000000101010000010100000, b=00000000000010100000101011000010, carry_in=0, sum=00000000000011001010101011000010, carry_out=0
VSIM 58>

```

myXor_testbench

Name	Value	Kind	Mode
R	11111111111111111111111111111111	Net	Out
B	11111111111111111111111111111111	Net	In
A	00000000000000000000000000000000	Net	In

Transcript

```

add wave -position end sim:/myXor_testbench/a
VSIM 62> step -current
# time = 0, a =0000000011110100010101001000000, b=0000000011110100000101001000000, res=0000000000000000010000000000000
# time = 20, a =00000000000000000000111111111111111, b=1111111111111111111111111111111, res=1111111111111100000000000000000
# time = 40, a =00000000000000000000111111111111111, b=0000000000000000000000000000000, res=0000000000000000111111111111111
# time = 60, a =000000000000000000000000000000000, b=1111111111111111111111111111111, res=1111111111111111111111111111111
VSIM 63>

```

half_subtractor_testbench

Name	Value	Kind	Mode
diff	St0	Net	Internal
borrow	St0	Net	Internal
b	1	Regis...Internal	
a	1	Regis...Internal	

Transcript

```

add wave -position end sim:/half_subtractor_testbench/a
VSIM 68> step -current
# time = 0, a =0, b=0, diff=0, borrow=0
# time = 20, a =1, b=0, diff=1, borrow=0
# time = 40, a =0, b=1, diff=1, borrow=1
# time = 60, a =1, b=1, diff=0, borrow=0
VSIM 69>

```

full_subtractor_testbench

Name	Value	Kind	Mode
diff	St1	Net	Internal
carry_in	1	Regis...Internal	
borrow	St1	Net	Internal
b	1	Regis...Internal	

Transcript

```

# time = 0, a =0, b=0, carry_in=0, diff=0, borrow=0
# time = 20, a =0, b=0, carry_in=1, diff=1, borrow=1
# time = 40, a =0, b=1, carry_in=0, diff=1, borrow=1
# time = 60, a =0, b=1, carry_in=1, diff=0, borrow=1
# time = 80, a =1, b=0, carry_in=0, diff=1, borrow=0
# time = 100, a =1, b=0, carry_in=1, diff=0, borrow=0
# time = 120, a =1, b=1, carry_in=0, diff=0, borrow=0
# time = 140, a =1, b=1, carry_in=1, diff=1, borrow=1

```

subtractor32_testbench

Name	Value	Kind	Mode
diff	0000000000000000101001010111011101	Net	Internal
carry_in	1	Regis...Internal	
borrow	St0	Net	Internal
b	000000000000000000000000101011000010	Pack... Internal	
a	000000000000000000101010000010100000	Pack... Internal	

Transcript

```

add wave -position end sim:/subtractor32_testbench/b
add wave -position end sim:/subtractor32_testbench/a
VSIM 82> step -current
# time = 0, a =000000000000000000001010000010100000, b=0000000000000010100000101001000000, carry_in=1, diff=111111111110101001011001011111, borrow=1
# time = 20, a =0000000000000000101010000010100000, b=000000000000000000000000101011000010, carry_in=1, diff=00000000000000101001010111011101, borrow=0
VSIM 83>

```

[illegible]

Name	Value	Kind	Mode
res	00000000000000000000000000000000	Net	Internal
b	11111111111111111111111111111111	Pack...	Internal
a	00000000000000000000000000000000	Pack...	Internal

```

Transcript
add wave -position end sim:/myNor_testbench/b
add wave -position end sim:/myNor_testbench/a
VSIM 42> step -current
# time = 0, a = 00000000111110100010101001000000, b=0000000011110100000101001000000, res=111111110000010111010101011111
# time = 20, a = 000000000000000000011111111111111, b=1111111111111111111111111111111, res=00000000000000000000000000000000
# time = 40, a = 000000000000000000011111111111111, b=0000000000000000000000000000000, res=111111111111110000000000000000
# time = 60, a = 0000000000000000000000000000000, b=1111111111111111111111111111111, res=00000000000000000000000000000000
VSIM 43>
  
```

Name	Value	Kind	Mode
res	00000000000000000000000000000000	Net	Internal
b	11111111111111111111111111111111	Pack...	Internal
a	00000000000000000000000000000000	Pack...	Internal

Name	Value	Kind	Mode
res	11111111111111111111111111111111	Net	Internal
b	11111111111111111111111111111111	Pack...	Internal
a	00000000000000000000000000000000	Pack...	Internal

[illegible]

Objects

Name	Value	Kind	Mode
s	111	Pack...	Internal
res	00000000000000001111111111111111	Net	Internal
b	00000000000000001111111111111111	Pack...	Internal
a	0000000000000000111100001111	Pack...	Internal

Transcript

```
VSI54 > step -current
# time = 0, a =00000000111110100010101001000000, b=00000000000010100000101000000010, s=000, res=00000001000001000011010001000010
# time = 20, a =00000000000000000000000000000000, b=00000000000000001111111111111111, s=000, res=00000000000000001111111111111111
# time = 40, a =00000011111110100010101001000000, b=00000101111110100000101001000000, s=001, res=00000110000000000010000000000000
# time = 60, a =000000000000000000000000111100001111, b=00000000000000001111111111111111, s=001, res=00000000000000001111000011110000
# time = 80, a =0000001100110100010101001000000, b=00000000111110100000101001000000, s=010, res=00000010101000000001111111111111
# time = 100, a =00000000111110100000101001000000, b=0000001100110100010101001000000, s=010, res=111111010101111110111111111111
# time = 120, a =000000000000010100010101001000000, b=00000000111110100000101001000000, s=011, res=xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
# time = 140, a =00000010111110100010101001000000, b=00000100111110100000101001000000, s=100, res=00000000000000000000000000000001
# time = 160, a =00000010111110100010101001000000, b=00000000111110100000101001000000, s=100, res=00000000000000000000000000000000
# time = 180, a =00000011111110100010101001000000, b=00000101111110100000101001000000, s=101, res=1111110000000001011101010110111111
# time = 200, a =000000000000000000000000111100001111, b=00000000000000001111111111111111, s=101, res=11111111111111110000000000000000
# time = 220, a =00000011111110100010101001000000, b=00000010111110100000101001000000, s=110, res=00000001111110100000101001000000
# time = 240, a =000000000000000000000000111100001111, b=00000000000000000000111111111111, s=110, res=000000000000000000000011100001111
# time = 260, a =00000011111110100010101001000000, b=00000101111110100000101001000000, s=111, res=00000111111101000101010010000000
# time = 280, a =000000000000000000000000111100001111, b=00000000000000001111111111111111, s=111, res=00000000000000001111111111111111
```

aluop=011 does not work because mult32.v does not exist.