CSE 331/503
Computer Organization
Homework 3 – ALU with Multiplication Design

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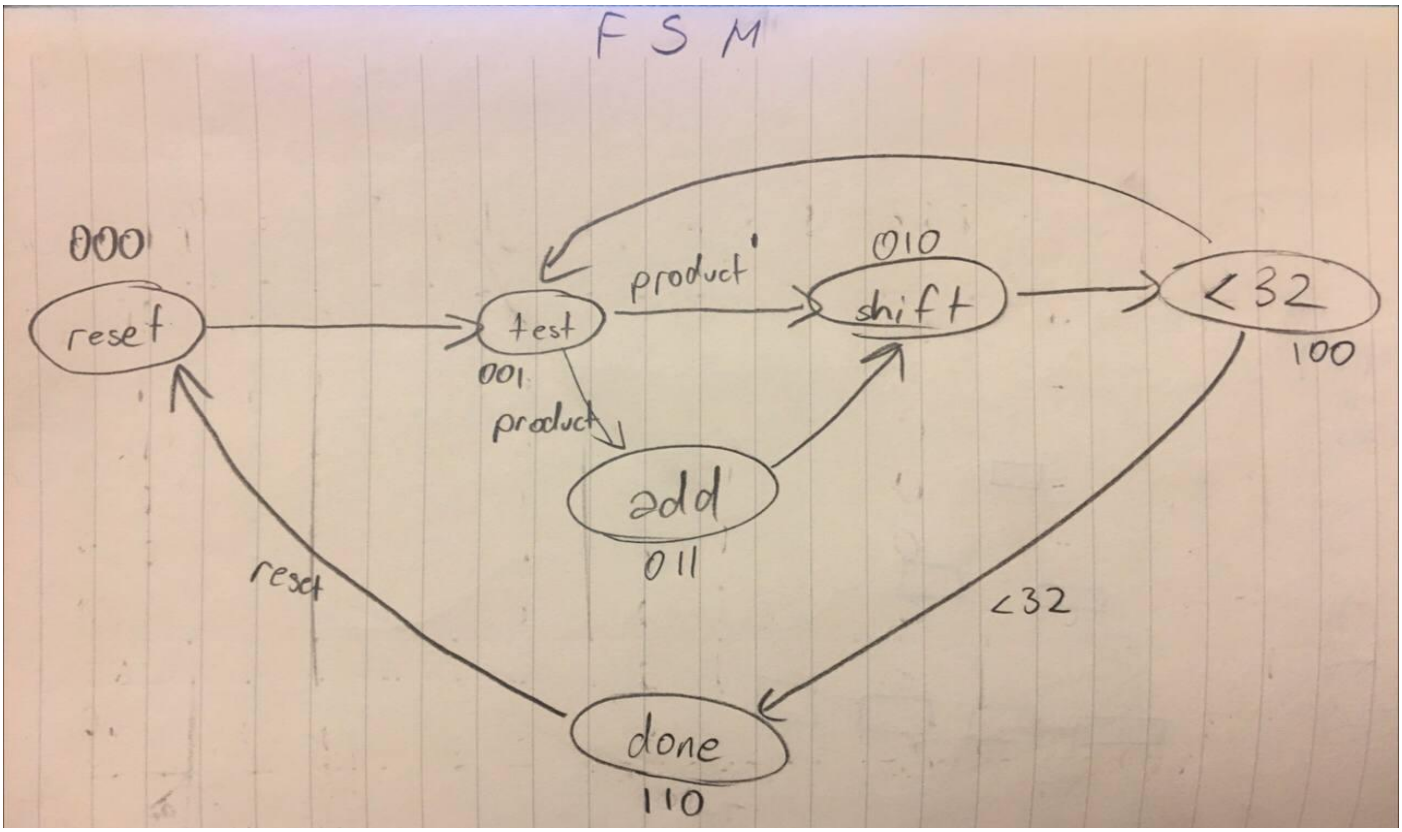


product <32 reset \ $S_2 S_1 S_0$	000	001	011	010	100	101	111	110
000	1	0	0	0	1	0	0	0
001	1	0	0	0	1	0	0	0
011	1	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	1	1	0	0	1	0	0	0
101	1	1	0	0	1	0	0	0
111	1	1	0	0	0	0	0	0
110	1	1	0	0	0	0	0	0

$$N_0 = S_2' S_1' (product) + S_1' S_0' (<32)' + S_2' S_1' S_0'$$

$S_2S_1S_0$ / product<32 reset	000	001	011	010	100	101	111	110
000	0	1	1	0	0	0	0	1
001	0	1	1	0	0	0	0	0
011	0	1	1	0	1	0	0	0
010	0	1	1	0	1	0	0	1
100	0	1	1	0	0	0	0	1
101	0	1	1	0	0	0	0	0
111	0	1	1	0	1	0	0	0
110	0	1	1	0	1	0	0	1

$N_1 = S_2' S_0 + S_2 S_1' S_0' (<32) + S_2 S_1 S_0' (reset)'$

	000	001	011	010	100	101	111	110
000	0	0	0	1	0	0	0	1
001	0	0	0	1	0	0	0	0
011	0	0	0	1	1	0	0	0
010	0	0	0	1	1	0	0	1
100	0	0	0	1	0	0	0	1
101	0	0	0	1	0	0	0	0
111	0	0	0	1	1	0	0	0
110	0	0	0	1	1	0	0	1

$N_2 = S_2 S_1' S_0' (<32) + S_1 S_0' (reset)' + S_2' S_1 S_0'$

Truth table

S_2	S_1	S_0	product	<32	reset	N_2	N_1	N_0	shift Right	write
0	0	0	x	x	x	0	0	1	0	0
0	0	1	0	x	x	0	1	0	0	0
0	0	1	1	x	x	0	1	1	0	0
0	1	0	x	x	x	1	0	0	1	0
0	1	1	x	x	x	0	1	0	1	1
1	0	0	x	0	x	0	0	1	0	0
1	0	0	x	1	x	1	1	0	0	0
1	1	0	x	x	0	1	1	0	0	0
1	1	0	x	x	1	0	0	0	0	0

$N_0 = S_2' S_1' S_0' + S_2' S_1' S_0 (product) + S_2 S_1' S_0' (<32)'$

$N_1 = S_2' S_1' S_0 (product)' + S_2' S_1' S_0 (product) + S_2' S_1 S_0 + S_2 S_1' S_0' (<32) + S_2 S_1 S_0' (reset)'$

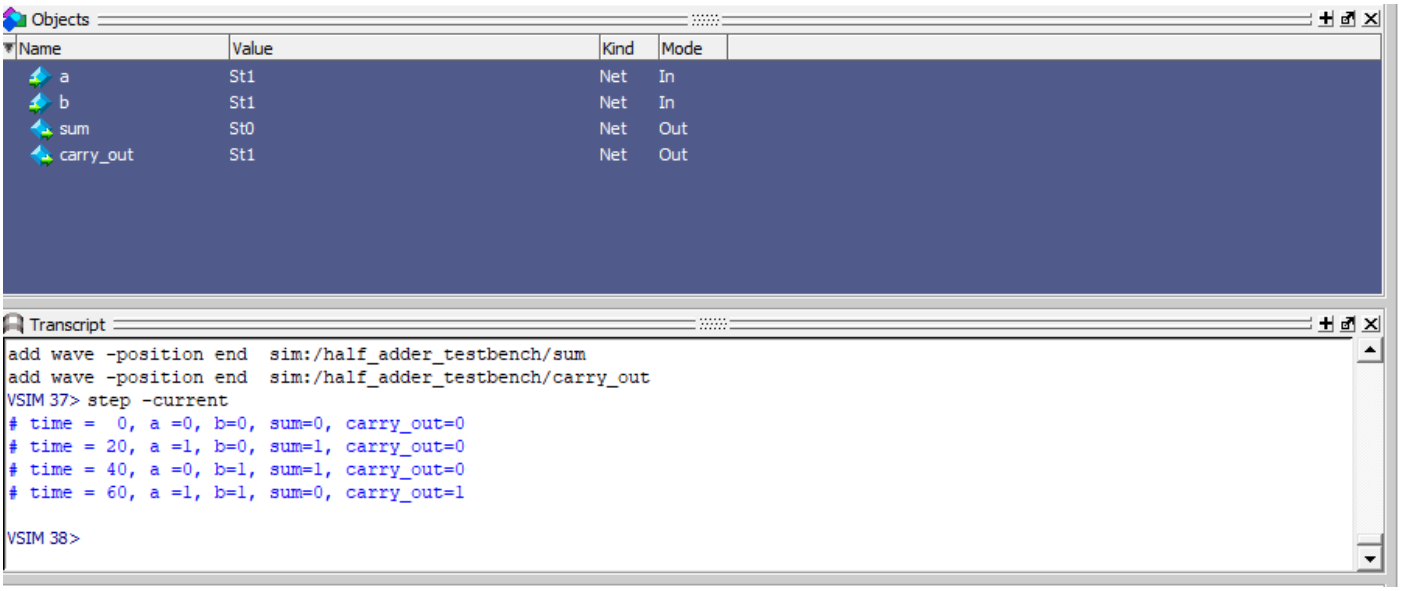
$N_2 = S_2' S_1 S_0' + S_2 S_1' S_0' (<32) + S_2 S_1 S_0' (reset)'$

shift right: $S_2' S_1 S_0' + S_2' S_1 S_0 = S_2' S_1$

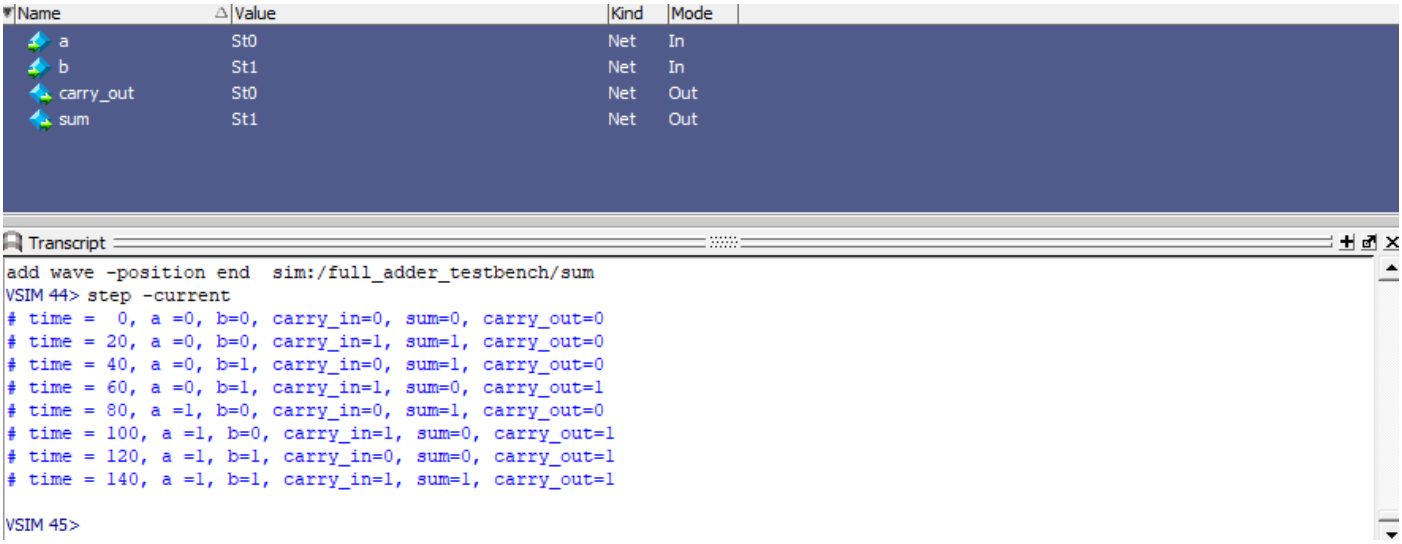
write $= S_2' S_1 S_0$

I couldn't understand how to implement par1 in verilog, thus my alu32 does not have mult32.v.

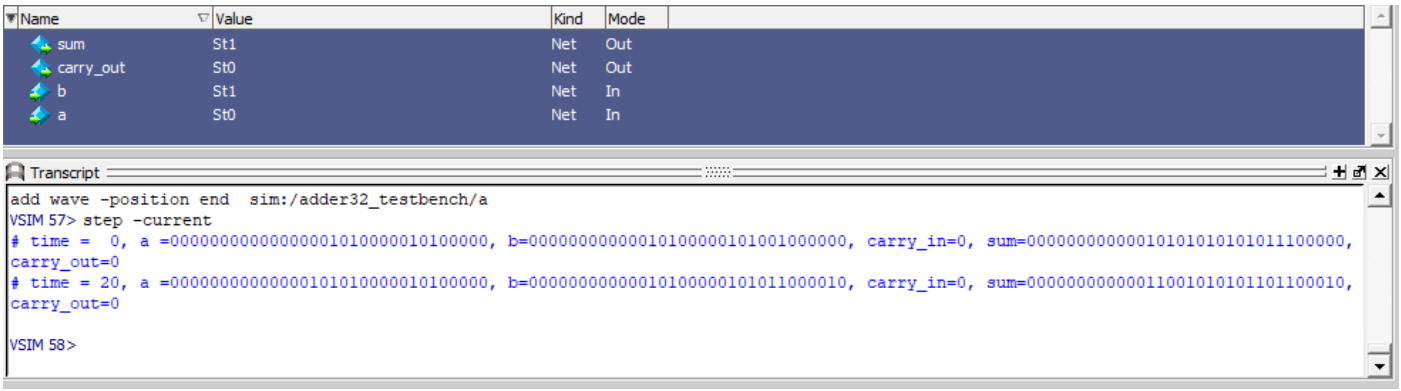
half_adder_testbench



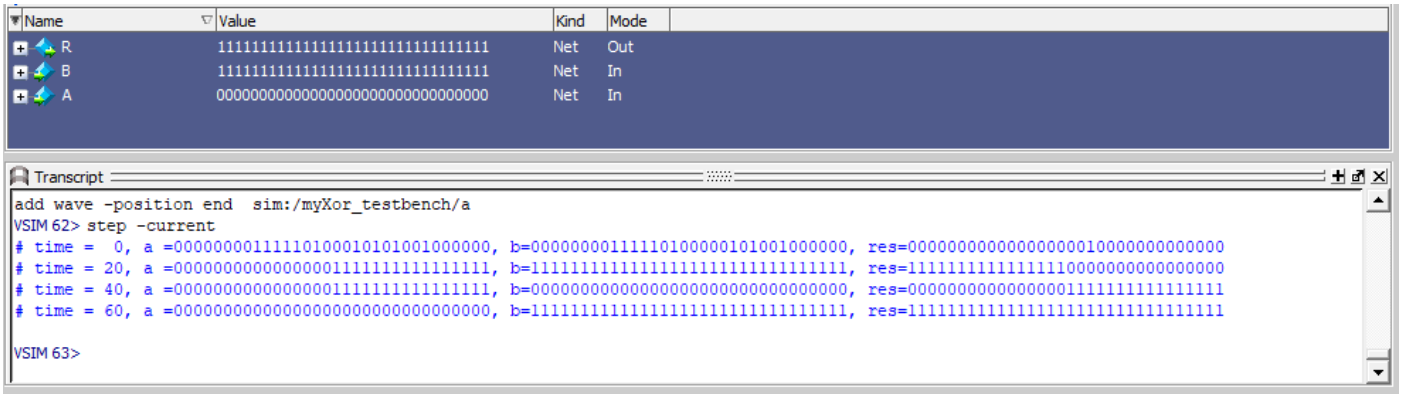
full_adder_testbench



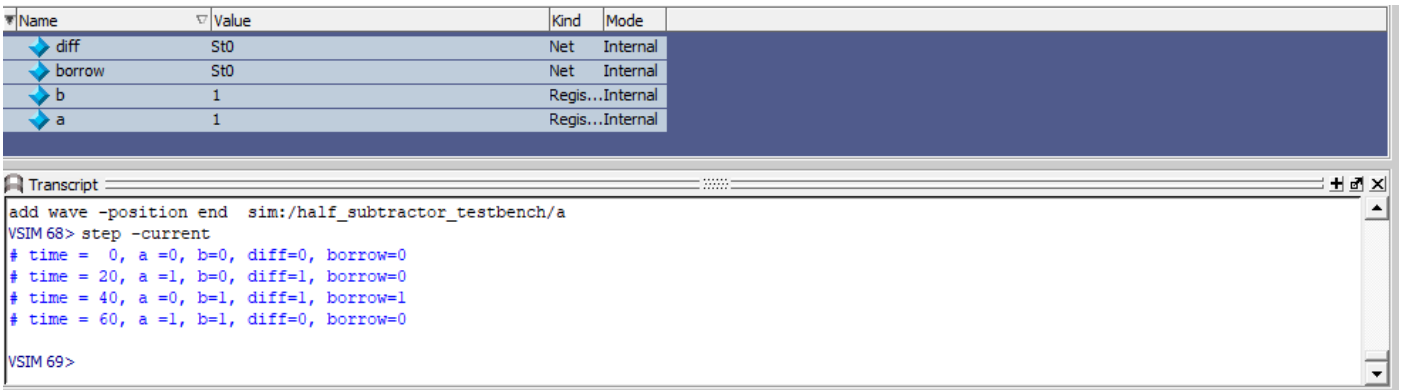
adder32_testbench



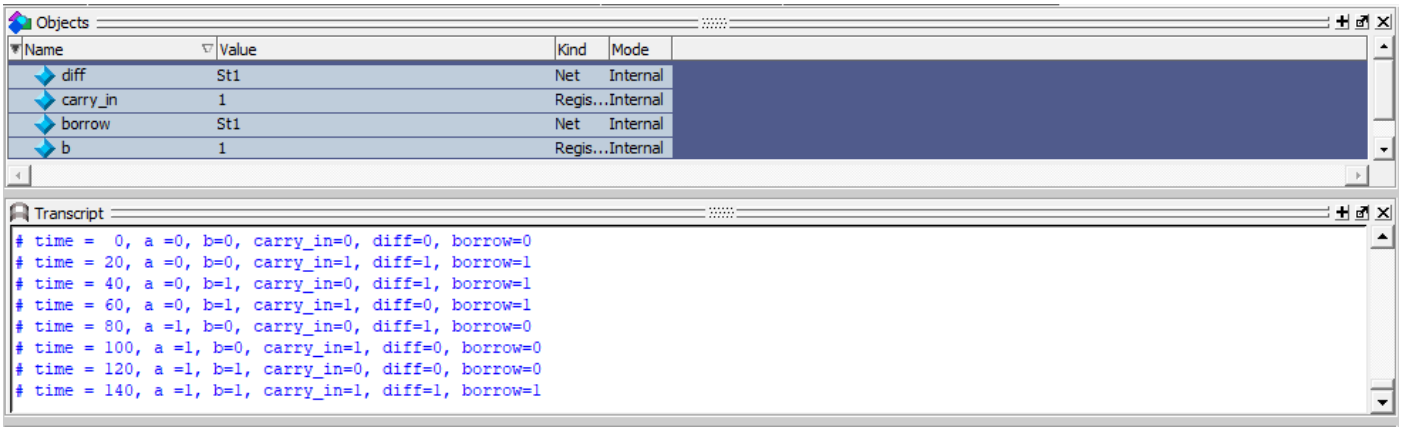
myXor_testbench



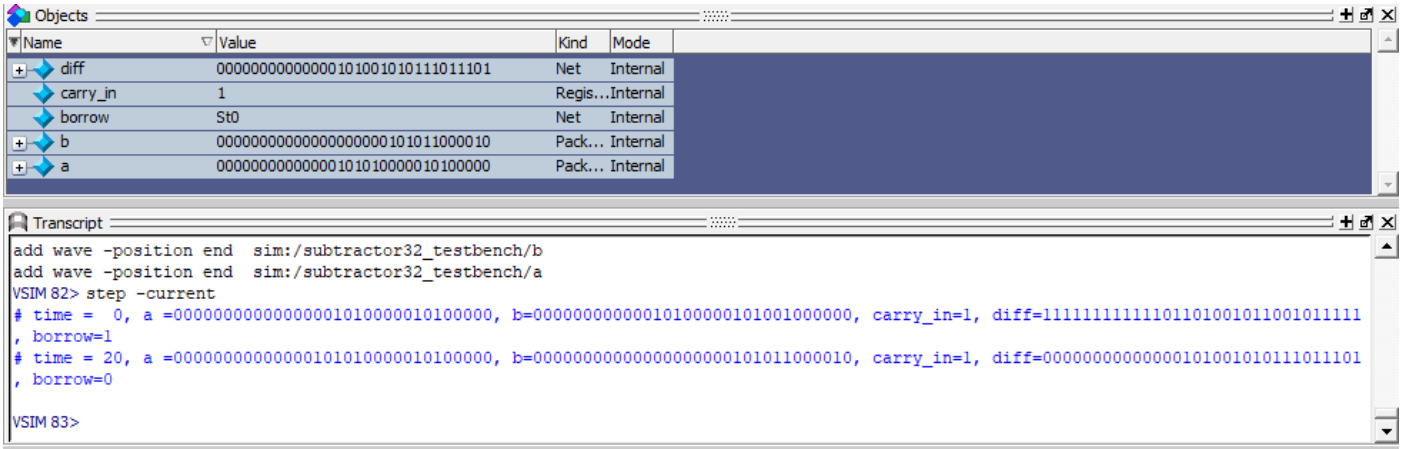
half_subtractor_testbench



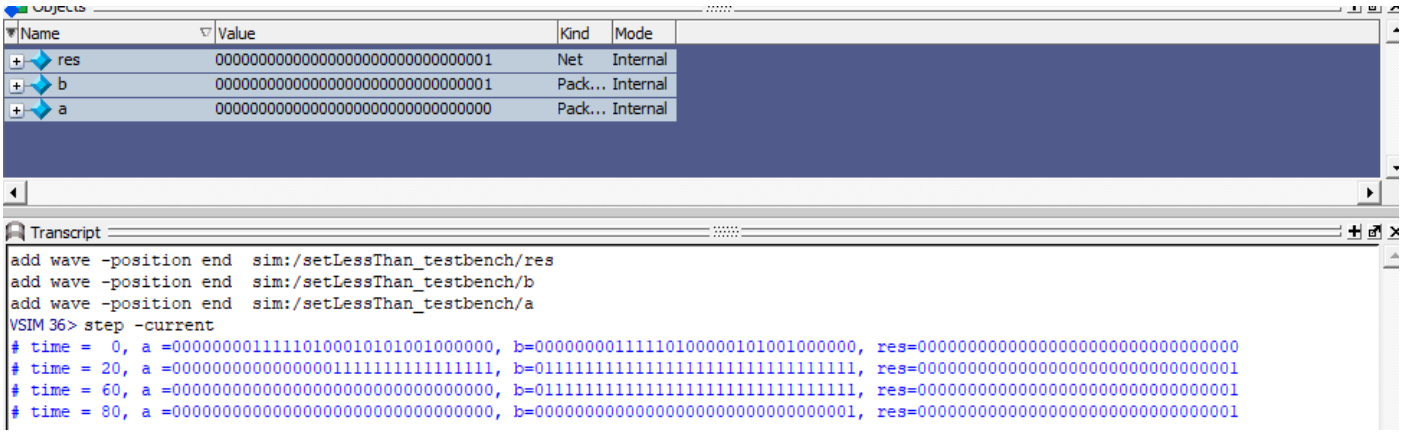
full_subtractor_testbench



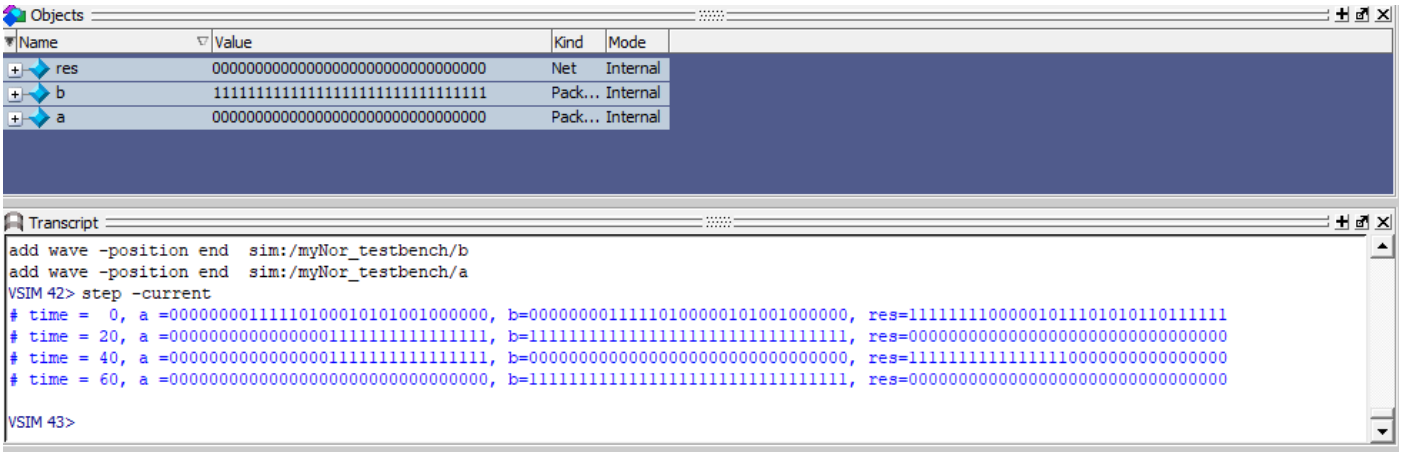
subtractor32_testbench



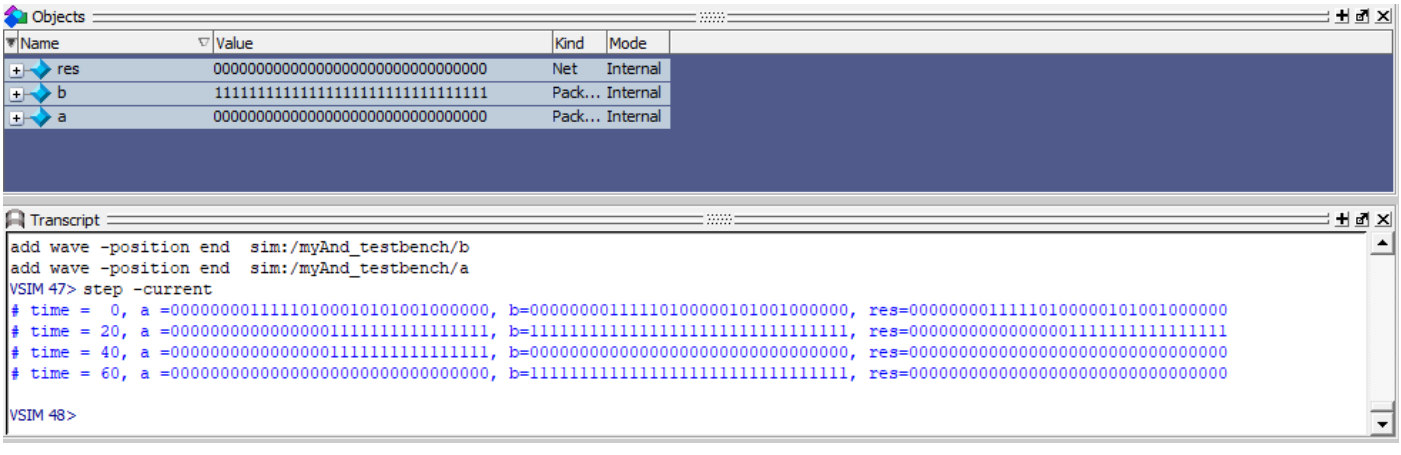
setLessThan_testbench



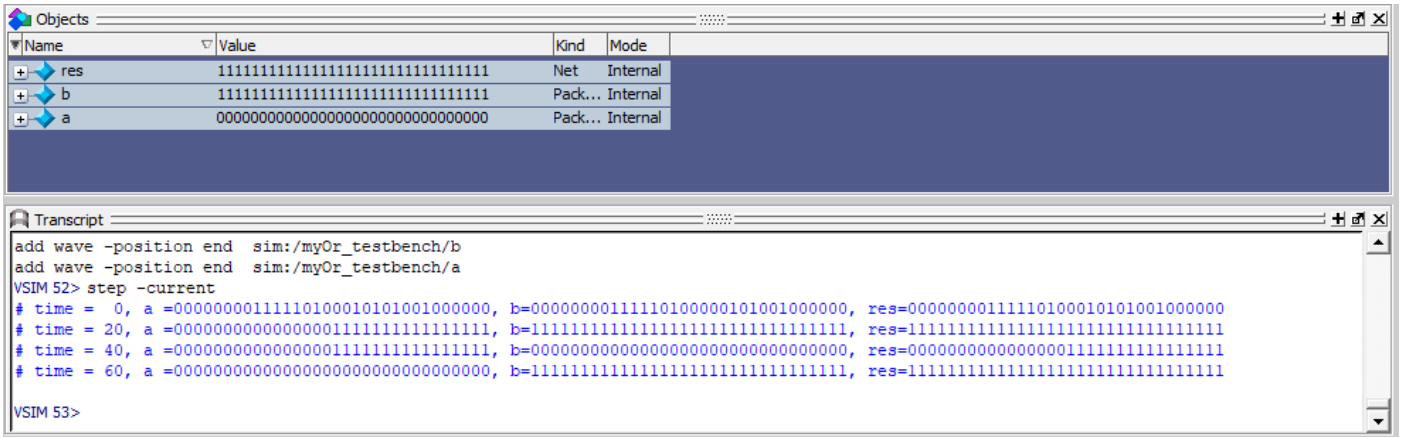
myNor_testbench



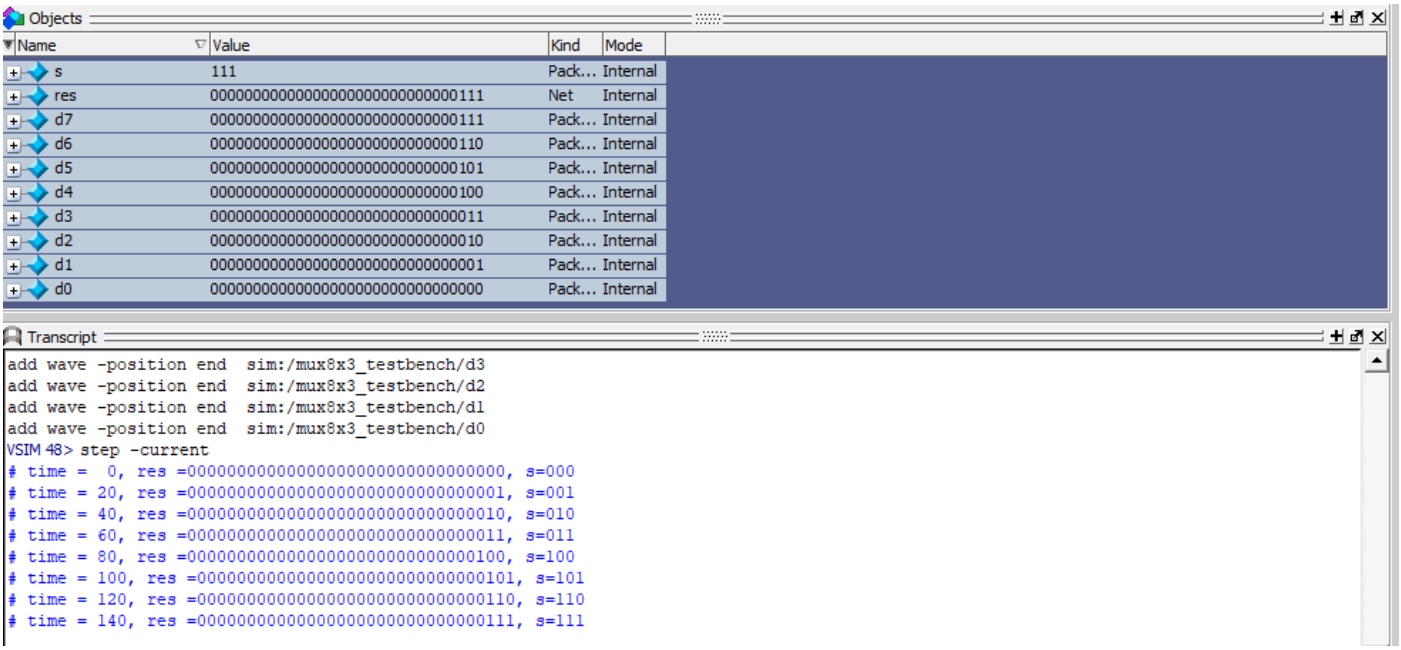
myAnd_testbench



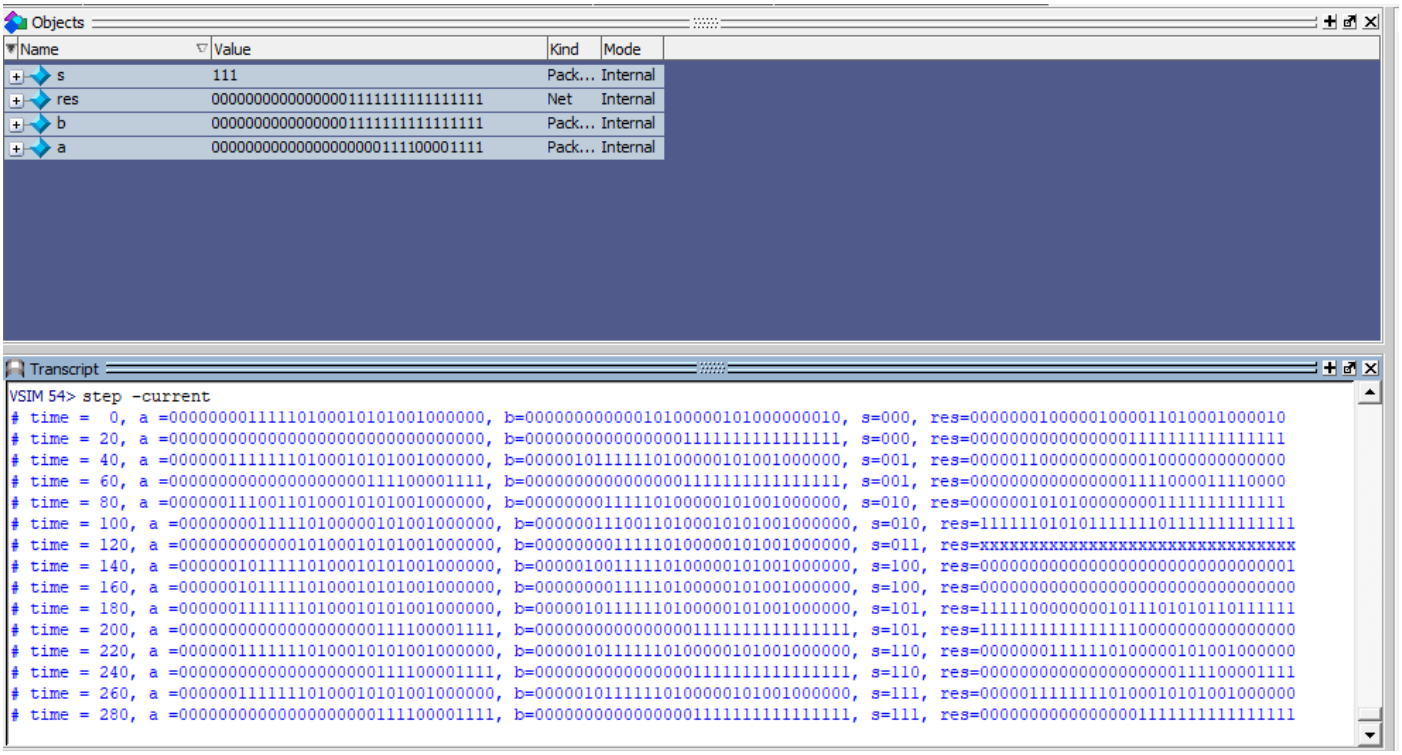
myOr_testbench



mux8x3_testbench



alu32_testbench



aluop=011 does not work because mult32.v does not exist.