T-HEAD

TH1520 Peripheral Interface User Manual

Revision	1.0.0
Security	Secret
Date	2023-08-26

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Revisions

Rev	Description	Author(s)	Date
V1.0.0	Initial version	T-Head	2023-08-26

Contents

Figures & Tables

List of Abbreviations

Abbreviations	Full Spelling	Chinese Explanation
ADC	Analog-to-Digital Converter	模数转换器
DMA	Direct Memory Access	直接存储器访问
DRD	Dual Role Device	双角色设备
FIFO	First Input First Output	先入先出
GMAC	Gigabit Media Access Control	千兆媒体接入控制
GPIO	General Purpose Input Output	通用输入/输出口
I2S	Inter-IC Sound	集成电路内置音频总线
MPJTAG	Multi-Processor JTAG	多 CPU 核 JTAG 调试接口
PIPE	The PHY Interface for the PCI Express, SATA, and USB Architectures	PCIe/SATA/USB 的物理层接口
PWM	Pulse Width Modulation	脉冲宽度调制
RX FIFO	Receiver FIFO	接收 FIFO
sclk	serial clock	串行时钟
sd	serial data	串行数据
TX FIFO	Transmitter FIFO	发送 FIFO
UART	Universal Asynchronous Receiver/Transmitter	通用异步收发器
UTMI	USB2.0 Transceiver Macrocell Interface	USB2.0 物理层接口
ws	word select	字段（声道）选择
xHCI	eXtensible Host Controller Interface	扩展主控制器接口

1 GMAC

1.1 Overview

The Ethernet IP Core is capable of operating at 10/100/1000Mbps for Ethernet and Fast Ethernet applications. An external PHY is needed for the complete Ethernet solution.

The Ethernet IP Core operates in half-duplex or full-duplex mode. In half-duplex mode, the controller supports the IEEE802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. In full-duplex mode, it supports the IEEE802.3 MAC Control Layer, including the Pause operation for flow control.

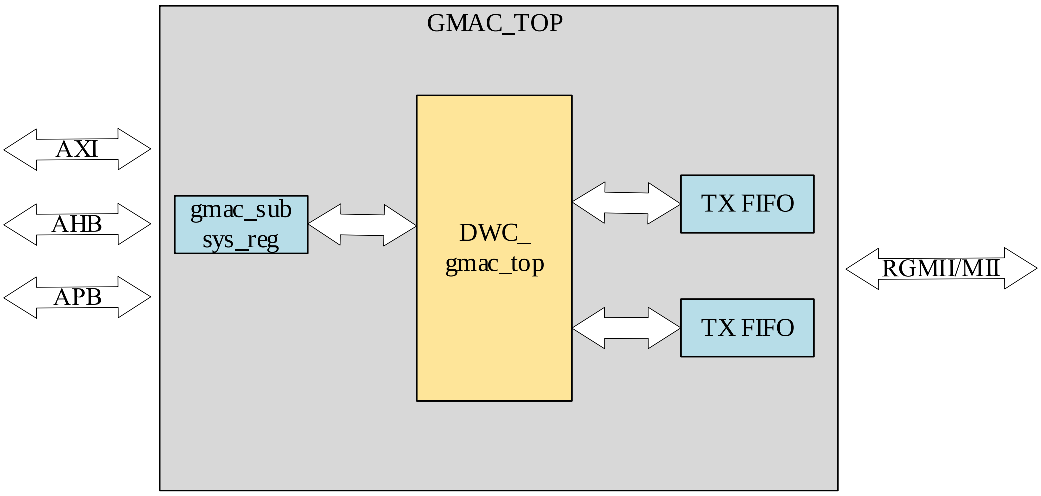

Figure & Table 1-1 GMAC top view

1.2 Main Features

- Compliant with IEEE802.3 Specification
- IEEE 1588-2008 standard for precision networked clock synchronization
- Supports 10/100/1000Mbps data transfer rate
- Supports RGMII/MII interface
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation options for receive frames
- MDIO master interface for PHY device configuration and management

1.3 Interface

GMAC interface as Figure & Table 1-2.

Figure & Table 1-2 GMAC interface

Pin Name	Direction	Width	Description
GMAC0_TXCLK	O	1	TX Clock for output
GMAC0_TXD	O	4	PHY Transmit data
GMAC0_TXEN	O	1	PHY Transmit enable
GMAC0_COL	I	1	This signal, valid only in MII mode, is asserted by the PHY when a collision is detected on the medium. Not used for TH1520 project.
GMAC0_CRS	I	1	This signal, valid only in MII mode, is asserted by the PHY when either the transmit or receive medium is not idle. Not used for TH1520 project.
GMAC0_RXCLK	I	1	RX clock for output
GMAC0_RXD	I	4	PHY Receive Data, use 0~3bit for TH1520 project.
GMAC0_RXDV	I	1	PHY Receive Data Valid
GMAC0_MDC	O	1	Management Data Clock
GMAC0_MDIO	IO	1	Management Data

GMAC interface connect to PHY as Figure & Table 1-3.

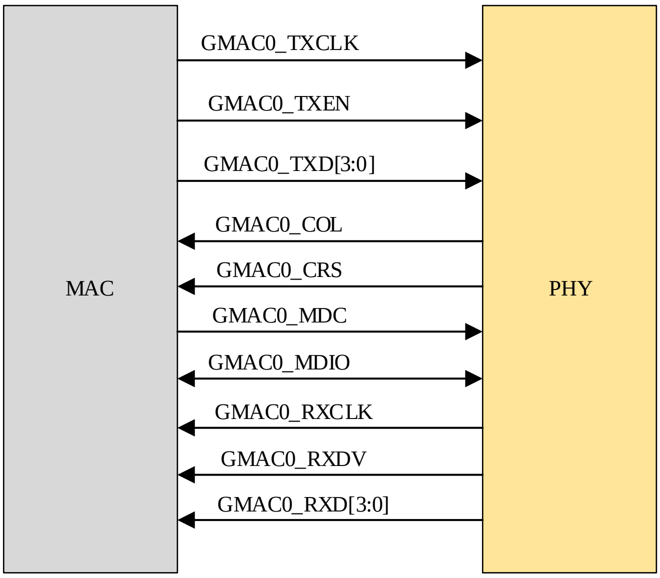

Figure & Table 1-3 GMAC connect to PHY

Figure & Table 1-4 shows timing of the RGMII mode.

Figure & Table 1-4 RGMII timing

Signal	Min	Typical	Max	Unit	Note
TXCK	-	125	125	MHz	Transmit frequency

Signal	Min	Typical	Max	Unit	Note
RXCK	-	125	-	MHz	Receive frequency
Duty	45%	50%	55%	%	TCK duty
tDLY	-0.3	-	1.3	ns	Output delay
tSETUP	1.0	-	-	ns	Setup time for input
tHOLD	0.6	-	-	ns	Hold time for input

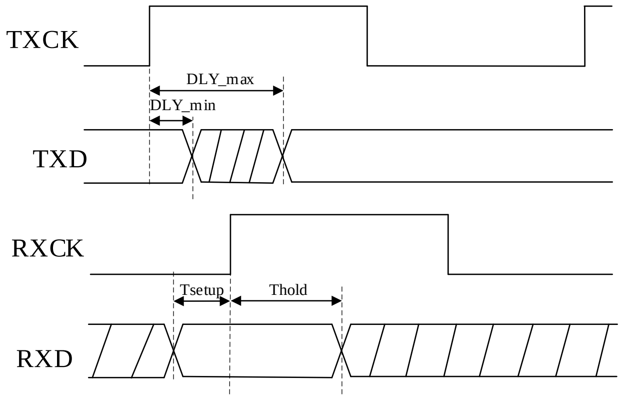

Figure & Table 1-5 RGMII transmit and receive timing

1.4 Function Description

The MAC supports many interfaces towards the PHY chip, such as RGMII and MII. The PHY interface can be selected only once after reset. The MAC communicates with the application side with the MAC Transmit Interface (MTI), MAC Receive Interface (MRI) and MAC Control Interface (MCI).

1.4.1 Transmission

Bus Interface Module (TBU): Interfaces the transmit path of the MAC with the external frame with a FIFO interface.

Frame Controller Module (TFC): Consists of two registers to hold data, byte enable, and the last data control received from the TBU. The register provides a buffer between the Application and the Transmit Protocol Engine to regulate data flow and convert the input data into an 8-bit bus towards the TPE.

Protocol Engine Module (TPE): Consists of a transmission state machine that controls the operation of Ethernet frame transmission.

- Generates preamble and SFD
- Generates transmit frame status
- Contains timestamp snapshot logic for IEEE 1588 support

1.4.2 Reception

Protocol Engine Module (RPE0): The RPE consists of the receive state machine which strips the preamble, SFD and carrier extension of the received Ethernet frame.

CRC Module (CRX): The Receive CRC (CRX) interfaces to the RPE module to check for any CRC error in the receiving frame.

Frame Controller Module (RFC): The Receive Frame Controller (RFC) receives the Ethernet frame data and status from the RPE module. The RFC module consists of a FIFO of parameterized depth and two state machines for writing and reading the FIFO. The FIFO holds the received Ethernet frame data and byte enables, along with a control bit to indicate the last data. The state machines manage the FIFO and provide a frame buffering for the receiving Ethernet frame from the RPE module. The main functions of the RFC module are:

- Data path conversion, which converts the 8-bit data to 32-bit data to the RBU module
- Frame filtering
- Attaching the calculated IP Checksum input from IPC
- Update the Receive Status and forward to RBU

1.5 Usage

1.5.1 Initializing Clock/Reset/PAD

Initializing sys-registers and ioctrl-registers for configuring txclk direction and txclk frequency.

- MII interface, txclk is input from pad; RGMII interface, txclk is output to pad
- 1000Mbps/100Mbps, configure PLL divider register, for txclk 125MHz/25MHz
- Make sure the gmac_prst_n/gmac_hrst_n/gmac_grst_n/gmac_arst_n is in release mode

1. Configure PHY interface type, MII interface or RGMII intreface.
2. Configure clock frequency, 125MHz for 1000Mbps, 25MHz for 100Mbps.
3. Configure clock enable.
4. Configure tx-clock direction:
   If the interface is MII, select tx-clk from PHY; else, select tx-clk from PLL.
   If the interface is MII, configure tx-clk as input direction, else, tx-clk as output direction.

1.5.2 Initializing DMA

1. Provide a software reset. This resets all of the GMAC internal registers and logic.
2. Wait for the completion of the reset process, which is only cleared after the reset operation is completed.
3. Initialize the Bus Mode Register.
4. Program the AXI Interface options.
5. Create a proper descriptor chain for transmit and receive. When OSF mode is used, at least two descriptors are required.

6. Make sure that your software creates three or more different transmit or receive descriptors in the chain before reusing any of the descriptors.
7. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor.
8. Clear the interrupt requests.
9. Enable the interrupts.
10. Confirm that all previous AHB or AXI transactions are complete.
11. Start the Receive and Transmit DMA.

1.5.3 Initializing MAC

The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is done before the DMA is set-up, then enable the MAC receiver (last step below) only after the DMA is active. Otherwise, received frames fills the Rx FIFO and overflow.

1. Control the management cycles for external PHY.
2. Set the appropriate filters for the incoming frames.
3. Program the proper flow control.
4. Program the Interrupt Mask register bits, as required, and if applicable, for your configuration.
5. Normal receive and transmit operation.
6. Stop and start transmission.

1.6 Register Description

GMAC Registers consists of two parts: APB registers and AHB registers.

APB registers are used to configure clock frequency/clock enable/clock direction/PHY interface type.

AHB registers are use to configure GMAC core (DesignWare Core part).

1.6.1 Register Memory Map

GMAC AHB Registers, as described in chapter 1.6.3.

GMAC APB Registers, the detailed description of GMAC registers is shown in Figure & Table 1-6.

Figure & Table 1-6 GMAC-APB register memory map

Name	Address Offset	Width	Access	Description
GMAC_CLK_EN	0x0	32bit	R/W	Clock enable register Reset value: 0x8
GMAC_RXCLK_DELAY_CTRL	0x4	32bit	R/W	rx-clk delay control register Reset value: 0x8000
GMAC_TXCLK_DELAY_CTRL	0x8	32bit	R/W	tx-clk delay control register Reset value: 0x8000

Name	Address Offset	Width	Access	Description
GMAC_PLLCLK_DIV	0xc	32bit	R/W	PLL divider number register Reset value: 0x4
GMAC_EPHY_DIV	0x10	32bit	R/W	ephy-clk divider number register Reset value: 0x14
GMAC_PTPCLK_DIV	0x14	32bit	R/W	ptp-clk divider number register Reset value: 0x2
GMAC_GTXCLK_SEL	0x18	32bit	R/W	gtx-clk select register Reset value: 0x1
GMAC_INTF_CTRL	0x1c	32bit	R/W	GMAC PHY interface type register Reset value: 0x0
GMAC_TXCLK_OEN	0x20	32bit	R/W	txclk output enable register Reset value: 0x1

1.6.2 Register and Field Description

GMAC AHB Register, please refer to *DesignWare Cores Ethernet GMAC Universal Databook* chapter 6.3. GMAC APB register field description as following:

1.6.2.1 GMAC_CLK_EN

- Name: GMAC_CLK_EN register
- Address Offset: 0x00
- Default Value: 0x0

Figure & Table 1-7 GMAC_CLK_EN

Bits	Name	Access	Description
31:8	Reserved		
7	gmac_mdc_clk_inv	R/W	Mdc clock inverter 0: mdc clock 1: Invert mdc clock Default: 0x0
6	gmac_ephy_ref_clk_enable	R/W	GMAC ephy reference clock enable 0: Disable 1: Enable Default: 0x0

Bits	Name	Access	Description
5	gmac_rx_clk_n_enable	R/W	GMAC rx-clk_n enable 0: Disable 1: Enable Default: 0x0
4	gmac_rx_clk_enable	R/W	GMAC rx-clk enable 0: Disable 1: Enable Default: 0x0
3	gmac_tx_clk_out_enable	R/W	GMAC tx-clk_out (for PHY) enable 0: Disable 1: Enable Default: 0x1
2	gmac_tx_clk_n_out_enable	R/W	GMAC tx-clk_n enable 0: Disable 1: Enable Default: 0x0
1	gmac_tx_clk_enable	R/W	GMAC tx-clk (for GMAC) enable 0: Disable 1: Enable Default: 0x0
0	gmac_tx_clk_in_inv	R/W	GMAC tx-clk input inverter 0: tx-clk 1: Invert tx-clk Default: 0x0

1.6.2.2 GMAC_RXCLK_DELAY_CTRL

- Name: GMAC_RXCLK_DELAY_CTRL register
- Address Offset: 0x04
- Default Value: 0x8000

Figure & Table 1-8 GMAC_RXCLK_DELAY_CTRL

Bits	Name	Access	Description
31:16	Reserved		
ASIC mode			

Bits	Name	Access	Description
15	bypass	R/W	Bypass clock Default: 0x1
14	invert	R/W	Invert clock Default: 0x0
13:5	reserved		
4:0	delay_ctrl	R/W	delay_ctrl Default: 0x0
FPGA mode			
15:14	reserved		
13	mmcm reset	R/W	mmcm reset, active low Default: 0x0
12	ps_start	R/W	Phase shift start. ps_start from low to high, mmcm start phase shift. Default: 0x0
11:0	ps_cfg	R/W	Phase shift value. Shift rx_clk (to gmac), shift value: ps_cfg*18ps Default: 0x0

1.6.2.3 GMAC_TXCLK_DELAY_CTRL

- Name: GMAC_TXCLK_DELAY_CTRL register
- Address Offset: 0x08
- Default Value: 0x8000

Figure & Table 1-9 GMAC_TXCLK_DELAY_CTRL

Bits	Name	Access	Description
31:16	Reserved		
ASIC mode			
15	bypass	R/W	Bypass clock Default: 0x1
14	invert	R/W	Invert clock Default: 0x0
13:5	Reserved		
4:0	delay_ctrl	R/W	delay_ctrl

Bits	Name	Access	Description
			Default: 0x0
FPGA mode			
15:14	reserved		
13	mmcm reset	R/W	mmcm reset, active low Default: 0x0
12	ps_start	R/W	Phase shift start. ps_start from low to high, mmcm start phase shift. Default: 0x0
11:0	ps_cfg	R/W	Phase shift value. Shift gmac_ephy_clk (to PHY), shift value: ps_cfg*18ps Default: 0x0

1.6.2.4 GMAC_PLLCLK_DIV

- Name: GMAC_PLLCLK_DIV register
- Address Offset: 0x0c
- Default Value: 0x4

Figure & Table 1-10 GMAC_PLLCLK_DIV

Bits	Name	Access	Description
31	gmac_pll_clk_div_en	R/W	PLL clock divider enable Default: 0x0 Software must configure to low, then configure to high.
30:8	Reserved	-	-
7:0	gmac_pll_clk_div_num	R/W	PLL clock divider number Default: 0x4

1.6.2.5 GMAC_EPHY_DIV

- Name: GMAC_EPHY_DIV register
- Address Offset: 0x010
- Default Value: 0x14

Figure & Table 1-11 GMAC_EPHY_DIV

Bits	Name	Access	Description
31	gmac_ephy_clk_div_en	R/W	ephy clock divider enable Default: 0x0

Bits	Name	Access	Description
			Software must configure to low, then configure to high.
30:8	Reserved	-	-
7:0	gmac_ephy_clk_div_num	R/W	ephy clock divider number Default: 0x14

1.6.2.6 GMAC_PTP_DIV

- Name: GMAC_PTP_DIV register
- Address Offset: 0x014
- Default Value: 0x2

Figure & Table 1-12 GMAC_PTP_DIV

Bits	Name	Access	Description
31	gmac_ptp_clk_div_en	R/W	PTP clock divider enable Default: 0x0 Software must configure to low, then configure to high.
30:8	Reserved	-	-
3:0	gmac_ptp_clk_div_num	R/W	PTP clock divider number Default: 0x2

1.6.2.7 GMAC_GTXCLK_SEL

- Name: GMAC_GTXCLK_SEL register
- Address Offset: 0x18
- Default Value: 0x1

Figure & Table 1-13 GMAC_GTXCLK_SEL

Bits	Name	Access	Description
31:1	Reserved		
0	gmac_gtxclk_sel	R/W	Gtx-clk select Default: 0x1 1: clk_after_pll_div 0: tx_clk_in_after_inv_mu

1.6.2.8 GMAC_PHY_INTF_SEL

- Name: GMAC_INTF_CTRL register
- Address Offset: 0x1c
- Default Value: 0x0

Figure & Table 1-14 GMAC_PHY_INTF_SEL

Bits	Name	Access	Description
31:1	Reserved		
0	gmac_phy_intf_sel	R/W	GMAC PHY interface select Default: 0x0 1: RGMII 0: GMII/MII

1.6.2.9 GMAC_TXCLK_OEN

- Name: GMAC_TXCLK_OEN register
- Address Offset: 0x20
- Default Value: 0x1

Figure & Table 1-15 GMAC_TXCLK_OEN

Bits	Name	Access	Description
31:1	Reserved		
0	gmac_txclk_oen	R/W	Tx-clk output enable Default: 0x1 1: tx-clk as input 0: tx_clk as output

1.6.3 GMAC Core Register Description

GMAC core register consists of DMA registers and GMAC registers.
The following are DMA registers.

1.6.3.1 Register 0 (Bus Mode Register)

The Bus Mode register establishes the bus operating modes for the DMA.

Figure & Table 1-16 Register 0 (Bus Mode Register)

Bits	Name	Access	Description
29:28	PRWG	R_W	Channel Priority Weights This field sets the priority weights for Channel 0 during the round-robin arbitration between the DMA channels for the system bus. ■ 00: The priority weight is 1. ■ 01: The priority weight is 2. ■ 10: The priority weight is 3.

Bits	Name	Access	Description
			■ 11: The priority weight is 4. This field is present in all DWC_gmac configurations except GMAC-AXI when you select the AV feature. Otherwise, this field is reserved and read-only (RO). Reset Value: 00
27	TXPR	R_W	Transmit Priority When set, this bit indicates that the transmit DMA has higher priority than the receive DMA during arbitration for the system-side bus. In the GMAC-AXI configuration, this bit is reserved and RO. Reset Value: 0
26	MB	R_W	Mixed Burst When this bit is set high and the FB bit is low, the AHB master interface starts all bursts of length more than 16 with INCR (undefined burst), whereas it reverts to fixed burst transfers (INCRx and SINGLE) for burst length of 16 and less. This bit is valid only in the GMAC-AHB configuration and reserved in all other configuration. Reset Value: 0
25	AAL	R_W	Address-Aligned Beats When this bit is set high and the FB bit is equal to 1, the AHB or AXI interface generates all bursts aligned to the start address LS bits. If the FB bit is equal to 0, the first burst (accessing the start address of data buffer) is not aligned, but subsequent bursts are aligned to the address. This bit is valid only in the GMAC-AHB and GMAC-AXI configurations and is reserved (RO with default value 0) in all other configurations. Reset Value: 0
24	PBLx8	R_W	PBLx8 Mode When set high, this bit multiplies the programmed PBL value (bit[22:17] and bit[13:8]) eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. Note: This bit function is not backward compatible. Before release 3.50a, this bit was 4xPBL. Reset Value: 0

Bits	Name	Access	Description
23	USP	R_W	Use Separate PBL When set high, this bit configures the Rx DMA to use the value configured in bit[22:17] as PBL. The PBL value in bit [13:8] is applicable only to the Tx DMA operations. When reset to low, the PBL value in bit[13:8] is applicable for both DMA engines. Reset Value: 0
22:17	RPBL	R_W	Rx DMA PBL This field indicates the maximum number of beats to be transferred in one Rx DMA transaction. This is the maximum value that is used in a single block Read or Write. The Rx DMA always attempts to burst as specified in the RPBL bit each time it starts a Burst transfer on the host bus. You can program RPBL with values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. This field is valid and applicable only when USP is set high. Reset Value: 01H
16	FB	R_W	Fixed Burst This bit controls whether the AHB or AXI master interface performs fixed burst transfers or not. When set, the AHB interface uses only SINGLE, INCR4, INCR8, or INCR16 during start of the normal burst transfers. When reset, the AHB or AXI interface uses SINGLE and INCR burst transfer operations. For more information, see Bit 0 (UNDEF) of the AXI Bus Mode register in the GMAC-AXI configuration. Reset Value: 0
15:14	PR	R_W	Priority Ratio These bits control the priority ratio in the weighted round-robin arbitration between the Rx DMA and Tx DMA. These bits are valid only when Bit 1 (DA) is reset. The priority ratio is Rx:Tx or Tx:Rx depending on whether Bit 27 (TXPR) is reset or set. ■ 00: The Priority Ratio is 1:1. ■ 01: The Priority Ratio is 2:1. ■ 10: The Priority Ratio is 3:1. ■ 11: The Priority Ratio is 4:1.

Bits	Name	Access	Description
			In the GMAC-AXI configuration, these bits are reserved and RO. Reset Value: 00
13:8	PBL	R_W	Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This is the maximum value that is used in a single block Read or Write. The DMA always attempts to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. When USP is set high, this PBL value is applicable only for Tx DMA transactions. If the number of beats to be transferred is more than 32, then perform the following steps: Set the PBLx8 mode. Set the PBL. For example, if the maximum number of beats to be transferred is 64, then first set PBLx8 to 1 and then set PBL to 8. The PBL values have the following limitation: The maximum number of possible beats (PBL) is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified. Reset Value: 01H
7	ATDS	R_W	Alternate Descriptor Size When set, the size of the alternate descriptor increases to 32 bytes (8 DWORDS). This is required when the Advanced Timestamp feature or the IPC Full Checksum Offload Engine (Type 2) is enabled in the receiver. The enhanced descriptor is not required if the Advanced Timestamp and IPC Full Checksum Offload Engine (Type 2) features are not enabled. In such case, you can use the 16 bytes descriptor to save 4 bytes of memory. This bit is present only when you select the Alternate Descriptor feature and any one of the following features during core configuration: ■ Advanced Timestamp feature ■ IPC Full Checksum Offload Engine (Type 2) feature Otherwise, this bit is reserved and is read-only.

Bits	Name	Access	Description
			When reset, the descriptor size reverts back to 4 DWORDs (16 bytes). This bit preserves the backward compatibility for the descriptor size. In versions prior to 3.50a, the descriptor size is 16 bytes for both normal and enhanced descriptors. In version 3.50a, descriptor size is increased to 32 bytes because of the Advanced Timestamp and IPC Full Checksum Offload Engine (Type 2) features. Reset Value: 0
6:2	DSL	R_W	Descriptor Skip Length This bit specifies the number of Word, Dword, or Lword (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When the DSL value is equal to zero, the descriptor table is taken as contiguous by the DMA in Ring mode. Reset Value: 00H
1	DA	R_W	DMA Arbitration Scheme This bit specifies the arbitration scheme between the transmit and receive paths of Channel 0. ■ 0: Weighted round-robin with Rx:Tx or Tx:Rx The priority between the paths is according to the priority specified in bit[15:14] (PR) and priority weights specified in Bit 27 (TXPR). ■ 1: Fixed priority The transmit path has priority over receive path when Bit 27 (TXPR) is set. Otherwise, receive path has priority over the transmit path. In the GMAC-AXI configuration, these bits are reserved and are RO. Reset Value: 0
0	SWR	R_WS_ SC	Software Reset When this bit is set, the MAC DMA Controller resets the logic and all internal registers of the MAC. It is cleared automatically after the reset operation is complete in all of the DWC_gmac clock domains. Before reprogramming any register of the DWC_gmac, you should read a zero (0) value in this bit.

Bits	Name	Access	Description
			Note: ■ The Software reset function is driven only by this bit. Bit 0 of Register 64 (Channel 1 Bus Mode Register) or Register 128 (Channel 2 Bus Mode Register) has no impact on the Software reset function. ■ The reset operation is completed only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for the software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Reset Value: 1

Figure & Table 1-17 provides the valid PBL range (including x8 mode) for different data bus widths and FIFO sizes.

NOTE

If the PBL is common for both transmit and receive DMA, the minimum Rx FIFO and Tx FIFO depths must be considered.

In Figure & Table 1-17, the valid PBL range, specified in the half-duplex mode, is applicable only for Tx FIFO. In addition, for 1000Mbps mode, if PBL is not specified in Figure & Table 1-17, it means that the PBL less than or equal to half of the depth is supported.

Figure & Table 1-17 Valid PBL range

Data Bus Width	FIFO Depth	Valid PBL Range in Full Duplex Mode	Valid PBL Range in Half Duplex Mode (Only for Tx FIFO)
32	128Bytes	16 or less	8 or less (10/100Mbps mode only)
	256Bytes	32 or less	32 or less (10/100Mbps mode only)
	512Bytes	64 or less	64 or less (10/100Mbps mode only)
	1KB	128 or less	■ 128 or less in 10/100Mbps mode ■ 64 or less in 1000Mbps mode
	2KB and higher	All	All
64	128Bytes	8 or less	4 or less (10/100Mbps mode only)
	256Bytes	16 or less	16 or less (10/100Mbps mode only)
	512Bytes	32 or less	32 or less (10/100Mbps mode only)
	1KB	64 or less	■ 64 or less in 10/100Mbps mode ■ 32 or less in 1000Mbps mode
	2KB	128 or less	128 or less

Data Bus Width	FIFO Depth	Valid PBL Range in Full Duplex Mode	Valid PBL Range in Half Duplex Mode (Only for Tx FIFO)
	4KB and higher	All	All
128	128Bytes	4 or less	2 or less (10/100Mbps mode only)
	256Bytes	8 or less	8 or less (10/10 Mbps mode only)
	512Bytes	16 or less	16 or less (10/100Mbps mode only)
	1KB	32 or less	■ 32 or less in 10/100Mbps mode only ■ 16 or less in 1000Mbps mode only
	2KB	64 or less	64 or less
	4KB	128 or less	128 or less
	8KB and higher	All	All

1.6.3.2 Register 1 (Transmit Poll Demand Register)

The Transmit Poll Demand register enables the Tx DMA to check whether or not the DMA owns the current descriptor. The Transmit Poll Demand command is given to wake up the Tx DMA if it is in the suspend mode. The Tx DMA can go into the suspend mode because of an underflow error in a transmitted frame or the unavailability of descriptors owned by it. You can give this command anytime, and the Tx DMA resets this command when it again starts fetching the current descriptor from host memory. When this register is read, it always returns zero.

Figure & Table 1-18 Register 1 (Transmit Poll Demand Register)

Bits	Name	Access	Description
31:0	TPD	RO_WT	Transmit Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 18 (Current Host Transmit Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the transmission returns to the Suspend state and Bit 2 (TU) of Register 5 (Status Register) is asserted. If the descriptor is available, the transmission resumes. Reset Value: 0000_0000H

1.6.3.3 Register 2 (Receive Poll Demand Register)

The Receive Poll Demand register enables the Rx DMA to check for new descriptors. This command is given to wake up the Rx DMA from the suspend state. The Rx DMA can go into the suspend state only because of the unavailability of descriptors it owns. When this register is read, it always returns zero.

Figure & Table 1-19 Register 2 (Receive Poll Demand Register)

Bits	Name	Access	Description
31:0	RPD	RO_WT	Receive Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 19 (Current Host Receive Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the reception returns to the suspended state and Bit 7 (RU) of Register 5 (Status Register) is asserted. If the descriptor is available, the Rx DMA returns to the active state. Reset Value: 0000_0000H

1.6.3.4 Register 3 (Receive Descriptor List Address Register)

The Receive Descriptor List Address register points to the start of the Receive Descriptor List. The descriptor lists reside in the host's physical memory space and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given.

You can write to this register only when Rx DMA has stopped, that is, Bit 1 (SR) is set to zero in Register 6 (Operation Mode Register). When stopped, this register can be written with a new descriptor list address.

When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

If this register is not changed when the SR bit is set to 0, then the DMA takes the descriptor address where it was stopped earlier.

Figure & Table 1-20 Register 3 (Receive Descriptor List Address Register)

Bits	Name	Access	Description
31:0	RDESLA	R_W	Start of Receive List This field contains the base address of the first descriptor in the Receive Descriptor list. The LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only. Reset Value: 0000_0000H

1.6.3.5 Register 4 (Transmit Descriptor List Address Register)

The Transmit Descriptor List Address register points to the start of the Transmit Descriptor List. The descriptor lists reside in the host's physical memory space and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB low.

You can write to this register only when the Tx DMA has stopped, that is, Bit 13 (ST) is set to zero in Register 6 (Operation Mode Register). When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly programmed descriptor base address.

If this register is not changed when the ST bit is set to 0, then the DMA takes the descriptor address where it was stopped earlier.

Figure & Table 1-21 Register 4 (Transmit Descriptor List Address Register)

Bits	Name	Access	Description
31:0	TDESLA	R_W	Start of Transmit List This field contains the base address of the first descriptor in the Transmit Descriptor list. The LSB bits (1:0, 2:0, 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and are internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only. Reset Value: 0000_0000H

1.6.3.6 Register 5 (Status Register)

The Status register contains all status bits that the DMA reports to the host. The software driver reads this register during an interrupt service routine or polling. Most of the fields in this register cause the host to be interrupted. The bits of this register are not cleared when read. Writing 1’b1 to (unreserved) Bits [16:0] of this register clears these bits and writing 1’b0 has no effect. Each field (Bits[16:0]) can be masked by masking the appropriate bit in Register 7 (Interrupt Enable Register).

Figure & Table 1-22 Register 5 (Status Register)

Bits	Name	Access	Description
31	-	RO	Reserved Reset Value: 0

Bits	Name	Access	Description
30	GLPII or GTMSI	RO	GLPII: GMAC LPI Interrupt (for Channel 0) This bit indicates an interrupt event in the LPI logic of the MAC. To reset this bit to 1'b0, the software must read the corresponding registers in the DWC_gmac to get the exact cause of the interrupt and clear its source. Note: GLPII status is given only in Channel 0 DMA register and is applicable only when the Energy Efficient Ethernet feature is enabled. Otherwise, this bit is reserved. When this bit is high, the interrupt signal from the MAC (sbd_intr_o) is high. GTMSI: GMAC TMS Interrupt (for Channel 1 and Channel 2) This bit indicates an interrupt event in the traffic manager and scheduler logic of DWC_gmac. To reset this bit, the software must read the corresponding registers (Channel Status Register) to get the exact cause of the interrupt and clear its source. Note: GTMSI status is given only in Channel 1 and Channel 2 DMA register when the AV feature is enabled and corresponding additional transmit channels are present. Otherwise, this bit is reserved. When this bit is high, the interrupt signal from the MAC (sbd_intr_o) is high. Reset Value: 0
29	TTI	RO	Timestamp Trigger Interrupt This bit indicates an interrupt event in the Timestamp Generator block of the DWC_gmac. The software must read the corresponding registers in the DWC_gmac to get the exact cause of the interrupt and clear its source to reset this bit to 1'b0. When this bit is high, the interrupt signal from the DWC_gmac subsystem (sbd_intr_o) is high. This bit is applicable only when the IEEE 1588 Timestamp feature is enabled. Otherwise, this bit is reserved. Reset Value: 0

Bits	Name	Access	Description
28	GPI	RO	GMAC PMT Interrupt This bit indicates an interrupt event in the PMT module of the DWC_gmac. The software must read the PMT Control and Status Register in the MAC to get the exact cause of interrupt and clear its source to reset this bit to 1'b0. The interrupt signal from the DWC_gmac subsystem (sbd_intr_o) is high when this bit is high. This bit is applicable only when the Power Management feature is enabled. Otherwise, this bit is reserved. Note: The GPI and pmt_intr_o interrupts are generated in different clock domains. Reset Value: 0
27	GMI	RO	GMAC MMC Interrupt This bit reflects an interrupt event in the MMC module of the DWC_gmac. The software must read the corresponding registers in the DWC_gmac to get the exact cause of the interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the DWC_gmac subsystem (sbd_intr_o) is high when this bit is high. This bit is applicable only when the MAC Management Counters (MMC) are enabled. Otherwise, this bit is reserved. Reset Value: 0
26	GLI	RO	GMAC Line Interface Interrupt When set, this bit reflects any of the following interrupt events in the DWC_gmac interfaces (if present and enabled in your configuration): ■ PCS (TBI, RTBI, or SGMII): Link change or auto-negotiation complete event ■ SMII or RGMII: Link change event ■ General Purpose Input Status (GPIS): Any LL or LH event on the gpi_i input ports To identify the exact cause of the interrupt, the software must first read Bit 11 and Bits[2:0] of Register 14 (Interrupt Status Register) and then to clear the source of interrupt (which also clears the GLI interrupt), read any of the following corresponding registers: ■ PCS (TBI, RTBI, or SGMII): Register 49 (AN Status Register)

Bits	Name	Access	Description
			■ SMII or RGMII: Register 54 (SGMII/RGMII/SMII Control and Status Register) ■ General Purpose Input (GPI): Register 56 (General Purpose IO Register) The interrupt signal from the DWC_gmac subsystem (sbd_intr_o) is high when this bit is high. Reset Value: 0
25:23	EB	RO	Error Bits This field indicates the type of error that caused a Bus Error, for example, error response on the AHB or AXI interface. This field is valid only when Bit 13 (FBI) is set. This field does not generate an interrupt. ■ 000: Error during Rx DMA Write Data Transfer ■ 011: Error during Tx DMA Read Data Transfer ■ 100: Error during Rx DMA Descriptor Write Access ■ 101: Error during Tx DMA Descriptor Write Access ■ 110: Error during Rx DMA Descriptor Read Access ■ 111: Error during Tx DMA Descriptor Read Access Note: 001 and 010 are reserved. Reset Value: 000
22:20	TS	RO	Transmit Process State This field indicates the Transmit DMA FSM state. This field does not generate an interrupt. ■ 3’b000: Stopped; Reset or Stop Transmit Command issued ■ 3’b001: Running; Fetching Transmit Transfer Descriptor ■ 3’b010: Running; Waiting for status ■ 3’b011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO) ■ 3’b100: TIME_STAMP write state ■ 3’b101: Reserved for future use ■ 3’b110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow ■ 3’b111: Running; Closing Transmit Descriptor Reset Value: 000

Bits	Name	Access	Description
19:17	RS	RO	Receive Process State This field indicates the Receive DMA FSM state. This field does not generate an interrupt. ■ 3’b000: Stopped: Reset or Stop Receive Command issued ■ 3’b001: Running: Fetching Receive Transfer Descriptor ■ 3’b010: Reserved for future use ■ 3’b011: Running: Waiting for receive packet ■ 3’b100: Suspended: Receive Descriptor Unavailable ■ 3’b101: Running: Closing Receive Descriptor ■ 3’b110: TIME_STAMP write state ■ 3’b111: Running: Transferring the receive packet data from receive buffer to host memory Reset Value: 000
16	NIS	R_SS_WC	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): ■ Register 5[0]: Transmit Interrupt ■ Register 5[2]: Transmit Buffer Unavailable ■ Register 5[6]: Receive Interrupt ■ Register 5[14]: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in Register 7) affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes NIS to be set, is cleared. Reset Value: 0
15	AIS	R_SS_WC	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): ■ Register 5[1]: Transmit Process Stopped

Bits	Name	Access	Description
			■ Register 5[3]: Transmit Jabber Timeout ■ Register 5[4]: Receive FIFO Overflow ■ Register 5[5]: Transmit Underflow ■ Register 5[7]: Receive Buffer Unavailable ■ Register 5[8]: Receive Process Stopped ■ Register 5[9]: Receive Watchdog Timeout ■ Register 5[10]: Early Transmit Interrupt ■ Register 5[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Reset Value: 0
14	ERI	R_SS_WC	Early Receive Interrupt This bit indicates that the DMA filled the first data buffer of the packet. This bit is cleared when the software writes 1 to this bit or Bit 6 (RI) of this register is set (whichever occurs earlier). Reset Value: 0
13	FBI	R_SS_WC	Fatal Bus Error Interrupt This bit indicates that a bus error occurred, as described in Bits [25:23]. When this bit is set, the corresponding DMA engine disables all of its bus accesses. Reset Value: 0
12:11	-	RO	Reserved Reset Value: 00
10	ETI	R_SS_WC	Early Transmit Interrupt This bit indicates that the frame to be transmitted is fully transferred to the MTL Transmit FIFO. Reset Value: 0

Bits	Name	Access	Description
9	RWT	R_SS_WC	Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer expired while receiving the current frame and the current frame is truncated after the watchdog timeout. Reset Value: 0
8	RPS	R_SS_WC	Receive Process Stopped This bit is asserted when the Receive Process enters the Stopped state. Reset Value: 0
7	RU	R_SS_WC	Receive Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Receive List and the DMA cannot acquire it. The Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, the Receive Process resumes when the next recognized incoming frame is received. This bit is set only when the previous Receive Descriptor is owned by the DMA. Reset Value: 0
6	RI	R_SS_WC	Receive Interrupt This bit indicates that the frame reception is complete. When reception is complete, the Bit 31 of RDES1 (Disable Interrupt on Completion) is reset in the last Descriptor, and the specific frame status information is updated in the descriptor. The reception remains in the Running state. Reset Value: 0
5	UNF	R_SS_WC	Transmit Underflow This bit indicates that the Transmit Buffer had an underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set. Reset Value: 0

Bits	Name	Access	Description
4	OVF	R_SS_WC	Receive Overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to the application, the overflow status is set in RDES0[11]. Reset Value: 0
3	TJT	R_SS_WC	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired, which happens when the frame size exceeds 2,048 (10,240 bytes when the Jumbo frame is enabled). When the Jabber Timeout occurs, the transmission process is aborted and placed in the stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert. Reset Value: 0
2	TU	R_SS_WC	Transmit Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Transmit List and the DMA cannot acquire it. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing Transmit descriptors, the host should change the ownership of the descriptor by setting TDES0[31] and then issue a Transmit Poll Demand command. Reset Value: 0
1	TPS	R_SS_WC	Transmit Process Stopped This bit is set when the transmission is stopped. Reset Value: 0
0	TI	R_SS_WC	Transmit Interrupt This bit indicates that the frame transmission is complete. When transmission is complete, Bit 31 (OWN) of TDES0 is reset, and the specific frame status information is updated in the descriptor. Reset Value: 0

1.6.3.7 Register 6 (Operation Mode Register)

The Operation Mode register establishes the Transmit and Receive operating modes and commands. This register should be the last CSR to be written as part of the DMA initialization. This register is also present in the GMAC-MTL configuration with bits unused and reserved 24, 13, 2, and 1.

Figure & Table 1-23 Register 6 (Operation Mode Register)

Bits	Name	Access	Description
31:27	-	RO	Reserved Reset Value: 0H
26	DT	R_W	Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the MAC does not drop the frames which only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors only in the encapsulated payload. When this bit is reset, all error frames are dropped if the FEF bit is reset. If the IPC Full Checksum Offload Engine (Type 2) is disabled, this bit is reserved (RO with value 1'b0). Reset Value: 0
25	RSF	R_W	Receive Store and Forward When this bit is set, the MTL reads a frame from the Rx FIFO only after the complete frame has been written to it, ignoring the RTC bits. When this bit is reset, the Rx FIFO operates in the cut-through mode, subject to the threshold specified by the RTC bits. Reset Value: 0
24	DFF	R_W	Disable Flushing of Received Frames When this bit is set, the Rx DMA does not flush any frames because of the unavailability of receive descriptors or buffers as it does normally when this bit is reset. (See “Receive Process Suspended” on page 83.) This bit is reserved (and RO) in the GMAC-MTL configuration. Reset Value: 0
23	RFA_2	R_W	MSB of Threshold for Activating Flow Control If the DWC_gmac is configured for an Rx FIFO size of 8KB or more, this bit (when set) provides additional threshold levels for activating the flow control in both halfduplex and full-duplex modes. This bit (as Most Significant Bit), along with the RFA (Bits [10:9]), gives the following thresholds for activating flow control:

Bits	Name	Access	Description
			■ 100: Full minus 5KB, that is, FULL – 5KB ■ 101: Full minus 6KB, that is, FULL – 6KB ■ 110: Full minus 7KB, that is, FULL – 7KB ■ 111: Reserved This bit is reserved (and RO) if the Rx FIFO is 4KB or less deep. Reset Value: 0
22	RFD_2	R_W	MSB of Threshold for Deactivating Flow Control If the DWC_gmac is configured for Rx FIFO size of 8KB or more, this bit (when set) provides additional threshold levels for deactivating the flow control in both half-duplex and full-duplex modes. This bit (as Most Significant Bit) along with the RFD (Bits [12:11]) gives the following thresholds for deactivating flow control: ■ 100: Full minus 5KB, that is, FULL – 5KB ■ 101: Full minus 6KB, that is, FULL – 6KB ■ 110: Full minus 7KB, that is, FULL – 7KB ■ 111: Reserved This bit is reserved (and RO) if the Rx FIFO is 4KB or less deep. Reset Value: 0
21	TSF	R_W	Transmit Store and Forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in Bits [16:14] are ignored. This bit should be changed only when the transmission is stopped. Reset Value: 0
20	FTF	R_WS_ SC	Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost or flushed. This bit is cleared internally when the flushing operation is complete. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt frame transmission.

Bits	Name	Access	Description
			Note: The flush operation is complete only when the Tx FIFO is emptied of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock (clk_tx_i) is required to be active. Reset Value: 0
19:17	-	RO	Reserved Reset Value: 000
16:14	TTC	R_W	Transmit Threshold Control These bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when Bit 21 (TSF) is reset. ■ 000: 64 ■ 001: 128 ■ 010: 192 ■ 011: 256 ■ 100: 40 ■ 101: 32 ■ 110: 24 ■ 111: 16 Reset Value: 000
13	ST	R_W	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by Register 4 (Transmit Descriptor List Address Register), or from the position retained when transmission was stopped previously. If the DMA does not own the current descriptor, transmission enters the Suspended state and Bit 2 (Transmit Buffer Unavailable) of Register 5 (Status Register) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting Register 4 (Transmit Descriptor List

Bits	Name	Access	Description
			Address Register), then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and it becomes the current position when transmission is restarted. To change the list address, you need to program Register 4 (Transmit Descriptor List Address Register) with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current frame is complete or the transmission is in the Suspended state. Note: For information about how to pause the transmission, see "Stopping and Starting Transmission" on page 715. Reset Value: 0
12:11	RFD	R_W	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill-level of Rx FIFO) at which the flow control is de-asserted after activation. ■ 00: Full minus 1KB, that is, FULL − 1KB ■ 01: Full minus 2KB, that is, FULL − 2KB ■ 10: Full minus 3KB, that is, FULL − 3KB ■ 11: Full minus 4KB, that is, FULL − 4KB The de-assertion is effective only after flow control is asserted. If the Rx FIFO is 8KB or more, an additional Bit (RFD_2) is used for more threshold levels as described in Bit 22. These bits are reserved and read-only when the Rx FIFO depth is less than 4KB. Note: For proper flow control, the value programmed in the "RFD_2, RFD" fields should be equal to or more than the value programmed in the "RFA_2, RFA" fields. Reset Value: 00
10:9	RFA	R_W	Threshold for Activating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill level of Rx FIFO) at which the flow control is activated. ■ 00: Full minus 1KB, that is, FULL−1KB ■ 01: Full minus 2KB, that is, FULL−2KB

Bits	Name	Access	Description
			■ 10: Full minus 3KB, that is, FULL−3KB ■ 11: Full minus 4KB, that is, FULL−4KB These values are applicable only to Rx FIFOs of 4KB or more and when Bit 8 (EFC) is set high. If the Rx FIFO is 8KB or more, an additional Bit (RFA_2) is used for more threshold levels as described in Bit 23. These bits are reserved and read-only when the depth of Rx FIFO is less than 4KB. Note: When FIFO size is exactly 4KB, although the DWC_gmac allows you to program the value of these bits to 11, the software should not program these bits to 2'b11. The value 2'b11 means flow control on FIFO empty condition. Reset Value: 00
8	EFC	R_W	Enable HW Flow Control When this bit is set, the flow control signal operation based on the fill-level of Rx FIFO is enabled. When reset, the flow control operation is disabled. This bit is not used (reserved and always reset) when the Rx FIFO is less than 4KB. Reset Value: 0
7	FEF	R_W	Forward Error Frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, or overflow). However, if the start byte (write) pointer of a frame is already transferred to the read controller side (in Threshold mode), then the frame is not dropped. In the GMAC-MTL configuration in which the Frame Length FIFO is also enabled during core configuration, the Rx FIFO drops the error frames if that frame's start byte is not transferred (output) on the ARI bus. When the FEF bit is set, all frames except runt error frames are forwarded to the DMA. If the Bit 25 (RSF) is set and the Rx FIFO overflows when a partial frame is written, then the frame is dropped irrespective of the FEF bit setting. However, if the Bit 25 (RSF) is reset and the Rx FIFO overflows when a partial frame is written, then a partial frame may be forwarded to the DMA. Note: When FEF bit is reset, the giant frames are dropped if the giant frame status is given in Rx Status (in Table 8-6 or Table 8-23) in the following

Bits	Name	Access	Description
			configurations: ■ The IP checksum engine (Type 1) and full checksum offload engine (Type 2) are not selected. ■ The advanced timestamp feature is not selected but the extended status is selected. The extended status is available with the following features: L3-L4 filter in GMAC-CORE or GMAC-MTL configurations Full checksum offload engine (Type 2) with enhanced descriptor format in the GMAC-DMA, GMAC-AHB, or GMAC-AXI configurations. Reset Value: 0
6	FUF	R_W	Forward Undersized Good Frames When set, the Rx FIFO forwards Undersized frames (that is, frames with no Error and length less than 64 bytes) including pad-bytes and CRC. When reset, the Rx FIFO drops all frames of less than 64 bytes, unless a frame is already transferred because of the lower value of Receive Threshold, for example, RTC = 01. Reset Value: 0
5	DGF	R_W	Drop Giant Frames When set, the MAC drops the received giant frames in the Rx FIFO, that is, frames that are larger than the computed giant frame limit. When reset, the MAC does not drop the giant frames in the Rx FIFO. Note: This bit is available in the following configurations in which the giant frame status is not provided in Rx status and giant frames are not dropped by default: ■ Configurations in which IP Checksum Offload (Type 1) is selected in Rx ■ Configurations in which the IPC Full Checksum Offload Engine (Type 2) is selected in Rx with normal descriptor format ■ Configurations in which the Advanced Timestamp feature is selected In all other configurations, this bit is not used (reserved and always reset). Reset Value: 0

Bits	Name	Access	Description
4:3	RTC	R_W	Receive Threshold Control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with length less than the threshold are automatically transferred. The value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. ■ 00: 64 ■ 01: 32 ■ 10: 96 ■ 11: 128 Reset Value: 00
2	OSF	R_W	Operate on Second Frame When this bit is set, it instructs the DMA to process the second frame of the Transmit data even before the status for the first frame is obtained. Reset Value: 0
1	SR	R_W	Start or Stop Receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes the incoming frames. The descriptor acquisition is attempted from the current position in the list, which is the address set by the Register 3 (Receive Descriptor List Address Register) or the position retained when the Receive process was previously stopped. If the DMA does not own the descriptor, reception is suspended and Bit 7 (Receive Buffer Unavailable) of Register 5 (Status Register) is set. The Start Receive command is effective only when the reception has stopped. If the command is issued before setting Register 3 (Receive Descriptor List Address Register), the DMA behavior is unpredictable. When this bit is cleared, the Rx DMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is effective

Bits	Name	Access	Description
			only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state. Reset Value: 0
0	-	RO	Reserved Reset Value: 0

1.6.3.8 Register 7 (Interrupt Enable Register)

The Interrupt Enable register enables the interrupts reported by Register 5 (Status Register). Setting a bit to 1'b1 enables a corresponding interrupt. After a hardware reset or software reset, all interrupts are disabled.

Figure & Table 1-24 Register 7 (Interrupt Enable Register)

Bits	Name	Access	Description
31:17	-	RO	Reserved Reset Value: 0000H
16	NIE	R_W	Normal Interrupt Summary Enable When this bit is set, normal interrupt summary is enabled. When this bit is reset, normal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ■ Register 5[0]: Transmit Interrupt ■ Register 5[2]: Transmit Buffer Unavailable ■ Register 5[6]: Receive Interrupt ■ Register 5[14]: Early Receive Interrupt Reset Value: 0
15	AIE	R_W	Abnormal Interrupt Summary Enable When this bit is set, abnormal interrupt summary is enabled. When this bit is reset, the abnormal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ■ Register 5[1]: Transmit Process Stopped ■ Register 5[3]: Transmit Jabber Timeout ■ Register 5[4]: Receive Overflow ■ Register 5[5]: Transmit Underflow ■ Register 5[7]: Receive Buffer Unavailable ■ Register 5[8]: Receive Process Stopped ■ Register 5[9]: Receive Watchdog Timeout

Bits	Name	Access	Description
			■ Register 5[10]: Early Transmit Interrupt ■ Register 5[13]: Fatal Bus Error Reset Value: 0
14	ERE	R_W	Early Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Early Receive Interrupt is enabled. When this bit is reset, the Early Receive Interrupt is disabled. Reset Value: 0
13	FBE	R_W	Fatal Bus Error Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Fatal Bus Error Interrupt is enabled. When this bit is reset, the Fatal Bus Error Enable Interrupt is disabled. Reset Value: 0
12:11	-	RO	Reserved Reset Value: 00
10	ETE	R_W	Early Transmit Interrupt Enable When this bit is set with an Abnormal Interrupt Summary Enable (Bit 15), the Early Transmit Interrupt is enabled. When this bit is reset, the Early Transmit Interrupt is disabled. Reset Value: 0
9	RWE	R_W	Receive Watchdog Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout Interrupt is disabled. Reset Value: 0
8	RSE	R_W	Receive Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped Interrupt is disabled. Reset Value: 0

Bits	Name	Access	Description
7	RUE	R_W	Receive Buffer Unavailable Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled. Reset Value: 0
6	RIE	R_W	Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. Reset Value: 0
5	UNE	R_W	Underflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Underflow Interrupt is enabled. When this bit is reset, the Underflow Interrupt is disabled. Reset Value: 0
4	OVE	R_W	Overflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Overflow Interrupt is enabled. When this bit is reset, the Overflow Interrupt is disabled. Reset Value: 0
3	TJE	R_W	Transmit Jabber Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, the Transmit Jabber Timeout Interrupt is disabled. Reset Value: 0
2	TUE	R_W	Transmit Buffer Unavailable Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable Interrupt is disabled. Reset Value: 0
1	TSE	R_W	Transmit Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmission Stopped Interrupt is

Bits	Name	Access	Description
			enabled. When this bit is reset, the Transmission Stopped Interrupt is disabled. Reset Value: 0
0	TIE	R_W	Transmit Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. Reset Value: 0

NOTE

Interrupt generated from each channel is combined by using the OR function and is given as a single bit output. Therefore, in AV mode, the software must read the DMA Interrupt Status register of all channels to get the source of interrupt.

1.6.3.9 Register 8 (Missed Frame and Buffer Overflow Counter Register)

The DMA maintains two counters to track the number of frames missed during reception. This register reports the current value of the counter. The counter is used for diagnostic purposes. Bits[15:0] indicate missed frames because of the host buffer being unavailable. Bits[27:17] indicate missed frames because of buffer overflow conditions (MTL and MAC) and runt frames (good frames of less than 64 bytes) dropped by the MTL.

Figure & Table 1-25 Register 8 (Missed Frame and Buffer Overflow Counter Register)

Bits	Name	Access	Description
31:29	-	RO	Reserved Reset Value: 000
28	OVFCNTOVF	R_SS_RC	Overflow Bit for FIFO Overflow Counter This bit is set every time the Overflow Frame Counter (Bits[27:17]) overflows, that is, the Rx FIFO overflows with the overflow frame counter at maximum value. In such a scenario, the overflow frame counter is reset to all-zeros and this bit indicates that the rollover happened. Reset Value: 0
27:17	OVFFRMCNT	R_SS_RC	Overflow Frame Counter This field indicates the number of frames missed by the application. This counter is incremented each time the MTL FIFO overflows. The counter is cleared when this register is read with mci_be_i[2] at 1’b1. Reset Value: 000H

Bits	Name	Access	Description
16	MISCNTOVF	R_SS_RC	Overflow Bit for Missed Frame Counter This bit is set every time Missed Frame Counter (Bits[15:0]) overflows, that is, the DMA discards an incoming frame because of the Host Receive Buffer being unavailable with the missed frame counter at maximum value. In such a scenario, the Missed frame counter is reset to all-zeros and this bit indicates that the rollover happened. Reset Value: 0
15:0	MISFRMCNT	R_SS_RC	Missed Frame Counter This field indicates the number of frames missed by the controller because of the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Reset Value: 0000H

1.6.3.10 Register 9 (Receive Interrupt Watchdog Timer Register)

This register, when written with a non-zero value, enables the watchdog timer for the Receive Interrupt (Bit 6) of Register 5 (Status Register).

Figure & Table 1-26 Register 9 (Receive Interrupt Watchdog Timer Register)

Bits	Name	Access	Description
31:8	-	RO	Reserved Reset Value: 000000H
7:0	RIWT	R_W	RI Watchdog Timer Count This bit indicates the number of system clock cycles multiplied by 256 for which the watchdog timer is set. The watchdog timer gets triggered with the programmed value after the Rx DMA completes the transfer of a frame for which the RI status bit is not set because of the setting in the corresponding descriptor RDES1[31]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per RDES1[31] of any received frame. Reset Value: 00H

1.6.3.11 Register 10 (AXI Bus Mode Register)

The AXI Bus Mode Register controls the behavior of the AXI master. It is mainly used to control the burst splitting and the number of outstanding requests. This register is present and valid only in the GMAC-AXI configuration. In addition, this register is valid only in the Channel 0 DMA when multiple channels are present in the AV mode.

Figure & Table 1-27 Register 10 (AXI Bus Mode Register)

Bits	Name	Access	Description
31	EN_LPI	R_W	Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the GMAC-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. Reset Value: 0
30	LPI_XIT_FRM	R_W	Unlock on Magic Packet or Remote Wake-Up Frame When set to 1, this bit enables the GMAC-AXI to come out of the LPI mode only when the magic packet or remote wake-up frame is received. When set to 0, this bit enables the GMAC-AXI to come out of LPI mode when any frame is received. Reset Value: 0
29:24	-	RO	Reserved Reset Value: 00H
23:20	WR_OSR_LMT	R_W	AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note: ■ Bit 22 is reserved if AXI_GM_MAX_WR_REQUESTS = 4. ■ Bit 23 bit is reserved if AXI_GM_MAX_WR_REQUESTS != 16. Reset Value: ‘h1
19:16	RD_OSR_LMT	R_W	AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1

Bits	Name	Access	Description
			Note: ■ Bit 18 is reserved if AXI_GM_MAX_RD_REQUESTS = 4. ■ Bit 19 is reserved if AXI_GM_MAX_RD_REQUESTS != 16. Reset Value: ‘h1
15:14	-	RO	Reserved Reset Value: 00
13	ONEKBBE	R_W	1KB Boundary Crossing Enable for the GMAC-AXI Master When set, the GMAC-AXI master performs burst transfers that do not cross 1KB boundary. When reset, the GMAC-AXI master performs burst transfers that do not cross 4KB boundary. Reset Value: 0
12	AXI_AAL	RO	Address-Aligned Beats This bit is read-only bit and reflects the Bit 25 (AAL) of Register 0 (Bus Mode Register). When this bit is set to 1, the GMAC-AXI performs address-aligned burst transfers on both read and write channels. Reset Value: 0
11:8	-	RO	Reserved Reset Value: 0H
7	BLEN256	R_W	AXI Burst Length 256 When this bit is set to 1, the GMAC-AXI is allowed to select a burst length of 256 on the AXI master interface. This bit is present only when the configuration parameter AXI_BL is set to 256. Otherwise, this bit is reserved and is read-only. Reset Value: 0
6	BLEN128	R_W	AXI Burst Length 128 When this bit is set to 1, the GMAC-AXI is allowed to select a burst length of 128 on the AXI master interface. This bit is present only when the configuration parameter AXI_BL is set to 128 or more. Otherwise, this bit is reserved and is read-only. Reset Value: 0

Bits	Name	Access	Description
5	BLEN64	R_W	AXI Burst Length 64 When this bit is set to 1, the GMAC-AXI is allowed to select a burst length of 64 on the AXI master interface. This bit is present only when the configuration parameter AXI_BL is set to 64 or more. Otherwise, this bit is reserved and is read-only. Reset Value: 0
4	BLEN32	R_W	AXI Burst Length 32 When this bit is set to 1, the GMAC-AXI is allowed to select a burst length of 32 on the AXI master interface. This bit is present only when the configuration parameter AXI_BL is set to 32 or more. Otherwise, this bit is reserved and is read-only. Reset Value: 0
3	BLEN16	R_W	AXI Burst Length 16 When this bit is set to 1 or UNDEF is set to 1, the GMAC-AXI is allowed to select a burst length of 16 on the AXI master interface. Reset Value: 0
2	BLEN8	R_W	AXI Burst Length 8 When this bit is set to 1, the GMAC-AXI is allowed to select a burst length of 8 on the AXI master interface. Setting this bit has no effect when UNDEF is set to 1. Reset Value: 0
1	BLEN4	R_W	AXI Burst Length 4 When this bit is set to 1, the GMAC-AXI is allowed to select a burst length of 4 on the AXI master interface. Setting this bit has no effect when UNDEF is set to 1. Reset Value: 0
0	UNDEF	RO	AXI Undefined Burst Length This bit is read-only bit and indicates the complement (invert) value of Bit 16 (FB) in Register 0 (Bus Mode Register). ■ When this bit is set to 1, the GMAC-AXI is allowed to perform any burst length equal to or below the maximum allowed burst length programmed in Bits[7:3]. ■ When this bit is set to 0, the GMAC-AXI is allowed to

Bits	Name	Access	Description
			perform only fixed burst lengths as indicated by BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4, or a burst length of 1. If UNDEF is set and none of the BLEN bits is set, then GMAC-AXI is allowed to perform a burst length of 16. Reset Value: 1

1.6.3.12 Register 11 (AHB or AXI Status Register)

This register provides the active status of the read and write channels of the AHB master interface or AXI interface. This register is present and valid only in the GMAC-AHB and GMAC-AXI configurations. This register is useful for debugging purposes. In addition, this register is valid only in the Channel 0 DMA when multiple channels are present in the AV mode.

Figure & Table 1-28 Register 11 (AHB or AXI Status Register)

Bits	Name	Access	Description
31:2	-	RO	Reserved Reset Value: 0000_0000H
1	AXIRDSTS	RO	AXI Master Read Channel Status When high, it indicates that AXI master's read channel is active and transferring data. Reset Value: 0
0	AXWHSTS	RO	AXI Master Write Channel or AHB Master Status When high, it indicates that AXI master's write channel is active and transferring data in the GMAC-AXI configuration. In the GMAC-AHB configuration, it indicates that the AHB master interface FSMs are in the non-idle state. Reset Value: 0

1.6.3.13 Register 18 (Current Host Transmit Descriptor Register)

The Current Host Transmit Descriptor register points to the start address of the current Transmit Descriptor read by the DMA.

Figure & Table 1-29 Register 18 (Current Host Transmit Descriptor Register)

Bits	Name	Access	Description
31	AE	R_W	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores

Bits	Name	Access	Description
			the address for filtering. Reset Value: 0
30	SA	R_W	Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received frame. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received frame. Reset Value: 0
29:24	MBC	R_W	Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: ■ Bit 29: Register 18[15:8] ■ Bit 28: Register 18[7:0] ■ Bit 27: Register 19[31:24] ■ ... ■ Bit 24: Register 19[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. Reset Value: 000000
23:16	-	RO	Reserved Reset Value: 00H
15:0	ADDRHI	R_W	MAC Address1[47:32] This field contains the upper 16 bits (47:32) of the second 6-byte MAC address. Reset Value: FFFFH

1.6.3.14 Register 19 (Current Host Receive Descriptor Register)

The Current Host Receive Descriptor register points to the start address of the current Receive Descriptor read by the DMA.

Figure & Table 1-30 Register 19 (Current Host Receive Descriptor Register)

Bits	Name	Access	Description
31:0	CURRDESAPTR	RO	Host Receive Descriptor Address Pointer

Bits	Name	Access	Description
			Cleared on Reset. Pointer updated by the DMA during operation. Reset Value: 0000_0000H

1.6.3.15 Register 20 (Current Host Transmit Buffer Address Register)

The Current Host Transmit Buffer Address register points to the current Transmit Buffer Address being read by the DMA.

Figure & Table 1-31 Register 20 (Current Host Transmit Buffer Address Register)

Bits	Name	Access	Description
31:0	CURTBUFAPTR	RO	Host Transmit Buffer Address Pointer Cleared on Reset. Pointer updated by the DMA during operation. Reset Value: 0000_0000H

1.6.3.16 Register 21 (Current Host Receive Buffer Address Register)

The Current Host Receive Buffer Address register points to the current Receive Buffer address being read by the DMA.

Figure & Table 1-32 Register 21 (Current Host Receive Buffer Address Register)

Bits	Name	Access	Description
31:0	CURRBUFAPTR	RO	Host Receive Buffer Address Pointer Cleared on Reset. Pointer updated by the DMA during operation. Reset Value: 0000_0000H

1.6.3.17 Register 22 (HW Feature Register)

This register indicates the presence of the optional features or functions of the DWC_gmac. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Figure & Table 1-33 Register 22 (HW Feature Register)

Bits	Name	Access	Description
31	-	RO	Reserved
30:28	ACTPHYIF	RO	Active or selected PHY interface When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion.

Bits	Name	Access	Description
			■ 000: GMII or MII ■ 001: RGMII ■ 010: SGMII ■ 011: TBI ■ 100: RMII ■ 101: RTBI ■ 110: SMII ■ 11: RevMII ■ All Others: Reserved
27	SAVLANINS	RO	Source Address or VLAN Insertion
26	FLEXIPPSEN	RO	Flexible Pulse-Per-Second Output
25	INTTSEN	RO	Timestamping with Internal System Time
24	ENHDESSEL	RO	Alternate (Enhanced Descriptor)
23:22	TXCHCNT	RO	Number of additional Tx Channels
21:20	RXCHCNT	RO	Number of additional Rx Channels
19	RXFIFOSIZE	RO	Rx FIFO > 2,048 Bytes
18	RXTYP2COE	RO	IP Checksum Offload (Type 2) in Rx
17	RXTYP1COE	RO	IP Checksum Offload (Type 1) in Rx Note: If IPCHKSUM_EN = Enabled and IPC_FULL_OFFLOAD = Enabled, then RXTYP1COE = 0 and RXTYP2COE = 1.
16	TXCOESEL	RO	Checksum Offload in Tx
15	AVSEL	RO	AV feature
14	EEESEL	RO	Energy Efficient Ethernet
13	TSVER2SEL	RO	IEEE 1588-2008 Advanced timestamp
12	TSVER1SEL	RO	Only IEEE 1588-2002 timestamp
11	MMCSEL	RO	RMON module
10	MGKSEL	RO	PMT magic packet
9	RWKSEL	RO	PMT remote wake-up frame
8	SMASEL	RO	SMA (MDIO) Interface
7	L3L4FLTREN	RO	Layer 3 and Layer 4 feature

Bits	Name	Access	Description
6	PCSSEL	RO	PCS registers (TBI, SGMII, or RTBI PHY interface)
5	ADDMACADRSEL	RO	Multiple MAC Address registers
4	HASHSEL	RO	HASH filter
3	EXTHASHEN	RO	Expanded DA Hash filter
2	HDSEL	RO	Half-duplex support
1	GMIISEL	RO	1000Mbps support
0	MIISEL	RO	10 or 100Mbps support

1.6.3.18 Register 76 (Channel 1 Slot Function Control and Status Register)

This register controls the slot comparison feature that the Channel 1 transmit DMA uses to fetch the buffer data from system memory.

Figure & Table 1-34 Register 76 (Channel 1 Slot Function Control and Status Register)

Bits	Name	Access	Description
31:20	-	RO	Reserved Reset Value: 00H
19:16	RSN	RO	Reference Slot Number This field gives the current value of the reference slot number in DMA used for comparison checking. Reset Value: 0H
15:2	-	RO	Reserved Reset Value: 000H
1	ASC	R_W	Advance Slot Check When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the transmit descriptor is: ■ equal to the reference slot number given in Bits [19:16] or ■ ahead of the reference slot number by up to two slots. This bit is applicable only when Bit 0 (ESC) is set. Reset Value: 0

Bits	Name	Access	Description
0	ESC	R_W	Enable Slot Comparison When set, this bit enables the checking of the slot numbers, programmed in the transmit descriptor, with the current reference given in Bits [19:16]. The DMA fetches the data from the corresponding buffer only when the slot number is equal to the reference slot number or is ahead of the reference slot number by one slot. When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Reset Value: 0

1.6.3.19 Register 88 (Channel 1 CBS Control Register)

This register controls the credit-based shaper algorithm in the Traffic Manager for scheduling the frames for transmission. This register is present only when you select the Transmit Channel 1 in the AV mode.

Figure & Table 1-35 Register 88 (Channel 1 CBS Control Register)

Bits	Name	Access	Description
31:18	-	RO	Reserved Reset Value: 00H
17	ABPSSIE	R_W	Average Bits Per Slot Interrupt Enable When this bit is set, the MAC asserts an interrupt (sbd_intr_o or mci_intr_o) when the average bits per slot status is updated (Bit 17 (ABSU) in Register 89) for Channel 1. When this bit is cleared, interrupt is not asserted for such an event. Reset Value: 0
16:7	-	RO	Reserved Reset Value: 00H

Bits	Name	Access	Description
6:4	SLC	R_W	Slot Count The software can program the number of slots (of duration 125 micro-sec) over which the average transmitted bits per slot (provided in the CBS Status register) need to be computed for Channel 1 when the credit-based shaper algorithm is enabled. The encoding is as follows: ■ 3'b000: 1 Slot ■ 3'b001: 2 Slots ■ 3'b010: 4 Slots ■ 3'b011: 8 Slots ■ 3'b100: 16 Slots ■ 3'b101-3'b111: Reserved Reset Value: 00
3:2	-	RO	Reserved Reset Value: 00
1	CC	R_W	Credit Control When reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no frame to transmit in Channel 1. When there is no frame waiting in Channel 1 and other channel is transmitting, no credit is accumulated. When set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no frame to transmit in Channel 1. The credit accumulates even when there is no frame waiting in Channel 1 and another channel is transmitting. Reset Value: 0
0	CBSD	R_W	Credit-Based Shaper Disable When set, the MAC disables the credit-based shaper algorithm for Channel 1 traffic and makes the traffic management algorithm to strict priority for Channel 1 over Channel 0. When reset, the credit-based shaper algorithm schedules the traffic in Channel 1 for transmission. Reset Value: 0

1.6.3.20 Register 89 (Channel 1 CBS Status Register)

This register provides the average traffic transmitted in Channel 1. This register is present only when you select the Transmit Channel 1 in the AV mode.

Figure & Table 1-36 Register 89 (Channel 1 CBS Status Register)

Bits	Name	Access	Description
31:18	-	RO	Reserved Reset Value: 000H
17	ABSU	R_SS_SC	ABS Updated When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application reads the ABS value. Reset Value: 0
16:0	ABS	RO	Average Bits per Slot This field contains the average transmitted bits per slot. This field is computed over programmed number of slots (SLC bits in the CBS Control Register) for Channel 1 traffic. The maximum value is 0x30D4 for 100Mbps and 0x1E848 for 1000Mbps. Reset Value: 000H

1.6.3.21 Register 90 (Channel 1 idleSlopeCredit Register)

This register provides the bandwidth allocated for the AV traffic on Channel 1. This register is present only when you select the Transmit Channel 1 in the AV mode.

Figure & Table 1-37 Register 90 (Channel 1 idleSlopeCredit Register)

Bits	Name	Access	Description
31:14	-	RO	Reserved Reset Value: 000H
13:0	ISC	R_W	idleSlopeCredit This field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Channel 1. This is the rate of change of credit in bits per cycle (40ns and 8ns for 100Mbps and 1000Mbps respectively) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1024. The maximum value is portTransmitRate, that is, 0x2000 in 1000Mbps mode and 0x1000 in 100Mbps mode. Reset Value: 000H

1.6.3.22 Register 91 (Channel 1 sendSlopeCredit Register)

This register provides the bandwidth that is available for the AV traffic on other channels. This register is present only when you select the Transmit Channel 1 in the AV mode.

Figure & Table 1-38 Register 91 (Channel 1 sendSlopeCredit Register) (Continued)

Bits	Name	Access	Description
13:0	SSC	R_W	sendSlopeCredit This field contains the sendSlopeCredit value required for credit-based shaper algorithm for Channel 1. This is the rate of change of credit in bits per cycle (40ns and 8ns for 100Mbps and 1000Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1024. The maximum value is portTransmitRate, that is, 0x2000 in 1000Mbps mode and 0x1000 in 100Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission. Reset Value: 000H

1.6.3.23 Register 92 (Channel 1 hiCredit Register)

This register provides the maximum value that can be accumulated for Channel 1 in the credit parameter of the credit-based shaper algorithm. This register is present only when you select the Transmit Channel 1 in the AV mode.

Figure & Table 1-39 Register 92 (Channel 1 hiCredit Register)

Bits	Name	Access	Description
31:29	-	RO	Reserved Reset Value: 0H
28:0	HC	R_W	hiCredit This field contains the hiCredit value required for the credit-based shaper algorithm for Channel 1. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum frame size which is 16,384 bytes or 131,072 bits. The value to be specified is 131,072*1,024 = 134,217,728 or 0x0800_0000. Reset Value: 0000000H

1.6.3.24 Register 93 (Channel 1 loCredit Register)

This register provides the minimum value that can be accumulated for Channel 1 in the credit parameter of the credit-based shaper algorithm. This register is present only when you select Transmit Channel 1 in the AV mode.

Figure & Table 1-40 Register 93 (Channel 1 loCredit Register)

Bits	Name	Access	Description
31:29	-	RO	Reserved Reset Value: 0x7
28:0	LC	R_W	loCredit This field contains the loCredit value required for the credit-based shaper algorithm for Channel 1. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum frame size which is 16,384 bytes or 131,072 bits. The value to be specified is 131,072*1,024 = 134,217,728 or 0x0800_0000. The programmed value is 2's complement (negative number), that is, 0xF800_0000. Reset Value: 0x1FFF_FFFF

1.6.3.25 Register 0 (MAC Configuration Register)

The MAC Configuration register establishes receive and transmit operating modes.

Figure & Table 1-41 Register 0 (MAC Configuration Register)

Bits	Name	Access	Description
31	-	RO	Reset Value：0
30:28	SARC	R_W	Source Address Insertion or Replacement Control This field controls the source address insertion or replacement for all transmitted frames. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits [29:28]: 2'b0*x*: The input signals mti_sa_ctrl_i and ati_sa_ctrl_i control the SA field generation. 2'b10: - If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers (registers 16 and 17) in the SA field of all transmitted frames. - If Bit 30 is set to 1 and the Enable MAC Address

Bits	Name	Access	Description
			Register 1 option is selected during core configuration, the MAC inserts the content of the MAC Address 1 registers (registers 18 and 19) in the SA field of all transmitted frames. 2'b11: - If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers (registers 16 and 17) in the SA field of all transmitted frames. - If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC replaces the content of the MAC Address 1 registers (registers 18 and 19) in the SA field of all transmitted frames. Changes to this field take effect only on the start of a frame. If you write this register field when a frame is being transmitted, only the subsequent frame can use the updated value, that is, the current frame does not use the updated value. These bits are reserved and RO when the Enable SA, VLAN, and CRC Insertion on TX feature is not selected during core configuration. Reset Value：0
27	TWOKPE	R_W	IEEE 802.3as Support for 2K Packets When set, the MAC considers all frames, with up to 2,000 bytes length, as normal packets. When Bit 20 (JE) is not set, the MAC considers all received frames of size more than 2K bytes as Giant frames. When this bit is reset and Bit 20 (JE) is not set, the MAC considers all received frames of size more than 1,518 bytes (1,522 bytes for tagged) as Giant frames. When Bit 20 is set, setting this bit has no effect on Giant Frame status. For more information about how the setting of this bit and Bit 20 impact the Giant frame status, see Figure & Table 1-42. Reset Value：00
26	SFTERR	R_W	SMII Force Transmit Error When set, this bit indicates to the PHY to force a transmit error in the SMII frame being transmitted. This bit is reserved if the SMII PHY port is not selected during core configuration.

Bits	Name	Access	Description
			Reset Value：0
25	CST	R_W	CRC Stripping for Type Frames When this bit is set, the last 4 bytes (FCS) of all frames of Ethernet type (Length/Type field greater than or equal to 1,536) are stripped and dropped before forwarding the frame to the application. This function is not valid when the IP Checksum Engine (Type 1) is enabled in the MAC receiver. This function is valid when Type 2 Checksum Offload Engine is enabled. Note: For information about how the settings of Bit 7 (ACS) and this bit impact the frame length, see Table 6-32. Reset Value：0
24	TC	R_W	Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. This bit is reserved (and RO) if the RGMII, SMII, or SGMII PHY port is not selected during core configuration. The details of this feature are explained in the following sections: ■ “Reduced Gigabit Media Independent Interface” ■ “Serial Media Independent Interface” ■ “Serial Gigabit Media Independent Interface” Reset Value：0
23	WD	R_W	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive frames of up to 16,383 bytes. When this bit is reset, the MAC does not allow a receive frame which more than 2,048 bytes (10,240 if JE is set high) or the value programmed in Register 55 (Watchdog Timeout Register). The MAC cuts off any bytes received after the watchdog limit number of bytes. Reset Value：0
22	JD	R_W	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer frames of up

Bits	Name	Access	Description
			to 16,383 bytes. When this bit is reset, the MAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission. Reset Value：0
21	BE	R_W	Frame Burst Enable When this bit is set, the MAC allows frame bursting during transmission in the GMII half-duplex mode. This bit is reserved (and RO) in the 10/100Mbps only or full-duplex-only configurations. Reset Value：0
20	JE	R_W	Jumbo Frame Enable When this bit is set, the MAC allows Jumbo frames of 9,018 bytes (9,022 bytes for VLAN tagged frames) without reporting a giant frame error in the receive frame status. Reset Value：0
19:17	IFG	R_W	Inter-Frame Gap These bits control the minimum IFG between frames during transmission. ■ 000: 96 bit times ■ 001: 88 bit times ■ 010: 80 bit times ■ ... ■ 111: 40 bit times In the half-duplex mode, the minimum IFG can be configured only for 64 bit times (IFG = 100). Lower values are not considered. In the 1000Mbps mode, the minimum IFG supported is 64 bit times (and above) in the GMAC-CORE configuration and 80 bit times (and above) in other configurations. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IFG. Reset Value：000
16	DCRS	R_W	Disable Carrier Sense During Transmission When set high, this bit makes the MAC transmitter ignore the (G)MII CRS signal during frame transmission in the half-duplex mode. This request results in no

Bits	Name	Access	Description
			errors generated because of Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC transmitter generates such errors because of Carrier Sense and can even abort the transmissions. This bit is reserved (and RO) in the full-duplex-only configurations. Reset Value：0
15	PS	R_W	Port Select This bit selects the Ethernet line speed. ■ 0: For 1000Mbps operations ■ 1: For 10 or 100Mbps operations In 10 or 100Mbps operations, this bit, along with FES bit, selects the exact line speed. In the 10/100Mbps-only (always 1) or 1000Mbps-only (always 0) configurations, this bit is read-only with the appropriate value. In default 10/100/1000Mbps configuration, this bit is R_W. The mac_portselect_o or mac_speed_o[1] signal reflects the value of this bit. Reset Value：0
14	FES	R_W	Speed This bit selects the speed in the MII, RMII, SMII, RGMII, SGMII, or RevMII interface: ■ 0: 10Mbps ■ 1: 100Mbps This bit is reserved (RO) by default and is enabled only when the parameter SPEED_SELECT = Enabled. This bit generates link speed encoding when Bit 24 (TC) is set in the RGMII, SMII, or SGMII mode. This bit is always enabled for RGMII, SGMII, SMII, or RevMII interface. In configurations with RGMII, SGMII, SMII, or RevMII interface, this bit is driven as an output signal (mac_speed_o[0]) to reflect the value of this bit in the mac_speed_o signal. In configurations with RMII, MII, or GMII interface, you can optionally drive this bit as an output signal (mac_speed_o[0]) to reflect its value in the mac_speed_o signal. Reset Value：0
13	DO	R_W	Disable Receive Own When this bit is set, the MAC disables the reception of frames when the phy_txen_o is asserted in the half-

Bits	Name	Access	Description
			duplex mode. When this bit is reset, the MAC receives all packets that are given by the PHY while transmitting. This bit is not applicable if the MAC is operating in the full-duplex mode. This bit is reserved (RO with default value) if the MAC is configured for the full-duplex-only operation. Reset Value：0
12	LM	R_W	Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Receive clock input (clk_rx_i) is required for the loopback to work properly, because the Transmit clock is not looped-back internally. Reset Value：0
11	DM	R_W	Duplex Mode When this bit is set, the MAC operates in the full-duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configuration. Reset Value：0
10	IPC	R_W	Checksum Offload When this bit is set, the MAC calculates the 16-bit one’s complement of the one’s complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25-26 or 29-30 (VLANtagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The MAC also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits (see Table 3-10 on page 138) are always cleared. If the IP Checksum Offload feature is not enabled

Bits	Name	Access	Description
			during core configuration, this bit is reserved (RO with default value). Reset Value：0
9	DR	R_W	Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current frame transmission and reports a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the MAC attempts retries based on the settings of the BL field (Bits [6:5]). This bit is applicable only in the half-duplex mode and is reserved (RO with default value) in the full-duplex-only configuration. Reset Value：0
8	LUD	R_W	Link Up or Down This bit indicates whether the link is up or down during the transmission of configuration in the RGMII, SGMII, or SMII interface: ■ 0: Link Down ■ 1: Link Up This bit is reserved (RO with default value) and is enabled when the RGMII, SGMII, or SMII interface is enabled during core configuration. Reset Value：0
7	ACS	R_W	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming frames only if the value of the length field is less than 1,536 bytes. All received frames with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming frames, without modifying them, to the Host. Note: For information about how the settings of Bit 25 (CST) and this bit impact the frame length, see Table 6-32. Reset Value：0
6:5	BL	R_W	Back-Off Limit The Back-Off limit determines the random integer

Bits	Name	Access	Description
			number (r) of slot time delays (4,096 bit times for 1000Mbps and 512 bit times for 10/100Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration. ■ 00: k= min (*n*, 10) ■ 01: k = min (*n*, 8) ■ 10: k = min (*n*, 4) ■ 11: k = min (*n*, 1) where *n* = retransmission attempt. The random integer *r* takes the value in the range $0 \le r < 2^k$. Reset Value：00
4	DC	R_W	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status, when the transmit state machine is deferred for more than 24,288 bit times in the 10 or 100Mbps mode. If the MAC is configured for 1000Mbps operation or if the Jumbo frame mode is enabled in the 10 or 100Mbps mode, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and then the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0 and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration. Reset Value：0
3	TE	R_W	Transmitter Enable

Bits	Name	Access	Description
			When this bit is set, the transmit state machine of the MAC is enabled for transmission on the GMII or MII. When this bit is reset, the MAC transmit state machine is disabled after the completion of the transmission of the current frame, and does not transmit any further frames. Reset Value：0
2	RE	R_W	Receiver Enable When this bit is set, the receiver state machine of the MAC is enabled for receiving frames from the GMII or MII. When this bit is reset, the MAC receive state machine is disabled after the completion of the reception of the current frame, and does not receive any further frames from the GMII or MII. Reset Value：0
1:0	PRELEN	R_W	Preamble Length for Transmit frames These bits control the number of preamble bytes that are added to the beginning of every Transmit frame. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. ■ 2'b00: 7 bytes of preamble ■ 2'b01: 5 bytes of preamble ■ 2'b10: 3 bytes of preamble ■ 2'b11: Reserved Reset Value: 00

Figure & Table 1-42 shows how the settings of Bit 27 and Bit 20 of Register 0 (MAC Configuration Register) impact the giant frame status.

Figure & Table 1-42 Giant frame status based on bit 27 and bit 20

Length/Type Field	Received Frame Length	Bit 27 (TWOKPE)	Bit 20 (JE)	Giant Frame Status
Untagged packet	> 1,518	0	0	1
	> 2,000	1	0	1
	> 9,018	x	1	1
VLAN tagged packet	> 1,522	0	0	1
	> 2,000	1	0	1
	> 9,022	x	1	1

Length/Type Field	Received Frame Length	Bit 27 (TWOKPE)	Bit 20 (JE)	Giant Frame Status
Note: For all other combinations, the Giant Frame status is 0.				

Table 6-32 shows how the settings of Bit 7 and Bit 25 of Register 0 (MAC Configuration Register) impact whether CRC length is included in the frame length.

1.6.3.26 Register 1 (MAC Frame Filter)

The MAC Frame Filter register contains the filter controls for receiving frames. Some of the controls from this register go to the address check block of the MAC, which performs the first level of address filtering. The second level of filtering is performed on the incoming frame, based on other controls such as Pass Bad Frames and Pass Control Frames.

Figure & Table 1-43 Register 1(MAC Frame Filter)

Bits	Name	Access	Description
31	RA	R_W	Receive All When this bit is set, the MAC Receiver module passes all received frames, irrespective of whether they pass the address filter or not, to the Application. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes only those frames to the Application that pass the SA or DA address filter. Reset Value: 0
30:22	-	RO	Reserved Reset Value: 00H
21	DNTU	R_W	Drop non-TCP/UDP over IP Frames When set, this bit enables the MAC to drop the non-TCP or UDP over IP frames. The MAC forward only those frames that are processed by the Layer 4 filter. When reset, this bit enables the MAC to forward all non-TCP or UDP over IP frames. If the Layer 3 and Layer 4 Filtering feature is not selected during core configuration, this bit is reserved (RO with default value). Reset Value: 0

Bits	Name	Access	Description
20	IPFE	R_W	Layer 3 and Layer 4 Filter Enable When set, this bit enables the MAC to drop frames that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When reset, the MAC forwards all frames irrespective of the match status of the Layer 3 and Layer 4 fields. If the Layer 3 and Layer 4 Filtering feature is not selected during core configuration, this bit is reserved (RO with default value). Reset Value: 0
19:17	-	RO	Reserved Reset Value: 000
16	VTFE	R_W	VLAN Tag Filter Enable When set, this bit enables the MAC to drop VLAN tagged frames that do not match the VLAN Tag comparison. When reset, the MAC forwards all frames irrespective of the match status of the VLAN Tag. Reset Value: 0
15:11	-	R_W	Reserved Reset Value: 00
10	HPF	R_W	Hash or Perfect Filter When this bit is set, it configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by the HMC or HUC bits. When this bit is low and the HUC or HMC bit is set, the frame is passed only if it matches the Hash filter. This bit is reserved (and RO) if the Hash filter is not selected during core configuration. Reset Value: 0
9	SAF	R_W	Source Address Filter Enable When this bit is set, the MAC compares the SA field of the received frames with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the frame. When this bit is reset, the MAC forwards the received frame to the application with updated SAF bit of the Rx Status depending on the SA address comparison.

Bits	Name	Access	Description
			Note: According to the IEEE specification, Bit 47 of the SA is reserved and set to 0. However, in DWC_gmac, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA. Reset Value: 0
8	SAIF	R_W	SA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers are marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers are marked as failing the SA Address filter. Reset Value: 0
7:6	PCF	R_W	Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast Pause frames). ■ 00: MAC filters all control frames from reaching the application. ■ 01: MAC forwards all control frames except Pause frames to application even if they fail the Address filter. ■ 10: MAC forwards all control frames to application even if they fail the Address Filter. ■ 11: MAC forwards control frames that pass the Address Filter. The following conditions should be true for the Pause frames processing: ■ Condition 1: The MAC is in the full-duplex mode and flow control is enabled by setting Bit 2 (RFE) of Register 6 (Flow Control Register) to 1. ■ Condition 2: The destination address (DA) of the received frame matches the special multicast address or the MAC Address 0 when Bit 3 (UP) of the Register 6 (Flow Control Register) is set. ■ Condition 3: The Type field of the received frame is 0x8808 and the OPCODE field is 0x0001. Note: This field should be set to 01 only when the Condition 1 is true, that is, the MAC is programmed to

Bits	Name	Access	Description
			operate in the full-duplex mode and the RFE bit is enabled. Otherwise, the Pause frame filtering may be inconsistent. When Condition 1 is false, the Pause frames are considered as generic control frames. Therefore, to pass all control frames (including Pause frames) when the full-duplex mode and flow control is not enabled, you should set the PCF field to 10 or 11 (as required by the application). Reset Value: 00
5	DBF	R_W	Disable Broadcast Frames When this bit is set, the AFM module blocks all incoming broadcast frames. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast frames. Reset Value: 0
4	PM	R_W	Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address field is '1') are passed. When reset, filtering of multicast frame depends on HMC bit. Reset Value: 0
3	DAIF	R_W	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed. Reset Value: 0
2	HMC	R_W	Hash Multicast When set, the MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA field with the values programmed in DA registers. If Hash Filter is not selected during core configuration, this bit is reserved (and RO).

Bits	Name	Access	Description
			Reset Value: 0
1	HUC	R_W	Hash Unicast When set, the MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA field with the values programmed in DA registers. If Hash Filter is not selected during core configuration, this bit is reserved (and RO). Reset Value: 0
0	PR	R_W	Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frames irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Receive Status Word are always cleared when PR is set. Reset Value: 0

1.6.3.27 Register 2 (Hash Table High Register)

The 64-bit Hash table is used for group address filtering. For hash filtering, the contents of the destination address in the incoming frame is passed through the CRC logic, and the upper 6 bits of the CRC register are used to index the contents of the Hash table. The most significant bit determines the register to be used (Hash Table High or Hash Table Low), and the other 5 bits determine which bit within the register. A hash value of 5b'00000 selects Bit 0 of the selected register, and a value of 5b'11111 selects Bit 31 of the selected register.

The hash value of the destination address is calculated in the following way:

1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).
2. Perform bitwise reversal for the value obtained in Step 1.
3. Take the upper 6 bits from the value obtained in Step 2.

For example, if the DA of the incoming frame is received as 0x1F52419CB6AF (0x1F is the first byte received on GMII interface), then the internally calculated 6-bit Hash value is 0x2C and Bit 12 of Hash Table High register is checked for filtering. If the DA of the incoming frame is received as 0xA00A98000045, then the calculated 6-bit Hash value is 0x07 and Bit 7 of Hash Table Low register is checked for filtering.

NOTE

To help you program the hash table, a sample C routine that generates a DA's 6-bit hash is included in the /sample_codes/ directory of your workspace.

If the corresponding bit value of the register is 1’b1, the frame is accepted. Otherwise, it is rejected. If the PM (Pass All Multicast) bit is set in Register 1, then all multicast frames are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table High or Low registers are written. Consecutive writes to these register should be performed only after at least 4 clock cycles in the destination clock domain when double-synchronization is enabled.

The Hash Table High register contains the upper 32 bits of the Hash table.

Figure & Table 1-44 Register 2 (Hash Table High Register)

Bits	Name	Access	Description
31:0	HTH	R_W	Hash Table High This field contains the upper 32 bits of the Hash table. Reset Value: 0000_0000H

1.6.3.28 Register 3 (Hash Table Low Register)

The Hash Table Low register contains the lower 32 bits of the Hash table. Both Register 2 and Register 3 are reserved if the Hash Filter Function is disabled or the 128-bit or 256-bit Hash Table is selected during core configuration.

Figure & Table 1-45 Register 3 (Hash Table Low Register)

Bits	Name	Access	Description
31:0	HTL	R_W	Hash Table Low This field contains the lower 32 bits of the Hash table. Reset Value: 0000_0000H

1.6.3.29 Register 4 (GMII Address Register)

The GMII Address register controls the management cycles to the external PHY through the management interface.

Figure & Table 1-46 Register 4 (GMII Address Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15:11	PA	R_W	Physical Layer Address This field indicates which of the 32 possible PHY devices are being accessed. For RevMII, this field gives the PHY Address of the RevMII module.

Bits	Name	Access	Description
			Reset Value: 00H
10:6	GR	R_W	GMII Register These bits select the desired GMII register in the selected PHY device. For RevMII, these bits select the desired CSR register in the RevMII Registers set. Reset Value: 00H
5:2	CR	R_W	CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design. The CSR clock corresponding to different GMAC configurations is given in Table 9-2 on page 564. The suggested range of CSR clock frequency applicable for each value (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range 1.0MHz-2.5MHz. ■ 0000: The CSR clock frequency is 60-100MHz and the MDC clock frequency is CSR clock/42. ■ 0001: The CSR clock frequency is 100-150MHz and the MDC clock frequency is CSR clock/62. ■ 0010: The CSR clock frequency is 20-35MHz and the MDC clock frequency is CSR clock/16. ■ 0011: The CSR clock frequency is 35-60MHz and the MDC clock frequency is CSR clock/26. ■ 0100: The CSR clock frequency is 150-250MHz and the MDC clock frequency is CSR clock/102. ■ 0101: The CSR clock frequency is 250-300MHz and the MDC clock is CSR clock/124. ■ 0110, 0111: Reserved When Bit 5 is set, you can achieve higher frequency of the MDC clock than the frequency limit of 2.5MHz (specified in the IEEE Std 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100MHz frequency and you program these bits as 1010, then the resultant MDC clock is of 12.5MHz which is outside the limit of IEEE 802.3 specified range. Program the following values only if the interfacing chips support faster MDC clocks. ■ 1000: CSR clock/4

Bits	Name	Access	Description
			■ 1001: CSR clock/6 ■ 1010: CSR clock/8 ■ 1011: CSR clock/10 ■ 1100: CSR clock/12 ■ 1101: CSR clock/14 ■ 1110: CSR clock/16 ■ 1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface. Reset Value: 0000
1	GW	R_W	GMII Write When set, this bit indicates to the PHY or RevMII that this is a Write operation using the GMII Data register. If this bit is not set, it indicates that this is a Read operation, that is, placing the data in the GMII Data register. Reset Value: 0
0	GB	R_WS_ SC	GMII Busy This bit should read logic 0 before writing to Register 4 and Register 5. During a PHY or RevMII register access, the software sets this bit to 1’b1 to indicate that a Read or Write access is in progress. Register 5 is invalid until this bit is cleared by the MAC. Therefore, Register 5 (GMII Data) should be kept valid until the MAC clears this bit during a PHY Write operation. Similarly for a read operation, the contents of Register 5 are not valid until this bit is cleared. The subsequent read or write operation should happen only after the previous operation is complete. Because there is no acknowledgment from the PHY to MAC after a read or write operation is completed, there is no change in the functionality of this bit even when the PHY is not present. Reset Value: 0

1.6.3.30 Register 5 (GMII Data Register)

The GMII Data register stores Write data to be written to the PHY register located at the address specified in Register 4 (GMII Address Register). This register also stores the Read data from the PHY register located at the address specified by Register 4.

Figure & Table 1-47 Register 5 (GMII Data Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15:0	GD	R_W	GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation. Reset Value: 0000H

1.6.3.31 Register 6 (Flow Control Register)

The Flow Control register controls the generation and reception of the Control (Pause Command) frames by the MAC's Flow control module. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause frame. The fields of the control frame are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control frame. The Busy bit remains set until the control frame is transferred onto the cable. The Host must make sure that the Busy bit is cleared before writing to the register.

Figure & Table 1-48 Register 6 (Flow Control Register)

Bits	Name	Access	Description
31:16	PT	R_W	Pause Time This field holds the value to be used in the Pause Time field in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain. Reset Value: 0000H
15:8	-	RO	Reserved Reset Value: 00H
7	DZPQ	R_W	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the Zero-Quanta Pause frames on the de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i/mti_flowctrl_i). When this bit is reset, normal operation with automatic Zero-Quanta Pause frame generation is enabled.

Bits	Name	Access	Description
			Reset Value: 0
6	-	RO	Reserved Reset Value: 0
5:4	PLT	R_W	Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second Pause frame is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256 – 28) slot times after the first Pause frame is transmitted. The following list provides the threshold values for different values: ■ 00: The threshold is Pause time minus 4 slot times (PT - 4 slot times). ■ 01: The threshold is Pause time minus 28 slot times (PT - 28 slot times). ■ 10: The threshold is Pause time minus 144 slot times (PT - 144 slot times). ■ 11: The threshold is Pause time minus 256 slot times (PT - 256 slot times). The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. Reset Value: 00
3	UP	R_W	Unicast Pause Frame Detect A pause frame is processed when it has the unique multicast address specified in the IEEE Std 802.3. When this bit is set, the MAC can also detect Pause frames with unicast address of the station. This unicast address should be as specified in the MAC Address0 High Register and MAC Address0 Low Register. When this bit is reset, the MAC only detects Pause frames with unique multicast address. Note: The MAC does not process a Pause frame if the multicast address of received frame is different from the unique multicast address. Reset Value: 0

Bits	Name	Access	Description
2	RFE	R_W	Receive Flow Control Enable When this bit is set, the MAC decodes the received Pause frame and disables its transmitter for a specified (Pause) time. When this bit is reset, the decode function of the Pause frame is disabled. Reset Value: 0
1	TFE	R_W	Transmit Flow Control Enable In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause frames. In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. Reset Value: 0
0	FCB_ BPA	R_WS_SC for FCB R_W for BPA	Flow Control Busy or Backpressure Activate This bit initiates a Pause frame in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. In the full-duplex mode, this bit should be read as 1'b0 before writing to the Flow Control register. To initiate a Pause frame, the Application must set this bit to 1'b1. During a transfer of the Control Frame, this bit continues to be set to signify that a frame transmission is in progress. After the completion of Pause frame transmission, the MAC resets this bit to 1'b0. The Flow Control register should not be written to until this bit is cleared. In the half-duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the MAC. During backpressure, when the MAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Reset Value: 0

1.6.3.32 Register 7 (VLAN Tag Register)

The VLAN Tag register contains the IEEE 802.1Q VLAN Tag to identify the VLAN frames. The MAC compares the 13th and 14th bytes of the receiving frame (Length/Type) with 16’h8100, and the following two bytes are compared with the VLAN tag. If a match occurs, the MAC sets the received VLAN bit in the receive frame status. The legal length of the frame is increased from 1,518 bytes to 1,522 bytes.

If the VLAN Tag register is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to these register should be performed only after at least four clock cycles in the destination clock domain.

Figure & Table 1-49 Register 7 (VLAN Tag Register)

Bits	Name	Access	Description
31:20	-	RO	Reserved Reset Value: 000H
19	VTHM	R_W	VLAN Tag Hash Table Match Enable When set, the most significant four bits of the VLAN tag's CRC are used to index the content of Register 354 (VLAN Hash Table Register). A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the frame matched the VLAN hash table. When Bit 16 (ETV) is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison whereas when ETV is reset, the CRC of the 16-bit VLAN tag is used for comparison. When reset, the VLAN Hash Match operation is not performed. If the VLAN Hash feature is not enabled during core configuration, this bit is reserved (RO with default value). Reset Value: 0
18	ESVL	R_W	Enable S-VLAN When this bit is set, the MAC transmitter and receiver also consider the S-VLAN (Type = 0x88A8) frames as valid VLAN tagged frames. Reset Value: 0
17	VTIM	R_W	VLAN Tag Inverse Match Enable When set, this bit enables the VLAN Tag inverse matching. The frames that do not have matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The frames with matched VLAN Tag are marked as matched. Reset Value: 0
16	ETV	R_W	Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for

Bits	Name	Access	Description
			comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged frame. Similarly, when enabled, only 12 bits of the VLAN tag in the received frame are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN frame are used for comparison and VLAN hash filtering. Reset Value: 0
15:0	VL	R_W	VLAN Tag Identifier for Receive Frames This field contains the 802.1Q VLAN tag to identify the VLAN frames and is compared to the 15th and 16th bytes of the frames being received for VLAN frames. The following list describes the bits of this field: ■ Bits [15:13]: User Priority ■ Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) ■ Bits[11:0]: VLAN tag's VLAN Identifier (VID) field When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the MAC does not check the fifteenth and 16th bytes for VLAN tag comparison, and declares all frames with a Type field value of 0x8100 or 0x88a8 as VLAN frames. Reset Value: 0000H

1.6.3.33 Register 8 (Version Register)

The Version registers identifies the version of the DWC_gmac. This register contains two bytes: one that Synopsys uses to identify the core release number, and the other that you set during core configuration.

Figure & Table 1-50 Register 8 (Version Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15:8	USERVER	RO	User-defined version (configured with coreConsultant) Reset Value: xxH
7:0	SNPSVER	RO	Synopsys-defined Version (3.7)

Bits	Name	Access	Description
			Reset Value: 37H

1.6.3.34 Register 9 (Debug Register)

The Debug register gives the status of all main modules of the transmit and receive data-paths and the FIFOs. An all-zero status indicates that the MAC is in idle state (and FIFOs are empty) and no activity is going on in the data-paths.

NOTE

The reset values given for the Debug register are valid only if the following clocks are present during reset operation:

- clk_csr_i, clk_app_i, hclk_i, or aclk_i
- clk_tx_i
- clk_rx_i

Figure & Table 1-51 Register 9 (Debug Register)

Bits	Name	Access	Description
31:26	-	RO	Reserved Reset Value: 00H
25	TXSTSFSTS	RO	MTL TxStatus FIFO Full Status When high, this bit indicates that the MTL TxStatus FIFO is full. Therefore, the MTL cannot accept any more frames for transmission. This bit is reserved in the GMAC-AHB and GMAC-DMA configurations. Reset Value: 0
24	TXFSTS	RO	MTL Tx FIFO Not Empty Status When high, this bit indicates that the MTL Tx FIFO is not empty and some data is left for transmission. Reset Value: 0
23	-	RO	Reserved Reset Value: 0
22	TWCSTS	RO	MTL Tx FIFO Write Controller Status When high, this bit indicates that the MTL Tx FIFO Write Controller is active and is transferring data to the Tx FIFO. Reset Value: 0

Bits	Name	Access	Description
21:20	TRCSTS	RO	MTL Tx FIFO Read Controller Status This field indicates the state of the Tx FIFO Read Controller: ■ 00: IDLE state ■ 01: READ state (transferring data to the MAC transmitter) ■ 10: Waiting for TxStatus from the MAC transmitter ■ 11: Writing the received TxStatus or flushing the Tx FIFO Reset Value: 00
19	TXPAUSED	RO	MAC Transmitter in Pause When high, this bit indicates that the MAC transmitter is in the Pause condition (in the full-duplex-only mode) and hence does not schedule any frame for transmission. Reset Value: 0
18:17	TFCSTS	RO	MAC Transmit Frame Controller Status This field indicates the state of the MAC Transmit Frame Controller module: ■ 00: IDLE state ■ 01: Waiting for status of previous frame or IFG or backoff period to be over ■ 10: Generating and transmitting a Pause frame (in the full-duplex mode) ■ 11: Transferring input frame for transmission Reset Value: 00
16	TPESTS	RO	MAC GMII or MII Transmit Protocol Engine Status When high, this bit indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data and is not in the IDLE state. Reset Value: 0
15:10	-	RO	Reserved Reset Value: 0H

Bits	Name	Access	Description
9:8	RXFSTS	RO	MTL RxFIFO Fill-Level Status This field gives the status of the fill-level of the Rx FIFO: ■ 00: Rx FIFO Empty ■ 01: Rx FIFO fill-level below flow-control deactivate threshold ■ 10: Rx FIFO fill-level above flow-control activate threshold ■ 11: Rx FIFO Full Reset Value: 00
7	-	RO	Reserved Reset Value: 0
6:5	RRCSTS	RO	MTL RxFIFO Read Controller State This field gives the state of the Rx FIFO read Controller: ■ 00: IDLE state ■ 01: Reading frame data ■ 10: Reading frame status (or timestamp) ■ 11: Flushing the frame data and status Reset Value: 00
4	RWCSTS	RO	MTL Rx FIFO Write Controller Active Status When high, this bit indicates that the MTL Rx FIFO Write Controller is active and is transferring a received frame to the FIFO. Reset Value: 0
3	-	RO	Reserved Reset Value: 0
2:1	RFCFCSTS	RO	MAC Receive Frame FIFO Controller Status When high, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Frame Controller Module. ■ RFCFCSTS[1] represents the status of small FIFO Read controller. ■ RFCFCSTS[0] represents the status of small FIFO Write controller. Reset Value: 00

Bits	Name	Access	Description
0	RPESTS	RO	MAC GMII or MII Receive Protocol Engine Status When high, this bit indicates that the MAC GMII or MII receive protocol engine is actively receiving data and not in IDLE state. Reset Value: 0

1.6.3.35 Register 12 (LPI Control and Status Register)

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read. This register is present only when you select the Energy Efficient Ethernet feature during core configuration.

Figure & Table 1-52 Register 12 (LPI Control and Status Register)

Bits	Name	Access	Description
31:20	-	RO	Reserved Reset Value: 00000H
19	LPITXA	R_W	LPI TX Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the transmit side. This bit is not functional in the GMACCORE configuration in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding frames (in the core) and pending frames (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any frame for transmission or the application issues a TX FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If TX FIFO Flush is set in Bit 20 of Register 6 (Operation Mode Register), when the MAC is in the LPI mode, the MAC exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. Reset Value: 0
18	PLSEN	R_W	PHY Link Status Enable This bit enables the link status received on the RGMII, SGMII, or SMII receive paths to be used for activating the LPI LS TIMER.

Bits	Name	Access	Description
			When set, the MAC uses the link-status bits of Register 54 (SGMII/RGMII/SMII Control and Status Register) and Bit 17 (PLS) for the LPI LS Timer trigger. When cleared, the MAC ignores the link-status bits of Register 54 and takes only the PLS bit. This bit is RO and reserved if you have not selected the RGMII, SGMII, or SMII PHY interface. Reset Value: 0
17	PLS	R_W	PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (okay) at least for the time indicated by the LPI LS TIMER. When set, the link is considered to be okay (up) and when reset, the link is considered to be down. Reset Value: 0
16	LPIEN	R_W_SC	LPI Enable When set, this bit instructs the MAC Transmitter to enter the LPI state. When reset, this bit instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. Reset Value: 0
15:10	-	RO	Reserved Reset Value: 00H
9	RLPIST	RO	Receive LPI State When set, this bit indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. Reset Value: 0
8	TLPIST	RO	Transmit LPI State When set, this bit indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. Reset Value: 0
7:4	-	RO	Reserved Reset Value: 0H

Bits	Name	Access	Description
3	RLPIEX	R_SS_RC	Receive LPI Exit When set, this bit indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register. Note: This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of CSR clock. Reset Value: 0
2	RLPIEN	R_SS_RC	Receive LPI Entry When set, this bit indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register. Note: This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of CSR clock. Reset Value: 0
1	TLPIEX	R_SS_RC	Transmit LPI Exit When set, this bit indicates that the MAC transmitter has exited the LPI state after the user has cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register. Reset Value: 0
0	TLPIEN	R_SS_RC	Transmit LPI Entry When set, this bit indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register. Reset Value: 0

1.6.3.36 Register 13 (LPI Timers Control Register)

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission. This register is present only when you select the Energy Efficient Ethernet feature during core configuration.

Figure & Table 1-53 Register 13 (LPI Timers Control Register)

Bits	Name	Access	Description
31:26	-	RO	Reserved

Bits	Name	Access	Description
			Reset Value: 00H
25:16	LST	R_W	LPI LS TIMER This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard. Reset Value: 0x3E8
15:0	TWT	R_W	LPI TW TIMER This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer. Reset Value: 0

1.6.3.37 Register 14 (Interrupt Status Register)

The Interrupt Status register identifies the events in the MAC that can generate interrupt. All interrupt events are generated only when the corresponding optional feature is selected during core configuration and enabled during operation. Therefore, these bits are reserved when the corresponding features are not present in the core.

Figure & Table 1-54 Register 14 (Interrupt Status Register)

Bits	Name	Access	Description
31:12	-	RO	Reserved Reset Value: 000000H
11	GPIIS	RO	GPI Interrupt Status When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field (Bits [3:0]) of Register 56 (General Purpose IO Register) and the corresponding GPIE bit is enabled. This bit is cleared on reading lane 0 (GPIS) of Register 56 (General Purpose IO Register). When the GPIO feature is not enabled, this bit is reserved. Reset Value: 0
10	LPIIS	RO	LPI Interrupt Status

Bits	Name	Access	Description
			When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared on reading Bit 0 of Register 12 (LPI Control and Status Register). In all other modes, this bit is reserved. Reset Value: 0
9	TSIS	RO/ R_SS_RC	Timestamp Interrupt Status When the Advanced Timestamp feature is enabled, this bit is set when any of the following conditions is true: ■ The system time value equals or exceeds the value specified in the Target Time High and Low registers. ■ There is an overflow in the seconds register. ■ The Auxiliary snapshot trigger is asserted. This bit is cleared on reading Bit 0 of Register 458 (Timestamp Status Register). If default Timestamping is enabled, when set, this bit indicates that the system time value is equal to or exceeds the value specified in the Target Time registers. In this mode, this bit is cleared after the completion of the read of this bit. In all other modes, this bit is reserved. Reset Value: 0
8	-	RO	Reserved Reset Value: 000H
7	MMCRXIPIS	RO	MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is valid only when you select the optional MMC module and Checksum Offload Engine (Type 2) during core configuration. Reset Value: 0
6	MMCTXIS	RO	MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is valid only when you select the optional MMC module during core configuration.

Bits	Name	Access	Description
			Reset Value: 0
5	MMCRXIS	RO	MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is valid only when you select the optional MMC module during core configuration. Reset Value: 0
4	MMCIS	RO	MMC Interrupt Status This bit is set high when any of the Bits [7:5] is set high and cleared only when all of these bits are low. This bit is valid only when you select the optional MMC module during core configuration. Reset Value: 0
3	PMTIS	RO	PMT Interrupt Status This bit is set when a magic packet or remote wake-up frame is received in the power-down mode (see Bits 5 and 6 in the PMT Control and Status Register). This bit is cleared when both Bits[6:5] are cleared because of a read operation to the PMT Control and Status register. This bit is valid only when you select the optional PMT module during core configuration. Reset Value: 0
2	PCSANCIS	RO	PCS Auto-Negotiation Complete This bit is set when the Auto-negotiation is completed in the TBI, RTBI, or SGMII PHY interface (Bit 5 in Register 49 (AN Status Register)). This bit is cleared when you perform a read operation to the AN Status register. This bit is valid only when you select the optional TBI, RTBI, or SGMII PHY interface during core configuration and operation. Reset Value: 0
1	PCSLCHGIS	RO	PCS Link Status Changed This bit is set because of any change in Link Status in the TBI, RTBI, or SGMII PHY interface (Bit 2 in Register 49 (AN Status Register)). This bit is cleared when you perform a read operation on the AN Status register. This bit is valid only when you select the optional TBI, RTBI, or SGMII PHY interface during core configuration

Bits	Name	Access	Description
			and operation. Reset Value: 0
0	RGSMIIIS	RO	RGMII or SMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII or SMII interface (Bit 3 in Register 54 (SGMII/RGMII/SMII Control and Status Register)). This bit is cleared when you perform a read operation on the SGMII/RGMII/SMII Control and Status Register. This bit is valid only when you select the optional RGMII or SMII PHY interface during core configuration and operation. Reset Value: 0

1.6.3.38 Register 15 (Interrupt Mask Register)

The Interrupt Mask Register bits enable you to mask the interrupt signal because of the corresponding event in the Interrupt Status Register. The interrupt signal is sbd_intr_o in the GMAC-AHB, GMAC-AXI, and GMAC-DMA configuration and mci_intr_o in the GMAC-MTL and GMAC-CORE configuration.

Figure & Table 1-55 Register 15 (Interrupt Mask Register)

Bits	Name	Access	Description
31:11	-	RO	Reserved Reset Value: 00000H
10	LPIIM	R_W	LPI Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the LPI Interrupt Status bit in Register 14 (Interrupt Status Register). This bit is valid only when you select the Energy Efficient Ethernet feature during core configuration. In all other modes, this bit is reserved. Reset Value: 0
9	TSIM	R_W	Timestamp Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of Timestamp Interrupt Status bit in Register 14 (Interrupt Status Register). This bit is valid only when IEEE1588 timestamping is enabled. In all other modes, this bit is reserved. Reset Value: 0

Bits	Name	Access	Description
8:4	-	RO	Reserved Reset Value: 00H
3	PMTIM	R_W	PMT Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PMT Interrupt Status bit in Register 14 (Interrupt Status Register). Reset Value: 0
2	PCSANCIM	R_W	PCS AN Completion Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PCS Auto-negotiation complete bit in Register 14 (Interrupt Status Register). Reset Value: 0
1	PCSLCHGIM	R_W	PCS Link Status Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the PCS Link-status changed bit in Register 14 (Interrupt Status Register). Reset Value: 0
0	RGSMIIIM	R_W	RGMII or SMII Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the RGMII or SMII Interrupt Status bit in Register 14 (Interrupt Status Register). Reset Value: 0

1.6.3.39 Register 16 (MAC Address0 High Register)

The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if 0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Figure & Table 1-56 Register 16 (MAC Address0 High Register)

Bits	Name	Access	Description
31	AE	RO	Address Enable This bit is always set to 1. Reset Value: 1
30:16	-	RO	Reserved Reset Value: 0000H
15:0	ADDRHI	R_W	MAC Address0 [47:32] This field contains the upper 16 bits (47:32) of the first 6-byte MAC address. The MAC uses this field for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames. Reset Value: FFFFH

1.6.3.40 Register 17 (MAC Address0 Low Register)

The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Figure & Table 1-57 Register 17 (MAC Address0 Low Register)

Bits	Name	Access	Description
31:0	ADDRLO	R_W	MAC Address0 [31:0] This field contains the lower 32 bits of the first 6-byte MAC address. This is used by the MAC for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames. Reset Value: FFFF_FFFFH

1.6.3.41 Register 18 (MAC Address1 High Register)

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station.

If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Figure & Table 1-58 Register 18 (MAC Address1 High Register)

Bits	Name	Access	Description
31	AE	R_W	Address Enable When this bit is set, the address filter module uses the

Bits	Name	Access	Description
			second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering. Reset Value: 0
30	SA	R_W	Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received frame. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received frame. Reset Value: 0
29:24	MBC	R_W	Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: ■ Bit 29: Register 18[15:8] ■ Bit 28: Register 18[7:0] ■ Bit 27: Register 19[31:24] ■ ... ■ Bit 24: Register 19[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. Reset Value: 000000
23:16	-	RO	Reserved Reset Value: 00H
15:0	ADDRHI	R_W	MAC Address1 [47:32] This field contains the upper 16 bits (47:32) of the second 6-byte MAC address. Reset Value: FFFFH

1.6.3.42 Register 19 (MAC Address1 Low Register)

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Figure & Table 1-59 Register 19 (MAC Address1 Low Register)

Bits	Name	Access	Description
31:0	ADDRLO	R_W	MAC Address1 [31:0] This field contains the lower 32 bits of the second 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process. Reset Value: FFFF_FFFFH

NOTE

- The descriptions for registers 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, and 46 (MAC Address2 High Register through MAC Address15 High Register) are the same as for the Register 18 (MAC Address1 High Register).
- The descriptions for registers 21, 23, 25, 27, 29, 31, 33, 35, 37, 38, 41, 43, 45, and 47 (MAC Address2 Low Register through MAC Address15 Low Register) are the same as for the Register 19 (MAC Address1 Low Register).
- The descriptions for registers 512, 514, 516, 518, 520, 522, 524, 526, 528, 530, 532, 534, 536, 538, 540, and 542 (MAC Address16 High Register through MAC Address31 High Register) are the same as for the Register 18 (MAC Address1 High Register).
- The descriptions for registers 513, 515, 517, 519, 521, 523, 525, 527, 529, 531, 533, 535, 537, 539, 541, and 543 (MAC Address16 Low Register through MAC Address31 Low Register) are the same as for the Register 19 (MAC Address1 Low Register).
- The descriptions for registers 546, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 568, 570, 572, 574, 576, 578, 580, 582, 584, 586, 588, 590, 592, 594, 596, 598, 600, 602, 604, 606, 608, 610, 612, 614, 616, 618, 620, 622, 624, 626, 628, 630, 632, 634, 636, 638, 640, 642, 644, 646, 648, 650, 652, 654, 656, 658, 660, 662, 664, 666, 668, 670, 672, 674, 676, 678, 680, 682, 684, 686, 688, 690, 692, 694, 696, 698, 700, 702, 704, 706, 708, 710, 712, 714, 716, 718, 720, 722, 724, 726, 728, 730, 732, and 734 (MAC Address33 High Register through MAC Address127 High Register) are the same as for the Register 544 (MAC Address32 High Register).
- The descriptions for registers 545, 547, 549, 551, 553, 555, 557, 559, 561, 563, 565, 567, 569, 571, 573, 575, 577, 579, 581, 583, 585, 587, 589, 591, 593, 595, 597, 599, 601, 603, 605, 607, 609, 611, 613, 615, 617, 619, 621, 623, 625, 627, 629, 631, 633, 635, 637, 639, 641, 643, 645, 647, 649, 651, 653, 655, 657, 659, 661, 663, 665, 667, 669, 671, 673, 675, 677, 679, 681, 683, 685, 687, 689, 691, 693, 695, 697, 699, 701, 703, 705, 707, 709, 711, 713, 715, 717, 719, 721, 723, 725, 727, 729, 731, 733, and 735 (MAC Address32 Low Register through MAC Address127 Low Register) are the same as for the Register 19 (MAC Address1 Low Register).

1.6.3.43 Register 544 (MAC Address32 High Register)

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station.

You can configure the MAC address registers to be double-synchronized by selecting the Synchronize CSR MAC Address to Tx/Rx Clock Domain option in coreConsultant. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register (Register 545) are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register (Register 545) after at least four clock cycles of the destination clock.

Figure & Table 1-60 Register 544 (MAC Address32 High Register)

Bits	Name	Access	Description
31	AE	R_W	Address Enable When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When reset, the address filter module ignores the address for filtering. Reset Value: 0
30:16	-	RO	Reserved Reset Value: 0000H
15:0	ADDRHI	R_W	MAC Address32 [47:32] This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address. Reset Value: FFFFH

1.6.3.44 Register 48 (AN Control Register)

The AN Control register enables and/or restarts auto-negotiation. It also enables PCS loopback. This register is optional and is present only when the MAC is configured for the TBI, SGMII, or RTBI PHY interface.

Figure & Table 1-61 Register 48 (AN Control Register)

Bits	Name	Access	Description
31:19	-	RO	Reserved Reset Value: 0000H
18	SGMRAL	R_W	SGMII RAL Control When set, this bit forces the SGMII RAL block to operate in the speed configured in the Speed and Port Select bits of the MAC Configuration register. This is useful when the SGMII interface is used in a direct MAC to MAC connection (without a PHY) and any MAC must reconfigure the speed. When reset, the SGMII RAL block operates according to the link speed status received on SGMII (from the PHY). This bit is reserved (and RO) if the SGMII PHY interface is not selected during core configuration. Reset Value: 0
17	LR	R_W	Lock to Reference When set, this bit enables the PHY to lock its PLL to the 125MHz reference clock. This bit controls the pcs_lck_ref_o signal on the TBI, RTBI, or SGMII interface.

Bits	Name	Access	Description
			Reset Value: 0
16	ECD	R_W	Enable Comma Detect When set, this bit enables the PHY for comma detection and word resynchronization. This bit controls the pcs_en_cdet_o signal on the TBI, RTBI, or SGMII interface. Reset Value: 0
15	-	RO	Reserved Reset Value: 0
14	ELE	R_W	External Loopback Enable When set, this bit causes the PHY to loopback the transmit data into the receive path. The pcs_ewrap_o signal is asserted high when this bit is set. Reset Value: 0
13	-	RO	Reserved Reset Value: 0
12	ANE	R_W	Auto-Negotiation Enable When set, this bit enables the MAC to perform auto-negotiation with the link partner. Clearing this bit disables the auto-negotiation. Reset Value: 0
11:10	-	RO	Reserved Reset Value: 00
9	RAN	R_WS_SC	Restart Auto-Negotiation When set, this bit causes auto-negotiation to restart if Bit 12 (ANE) is set. This bit is self-clearing after auto-negotiation starts. This bit should be cleared for normal operation. Reset Value: 0
8:0	-	RO	Reserved Reset Value: 00H

1.6.3.45 Register 49 (AN Status Register)

The AN Status register indicates the link and the auto-negotiation status. This register is optional and is present only when the MAC is configured for the TBI, RTBI, or SGMII PHY interface.

Figure & Table 1-62 Register 49 (AN Status Register)

Bits	Name	Access	Description
31:9	-	RO	Reserved Reset Value: 00_0000H
8	ES	RO	Extended Status This bit is tied to high if the TBI or RTBI interface is selected during core configuration indicating that the MAC supports extended status information in Register 53 (TBI Extended Status Register). This bit is tied to low if the SGMII interface is selected and the TBI or RTBI interface is not selected during core configuration indicating that Register 53 is not present. Reset Value: 1: TBI or RTBI interface 0: SGMII interface without TBI or RTBI interface
7:6	-	RO	Reserved Reset Value: 00
5	ANC	RO	Auto-Negotiation Complete When set, this bit indicates that the auto-negotiation process is complete. This bit is cleared when auto-negotiation is reinitiated. Reset Value: 0
4	-	RO	Reserved Reset Value: 0
3	ANA	RO	Auto-Negotiation Ability This bit is always high because the MAC supports auto-negotiation. Reset Value: 1
2	LS	R_SS_SC_LLO	Link Status This bit indicates whether the data channel (link) is up or down. For the TBI, RTBI or SGMII interfaces, if ANEG is going on, data cannot be transferred across the link and hence the link is given as down. Reset Value: 0
1:0	-	RO	Reserved Reset Value: 00

1.6.3.46 Register 50 (Auto-Negotiation Advertisement Register)

The Auto-Negotiation Advertisement register indicates the link and the auto-negotiation status. This register is optional and is present only when the MAC is configured for the TBI or RTBI PHY interface.

Figure & Table 1-63 Register 50 (Auto-Negotiation Advertisement Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15	NP	RO	Next Page Support This bit is always low because the MAC does not support the next page. Reset Value: 0
14	-	RO	Reserved Reset Value: 0
13:12	RFE	R_W	Remote Fault Encoding These bits provide a remote fault encoding, indicating to a link partner that a fault or error condition has occurred. The encoding of these bits is defined in IEEE 802.3z, Section 37.2.1.5. Reset Value: 00
11:9	-	RO	Reserved Reset Value: 000
8:7	PSE	R_W	Pause Encoding These bits provide an encoding for the Pause bits, indicating that the MAC is capable of configuring the Pause function as defined in IEEE 802.3x. The encoding of these bits is defined in IEEE 802.3z, Section 37.2.1.4. Reset Value: 11
6	HD	R_W	Half-Duplex When set high, this bit indicates that the MAC supports the half-duplex mode. This bit is always low (and RO) when the MAC is configured for the full-duplex-only mode. Reset Value: 1
5	FD	R_W	Full-Duplex When set high, this bit indicates that the MAC supports the full-duplex mode.

Bits	Name	Access	Description
			Reset Value: 1
4:0	-	RO	Reserved Reset Value: 00000

1.6.3.47 Register 51 (Auto-Negotiation Link Partner Ability Register)

The Auto-Negotiation Link Partner Ability register contains the advertised ability of the link partner. This register is optional and present only when the MAC is configured for the TBI or RTBI PHY interface.

Figure & Table 1-64 Register 51 (Auto-Negotiation Link Partner Ability Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15	NO	RO	Next Page Support When set, this bit indicates that more next page information is available. When cleared, this bit indicates that next page exchange is not desired. Reset Value: 0
14	ACK	RO	Acknowledge When set, the auto-negotiation function uses this bit to indicate that the link partner has successfully received the base page of the MAC. When cleared, it indicates that the link partner did not successfully receive the base page of the MAC. Reset Value: 0
13:12	RFE	RO	Remote Fault Encoding These bits provide a remote fault encoding, indicating a fault or error condition of the link partner. The encoding of these bits is defined in IEEE 802.3z, Section 37.2.1.5. Reset Value: 00
11:9	-	RO	Reserved Reset Value: 000
8:7	PSE	RO	Pause Encoding These bits provide an encoding for the Pause bits, indicating that the link partner's capability of configuring the Pause function as defined in the IEEE 802.3x specification. The encoding of these bits is

Bits	Name	Access	Description
			defined in IEEE 802.3z, Section 37.2.1.4. Reset Value: 00
6	HD	RO	Half-Duplex When set, this bit indicates that the link partner has the ability to operate in the half-duplex mode. When cleared, this bit indicates that the link partner does not have the ability to operate in the half-duplex mode. Reset Value: 0
5	FD	RO	Full-Duplex When set, this bit indicates that the link partner has the ability to operate in the full-duplex mode. When cleared, this bit indicates that the link partner does not have the ability to operate in the full-duplex mode. Reset Value: 0
4:0	-	RO	Reserved Reset Value: 00000

1.6.3.48 Register 52 (Auto-Negotiation Expansion Register)

The Auto-Negotiation Expansion register indicates if the MAC received a new base page from the link partner. This register is optional and is present only when the MAC is configured for the TBI or RTBI PHY interface.

Figure & Table 1-65 Register 52 (Auto-Negotiation Expansion Register)

Bits	Name	Access	Description
31:3	-	RO	Reserved Reset Value: 0000_0000H
2	NPA	RO	Next Page Ability This bit is always low because the MAC does not support the next page function. Reset Value: 0
1	NPR	RO	New Page Received When set, this bit indicates that the MAC has received a new page. This bit is cleared when read. Reset Value: 0
0	-	RO	Reserved Reset Value: 0

1.6.3.49 Register 53 (TBI Extended Status Register)

The TBI Extended Status register indicates all modes of operation of the MAC. This register is optional and is present only when the MAC is configured for the TBI or RTBI PHY interface.

Figure & Table 1-66 Register 53 (TBI Extended Status Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15	GFD	RO	1000BASE-X Full-Duplex Capable This bit indicates that the MAC is able to perform the full-duplex and 1000BASE-X operations. Reset Value: 1
14	GHD	RO	1000BASE-X Half-Duplex Capable This bit indicates that the MAC is able to perform the half-duplex and 1000BASE-X operations. This bit is always low when the MAC is configured for the full-duplex-only operation during core configuration. Reset Value: 1
13:0	-	RO	Reserved Reset Value: 0000H

1.6.3.50 Register 54 (SGMII/RGMII/SMII Control and Status Register)

The SGMII/RGMII/SMII Control and Status register indicates the status signals received by the SGMII, RGMII, or SMII interface (selected at reset) from the PHY. This register is optional and is present only when the MAC is configured for the SGMII, RGMII, or SMII PHY interface.

Figure & Table 1-67 Register 54 (SGMII/RGMII/SMII Control and Status Register)

Bits	Name	Access	Description
31:17	-	RO	Reserved Reset Value: 000H
16	SMIDRXS	R_W	Delay SMII RX Data Sampling with respect to the SMII SYNC Signal When set, the first bit of the SMII RX data is sampled one cycle after the SMII SYNC signal. When reset, the first bit of the SMII RX data is sampled along with the SMII SYNC signal. If the SMII PHY Interface with source synchronous mode is selected during core configuration, this bit is reserved (RO with default value).

Bits	Name	Access	Description
			Reset Value: 0
15:6	-	RO	Reserved Reset Value: 000H
5	FALSCARDET	RO	False Carrier Detected This bit indicates whether the SMII PHY detected false carrier (1'b1). This bit is reserved when the MAC is configured for the SGMII or RGMII PHY interface. Reset Value: 0
4	JABTO	RO	Jabber Timeout This bit indicates whether there is jabber timeout error (1'b1) in the received frame. This bit is reserved when the MAC is configured for the SGMII or RGMII PHY interface. Reset Value: 0
3	LNKSTS	RO	Link Status This bit indicates whether the link between the local PHY and the remote PHY is up or down. It gives the status of the link between the SGMII of MAC and the SGMII of the local PHY. The status bits are received from the local PHY during ANEG between the MAC and PHY on the SGMII link. Reset Value: 0
2:1	LNKSPEED	RO	Link Speed This bit indicates the current speed of the link: ■ 00: 2.5MHz ■ 01: 25MHz ■ 10: 125MHz Bit 2 is reserved when the MAC is configured for the SMII PHY interface. Reset Value: 10 for SGMII 00 for RGMII and SMII
0	LNKMOD	RO	Link Mode This bit indicates the current mode of operation of the link: ■ 1’b0: Half-duplex mode ■ 1’b1: Full-duplex mode

Bits	Name	Access	Description
			Reset Value: 0

1.6.3.51 Register 55 (Watchdog Timeout Register)

This register controls the watchdog timeout for received frames.

Figure & Table 1-68 Register 55 (Watchdog Timeout Register)

Bits	Name	Access	Description
31:17		RO	Reserved Reset Value: 0000H
16	PWE	R_W	Programmable Watchdog Enable When this bit is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, the WTO field (Bits[13:0]) is used as watchdog timeout for a received frame. When this bit is cleared, the watchdog timeout for a received frame is controlled by the setting of Bit 23 (WD) and Bit 20 (JE) in Register 0 (MAC Configuration Register). Reset Value: 0
15:14		RO	Reserved Reset Value: 00
13:0	WTO	R_W	Watchdog Timeout When Bit 16 (PWE) is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, this field is used as watchdog timeout for a received frame. If the length of a received frame exceeds the value of this field, such frame is terminated and declared as an error frame. Note: When Bit 16 (PWE) is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE Std 802.3-specified valid tagged frames are declared as error frames and are dropped. Reset Value: 0000H

1.6.3.52 Register 56 (General Purpose IO Register)

This register provides the control to drive up to 4 bits of output ports (GPO) and the status of up to 4 input ports (GPIS). It also provides the control to generate interrupts on events occurring on the gpi_i pin.

Figure & Table 1-69 Register 56 (General Purpose IO Register)

Bits	Name	Access	Description
31:28		RO	Reserved Reset Value: 0H
27:24	GPIT	R_W	GPI Type When set, this bit indicates that the corresponding GPIS is of latched-low (LL) type. When reset, this bit indicates that the corresponding GPIS is of latched-high (LH) type. The number of bits available in this field depend on the GP Input Signal Width option. Other bits are not used (reserved and always reset). Reset Value: 0H
23:20		RO	Reserved Reset Value: 0H
19:16	GPIE	R_W	GPI Interrupt Enable When this bit is set and the programmed event (LL or LH) occurs on the corresponding GPIS bit, Bit 11 (GPIIS) of Register 14 (Interrupt Status Register) is set. Accordingly, the interrupt is generated on the mci_intr_o or sbd_intr_o. The GPIIS bit is cleared when the host reads the Bits[7:0] of this register. When reset, Bit 11 (GPIIS) of Register 14 (Interrupt Status Register) is not set when any event occurs on the corresponding GPIS bits. The number of bits available in this field depend on the GP Input Signal Width option. Other bits are not used (reserved and always reset). Reset Value: 0H
15:12		RO	Reserved Reset Value: 0H
11:8	GPO	R_W	General Purpose Output When this bit is set, it directly drives the gpo_o output ports. When this bit is reset, it does not directly drive the gpo_o output ports. The number of bits available in this field depend on the GP Output Signal Width option. Other bits are not used (reserved and always reset). Reset Value: 0H

Bits	Name	Access	Description
7:4		RO	Reserved Reset Value: 0H
3:0	GPIS	LL, LH	General Purpose Input Status This field gives the status of the signals connected to the gpi_i input ports. This field is of the following types based on the setting of the corresponding GPIT field of this register: ■ Latched-low (LL): This field is cleared when the corresponding gpi_i input becomes low. This field remains low until the host reads this field. After this, this field reflects the current value of the gpi_i input. ■ Latched-high (LH): This field is set when the corresponding gpi_i input becomes high. This field remains high until the host reads this field. After this, this field reflects the current value of the gpi_i input. The number of bits available in this field depend on the GP Input Signal Width option. Other bits are not used (reserved and always reset). Reset Value: 0H

1.6.3.53 Register 256 (Layer 3 and Layer 4 Control Register 0)

This register controls the operations of the filter 0 of Layer 3 and Layer 4. This register is reserved if the Layer 3 and Layer 4 Filtering feature is not selected during core configuration.

Figure & Table 1-70 Register 256 (Layer 3 and Layer 4 Control Register 0)

Bits	Name	Access	Description
31:22	-	RO	Reserved Reset Value: 000H
21	L4DPIM0	R_W	Layer 4 Destination Port Inverse Match Enable When set, this bit indicates that the Layer 4 Destination Port number field is enabled for inverse matching. When reset, this bit indicates that the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when Bit 20 (L4DPM0) is set high. Reset Value: 0
20	L4DPM0	R_W	Layer 4 Destination Port Match Enable

Bits	Name	Access	Description
			When set, this bit indicates that the Layer 4 Destination Port number field is enabled for matching. When reset, the MAC ignores the Layer 4 Destination Port number field for matching. Reset Value: 0
19	L4SPIM0	R_W	Layer 4 Source Port Inverse Match Enable When set, this bit indicates that the Layer 4 Source Port number field is enabled for inverse matching. When reset, this bit indicates that the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when Bit 18 (L4SPM0) is set high. Reset Value: 0
18	L4SPM0	R_W	Layer 4 Source Port Match Enable When set, this bit indicates that the Layer 4 Source Port number field is enabled for matching. When reset, the MAC ignores the Layer 4 Source Port number field for matching. Reset Value: 0
17	-	RO	Reserved Reset Value: 0
16	L4PEN0	R_W	Layer 4 Protocol Enable When set, this bit indicates that the Source and Destination Port number fields for UDP frames are used for matching. When reset, this bit indicates that the Source and Destination Port number fields for TCP frames are used for matching. The Layer 4 matching is done only when either L4SPM0 or L4DPM0 bit is set high. Reset Value: 0
15:11	L3HDBM0	R_W	Layer 3 IP DA Higher Bits Match IPv4 Frames: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 frames. The following list describes the values of this field: ■ 0: No bits are masked. ■ 1: LSb[0] is masked. ■ 2: Two LSbs [1:0] are masked. ■ ...

Bits	Name	Access	Description
			■ 31: All bits except MSb are masked. IPv6 Frames: Bits [12:11] of this field correspond to Bits [6:5] of L3HSBM0, which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 frames. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: ■ 0: No bits are masked. ■ 1: LSb[0] is masked. ■ 2: Two LSbs [1:0] are masked. ■ ... ■ 127: All bits except MSb are masked. This field is valid and applicable only if L3DAM0 or L3SAM0 is set high. Reset Value: 00H
10:6	L3HSBM0	R_W	Layer 3 IP SA Higher Bits Match IPv4 Frames: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 frames. The following list describes the values of this field: ■ 0: No bits are masked. ■ 1: LSb[0] is masked. ■ 2: Two LSbs [1:0] are masked. ■ ... ■ 31: All bits except MSb are masked. IPv6 Frames: This field contains Bits [4:0] of the field that indicates the number of higher bits of IP Source or Destination Address matched in the IPv6 frames. This field is valid and applicable only if L3DAM0 or L3SAM0 is set high. Reset Value: 00H
5	L3DAIM0	R_W	Layer 3 IP DA Inverse Match Enable When set, this bit indicates that the Layer 3 IP Destination Address field is enabled for inverse matching. When reset, this bit indicates that the Layer 3 IP Destination Address field is enabled for perfect matching.

Bits	Name	Access	Description
			This bit is valid and applicable only when Bit 4 (L3DAM0) is set high. Reset Value: 0
4	L3DAM0	R_W	Layer 3 IP DA Match Enable When set, this bit indicates that Layer 3 IP Destination Address field is enabled for matching. When reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When Bit 0 (L3PEN0) is set, you should set either this bit or Bit 2 (L3SAM0) because either IPv6 DA or SA can be checked for filtering. Reset Value: 0
3	L3SAIM0	R_W	Layer 3 IP SA Inverse Match Enable When set, this bit indicates that the Layer 3 IP Source Address field is enabled for inverse matching. When reset, this bit indicates that the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when Bit 2 (L3SAM0) is set high. Reset Value: 0
2	L3SAM0	R_W	Layer 3 IP SA Match Enable When set, this bit indicates that the Layer 3 IP Source Address field is enabled for matching. When reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When Bit 0 (L3PEN0) is set, you should set either this bit or Bit 4 (L3DAM0) because either IPv6 SA or DA can be checked for filtering. Reset Value: 0
1	-	RO	Reserved Reset Value: 0
0	L3PEN0	R_W	Layer 3 Protocol Enable When set, this bit indicates that the Layer 3 IP Source or Destination Address matching is enabled for the IPv6 frames. When reset, this bit indicates that the Layer 3 IP Source or Destination Address matching is enabled for the IPv4 frames. The Layer 3 matching is done only when either L3SAM0 or L3DAM0 bit is set high.

Bits	Name	Access	Description
			Reset Value: 0

1.6.3.54 Register 257 (Layer 4 Address Register 0)

You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option in coreConsultant. If the Layer 3 and Layer 4 Address Registers are configured to be double-synchronized to the Rx clock domains, then the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform the consecutive writes to the same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

If the Layer 3 and Layer 4 Filtering feature is not selected during core configuration, this register and registers 260 through 299 are reserved (RO with default value).

Figure & Table 1-71 Register 257 (Layer 4 Address Register 0)

Bits	Name	Access	Description
31:16	L4DP0	R_W	Layer 4 Destination Port Number Field When Bit 16 (L4PEN0) is reset and Bit 20 (L4DPM0) is set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 frames. When Bit 16 (L4PEN0) and Bit 20 (L4DPM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 frames. Reset Value: 0000H
15:0	L4SP0	R_W	Layer 4 Source Port Number Field When Bit 16 (L4PEN0) is reset and Bit 20 (L4DPM0) is set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 frames. When Bit 16 (L4PEN0) and Bit 20 (L4DPM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 frames. Reset Value: 0000H

1.6.3.55 Register 260 (Layer 3 Address 0 Register 0)

For IPv4 frames, the Layer 3 Address 0 Register 0 contains the 32-bit IP Source Address field. For IPv6 frames, it contains Bits [31:0] of the 128-bit IP Source Address or Destination Address field.

Figure & Table 1-72 Register 260 (Layer 3 Address 0 Register 0)

Bits	Name	Access	Description
31:0	L3A00	R_W	Layer 3 Address 0 Field When Bit 0 (L3PEN0) and Bit 2 (L3SAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [31:0] of the IP Source Address field in the IPv6 frames. When Bit 0 (L3PEN0) and Bit 4 (L3DAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [31:0] of the IP Destination Address field in the IPv6 frames. When Bit 0 (L3PEN0) is reset and Bit 2 (L3SAM0) is set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with the IP Source Address field in the IPv4 frames. Reset Value: 00000000H

1.6.3.56 Register 261 (Layer 3 Address 1 Register 0)

For IPv4 frames, the Layer 3 Address 1 Register 0 contains the 32-bit IP Destination Address field. For IPv6 frames, it contains Bits [63:32] of the 128-bit IP Source Address or Destination Address field.

Figure & Table 1-73 Register 261 (Layer 3 Address 1 Register 0)

Bits	Name	Access	Description
31:0	L3A10	R_W	Layer 3 Address 1 Field When Bit 0 (L3PEN0) and Bit 2 (L3SAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [63:32] of the IP Source Address field in the IPv6 frames. When Bit 0 (L3PEN0) and Bit 4 (L3DAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [63:32] of the IP Destination Address field in the IPv6 frames. When Bit 0 (L3PEN0) is reset and Bit 4 (L3DAM0) is set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with the IP Destination Address field in the IPv4 frames.

Bits	Name	Access	Description
			Reset Value: 00000000H

1.6.3.57 Register 262 (Layer 3 Address 2 Register 0)

For IPv4 frames, the Layer 3 Address 2 Register 0 is reserved. For IPv6 frames, it contains Bits [95:64] of the 128-bit IP Source Address or Destination Address field.

Figure & Table 1-74 Register 262 (Layer 3 Address 2 Register 0)

Bits	Name	Access	Description
31:0	L3A20	R_W	Layer 3 Address 2 Field When Bit 0 (L3PEN0) and Bit 2 (L3SAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [95:64] of the IP Source Address field in the IPv6 frames. When Bit 0 (L3PEN0) and Bit 4 (L3DAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [95:64] of the IP Destination Address field in the IPv6 frames. When Bit 0 (L3PEN0) is reset in Register 256 (Layer 3 and Layer 4 Control Register 0), this register is not used. Reset Value: 00000000H

1.6.3.58 Register 263 (Layer 3 Address 3 Register 0)

For IPv4 frames, the Layer 3 Address 3 Register 0 is reserved. For IPv6 frames, it contains Bits [127:96] of the 128-bit IP Source Address or Destination Address field.

Figure & Table 1-75 Register 263 (Layer 3 Address 3 Register 0)

Bits	Name	Access	Description
31:0	L3A30	R_W	Layer 3 Address 3 Field When Bit 0 (L3PEN0) and Bit 2 (L3SAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [127:96] of the IP Source Address field in the IPv6 frames. When Bit 0 (L3PEN0) and Bit 4 (L3DAM0) are set in Register 256 (Layer 3 and Layer 4 Control Register 0), this field contains the value to be matched with Bits [127:96] of the IP Destination Address field in the IPv6 frames. When Bit 0 (L3PEN0) is reset in Register 256 (Layer 3

Bits	Name	Access	Description
			and Layer 4 Control Register 0), this register is not used. Reset Value: 00000000H

NOTE

- Registers 268, 280, and 292 are similar to Register 256 (Layer 3 and Layer 4 Control Register 0).
- Registers 269, 281, and 293 are similar to Register 257 (Layer 4 Address Register 0).
- Registers 272, 284, and 296 are similar to Register 260 (Layer 3 Address 0 Register 0).
- Registers 273, 285, and 297 are similar to Register 261 (Layer 3 Address 1 Register 0).
- Registers 274, 286, and 298 are similar to Register 262 (Layer 3 Address 2 Register 0).
- Registers 275, 287, and 299 are similar to Register 263 (Layer 3 Address 3 Register 0).
- Registers 268 through 275 are present when you select more than one Layer 3 and Layer 4 filters in coreConsultant.
- Registers 280 through 287 are present when you select more than two Layer 3 and Layer 4 filters in coreConsultant.
- Registers 292 through 299 are present when you select four Layer 3 and Layer 4 filters in coreConsultant.

1.6.3.59 Register 320 (Hash Table Register 0)

This register contains the first 32 bits of the hash table when the width of the Hash table is 128 bits or 256 bits. You can specify the width of the hash table by using the Hash Table Size option in coreConsultant.

The 128-bit or 256-bit Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming frame is passed through the CRC logic and the upper seven (eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determine the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 7b'1100000 (in 128-bit Hash) selects Bit 0 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.

The hash value of the destination address is calculated in the following way:

1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).
2. Perform bitwise reversal for the value obtained in Step 1.
3. Take the upper 7 (or 8) bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1’b1, the frame is accepted. Otherwise, it is rejected.

If the Bit 1 (Pass All Multicast) is set in Register 1 (MAC Frame Filter), then all multicast frames are accepted regardless of the multicast hash values.

If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.

NOTE

If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Figure & Table 1-76 Register 320 (Hash Table Register 0)

Bits	Name	Access	Description
31:0	HT31T0	R_W	First 32 bits of Hash Table This field contains the first 32 Bits (31:0) of the Hash table. Reset Value: 0000_0000H

NOTE

- Registers 321 through 327 are similar to Register 320 (Hash Table Register 0).
- Registers 324 through 327 are present only when you select the 256-bit Hash table during core configuration.

1.6.3.60 Register 353 (VLAN Tag Inclusion or Replacement Register)

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the transmit frames. This register is present only when the Enable SA, VLAN, and CRC Insertion on TX option is selected during core configuration.

Figure & Table 1-77 Register 353 (VLAN Tag Inclusion or Replacement Register)

Bits	Name	Access	Description
31:20	-	RO	Reserved Reset Value: 000H
19	CSVL	R_W	C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted frames. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the transmitted frames. Reset Value: 0
18	VLP	R_W	VLAN Priority Control When this bit is set, the control Bits [17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used, and Bits [17:16] are ignored. Reset Value: 0
17:16	VLC	R_W	VLAN Tag Control in Transmit Frames ■ 2’b00: No VLAN tag deletion, insertion, or replacement ■ 2’b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted frames with VLAN tags. ■ 2’b10: VLAN tag insertion

Bits	Name	Access	Description
			The MAC inserts VLT in bytes 15 and 16 of the frame after inserting the Type value (0x8100/0x88a8) in bytes 13 and 14. This operation is performed on all transmitted frames, irrespective of whether they already have a VLAN tag. ■ 2’b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted frames (Bytes 13 and 14 are 0x8100/0x88a8). Note: Changes to this field take effect only on the start of a frame. If you write this register field when a frame is being transmitted, only the subsequent frame can use the updated value, that is, the current frame does not use the updated value. Reset Value: 00
15:0	VLT	R_W	VLAN Tag for Transmit Frames This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority, Bit 12 is the CFI/DEI, and Bits[11:0] are the VLAN tag’s VID field. Reset Value: 0000H

1.6.3.61 Register 354 (VLAN Hash Table Register)

The 16-bit Hash table is used for group address filtering based on VLAN tag when Bit 19 (VTHM) of Register 7 (VLAN Tag Register) is set. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on Bit 16 (ETV) of VLAN Tag Register) in the incoming frame is passed through the CRC logic and the upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table.

The hash value of the destination address is calculated in the following way:

1. Calculate the 32-bit CRC for the VLAN tag or ID (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).
2. Perform bitwise reversal for the value obtained in Step 1.
3. Take the upper four bits from the value obtained in Step 2.

If the corresponding bit value of the register is 1’b1, the frame is accepted. Otherwise, it is rejected. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] (in little-endian mode) or Bits[7:0] (in big-endian mode) of this register are written.

NOTE

- If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.
- To help you program the hash table, a sample C routine that generates a VLAN tag’s 4-bit hash is included in /sample_codes/ directory of your workspace.

This register is valid and present only when VLAN Hash feature is enabled during core configuration.

Figure & Table 1-78 Register 354 (VLAN Hash Table Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15:0	VLHT	R_W	VLAN Hash Table This field contains the 16-bit VLAN Hash Table. Reset Value: 0000H

1.6.3.62 Register 448 (Timestamp Control Register)

This register controls the operation of the System Time generator and the processing of PTP packets for timestamping in the Receiver.

Figure & Table 1-79 Register 448 (Timestamp Control Register)

Bits	Name	Access	Description
31:29	-	RO	Reserved Reset Value: 000
28	ATSEN3	R_W	Auxiliary Snapshot 3 Enable This field controls capturing the Auxiliary Snapshot Trigger 3. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[3] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration or the selected number in the Number of IEEE 1588 Auxiliary Snapshot Inputs option is less than four. Reset Value: 0
27	ATSEN2	R_W	Auxiliary Snapshot 2 Enable This field controls capturing the Auxiliary Snapshot Trigger 2. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[2] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration or the selected number in the Number of

Bits	Name	Access	Description
			IEEE 1588 Auxiliary Snapshot Inputs option is less than three. Reset Value: 0
26	ATSEN1	R_W	Auxiliary Snapshot 1 Enable This field controls capturing the Auxiliary Snapshot Trigger 1. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration or the selected number in the Number of IEEE 1588 Auxiliary Snapshot Inputs option is less than two. Reset Value: 0
25	ATSEN0	R_W	Auxiliary Snapshot 0 Enable This field controls capturing the Auxiliary Snapshot Trigger 0. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration. Reset Value: 0
24	ATSFC	R_WS_SC	Auxiliary Snapshot FIFO Clear When set, it resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, auxiliary snapshots get stored in the FIFO. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration. Reset Value: 0
23:19	-	RO	Reserved Reset Value: 0
18	TSENMACADDR	R_W	Enable MAC address for PTP Frame Filtering When set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP frames when PTP is directly sent over Ethernet. Reset Value: 0

Bits	Name	Access	Description
17:16	SNAPTYPSEL	R_W	Select PTP packets for Taking Snapshots These bits along with Bits 15 and 14 decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Table 6-70 on page 462. Reset Value: 00
15	TSMSTRENA	R_W	Enable Snapshot for Messages Relevant to Master When set, the snapshot is taken only for the messages relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. Reset Value: 0
14	TSEVNTENA	R_W	Enable Timestamp Snapshot for Event Messages When set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Table 6-70 on page 462. Reset Value: 0
13	TSIPV4ENA	R_W	Enable Processing of PTP Frames Sent over IPv4-UDP When set, the MAC receiver processes the PTP packets encapsulated in UDP over IPv4 packets. When this bit is cleared, the MAC ignores the PTP transported over UDP-IPv4 packets. This bit is set by default. Reset Value: 1
12	TSIPV6ENA	R_W	Enable Processing of PTP Frames Sent over IPv6-UDP When set, the MAC receiver processes PTP packets encapsulated in UDP over IPv6 packets. When this bit is cleared, the MAC ignores the PTP transported over UDP-IPv6 packets. Reset Value: 0
11	TSIPENA	R_W	Enable Processing of PTP over Ethernet Frames When set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet frames. When this bit is cleared, the MAC ignores the PTP over Ethernet packets. Reset Value: 0

Bits	Name	Access	Description
10	TSVER2ENA	R_W	Enable PTP packet Processing for Version 2 Format When set, the PTP packets are processed using the 1588 version 2 format. Otherwise, the PTP packets are processed using the version 1 format. The IEEE 1588 Version 1 and Version 2 format are described in "PTP Processing and Control" on page 155. Reset Value: 0
9	TSCTRLSSR	R_W	Timestamp Digital or Binary Rollover Control When set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment has to be programmed correctly depending on the PTP reference clock frequency and the value of this bit. Reset Value: 0
8	TSENALL	R_W	Enable Timestamp for All Frames When set, the timestamp snapshot is enabled for all frames received by the MAC. Reset Value: 0
7:6	-	RO	Reserved Reset Value: 00
5	TSADDREG	R_WS_SC	Addend Reg Update When set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This is cleared when the update is completed. This register bit should be zero before setting it. Reset Value: 0
4	TSTRIG	R_WS_SC	Timestamp Interrupt Trigger Enable When set, the timestamp interrupt is generated when the System Time becomes greater than the value written in the Target Time register. This bit is reset after the generation of the Timestamp Trigger Interrupt. Reset Value: 0
3	TSUPDT	R_WS_SC	Timestamp Update When set, the system time is updated (added or subtracted) with the value specified in Register 452

Bits	Name	Access	Description
			(System Time – Seconds Update Register) and Register 453 (System Time – Nanoseconds Update Register). This bit should be read zero before updating it. This bit is reset when the update is completed in hardware. The "Timestamp Higher Word" register (if enabled during core configuration) is not updated. Reset Value: 0
2	TSINIT	R_WS_SC	Timestamp Initialize When set, the system time is initialized (overwritten) with the value specified in the Register 452 (System Time – Seconds Update Register) and Register 453 (System Time – Nanoseconds Update Register). This bit should be read zero before updating it. This bit is reset when the initialization is complete. The "Timestamp Higher Word" register (if enabled during core configuration) can only be initialized. Reset Value: 0
1	TSCFUPDT	R_W	Timestamp Fine or Coarse Update When set, this bit indicates that the system times update should be done using the fine update method. When reset, it indicates the system timestamp update should be done using the Coarse method. Reset Value: 0
0	TSENA	R_W	Timestamp Enable When set, the timestamp is added for the transmit and receive frames. When disabled, timestamp is not added for the transmit and receive frames and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the receive side, the MAC processes the 1588 frames only if this bit is set. Reset Value: 0

Figure & Table 1-80 indicates the PTP messages, for which a snapshot is taken depending on Bits [17:14] (SNAPTYPSEL), in Register 448 (Timestamp Control Register).

Figure & Table 1-80 Timestamp snapshot dependency on register bits

SNAPTYPSEL (Bits 17:16)	TSMSTRENA (Bit 15)	TSEVNTENA (Bit 14)	PTP Messages
00	X	0	SYNC, Follow_Up, Delay_Req, Delay_Resp
00	0	1	SYNC
00	1	1	Delay_Req
01	X	0	SYNC, Follow_Up, Delay_Req, Delay_Resp, Pdelay_Req, Pdelay_Resp, Pdelay_Resp_Follow_Up
01	0	1	SYNC, Pdelay_Req, Pdelay_Resp
01	1	1	Delay_Req, Pdelay_Req, Pdelay_Resp
10	X	X	SYNC, Delay_Req
11	X	X	Pdelay_Req, Pdelay_Resp

1.6.3.63 Register 449 (Sub-Second Increment Register)

This register is present only when the IEEE 1588 timestamp feature is selected without an external timestamp input. In the Coarse Update mode (TSCFUPDT bit in Register 448), the value in this register is added to the system time every clock cycle of clk_ptp_ref_i. In the Fine Update mode, the value in this register is added to the system time whenever the Accumulator gets an overflow.

Figure & Table 1-81 Register 449 (Sub-Second Increment Register)

Bits	Name	Access	Description
31:8	-	RO	Reserved Reset Value: 000000H
7:0	SSINC	R_W	Sub-second Increment Value The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when PTP clock is 50MHz (period is 20 ns), you should program 20 (0x14) when the System Time- Nanoseconds register has an accuracy of 1ns [Bit 9 (TSCTRLSSR) is set in Register 448 (Timestamp Control Register)]. When TSCTRLSSR is cleared, the Nanoseconds register has a resolution of ~0.465ns. In this case, you should program a value of 43 (0x2B) that is derived by 20ns/0.465. Reset Value: 00H

1.6.3.64 Register 450 (System Time – Seconds Register)

The System Time−Seconds register, along with System Time−Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).

These registers (450 and 451) are present only when the IEEE 1588 Timestamp feature is selected without external timestamp input.

Figure & Table 1-82 Register 450 (System Time – Seconds Register)

Bits	Name	Access	Description
31:0	TSS	RO	Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC. Reset Value: 00000000H

1.6.3.65 Register 451 (System Time – Nanoseconds Register)

Figure & Table 1-83 Register 451 (System Time – Nanoseconds Register)

Bits	Name	Access	Description
31	-	RO	Reserved Reset Value: 0
30:0	TSSS	RO	Timestamp Sub Seconds The value in this field has the sub second representation of time, with an accuracy of 0.46ns. When Bit 9 (TSCTRLSSR) is set in Register 448 (Timestamp Control Register), each bit represents 1ns and the maximum value is 0x3B9A_C9FF, after which it rolls-over to zero. Reset Value: 00000000H

1.6.3.66 Register 452 (System Time – Seconds Update Register)

The System Time−Seconds Update register, along with the System Time−Nanoseconds Update register, initializes or updates the system time maintained by the MAC. You must write both of these registers before setting the TSINIT or TSUPDT bits in the Timestamp Control register. This register is present only when the IEEE 1588 Timestamp feature is selected without external timestamp input.

Figure & Table 1-84 Register 452(System Time – Seconds Update Register)

Bits	Name	Access	Description
31:0	TSS	R_W	Timestamp Second The value in this field indicates the time in seconds to

Bits	Name	Access	Description
			be initialized or added to the system time. Reset Value: 00000000H

1.6.3.67 Register 453 (System Time – Nanoseconds Update Register)

This register is present only when IEEE 1588 timestamp feature is selected without external timestamp input.

Figure & Table 1-85 Register 453 (System Time – Nanoseconds Update Register)

Bits	Name	Access	Description
31	ADDSUB	R_W	Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. Reset Value: 0
30:0	TSSS	R_W	Timestamp Sub Seconds The value in this field has the sub second representation of time, with an accuracy of 0.46ns. When Bit 9 (TSCTRLSSR) is set in Register 448 (Timestamp Control Register), each bit represents 1ns and the programmed value should not exceed 0x3B9A_C9FF. Reset Value: 00000000H

1.6.3.68 Register 454 (Timestamp Addend Register)

This register is present only when the IEEE 1588 Timestamp feature is selected without external timestamp input. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in Register 448). This register content is added to a 32-bit accumulator in every clock cycle (of clk_ptp_ref_i) and the system time is updated whenever the accumulator overflows.

Figure & Table 1-86 Register 454 (Timestamp Addend Register)

Bits	Name	Access	Description
31:0	TSAR	R_W	Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization. Reset Value: 00000000H

1.6.3.69 Register 455 (Target Time Seconds Register)

The Target Time Seconds register, along with Target Time Nanoseconds register, is used to schedule an interrupt event (Register 458[1] when Advanced Timestamping is enabled; otherwise, TS interrupt bit in Register14[9]) when the system time exceeds the value programmed in these registers.

This register is present only when the IEEE 1588 Timestamp feature is selected without external timestamp input.

Figure & Table 1-87 Register 455 (Target Time Seconds Register)

Bits	Name	Access	Description
31:0	TSTR	R_W	Target Time Seconds Register This register stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, then based on Bits [6:5] of Register 459 (PPS Control Register), the MAC starts or stops the PPS signal output and generates an interrupt (if enabled). Reset Value: 00000000H

1.6.3.70 Register 456 (Target Time Nanoseconds Register)

This register is present only when the IEEE 1588 Timestamp feature is selected without external timestamp input.

Figure & Table 1-88 Register 456 (Target Time Nanoseconds Register)

Bits	Name	Access	Description
31	TRGTBUSY	R_WS_SC	Target Time Register Busy The MAC sets this bit when the PPSCMD field (Bit [3:0]) in Register 459 (PPS Control Register) is programmed to 010 or 011. Programming the PPSCMD field to 010 or 011, instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain. The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. This bit is reserved when the Enable Flexible Pulse-Per-Second Output feature is not selected. Reset Value: 0

Bits	Name	Access	Description
30:0	TTSLO	R_W	Target Timestamp Low Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the both Target Timestamp registers, then based on the TRGTMODSEL0 field (Bits [6:5]) in Register 459 (PPS Control Register), the MAC starts or stops the PPS signal output and generates an interrupt (if enabled). This value should not exceed 0x3B9A_C9FF when Bit 9 (TSCTRLSSR) is set in Register 448 (Timestamp Control Register). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. Reset Value: 00000000H

1.6.3.71 Register 457 (System Time - Higher Word Seconds Register)

This register is present only when the IEEE 1588 Advanced Timestamp feature is selected without an external timestamp input.

Figure & Table 1-89 Register 457 (System Time - Higher Word Seconds Register)

Bits	Name	Access	Description
31:16	-	RO	Reserved Reset Value: 0000H
15:0	TSHWR	R_W_SU	Timestamp Higher Word Register This field contains the most significant 16-bits of the timestamp seconds value. This register is optional and can be selected using the Enable IEEE 1588 Higher Word Register option during core configuration. The register is directly written to initialize the value. This register is incremented when there is an overflow from the 32-bits of the System Time - Seconds register. Reset Value: 0000H

1.6.3.72 Register 458 (Timestamp Status Register)

This register is present only when the Advanced IEEE 1588 Timestamp feature is selected. All bits except Bits[27:25] gets cleared when the host reads this register.

Figure & Table 1-90 Register 458 (Timestamp Status Register)

Bits	Name	Access	Description
31:30	-	RO	Reserved

Bits	Name	Access	Description
			Reset Value: 00
29:25	ATSNS	RO	Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected during core configuration. Reset Value: 00000
24	ATSSTM		Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected during core configuration.
23:20	-	RO	Reserved Reset Value: 0H
19:16	ATSSTN	R_SS_RC	Auxiliary Timestamp Snapshot Trigger Identifier These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: ■ Bit 16: Auxiliary trigger 0 ■ Bit 17: Auxiliary trigger 1 ■ Bit 18: Auxiliary trigger 2 ■ Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken. Reset Value: 0000
15:10	-	RO	Reserved Reset Value: 00H

Bits	Name	Access	Description
9	TSTRGTERR3	R_SS_RC	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 496 and Register 497, is already elapsed. This bit is cleared when read by the application. Reset Value: 0
8	TSTARGT3	R_SS_RC	Timestamp Target Time Reached for Target Time PPS3 When set, this bit indicates that the value of system time is greater than or equal to the value specified in Register 496 (PPS3 Target Time High Register) and Register 497 (PPS3 Target Time Low Register). Reset Value: 0
7	TSTRGTERR2	R_SS_RC	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 488 and Register 489, is already elapsed. This bit is cleared when read by the application. Reset Value: 0
6	TSTARGT2	R_SS_RC	Timestamp Target Time Reached for Target Time PPS2 When set, this bit indicates that the value of system time is greater than or equal to the value specified in Register 488 (PPS2 Target Time High Register) and Register 489 (PPS2 Target Time Low Register). Reset Value: 0
5	TSTRGTERR1	R_SS_RC	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 480 and Register 481, is already elapsed. This bit is cleared when read by the application. Reset Value: 0
4	TSTARGT1	R_SS_RC	Timestamp Target Time Reached for Target Time PPS1 When set, this bit indicates that the value of system time is greater than or equal to the value specified in Register 480 (PPS1 Target Time High Register) and Register 481 (PPS1 Target Time Low Register). Reset Value: 0
3	TSTRGTERR	R_SS_RC	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 455 and Register 456, is already elapsed. This bit is cleared when read by the application. Reset Value: 0

Bits	Name	Access	Description
2	AUXTSTRIG	R_SS_RC	Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Enable IEEE 1588 Auxiliary Snapshot feature is selected. Reset Value: 0
1	TSTARGT	R_SS_RC	Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the Register 455 (Target Time Seconds Register) and Register 456 (Target Time Nanoseconds Register). Reset Value: 0
0	TSSOVF	R_SS_RC	Timestamp Seconds Overflow When set, this bit indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Reset Value: 0

1.6.3.73 Register 459 (PPS Control Register)

This register is present only when the Advanced Timestamp feature is selected and External Timestamp is not enabled.

NOTE

- Bits[30:24] are valid only when four Flexible PPS outputs are selected.
- Bits[22:16] are valid only when three or more Flexible PPS outputs are selected.
- Bits[14:8] are valid only when two or more Flexible PPS outputs are selected.
- Bits[6:4] are valid only when Flexible PPS feature is selected.

Figure & Table 1-91 Register 459 (PPS Control Register)

Bits	Name	Access	Description
26:24	PPSCMD3	R_WS_SC	Flexible PPS3 Output Control This field controls the flexible PPS3 output (ptp_pps_o[3]) signal. This field is similar to PPSCMD0[2:0] in functionality. Reset Value: 000
23	-	RO	Reserved Reset Value: 0

Bits	Name	Access	Description
22:21	TRGTMODSEL2	R_W	Target Time Register Mode for PPS2 Output This field indicates the Target Time registers (register 488 and 489) mode for PPS2 output signal. This field is similar to the TRGTMODSEL0 field. Reset Value: 00
20:19	-	RO	Reserved Reset Value: 00
18:16	PPSCMD2	R_WS_SC	Flexible PPS2 Output Control This field controls the flexible PPS2 output (ptp_pps_o[2]) signal. This field is similar to PPSCMD0[2:0] in functionality. Reset Value: 000
15	-	RO	Reserved Reset Value: 0
14:13	TRGTMODSEL1	R_W	Target Time Register Mode for PPS1 Output This field indicates the Target Time registers (register 480 and 481) mode for PPS1 output signal. This field is similar to the TRGTMODSEL0 field. Reset Value: 00
12:11	-	RO	Reserved Reset Value: 00
10:8	PPSCMD1	R_WS_SC	Flexible PPS1 Output Control This field controls the flexible PPS1 output (ptp_pps_o[1]) signal. This field is similar to PPSCMD0[2:0] in functionality. Reset Value: 00
7	-	RO	Reserved Reset Value: 0

Bits	Name	Access	Description
6:5	TRGTMODSEL0	R_W	Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (register 455 and 456) mode for PPS0 output signal: ■ 00: Indicates that the Target Time registers are programmed only for generating the interrupt event. ■ 01: Reserved ■ 10: Indicates that the Target Time registers are programmed for generating the interrupt event and starting or stopping the generation of the PPS0 output signal. ■ 11: Indicates that the Target Time registers are programmed only for starting or stopping the generation of the PPS0 output signal. No interrupt is asserted. Reset Value: 00
4	PPSEN0	R_W	Flexible PPS Output Mode Enable When set low, Bits [3:0] function as PPSCTRL (backward compatible). When set high, Bits[3:0] function as PPSCMD. Reset Value: 0
3:0	PPSCTRL0	R_W	PPSCTRL0: PPS0 Output Frequency Control This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: ■ 0001: The binary rollover is 2Hz, and the digital rollover is 1Hz. ■ 0010: The binary rollover is 4Hz, and the digital rollover is 2Hz. ■ 0011: The binary rollover is 8Hz, and the digital rollover is 4Hz. ■ 0100: The binary rollover is 16Hz, and the digital rollover is 8Hz. ■ ... ■ 1111: The binary rollover is 32.768KHz, and the digital rollover is 16.384KHz.

Bits	Name	Access	Description
			Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: ■ When PPSCTRL = 0001, the PPS (1Hz) has a low period of 537ms and a high period of 463ms. ■ When PPSCTRL = 0010, the PPS (2Hz) is a sequence of: - One clock of 50 percent duty cycle and 537ms period - Second clock of 463ms period (268ms low and 195ms high) ■ When PPSCTRL = 0011, the PPS (4Hz) is a sequence of: - Three clocks of 50 percent duty cycle and 268ms period - Fourth clock of 195ms period (134ms low and 61ms high) This behavior is because of the non-linear toggling of bits in the digital rollover mode in Register 451 (System Time – Nanoseconds Register). Reset Value: 0H

1.6.3.74 Register 460 (Auxiliary Timestamp – Nanoseconds Register)

This register, along with Register 461 (Auxiliary Timestamp – Seconds Register), gives the 64-bit timestamp stored as auxiliary snapshot. The two registers together form the read port of a 64-bit wide FIFO with a depth of 4, 8, or 16 as selected during core configuration. Multiple snapshots can be stored in this FIFO. The ATSNS bits in the Timestamp Status register indicate the fill-level of this FIFO. The top of the FIFO is removed only when the last byte of Register 461 (Auxiliary Timestamp - Seconds Register) is read. In the little-endian mode, this means when Bits[31:24] are read. In big-endian mode, it corresponds to the reading of Bits[7:0] of Register 461 (Auxiliary Timestamp - Seconds Register).

This register and Register 461 (Auxiliary Timestamp - Seconds Register) are present only when you select the Auxiliary Snapshot Enable feature during core configuration.

Figure & Table 1-92 Register 460 (Auxiliary Timestamp – Nanoseconds Register)

Bits	Name	Access	Description
31:26	-	RO	Reserved Reset Value: 00H
25:24	PTPCH	R_W	Channel for Queuing the PTP Packets This field specifies the channel on which the untagged PTP packets, sent over the Ethernet payload and not over IPv4 or IPv6, are queued. ■ 00: Channel 0 ■ 01: Channel 1 ■ 10: Channel 2 ■ 11: Reserved These bits are reserved if the receive paths of Channel 1 or Channel 2 are not enabled. Reset Value: 00
23	-	RO	Reserved Reset Value: 0
22:21	AVCH	R_W	Channel for Queuing the AV Control Packets This field specifies the channel on which the received untagged AV control packets are queued. ■ 00: Channel 0 ■ 01: Channel 1 ■ 10: Channel 2 ■ 11: Reserved These bits are reserved if the receive paths of Channel 1 or Channel 2 are not enabled. Reset Value: 00
20	AVCD	R_W	AV Channel Disable When this bit is set, the MAC forwards all packets to the default Channel 0 and the values programmed in the AVP, AVCH, and PTPCH fields are ignored. This bit is reserved and read-only if Channel 1 or Channel 2 receive paths are not selected during core configuration. Reset Value: 0
19	VQE	R_W	VLAN Tagged Non-AV Packets Queueing Enable When this bit is set, the MAC also queues non-AV VLAN tagged packets into the available channels according

Bits	Name	Access	Description
			to the value of the AVP bits. This bit is reserved and read-only if Channel 1 and Channel 2 Receive paths are not selected during core configuration. Reset Value: 0
18:16	AVP	R_W	AV Priority for Queuing The value programmed in these bits control the receive channel (0, 1, or 2) to which an AV packet with a given priority must be queued. ■ If only Channel 1 receive path is enabled, the AV packets with priority value greater than or equal to the programmed value are queued on Channel 1 and all other packets are queued on Channel 0. ■ If Channel 2 receive path is also enabled, the AV packets with priority value greater than or equal to the programmed value are queued on Channel 2. The AV packets with value less than the programmed value on Channel 1 and all other packets are queued on Channel 0. These bits are applicable only if at least one additional receive channel is selected in the AV mode. Reset Value: 000
15:0	AVT	R_W	AV EtherType Value This field contains the value that is compared with the EtherType field of the incoming (tagged or untagged) Ethernet frame to detect an AV packet. Reset Value: 0000H

1.6.3.75 Register 461 (Auxiliary Timestamp - Seconds Register)

Figure & Table 1-93 Register 461 (Auxiliary Timestamp - Seconds Register)

Bits	Name	Access	Description
31:0	AUXTSHI	RO	Contains the lower 32 bits of the Seconds field of the auxiliary timestamp. Reset Value: 00000000H

1.6.3.76 Register 462 (AV MAC Control Register)

This register controls the AV traffic by identifying the AV traffic and queuing it to appropriate channel. This register is present only when you select the AV feature during core configuration.

Figure & Table 1-94 Register 462 (AV MAC Control Register)

Bits	Name	Access	Description
22:21	AVCH	R_W	Channel for Queuing the AV Control Packets This field specifies the channel on which the received untagged AV control packets are queued. ■ 00: Channel 0 ■ 01: Channel 1 ■ 10: Channel 2 ■ 11: Reserved These bits are reserved if the receive paths of Channel 1 or Channel 2 are not enabled. Reset Value: 00
20	AVCD	R_W	AV Channel Disable When this bit is set, the MAC forwards all packets to the default Channel 0 and the values programmed in the AVP, AVCH, and PTPCH fields are ignored. This bit is reserved and read-only if Channel 1 or Channel 2 receive paths are not selected during core configuration. Reset Value: 0
19	VQE	R_W	VLAN Tagged Non-AV Packets Queueing Enable When this bit is set, the MAC also queues non-AV VLAN tagged packets into the available channels according to the value of the AVP bits. This bit is reserved and read-only if Channel 1 and Channel 2 Receive paths are not selected during core configuration. Reset Value: 0
18:16	AVP	R_W	AV Priority for Queuing The value programmed in these bits control the receive channel (0, 1, or 2) to which an AV packet with a given priority must be queued. ■ If only Channel 1 receive path is enabled, the AV packets with priority value greater than or equal to the programmed value are queued on Channel 1 and all other packets are queued on Channel 0. ■ If Channel 2 receive path is also enabled, the AV packets with priority value greater than or equal to the programmed value are queued on Channel 2. The AV packets with value less than the

Bits	Name	Access	Description
			programmed value on Channel 1 and all other packets are queued on Channel 0. These bits are applicable only if at least one additional receive channel is selected in the AV mode. Reset Value: 000
15:0	AVT	R_W	AV EtherType Value This field contains the value that is compared with the EtherType field of the incoming (tagged or untagged) Ethernet frame to detect an AV packet. Reset Value: 0000H

1.6.3.77 Register 472 (PPS0 Interval Register)

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]).

Figure & Table 1-95 Register 472 (PPS0 Interval Register)

Bits	Name	Access	Description
31:0	PPSINT	R_W	PPS0 Output Signal Interval These bits store the interval between the rising edges of PPS0 signal output in terms of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50MHz (period of 20ns), and desired interval between rising edges of PPS0 signal output is 100ns (that is, five units of sub-second increment value), then you should program value 4 (5 - 1) in this register. Reset Value: 00000000H

1.6.3.78 Register 473 (PPS0 Width Register)

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of the PPS0 signal output (ptp_pps_o[0]).

Figure & Table 1-96 Register 473 (PPS0 Width Register)

Bits	Name	Access	Description
31:0	PPSWIDTH	R_W	PPS0 Output Signal Width These bits store the width between the rising edge and corresponding falling edge of the PPS0 signal output in terms of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50MHz (period of 20ns), and desired width between the rising and corresponding falling edges of PPS0 signal output is 80ns (that is, four units of sub-second increment value), then you should program value 3 (4 – 1) in this register. Note: The value programmed in this register must be lesser than the value programmed in Register 472 (PPS0 Interval Register). Reset Value: 00000000H

1.6.3.79 Register 480 (PPS1 Target Time Seconds Register)

The PPS1 Target Time Seconds register, along with PPS1 Target Time Nanoseconds register, is used to schedule an interrupt event (Bit 1 (TSTARGT) of Register 458 (Timestamp Status Register)) when the system time exceeds the value programmed in these registers.

This register is present only when more than one Flexible PPS output is selected during core configuration.

Figure & Table 1-97 Register 480 (PPS1 Target Time Seconds Register)

Bits	Name	Access	Description
31:0	TSTRH1	R_W	PPS1 Target Time Seconds Register This register stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, then based on Bits [14:13], TRGTMODSEL1, of Register 459 (PPS Control Register), the MAC starts or stops the PPS signal output and generates an interrupt (if enabled). Reset Value: 00000000H

1.6.3.80 Register 481 (PPS1 Target Time Nanoseconds Register)

This register is present only when more than one Flexible PPS output is selected during core configuration.

Figure & Table 1-98 Register 481 (PPS1 Target Time Nanoseconds Register)

Bits	Name	Access	Description
31	TRGTBUSY1	R_WS_SC	PPS1 Target Time Register Busy The MAC sets this bit when the PPSCMD1 field (Bits [10:8]) in Register 459 (PPS Control Register) is programmed to 010 or 011. Programming the PPSCMD1 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. Reset Value: 0
30:0	TTSL1	R_W	Target Time Low for PPS1 Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the both Target Timestamp registers, then based on the TRGTMODSEL1 field (Bits [14:13]) in Register 459 (PPS Control Register), the MAC starts or stops the PPS signal output and generates an interrupt (if enabled). This value should not exceed 0x3B9A_C9FF when Bit 9 (TSCTRLSSR) is set in Register 448 (Timestamp Control Register). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. Reset Value: 00000000H

2 USB

2.1 Overview

The USB3 DRD (Dule Role Device) module is designed in this chip. It supports DRD mode, which supports either device or host operation separately, not simultaneously. The USB3 DRD module supports the USB 3.0 SuperSpeed (5Gbps) protocol and data rate and is backward compatible with USB 2.0 high-speed (480Mbps), full-speed (12Mbps), and low-speed (1.5Mbps) protocols and data rates. USB3 DRD module includes USB3 DRD controller and PHY.

USB3 DRD module supports xHCI1.1 and can use standard or open-source xHCI and class drivers.

It can be used in portable electronic devices, such as high-bandwidth mass storage disks, and high-bandwidth applications.

2.2 Main Features

The main features which supported by USB3 DRD module are as below:

- Supports USB3.0 standard protocol, can be configured as device or host mode
- Supports either device or host operation separately, not simultaneously
- Supports super speed (5Gbps IN and 5Gbps OUT), high speed (480Mbps), full speed (12Mbps), low speed (1.5Mbps, host mode only)
- Supports DMA access (internal DMA controller)
- Supports control transfer, interrupt transfer, bulk transfer, isochronous transfer
- Power-saving features (clock gating)
- Descriptor caching and data pre-fetching used to meet system performance in high-latency systems
- Same programming model for SuperSpeed (SS), High-Speed (HS), Full-Speed (FS), and Low-Speed (LS)
- xHCI1.1 compatible
- Standard or open-source xHCI and class drivers

2.3 Interface

The PAD of the USB is described in the following Figure & Table 2-1:

Figure & Table 2-1 Pin description table

Pin Name	Direction	Width	Description
USB_DRD_DM	IO	1	USB D- Signal This bidirectional pin carries USB2.0 data to and from the USB 3.0 femtoPHY. In HS operation, this pin receives/transmits a

Pin Name	Direction	Width	Description
			maximum of 800mV or 400mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally.
USB_DRD_DP	IO	1	USB D+ Signal This bidirectional pin carries USB2.0 data to and from the USB 3.0 femtoPHY. In HS operation, this pin receives/transmits a maximum of 800mV or 400mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally.
USB_DRD_ID	IO	1	USB Mini-Receptacle Identifier and Test Point for DC Points Probes Inside USB 3.0 femtoPHY Differentiates a mini-A from a mini-B plug. The ID<#> line is sampled only when the IDPULLUP0 signal is high. After sampling the ID<#> line, IDDIG0 indicates whether a mini-A or mini-B cable is connected. If this signal is not used, internal resistance pulls the signal's voltage level up to the analog I/O supply level when IDPULLUP0 is high. If IDPULLUP0 is low, ID<#> is pulled down to the PHY ground. The ID<#> pin can also be used as an input/output analog test signal. Voltage on this node is determined by the test interface mode and the VATESTENB signal. If ID<#> is not used, leave it floating and tie VATESTENB low.
USB_DRD_VBUS	IO	1	USB 5-V Power Supply Pin USB power supply pin. A charge pump external to the USB 3.0 femtoPHY must provide power to this pin. The PHY VBUS<#> pin must not connect directly to the 5-V VBUS voltage on the USB 3.0 link; instead, this pin must be isolated by an external resistor (REXT1) so that the PHY VBUS<#> pin sources a lower voltage.
USB_DRD_RCLKN	I	1	ref_pad_clk_m is Low-Swing Differential Input Clock Pair With Pad. Reference clock from external source: either ref_pad_clk_\{p,m\} or ref_alt_clk_\{p,m\} can be used, but never both. The selection is based on ref_use_pad and whether the reference clock is provided to the core via an ondie distribution network or external pins.
USB_DRD_RCLKP	I	1	ref_pad_clk_p is Low-Swing Differential Input Clock Pair With Pad.

Pin Name	Direction	Width	Description
			Reference clock from external source: either ref_pad_clk_\{p,m\} or ref_alt_clk_\{p,m\} can be used, but never both. The selection is based on ref_use_pad and whether the reference clock is provided to the core via an ondie distribution network or external pins.
USB_DRD_RES	IO	1	Reference Resistor Connection Attach a precision resistor-to-ground on the board, with the following specifications: ■ Resistance: 200Ohm ■ Temperature: Coefficient +/-100 ppm/degree C ■ Tolerance: +/-1%
USB_DRD_RXM	I	1	rxX_m is High-Speed Differential Receive Pair. Receive differential pair.
USB_DRD_RXP	I	1	rxX_p is High-Speed Differential Receive Pair. Receive differential pair.
USB_DRD_TXM	O	1	txX_m is High-Speed Differential Transmit Pair. Transmit differential pair.
USB_DRD_TXP	O	1	txX_p is High-Speed Differential Transmit Pair. Transmit differential pair.

2.4 Function Description

The functional logic diagram of USB3 DRD is as Figure & Table 2-2 Functional logic diagram. The USB3 DRD includes one USB3 DRD controller, one USB3.0 femtoPHY, and three SRAMs. The controller and PHY are connected through PIPE/UTMI interface.

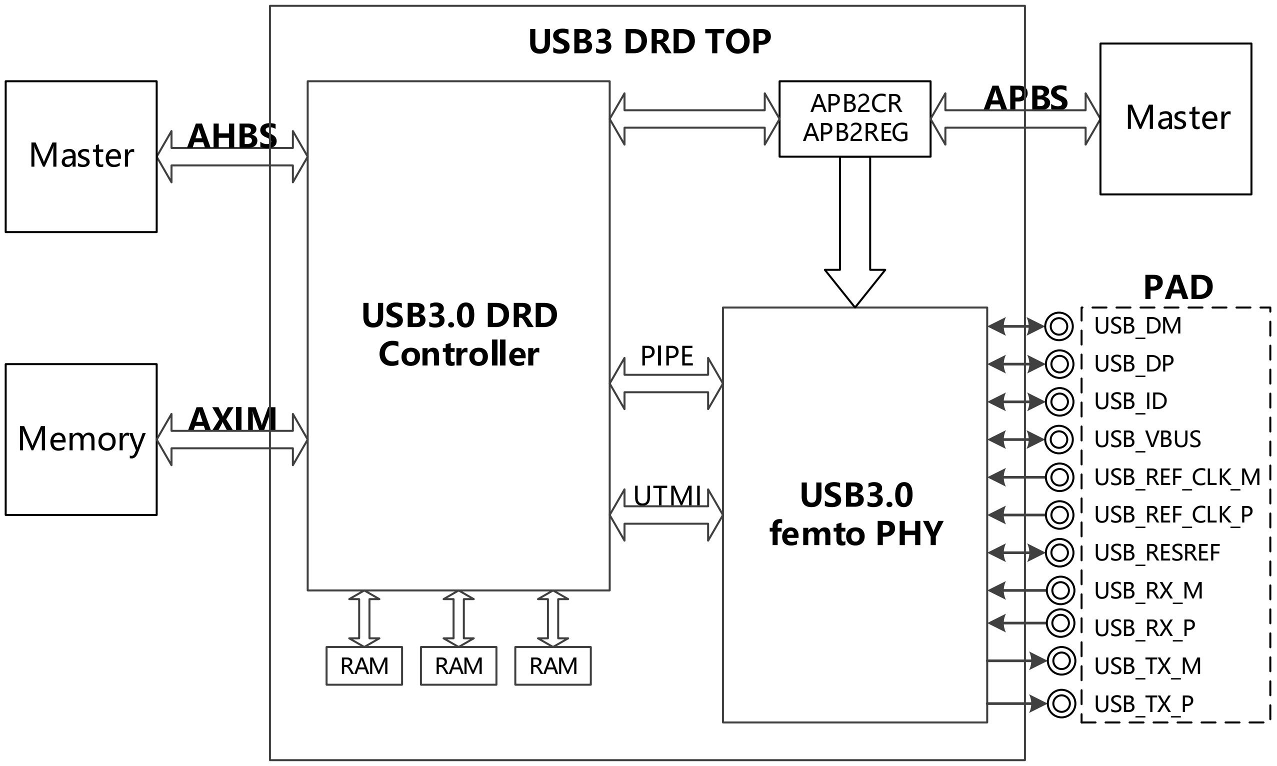

Figure & Table 2-2 Functional logic diagram

The peripheral interfaces of USB3 DRD includes High-Speed AHB Slave Bus interface used for registers configuration of controller, High-Speed AXI Master Bus interface used for data transmission, Low-Speed APB Bus interface used for controlling some signals of controller and PHY in initialization or ATE tests, and PADs connected with USB socket.

2.5 Usage

2.5.1 Clock and Reset

These clock and reset initialization process should be configured before USB3 DRD controller initialization:

1. Write 1’b1 to the usb3_drd_clk_en/usb3_drd_ctrl_ref_clk_en/usb3_drd_phy_ref_clk_en fields of the clock register MISCSYS_USB_CLK_CTRL [0xFF_EC02_C104] to enable the AHB/AXI/APB configuration clock, the controller reference clock, PHY reference clock and suspend clock. Note that this register is enabled by default.
2. Write 1’b1 to the REF_SSP_EN field of the system register REF_SSP_EN [0xFF_EC03_F034] to enable the PHY internal reference clock.
3. Before using USB, enable the IOPMP module of USB. The base address of USB_IOPMP is 0xFF_FC02_E000. For details, refer to the IOPMP manual.
4. After completing the above steps for 10us, write 1 to sw_usb3_drd_vccrst_n/sw_usb3_drd_phyrst_n/sw_usb3_drd_prst_n of the reset register USB3_DRD_SWRST [0xFF_EC02_C014] to de-assert USB DRD’s reset.
5. Initialize USB 3.0 controller registers to start transition.

2.5.2 Switching Host/Device Mode

The sequence for switching modes in DRD configuration is as follows:

- Switching from Device to Host:

1. Reset the controller using GCTL[11] (CoreSoftReset).
2. Set GCTL[13:12] (PrtCapDir) to 2'b01 (Host mode).
3. Reset the host using USBCMD.HCRESET.
4. Follow the steps in "Initializing Host Registers" section of the Programming Guide.

- Switching from Host to Device:

1. Reset the controller using GCTL[11] (CoreSoftReset).
2. Set GCTL[13:12] (PrtCapDir) to 2'b10 (Device mode).
3. Reset the device by setting DCTL[30] (CSftRst).
4. Follow the steps in "Register Initialization" section of the Programming Guide.

2.6 Register Description

The USB's register involves four parts:

- Controller register
- xHCI register
- PHY register
- System control status register

The base address of the four-segment register is as follows:

- The USB's AHB interface (base address: 0xFF_E704_0000) can access controller register and xHCI general register.
  The controller register's base address is 0xFF_E704_0000.
  The xHCI register's base address is 0xFF_E704_0020.
- The USB's APB interface (base address: 0xFF_EC03_0000) can access PHY registers and system control status register.
  The PHY register's base address is 0xFF_EC03_0000, and the offset address is the register description offset address*2.
  The system control status register's base address is 0xFF_EC03_F000.

The system control status register is described in detail as follows：

2.6.1 Register Memory Map

Register	Offset	Description	Section/Page
USB_CLK_GATE_STS	0x0	Clock gate status register	2.6.2.1/134
USB_LOGIC_ANALYZER_TRACE_STS0	0x4	Logic analyzer trace 0 register	2.6.2.2/135
USB_LOGIC_ANALYZER_TRACE_STS1	0x8	Logic analyzer trace 1 register	2.6.2.3/135

Register	Offset	Description	Section/Page
USB_GPIO	0xc	GPIO register	2.6.2.4/135
USB_DEBUG_STS0	0x10	DEBUG 0 register	2.6.2.5/135
USB_DEBUG_STS1	0x14	DEBUG 1 register	2.6.2.6/136
USB_DEBUG_STS2	0x18	DEBUG 2 register	2.6.2.7/136
USBCTL_CLK_CTRL0	0x1c	HS Jitter adjustment register	2.6.2.8/136
USBPHY_CLK_CTRL1	0x20	PHY clock control register	2.6.2.9/136
USBPHY_TEST_CTRL0	0x24	PHY test control 0 register	2.6.2.10/138
USBPHY_TEST_CTRL1	0x28	PHY test control 1 register	2.6.2.11/140
USBPHY_TEST_CTRL2	0x2c	PHY test control 2 register	2.6.2.12/143
USBPHY_TEST_CTRL3	0x30	PHY test control 3 register	2.6.2.13/144
REF_SSP_EN	0x34	Reference clock enable register	2.6.2.14/145
USB_HADDR_SEL	0x38	AHB address select register	2.6.2.15/145
USB_SYS	0x3c	USB system control register	2.6.2.16/145
USB_HOST_STATUS	0x40	Host status register	2.6.2.17/147
USB_HOST_CTRL	0x44	Host control register	2.6.2.18/149
USBPHY_HOST_CTRL	0x48	USB PHY host control register	2.6.2.19/153
USBPHY_HOST_STATUS	0x4c	USB PHY host status register	2.6.2.20/154
USB_TEST_REG0	0x50	USB test register 0	2.6.2.21/155
USB_TEST_REG1	0x54	USB test register 1	2.6.2.22/156
USB_TEST_REG2	0x58	USB test register 2	2.6.2.23/156
USB_TEST_REG3	0x5c	USB test register 3	2.6.2.24/156

2.6.2 Register and Field Description

2.6.2.1 USB_CLK_GATE_STS

- Description: Clock gate status register
- Offset: 0x0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	

Bits	Field Name	Access	Description
[2:0]	CLK_GATE_CTRL	RO	Clock gate status Value After Reset: 0x0

2.6.2.2 USB_LOGIC_ANALYZER_TRACE_STS0

- Description: Logic analyzer trace 0 register
- Offset: 0x4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	LOGIC_ANALYZER_TRACE0	RO	Logic analyzer trace 0 Value After Reset: 0x0

2.6.2.3 USB_LOGIC_ANALYZER_TRACE_STS1

- Description: Logic analyzer trace 1 register
- Offset: 0x8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	LOGIC_ANALYZER_TRACE1	RO	Logic analyzer trace 1 Value After Reset: 0x0

2.6.2.4 USB_GPIO

- Description: GPIO register
- Offset: 0xc
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	GP_OUT	RO	GPIO OUT Value After Reset: 0x0
[15:0]	GP_IN	RW	GPIO IN Value After Reset: 0x0

2.6.2.5 USB_DEBUG_STS0

- Description: Debug 0 register
- Offset: 0x10
- Default Value: 0x40

Bits	Field Name	Access	Description
[31:0]	DEBUG0	RO	USB debug 0 Value After Reset: 0x40

2.6.2.6 USB_DEBUG_STS1

- Description: Debug 1 register
- Offset: 0x14
- Default Value: 0x3c400

Bits	Field Name	Access	Description
[31:0]	DEBUG1	RO	USB debug 1 Value After Reset: 0x3C400

2.6.2.7 USB_DEBUG_STS2

- Description: Debug 2 register
- Offset: 0x18
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2:0]	DEBUG2	RO	USB debug 2 Value After Reset: 0x00

2.6.2.8 USBCTL_CLK_CTRL0

- Description: HS jitter adjustment register
- Offset: 0x1c
- Default Value: 0x20

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5:0]	FLADJ_30MHZ_REG	RW	HS jitter adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125's duration. Value After Reset: 0x20

2.6.2.9 USBPHY_CLK_CTRL1

- Description: PHY clock control register
- Offset: 0x20

- Default Value: 0x2a00

Bits	Field Name	Access	Description
[31:29]	RESERVED_3	-	
[28:20]	PHY_SSC_REF_CLK_SEL	RW	Spread Spectrum Reference Clock Shifting Enables non-standard oscillator frequencies to generate targeted MPLL output rates. Input corresponds to frequency-synthesis coefficient. ■ ssc_ref_clk_sel[8:6] = modulous - 1 ■ ssc_ref_clk_sel[5:0] = 2's complement push amount Value After Reset: 0x0
[19]	RESERVED_2	-	
[18:16]	PHY_SSC_RANGE	RW	Spread Spectrum Clock Range Selects the range of spread spectrum modulation when ssc_en is asserted and the PHY is spreading the high-speed transmit clocks. Applies a fixed offset to the phase accumulator. Value After Reset: 0x0
[15]	REF_CLK_SEL	RW	Select reference clock connected to ref_pad_clk_\{p,m\}. When asserted, selects the external ref_pad_clk_\{p,m\} inputs as the reference clock source. When ref_use_pad is de-asserted, ref_alt_clk_\{p,m\} are selected for an on-chip reference clock source. Value After Reset: 0x0
[14]	PHY_REF_CLKDIV2	RW	Input Reference Clock Divider Control If the input reference clock frequency is greater than 100MHz, this signal must be asserted. The reference clock frequency is then divided by 2 to keep it in the range required by the MPLL. Value After Reset: 0x0
[13:8]	PHY_FSEL	RW	Frequency Select Selects the reference clock frequency used for both SS and HS operations. Value After Reset: 0x2A
[7]	RESERVED_1	-	
[6:0]	PHY_MPLL_MULTIPLIER	RW	MPLL Frequency Multiplier Control Multiplies the reference clock to a frequency suitable

Bits	Field Name	Access	Description
			for intended operating speed. Value After Reset: 0x0

2.6.2.10 USBPHY_TEST_CTRL0

- Description: PHY test control 0 register
- Offset: 0x24
- Default Value: 0x95182

Bits	Field Name	Access	Description
[31:29]	RESERVED_4	-	
[28:24]	LANE0_TX_TERM_OFFSET	RW	Transmitter Termination Offset Reserved. Set to 5'b00000. Value After Reset: 0x0
[23:21]	RESERVED_3	-	
[20:16]	LOS_LEVEL	RW	Loss-of-Signal Detector Sensitivity Level Control Reserved. Set this bus to 0x09. Value After Reset: 0x9
[15]	RESERVED_2	-	
[14:12]	LOS_BIAS	RW	Loss-of-Signal Detector Threshold Level Control Sets the LOS detection threshold level. To enable tuning at the board level, connect this bus to a register. ■ 111: 135mV ■ 110: 120mV ■ 101: 105mV ■ 100: 90mV ■ 011: 75mV ■ 010: 60mV ■ 001: 45mV ■ 000: Invalid Default: 3'b101 Value After Reset: 0x5
[11]	RTUNE_ACK	RO	Resistor Tune Acknowledge While asserted, indicates that a resistor tune is still in progress. Value After Reset: 0x0

Bits	Field Name	Access	Description
[10]	RTUNE_REQ	RW	Resistor Tune Request Assertion triggers a resistor tune request (if one is not already in progress). When this signal is asserted, rtune_ack goes high until calibration of the termination impedances is complete. Value After Reset: 0x0
[9:8]	VDATREFTUNE0	RW	Data Detect Voltage Adjustment Adjusts the threshold voltage level (Vdat_ref) used to detect data during charger-type detection. ■ 11: -20% ■ 10: -10% ■ 01: 0 (default) ■ 00: +10% Value After Reset: 0x1
[7:4]	TXVREFTUNE0	RW	HS DC Voltage Level Adjustment Adjusts the high-speed DC level voltage. To enable tuning at the board level, connect this bus to a register. ■ 1111: +8.75% ■ 1110: +7.5% ■ 1101: +6.25% ■ 1100: +5% ■ 1011: +3.75% ■ 1010: +2.5% ■ 1001: +1.25% ■ 1000: 0 (default) ■ 0111: -1.25% ■ 0110: -2.5% ■ 0101: -3.75% ■ 0100: -5% ■ 0011: -6.25% ■ 0010: -7.5% ■ 0001: -8.75% ■ 0000: -10% Value After Reset: 0x8
[3:2]	RESERVED_1	-	
[1:0]	TXRISETUNE0	RW	HS Transmitter Rise/Fall Time Adjustment

Bits	Field Name	Access	Description
			Adjusts the rise/fall times of the high-speed waveform. To enable tuning at the board level, connect this bit to a register. ■ 11: -10% ■ 10: 0 (default) ■ 01: +15% ■ 00: +20% Value After Reset: 0x2

2.6.2.11 USBPHY_TEST_CTRL1

- Description: PHY test control 1 register
- Offset: 0x28
- Default Value: 0x10303344

Bits	Field Name	Access	Description
[31:30]	RESERVED_7	-	
[29:28]	TXRESTUNE0	RW	USB Source Impedance Adjustment Some applications require additional devices to be added on the USB, such as a series switch, which can add significant series resistance. This bus adjusts the driver source impedance (for both pull-up/pulldown impedances in LS/FS mode and the pull-down impedance in HS mode) to compensate for added series resistance on the USB. ■ 11: -4Ohm ■ 10: -2Ohm ■ 01: 0 (default) ■ 00: +1.5Ohm Value After Reset: 0x1
[27:26]	RESERVED_6	-	
[25:24]	TXPREEMPAMPTUNE0	RW	HS Transmitter Pre-Emphasis Current Control This signal controls the amount of current sourced to DP<#> and DM<#> after a J-to-K or K-to-J transition. The HS Transmitter pre-emphasis current is defined in terms of unit amounts. One unit amount is approximately 600uA and is defined as 1X pre-emphasis current. ■ 11: 3x pre-emphasis current

Bits	Field Name	Access	Description
			■ 10: 2x pre-emphasis current ■ 01: 1x pre-emphasis current ■ 00: Disabled (default) If these signals are not used, set them to 2'b00. Value After Reset: 0x0
[23:22]	RESERVED_5	-	
[21:20]	TXHSXVTUNE0	RW	Transmitter High-Speed Crossover Adjustment This bus adjusts the voltage at which the DP<#> and DM<#> signals cross while transmitting in HS mode. ■ 11: 0 (default) ■ 10: +15mV ■ 01: -15mV ■ 00: Reserved Value After Reset: 0x3
[19:17]	RESERVED_4	-	
[16]	TXPREEMPPULSETUNE0	RW	HS Transmitter Pre-Emphasis Duration Control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP<#> or DM<#>. The HS Transmitter pre-emphasis duration is defined in terms of unit amounts. One unit of pre-emphasis duration is approximately 580ps and is defined as 1X pre-emphasis duration. This signal is valid only if either TXPREEMPAMPTUNE<#>[1] or TXPREEMPAMPTUNE<#>[0] is set to 1'b1. ■ 1: Short ■ 0: Long (default) If TXPREEMPPULSETUNE<#> is not used, set it to 1'b0. Value After Reset: 0x0
[15:12]	TXFSLSTUNE0	RW	FS/LS Source Impedance Adjustment Adjusts the low- and full-speed single-ended source impedance while driving high. To enable tuning at the board level, connect this bus to a register. ■ 1111: -5% ■ 0111: -2.5% ■ 0011: 0 (default) ■ 0001: +2.5% ■ 0000: +5%

Bits	Field Name	Access	Description
			This parameter control is encoded in thermometer code. Any nonthermometer code setting (that is, 1001) is reserved and not supported. Value After Reset: 0x3
[11]	RESERVED_3	-	
[10:8]	SQRXTUNE0	RW	Squelch Threshold Adjustment Adjusts the voltage level for the threshold used to detect valid high speed data. To enable tuning at the board level, connect this bus to a register. ■ 111: -20% ■ 110: -15% ■ 101: -10% ■ 100: -5% ■ 011: 0 (default) ■ 010: +5% ■ 001: +10% ■ 000: +15% Value After Reset: 0x3
[7]	RESERVED_2	-	
[6:4]	OTGTUNE0	RW	VBUS Valid Threshold Adjustment This bus adjusts the voltage level for the VBUS<#> valid threshold. To enable tuning at the board level, connect this bus to a register. ■ 111: +9% ■ 110: +6% ■ 101: +3% ■ 100: 0 (default) ■ 011: -3% ■ 010: -6% ■ 001: -9% ■ 000: -12% Value After Reset: 0x4
[3]	RESERVED_1	-	
[2:0]	COMPDISTUNE0	RW	Disconnect Threshold Adjustment Adjusts the voltage level for the threshold used to

Bits	Field Name	Access	Description
			detect a disconnect event at the host. To enable tuning at the board level, connect this bus to a register. ■ 111: +4.5% ■ 110: +3% ■ 101: +1.5% ■ 100: 0 (default) ■ 011: -1.5% ■ 010: -3% ■ 001: -4.5% ■ 000: -6% Value After Reset: 0x4

2.6.2.12 USBPHY_TEST_CTRL2

- Description: PHY test control 2 register
- Offset: 0x2c
- Default Value: 0x1c1c0f0

Bits	Field Name	Access	Description
[31:26]	RESERVED_3	-	
[25:20]	PCS_TX_DEEMPH_6DB	RW	TX De-Emphasis at 6dB This static value sets the TX driver de-emphasis value when pipeP_tx_deemph[1:0] is set to 2'b10 (according to the PIPE3 specification). This bus is provided for completeness and as a second potential launch amplitude. Default: 28 Value After Reset: 0x1C
[19:18]	RESERVED_2	-	
[17:12]	PCS_TX_DEEMPH_3P5DB	RW	TX De-Emphasis at 3.5dB This static value sets the TX driver de-emphasis value when pipeX_tx_deemph[1:0] is set to 2'b01 (according to the PIPE3 specification). To enable tuning at the board level for RX eye compliance, connect this signal to a register. Default: 28 Value After Reset: 0x1C
[11:10]	RESERVED_1	-	

Bits	Field Name	Access	Description
[9:0]	PCS_RX_LOS_MASK_VAL	RW	Configurable Loss-of-Signal Mask Width Sets the number of reference clock cycles to mask the incoming LFPS in U3 and U2 states. Masks the incoming LFPS for the number of reference clock cycles equal to the value of pcs_rx_los_mask_val[9:0]. This control filters out short, non-compliant LFPS glitches sent by a non-compliant host. Value After Reset: 0xF0

2.6.2.13 USBPHY_TEST_CTRL3

- Description: PHY test control 3 register
- Offset: 0x30
- Default Value: 0x47f

Bits	Field Name	Access	Description
[31:12]	RESERVED_2	-	
[11]	PHY_LOOPBACKENB0	RW	Loopback Test Enable This controller signal places the USB 3.0 femtoPHY in HS loopback mode, which concurrently enables the HS receive and transmit logic. ■ 1: During HS data transmission, the HS receive logic is enabled. ■ 0: During HS data transmission, the HS receive logic is disabled. Value After Reset: 0x0
[10:8]	TX_VBOOST_LVL	RW	TX Voltage Boost Level Sets the boosted transmit launch amplitude (mVppd). To enable tuning at the board level, connect this bus to a register. Default: 3'b100 Value After Reset: 0x4
[7]	RESERVED_1	-	
[6:0]	PCS_TX_SWING_FULL	RW	TX Amplitude (Full Swing Mode) This static value sets the launch amplitude of the transmitter. To enable tuning at the board level for RX eye compliance, connect this signal to a register. Default: 127 (7b'1111111)

Bits	Field Name	Access	Description
			Value After Reset: 0x7F

2.6.2.14 REF_SSP_EN

- Description: Reference clock enable register
- Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	REF_SSP_EN	RW	Reference Clock Enable for SS function Enables the reference clock to the prescaler. The ref_ssp_en signal must remain de-asserted until the reference clock is running at the appropriate frequency, at which point ref_ssp_en can be asserted. For lower power states, ref_ssp_en can also be de-asserted. Value After Reset: 0x0

2.6.2.15 USB_HADDR_SEL

- Description: AHB address select register
- Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:4]	RESERVED_1	-	
[3:0]	HADDR_SEL	RW	Used to select haddr[19:16]: 0x0 to 0x3: Normal AHB bus's reg Access (only 0x0 useful) 0x4 to 0x7: Internal RAM 0 - Debug Access (256KB) 0x8 to 0xb: Internal RAM 1 - Debug Access (256KB) 0xc to 0xf: Internal RAM 2 - Debug Access (256KB) Value After Reset: 0x0

2.6.2.16 USB_SYS

- Description: USB system control register
- Offset: 0x3c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:9]	RESERVED_1	-	
[8]	ATERESET	RW	Reset Input from Automatic Test Equipment When the USB 3.0 femtoPHY is powered up (not in Suspend or Sleep mode), an automatic tester can use this test signal to disable PHYCLOCK<#> and FREECLK, then re-enable them with an aligned phase. ■ 1: PHYCLOCK<#> and FREECLK outputs are disabled. ■ 0: PHYCLOCK<#> and FREECLK outputs are available within a specific period after ATERESET is de-asserted. Value After Reset: 0x0
[7:4]	BUS_FILTER_BYPASS	RW	Bus Filter Bypass. Disables the internal bus filters that are enabled by DWC_USB3_EN_BUS_FILTERS coreConsultant parameter. This static signal is present only when DWC_USB3_EN_BUS_FILTERS is 1. It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the controller. The function of each bit is: ■ bus_filter_bypass[3]: Reserved ■ bus_filter_bypass[2]: Bypass the filter for utmisrp_bvalid ■ bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports ■ bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In Host-only mode, internal bus filters are not needed. Therefore, bus_filter_bypass[2:0] must be connected to logic high value (3'b111). The reserved bit can be tied to 0 or 1, but should not be floating. Values: ■ 1'b0: Bus filter(s) enabled ■ 1'b1: Bus filter(s) disabled (bypassed) Value After Reset: 0x0
[3]	VATESTENB	RW	Analog Test Pin Select Enables analog test voltages to be placed on the ID<#> pin. ■ 1: Analog test voltages can be viewed or applied on ID<#>.

Bits	Field Name	Access	Description
			■ 0: Analog test voltages cannot be viewed or applied on ID<#>. Value After Reset: 0x0
[2]	TEST_POWERDOWN_SSP	RW	SS Function Circuits Power-Down Control Powers down all SS function circuitry in the PHY for IDDQ testing. Before asserting this signal, ensure that phy_reset is set to 1'b1. Value After Reset: 0x0
[1]	TEST_POWERDOWN_HSP	RW	HS Function Circuits Power-Down Control Powers down all HS function circuitry in the PHY for IDDQ testing. Before asserting this signal, ensure that VDATSRCENB<#>, VDATDETENB<#>, DCDENB<#>, BYPASSSEL<#>, and test_burnin are set to 1'b0. Value After Reset: 0x0
[0]	COMMONONN	RW	Common Block Power-Down Control Controls the power-down signals in the PLL block when the USB 3.0 femtoPHY is in Suspend or Sleep mode. ■ 1: In Suspend or Sleep mode, the PLL block is powered down. ■ 0: In Suspend or Sleep mode, the PLL block remains powered and continues to draw current. While the PHY is not in either Suspend mode nor Sleep state, COMMONONN can be dynamically controlled. Value After Reset: 0x0

2.6.2.17 USB_HOST_STATUS

- Description: Host status register
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:22]	RESERVED_3	-	
[21]	HOST_SYSTEM_ERR	RO	Host System Error This signal indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field. This signal is asserted only if the USBCMD.HSEE field is set

Bits	Field Name	Access	Description
			to '1'. It can occur when the host controller encounters an 'Error' response in the AHB, the AXI, or the Native Master Bus. When the USBSTS.HSE field is cleared by software, this signal is de-asserted unless the master continues to assert its bus error output. The typical software response to an HSE is to reset the controller. For more details, refer to section 4.10.2.6 of the xHCI 1.0 specification. Value After Reset: 0x0
[20]	HOST_LEGACY_SMI_INTERRUPT	RO	SMI interrupt, active high. The PCIe interface need to pass this SMI interrupt output. Value After Reset: 0x0
[19:18]	RESERVED_2	-	
[17:16]	OPERATIONAL_MODE	RO	Port capability direction This signal defines the mode of operation of the controller. It directly reflects the value programmed in bit[13:12] of the GCTL register. PRTCAPDIR: Port Capability Direction (PrtCapDir) ■ 2'b01: For Host configurations ■ 2'b10: For Device configurations Value After Reset: 0x0
[15:14]	RESERVED_1	-	
[13:12]	HUB_VBUS_CTRL	RO	Port Power control for each downstream port ■ 0: VBUS OFF ■ 1: VBUS ON The lower bits are for USB 2.0 ports and the higher bits are for USB 3.0 SS ports: hub_vbus_ctrl[N-1:0] = { hub_vbus_ctrl['DWC_USB3_NUM_U3_ROOT_PORTS-1:0], hub_vbus_ctrl['DWC_USB3_NUM_U2_ROOT_PORTS-1:0]} Value After Reset: 0x0
[11:0]	HOST_CURRENT_BELT	RO	Current BELT Value This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode.

Bits	Field Name	Access	Description
			Value After Reset: 0x0

2.6.2.18 USB_HOST_CTRL

- Description: Host control register
- Offset: 0x44
- Default Value: 0x1101

Bits	Field Name	Access	Description
[31:26]	RESERVED_4	-	
[25]	PIPE3_POWERPRESENT	RW	Not used, reserved Value After Reset: 0x0
[24]	UTMIOTG_VBUSVALID	RW	Vbus Valid. Indicates if the voltage Vbus is valid for Host and A-Device operation. The comparator thresholds are: ■ 1'b0: Vbus < 4.4V ■ 1'b1: Vbus > 4.75V This signal must be a filtered signal if DWC_USB3_EN_BUS_FILTERS is chosen as 0. It must be the same as pipe3_PowerPresent. This input must be driven in all non-peripheral (host) modes if DWC_USB3_HSPHY_INTERFACE is chosen as UTMI. In Host-only mode, this signal must be connected to logic high value of 1'b1. Value After Reset: 0x0
[23:22]	RESERVED_3	-	
[21:20]	HUB_PORT_OVERCURRENT	RW	This is the per port Overcurrent indication of the root-hub ports: ■ 0: No Overcurrent ■ 1: Overcurrent The lower bits are for USB 2.0 ports and the higher bits are for USB 3.0 SS ports: hub_port_overcurrent[N-1:0] = { hub_port_overcurrent['DWC_USB3_NUM_U3_ROOT_PORTS-1:0], hub_port_overcurrent['DWC_USB3_NUM_U2_ROOT_PORTS-1:0]} The minimum required overcurrent duration is 3 suspend clock periods.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[19:18]	RESERVED_2	-	
[17:16]	HUB_PORT_PERM_ATTACH	RW	Indicates if the device attached to a downstream port is permanently attached or not. ■ 0: Not permanently attached ■ 1: Permanently attached The lower bits are for USB 2.0 ports and the higher bits are for USB 3.0 SS ports: hub_port_perm_attach[N-1:0] = { hub_port_perm_attach['DWC_USB3_NUM_U3_ROOT_PORTS-1:0], [hub_port_perm_attach['DWC_USB3_NUM_U2_ROOT_PORTS-1:0]} Value After Reset: 0x0
[15:12]	HOST_NUM_U2_PORT	RW	Number of USB 2.0 Ports. This signal overrides the 'DWC_USB3_NUM_U2_ROOT_PORTS synthesis configuration parameter. This allows you, for example, to develop a chip with a 4-Port USB 2.0 host and package it as only two USB 2.0 ports in a board. The upper two ports are not enabled. The 'Number of Ports' field of the HCSPARAMS1 register is controlled by this port. The 'Number of Ports' indicates 'host_num_u3_ports + host_num_u2_port' value. If you do not require the override feature, assign this port as follows: assign host_num_u2_ports3:0] = 'DWC_USB3_NUM_ U2_ROOT_PORTS; Value After Reset: 0x1
[11:8]	HOST_NUM_U3_PORT	RW	Number of USB 3.0 SS Ports. This signal overrides the 'DWC_USB3_NUM_U3_ROOT_PORTS synthesis configuration parameter. This allows you, for example, to develop a chip with a 4-Port USB 3.0 SS host and package it as only two USB 3.0 SS ports in a board. The upper two ports are not enabled. The 'Number of Ports' field of the HCSPARAMS1 register is controlled by this port. The 'Number of Ports' indicates 'host_num_u3_ports + host_num_u2_port' value.

Bits	Field Name	Access	Description
			If you do not require the override feature, assign this port as follows: assign host_num_u3_port[3:0] = 'DWC_USB3_NUM_ U3_ROOT_PORTS; Value After Reset: 0x1
[7]	RESERVED_1	-	
[6]	HOST_U2_PORT_DISABLE	RW	USB 2.0 Port Disable control ■ 0: Port enabled. ■ 1: Port disabled. This signal, when '1', stops reportingconnect/disconnect events the port and keeps the port in disabled state. This could be used for security reasons where hardware can disable a port irrespective of whether xHCI driver enables a port or not. The 'Number of Ports' field of the HCSPARAMS1 register is not affected by this signal. This signal should be either static (should not change during operation), or change only once from 0 to 1 during operation and stay at 1 after that. Note: Port-0 (the first U2 port) must not be disabled if any other U2 port is operational. Value After Reset: 0x0
[5]	HOST_U3_PORT_DISABLE	RW	USB 3.0 SS Port Disable control ■ 0: Port enabled. ■ 1: Port disabled. This signal, when '1', stops reporting connect/disconnect events the port and keeps the port in disabled state. This could be used for security reasons where hardware can disable a port irrespective of whether xHCI driver enables a port or not. The 'Number of Ports' field of the HCSPARAMS1 register is not affected by this signal. This signal should be either static (should not change during operation), or change only once from 0 to 1 during operation and stay at 1 after that. Note: ■ This signal is not present in USB 2.0-only mode.

Bits	Field Name	Access	Description
			■ The SuperSpeed Port0 (first SS port) must not be disabled if the other SuperSpeed ports are operational. Value After Reset: 0x0
[4]	HOST_PORT_POWER_CONTROL_PRESENT	RW	This port defines bit[3] of Capability Parameters (HCCPARAMS). Change the PPC value through the pin Port Power Control (PPC). This indicates whether the host controller implementation includes port power control. ■ 0: Indicates that the port does not have port power switches. ■ 1: Indicates that the port has port power switches. Value After Reset: 0x0
[3]	HOST_MSI_ENABLE	RW	This enables the pulse type interrupt signal (one bus clock cycle) 'interrupt' port instead of level-sensitive interrupt. When interfacing to PCIe, this allows you to easily map 'interrupt' to MSI in the PCIe controller. MSI can only be enabled in the Host mode. There is no MSI support in the Device mode yet. So if the controller is configured in the DRD mode, it can only use wire interrupt which is a level signal. Value After Reset: 0x0
[2]	HOST_LEGACY_SMI_PCI_CMD_REG_WR	RW	PCI command register write, one clock pulse. The PCIe interface needs to generate one clock pulse during PCIe command register write. Tie this low if you are not using Legacy support. Value After Reset: 0x0
[1]	HOST_LEGACY_SMI_BAR_WR	RW	PCI Base Address register (BAR) write, one clock pulse. The PCIe interface need to generate one clock pulse during PCIe Base Address register (BAR) write. Tie this low, if you are not using legacy support. Value After Reset: 0x0
[0]	XHC_BME	RW	This signal is used to disable the bus mastering capability of the xHC. In a PCI system, it comes from the Bus Master Enable (BME) bit of the Device Control Register in the PCI Configuration register space. ■ 1'b0: Bus mastering capability is disabled. The host controller cannot use the bus master interface. ■ 1'b1: Bus mastering capability is enabled.

Bits	Field Name	Access	Description
			Note: In Host mode, ■ For a non-PCI system, the xhc_bme is always tied to 1'b1 for the controller master to work. ■ For a PCI system, connect the BME register bit of the PCI to this xhc_bme input. In Device mode, the xhc_bme can be any value, but it is recommended to tie this signal to 1. Value After Reset: 0x1

2.6.2.19 USBPHY_HOST_CTRL

- Description: USB PHY host control register
- Offset: 0x48
- Default Value: 0x18

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	VBUSVLDEXT0	RW	External VBUS Valid Select Selects the VBUSVLDEXT<#> input or the internal Session Valid comparator to indicate when the VBUS<#> signal on the USB cable is valid. ■ 1: VBUSVLDEXT<#> input is used. ■ 0: Internal Session Valid comparator is used. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Value After Reset: 0x0
[4]	RX0LOSLFPSEN	RW	RX LOS LFPS Filter Enable (0) Enables the RX LOS LFPS filter. During USB 3.0 operation, set to 1'b1. ■ 1: Enables RX LOS LFPS filter. ■ 0: Disables RX LOS LFPS filter. Change this pin setting only during a reset. Value After Reset: 0x1

Bits	Field Name	Access	Description
[3]	OTGDISABLE0	RW	OTG Block Disable This controller signal powers down the OTG block, which disables the VBUS Valid and Session End comparators. The Session Valid comparator (the output of which is used to enable the pull-up resistor on DP<#> in Device mode) is always on irrespective of the state of OTGDISABLE0. If the application does not use the OTG function, this input can be set high to save power. ■ 1: OTG block is powered down. ■ 0: OTG block is powered up. Value After Reset: 0x1
[2]	VBUSVLDEXTSEL0	RW	Value After Reset: 0x0
[1]	DRVVBUS0	RW	Drive VBUS This controller signal controls the VBUS Valid comparator. This signal drives 5 V on VBUS<#> through an external charge pump. When OTGDISABLE0 is set to 1'b0 and DRVVBUS0 is asserted, the Bandgap circuitry and VBUS Valid comparator are powered, even in Suspend or Sleep mode. ■ 1: VBUS Valid comparator is enabled. ■ 0: VBUS Valid comparator is disabled. Value After Reset: 0x0
[0]	IDPULLUP0	RW	Analog ID Input Sample Enable This controller signal controls ID<#> line sampling. ■ 1: ID<#> pin sampling is enabled, and the IDDIG0 output is valid. ■ 0: ID<#> pin sampling is disabled, and the IDDIG0 output is not valid. Value After Reset: 0x0

2.6.2.20 USBPHY_HOST_STATUS

- Description: USB PHY host status register
- Offset: 0x4c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:3]	RESERVED_1	-	
[2]	VBUSVALID0	RO	VBUS Valid Indicator This controller signal is output from the USB 3.0 femtoPHY's VBUS. Valid comparator and indicates whether the VBUS0 output is at a valid level. ■ 1: VBUS<#> output is valid. ■ 0: VBUS<#> output is not valid. Value After Reset: 0x0
[1]	IDDIG0	RO	Mini A/B Plug Indicator This controller signal indicates whether the connected plug is a mini-A or mini-B plug. This signal must be valid within 20ms after the IDPULLUP0 signal is set to 1'b1. ■ 1: Connected plug is a mini-B plug. ■ 0: Connected plug is a mini-A plug. Value After Reset: 0x0
[0]	OTGSESSVLD0	RO	OTG Device Session Valid Indicator (Low Voltage) This controller signal is output from the USB 3.0 femtoPHY's Session Valid comparator and indicates whether the voltage on VBUS is below the OTG Device Session Valid threshold. ■ 1: The voltage on VBUS is above the OTG Device Session Valid threshold. ■ 0: The voltage on VBUS is below the OTG Device Session Valid threshold. Value After Reset: 0x0

2.6.2.21 USB_TEST_REG0

- Description: USB test register 0
- Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	USB_TEST_REG0	RW	USB test register 0 Value After Reset: 0x0

2.6.2.22 USB_TEST_REG1

- Description: USB test register 1
- Offset: 0x54
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	USB_TEST_REG1	RW	USB test register 1 Value After Reset: 0x0

2.6.2.23 USB_TEST_REG2

- Description: USB test register 2
- Offset: 0x58
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	USB_TEST_REG2	RW	USB test register 2 Value After Reset: 0xFFFFFFFF

2.6.2.24 USB_TEST_REG3

- Description: USB test register 3
- Offset: 0x5c
- Default Value: 0xffffffff

Bits	Field Name	Access	Description
[31:0]	USB_TEST_REG3	RW	USB test register 3 Value After Reset: 0xFFFFFFFF

3 MPJTAG

3.1 Overview

Multi-Processor JTAG (MPJTAG) is designed to supports the debugging of multiple CPU cores in the SoC. The JTAG debug interfaces of multiple CPU cores are aggregated into a JTAG interface through MUX. A debugger is used externally to debug multiple CPU cores in the SoC. Only one CPU core can be debugged at a time.

The TAP controller in the MPJTAG module has a standard JTAG FSM for accepting JTAG port commands and updating internal registers. These registers include MUX select register, some control and status registers, and system descriptor registers. The system descriptor describes CPU core information in the current SoC, such as the number of CPUs, the number of cores in each CPU, and the status of the debug interface.

The structure of the MPJTAG module is shown in Figure & Table 3-1:

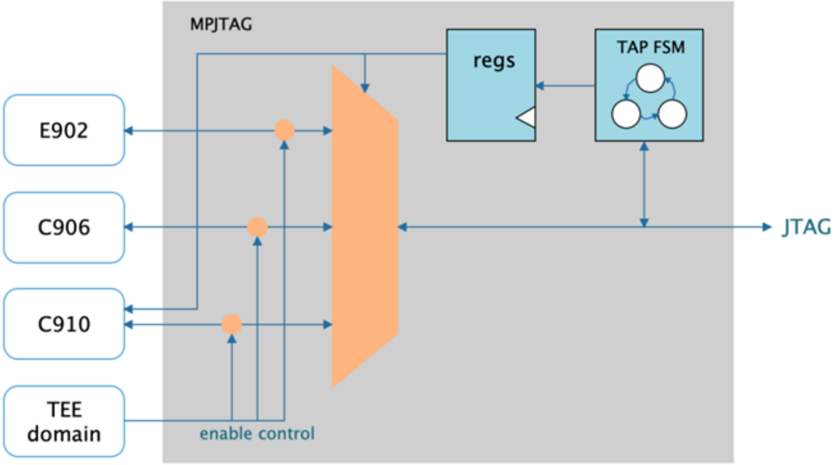

Figure & Table 3-1 MPJTAG function block diagram

3.2 Main Features

MPJTAG is used for CPU debugging and has the following features:

- Supports simultaneous debugging of E902, C906, and C910
- The C910 TEE core and C910 REE core can be debugged separately or in parallel
- Let the debugger obtain the CPU model parameters in the SoC in case of CPU power failure

3.3 Interface

Figure & Table 3-2 Pin description table

Pin Name	Direction	Width	Description
CPU_JTG_TCLK	I	1	JTAG test clock input

Pin Name	Direction	Width	Description
CPU_JTG_TMS	I	1	JTAG test mode select
CPU_JTG_TDI	I	1	JTAG test data input
CPU_JTG_TDO	O	1	JTAG test data output
CPU_JTG_TRST	I	1	JTAG test reset input, active low

CPU_JTG_TCLK is a clock signal generated by the external debugger. CPU_JTG_TMS and CPU_JTG_TDI serve as input interfaces of MPJTAG and sample on the rising edge of CPU_JTG_TCLK. CPU_JTG_TDO serves as the output interface and is set on the falling edge of CPU_JTG_TCLK. The timing characteristics of MPJTAG interfaces are as follows:

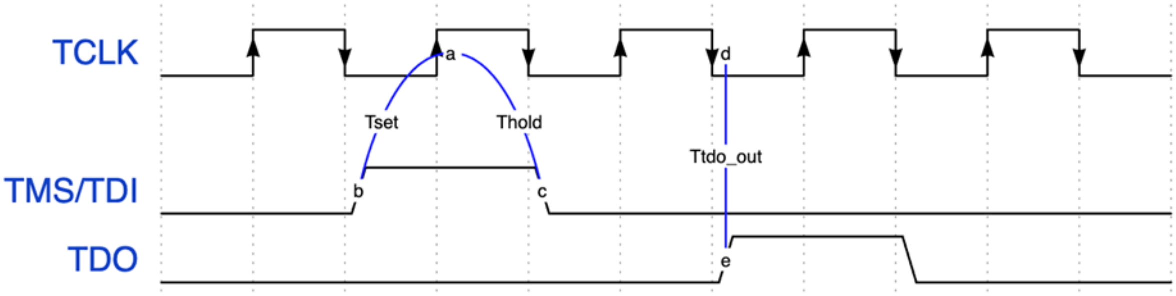

Figure & Table 3-3 MPJTAG timing diagram

Figure & Table 3-4 MPJTAG timing characteristics

Symbol	Parameter	Min	Max	Unit
fTCLK	TCLK clock frequency	1	24000	kHz
Tset	TDI, TMS setup time before rising TCK	21	--	ns
Thold	TDI, TMS hold time after rising TCK	21	--	ns
Ttdo_out	TDO output delay time from falling TCK	1	16	ns

3.4 Function Description

MPJTAG mainly has the following two functions: logging SoC information and selecting debug path for CPU core.

3.4.1 SoC Information

A set of system descriptor read-only registers in MPJTAG are used to describe information of each CPU core in the SoC, such as CPU model, CPU ID, and CPU JTAG enable. These registers are not mapped to the MPJTAG register list, but indirectly accessed using SD_ADDR and SD_DATA registers. Each set of registers are organized using the secondary index, as shown in Figure & Table 3-5.

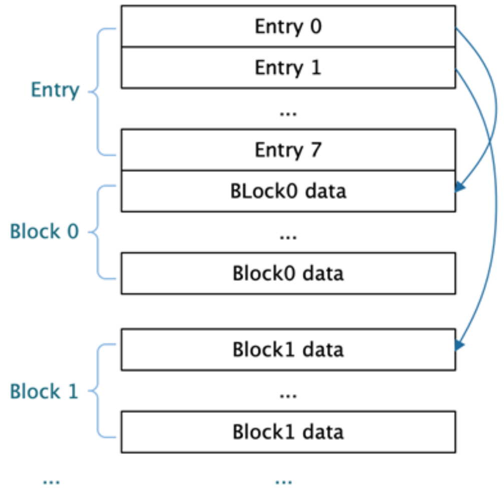

Figure & Table 3-5 System descriptor register map

The Entry storage area needs to be continuous. Each Entry contains 32 bits. The upper 28 bits is the address pointing to the block. Bit [0] is Exists, indicating whether the block exists. The Entry area ends with a value of all 0s. The Entry format is as follows:

31:4	3:1	0
INDEX	RESERVED	EXISTS

The Block register group consists of header and contents, where the header is 4 bytes and stores Magic, Vendor ID, SD ID and Version.

- Magic is a fixed value to ensure the credibility of the descriptor module.
- Vendor ID indicates the supplier using the system descriptor module.
- SD ID indicates the contents of the module.
- Version refers to the version information of the specified SD ID, that is, SD ID plus Version indicates the content and format of the information saved in the contents.

31:28	27:16	15:4	3:0
Magic (0x9)	Vendor(0x5B7)	SD_ID (0x0)	Version (0x0)

Contents are related to SD IDs. Different IDs correspond to different contents. Currently only ID 0 is used, indicating CPU and information.

31:27	26:23	22:19	18:15	14:10	9	8	7:0
CPI_INDX	CORE_ID	GROUP	CLASTER	POWER_DOMAIN	TEE	JTAG_EN	RESERVED
MISA[31:0]							
MISA[63:32]							
CPUID 0							
CPUID 1							
CPUID 2							

31:27	26:23	22:19	18:15	14:10	9	8	7:0
CPUID 3							
CPUID 4							
CPUID 5							
CPUID 6							

3.4.2 CPU Core Select

MPJTAG manages the connection and disconnection between the three CPU cores in the SoC and the external JTAG interface. The registers in MPJTAG are also updated through the JTAG interface. In order to support the communication of the three CPU cores and MPJTAG internal registers with the JTAG interface, MPJTAG is designed with a CPUSEL register. Each bit in the CPUSEL register is used to select a CPU core. When CPUSEL is 0, it means that no CPU core is selected. In this case, the external debugger can operate the registers in MPJTAG, including the CPUSEL register.

31:3	2	1	0
RESERVED	C910_SEL	C906_SEL	E902_SEL

3.5 Register Description

3.5.1 Register Memory Map

Name	JTAG Address	CPU Access Address	Width	JTAG RW	CPU RW	Default Value	Description	Section/Page
HACR	-	-	16	R/W	-	0x8200	Debug controller command register	3.5.2.1/161
DBGID	5'b00010	-	32	RO	-	0x1000301	Debug controller ID register	3.5.2.2/161
CPUSEL	5'b11010	-	32	R/W	-	0x0	Multi-core CPU select register	3.5.2.3/162
CPUST	5'b11011	-	32	RO	-	0x0	Multi-core CPU status register	
SD_ADDR	5'b11100	-	32	RW	-	0x0	System descriptor address select register	3.5.2.4/162
SD_DATA	5'b11101	-	32	RO	-	0x0	System descriptor data read register	3.5.2.5/162
HCR	5’b01101	0xFFFF019180	32	RW	RW	0x0	MPJTAG control register	3.5.2.6/163
EHSR	5’b01111	0xFFFF019184	32	RO	RO	0x0	MPJTAG status register	3.5.2.7/163

3.5.2 Register and Field Description

3.5.2.1 HACR

- Description: This register is equivalent to the IR register in JTAG, and updated in the Shift_IR and Update_IR states of TAP FSM.
- Offset: 0x0
- Default Value: 0x8200

Bits	Field Name	Access	Description
[7:0]	RESERVED_1	-	
[12:8]	RS	RW	RS[4:0]: Register select, pointing to the register of this JTAG operation
[14:13]	RESERVED_2	-	
[15]	R/W	RW	R/W: Indicates whether this JTAG operation is read or write. 0: Write operation 1: Read operation
[31:16]	RESERVED_3	-	

3.5.2.2 DBGID

- Description: MPJTAG ID register for external debugger identification, not accessible by CPU
- Offset: 0x2
- Default Value: 0x10c0322

Bits	Field Name	Access	Description
[3:0]	ID_VER	RO	Version defined by the bit field of this DBGID register
[7:4]	ISA_VER	RO	CPU instruction set type in SoC
[12:8]	CPU_CNT	RO	The number of CPU cores in SoC
[17:13]	RESERVED_1	-	
[18]	HACR16	RO	The JTAG IR register in MPJTAG, the width of the HACR register 0x0: HACR is 8bit width. 0x1: HACR is 16bit width.
[19]	HAS_SD	RO	The default is 1, indicating that there are system descriptor registers in MPJTAG.
[23:20]	RESERVED_2	-	

Bits	Field Name	Access	Description
[25:24]	MARK	RO	MPJTAG flag, indicating whether this ID register is the ID register in CPU or the ID register in MPJTAG. 0x0: HAD ID register in CPU core 0x1: DBGID register in MPJTAG
[27:26]	RESERVED_3	-	
[31:28]	CDI_TYPE	RO	Debug interface type. The default is 0, which means JTAG interface.

3.5.2.3 CPUSEL

- Description: CPU channel select, one-hot encoding, each bit corresponds to a CPU core, not accessible by CPU
- Offset: 0x1A
- Default Value: 0x0

Bits	Field Name	Access	Description
[0]	C910_SEL	RW	C910 CPU JTAG debug channel select
[1]	C906_SEL	RW	C906 CPU JTAG debug channel select
[2]	E902_SEL	RW	E902 CPU JTAG debug channel select
[31:3]	RESERVED_1	-	

3.5.2.4 SD_ADDR

- Description: System descriptor register address select, not accessible by CPU
- Offset: 0x1C
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SD_ADDR	RW	System descriptor register address select, automatic accumulation after reading SD_DATA

3.5.2.5 SD_DATA

- Description: System descriptor register data, not accessible by CPU
- Offset: 0x1D
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	SD_DATA	RO	System descriptor register data

3.5.2.6 HCR

- Description: MPJTAG control register, readable and writable by CPU
- Offset: 0x0D for JTAG, 0xFFFF019180 for CPU
- Default Value: 0x0

Bits	Field Name	Access	Description
[17:0]	RESERVED_1	-	
[18]	JW_INT_EN	RW	External debugger write data interrupt enable
[19]	JR_INT_EN	RW	External debugger read data interrupt enable
[31:20]	RESERVED_2	-	

3.5.2.7 EHSR

- Description: MPJTAG status register, readable by CPU
- Offset: 0x0F for JTAG, 0xFFFF019184 for CPU
- Default Value: 0x0

Bits	Field Name	Access	Description
[15:0]	RESERVED_1	-	
[16]	J2C_DATA_VLD	RO	Data in the JTAG2CPU register is valid.
[17]	C2J_DATA_VLD	RO	Data in the CPU2JTAG register is valid.
[18]	JW_INT_ST	RO	External debugger write data interrupt status is valid.
[19]	JR_INT_ST	RO	External debugger read data interrupt status is valid.
[31:20]	RESERVED_2	-	

3.5.2.8 System Descriptor

Addr	Entry/Block	Reg Name	Default Value	Description
0x0	Entries	ENTRY0	0x00000081	Block 0 start address, and Block 0 data is valid.
0x1		ENTRY1	0x00000131	Block 1 start address, and Block 1 data is valid.
0x2		ENTRY2	0x000001E1	Block 2 start address, and Block 2 data is valid.
0x3		ENTRY3	0x00000291	Block 3 start address, and Block 3 data is valid.
0x4		ENTRY4	0x00000341	Block 4 start address, and Block 4 data is valid.
0x5		ENTRY5	0x000003F1	Block 5 start address, and Block 5 data is valid.

Addr	Entry/Block	Reg Name	Default Value	Description
0x6		ENTRY6	0x00000000	Block 6 start address, and Block 6 data is valid.
0x7		RESERVED	0x00000000	-
0x8	System Descriptor Block 0	BLOCK_HEADER	0x95B70000	Block header
0x9		CPU_ST	0x00000500	CPU and CPU core number and status
0xA		MISA[31:0]	0x40101014	CPU machine mode processor instruction set features, lower 32 bits
0xB		MISA{63:32]	0x00000000	CPU machine mode processor instruction set features, upper 32 bits
0xC		CPUID0	0x0804000D	CPU ID 0
0xD		CPUID1	0x12080000	CPU ID 1
0xE		CPUID2	0x2420F038	CPU ID 2
0xF		CPUID3	0x00000000	CPU ID 3
0x10		CPUID4	0x00000000	CPU ID 4
0x11		CPUID5	0x00000000	CPU ID 5
0x12		CPUID6	0x00000000	CPU ID 6
0x13	System Descriptor Block 1	BLOCK_HEADER	0x95B70000	Block header
0x14		CPU_ST	0x08000900	CPU and CPU core number and status
0x15		MISA[31:0]	0x00B4112D	CPU machine mode processor instruction set features, lower 32 bits
0x16		MISA{63:32]	0x80000000	CPU machine mode processor instruction set features, upper 32 bits
0x17		CPUID0	0x0910090D	CPU ID 0
0x18		CPUID1	0x12006000	CPU ID 1
0x19		CPUID2	0x260C0001	CPU ID 2
0x1A		CPUID3	0x30030066	CPU ID 3
0x1B		CPUID4	0x42180000	CPU ID 4
0x1C		CPUID5	0x50000000	CPU ID 5
0x1D		CPUID6	0x60000853	CPU ID 6
0x1E	System	BLOCK_HEADER	0x95B70000	Block header

Addr	Entry/Block	Reg Name	Default Value	Description
0x1F	Descriptor Block 2	CPU_ST	0x10080F00	CPU and CPU core number and status
0x20		MISA[31:0]	0x00B4112D	CPU machine mode instruction set features, lower 32 bits
0x21		MISA{63:32]	0x80000000	CPU machine mode processor instruction set features, upper 32 bits
0x22		CPUID0	0x090C090D	CPU ID 0
0x23		CPUID1	0x110C9000	CPU ID 1
0x24		CPUID2	0x260C0001	CPU ID 2
0x25		CPUID3	0x30530077	CPU ID 3
0x26		CPUID4	0x42080407	CPU ID 4
0x27		CPUID5	0x50000003	CPU ID 5
0x28		CPUID6	0x60000A53	CPU ID 6
0x29	System Descriptor Block 3	BLOCK_HEADER	0x95B70000	Block header
0x2A		CPU_ST	0x10880F00	CPU and CPU core number and status
0x2B		MISA[31:0]	0x00B4112D	CPU machine mode processor instruction set features, lower 32 bits
0x2C		MISA{63:32]	0x80000000	CPU machine mode processor instruction set features, upper 32 bits
0x2D		CPUID0	0x090C090D	CPU ID 0
0x2E		CPUID1	0x110C9000	CPU ID 1
0x2F		CPUID2	0x260C0001	CPU ID 2
0x30		CPUID3	0x30530077	CPU ID 3
0x31		CPUID4	0x42080407	CPU ID 4
0x32		CPUID5	0x50000003	CPU ID 5
0x33		CPUID6	0x60000A53	CPU ID 6
0x34	System Descriptor Block 4	BLOCK_HEADER	0x95B70000	Block header
0x35		CPU_ST	0x11080F00	CPU and CPU core number and status
0x36		MISA[31:0]	0x00B4112D	CPU machine mode processor instruction set features, lower 32 bits
0x37		MISA{63:32]	0x80000000	CPU machine mode processor instruction set

Addr	Entry/Block	Reg Name	Default Value	Description
				features, upper 32 bits
0x38		CPUID0	0x090C090D	CPU ID 0
0x39		CPUID1	0x110C9000	CPU ID 1
0x3A		CPUID2	0x260C0001	CPU ID 2
0x3B		CPUID3	0x30530077	CPU ID 3
0x3C		CPUID4	0x42080407	CPU ID 4
0x3D		CPUID5	0x50000003	CPU ID 5
0x3E		CPUID6	0x60000A53	CPU ID 6
0x3F	System Descriptor Block 5	BLOCK_HEADER	0x95B70000	Block header
0x40		CPU_ST	0x11880F00	CPU and CPU core number and status
0x41		MISA[31:0]	0x00B4112D	CPU machine mode processor instruction set features, lower 32 bits
0x42		MISA{63:32]	0x80000000	CPU machine mode processor instruction set features, upper 32 bits
0x43		CPUID0	0x090C090D	CPU ID 0
0x44		CPUID1	0x110C9000	CPU ID 1
0x45		CPUID2	0x260C0001	CPU ID 2
0x46		CPUID3	0x30530077	CPU ID 3
0x47		CPUID4	0x42080407	CPU ID 4
0x48		CPUID5	0x50000003	CPU ID 5
0x49		CPUID6	0x60000A53	CPU ID 6

3.6 Usage

3.6.1 Read System Descriptor Registers

System Descriptor registers cannot be read directly. They need to be read indirectly through the SD_ADDR and SD_DATA registers: First set the SD_ADDR register to point to the address of the System Descriptor register to be read, then read the SD_DATA register to get the value of the corresponding System Descriptor register. The SD_ADDR register automatically accumulates, if you continue to read the SD_DATA register, the value of the next System Descriptor register will be read. If you want to traverse all System Descriptor registers, read as follows:

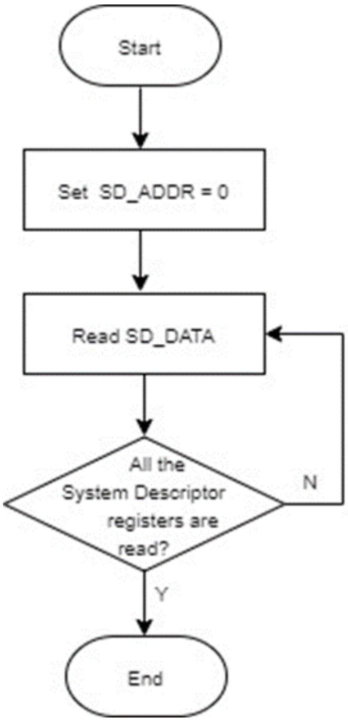

Figure & Table 3-6 System descriptor read flow chart

4 ADC

4.1 Overview

ADC can convert the external analog signal into a certain proportion of digital value, so as to realize the measurement of analog signal, which can be applied to voltage measurement, key detection and so on. ADC module includes ADC controller and PHY. The controller supports one APB slave bus interface to configuration register. ADC module is a power and area optimized successive-approximation ADC, having the resolution selectable between 12/10/8 and 6 bit. ADC supports 8 independent single-ended channels.

4.2 Main Features

The main features which supported by ADC module are as below:

- Supports selectable 12/10/8/6 bit resolution
- Supports max 2.63MSPS conversion rate (12bit, main clock: 73.728MHz)
- Supports 8 independent single-ended inputs
- 1.8V analog power supply, 0.8V digital power supply, 0~1.8V input full-scale range voltage
- Typical 12bit Signal-to-Noise and Distortion Ratio (SINAD) 62.5dB (TBD)
- Supports internal bandgap and reference voltage buffer
- Supports one_shot and continuous mode
- Supports interruption reporting of abnormal sampling values

4.3 Interface

The PAD of the ADC is described in the following Figure & Table 4-1:

Figure & Table 4-1 ADC PAD description table

Pin Name	Direction	Width	Description
ADC_DISLVL	IO	1	No digital supply This signal must be asserted high, when avddhv is present but dvdd is not within the specified range (for example during system startup). This sets the interface between internal blocks to a known state, preventing current consumption on the analog supply (avddhv). To set the module into deep power down mode, this signal should be asserted high (with enadc and selbg = 1'b0). Note: This input signal must have 1.8 V level (avddhv).
ADC_VREF	IO	1	Positive reference voltage, when selref=1'b0

Pin Name	Direction	Width	Description
ADC_AGNDREF	IO	1	Negative reference voltage Must be connected to analog ground.
ADC_VIN_CH0_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH0_P are the signal inputs.
ADC_VIN_CH1_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH1_P are the signal inputs.
ADC_VIN_CH2_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH2_P are the signal inputs.
ADC_VIN_CH3_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH3_P are the signal inputs.
ADC_VIN_CH4_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH4_P are the signal inputs.
ADC_VIN_CH5_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH5_P are the signal inputs.
ADC_VIN_CH6_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH6_P are the signal inputs.
ADC_VIN_CH7_P	IO	1	In single ended input mode (seldiff = 1’b0), ADC_VIN_CH7_P are the signal inputs.
ADC_VBG	IO	1	External voltage reference for built-in reference buffer, when selbg = 1’b0 and selref = 1’b1

4.4 Function Description

The functional logic diagram of ADC is as Figure & Table 4-2. The ADC Top includes one ADC_T12_registers, one CLK_GEN, one CTRL_TX, one CTRL_RX, and one ADC PHY.

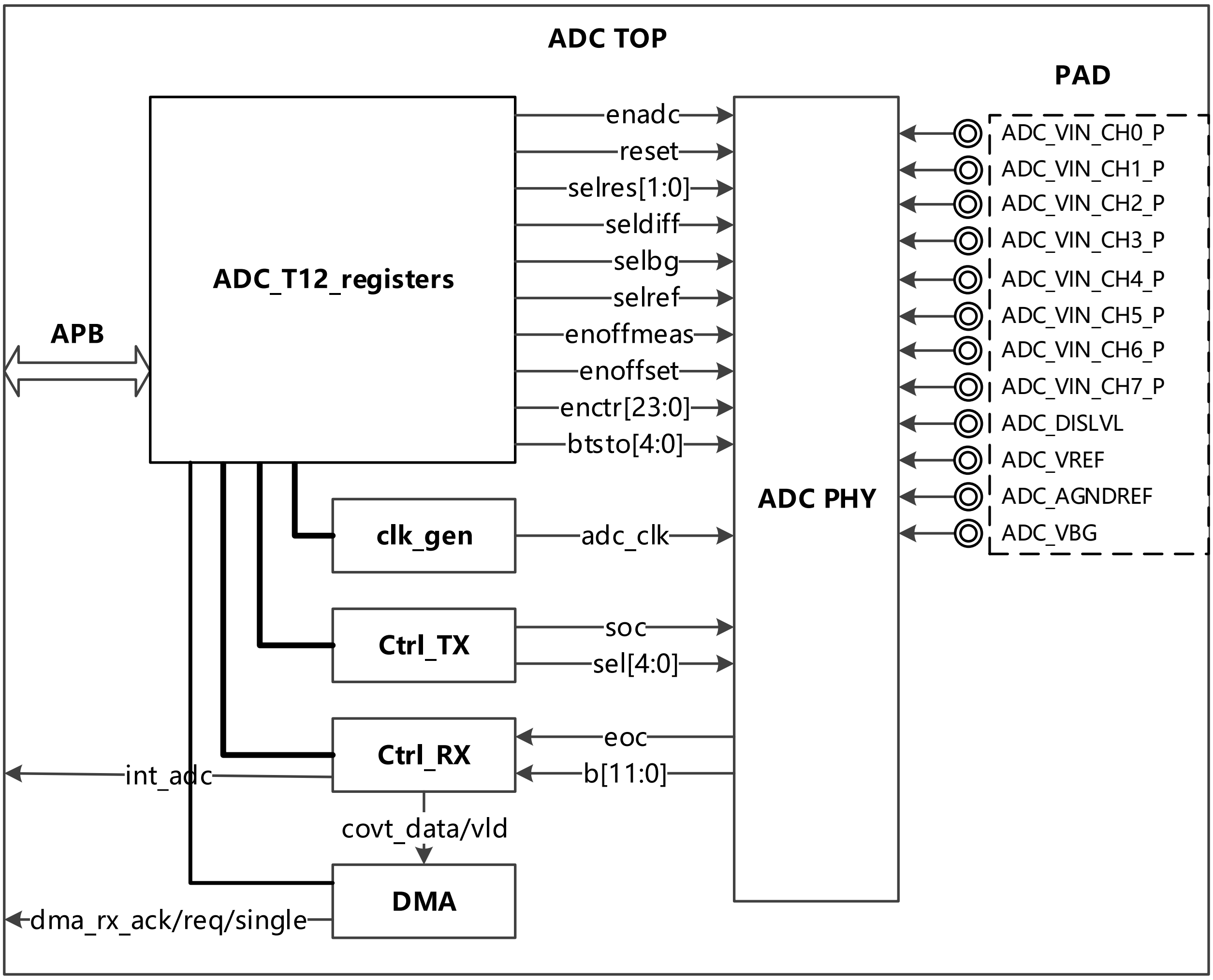

Figure & Table 4-2 Functional logic diagram

4.5 Usage

4.5.1 Clock and Reset

These clock and reset initialization process should be configured before ADC controller initialization:

1. Configure the ADC clock registers to open apb_pclk.
2. Configure the ADC reset registers to deassert apb_presetn.
3. Initialize ADC registers to start conversion.

4.5.2 Initialization and Operation

The software initializes the ADC by controlling the following registers：

- ADC_PHY_CFG/ADC_PHY_TEST: Used to control ADC marco’s working mode.
  Note: TH1520’s ADC only supports single ended inputs.
  adc_phy_enctr need change to 0x8E0 for ADC ‘s SPEC.

- ADC_OP_CTRL/ADC_OP_SINGLE_START/ADC_FCLK_CTRL/ADC_START_TIME/ADC_SAMPLE_TIME: Used to control operation mode, enable channels, enable DMA and fclk 's frequency and phase and sampling rate.
  Note: Please follow the register description.
- ADC_SAMPLE_DATA: Used to access sample data from ADC.
  Note: The sampled data follows the following data format:

	31	30：28	27：16	15	14：12	11：0
Continous mode	**Vld**	**Ch**	**Data1[11:0]**	**Vld**	**Ch**	**Data0[11:0]**
Single mode	**0**	**0**	**0**	**Vld**	**Ch**	**Data0[11:0]**

Figure & Table 4-3 ADC sampled data format diagram

- ADC_INT_*_MASK/ADC_INT_*_STATUS/ADC_INT_*_VALUE_*/ADC_DFX_SOC_CNT_*: Used to control generate interrupt and DFx.
  Note: ADC supports two types of interrupts:
  - Actual interrupt: When same channel's adc_int_actual_mask_vect[i] is unmask (1'b0), the sample data's value smaller than adc_int_actual_lvalue or the sample data's value larger than adc_int_actual_hvalue, then the channel generates an interrupt (adc_int_actual_st).
  - Delta interrupt: When same channel's adc_int_delta_mask_vect[i] is unmask (1'b0), the sample data's difference between the last measured value and this measured value is greater than adc_int_delta_value, then the channel generates an interrupt (adc_int_delta_st).

4.5.3 Offset Measurement

The ADC has no offset compensation mechanism. However, it allows for its offset to be measured. Offset can be measured at bottom scale for single ended mode. During offset measurement, the conversion happens on the same manner as regular operation, only sampling is affected. Both continuous and single conversion modes are supported.

- To enter ADC’s offset measurement mode, set ADC_PHY_CTRL. ADC_PHY_ENOFFMEAS to 1’b1.
- Set the ADC_OP_CTRL. ADC_CH_EN_VECT to 8’h1.
- Set ADC_PHY_CTRL. ADC_PHY_ENOFFSET to 1’b1 (The expected added offset is 256 LSB for 12bit resolution).
- The offset value is read from ADC_SMP_DATA’s ADC conversion data.

Note: Ideal offset code (with ADC_PHY_ENOFFSET) is bottom-scale (12’h256). If offset value is smaller than 12’h256, the offset can be negative. In this case, ADC_PHY_CTRL. ADC_PHY_ENOFFSET must remain 1’b1 during normal operation. Due to noise concern, the offset measurement requires the average of several samples. The use of at least 8 is recommended.

4.6 Register Description

4.6.1 Register Memory Map

Register	Offset	Description	Section/Page
ADC_PHY_CFG	0x0	The selbg and selref control signals must remain unchanged after a startup sequence. A new startup sequence must be made for any change in these control signals.	4.6.2.1/174
ADC_PHY_CTRL	0x4	Used to control the ADC's enable and reset	4.6.2.2/175
ADC_PHY_TEST	0x8	Used to control the ADC's test. Synopsys internal use only.	4.6.2.3/176
ADC_OP_CTRL	0xC	Used to control the ADC's operation mode, enable channels, and enable DMA.	4.6.2.4/176
ADC_OP_SINGLE_START	0x10	In single mode, used to start a conversion	4.6.2.5/177
ADC_FCLK_CTRL	0x14	Used to control fclk 's frequency and phase	4.6.2.6/177
ADC_START_TIME	0x18	Used to control ADC's init time for ADC phy's SPEC.	4.6.2.7/178
ADC_SAMPLE_TIME	0x1C	Used to set ADC sampling rate.	4.6.2.8/179
ADC_SAMPLE_DATA	0x20	Used to get ADC sample data	4.6.2.9/179
ADC_INT_ACTUAL_MASK	0x50	Used to set actual interrupt mask. 1'b1: Mask the actual interrupt. 1'b0: Unmask the actual interrupt. Actual interrupt: When same channel's adc_int_actual_mask_vect[i] is unmask (1'b0), the sample data's value smaller than adc_int_actual_lvalue or the sample data's value larger than adc_int_actual_hvalue, then the channel generates an interrupt (adc_int_actual_st).	4.6.2.10/179
ADC_INT_DELTA_MASK	0x54	Used to set delta interrupt mask. 1'b1: Mask the delta interrupt. 1'b0: Unmask the delta interrupt. Delta interrupt: When same channel's adc_int_delta_mask_vect[i] is unmask (1'b0), the sample data's difference	4.6.2.11/180

Register	Offset	Description	Section/Page
		between the last measured value and this measured value is greater than adc_int_delta_value, then the channel generates an interrupt (adc_int_delta_st).	
ADC_INT_ACTUAL_STATUS	0x58	Actual interrupt status 1'b1: The actual interrupt valid. 1'b0: The actual interrupt invalid.	4.6.2.12/180
ADC_INT_DELTA_STATUS	0x5C	Delta interrupt status 1'b1: The delta interrupt valid. 1'b0: The delta interrupt invalid	4.6.2.13/181
ADC_INT_ACTUAL_VALUE_CH0	0x60	Channel 0's actual interrupt's high and low value	4.6.2.14/182
ADC_INT_ACTUAL_VALUE_CH1	0x64	Channel 1's actual interrupt's high and low value	4.6.2.15/182
ADC_INT_ACTUAL_VALUE_CH2	0x68	Channel 2's actual interrupt's high and low value	4.6.2.16/183
ADC_INT_ACTUAL_VALUE_CH3	0x6C	Channel 3's actual interrupt's high and low value	4.6.2.17/183
ADC_INT_ACTUAL_VALUE_CH4	0x70	Channel 4's actual interrupt's high and low value	4.6.2.18/183
ADC_INT_ACTUAL_VALUE_CH5	0x74	Channel 5's actual interrupt's high and low value	4.6.2.19/184
ADC_INT_ACTUAL_VALUE_CH6	0x78	Channel 6's actual interrupt's high and low value	4.6.2.20/184
ADC_INT_ACTUAL_VALUE_CH7	0x7C	Channel 7's actual interrupt's high and low value	4.6.2.21/185
ADC_INT_DELTA_VALUE_CH0	0x90	Channel 0's delta interrupt's high and low value	4.6.2.22/185
ADC_INT_DELTA_VALUE_CH1	0x94	Channel 1's delta interrupt's high and low value	4.6.2.23/185
ADC_INT_DELTA_VALUE_CH2	0x98	Channel 2's delta interrupt's high and low value	4.6.2.24/186
ADC_INT_DELTA_VALUE_CH3	0x9C	Channel 3's delta interrupt's high and low value	4.6.2.25/186
ADC_INT_DELTA_VALUE_CH4	0xA0	Channel 4's delta interrupt's high and low	4.6.2.26/186

Register	Offset	Description	Section/Page
		value	
ADC_INT_DELTA_VALUE_CH5	0xA4	Channel 5's delta interrupt's high and low value	4.6.2.27/187
ADC_INT_DELTA_VALUE_CH6	0xA8	Channel 6's delta interrupt's high and low value	4.6.2.28/187
ADC_INT_DELTA_VALUE_CH7	0xAC	Channel 7's delta interrupt's high and low value	4.6.2.29/188
ADC_DFX_SOC_CNT_CH0	0xC0	Channel 0's soc counter value	4.6.2.30/188
ADC_DFX_EOC_CNT_CH0	0xC4	Channel 0's eoc counter value	4.6.2.31/188
ADC_DFX_SOC_CNT_CH1	0xC8	Channel 1's soc counter value	4.6.2.32/188
ADC_DFX_EOC_CNT_CH1	0xCC	Channel 1's eoc counter value	4.6.2.33/189
ADC_DFX_SOC_CNT_CH2	0xD0	Channel 2's soc counter value	4.6.2.34/189
ADC_DFX_EOC_CNT_CH2	0xD4	Channel 2's eoc counter value	4.6.2.35/189
ADC_DFX_SOC_CNT_CH3	0xD8	Channel 3's soc counter value	4.6.2.36/189
ADC_DFX_EOC_CNT_CH3	0xDC	Channel 3 's eoc counter value	4.6.2.37/190
ADC_DFX_SOC_CNT_CH4	0xE0	Channel 4's soc counter value	4.6.2.38/190
ADC_DFX_EOC_CNT_CH4	0xE4	Channel 4's eoc counter value	4.6.2.39/190
ADC_DFX_SOC_CNT_CH5	0xE8	Channel 5's soc counter value	4.6.2.40/191
ADC_DFX_EOC_CNT_CH5	0xEC	Channel 5's eoc counter value	4.6.2.41/191
ADC_DFX_SOC_CNT_CH6	0xF0	Channel 6's soc counter value	4.6.2.42/191
ADC_DFX_EOC_CNT_CH6	0xF4	Channel 6's eoc counter value	4.6.2.43/191
ADC_DFX_SOC_CNT_CH7	0xF8	Channel 7's soc counter value	4.6.2.44/192
ADC_DFX_EOC_CNT_CH7	0xFC	Channel 7's eoc counter value	4.6.2.45/192

4.6.2 Register and Field Description

4.6.2.1 ADC_PHY_CFG

- Description: The selbg and selref control signals must remain unchanged after a startup sequence. A new startup sequence must be made for any change in these control signals.
- Offset: 0x0
- Default Value: 0x1102

Bits	Name	Access	Description
[31:13]	RESERVED_4	-	
[12]	ADC_PHY_SELREF	RW	Selects the full-scale input range of the converter. 1'b1: Uses the internal reference generator. (default) 1'b0: Uses the voltage applied to vref. Value After Reset: 0x1
[11:9]	RESERVED_3	-	
[8]	ADC_PHY_SELBG	RW	Enables the internal bandgap reference voltage generator. 1'b1: Internal bandgap is active. The ADC_VBG pin is at high impedance. (default) 1'b0: Internal bandgap is in power-down. User should connect an external 1.2V voltage to vbg pin, if the built-in reference buffer is to be used. (ADC_PHY_SELREF = 1'b1) Value After Reset: 0x1
[7:5]	RESERVED_2	-	
[4]	ADC_PHY_SELDIFF	RW	Selects the ADC input mode. 1'b0: Single ended inputs (default) 1'b1: Differential input Value After Reset: 0x0
[3:2]	RESERVED_1	-	
[1:0]	ADC_PHY_SELRES	RW	Selects the ADC resolution. 2'h0: 6-bit mode 2'h1: 8-bit mode 2'h2: 10-bit mode (default) 2'h3: 12-bit mode Value After Reset: 0x2

4.6.2.2 ADC_PHY_CTRL

- Description: Used to control the ADC's enable and reset.
- Offset: 0x4
- Default Value: 0x0

Bits	Name	Access	Description
[31:13]	RESERVED_4	-	

Bits	Name	Access	Description
[12]	ADC_PHY_ENOFFSET	RW	Adds analog positive offset, default 1'b0 1'b1: Adds a positive offset on the analog input signal. 1'b0: Not add a positive offset on the analog input signal. Value After Reset: 0x0
[11:9]	RESERVED_3	-	
[8]	ADC_PHY_ENOFFMEAS	RW	Enables offset measurement 1'b1: Sample zero input 1'b0: Sample selected input (default) Value After Reset: 0x0
[7:5]	RESERVED_2	-	
[4]	ADC_PHY_RESET	RW	Abort conversions. Activating this signal will set the ADC to the sampling phase. Value After Reset: 0x0
[3:1]	RESERVED_1	-	
[0]	ADC_PHY_ENADC	RW	1'b0: ADC in power-down/standby mode. 1'b1: ADC in normal operation. Value After Reset: 0x0

4.6.2.3 ADC_PHY_TEST

- Description: Used to control the ADC’s test. Synopsys internal use only.
- Offset: 0x8
- Default Value: 0x0

Bits	Name	Access	Description
[31:29]	RESERVED_1	-	
[28:24]	ADC_PHY_BTSTO	RO	Testing interface Input. Synopsys internal use only. In normal operation, these signals should be tied low. Value After Reset: 0x0
[23:0]	ADC_PHY_ENCTR	RW	Testing interface output. Synopsys internal use only. Value After Reset: 0x0

4.6.2.4 ADC_OP_CTRL

- Description: Used to control the ADC's operation mode, enable channels, and enable DMA.

- Offset: 0xC
- Default Value: 0x10

Bits	Name	Access	Description
[31:20]	RESERVED_3	-	
[19:12]	ADC_CH_EN_VECT	RW	bit19: Channel 7 enable bit18: Channel 6 enable bit17: Channel 5 enable bit16: Channel 4 enable bit15: Channel 3 enable bit14: Channel 2 enable bit13: Channel 1 enable bit12: Channel 0 enable Value After Reset: 0x0
[11:5]	RESERVED_2	-	
[4]	ADC_DMA_ENABLE	RW	adc_dma_enable, used to enable ADC DMA ctrl. Value After Reset: 0x1
[3:1]	RESERVED_1	-	
[0]	ADC_OP_MODE	RW	1: Single mode 0: Continuous mode Value After Reset: 0x0

4.6.2.5 ADC_OP_SINGLE_START

- Description: In single mode, used to start a conversion.
- Offset: 0x10
- Default Value: 0x0

Bits	Name	Access	Description
[31:1]	RESERVED_1	-	
[0]	ADC_OP_SINGLE_START	W1S	In single mode, used to start a conversion for each channels that be enabled by adc_ch_en_vect. Value After Reset: 0x0

4.6.2.6 ADC_FCLK_CTRL

- Description: Used to control fclk's frequency and phase.
- Offset: 0x14
- Default Value: 0x10004

Bits	Name	Access	Description
[31:25]	RESERVED_3	-	
[24]	ADC_FCLK_INIT_VALUE	RW	Fclk ctrl reg's init value, used for debug. Value After Reset: 0x0
[23:22]	RESERVED_2	-	
[21:16]	ADC_FCLK_PHASE_SEL	RW	Fclk ctrl reg's phase select, used for debug. Value After Reset: 0x1
[15:7]	RESERVED_1	-	
[6:0]	ADC_FCLK_DIV	RW	Fclk = (0.7~70MHz), div to 0.7MHz use coreclk 73.728MHz = 105 = 0x69 Typ FCLK = coreclk/4 = 73.728/4 = 18.432MHz Must not use (0, 1, 3, 5, 7, 9), this are Invalid configuration for clock duty cycle (45%~55%). Value After Reset: 0x4

4.6.2.7 ADC_START_TIME

- Description: Used to control ADC's init time for ADC PHY's SPEC.
- Offset: 0x18
- Default Value: 0x160

Bits	Name	Access	Description
[31:9]	RESERVED_1	-	
[8:0]	ADC_START_TIME	RW	Fclk = (0.7~70MHz), cnt 5us@70MHz = 350 = 0x15E 1. When the ADC is moving from power down mode into normal operation with internal reference, it is needed to wait the defined power up time (tpup = 5us) before starting the conversion cycle. 2. When the ADC is moving from standby mode into normal operation with internal reference, it is needed to wait the defined wake up time (twup = 1.5us) before starting the conversion cycle. 3. When the ADC is moving from power down mode into normal operation with external reference, it is needed to wait the defined ADC Enable time (tenadc = 5 clk cycles) before starting the conversion cycle. Value After Reset: 0x160

4.6.2.8 ADC_SAMPLE_TIME

- Description: Used to set ADC sampling rate.
- Offset: 0x1C
- Default Value: 0x10

Bits	Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	ADC_SAMPLE_TIME	RW	Used to set ADC sampling rate. ADC Sampling Rate = Fclk/(1 + adc_sample_time) Value After Reset: 0x10

4.6.2.9 ADC_SAMPLE_DATA

- Description: Used to get ADC sample data.
- Offset: 0x20
- Default Value: 0x0

Bits	Name	Access	Description
[31:0]	ADC_SMP_DATA	RO	In single mode: bit[31:16]: Reserved bit[15]: Data valid bit[14:12]: Channel number bit[11:0]: ADC conversion data In continuous mode: bit[31]: Data valid bit[30:28]: Channel number bit[27:16]: ADC conversion data bit[15]: Data valid bit[14:12]: Channel number bit[11:0]: ADC conversion data Value After Reset: 0x0

4.6.2.10 ADC_INT_ACTUAL_MASK

- Description: Used to set actual interrupt mask. 1'b1: mask the actual interrupt. 1'b0: Unmask the actual interrupt. Actual interrupt: When same channel's adc_int_actual_mask_vect[i] is unmask (1'b0), the sample data's value smaller than adc_int_actual_lvalue or the sample data's value larger than adc_int_actual_hvalue, then the channel generates an interrupt (adc_int_actual_st).

- Offset: 0x50
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	ADC_INT_ACTUAL_MASK_VECT	RW	bit7: Channel 7 actual interrupt mask bit6: Channel 6 actual interrupt mask bit5: Channel 5 actual interrupt mask bit4: Channel 4 actual interrupt mask bit3: Channel 3 actual interrupt mask bit2: Channel 2 actual interrupt mask bit1: Channel 1 actual interrupt mask bit0: Channel 0 actual interrupt mask Value After Reset: 0x0

4.6.2.11 ADC_INT_DELTA_MASK

- Description: Used to set delta interrupt mask. 1'b1: Mask the delta interrupt. 1'b1: Unmask the delta interrupt. Delta interrupt: When same channel's adc_int_delta_mask_vect[i] is unmask (1'b0), the sample data's difference between the last measured value and this measured value is greater than adc_int_delta_value, then the channel generates an interrupt (adc_int_delta_st).
- Offset: 0x54
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	RESERVED_1	-	
[7:0]	ADC_INT_DELTA_MASK_VECT	RW	bit7: Channel 7 delta interrupt mask bit6: Channel 6 delta interrupt mask bit5: Channel 5 delta interrupt mask bit4: Channel 4 delta interrupt mask bit3: Channel 3 delta interrupt mask bit2: Channel 2 delta interrupt mask bit1: Channel 1 delta interrupt mask bit0: Channel 1 delta interrupt mask Value After Reset: 0x0

4.6.2.12 ADC_INT_ACTUAL_STATUS

- Description: Actual interrupt status. 1'b1: The actual interrupt valid. 1'b0: The actual interrupt invalid.

- Offset: 0x58
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	RESERVED_1	-	
[7]	ADC_INT_ACTUAL_ST_CH7	RC	Channel 7 actual interrupt status Value After Reset: 0x0
[6]	ADC_INT_ACTUAL_ST_CH6	RC	Channel 6 actual interrupt status Value After Reset: 0x0
[5]	ADC_INT_ACTUAL_ST_CH5	RC	Channel 5 actual interrupt status Value After Reset: 0x0
[4]	ADC_INT_ACTUAL_ST_CH4	RC	Channel 4 actual interrupt status Value After Reset: 0x0
[3]	ADC_INT_ACTUAL_ST_CH3	RC	Channel 3 actual interrupt status Value After Reset: 0x0
[2]	ADC_INT_ACTUAL_ST_CH2	RC	Channel 2 actual interrupt status Value After Reset: 0x0
[1]	ADC_INT_ACTUAL_ST_CH1	RC	Channel 1 actual interrupt status Value After Reset: 0x0
[0]	ADC_INT_ACTUAL_ST_CH0	RC	Channel 0 actual interrupt status Value After Reset: 0x0

4.6.2.13 ADC_INT_DELTA_STATUS

- Description: Delta interrupt status. 1'b1: The delta interrupt valid. 1'b0: The delta interrupt invalid.
- Offset: 0x5C
- Default Value: 0x0

Bits	Name	Access	Description
[31:8]	RESERVED_1	-	
[7]	ADC_INT_DELTA_ST_CH7	RC	Channel 7 delta interrupt status Value After Reset: 0x0
[6]	ADC_INT_DELTA_ST_CH6	RC	Channel 6 delta interrupt status Value After Reset: 0x0
[5]	ADC_INT_DELTA_ST_CH5	RC	Channel 5 delta interrupt status

Bits	Name	Access	Description
			Value After Reset: 0x0
[4]	ADC_INT_DELTA_ST_CH4	RC	Channel 4 delta interrupt status Value After Reset: 0x0
[3]	ADC_INT_DELTA_ST_CH3	RC	Channel 3 delta interrupt status Value After Reset: 0x0
[2]	ADC_INT_DELTA_ST_CH2	RC	Channel 2 delta interrupt status Value After Reset: 0x0
[1]	ADC_INT_DELTA_ST_CH1	RC	Channel 1 delta interrupt status Value After Reset: 0x0
[0]	ADC_INT_DELTA_ST_CH0	RC	Channel 0 delta interrupt status Value After Reset: 0x0

4.6.2.14 ADC_INT_ACTUAL_VALUE_CH0

- Description: Channel 0's actual interrupt's high and low value
- Offset: 0x60
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH0	RW	Channel 0's actual interrupt's high value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH0	RW	Channel 0's actual interrupt's low value Value After Reset: 0x0

4.6.2.15 ADC_INT_ACTUAL_VALUE_CH1

- Description: Channel 1's actual interrupt's high and low value
- Offset: 0x64
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH1	RW	Channel 1's actual interrupt's high value Value After Reset: 0x0

Bits	Name	Access	Description
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH1	RW	Channel 1's actual interrupt's low value Value After Reset: 0x0

4.6.2.16 ADC_INT_ACTUAL_VALUE_CH2

- Description: Channel 2's actual interrupt's high and low value
- Offset: 0x68
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH2	RW	Channel 2's actual interrupt's high value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH2	RW	Channel 2's actual interrupt's low value Value After Reset: 0x0

4.6.2.17 ADC_INT_ACTUAL_VALUE_CH3

- Description: Channel 3's actual interrupt's high and low value
- Offset: 0x6C
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH3	RW	Channel 3's actual interrupt's high value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH3	RW	Channel 3's actual interrupt's low value Value After Reset: 0x0

4.6.2.18 ADC_INT_ACTUAL_VALUE_CH4

- Description: Channel 4's actual interrupt's high and low value
- Offset: 0x70
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH4	RW	Channel 4's actual interrupt's high value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH4	RW	Channel 4's actual interrupt's low value Value After Reset: 0x0

4.6.2.19 ADC_INT_ACTUAL_VALUE_CH5

- Description: Channel 5's actual interrupt's high and low value
- Offset: 0x74
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH5	RW	Channel 5's actual interrupt's high value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH5	RW	Channel 5's actual interrupt's low value Value After Reset: 0x0

4.6.2.20 ADC_INT_ACTUAL_VALUE_CH6

- Description: Channel 6's actual interrupt's high and low value
- Offset: 0x78
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH6	RW	Channel 6's actual interrupt's high value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH6	RW	Channel 6's actual interrupt's low value Value After Reset: 0x0

4.6.2.21 ADC_INT_ACTUAL_VALUE_CH7

- Description: Channel 7's actual interrupt's high and low value
- Offset: 0x7C
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_ACTUAL_HVALUE_CH7	RW	Channel 7's actual interrupt's high value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_ACTUAL_LVALUE_CH7	RW	Channel 7's actual interrupt's low value Value After Reset: 0x0

4.6.2.22 ADC_INT_DELTA_VALUE_CH0

- Description: Channel 0's delta interrupt's high and low value
- Offset: 0x90
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH0	RW	Channel 0's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_DELTA_VALUE_CH0	RW	Channel 0's delta interrupt's delta value Value After Reset: 0x0

4.6.2.23 ADC_INT_DELTA_VALUE_CH1

- Description: Channel 1's delta interrupt's high and low value
- Offset: 0x94
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH1	RW	Channel 1's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	

Bits	Name	Access	Description
[11:0]	ADC_INT_DELTA_VALUE_CH1	RW	Channel 1's delta interrupt's delta value Value After Reset: 0x0

4.6.2.24 ADC_INT_DELTA_VALUE_CH2

- Description: Channel 2's delta interrupt's high and low value
- Offset: 0x98
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH2	RW	Channel 2's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_DELTA_VALUE_CH2	RW	Channel 2's delta interrupt's delta value Value After Reset: 0x0

4.6.2.25 ADC_INT_DELTA_VALUE_CH3

- Description: Channel 3's delta interrupt's high and low value
- Offset: 0x9C
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH3	RW	Channel 3's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_DELTA_VALUE_CH3	RW	Channel 3's delta interrupt's delta value Value After Reset: 0x0

4.6.2.26 ADC_INT_DELTA_VALUE_CH4

- Description: Channel 4's delta interrupt's high and low value
- Offset: 0xA0
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH4	RW	Channel 4's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_DELTA_VALUE_CH4	RW	Channel 4's delta interrupt's delta value Value After Reset: 0x0

4.6.2.27 ADC_INT_DELTA_VALUE_CH5

- Description: Channel 5's delta interrupt's high and low value
- Offset: 0xA4
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH5	RW	Channel 5's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_DELTA_VALUE_CH5	RW	Channel 5's delta interrupt's delta value Value After Reset: 0x0

4.6.2.28 ADC_INT_DELTA_VALUE_CH6

- Description: Channel 6's delta interrupt's high and low value
- Offset: 0xA8
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH6	RW	Channel 6's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_DELTA_VALUE_CH6	RW	Channel 6's delta interrupt's delta value Value After Reset: 0x0

4.6.2.29 ADC_INT_DELTA_VALUE_CH7

- Description: Channel 7's delta interrupt's high and low value
- Offset: 0xAC
- Default Value: 0x0

Bits	Name	Access	Description
[31:28]	RESERVED_2	-	
[27:16]	ADC_INT_DELTA_INIT_CH7	RW	Channel 7's delta interrupt's initial value Value After Reset: 0x0
[15:12]	RESERVED_1	-	
[11:0]	ADC_INT_DELTA_VALUE_CH7	RW	Channel 7's delta interrupt's delta value Value After Reset: 0x0

4.6.2.30 ADC_DFX_SOC_CNT_CH0

- Description: Channel 0's soc counter value
- Offset: 0xC0
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH0	RC	Channel 0's soc counter value Value After Reset: 0x0

4.6.2.31 ADC_DFX_EOC_CNT_CH0

- Description: Channel 0's eoc counter value
- Offset: 0xC4
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_EOC_CNT_CH0	RC	Channel 0's eoc counter value Value After Reset: 0x0

4.6.2.32 ADC_DFX_SOC_CNT_CH1

- Description: Channel 1's soc counter value
- Offset: 0xC8
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH1	RC	Channel 1's soc counter value Value After Reset: 0x0

4.6.2.33 ADC_DFX_EOC_CNT_CH1

- Description: Channel 1's eoc counter value
- Offset: 0xCC
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_EOC_CNT_CH1	RC	Channel 1's eoc counter value Value After Reset: 0x0

4.6.2.34 ADC_DFX_SOC_CNT_CH2

- Description: Channel 2's soc counter value
- Offset: 0xD0
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH2	RC	Channel 2's soc counter value Value After Reset: 0x0

4.6.2.35 ADC_DFX_EOC_CNT_CH2

- Description: Channel 2's eoc counter value
- Offset: 0xD4
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_EOC_CNT_CH2	RC	Channel 2's eoc counter value Value After Reset: 0x0

4.6.2.36 ADC_DFX_SOC_CNT_CH3

- Description: Channel 3's soc counter value

- Offset: 0xD8
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH3	RC	Channel 3's soc counter value Value After Reset: 0x0

4.6.2.37 ADC_DFX_EOC_CNT_CH3

- Description: Channel 3's eoc counter value
- Offset: 0xDC
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_EOC_CNT_CH3	RC	Channel 3's eoc counter value Value After Reset: 0x0

4.6.2.38 ADC_DFX_SOC_CNT_CH4

- Description: Channel 4's soc counter value
- Offset: 0xE0
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH4	RC	Channel 4's soc counter value Value After Reset: 0x0

4.6.2.39 ADC_DFX_EOC_CNT_CH4

- Description: Channel 4's eoc counter value
- Offset: 0xE4
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_EOC_CNT_CH4	RC	Channel 4's eoc counter value Value After Reset: 0x0

4.6.2.40 ADC_DFX_SOC_CNT_CH5

- Description: Channel 5's soc counter value
- Offset: 0xE8
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH5	RC	Channel 5's soc counter value Value After Reset: 0x0

4.6.2.41 ADC_DFX_EOC_CNT_CH5

- Description: Channel 5's eoc counter value
- Offset: 0xEC
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_EOC_CNT_CH5	RC	Channel 5's eoc counter value Value After Reset: 0x0

4.6.2.42 ADC_DFX_SOC_CNT_CH6

- Description: Channel 6's soc counter value
- Offset: 0xF0
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH6	RC	Channel 6's soc counter value Value After Reset: 0x0

4.6.2.43 ADC_DFX_EOC_CNT_CH6

- Description: Channel 6's eoc counter value
- Offset: 0xF4
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	

Bits	Name	Access	Description
[23:0]	ADC_DFX_EOC_CNT_CH6	RC	Channel 6's eoc counter value Value After Reset: 0x0

4.6.2.44 ADC_DFX_SOC_CNT_CH7

- Description: Channel 7's soc counter value
- Offset: 0xF8
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_SOC_CNT_CH7	RC	Channel 7's soc counter value Value After Reset: 0x0

4.6.2.45 ADC_DFX_EOC_CNT_CH7

- Description: Channel 7's eoc counter value
- Offset: 0xFC
- Default Value: 0x0

Bits	Name	Access	Description
[31:24]	RESERVED_1	-	
[23:0]	ADC_DFX_EOC_CNT_CH7	RC	Channel 7's eoc counter value Value After Reset: 0x0

5 I2S

5.1 Overview

The Inter-IC Sound (I2S) bus is a simple three-wire serial bus protocol developed by Philips to transfer stereo audio data. The bus only handles the transfer of audio data. This module is a component designed to be used in systems that process digital audio signals, such as:

- A/D and D/A converters
- Digital signal processors
- Error correction for compact disc and digital recording
- Digital filters
- Digital input/output interfaces

Currently, many digital audio systems are attracting the consumers on the market, in the form of compact discs, digital audio tapes, digital sound processors, and digital TV. The I2S bus interface can be used to connect to an external 8/16/24/32-bit stereo audio CODEC IC for minidisk and portable applications.

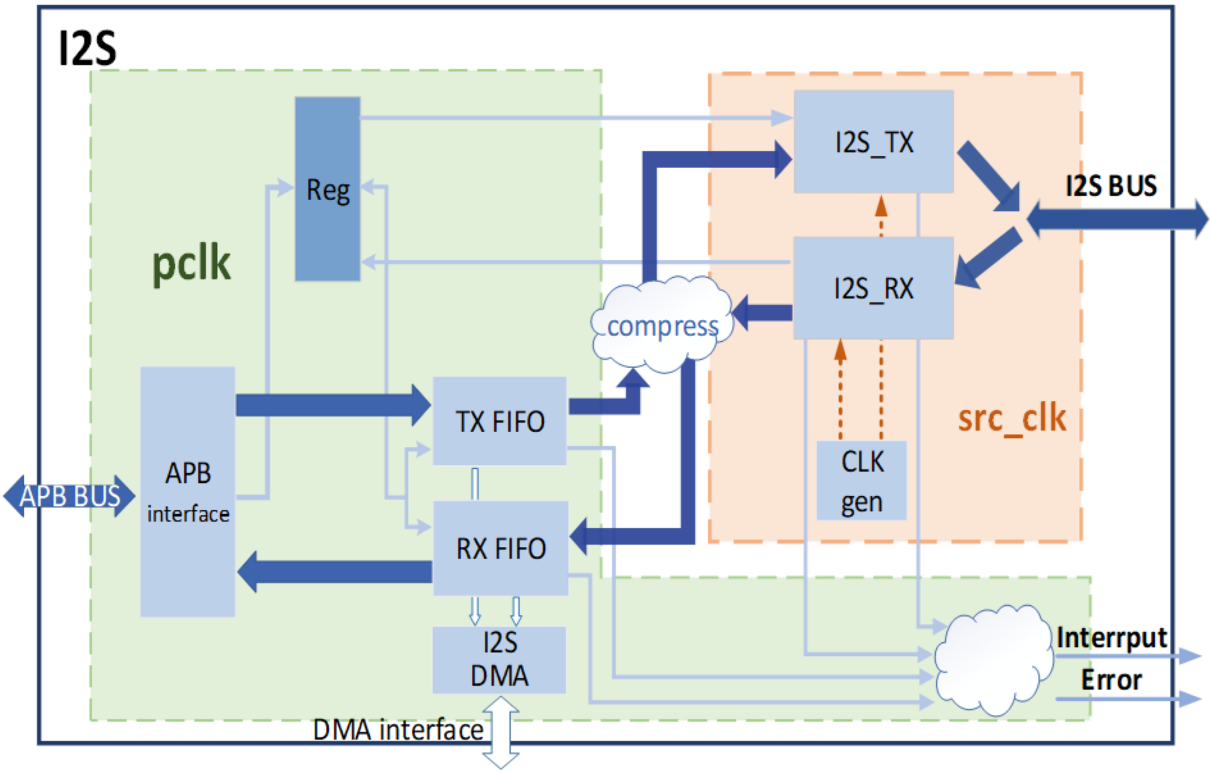

Figure & Table 5-1 I2S block function diagram

5.2 Main Features

The I2S bus interface has the following features:

- APB data bus width of 32 bits

- I2S transmitter and receiver based on the Philips I2S serial protocol
- Serial-master or serial-slave operation
- FIFO – The depth of the transmit and receive FIFO is 32 while the width is 32 bits.
- Programmable FIFO thresholds
- The resolution of the audio data is 16, 24 or 32 bits. I2S can transform data from 16 bits to 24 bits or 32 bits and vice-versa. When I2S works in slave mode, it can auto detect whether the data in transmission is 16 bits, 24 bits or 32 bits.
- DMA Controller Interface: Enables the I2S to interface to a DMA controller over the APB bus using a handshaking interface for transfer requests.
- Independent masking of interrupts and errors: All individual interrupt and error can all be masked independently.
- One combined interrupt line from the I2S to the interrupt controller
- One combined error line from the I2S to the error controller
- Compatible with three serial audio formats: left-justified, I2S, right-justified
- I2S enable signal for multi-blocks synchronous
- Supports audio sample compress.

5.3 Interface

The PAD of the I2S is described in the following Figure & Table 5-2:

Figure & Table 5-2 Pin description table

Pin Name	Direction	Width	Description
I2S_SDA0	IO	1	Serial data 0
I2S_SDA1	IO	1	Serial data 1
I2S_SDA2	IO	1	Serial data 2
I2S_SDA3	IO	1	Serial data 3
I2S_MCLK	O	1	Serial clock when I2S acts as a master.
I2S_SCLK	I	1	Serial clock when I2S acts as a slave.
I2S_WS	IO	1	Word select signal

5.4 Function Description

The bus consists of a serial data line (sd), a word-select line (ws), and a serial clock (sclk). The serial data line is time multiplexed to allow the transfer of two data streams (such as, left and right stereo data).

Figure & Table 5-3 illustrates three simple system configurations for the I2S component. Note that the examples show a second instantiation of the I2S component, which acts as the receiver configured as either a slave or master.

Examples 1 and 2 in the figure show that either the transmitter or the receiver can act as the bus master. The master is responsible for generating the shared sclk and ws clocking signals. In complex systems where there may be several transmitters and receivers, a separate system master can be used. As illustrated in example 3 in the figure, this system master can also be combined with one of the transmitters or receivers in the system. The “controller” in this example is enabled and disabled by configuring the component to act as a master and by programming the clock enable and clock configuration registers.

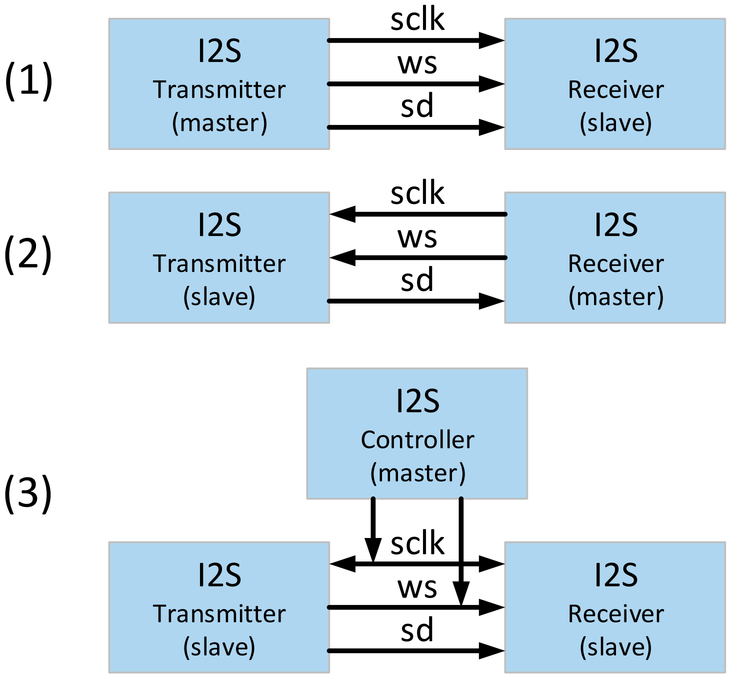

Figure & Table 5-3 Simple system configurations for I2S

The serial data is transmitted in two’s complement format with the most significant bit (MSB) first. This means that the transmitter and receiver can have different word lengths, and neither the transmitter nor receiver need to know what size words the other can handle. If the word being transferred is too large for the receiver, the least significant bits (LSB) are truncated. Similarly, if the word size is less than what the receiver can handle, the data is zero padded.

The word select line is used to control the time multiplexed data streams. For instance, when ws is low, the word being transferred is left stereo data; when ws is high, the word being transferred is right stereo data. It can be configured by RALOLRC and LALOLRC in register IISCNF_IN and IISCNF_OUT. This format is illustrated in Figure & Table 5-4. For standard I2S formats, the MSB of a word is sent one sclk cycle after a ws change. Serial data sent by the transmitter can be synchronized with either the negative edge or positive edge of the sclk signal. However, the receiver must latch the serial data on the rising edge of sclk.

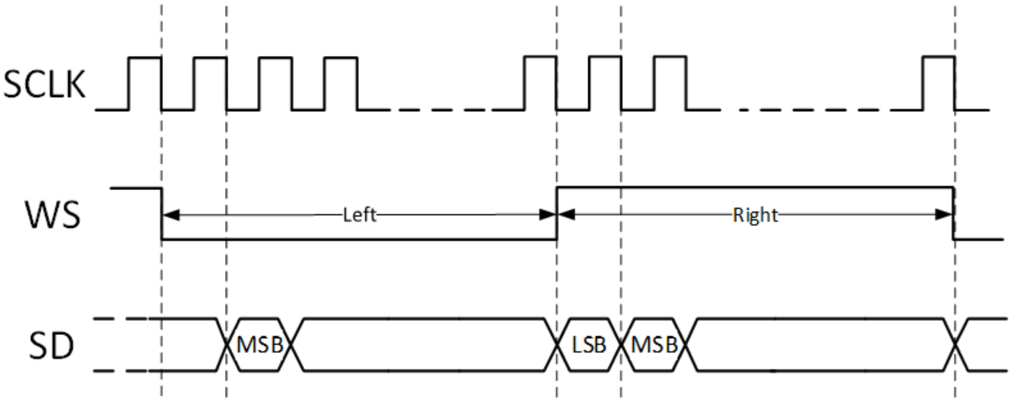

Figure & Table 5-4 I2S standard stereo frame format

At the same time, this I2S module can receive and transmit audio data in left-justified format (illustrated in Figure & Table 5-5) and right-justified format (illustrated in Figure & Table 5-6), the frame format can be configured by RSAFS and TSAFS in registers IISCNF_IN and IISCNF_OUT.

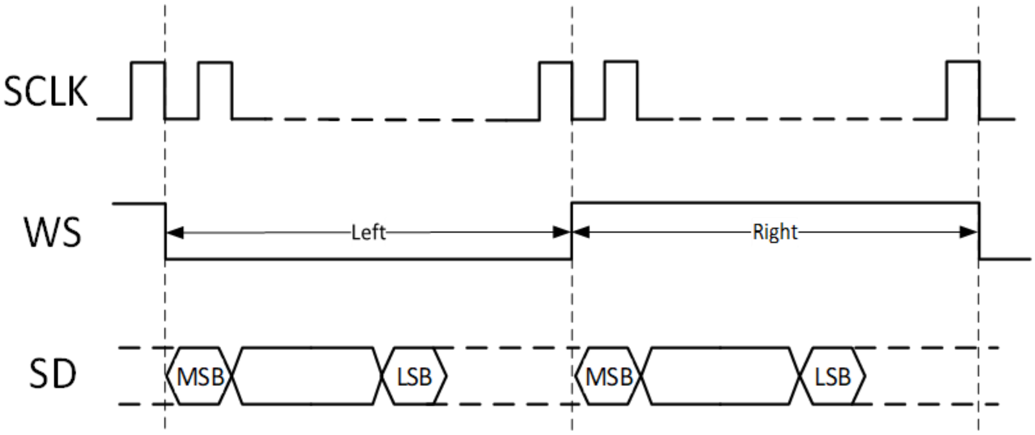

Figure & Table 5-5 I2S stereo frame format in left-justified

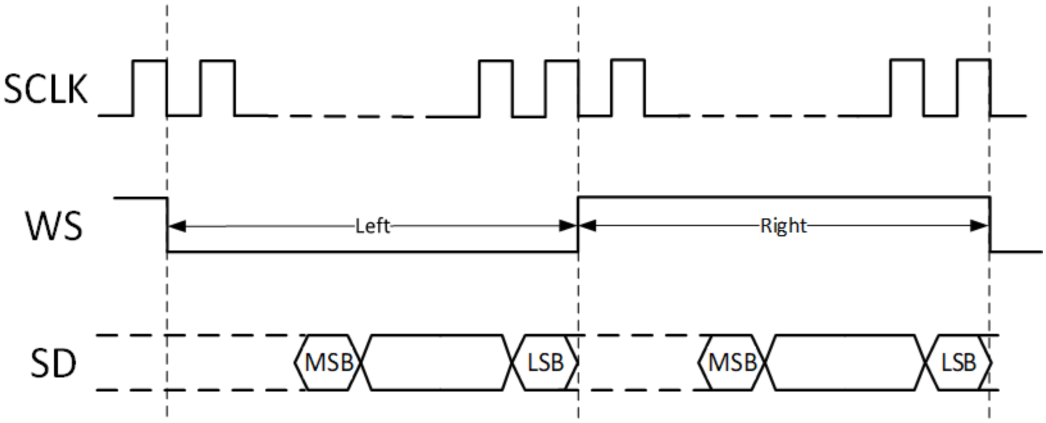

Figure & Table 5-6 I2S stereo frame format in right-justified

5.4.1 Reset

There is only one reset, APB reset rst_b LOW active, in I2S module. After reset, all the registers, FSMs, counters, DMA interface, interrupt interface and so on will be its default value, both of FIFOs will be initial, and all internal generated clock will be closed.

5.4.2 I2S Enable

User must enable the I2S component before any data can be received or transmitted into the FIFOs. To enable the I2S, set the I2S Enable (IISEN) bit (offset: 0x00, IISEN[0]) to 1. To disable the I2S, set this bit to 0.

After disable, the following events occur:

- TX and RX FIFOs are cleared, and read/write pointers are reset.
- Any data in the process of being transmitted or received is lost.
- All other programmable enables (such as transmitter/receiver block enable signals and individual TX/RX channel enables) in the component are overridden.

5.4.3 Clock

5.4.3.1 Circuit Diagram

For I2S support 16-bit, 24-bit and 32-bit data and there are several kinds of sample frequency (fs). The frequency of word selects signal (ws) is sample frequency. The commonly used sample frequency (fs) is 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz,32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz and 192kHz. For user's convenience, here the I2S only needs the user to provide a source clock (src_clk), then the I2S clkgen block will generate the sample frequency (fs) through three dividers. I2S clkgen circuit diagram is as Figure & Table 5-7:

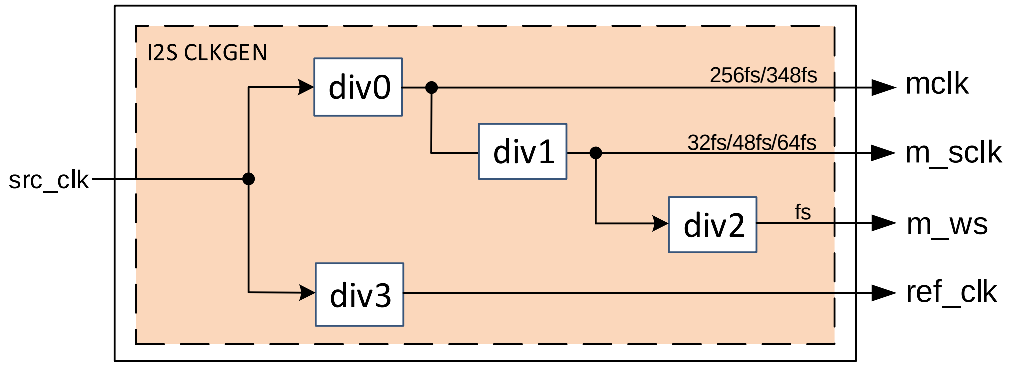

Figure & Table 5-7 I2S clkgen circuit diagram

5.4.3.2 Analyse the Signals

- src_clk: Source clock, comes from system clock. Here we need a src_clk as Figure & Table 5-8:

Figure & Table 5-8 Clock configuration

FS (kHz)		8	11.025	16	22.5	24	32	44.1	48	64	88.2	96	192
Mclk (kHz)	256*fs	2.048	2.8224	4.096	5.76	6.144	8.192	11.2896	12.288	16.384	22.5792	24.576	49.152
	384*fs	3.072	4.2336	6.144	8.64	9.216	12.288	16.9344	18.432	24.576	33.8688	36.864	73.728
Src_clk	@ master mode: src_clk = mclk * n (n = integer, n > 0), Src_clk > sclk*10/3												

FS (kHz)	8	11.025	16	22.5	24	32	44.1	48	64	88.2	96	192
	@ slave mode: src_clk > sclk*20/3											

- mclk: Main clock, divided by DIV0 divider from src_clk, connect to output interface. Users need to configure register FSSTA[16] to select which mclk you will get, 256*fs or 384 *fs, and configuring register DIV0_LEVEL[7:0] to divide src_clk. Make sure mclk frequency is 256*fs or 384* fs.

  mclk = src_clk /div0 = 256 fs or 348fs
- m_sclk: Serial clock. Users need to configure register FSSTA[13:12] to select the m_sclk you need.

  m_sclk = m_ws*2*data_bit_width = 32*fs or 48*fs or 64*fs
- m_ws: Sample frequency, namely fs. It must fix the commonly sample frequency.
- ref_clk: Reference clk, used for slave detect the I2S input sample frequency.

  ref_clk = src_sclk/((DIV3[7:0] + 1)*2)

5.4.3.3 Configurable Registers in I2S clkgen

In order to generate the commonly fs by dividing src_clk, users need to configure these registers: DIV0_LEVEL, DIV1_LEVEL, DIV2_LEVEL and DIV3_LEVEL.

- mclk = src_clk DIV0[7:0] = 0

  mclk = src_clk/DIV0[7:0] DIV0[7:0] ≧ 1

  For example:
  - DIV0[7:0] = 0x0a --> mclk = src_clk/10
  - DIV0[7:0] = 0x19 --> mclk = src_clk/25
- ref_clk = src_sclk/((DIV3[7:0] + 1)*2)
  - This reference clock is used for slave mode to detect the I2S input sample frequency (fs).
  - For the all fs, users should generate ref_clk by configuring DIV3[7:0] in DIV3_LEVEL register in this frequency:

    3.072MHz <= ref_clk <= 4.032MHz
  - Then user may check the calculating result of input sample frequency in registers FADTLR and FSSTA.

5.4.4 DMA Interface

There are DMA interfaces (dma_*_ack, dma_*_req and dma_*_single) in pclk domain for each TX and RX FIFO for reducing CPU overload.

- dma_*_ack: This signal is asserted after the data phase of the last APB transfer in the current transaction.
- dma_*_req: This signal is asserted when the I2S module request a burst transaction.
- dma_*_single: This is a status signal, it is asserted when the I2S module can transfer at least one data. This signal is only suitable for DMA which supports this function.

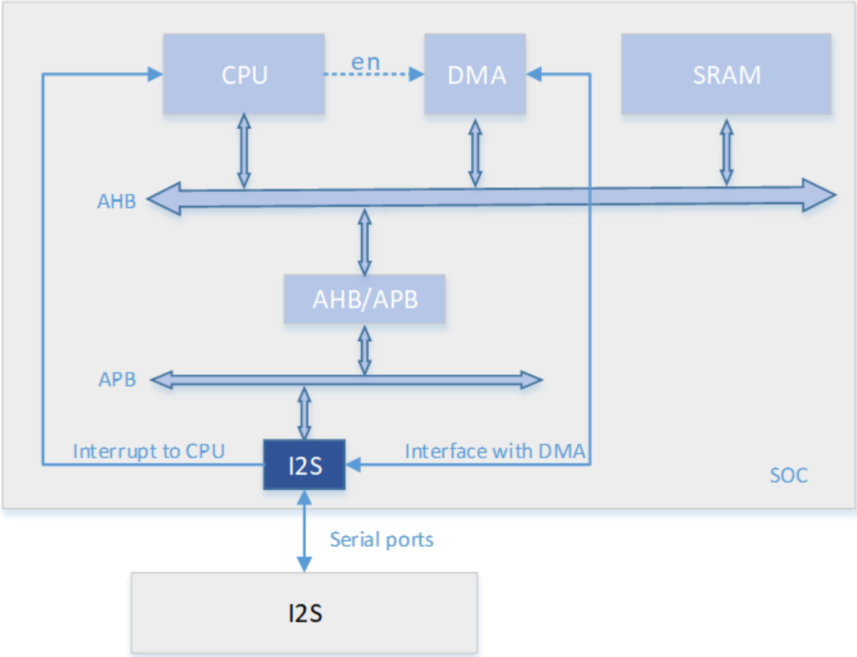

Figure & Table 5-9 I2S in system

Figure & Table 5-9 shows the location and connection of I2S in the system. When users want to use I2S DMA interface, you must configure DMA and I2S by the flow:

1. CPU configures I2S control registers, then enables I2S.
2. CPU configures DMA control registers, then enables I2S DMA interface.
3. I2S transfers data with DMA through data channel APB and controls channel DMA interface.
4. If CPU wants to access I2S, it must wait till the DMA completely transfers data with I2S. CPU can check the state of I2S registers or interrupts.

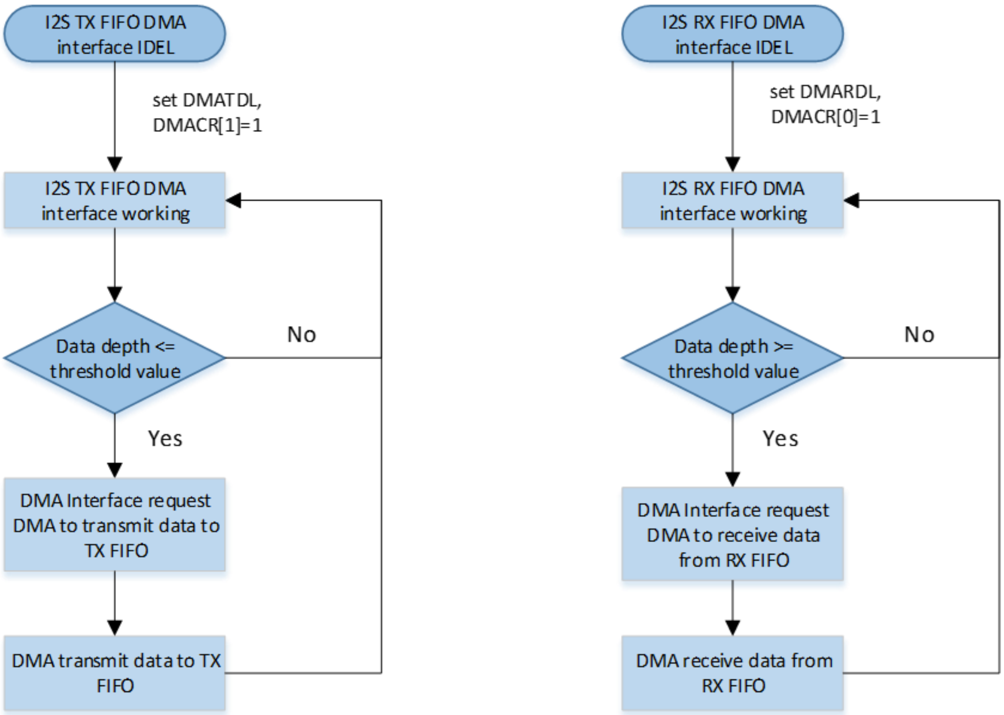
I2S TX FIFO DMA interface IDEL
set DMATDL, DMACR[1]=1
I2S TX FIFO DMA interface working
Data depth <= threshold value
No
Yes
DMA Interface request DMA to transmit data to TX FIFO
DMA transmit data to TX FIFO
I2S RX FIFO DMA interface IDEL
set DMARDL, DMACR[0]=1
I2S RX FIFO DMA interface working
Data depth >= threshold value
No
Yes
DMA Interface request DMA to receive data from RX FIFO
DMA receive data from RX FIFO

Figure & Table 5-10 TX FIFO and RX FIFO DMA interface work flow

The dma_*_req is triggered by the event when the condition of threshold trigger is satisfied. After the DMA burst transaction completed through APB interface, the DMA will assert dma_*_ack feedback to DMA interface, then the dma_*_req will be cleared. After this, the condition of threshold trigger is satisfied still, the dma_req_* will be set again. The timing of DMA interface is shown in Figure & Table 5-11.

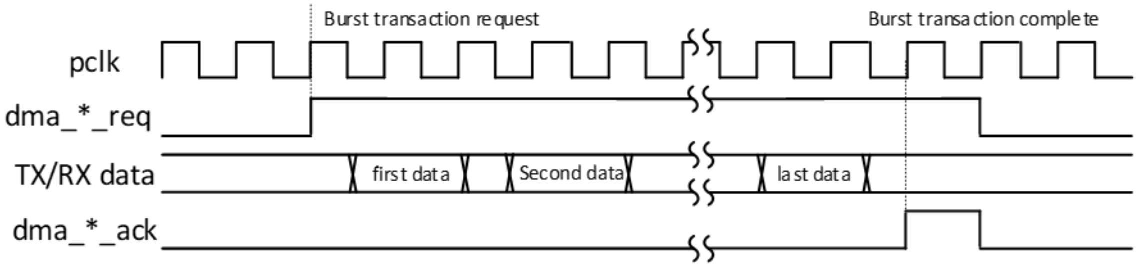

Figure & Table 5-11 DMA interface timing

In order to make FIFOs not overflow, user has to configure the DMA transaction size according to the DMA interface threshold. See reference documentation of DMA for detailed information.

5.4.5 Interrupt and Errors

There are three main types of interrupts and errors in the I2S module: One is about FIFO level (totally 2 individual interrupts and 4 individual errors), one is about transfer mode (totally 3 individual interrupts), the other is about register address (totally 1 individual error). All interrupts and errors are masked by default after reset. These individual interrupts and errors are ORed together to form the combined interrupt or error signal which is seen outside. The interrupt or error is active high.

5.4.5.1 I2S FIFO Level Interrupts

- Transmit FIFO Threshold Empty Interrupt (i2s_txe_intr): Set when the transmit FIFO is equal to or below its threshold value and requires service to prevent an underrun. The threshold value, set through a software-programmable register, determines the level of transmit FIFO entries at which an interrupt is generated.
- Receive FIFO Threshold Full Interrupt (i2s_rxf_intr): Set when the receive FIFO is equal to or above its threshold value plus 1 and requires service to prevent an overflow. The threshold value, set through a software-programmable register, determines the level of receive FIFO entries at which an interrupt is generated.

5.4.5.2 I2S FIFO Level Errors

- Transmit FIFO Overflow Error (i2s_txo_err): Set when an APB access attempts to write into the transmit FIFO after it has been completely filled. When set, data written from the APB is discarded.
- Transmit FIFO Underflow Error (i2s_txu_err): Set when an APB access attempts to read from the transmit FIFO when it is empty. When set, zeros are read back from the transmit FIFO.

- Receive FIFO Overflow Error (i2s_rxo_err): Set when the receive logic attempts to place data into the receive FIFO after it has been completely filled. When set, newly received data is discarded.
- Receive FIFO Underflow Error (i2s_rxu_err): Set when an APB access attempts to read from the receive FIFO when it is empty. When set, zeros are read back from the receive FIFO.

5.4.5.3 I2S Transfer Mode Interrupts

- I2S RX Busy Flag Change (i2s_rxbfc_intr): Set when I2S RX status changes from idle to busy or from busy to idle.
- I2S TX Busy Flag Change (i2s_txbfc_intr): Set when I2S TX status changes from idle to busy or from busy to idle.
- Input Sample Frequency Change (in_fsc_intr): Set when input sample audio frequency change.

5.4.5.4 I2S Register Address Error

- I2S Wrong Register Address Error (i2s_waddr_err): Set when APB access attempts to read or write a register in a wrong address.

5.4.5.5 Relationship of Interrupt & Error Registers

Each interrupt or error is controlled by control bits in the control registers ICR and IMR, and each interrupt or error will generate two state bits in state registers RISR and ISR.

If interrupt or error event happens, the RISR will be set, the state value is maintained at 1 until it is cleared by the writing 1 to the ICR register. If IMR is 0, the interrupt or error will be masked.

The relationship between those registers is described in Figure & Table 5-12:

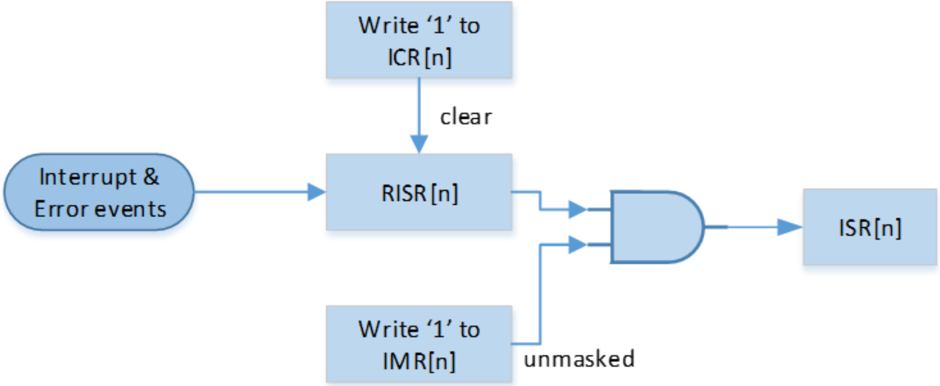

Figure & Table 5-12 relationship of interrupt & error registers

5.5 Usage

The I2S module of the peripheral subsystem is used for two purposes:

- Input and output of general audio interface
- HDMI audio output

For details on how to configure I2S, see section

For details on how to configure I2S software，please refer to the sections Function Description and Register Description.

5.6 Register Description

5.6.1 Register Memory Map

Figure & Table 5-13 Memory map of I2S

Register	Offset	Description	Section/Page
IISEN	0x00	IIS_IO enable register Reset Value: 0x00	5.6.2.1/203
FUNCMODE	0x04	IIS_IO function mode Reset Value: 0x00	5.6.2.2/204
IISCNF_IN	0x08	I2S interface configuration in (on RX side) Reset Value: 0x00	5.6.2.3/204
FSSTA	0x0C	I2S ATX audio input control/state register Reset Value: 0xf0	5.6.2.4/206
IISCNF_OUT	0x10	I2S interface configuration in (on TX side) Reset Value: 0x00	5.6.2.5/211
FADTLR	0x14	I2S FS auto detected threshold level register Reset Value: 0x00	5.6.2.6/212
SCCR	0x18	Sample compress control register Reset Value: 0x00	5.6.2.7/213
TXFTLR	0x1C	Transmit FIFO threshold level Reset Value: 0x10	5.6.2.8/216
RXFTLR	0x20	Receive FIFO threshold level Reset Value: 0x10	5.6.2.9/217
TXFLR	0x24	Transmit FIFO level register Reset Value: 0x00	5.6.2.10/217
RXFLR	0x28	Receive FIFO level register Reset Value: 0x00	5.6.2.11/217
SR	0x2C	Status register Reset Value: 0x0C	5.6.2.12/218
IMR	0x30	Interrupt mask register	5.6.2.13/219

Register	Offset	Description	Section/Page
		Reset Value: 0x7F	
ISR	0x34	Interrupt status register Reset Value: 0x20	5.6.2.14/220
RISR	0x38	Raw interrupt status register Reset Value: 0x20	5.6.2.15/221
ICR	0x3C	Interrupt clear register Reset Value: 0x00	5.6.2.16/222
DMACR	0x40	DMA control register Reset Value: 0x00	5.6.2.17/223
DMATDLR	0x44	DMA transmit data level Reset Value: 0x10	5.6.2.18/224
DMARDLR	0x48	DMA receive data level Reset Value: 0x00	5.6.2.19/224
DIV0_LEVEL	0x50	Divide source clock, get mclk Reset Value: 0x00	5.6.2.20/224
DIV3_LEVEL	0x54	Divide source clock, get reference clock Reset Value: 0x00	5.6.2.21/225

5.6.2 Register and Field Description

5.6.2.1 IISEN

- Name: I2S enable register
- Description: This register controls the I2S enable, the I2S is enabled and disabled by writing to the I2SEN bit.
- Address Offset: 0x00

Figure & Table 5-14 IISEN field description

Bits	Name	Access	Description
31:1	Reserved and read as zero.		
0	I2SEN	R/W	I2S enable bit 1: Enable 0: Disable (default)

5.6.2.2 FUNCMODE

- Name: Function mode register
- Description: This register controls the function mode. It is impossible to write to this register when I2S is enabled. The MODE bit can only be written when the corresponding MODE_wen is asserted at the same time. A single writing to the MODE bit or the MODE_wen bit is useless and will be ignored. Read the MODE_wen bit will always return 0.
- Address Offset: 0x04

Figure & Table 5-15 FUNCMODE field description

Bits	Name	Access	Description
31:12	Reserved and read as zero.		
11:8	CH_SEL	R/W	I2S channel select CH_SEL[n]: Channel [n] enable 0: Channel[n] disabled. 1: Channel[n] enabled.
7:5	Reserved and read as zero.		
4	I2S_RMODE	R/W	RX mode enable 0: The module is in RX mode. (default) 1: The RX mode is disabled for the module.
3:1	Reserved and read as zero.		
0	I2S_TMODE	R/W	TX mode enable 0: The module is in TX mode. (default) 1: The TX mode is disabled for the module.

5.6.2.3 IISCNF_IN

- Name: I2S receiver input interface format
- Description: This register controls the IIS input interface format. It is impossible to write to this register when I2S is enabled.
- Address Offset: 0x08

Figure & Table 5-16 IISCNF_IN field description

Bits	Name	Access	Description
31:14	Reserved and read as zero.		
13:12	RDELAY1	R/W	I2S receiver s_sclk and s_ws delay level 00: No delay (default) 01: Add 1 src_clk cycle delay. 10: Add 2 src_clk cycle delay.

Bits	Name	Access	Description
			11: Add 3 src_clk cycle delay.
11: 10	Reserved and read as zero.		
9	RX_CLK_SEL	R/W	I2S RX clock source select in device mode 0: src_clk (default) 1: mclk_i
8	I2S_RXMODE	R/W	I2S receiver operation mode select 0: Slave mode (default) 1: Master mode
7:6	Reserved and read as zero.		
5	RX_CH_SEL	R/W	I2S sample channel select in mono channel mode 0: Right channel (default) 1: Left channel
4	RX_VOICE_EN	R/W	I2S sample source type select 0: Source is stereo, has different right and left channel signal. (default) 1: Source is mono, the data of left and right channels are same, only receive and store one of them.
3	-	N/A	Reserved
2	RALOLRC	R/W	Active level of left/right channel 0: Low for left channel (default) 1: High for left channel (Low for right channel)
1:0	RSAFS	R/W	Serial-audio format select 0x0: I2S (default) 0x1: Right-justified 0x2: Left-justified
NOTE: 1: In I2S receiver mode, the SD signal is provided by other devices. It can cause a delay during the signal input by PAD.			

The left channel audio data always comes first, Figure & Table 5-17 shows the I2S bus format when RALOLRC=1.

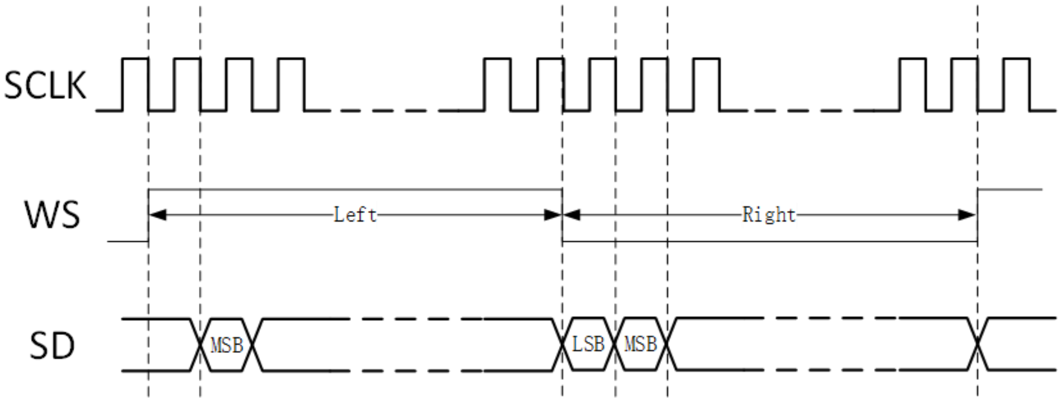

Figure & Table 5-17 I2S standard stereo frame format @RALOLRC=1

5.6.2.4 FSSTA

- Name: I2S serial audio input control register
- Description: This register controls the data width mode of I2S and the auto detecting of slave clock. It is impossible to write to this register when I2S is enabled.
- Address Offset: 0x0C

Figure & Table 5-18 FSSTA field description

Bits	Name	Access	Description
31:17	Reserved and read as zero.		
16	MCLK_SEL	R/W	Mclk frequency select 0: mclk =256*fs (default) 1: mclk = 384*fs
15:14	Reserved and read as zero.		
13:12	SCLK_SEL	R/W	sclk frequency select 00: sclk = 32*fs (default) 01: sclk = 48*fs 1?: sclk = 64*fs
11:8	DATAWTH	R/W	I2S data width mode 0000: 16-bits input/output (both right and left channel) and FIFO stores data in 16-bits. (default) 0001: 16-bits input/output (both right and left channel) and FIFO stores data in 24-bits. 001?: 16-bits input/output (both right and left channel) and FIFO stores data in 32 bit 0100: 24-bits input/output (both right and left channel) and FIFO stores data in 16-bits. 0101: 24-bits input/output (both right and left channel) and FIFO stores data in 24-bits.

Bits	Name	Access	Description
			011?: 24-bits input/output (both right and left channel) and FIFO stores data in 32-bits. 1000: 32-bits input/output (both right and left channel) and FIFO stores data in 16-bits. 1001: 32-bits input/output (both right and left channel) and FIFO stores data in 24-bits. 1?1?: 32-bits input/output (both right and left channel) and FIFO stores data in 32-bits.
7:6	ARS	R	Audio rate scale factor (RX mode only) 00: 1 (default) 01: 0.5 10: 0.25 11: 0.125 See details in Tale 4-6.
5:4	AFR	R	Input audio fs fundamental rate (RX mode only) 00: 88.2KHz (default) 01: 96KHz 10: 64KHz 11: 192KHz See details in Tale 4-6.
3:1	Reserved and read as zero.		
0	AIRAD	R/W	Audio input rate auto detected bit (RX mode only) 0: No detect (default) 1: Audio input rate is auto detected by hardware. (RX mode only)

With FIFO data-width of 32-bit, FIFO stores data in 16-bit means that it can store two sample once. FIFO stores data in 24-bit and 32-bit means that it can store one sample once. The data width changes as Figure & Table 5-19 to Figure & Table 5-27:

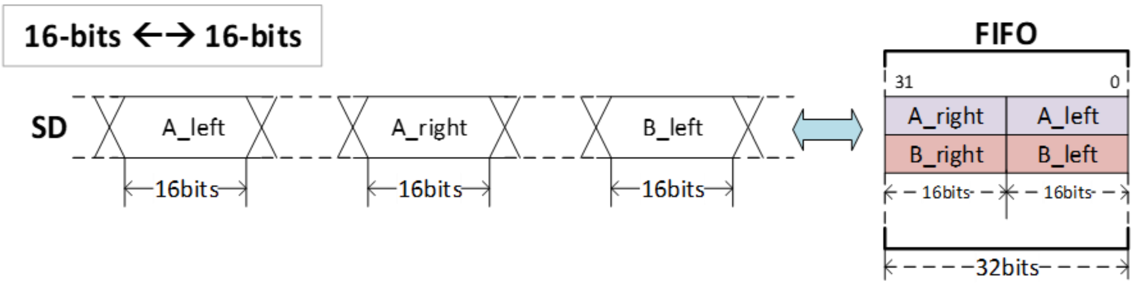

Figure & Table 5-19 16-bits input/output and FIFO stores data in 16-bits

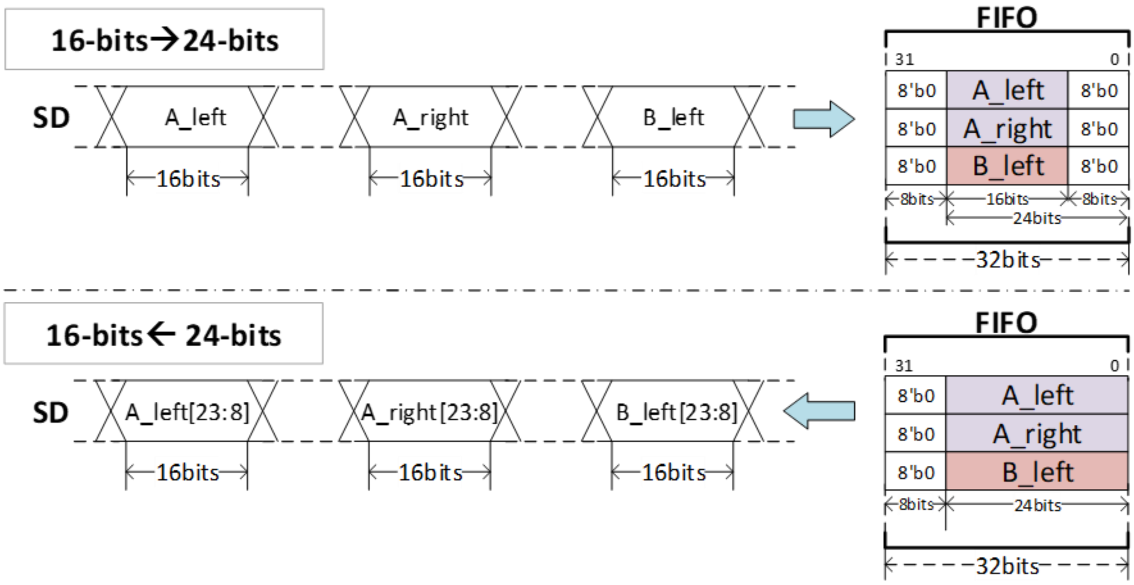

Figure & Table 5-20 16-bits input/output and FIFO stores data in 24-bits

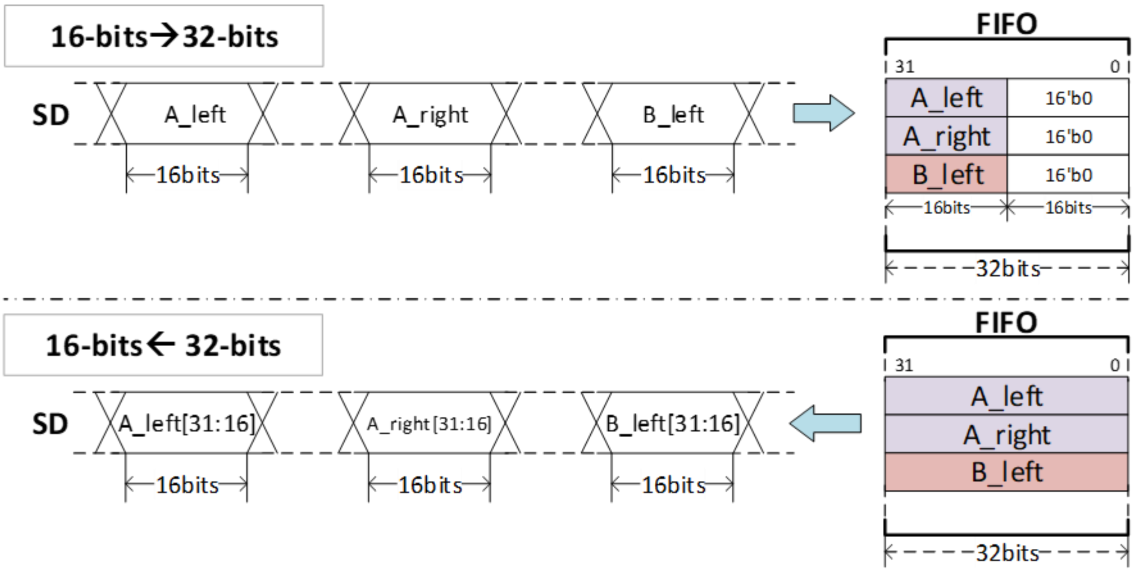

Figure & Table 5-21 16-bits input/output and FIFO stores data in 32-bits

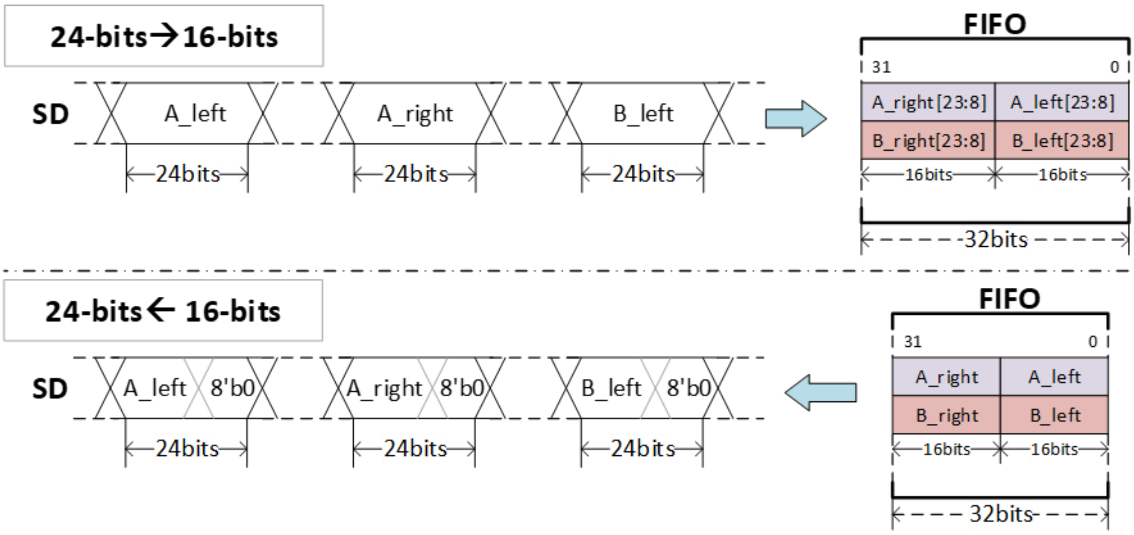

Figure & Table 5-22 24-bits input/output and FIFO stores data in 16-bits

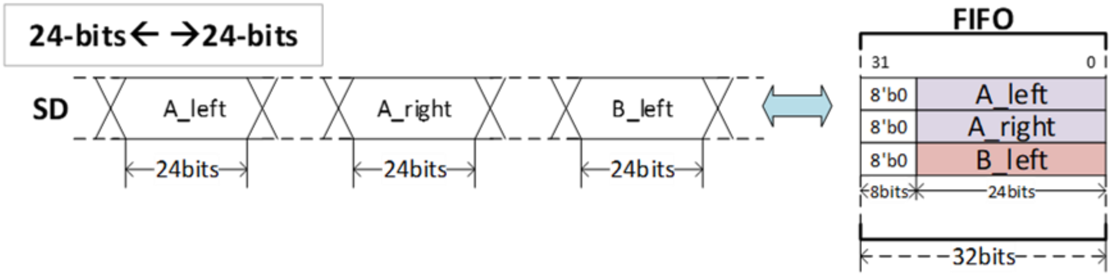

Figure & Table 5-23 24-bits input/output and FIFO stores data in 24-bits

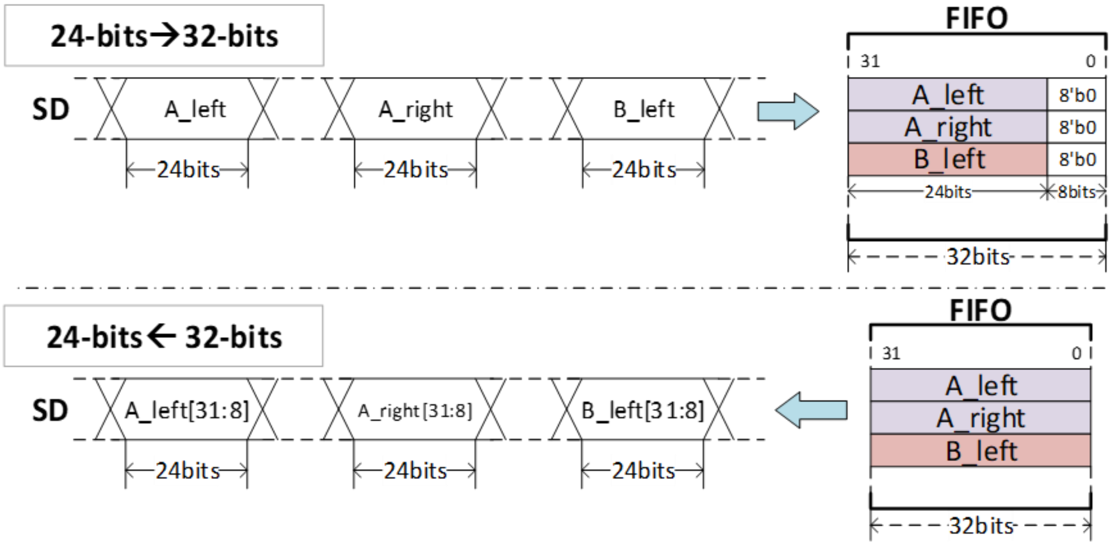

Figure & Table 5-24 24-bits input/output and FIFO stores data in 32-bits

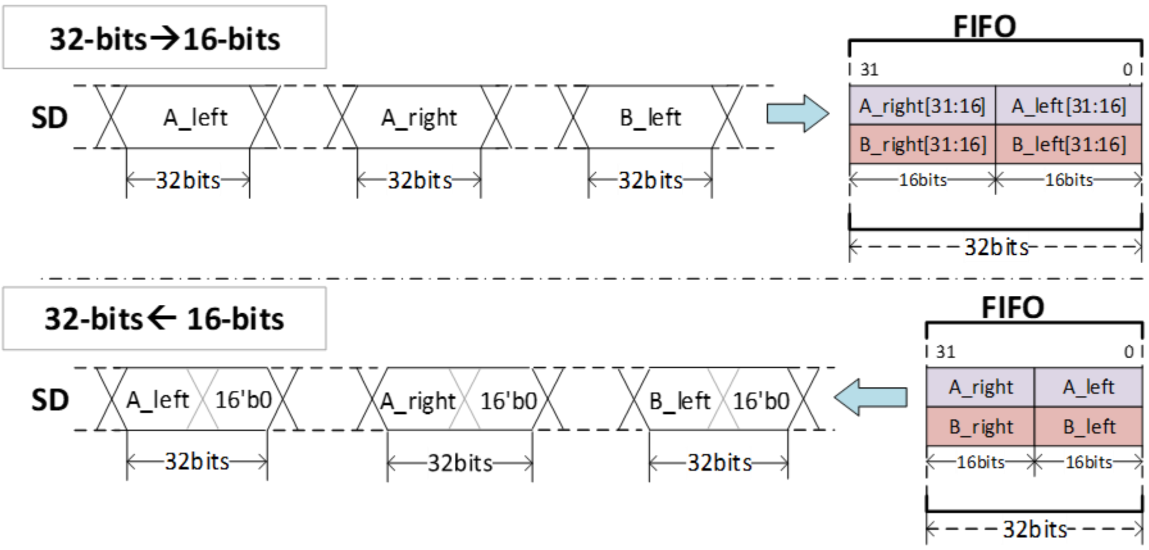

Figure & Table 5-25 32-bits input/output and FIFO stores data in 16-bits

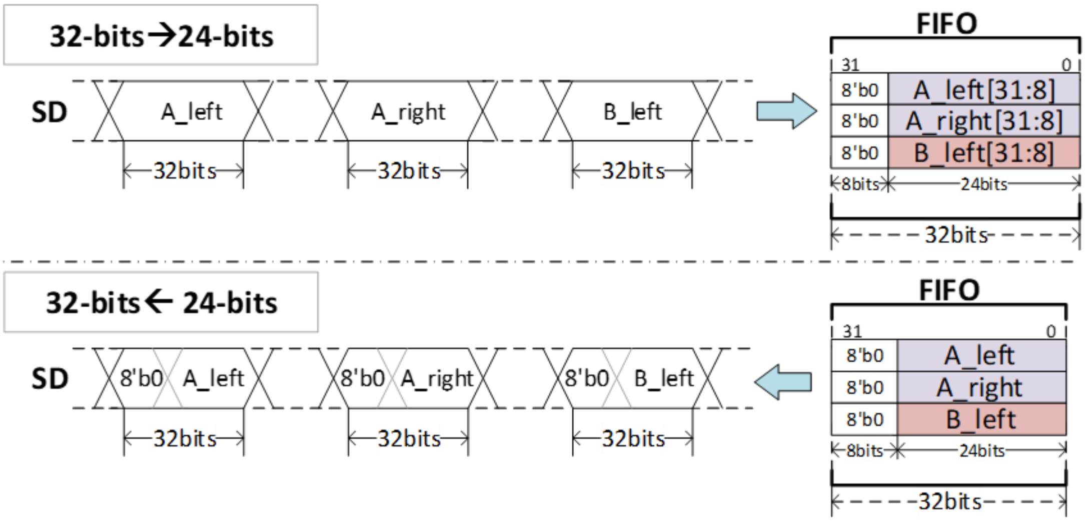

Figure & Table 5-26 32-bits input/output and FIFO stores data in 24-bits

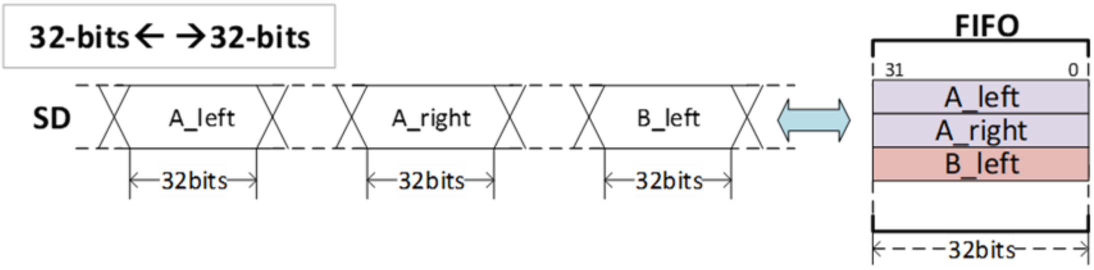

Figure & Table 5-27 32-bits input/output and FIFO store data in 32-bits

The actual value of input sample frequency is resulted from AFR and ARS:

Figure & Table 5-28 Actual input sample frequency

AFR	ARS	FS (kHz)
2’b00	2’b00	88.2

AFR	ARS	FS (kHz)
	2’b01	44.1
	2’b10	22.05
	2’b11	11.025
2’b01	2’b00	96
	2’b01	48
	2’b10	24
	2’b11	12
2’b10	2’b00	64
	2’b01	32
	2’b10	16
	2’b11	8
2’b11	2’b00	192
	2’b10	error
	2’b11	default

5.6.2.5 IISCNF_OUT

- Name: I2S transmitter interface format register
- Description: This register controls the I2S output interface format. It is impossible to write to this register when I2S is enabled.
- Address Offset: 0x10

Figure & Table 5-29 IISCNF_OUT field description

Bits	Name	Access	Description
31:6	Reserved and read as zero.		
5	TX_CLK_SEL	R/W	I2S TX source clock select in device mode 0: src_clk (default) 1: mclk_i
4	I2S_TXMODE	R/W	TX work mode select signal 0: Chip is master. (default) 1: Chip is slave.
3	TX_VOICE_EN	R/W	Sample source type select 0: Source is stereo, has different right and left channel

Bits	Name	Access	Description
			signal. (default) 1: Source is mono, the data of left and right channels are same, take one data from TX FIFO and extend it into stereo.
2	TALOLRC	R/W	Active level of left/right channel 0: Low for left channel (default) 1: High for left channel
1:0	TSAFS	R/W	Serial audio format select 0x0: I2S (default) 0x1: Right-justified 0x2: Left-justified

5.6.2.6 FADTLR

- Name: I2S FS auto detection threshold level
- Description: This register reflects the IIS FS auto detection threshold level, which controls the judgement of the input IIS audio sample frequency in receive mode. A quick reference clock between 3.072MHz and 4.032MHz is used to count the period of the input I2S audio fs (s_ws). Through the count value, the input I2S audio sample frequency can be judged. It is impossible to write to this register when I2S is enabled.
- Address Offset: 0x14

Figure & Table 5-30 FADTLR field description

Bits	Name	Access	Description
31:39	Reserved and read as zero.		
28:24	192FTR	R/W	192KHz FS threshold register These bits set the center count of 192kHz fs. 192FTR = ref_clk/192k If the reference clock frequency is 3.072MHz, because 192K*16 = 3.072M, usually this register should be set to 0x10. When the count value is in the range [14, 18], the input I2S audio FS is regarded as 192kHz.
23:22	Reserved and read as zero.		
21:16	64FTR	R/W	64K FS threshold register These bits set the center count of 64kHz, 32kHz, 16kHz and 8kHz fs. 64FTR = ref_clk/64k If the reference clock frequency is 3.072MHz, because

Bits	Name	Access	Description
			64K*48 = 3.072M, usually this register should be set to 0x30. When the count value is in the range [46, 50], the input I2S fs is regarded as (64*ARS)kHz.
15:14	Reserved and read as zero.		
13:8	88FTR	R/W	88.2K FS threshold register These bits set the center count of 88.2kHz, 44.1kHz, 22.05kHz and 11.025kHz fs. 88FTR = ref_clk/88.2k If the reference clock frequency is 3.072MHz, because 88.2K*35 = 3.072M, usually this register should be set to 0x23. When the count value is in the range [33, 37], the input I2S fs is regarded as (88.2*ARS)KHz.
7:6	Reserved and read as zero.		
5:0	96FTR	R/W	96K FS threshold register These bits set the center count of 96kHz, 48kHz, 24kHz and 12kHz fs. 96FTR = ref_clk/96k If the reference clock frequency is 3.072MHz, because 96K*32= 3.072M, this register should be set to 0x20. When the count value is in the range [30, 34], the input I2S fs is regarded as (96*ARS)kHz.

5.6.2.7 SCCR

- Name: I2S Sample Compress Control Register
- Description: This register controls the compress of audio sample data.
- Address Offset: 0x18

Figure & Table 5-31 SCCR field description

Bits	Name	Access	Description
31:13	Reserved and read as zero.		
12:8	TVCCR	R/W	TX Volume compress control register Based on this register value, right shift the output sample data, the blank bits on the left side are filled with the original MSB, that’s bit 15 or bit 23 or bit 31, it depends on the data width (16/24/32-bits). 0: No compress 1: Shift the sample length from 16/24/32 bits to 15/23/31 bits.

Bits	Name	Access	Description
			2: Shift the sample length from 16/24/32 bits to 14/22/30 bits. ... 15: Shift the sample length from 16/24/32 bits to 1/9/17 bit. Else: Shift the sample length from 16/24/32 bits to 0/8/16 bit. See Figure & Table 5-32, Figure & Table 5-33, Figure & Table 5-34.
7	Reserved and read as zero.		
6:5	SSRCR	R/W	RX Sub sample rate compress control register Based on this register value, compress the input sample data. 0: No compress 1: Compress the sample data one time, that means discard one of every two samples, receive the first data of two. 2: Compress the sample data two times, that means discard two of every three samples, receive the first data of three. 3: No compress See Figure & Table 5-35, Figure & Table 5-36, Figure & Table 5-37, Figure & Table 5-38, Figure & Table 5-39, Figure & Table 5-40.
4:0	RVCCR	R/W	RX volume compress control register Based on this register value, right shift the input sample data, the blank bits on the left side are filled with the original MSB, that's bit 15 or bit 23 or bit 31, it depends on the data width (16/24/32-bits). 0: No compress 1: Shift the sample data from 16/24/32 bits to 15/23/31 bits. 2: Shift the sample data from 16/24/32 bits to 14/22/30 bits. ... 15: Shift the sample data from 16/24/32 bits to 1/9/17 bit. Else: Shift the sample length from 16/24/32 bits to 0/8/16 bit.

Bits	Name	Access	Description
			See Figure & Table 5-32, Figure & Table 5-33, Figure & Table 5-34.

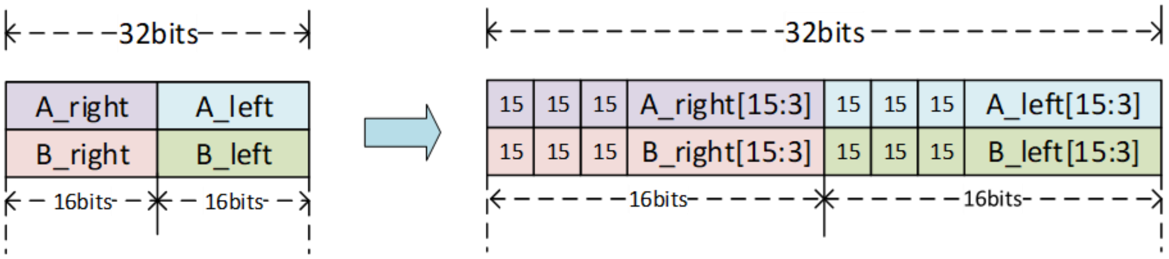

Figure & Table 5-32 Data compress @T/RVCCR=3, DATAWTH[1:0]=00

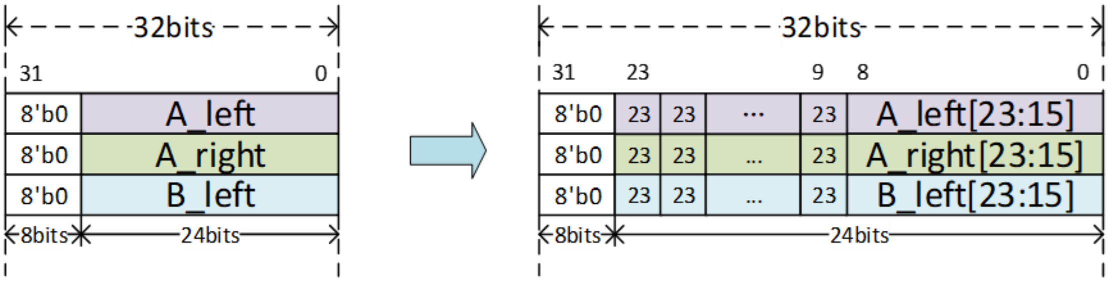

Figure & Table 5-33 Data compress @T/RVCCR=15, DATAWTH[1:0]=01

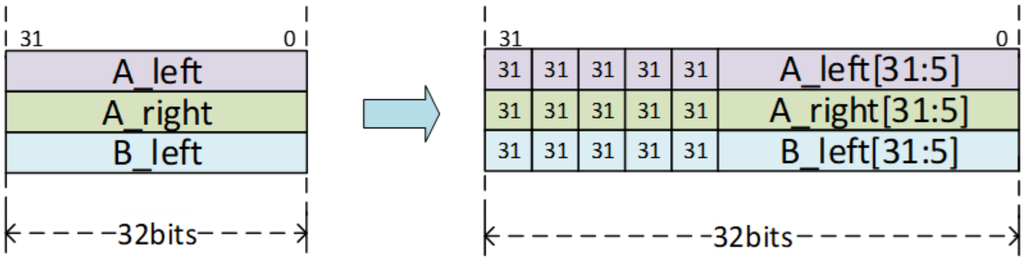

Figure & Table 5-34 Data compress @T/RVCCR=5,DATAWTH[1:0]=1?

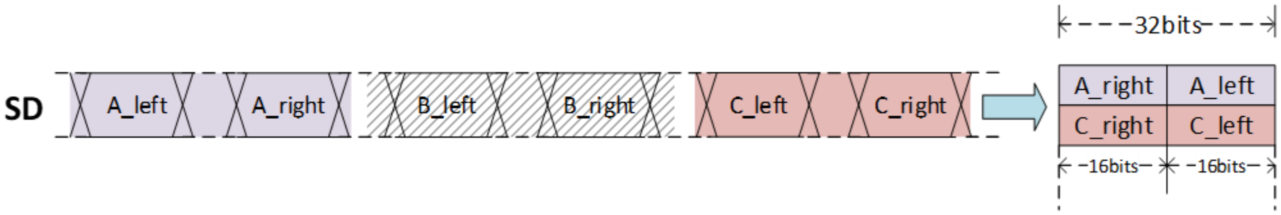

Figure & Table 5-35 Data compress @SSRCR=1, DATAWTH[1:0]=00 @stereo source

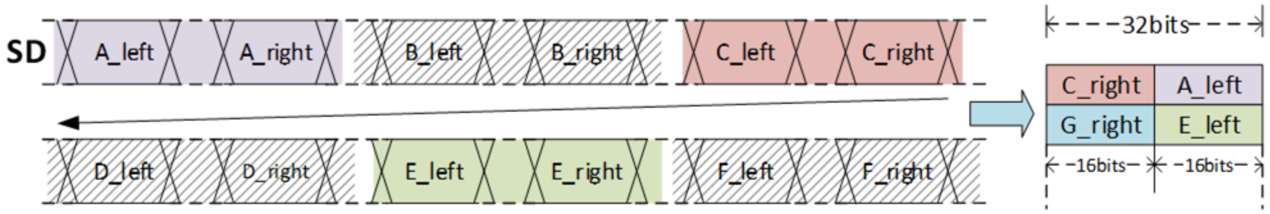

Figure & Table 5-36 Data compress @SSRCR=1, DATAWTH[1:0]=00 @mono source

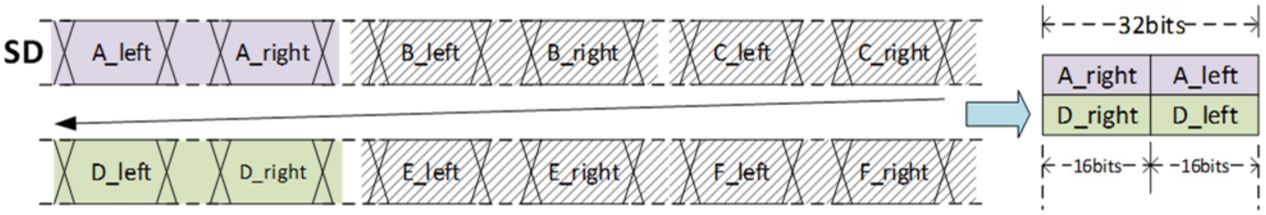

Figure & Table 5-37 Data compress @SSRCR=2, DATAWTH[1:0]=00 @stereo source

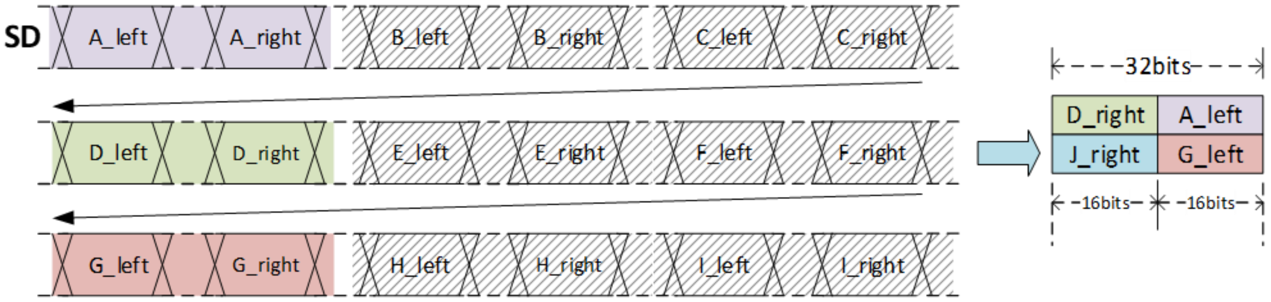

Figure & Table 5-38 Data compress @SSRCR=2, DATAWTH[1:0]=00 @mono source

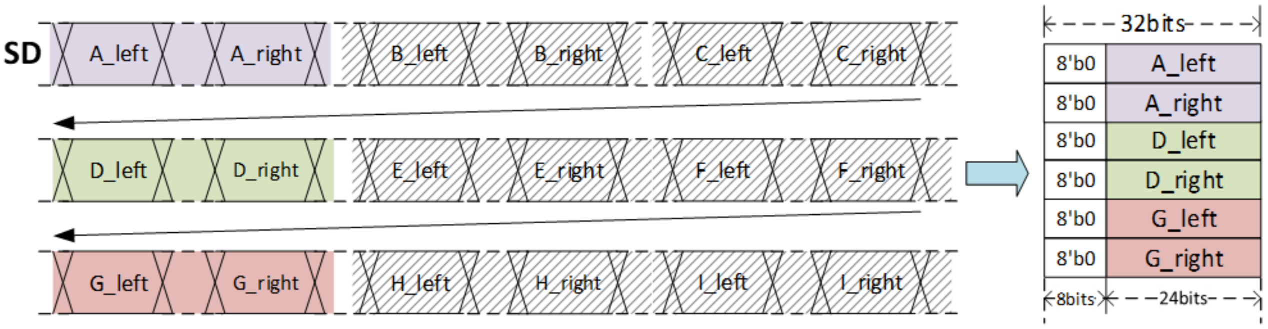

Figure & Table 5-39 Data compress @SSRCR=2, DATAWTH[1:0]=01 @stereo source

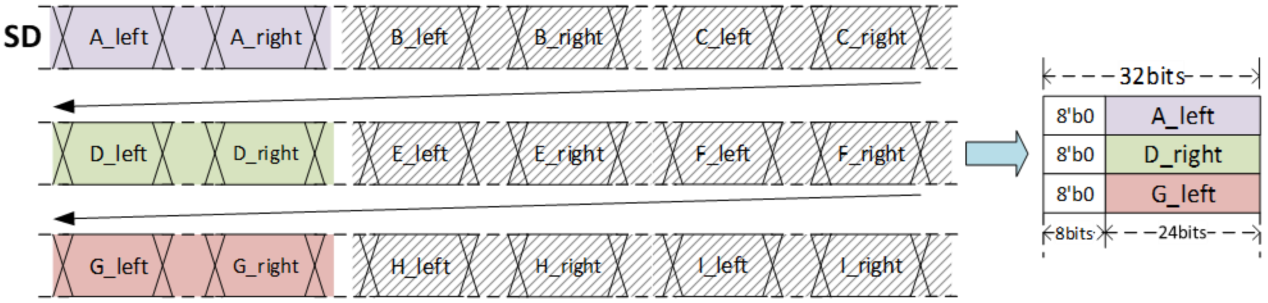

Figure & Table 5-40 Data compress @SSRCR=2, DATAWTH[1:0]=01 @mono source

5.6.2.8 TXFTLR

- Name: I2S transmit FIFO threshold register
- Description: This register controls the threshold value of the transmit FIFO. It is impossible to write to this register when I2S (or SPDIF) is enabled.

- Address Offset: 0x1C

Figure & Table 5-41 TXFTLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	TFT	R/W	Transmit FIFO threshold Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO threshold is configurable in the range 0-31. The default value is 16.

5.6.2.9 RXFTLR

- Name: I2S receive FIFO threshold register
- Description: This register controls the threshold value for the receive FIFO. It is impossible to write to this register when I2S (or SPDIF) is enabled.
- Address Offset: 0x20

Figure & Table 5-42 RXFTLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	RFT	R/W	Receive FIFO threshold Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO threshold is configurable in the range 1-31, when set to 0, threshold = 32. The default value is 16.

5.6.2.10 TXFLR

- Name: I2S transmit FIFO level register
- Description: This register contains the number of valid data entries in the transmit FIFO.
- Address Offset: 0x24

Figure & Table 5-43 TXFLR field description

Bits	Name	Access	Description
31:6	Reserved and read as zero.		
5:0	TXTFL	R	Transmit FIFO level Contains the current number of valid data entries in the transmit FIFO.

5.6.2.11 RXFLR

- Name: I2S receive FIFO level register

- Description: This register contains the number of valid data entries in the receive FIFO.
- Address Offset: 0x28

Figure & Table 5-44 RXFLR field description

Bits	Name	Access	Description
31:6	Reserved and read as zero.		
5:0	RXTFL	R	Receive FIFO level Contains the current number of valid data entries in the receive FIFO.

5.6.2.12 SR

- Name: I2S state register
- Description: This is a read-only register that is used to indicate the current transfer status, FIFO status, and any transmit/receive error that has occurred.
- Address Offset: 0x2C

Figure & Table 5-45 SR field description

Bits	Name	Access	Description
31:6	Reserved and read as zero.		
5	RFF	R	Receive FIFO Full When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full. 1: Receive FIFO is full.
4	RFNE	R	Receive FIFO Not Empty Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. 0: Receive FIFO is empty. 1: Receive FIFO is not empty.
3	TFE	R	Transmit FIFO Empty When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.
2	TFNF	R	Transmit FIFO Not Full Set when the transmit FIFO contains one or more empty entries, and is cleared when the FIFO is full.

Bits	Name	Access	Description
			0: Transmit FIFO is full. 1: Transmit FIFO is not full.
1	TX_BUSY	R	I2S Tx Busy Flag 0: I2S TX is idle or disabled. 1: I2S TX is transmitting data.
0	RX_BUSY	R	I2S Rx Busy Flag 0: I2S RX is idle or disabled. 1: I2S RX is receiving data.

5.6.2.13 IMR

- Name: I2S interrupt mask register
- Description: This read/write register masks or enables all interrupts generated by the I2S.
- Address Offset: 0x30

Figure & Table 5-46 IMR field description

Bits	Name	Access	Description
31	IFSCM	R/W	Input Sample Frequency Change Mask 0: in_fsc_intr interrupt is masked. (in auto detect mode) (default) 1: in_fsc_intr interrupt is not masked. (in auto detect mode)
30:7	Reserved and read as zero.		
6	RXFIM	R/W	Receive FIFO Threshold Full Interrupt Mask 0: i2s_rxf_intr interrupt is masked. 1: i2s_rxf_intr interrupt is not masked. (default)
5	TXEIM	R/W	Transmit FIFO Threshold Empty Interrupt Mask 0: i2s_txe_intr interrupt is masked. 1: i2s_txe_intr interrupt is not masked. (default)
4	RXOIM	R/W	Receive FIFO Overflow Error Mask 0: i2s_rxo_err error is masked. 1: i2s_rxo_err error is not masked. (default)
3	RXUIM	R/W	Receive FIFO Underflow Error Mask 0: i2s_rxu_err error is masked. 1: i2s_rxu_err error is not masked. (default)

Bits	Name	Access	Description
2	TXOIM	R/W	Transmit FIFO Overflow Error Mask 0: i2s_txo_err error is masked. 1: i2s_txo_err error is not masked. (default)
1	TXUIRM	R/W	Transmit FIFO Underflow Error Mask 0: i2s_txu_err error is masked. 1: i2s_txu_err error is not masked. (default)
0	WADEM	R/W	I2S wrong address Error Mask 0: i2s_waddr_err error is masked. 1: i2s_waddr_err error is not masked.(default)

5.6.2.14 ISR

- Name: I2S interrupt status register
- Description: This register indicates the status of the I2S interrupts after they have been masked.
- Address Offset: 0x34

Figure & Table 5-47 ISR field description

Bits	Name	Access	Description
31	IFSCS	R	Input Sample Frequency Change Interrupt Status after masking 0: in_fsc_intr interrupt is active. (in auto detect mode) 1: in_fsc_intr interrupt is not active. (in auto detect mode)
30:7	Reserved and read as zero.		
6	RXFIS	R	Receive FIFO Threshold Full Interrupt Status after masking 0: i2s_rxf_intr interrupt is not active. 1: i2s_rxf_intr interrupt is active.
5	TXEIS	R	Transmit FIFO Threshold Empty Interrupt Status after masking 0: i2s_txe_intr interrupt is not active. 1: i2s_txe_intr interrupt is active.
4	RXOIS	R	Receive FIFO Overflow Error Status after masking 0: i2s_rxo_err error is not active. 1: i2s_rxo_err error is active.
3	RXUIS	R	Receive FIFO Underflow Error Status after masking

Bits	Name	Access	Description
			0: i2s_rxu_err error is not active. 1: i2s_rxu_err error is active.
2	TXOIS	R	Transmit FIFO Overflow Error Status after masking 0: i2s_txo_err error is not active. 1: i2s_txo_err error is active.
1	TXUIRS	R	Transmit FIFO Underflow Error Status after masking 0: i2s_txu_err error is not active. 1: i2s_txu_err error is active.
0	WADES	R	I2S wrong address Error Status after masking 0: i2s_waddr_err error is not active. 1: i2s_waddr_err error is active.

5.6.2.15 RISR

- Name: I2S raw interrupt status register
- Description: This read-only register reports the status of the I2S interrupts prior to masking.
- Address Offset: 0x38

Figure & Table 5-48 RISR field description

Bits	Name	Access	Description
31	RIFSCS	R	Input Sample Frequency Change Raw Interrupt Status prior to masking 0: in_fsc_intr interrupt is active. (in auto detect mode) 1: in_fsc_intr interrupt is not active. (in auto detect mode)
30:7	Reserved and read as zero.		
6	RXFIR	R	Receive FIFO Threshold Full Raw Interrupt Status prior to masking 0: i2s_rxf_intr interrupt is not active. 1: i2s_rxf_intr interrupt is active.
5	TXEIR	R	Transmit FIFO Threshold Empty Raw Interrupt Status prior to masking 0: i2s_txe_intr interrupt is not active. 1: i2s_txe_intr interrupt is active.
4	RXOIR	R	Receive FIFO Overflow Raw Error Status prior to masking 0: i2s_rxo_err interrupt is not active.

Bits	Name	Access	Description
			1: i2s_rxo_err error is active.
3	RXUIR	R	Receive FIFO Underflow Raw Error Status prior to masking 0: i2s_rxu_err error is not active. 1: i2s_rxu_err error is active.
2	TXOIR	R	Transmit FIFO Overflow Raw Error Status prior to masking 0: i2s_txo_err error is not active. 1: i2s_txo_err error is active.
1	TXUIR	R	Transmit FIFO Underflow Raw Error Status prior to masking 0: i2s_txu_err error is not active. 1: i2s_txu_err error is active.
0	RWADES	R	I2S wrong address Raw Error Status prior to masking 0: i2s_waddr_err error is not active. 1: i2s_waddr_err error is active.

5.6.2.16 ICR

- Name: I2S interrupt clear register
- Description: This write-only register is used to clear I2S interrupts.
- Address Offset: 0x3C

Figure & Table 5-49 ICR field description

Bits	Name	Access	Description
31	CRIFSC	W	Clear Input Sample Frequency Change Interrupt 0: Not clear in_fsc_intr interrupt. 1: Clear in_fsc_intr interrupt.
30:7	Reserved and read as zero.		
6	RXFIC	W	Clear Receive FIFO Threshold Full Interrupt 0: Not clear i2s_rxf_intr interrupt. 1: Clear i2s_rxf_intr interrupt.
5	TXEIC	W	Clear Transmit FIFO Threshold Empty Interrupt 0: Not clear i2s_txe_intr interrupt. 1: Clear i2s_txe_intr interrupt.
4	RXOIC	W	Clear Receive FIFO Overflow Error

Bits	Name	Access	Description
			0: Not clear i2s_rxo_err error. 1: Clear i2s_rxo_err error.
3	RXUIC	W	Clear Receive FIFO Underflow Error 0: Not clear i2s_rxu_err interrupt. 1: Clear i2s_rxu_err interrupt.
2	TXOIC	W	Clear Transmit FIFO Overflow Error Status 0: Not clear i2s_txo_err interrupt. 1: Clear i2s_txo_err interrupt.
1	TXUIC	W	Clear Transmit FIFO Underflow Error 0: Not clear i2s_txu_err interrupt. 1: Clear i2s_txu_err interrupt.
0	CWADEC	W	Clear I2S wrong address Error 0: Not clear i2s_waddr_err interrupt. 1: Clear i2s_waddr_err interrupt.

5.6.2.17 DMACR

- Name: I2S DMA control register
- Description: The register is used to enable the DMA controller interface operation.
- Address Offset: 0x40

Figure & Table 5-50 DMACR field description

Bits	Name	Access	Description
31:2	Reserved and read as zero.		
1	TDMAE	R/W	Transmit DMA Enable This bit enables/disables the transmit FIFO DMA channel. 0: Transmit DMA disabled. (default) 1: Transmit DMA enabled.
0	RDMAE	R/W	Receive DMA Enable This bit enables/disables the receive FIFO DMA channel. 0: Receive DMA disabled. (default) 1: Receive DMA enabled.

5.6.2.18 DMATDLR

- Name: I2S DMA transmit data level register
- Description: This register controls the I2S DMA transmit data level.
- Address Offset: 0x44

Figure & Table 5-51 DMATDLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	DMATDL	R/W	Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. The watermark level = DMATDL; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1. The default value is 16, it can be configured in the range 0-31. When set to 0, threshold = 32.

5.6.2.19 DMARDLR

- Name: I2S DMA receive data level register
- Description: This register controls the I2S DMA receive data level.
- Address Offset: 0x48

Figure & Table 5-52 DMARDLR field description

Bits	Name	Access	Description
31:5	Reserved and read as zero.		
4:0	DMARDL	R/W	DMA Receive Data Level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value, and RDMAE = 1. The default value is 0, it can be configured in the range 1-31. When set to 0, threshold = 32.

5.6.2.20 DIV0_LEVEL

- Name: I2S divider0 control register
- Description: Write to this register as a divider which divides src_clk then gets mclk.
- Address Offset: 0x50

Figure & Table 5-53 DIV0_LEVEL field description

Bits	Name	Access	Description
31:8	Reserved and read as zero.		
7:0	DIV0	R/W	A divider for getting mclk from src_clk 0: No divide (default) Else: divide = DIV0

5.6.2.21 DIV3_LEVEL

- Name: I2S divider3 control register
- Description: Write to this register as a divider which divides src_clk then gets ref_clk.
- Address Offset: 0x54

Figure & Table 5-54 DIV3_LEVEL field description

Bits	Name	Access	Description
31:8	Reserved and read as zero.		
7:0	DIV3	R/W	A divider for getting the ref_clk from src_clk divide = (DIV3 + 1)*2

6 PWM

6.1 Overview

Pulse Width Modulation (PWM) can control the motor and other equipment by generating periodic pulse waveform. The pulse width and the number of cycles can be configured by register.

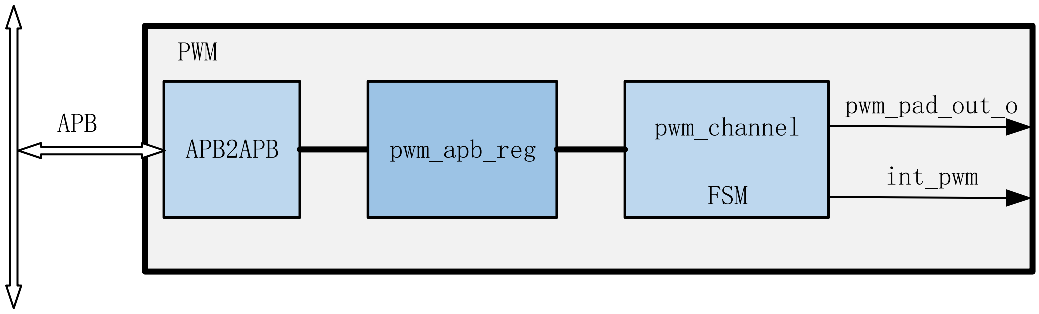

Figure & Table 6-1 PWM block function diagram

6.2 Main Features

The PWM module consists of 6 PWM generators, each generator is related to 1 IO pin, each generator has the following features:

- Cycle frequency can be set, with a maximum support of 12MHz
- Duty cycle configurable
- Supports one shot mode and continuous mode
- Supports event triggering mode in one shot mode

6.3 Interface

PWM output sequence diagram is shown in Figure & Table 6-2, in which period and high and low level phase length can be configured:

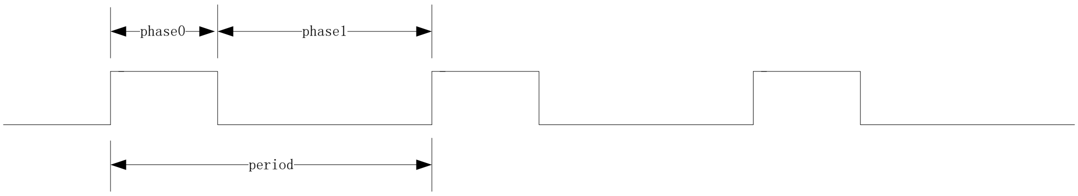

Figure & Table 6-2 PWM interface timing diagram

The PAD of PWM is described in Figure & Table 6-3:

Figure & Table 6-3 Pin description table

Pin Name	Direction	Width	Description
PWM0	O	1	PWM channel 0’s out data of pulse waveform
PWM1	O	1	PWM channel 1’s out data of pulse waveform
PWM2	O	1	PWM channel 2’s out data of pulse waveform
PWM3	O	1	PWM channel 3’s out data of pulse waveform
PWM4	O	1	PWM channel 4’s out data of pulse waveform
PWM5	O	1	PWM channel 5’s out data of pulse waveform

6.4 Function Description

6.4.1 Data and Control Flow

PWM pulse generation mode is divided into one shot mode and continuous mode. The number of cycles of the one shot mode pulse can be configured through the register PWM RPT. Continuous mode can update configuration information during the process.

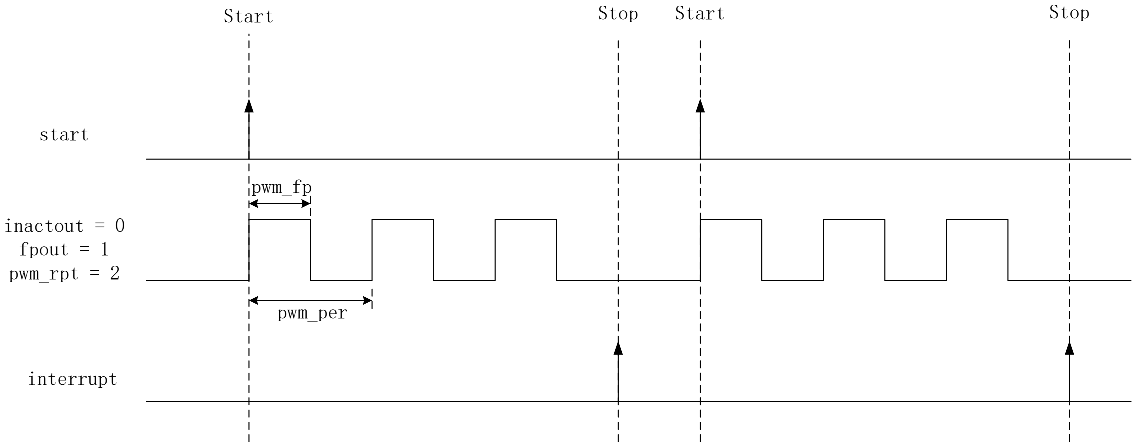

Figure & Table 6-4 One shot mode diagram

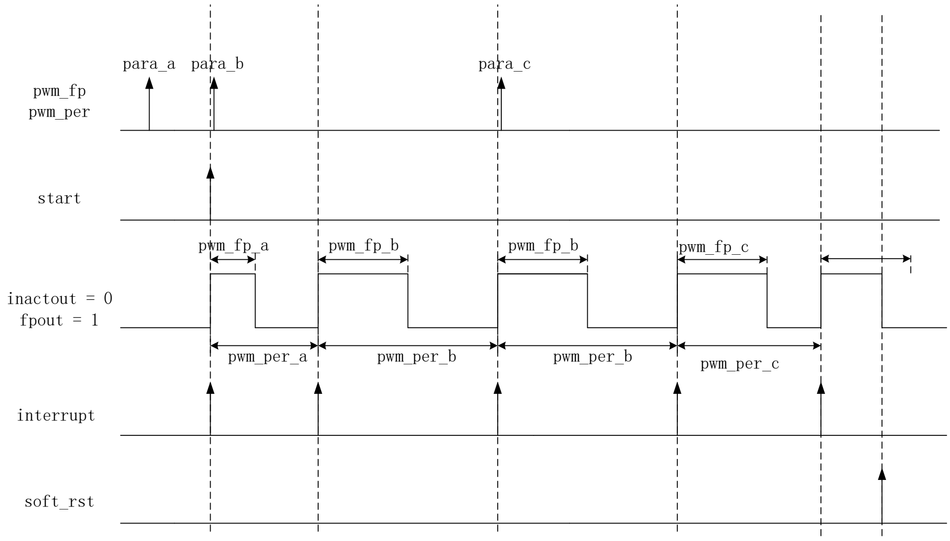

Figure & Table 6-5 Continuous mode diagram

6.4.2 PWM Interrupts

PWM provides an interrupt signal int_pwm. See the interrupt vector table of the chip for details.

6.5 Usage

6.5.1 One Shot Mode

One shot mode configuration is as follows:

1. Configure the information related to the register PWM_CTRL, except bit0 [start] and bit2 [cfg_update].
2. Configure the registers PWM_RPT, PWM_PER and PWM_FP.
3. Configure bit2 of register PWM_CTRL, write 1.
4. Configure bit0 of register PWM_CTRL, write 1.
5. View PWM_STATUS and PWM_INTR_STA.

6.5.2 Continuous Mode

Continuous mode configuration is as follows:

1. Configure the information related to the register PWM_CTRL, except bit0 [start] and bit2 [cfg_update].
2. Configure the registers PWM_RPT, PWM_PER and PWM_FP.
3. Configure bit2 of register PWM_CTRL, write 1.
4. Configure bit0 of register PWM_CTRL, write 1.
5. View PWM_STATUS and PWM_INTR_STA.

6.6 Register Description

6.6.1 Register Memory Map

Register	Offset	Description	Section/Page
PWM_CTRL_0	0x00	PWM channel 0 control register	6.6.2.1/230
PWM_RPT_0	0x04	PWM channel 0 one shot control register	6.6.2.2/231
PWM_PER_0	0x08	PWM channel 0 periodic control register	6.6.2.3/231
PWM_FP_0	0x0c	PWM channel 0 first phase control register	6.6.2.4/231
PWM_STATUS_0	0x10	PWM channel 0 status register	6.6.2.5/232
PWM_CTRL_1	0x20	PWM channel 1 control register	6.6.2.6/232
PWM_RPT_1	0x24	PWM channel 1 one shot control register	6.6.2.7/233
PWM_PER_1	0x28	PWM channel 1 periodic control register	6.6.2.8/234
PWM_FP_1	0x2c	PWM channel 1 first phase control register	6.6.2.9/234
PWM_STATUS_1	0x30	PWM channel 1 status register	6.6.2.10/234
PWM_CTRL_2	0x40	PWM channel 2 control register	6.6.2.11/235
PWM_RPT_2	0x44	PWM channel 2 one shot control register	6.6.2.12/236
PWM_PER_2	0x48	PWM channel 2 periodic control register	6.6.2.13/236
PWM_FP_2	0x4c	PWM channel 2 first phase control register	6.6.2.14/236
PWM_STATUS_2	0x50	PWM channel 2 status register	6.6.2.15/237
PWM_CTRL_3	0x60	PWM channel 3 control register	6.6.2.16/237
PWM_RPT_3	0x64	PWM channel 3 one shot control register	6.6.2.17/238
PWM_PER_3	0x68	PWM channel 3 periodic control register	6.6.2.18/239
PWM_FP_3	0x6c	PWM channel 3 first phase control register	6.6.2.19/239
PWM_STATUS_3	0x70	PWM channel 3 status register	6.6.2.20/239
PWM_CTRL_4	0x80	PWM channel 4 control register	6.6.2.21/240
PWM_RPT_4	0x84	PWM channel 4 one shot control register	6.6.2.22/241
PWM_PER_4	0x88	PWM channel 4 periodic control register	6.6.2.23/241
PWM_FP_4	0x8c	PWM channel 4 first phase control register	6.6.2.24/241
PWM_STATUS_4	0x90	PWM channel 4 status register	6.6.2.25/242
PWM_CTRL_5	0xa0	PWM channel 5 control register	6.6.2.26/242

Register	Offset	Description	Section/Page
PWM_RPT_5	0xa4	PWM channel 5 one shot control register	6.6.2.27/243
PWM_PER_5	0xa8	PWM channel 5 periodic control register	6.6.2.28/244
PWM_FP_5	0xac	PWM channel 5 first phase control register	6.6.2.29/244
PWM_STATUS_5	0xb0	PWM channel 5 status register	6.6.2.30/244
PWM_INTR_STA	0xff0	PWM interrupt status register	6.6.2.31/245

6.6.2 Register and Field Description

6.6.2.1 PWM_CTRL_0

- Description: PWM channel 0 control register
- Offset: 0x00
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	INACTOUT	RW	PWM output level when not enabled Value After Reset: 0x0
[8]	FPOUT	RW	PWM output level of the first phase in a cycle Value After Reset: 0x0
[7:6]	EVTRIG	RW	Event triggering mode in one shot mode 1: Rising edge trigger 2: Falling edge trigger 0&3: General mode, that is, the output of PWM signal is not based on external signal. Value After Reset: 0x0
[5:4]	MODE	RW	PWM mode 1: One shot mode 2: Continuous mode 0&3: Reserved Value After Reset: 0x0
[3]	INTEN	RW	Interrupt enable 0: Disable 1: Enable Value After Reset: 0x0

Bits	Field Name	Access	Description
[2]	CFG_UPDATE	RW	In continuous mode, the PWM_PER and PWM_FP registers are updated in the middle. When the register value is changed, the cfg_update is configured from 0 to 1 (indicating that both register values are updated at the same time). Value After Reset: 0x0
[1]	SOFT_RST	RW	The software reset enable is used to turn off PWM_cycle (PWM status[7:0]) at any time. Value After Reset: 0x0
[0]	START	RW	PWM start coding enable, rising edge effective (i.e. from 0 to 1) Value After Reset: 0x0

6.6.2.2 PWM_RPT_0

- Description: PWM channel 0 one shot control register
- Offset: 0x04
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	ONE_SHOT_RPT	RW	The number of cycles repeated in one shot transmission Value After Reset: 0x0

6.6.2.3 PWM_PER_0

- Description: PWM channel 0 periodic control register
- Offset: 0x08
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_PER	RW	The number of beats of the system clock that a periodic waveform lasts. If PWM_per is 0, no PWM effective signal is output. Value After Reset: 0x0

6.6.2.4 PWM_FP_0

- Description: PWM channel 0 first phase control register
- Offset: 0x0c

- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_FP	RW	The number of beats in the first phase of a periodic waveform. If PWM_FP is larger than PWM_ per, all effective signals are FPOUT. If PWM FP is 0, all effective signals are! FPOUT. Value After Reset: 0x0

6.6.2.5 PWM_STATUS_0

- Description: PWM channel 0 status register
- Offset: 0x10
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	PWM_OUT	RW	PWM current value of the waveform Value After Reset: 0x0
[8]	PWM_BUSY	RW	PWM state of the state machine 0: Idle 1: Busy Value After Reset: 0x0
[7:0]	PWM_CYCLE	RW	In continuous mode, the number of cycles that the same group of PWM_per & PWM_FP parameters have output. Value After Reset: 0x0

6.6.2.6 PWM_CTRL_1

- Description: PWM channel 1 control register
- Offset: 0x20
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	INACTOUT	RW	PWM output level when not enabled Value After Reset: 0x0
[8]	FPOUT	RW	PWM output level of the first phase in a cycle Value After Reset: 0x0

Bits	Field Name	Access	Description
[7:6]	EVTRIG	RW	Event triggering mode in one shot mode 1: Rising edge trigger 2: Falling edge trigger 0&3: General mode, that is, the output of PWM signal is not based on external signal. Value After Reset: 0x0
[5:4]	MODE	RW	PWM mode 1: One shot mode 2: Continuous mode 0&3: Reserved Value After Reset: 0x0
[3]	INTEN	RW	Interrupt enable 0: Disable 1: Enable Value After Reset: 0x0
[2]	CFG_UPDATE	RW	In continuous mode, the PWM_PER and PWM_FP registers are updated in the middle. When the register value is changed, the cfg_update is configured from 0 to 1 (indicating that both register values are updated at the same time). Value After Reset: 0x0
[1]	SOFT_RST	RW	The software reset enable is used to turn off PWM_cycle (PWM status[7:0]) at any time. Value After Reset: 0x0
[0]	START	RW	PWM start coding enable, rising edge effective (i.e. from 0 to 1) Value After Reset: 0x0

6.6.2.7 PWM_RPT_1

- Description: PWM channel 1 one shot control register
- Offset: 0x24
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	ONE_SHOT_RPT	RW	The number of cycles repeated in one shot

Bits	Field Name	Access	Description
			transmission Value After Reset: 0x0

6.6.2.8 PWM_PER_1

- Description: PWM channel 1 periodic control register
- Offset: 0x28
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_PER	RW	The number of beats of the system clock that a periodic waveform lasts. If PWM_per is 0, no PWM effective signal is output. Value After Reset: 0x0

6.6.2.9 PWM_FP_1

- Description: PWM channel 1 first phase control register
- Offset: 0x2c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_FP	RW	The number of beats in the first phase of a periodic waveform. If PWM_FP is larger than PWM_per, all effective signals are FPOUT. If PWM FP is 0, all effective signals are! FPOUT. Value After Reset: 0x0

6.6.2.10 PWM_STATUS_1

- Description: PWM channel 1 status register
- Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	PWM_OUT	RW	PWM current value of the waveform Value After Reset: 0x0
[8]	PWM_BUSY	RW	PWM state of the state machine 0: Idle

Bits	Field Name	Access	Description
			1: Busy Value After Reset: 0x0
[7:0]	PWM_CYCLE	RW	In continuous mode, the number of cycles that the same group of PWM_per & PWM_FP parameters have output. Value After Reset: 0x0

6.6.2.11 PWM_CTRL_2

- Description: PWM channel 2 control register
- Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	INACTOUT	RW	PWM output level when not enabled Value After Reset: 0x0
[8]	FPOUT	RW	PWM output level of the first phase in a cycle Value After Reset: 0x0
[7:6]	EVTRIG	RW	Event triggering mode in one shot mode 1: Rising edge trigger 2: Falling edge trigger 0&3: General mode, that is, the output of PWM signal is not based on external signal. Value After Reset: 0x0
[5:4]	MODE	RW	PWM mode 1: One shot mode 2: Continuous mode 0&3: Reserved Value After Reset: 0x0
[3]	INTEN	RW	Interrupt enable 0: Disable 1: Enable Value After Reset: 0x0
[2]	CFG_UPDATE	RW	In continuous mode, the PWM_PER and PWM_FP registers are updated in the middle. When the register value is changed, the cfg_update is configured from 0

Bits	Field Name	Access	Description
			to 1 (indicating that both register values are updated at the same time). Value After Reset: 0x0
[1]	SOFT_RST	RW	The software reset enable is used to turn off PWM_cycle (PWM status[7:0]) at any time. Value After Reset: 0x0
[0]	START	RW	PWM start coding enable, rising edge effective (i.e. from 0 to 1) Value After Reset: 0x0

6.6.2.12 PWM_RPT_2

- Description: PWM channel 2 one shot control register
- Offset: 0x44
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	ONE_SHOT_RPT	RW	The number of cycles repeated in one shot transmission Value After Reset: 0x0

6.6.2.13 PWM_PER_2

- Description: PWM channel 2 periodic control register
- Offset: 0x48
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_PER	RW	The number of beats of the system clock that a periodic waveform lasts. If PWM_per is 0, no PWM effective signal is output. Value After Reset: 0x0

6.6.2.14 PWM_FP_2

- Description: PWM channel 2 first phase control register
- Offset: 0x4c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_FP	RW	The number of beats in the first phase of a periodic waveform. If PWM_FP is larger than PWM_per, all effective signals are FPOUT. If PWM FP is 0, all effective signals are! FPOUT. Value After Reset: 0x0

6.6.2.15 PWM_STATUS_2

- Description: PWM channel 2 status register
- Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	PWM_OUT	RW	PWM current value of the waveform Value After Reset: 0x0
[8]	PWM_BUSY	RW	PWM state of the state machine 0: Idle 1: Busy Value After Reset: 0x0
[7:0]	PWM_CYCLE	RW	In continuous mode, the number of cycles that the same group of PWM_per & PWM_FP parameters have output. Value After Reset: 0x0

6.6.2.16 PWM_CTRL_3

- Description: PWM channel 3 control register
- Offset: 0x60
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	INACTOUT	RW	PWM output level when not enabled Value After Reset: 0x0
[8]	FPOUT	RW	PWM output level of the first phase in a cycle Value After Reset: 0x0
[7:6]	EVTRIG	RW	Event triggering mode in one shot mode

Bits	Field Name	Access	Description
			1: Rising edge trigger 2: Falling edge trigger 0&3: General mode, that is, the output of PWM signal is not based on external signal. Value After Reset: 0x0
[5:4]	MODE	RW	PWM mode 1: One shot mode 2：Continuous mode 0&3: Reserved Value After Reset: 0x0
[3]	INTEN	RW	Interrupt enable 0: Disable 1: Enable Value After Reset: 0x0
[2]	CFG_UPDATE	RW	In continuous mode, the PWM_PER and PWM_FP registers are updated in the middle. When the register value is changed, the cfg_update is configured from 0 to 1 (indicating that both register values are updated at the same time). Value After Reset: 0x0
[1]	SOFT_RST	RW	The software reset enable is used to turn off PWM_cycle (PWM status[7:0]) at any time. Value After Reset: 0x0
[0]	START	RW	PWM start coding enable, rising edge effective (i.e. from 0 to 1) Value After Reset: 0x0

6.6.2.17 PWM_RPT_3

- Description: PWM channel 3 one shot control register
- Offset: 0x64
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	ONE_SHOT_RPT	RW	The number of cycles repeated in one shot transmission

Bits	Field Name	Access	Description
			Value After Reset: 0x0

6.6.2.18 PWM_PER_3

- Description: PWM channel 3 periodic control register
- Offset: 0x68
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_PER	RW	The number of beats of the system clock that a periodic waveform lasts. If PWM_per is 0, no PWM effective signal is output. Value After Reset: 0x0

6.6.2.19 PWM_FP_3

- Description: PWM channel 3 first phase control register
- Offset: 0x6c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_FP	RW	The number of beats in the first phase of a periodic waveform. If PWM_FP is larger than PWM_per, all effective signals are FPOUT. If PWM FP is 0, all effective signals are! FPOUT. Value After Reset: 0x0

6.6.2.20 PWM_STATUS_3

- Description: PWM channel 3 status register
- Offset: 0x70
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	PWM_OUT	RW	PWM current value of the waveform Value After Reset: 0x0
[8]	PWM_BUSY	RW	PWM state of the state machine 0: Idle 1: Busy

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[7:0]	PWM_CYCLE	RW	In continuous mode, the number of cycles that the same group of PWM_per & PWM_FP parameters have output. Value After Reset: 0x0

6.6.2.21 PWM_CTRL_4

- Description: PWM channel 4 control register
- Offset: 0x80
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	INACTOUT	RW	PWM output level when not enabled Value After Reset: 0x0
[8]	FPOUT	RW	PWM output level of the first phase in a cycle Value After Reset: 0x0
[7:6]	EVTRIG	RW	Event triggering mode in one shot mode 1: Rising edge trigger 2: Falling edge trigger 0&3: General mode, that is, the output of PWM signal is not based on external signal. Value After Reset: 0x0
[5:4]	MODE	RW	PWM mode 1: One shot mode 2: Continuous mode 0&3: Reserved Value After Reset: 0x0
[3]	INTEN	RW	Interrupt enable 0: Disable 1: Enable Value After Reset: 0x0
[2]	CFG_UPDATE	RW	In continuous mode, the PWM_PER and PWM_FP registers are updated in the middle. When the register value is changed, the cfg_update is configured from 0 to 1 (indicating that both register values are updated

Bits	Field Name	Access	Description
			at the same time). Value After Reset: 0x0
[1]	SOFT_RST	RW	The software reset enable is used to turn off PWM_cycle (PWM status[7:0]) at any time. Value After Reset: 0x0
[0]	START	RW	PWM start coding enable, rising edge effective (i.e. from 0 to 1) Value After Reset: 0x0

6.6.2.22 PWM_RPT_4

- Description: PWM channel 4 one shot control register
- Offset: 0x84
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	ONE_SHOT_RPT	RW	The number of cycles repeated in one shot transmission Value After Reset: 0x0

6.6.2.23 PWM_PER_4

- Description: PWM channel 4 periodic control register
- Offset: 0x88
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_PER	RW	The number of beats of the system clock that a periodic waveform lasts. If PWM_per is 0, no PWM effective signal is output. Value After Reset: 0x0

6.6.2.24 PWM_FP_4

- Description: PWM channel 4 first phase control register
- Offset: 0x8c
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_FP	RW	The number of beats in the first phase of a periodic waveform. If PWM_FP is larger than PWM_per, all effective signals are FPOUT. If PWM FP is 0, all effective signals are! FPOUT. Value After Reset: 0x0

6.6.2.25 PWM_STATUS_4

- Description: PWM channel 4 status register
- Offset: 0x90
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	PWM_OUT	RW	PWM current value of the waveform Value After Reset: 0x0
[8]	PWM_BUSY	RW	PWM state of the state machine 0: Idle 1: Busy Value After Reset: 0x0
[7:0]	PWM_CYCLE	RW	In continuous mode, the number of cycles that the same group of PWM_per & PWM_FP parameters have output. Value After Reset: 0x0

6.6.2.26 PWM_CTRL_5

- Description: PWM channel 5 control register
- Offset: 0xa0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	INACTOUT	RW	PWM output level when not enabled Value After Reset: 0x0
[8]	FPOUT	RW	PWM output level of the first phase in a cycle Value After Reset: 0x0
[7:6]	EVTRIG	RW	Event triggering mode in one shot mode

Bits	Field Name	Access	Description
			1: Rising edge trigger 2: Falling edge trigger 0&3: General mode, that is, the output of PWM signal is not based on external signal. Value After Reset: 0x0
[5:4]	MODE	RW	PWM mode 1: One shot mode 2: Continuous mode 0&3: Reserved Value After Reset: 0x0
[3]	INTEN	RW	Interrupt enable 0: Disable 1: Enable Value After Reset: 0x0
[2]	CFG_UPDATE	RW	In continuous mode, the PWM_PER and PWM_FP registers are updated in the middle. When the register value is changed, the cfg_update is configured from 0 to 1 (indicating that both register values are updated at the same time). Value After Reset: 0x0
[1]	SOFT_RST	RW	The software reset enable is used to turn off PWM_cycle (PWM status[7:0]) at any time. Value After Reset: 0x0
[0]	START	RW	PWM start coding enable, rising edge effective (i.e. from 0 to 1) Value After Reset: 0x0

6.6.2.27 PWM_RPT_5

- Description: PWM channel 5 one shot control register
- Offset: 0xa4
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:16]	RESERVED_1	-	
[15:0]	ONE_SHOT_RPT	RW	The number of cycles repeated in one shot transmission

Bits	Field Name	Access	Description
			Value After Reset: 0x0

6.6.2.28 PWM_PER_5

- Description: PWM channel 5 periodic control register
- Offset: 0xa8
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_PER	RW	The number of beats of the system clock that a periodic waveform lasts. If PWM_per is 0, no PWM effective signal is output. Value After Reset: 0x0

6.6.2.29 PWM_FP_5

- Description: PWM channel 5 first phase control register
- Offset: 0xac
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:0]	PWM_FP	RW	The number of beats in the first phase of a periodic waveform. If PWM_FP is larger than PWM_per, all effective signals are FPOUT. If PWM FP is 0, all effective signals are! FPOUT. Value After Reset: 0x0

6.6.2.30 PWM_STATUS_5

- Description: PWM channel 5 status register
- Offset: 0xb0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:10]	RESERVED_1	-	
[9]	PWM_OUT	RW	PWM current value of the waveform Value After Reset: 0x0
[8]	PWM_BUSY	RW	PWM state of the state machine 0: Idle 1: Busy

Bits	Field Name	Access	Description
			Value After Reset: 0x0
[7:0]	PWM_CYCLE	RW	In continuous mode, the number of cycles that the same group of PWM_per & PWM_FP parameters have output. Value After Reset: 0x0

6.6.2.31 PWM_INTR_STA

- Description: PWM Interrupt status register
- Offset: 0xff0
- Default Value: 0x0

Bits	Field Name	Access	Description
[31:6]	RESERVED_1	-	
[5]	PWM5_INTR	RO	PWM 5 interrupt status of output Value After Reset: 0x0
[4]	PWM4_INTR	RO	PWM 4 interrupt status of output Value After Reset: 0x0
[3]	PWM3_INTR	RO	PWM 3 interrupt status of output Value After Reset: 0x0
[2]	PWM2_INTR	RO	PWM 2 interrupt status of output Value After Reset: 0x0
[1]	PWM1_INTR	RO	PWM 1 interrupt status of output Value After Reset: 0x0
[0]	PWM0_INTR	RO	PWM 0 interrupt status of output Value After Reset: 0x0

7 I2C

7.1 Overview

The I2C bus provides support for the communications link between integrated circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters, CODECs, and many types of microprocessors.

There are 9 I2C instances in chip, 1 in always-on power domain, 2 in audio_subsys, 6 in power-down power domain.

7.2 Main Features

The I2C has the following features:

- Two-wire I2C serial interface - consists of a serial data line (SDA) and a serial clock (SCL)
- Three speeds:
  - Standard mode (0 to 100Kb/s)
  - Fast mode (⩽ 400Kb/s) or fast mode plus (⩽ 1000Kb/s)1
  - High-speed mode (⩽ 3.4Mb/s)
- Clock synchronization
- Master OR slave I2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- Bulk transmit mode
- Transmit and receive buffers
- Interrupt or polled-mode operation
- Handles bit and byte waiting at all bus speeds
- DMA handshaking interface
- Programmable SDA hold time (tHD;DAT)
- Bus clear feature
- Device ID feature

7.3 Interface

Figure & Table 7-1 Pin description table

Pin Name	Direction	Width	Description
I2C_AON_SCL	I/O	1	I2C clock signal, I2C in always-on power domain
I2C_AON_SDA	I/O	1	I2C data signal, I2C in always-on power domain

Pin Name	Direction	Width	Description
I2C[i]_SCL, i=0~5	I/O	1	I2C clock signal, I2C in power-down power domain
I2C[i]_SDA, i=0~5	I/O	1	I2C data signal, I2C in power-down power domain
AUDIO_PA6	I/O	1	I2C0 in audio_subsys, I2C0_SCL
AUDIO_PA7	I/O	1	I2C0 in audio_subsys, I2C0_SDA
AOGPIO_9	I/O	1	I2C1 in audio_subsys, I2C1_SCL
AOGPIO_10	I/O	1	I2C1 in audio_subsys, I2C1_SDA

I2C supports standard mode and fast mode. Its timing parameters are shown in Figure & Table 7-2.

Figure & Table 7-2 I2C standard-mode and fast-mode timing characteristic

Symbol	Parameter	Condition	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		-	-	0	50	ns
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated.	4.0	-	0.6	-	us
t_{LOW}	Low period of SCL clock		4.7	-	1.3	-	us
t_{HIGH}	High period of SCL clock		4.0	-	0.6	-	us
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	us
$t_{HD;DAT}$	Data hold time		5.0	-	-	-	us
$t_{SU;DAT}$	Data set-up time		250	-	100	-	ns
t_r	Rise time of both SDA and SCL		-	1000	20	300	ns
t_f	Fall time of both SDA and SCL		-	300	-	300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4.0	-	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	us
C_b	Capacitive load for each bus line		-	400	-	400	pF
$t_{VD;DAT}$	Data valid time		-	3.45	-	0.9	us

Symbol	Parameter	Condition	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
$t_{VD;ACK}$	Data valid acknowledge time		-	3.45	-	0.9	us

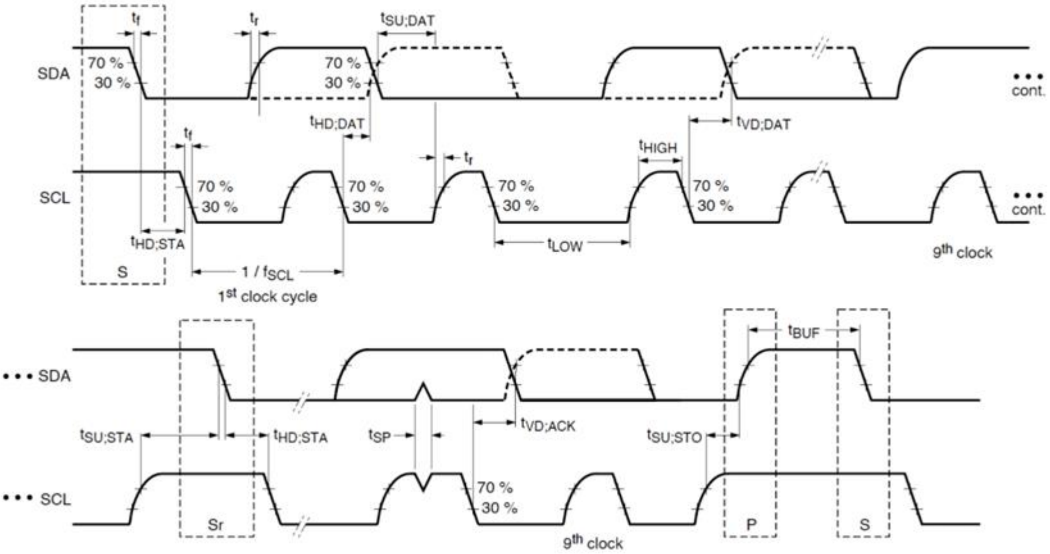

Figure & Table 7-3 I2C standard-mode and fast-mode timing characteristic

Figure & Table 7-4 I2C high-speed-mode timing characteristic

Symbol	Parameter	Condition	High Mode		Unit
			Min	Max	
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	10	ns
f_{SCL}	SCL clock frequency		0	3.4	MHz
$t_{SU;STA}$	Set-up time for a repeated START condition		160	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition		160	-	ns
t_{LOW}	Low period of SCL clock		160	-	ns
t_{HIGH}	High period of SCL clock		60	-	ns
$t_{SU;DAT}$	Data set-up time		10	-	ns
$t_{HD;DAT}$	Data hold time		0	70	ns
t_{rCL}	Rise time of SCL		10	40	ns
t_{rCL1}	Rise time of SCL after a repeated START condition and after an acknowledge bit		10	80	ns

Symbol	Parameter	Condition	High Mode		Unit
			Min	Max	
t_{fCL}	Fall time of SCL		10	40	ns
t_{rDA}	Rise time of SDA		10	80	ns
t_{fDA}	Fall time of SDA		10	80	ns
$t_{SU;STO}$	Set-up time for STOP condition		160	-	ns
C_b	Capacitive load for each bus line	SDA and SCL lines	-	100	pF

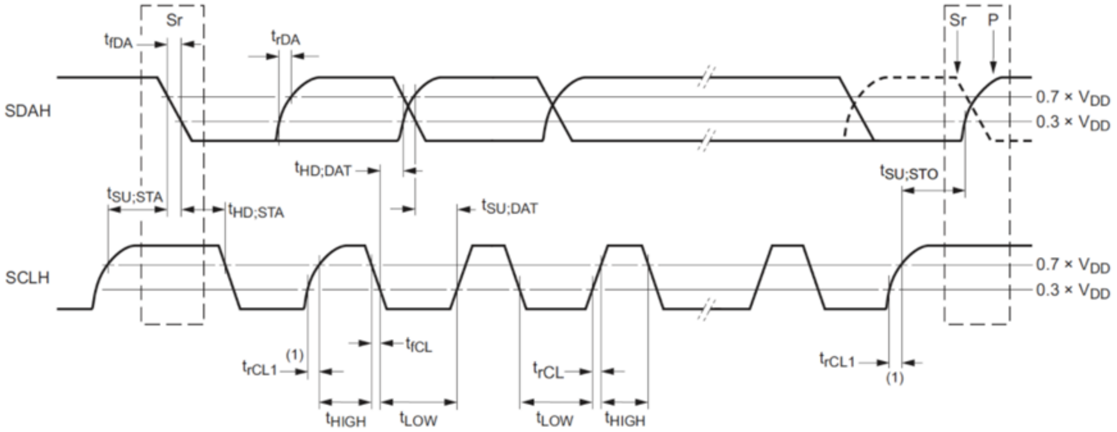

Figure & Table 7-5 I2C high-speed-mode timing characteristic

7.4 Usage

To use the I2C as a slave, perform the following steps:

1. Disable the I2C by writing 0 to bit 0 of the IC_ENABLE register.
2. Write to the IC_SAR register (bit[9:0]) to set the slave address. This is the address to which the I2C responds.
3. Write to the IC_CON register to specify which type of addressing is supported (7- or 10-bit by setting bit 3). Enable the I2C in slave-only mode by writing 0 into bit 6 (IC_SLAVE_DISABLE) and 0 to bit 0 (MASTER_MODE).
4. Enable the I2C by writing 1 in bit 0 of the IC_ENABLE register.

To use the I2C as a master when the I2C_DYNAMIC_TAR_UPDATE configuration

1. Disable the I2C by writing 0 to the IC_ENABLE register.
2. Write to the IC_CON register to set the maximum speed mode supported (bit[2:1]) and the desired speed of the I2C master-initiated transfers, either 7-bit or 10-bit addressing (bit 4). Ensure that bit 6 (IC_SLAVE_DISABLE) is written with 1 and bit 0 (MASTER_MODE) is written with 1.

3. Write to the IC_TAR register the address of the I2C device to be addressed (bit[9:0]). This register also indicates whether a General Call or a START BYTE command is going to be performed by I2C.
4. Only applicable for high-speed mode transfers. Write to the IC_HS_MADDR register the desired master code for the I2C. The master code is programmer-defined.
5. Enable the I2C by writing 1 in bit 0 of the IC_ENABLE register.
6. Now write transfer direction and data to be sent to the IC_DATA_CMD register. If the IC_DATA_CMD register is written before the I2C is enabled, the data and commands are lost as the buffers are kept cleared when I2C is disabled. This step generates the START condition and the address byte on the I2C. Once I2C is enabled and there is data in the TX FIFO, I2C starts reading the data.

7.5 Register Description

7.5.1 Register Memory Map

Register	Offset	Description	Section/Page
IC_CON	0x0	I2C Control Register	7.5.2.1/252
IC_TAR	0x4	I2C Target Address Register	7.5.2.2/256
IC_SAR	0x8	I2C Slave Address Register	7.5.2.3/258
IC_HS_MADDR	0xc	I2C High Speed Master Mode Code Address Register	7.5.2.4/259
IC_DATA_CMD	0x10	I2C Rx/Tx Data Buffer and Command Register	7.5.2.5/260
IC_SS_SCL_HCNT	0x14	Standard Speed I2C Clock SCL High Count Register	7.5.2.6/261
IC_SS_SCL_LCNT	0x18	Standard Speed I2C Clock SCL Low Count Register	7.5.2.7/262
IC_FS_SCL_HCNT	0x1c	Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register	7.5.2.8/263
IC_FS_SCL_LCNT	0x20	Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register	7.5.2.9/263
IC_HS_SCL_HCNT	0x24	High Speed I2C Clock SCL High Count Register	7.5.2.10/264
IC_HS_SCL_LCNT	0x28	High Speed I2C Clock SCL Low Count Register	7.5.2.11/265
IC_INTR_STAT	0x2c	I2C Interrupt Status Register	7.5.2.12/266
IC_INTR_MASK	0x30	I2C Interrupt Mask Register	7.5.2.13/270

Register	Offset	Description	Section/Page
IC_RAW_INTR_STAT	0x34	I2C Raw Interrupt Status Register	7.5.2.14/273
IC_RX_TL	0x38	I2C Receive FIFO Threshold Register	7.5.2.15/274
IC_TX_TL	0x3c	I2C Transmit FIFO Threshold Register	7.5.2.16/274
IC_CLR_INTR	0x40	Clear Combined and Individual Interrupt Register	7.5.2.17/275
IC_CLR_RX_UNDER	0x44	Clear RX_UNDER Interrupt Register	7.5.2.18/275
IC_CLR_RX_OVER	0x48	Clear RX_OVER Interrupt Register	7.5.2.19/276
IC_CLR_TX_OVER	0x4c	Clear TX_OVER Interrupt Register	7.5.2.20/276
IC_CLR_RD_REQ	0x50	Clear RD_REQ Interrupt Register	7.5.2.21/277
IC_CLR_TX_ABRT	0x54	Clear TX_ABRT Interrupt Register	7.5.2.22/277
IC_CLR_RX_DONE	0x58	Clear RX_DONE Interrupt Register	7.5.2.23/278
IC_CLR_ACTIVITY	0x5c	Clear ACTIVITY Interrupt Register	7.5.2.24/278
IC_CLR_STOP_DET	0x60	Clear STOP_DET Interrupt Register	7.5.2.25/279
IC_CLR_START_DET	0x64	Clear START_DET Interrupt Register	7.5.2.26/279
IC_CLR_GEN_CALL	0x68	Clear GEN_CALL Interrupt Register	7.5.2.27/280
IC_ENABLE	0x6c	I2C Enable Register	7.5.2.28/280
IC_STATUS	0x70	I2C Status Register	7.5.2.29/282
IC_TXFLR	0x74	I2C Transmit FIFO Level Register	7.5.2.30/285
IC_RXFLR	0x78	I2C Receive FIFO Level Register	7.5.2.31/286
IC_SDA_HOLD	0x7c	I2C SDA Hold Time Length Register	7.5.2.32/287
IC_TX_ABRT_SOURCE	0x80	I2C Transmit Abort Source Register	7.5.2.33/287
IC_DMA_CR	0x88	DMA Control Register	7.5.2.34/294
IC_DMA_TDLR	0x8c	DMA Transmit Data Level Register	7.5.2.35/295
IC_DMA_RDLR	0x90	I2C Receive Data Level Register	7.5.2.36/296
IC_SDA_SETUP	0x94	I2C SDA Setup Register	7.5.2.37/297
IC_ACK_GENERAL_CALL	0x98	I2C ACK General Call Register	7.5.2.38/297
IC_ENABLE_STATUS	0x9c	I2C Enable Status Register	7.5.2.39/298
IC_FS_SPKLEN	0xa0	I2C SS, FS or FM+ spike suppression limit	7.5.2.40/300
IC_HS_SPKLEN	0xa4	I2C HS spike suppression limit register	7.5.2.41/301

Register	Offset	Description	Section/Page
IC_SCL_STUCK_AT_LOW_TIMEOUT	0xac	I2C SCL Stuck at Low Timeout	7.5.2.42/302
IC_SDA_STUCK_AT_LOW_TIMEOUT	0xb0	I2C SDA Stuck at Low Timeout	7.5.2.43/302
IC_CLR_SCL_STUCK_DET	0xb4	Clear SCL Stuck at Low Detect Interrupt Register	7.5.2.44/303
REG_TIMEOUT_RST	0xf0	Register timeout counter reset value	7.5.2.45/303
IC_COMP_PARAM_1	0xf4	Component Parameter Register	7.5.2.46/304
IC_COMP_VERSION	0xf8	I2C Component Version Register	7.5.2.47/306
IC_COMP_TYPE	0xfc	I2C Component Type Register	7.5.2.48/306

7.5.2 Register and Field Description

7.5.2.1 IC_CON

- Name: I2C Control Register
- Description: This register can be written only when the DW_apb_i2c is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect.
- Size: 32 bits
- Offset: 0x0
- Exists: Always

Bits	Name	Access	Description
31:16	RSVD_IC_CON_2	R	IC_CON_2 Reserved bits - Read Only Exists: Always
15:12	RSVD_IC_CON_1	R	IC_CON_1 Reserved bits - Read Only Exists: Always
11	BUS_CLEAR_FEATURE_CTRL	R/W	In Master mode: ■ 1'b1: Bus Clear Feature is enabled. ■ 1'b0: Bus Clear Feature is disabled. In Slave mode, this register bit is not applicable. Values: ■ 0x1 (ENABLED): Bus Clear Feature is enabled. ■ 0x0 (DISABLED): Bus Clear Feature is disabled. Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
10	STOP_DET_IF_MASTER_ACTIVE	RO	In Master mode: ■ 1'b1: Issues the STOP_DET interrupt only when master is active. ■ 1'b0: Issues the STOP_DET irrespective of whether master is active or not. Values: ■ 0x1 (ENABLED): Master issues the STOP_DET interrupt only when master is active. ■ 0x0 (DISABLED): Master issues the STOP_DET interrupt irrespective of whether master is active or not. Value After Reset: 0x0 Exists: Always
9	RX_FIFO_FULL_HLD_CTRL	RO	This bit controls whether DW_apb_i2c should hold the bus when the Rx FIFO is physically full to its RX_BUFFER_DEPTH. Values: ■ 0x1 (ENABLED): Hold bus when RX_FIFO is full. ■ 0x0 (DISABLED): Overflow when RX_FIFO is full. Value After Reset: 0x0 Exists: Always
8	TX_EMPTY_CTRL	R/W	This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register. Values: ■ 0x1 (ENABLED): Controlled generation of TX_EMPTY interrupt ■ 0x0 (DISABLED): Default behavior of TX_EMPTY interrupt Value After Reset: 0x0 Exists: Always
7	STOP_DET_IFADDRESSED	R/W	In slave mode: ■ 1'b1: Issues the STOP_DET interrupt only when it is addressed. ■ 0'b0: Issues the STOP_DET irrespective of whether it's addressed or not. NOTE: During a general call address, this slave does not issue the STOP_DET interrupt if

Bits	Name	Access	Description
			STOP_DET_IF_ADDRESSED = 1'b1, even if the slave responds to the general call address by generating ACK. The STOP_DET interrupt is generated only when the transmitted address matches the slave address (SAR). Values: ■ 0x1 (ENABLED): Slave issues STOP_DET intr only if addressed. ■ 0x0 (DISABLED): Slave issues STOP_DET intr always. Value After Reset: 0x0 Exists: Always
6	IC_SLAVE_DISABLE	R/W	This bit controls whether I2C has its slave disabled, which means once the presetn signal is applied, then this bit takes on the value of the configuration parameter IC_SLAVE_DISABLE. You have the choice of having the slave enabled or disabled after reset is applied, which means software does not have to configure the slave. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave. NOTE: Software should ensure that if this bit is written with 0, then bit 0 should also be written with 0. Values: ■ 0x1 (SLAVE_DISABLED): Slave mode is disabled. ■ 0x0 (SLAVE_ENABLED): Slave mode is enabled. Value After Reset: IC_SLAVE_DISABLE Exists: Always
5	IC_RESTART_EN	R/W	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several DW_apb_i2c operations. When RESTART is disabled, the master is prohibited from performing the following functions: ■ Sending a START BYTE ■ Performing any high-speed mode operation ■ High-speed mode operation ■ Performing direction changes in combined format

Bits	Name	Access	Description
			mode ■ Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple DW_apb_i2c transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. Values: ■ 0x1 (ENABLED): Master restart enabled. ■ 0x0 (DISABLED): Master restart disabled. Value After Reset: IC_RESTART_EN Exists: Always
4	RSVD_IC_CON_1	R	IC_CON_1 Reserved bits - Read Only Exists: Always
3	IC_10BITADDR_SLAVE	R/W	When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses. ■ 0: 7-bit addressing. The DW_apb_i2c ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the IC_SAR register are compared. ■ 1: 10-bit addressing. The DW_apb_i2c responds to only 10-bit addressing transfers that match the full 10 bits of the IC_SAR register. Values: ■ 0x1 (ADDR_10BITS): Slave 10Bit addressing ■ 0x0 (ADDR_7BITS): Slave 7Bit addressing Value After Reset: IC_10BITADDR_SLAVE Exists: Always
2:1	SPEED	R/W	These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. These bits must be programmed appropriately for slave mode also, as it is used to capture correct value of spike filter as per the speed mode. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.

Bits	Name	Access	Description
			1: Standard mode (100kbit/s) 2: Fast mode (<= 400kbit/s) or fast mode plus (<1000Kbit/s) 3: High speed mode (3.4Mbit/s) Note: This field is not applicable when IC_ULTRA_FAST_MODE = 1. Values: ■ 0x1 (STANDARD): Standard speed mode of operation ■ 0x2 (FAST): Fast or Fast Plus mode of operation ■ 0x3 (HIGH): High speed mode of operation Value After Reset: IC_MAX_SPEED_MODE Exists: Always
0	MASTER_MODE	R/W	This bit controls whether the DW_apb_i2c master is enabled. NOTE: Software should ensure that if this bit is written with 1 then bit 6 should also be written with a 1. Values: ■ 0x1 (ENABLED): Master mode is enabled. ■ 0x0 (DISABLED): Master mode is disabled. Value After Reset: IC_MASTER_MODE Exists: Always

7.5.2.2 IC_TAR

- Name: I2C Target Address Register
- Description: If the configuration parameter I2C_DYNAMIC_TAR_UPDATE is set to 'No' (0), this register is 12 bits wide, and bits 31:12 are reserved. This register can be written to only when IC_ENABLE[0] is set to 0.
  However, if I2C_DYNAMIC_TAR_UPDATE = 1, then the register becomes 13 bits wide. In this case, writes to IC_TAR succeed when one of the following conditions are true:
  - DW_apb_i2c is NOT enabled (IC_ENABLE[0] is set to 0); or
  - DW_apb_i2c is enabled (IC_ENABLE[0] = 1); DW_apb_i2c is NOT engaged in any Master (tx, rx) operation (IC_STATUS[5] = 0); DW_apb_i2c is enabled to operate in Master mode (IC_CON[0] = 1); there are NO entries in the TX FIFO (IC_STATUS[2] = 1).

  You can change the TAR address dynamically without losing the bus, only if the following conditions are met.

   - DW_apb_i2c is enabled (IC_ENABLE[0] = 1); IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter is set to 1; DW_apb_i2c is enabled to operate in Master mode (IC_CON[0] = 1); there are NO entries in the Tx FIFO and the master is in HOLD state (IC_INTR_STAT[13] = 1).

  Note: If the software or application is aware that the DW_apb_i2c is not using the TAR address for the pending commands in the Tx FIFO, then it is possible to update the TAR address even while the Tx FIFO has entries (IC_STATUS[2] = 0).

   - It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

- Size: 32 bits
- Offset: 0x4
- Exists: Always

Bits	Name	Access	Description
31:13	RSVD_IC_TAR	R	IC_TAR_2 Reserved bits - Read Only Exists: Always
12	IC_10BITADDR_MASTER	R/W	This bit controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. ■ 0: 7-bit addressing ■ 1: 10-bit addressing Values: ■ 0x1 (ADDR_10BITS): Address 10Bit transmission format ■ 0x0 (ADDR_7BITS): Address 7Bit transmission format Value After Reset: IC_10BITADDR_MASTER Exists: Always
11	SPECIAL	R/W	This bit indicates whether software performs a Device-ID or General Call or START BYTE command. ■ 0: Ignore bit 10 GC_OR_START and use IC_TAR normally. ■ 1: Perform special I2C command as specified in Device_ID or GC_OR_START bit. Values: ■ 0x1 (ENABLED): Enables programming of GENERAL_CALL or START_BYTE transmission. ■ 0x0 (DISABLED): Disables programming of GENERAL_CALL or START_BYTE transmission. Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
10	GC_OR_START	R/W	If bit 11 (SPECIAL) is set to 1 and bit 13(Device-ID) is set to 0, then this bit indicates whether a General Call or START byte command is to be performed by the DW_apb_i2c. ■ 0: General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The DW_apb_i2c remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. ■ 1: START BYTE Values: ■ 0x1 (START_BYTE): START byte transmission ■ 0x0 (GENERAL_CALL): GENERAL_CALL byte transmission Value After Reset: 0x0 Exists: Always
9:0	IC_TAR	R/W	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave. Value After Reset: IC_DEFAULT_TAR_SLAVE_ADDR Exists: Always

7.5.2.3 IC_SAR

- Name: I2C Slave Address Register
- Description: I2C Slave Address Register
- Size: 32 bits
- Offset: 0x8
- Exists: Always

Bits	Name	Access	Description
31:10	RSVD_IC_SAR	R	IC_SAR Reserved bits - Read Only Exists: Always

Bits	Name	Access	Description
9:0	IC_SAR	R/W	The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the IC_SAR or IC_TAR to a reserved value. Refer to Table "I2C/SMBus Definition of Bits in First Byte" for a complete list of these reserved values. Value After Reset: IC_DEFAULT_SLAVE_ADDR Exists: Always

7.5.2.4 IC_HS_MADDR

- Name: I2C High Speed Master Mode Code Address Register
- Description: I2C High Speed Master Mode Code Address Register
- Size: 32 bits
- Offset: 0xc
- Exists: Always

Bits	Name	Access	Description
31:3	RSVD_IC_HS_MAR	R	IC_HS_MAR Reserved bits - Read Only Exists: Always
2:0	IC_HS_MAR	R/W	This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high-speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Value After Reset: IC_HS_MASTER_CODE

Bits	Name	Access	Description
			Exists: Always

7.5.2.5 IC_DATA_CMD

- Name: I2C Rx/Tx Data Buffer and Command Register
- Description: I2C Rx/Tx Data Buffer and Command Register. This is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO.

  The size of the register changes as follows:

  Write:

  – 11 bits when IC_EMPTYFIFO_HOLD_MASTER_EN = 1

  – 9 bits when IC_EMPTYFIFO_HOLD_MASTER_EN = 0

  Read:

  – 12 bits when IC_FIRST_DATA_BYTE_STATUS = 1

  – bits when IC_FIRST_DATA_BYTE_STATUS = 0

  Note: In order for the DW_apb_i2c to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise, the DW_apb_i2c will stop acknowledging.
- Size: 32 bits
- Offset: 0x10
- Exists: Always

Bits	Name	Access	Description
31:9	RSVD_IC_DATA_CMD	R	IC_DATA_CMD Reserved bits - Read Only Exists: Always Volatile: true
8	CMD	W	This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after

			receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs. Values: ■ 0x1 (READ): Master Read Command ■ 0x0 (WRITE): Master Write Command Value After Reset: 0x0 Exists: Always Volatile: True
7:0	DAT	R/W	This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.6 IC_SS_SCL_HCNT

- Name: Standard Speed I2C Clock SCL High Count Register
- Description: Standard Speed I2C Clock SCL High Count Register
- Size: 32 bits
- Offset: 0x14
- Exists: Always

Bits	Name	Access	Description
31:16	RSVD_IC_SS_SCL_HIGH_COUNT	R	IC_SS_SCL_HCNT Reserved bits - Read Only Exists: Always
15:0	IC_SS_SCL_HCNT	R/W	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for standard speed. For more information, refer to "IC_CLK Frequency Configuration". This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is

Bits	Name	Access	Description
			important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. NOTE: This register must not be programmed to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10. Value After Reset: IC_SS_SCL_HIGH_COUNT Exists: Always

7.5.2.7 IC_SS_SCL_LCNT

- Name: Standard Speed I2C Clock SCL Low Count Register
- Description: Standard Speed I2C Clock SCL Low Count Register
- Size: 32 bits
- Offset: 0x18
- Exists: Always

Bits	Name	Access	Description
31:16	RSVD_IC_SS_SCL_LOW_COUNT	R	RSVD_IC_SS_SCL_LOW_COUNT Reserved bits - Read Only Exists: Always
15:0	IC_SS_SCL_LCNT	R/W	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. For more information, refer to "IC_CLK Frequency Configuration" This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set. For designs with APB_DATA_WIDTH = 8, the order of programming is important to ensure the correct operation of DW_apb_i2c. The lower byte must be programmed first, and then the upper byte is programmed. When the configuration parameter

Bits	Name	Access	Description
			IC_HC_COUNT_VALUES is set to 1, this register is read only. Value After Reset: IC_SS_SCL_LOW_COUNT Exists: Always

7.5.2.8 IC_FS_SCL_HCNT

- Name: Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register
- Description: Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register
- Size: 32 bits
- Offset: 0x1c
- Exists: Always

Bits	Name	Access	Description
31:16	RSVD_IC_FS_SCL_HCNT	R	IC_FS_SCL_HCNT Reserved bits - Read Only Exists: Always
15:0	IC_FS_SCL_HCNT	R/W	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast mode or fast mode plus. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to "IC_CLK Frequency Configuration". This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. Value After Reset: IC_FS_SCL_HIGH_COUNT Exists: Always

7.5.2.9 IC_FS_SCL_LCNT

- Name: Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register

- Description: Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register
- Size: 32 bits
- Offset: 0x20
- Exists: Always

Bits	Name	Access	Description
31:16	RSVD_IC_FS_SCL_LCNT	R	IC_FS_SCL_LCNT Reserved bits - Read Only Exists: Always
15:0	IC_FS_SCL_LCNT	R/W	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. It is used in high speed mode to send the Master Code and START BYTE or General CALL. For more information, refer to "IC_CLK Frequency Configuration". This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE = standard. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. When the configuration parameter IC_HC_COUNT_VALUES is set to 1, this register is read only. Value After Reset: IC_FS_SCL_LOW_COUNT Exists: Always

7.5.2.10 IC_HS_SCL_HCNT

- Name: High Speed I2C Clock SCL High Count Register
- Description: High Speed I2C Clock SCL High Count Register
- Size: 32 bits
- Offset: 0x24
- Exists: Always

Bits	Name	Access	Description
31:16	RSVD_IC_HS_SCL_HCNT	R	IC_HS_SCL_HCNT Reserved bits - Read Only Exists: Always
15:0	IC_HS_SCL_HCNT	R/W	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high period count for high speed, refer to "IC_CLK Frequency Configuration". The SCL High time depends on the loading of the bus. For 100pF loading, the SCL High time is 60ns; for 400pF loading, the SCL High time is 120ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set. For designs with APB_DATA_WIDTH = 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. Value After Reset: IC_HS_SCL_HIGH_COUNT Exists: Always

7.5.2.11 IC_HS_SCL_LCNT

- Name: High Speed I2C Clock SCL Low Count Register
- Description: High Speed I2C Clock SCL Low Count Register
- Size: 32 bits
- Offset: 0x28
- Exists: Always

Bits	Name	Access	Description
31:16	RSVD_IC_HS_SCL_LOW_CNT	R	IC_HS_SCL_LCNT Reserved bits - Read Only Exists: Always
15:0	IC_HS_SCL_LCNT	R/W	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. For more information, refer to "IC_CLK Frequency Configuration".

Bits	Name	Access	Description
			The SCL low time depends on the loading of the bus. For 100pF loading, the SCL low time is 160ns; for 400pF loading, the SCL low time is 320ns. This register goes away and becomes read-only returning 0s if IC_MAX_SPEED_MODE != high. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted results in 8 being set. For designs with APB_DATA_WIDTH == 8 the order of programming is important to ensure the correct operation of the DW_apb_i2c. The lower byte must be programmed first. Then the upper byte is programmed. If the value is less than 8 then the count value gets changed to 8. Value After Reset: IC_HS_SCL_LOW_COUNT Exists: Always

7.5.2.12 IC_INTR_STAT

- Name: I2C Interrupt Status Register
- Description: I2C Interrupt Status Register
  Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the IC_RAW_INTR_STAT register.
- Size: 32 bits
- Offset: 0x2c
- Exists: Always

Bits	Name	Access	Description
31:15	RSVD_IC_INTR_STAT	R	IC_INTR_STAT Reserved bits - Read Only Exists: Always Volatile: True
14	R_SCL_STUCK_AT_LOW	R	See IC_RAW_INTR_STAT for a detailed description of R_SCL_STUCK_AT_LOW bit. Values: ■ 0x1 (ACTIVE): R_SCL_STUCK_AT_LOW interrupt is active. ■ 0x0 (INACTIVE): R_SCL_STUCK_AT_LOW interrupt is

Bits	Name	Access	Description
			inactive. Value After Reset: 0x0 Exists: Always Volatile: True
13	R_MASTER_ON_HOLD	R	See IC_RAW_INTR_STAT for a detailed description of R_MASTER_ON_HOLD bit. Values: ■ 0x1 (ACTIVE): R_MASTER_ON_HOLD interrupt is active. ■ 0x0 (INACTIVE): R_MASTER_ON_HOLD interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
12	R_RESTART_DET	R	See IC_RAW_INTR_STAT for a detailed description of R_RESTART_DET bit. Values: ■ 0x1 (ACTIVE): R_RESTART_DET interrupt is active. ■ 0x0 (INACTIVE): R_RESTART_DET interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
11	R_GEN_CALL	R	See IC_RAW_INTR_STAT for a detailed description of R_GEN_CALL bit. Values: ■ 0x1 (ACTIVE): R_GEN_CALL interrupt is active. ■ 0x0 (INACTIVE): R_GEN_CALL interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
10	R_START_DET	R	See IC_RAW_INTR_STAT for a detailed description of R_START_DET bit. Values: ■ 0x1 (ACTIVE): R_START_DET interrupt is active. ■ 0x0 (INACTIVE): R_START_DET interrupt is inactive.

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: Always Volatile: True
9	R_STOP_DET	R	See IC_RAW_INTR_STAT for a detailed description of R_STOP_DET bit. Values: ■ 0x1 (ACTIVE): R_STOP_DET interrupt is active. ■ 0x0 (INACTIVE): R_STOP_DET interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
8	R_ACTIVITY	R	See IC_RAW_INTR_STAT for a detailed description of R_ACTIVITY bit. Values: ■ 0x1 (ACTIVE): R_ACTIVITY interrupt is active. ■ 0x0 (INACTIVE): R_ACTIVITY interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
7	R_RX_DONE	R	See IC_RAW_INTR_STAT for a detailed description of R_RX_DONE bit. Values: ■ 0x1 (ACTIVE): R_RX_DONE interrupt is active. ■ 0x0 (INACTIVE): R_RX_DONE interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
6	R_TX_ABRT	R	See IC_RAW_INTR_STAT for a detailed description of R_TX_ABRT bit. Values: ■ 0x1 (ACTIVE): R_TX_ABRT interrupt is active. ■ 0x0 (INACTIVE): R_TX_ABRT interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True

Bits	Name	Access	Description
5	R_RD_REQ	R	See IC_RAW_INTR_STAT for a detailed description of R_RD_REQ bit. Values: ■ 0x1 (ACTIVE): R_RD_REQ interrupt is active. ■ 0x0 (INACTIVE): R_RD_REQ interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
4	R_TX_EMPTY	R	See IC_RAW_INTR_STAT for a detailed description of R_TX_EMPTY bit. Values: ■ 0x1 (ACTIVE): R_TX_EMPTY interrupt is active. ■ 0x0 (INACTIVE): R_TX_EMPTY interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
3	R_TX_OVER	R	See IC_RAW_INTR_STAT for a detailed description of R_TX_OVER bit. Values: ■ 0x1 (ACTIVE): R_TX_OVER interrupt is active. ■ 0x0 (INACTIVE): R_TX_OVER interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
2	R_RX_FULL	R	See IC_RAW_INTR_STAT for a detailed description of R_RX_FULL bit. Values: ■ 0x1 (ACTIVE): R_RX_FULL interrupt is active. ■ 0x0 (INACTIVE): R_RX_FULL interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
1	R_RX_OVER	R	See IC_RAW_INTR_STAT for a detailed description of R_RX_OVER bit. Values: ■ 0x1 (ACTIVE): R_RX_OVER interrupt is active.

Bits	Name	Access	Description
			■ 0x0 (INACTIVE): R_RX_OVER interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True
0	R_RX_UNDER	R	See IC_RAW_INTR_STAT for a detailed description of R_RX_UNDER bit. Values: ■ 0x1 (ACTIVE): RX_UNDER interrupt is active. ■ 0x0 (INACTIVE): RX_UNDER interrupt is inactive. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.13 IC_INTR_MASK

- Name: I2C Interrupt Mask Register
- Description: I2C Interrupt Mask Register
  These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.
- Size: 32 bits
- Offset: 0x30
- Exists: Always

Bits	Name	Access	Description
31:15	RSVD_IC_INTR_STAT	R	IC_INTR_STAT Reserved bits - Read Only Exists: Always
14	M_SCL_STUCK_AT_LOW	R/W	This bit masks the R_SCL_STUCK_AT_LOW interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): SCL_STUCK_AT_LOW interrupt is unmasked. ■ 0x0 (ENABLED): SCL_STUCK_AT_LOW interrupt is masked. Value After Reset: 0x1 Exists: Always
13:12	RSVD_IC_INTR_STAT_1	R	IC_INTR_STAT Reserved bits - Read Only Exists: Always

Bits	Name	Access	Description
11	M_GEN_CALL	R/W	This bit masks the R_GEN_CALL interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): GEN_CALL interrupt is unmasked. ■ 0x0 (ENABLED): GEN_CALL interrupt is masked. Value After Reset: 0x1 Exists: Always
10	M_START_DET	R/W	This bit masks the R_START_DET interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): START_DET interrupt is unmasked. ■ 0x0 (ENABLED): START_DET interrupt is masked. Value After Reset: 0x0 Exists: Always
9	M_STOP_DET	R/W	This bit masks the R_STOP_DET interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): STOP_DET interrupt is unmasked. ■ 0x0 (ENABLED): STOP_DET interrupt is masked. Value After Reset: 0x0 Exists: Always
8	M_ACTIVITY	R/W	This bit masks the R_ACTIVITY interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): ACTIVITY interrupt is unmasked. ■ 0x0 (ENABLED): ACTIVITY interrupt is masked. Value After Reset: 0x0 Exists: Always
7	M_RX_DONE	R/W	This bit masks the R_RX_DONE interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): RX_DONE interrupt is unmasked. ■ 0x0 (ENABLED): RX_DONE interrupt is masked. Value After Reset: 0x1 Exists: Always

Bits	Name	Access	Description
6	M_TX_ABRT	R/W	This bit masks the R_TX_ABRT interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): TX_ABORT interrupt is unmasked. ■ 0x0 (ENABLED): TX_ABORT interrupt is masked. Value After Reset: 0x1 Exists: Always
5	M_RD_REQ	R/W	This bit masks the R_RD_REQ interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): RD_REQ interrupt is unmasked. ■ 0x0 (ENABLED): RD_REQ interrupt is masked. Value After Reset: 0x1 Exists: Always
4	M_TX_EMPTY	R/W	This bit masks the R_TX_EMPTY interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): TX_EMPTY interrupt is unmasked. ■ 0x0 (ENABLED): TX_EMPTY interrupt is masked. Value After Reset: 0x1 Exists: Always
3	M_TX_OVER	R/W	This bit masks the R_TX_OVER interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): TX_OVER interrupt is unmasked. ■ 0x0 (ENABLED): TX_OVER interrupt is masked. Value After Reset: 0x1 Exists: Always
2	M_RX_FULL	R/W	This bit masks the R_RX_FULL interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): RX_FULL interrupt is unmasked. ■ 0x0 (ENABLED): RX_FULL interrupt is masked. Value After Reset: 0x1 Exists: Always

Bits	Name	Access	Description
1	M_RX_OVER	R/W	This bit masks the R_RX_OVER interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): RX_OVER interrupt is unmasked. ■ 0x0 (ENABLED): RX_OVER interrupt is masked. Value After Reset: 0x1 Exists: Always
0	M_RX_UNDER	R/W	This bit masks the R_RX_UNDER interrupt in IC_INTR_STAT register. Values: ■ 0x1 (DISABLED): RX_UNDER interrupt is unmasked. ■ 0x0 (ENABLED): RX_UNDER interrupt is masked. Value After Reset: 0x1 Exists: Always

7.5.2.14 IC_RAW_INTR_STAT

- Name: I2C Raw Interrupt Status Register
- Description: I2C Raw Interrupt Status Register
  Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the DW_apb_i2c.
- Size: 32 bits
- Offset: 0x34
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_ACTIVITY	R	IC_CLR_ACTIVITY Reserved bits - Read Only Exists: Always Volatile: true
0	CLR_ACTIVITY	R	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always

Bits	Name	Access	Description
			Volatile: True

7.5.2.15 IC_RX_TL

- Name: I2C Receive FIFO Threshold Register
- Description: I2C Receive FIFO Threshold Register
- Size: 32 bits
- Offset: 0x38
- Exists: Always

Bits	Name	Access	Description
31:8	RSVD_IC_RX_TL	R	IC_RX_TL Reserved bits - Read Only Exists: Always
7:0	RX_TL	R/W	Receive FIFO Threshold Level Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries. Value After Reset: 0x0 Exists: Always

7.5.2.16 IC_TX_TL

- Name: I2C Transmit FIFO Threshold Register
- Description: I2C Transmit FIFO Threshold Register
- Size: 32 bits
- Offset: 0x3c
- Exists: Always

Bits	Name	Access	Description
31:8	RSVD_IC_TX_TL	R	IC_TX_TL Reserved bits - Read Only Exists: Always
7:0	TX_TL	R/W	Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional

Bits	Name	Access	Description
			restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries. Value After Reset: 0x0 Exists: Always

7.5.2.17 IC_CLR_INTR

- Name: Clear Combined and Individual Interrupt Register
- Description: Clear Combined and Individual Interrupt Register
- Size: 32 bits
- Offset: 0x40
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_INTR	R	CLR_INTR Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_INTR	R	Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.18 IC_CLR_RX_UNDER

- Name: Clear RX_UNDER Interrupt Register
- Description: Clear RX_UNDER Interrupt Register
- Size: 32 bits
- Offset: 0x44
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_RX_UNDER	R	IC_CLR_RX_UNDER Reserved bits - Read Only Exists: Always

Bits	Name	Access	Description
			Volatile: True
0	CLR_RX_UNDER	R	Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.19 IC_CLR_RX_OVER

- Name: Clear RX_OVER Interrupt Register
- Description: Clear RX_OVER Interrupt Register
- Size: 32 bits
- Offset: 0x48
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_RX_OVER	R	IC_CLR_RX_OVER Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_RX_OVER	R	Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.20 IC_CLR_TX_OVER

- Name: Clear TX_OVER Interrupt Register
- Description: Clear TX_OVER Interrupt Register
- Size: 32 bits
- Offset: 0x4c
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_TX_OVER	R	IC_CLR_TX_OVER Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_TX_OVER	R	Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.21 IC_CLR_RD_REQ

- Name: Clear RD_REQ Interrupt Register
- Description: Clear RD_REQ Interrupt Register
- Size: 32 bits
- Offset: 0x50
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_RD_REQ	R	IC_CLR_RD_REQ Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_RD_REQ	R	Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.22 IC_CLR_TX_ABRT

- Name: Clear TX_ABRT Interrupt Register
- Description: Clear TX_ABRT Interrupt Register
- Size: 32 bits
- Offset: 0x54
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_TX_ABRT	R	IC_CLR_TX_ABRT Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_TX_ABRT	R	Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing

Bits	Name	Access	Description
			IC_TX_ABRT_SOURCE. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.23 IC_CLR_RX_DONE

- Name: Clear RX_DONE Interrupt Register
- Description: Clear RX_DONE Interrupt Register
- Size: 32 bits
- Offset: 0x58
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_RX_DONE	R	IC_CLR_RX_DONE Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_RX_DONE	R	Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.24 IC_CLR_ACTIVITY

- Name: Clear ACTIVITY Interrupt Register
- Description: Clear ACTIVITY Interrupt Register
- Size: 32 bits
- Offset: 0x5c
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_ACTIVITY	R	IC_CLR_ACTIVITY Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_ACTIVITY	R	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on

Bits	Name	Access	Description
			the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.25 IC_CLR_STOP_DET

- Name: Clear STOP_DET Interrupt Register
- Description: Clear STOP_DET Interrupt Register
- Size: 32 bits
- Offset: 0x60
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_STOP_DET	R	IC_CLR_STOP_DET Reserved bits - Read Only Exists: Always Volatile: true
0	CLR_STOP_DET	R	Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.26 IC_CLR_START_DET

- Name: Clear START_DET Interrupt Register
- Description: Clear START_DET Interrupt Register
- Size: 32 bits
- Offset: 0x64
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_START_DET	R	IC_CLR_START_DET Reserved bits - Read Only Exists: Always Volatile: true
0	CLR_START_DET	R	Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.27 IC_CLR_GEN_CALL

- Name: Clear GEN_CALL Interrupt Register
- Description: Clear GEN_CALL Interrupt Register
- Size: 32 bits
- Offset: 0x68
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_CLR_GEN_CALL	R	IC_CLR_GEN_CALL Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_GEN_CALL	R	Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.28 IC_ENABLE

- Name: I2C ENABLE Register
- Description: I2C Enable Register
- Size: 32 bits
- Offset: 0x6c
- Exists: Always

Bits	Name	Access	Description
31:4	RSVD_IC_ENABLE_2	R	IC_ENABLE Reserved bits - Read Only Exists: Always
3	SDA_STUCK_RECOVERY_ENABLE	R/W	If SDA is stuck at low indicated through the TX_ABORT interrupt (IC_TX_ABRT_SOURCE[17]), then this bit is used as a control knob to initiate the SDA Recovery Mechanism (that is, send at most 9 SCL clocks and STOP to release the SDA line) and then this bit gets auto clear Values: ■ 0x1 (SDA_STUCK_RECOVERY_ENABLED): Master

Bits	Name	Access	Description
			initiates the SDA stuck at low recovery mechanism. ■ 0x0 (SDA_STUCK_RECOVERY_DISABLED): Master disabled the SDA stuck at low recovery mechanism. Value After Reset: 0x0 Exists: Always
2	TX_CMD_BLOCK	R/W	In Master mode: ■ 1'b1: Blocks the transmission of data on I2C bus even if Tx FIFO has data to transmit. ■ 1'b0: The transmission of data starts on I2C bus automatically, as soon as the first data is available in the Tx FIFO. Note: To block the execution of Master commands, set the TX_CMD_BLOCK bit only when Tx FIFO is empty (IC_STATUS[2]==1) and Master is in Idle state (IC_STATUS[5] == 0). Any further commands put in the Tx FIFO are not executed until TX_CMD_BLOCK bit is unset. Values: ■ 0x1 (BLOCKED): Tx Command execution blocked. ■ 0x0 (NOT_BLOCKED): Tx Command execution not blocked. Value After Reset: 0x0 Exists: Always
1	ABORT	R/W	When set, the controller initiates the transfer abort. ■ 0: ABORT not initiated or ABORT done ■ 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation. For a detailed description on how to abort I2C transfers, refer to "Aborting I2C Transfers". Values:

Bits	Name	Access	Description
			■ 0x1 (ENABLED): ABORT operation in progress ■ 0x0 (DISABLE): ABORT operation not in progress Value After Reset: 0x0 Exists: Always
0	ENABLE	R/W	Controls whether the DW_apb_i2c is enabled. ■ 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state). ■ 1: Enables DW_apb_i2c. Software can disable DW_apb_i2c while it is active. However, it is important that care be taken to ensure that DW_apb_i2c is disabled properly. A recommended procedure is described in "Disabling DW_apb_i2c". When DW_apb_i2c is disabled, the following occurs: ■ The TX FIFO and RX FIFO get flushed. ■ Status bits in the IC_INTR_STAT register are still active until DW_apb_i2c goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the DW_apb_i2c stops the current transfer at the end of the current byte and does not acknowledge the transfer. In systems with asynchronous pclk and ic_clk when IC_CLK_TYPE parameter set to asynchronous (1), there is a two ic_clk delay when enabling or disabling the DW_apb_i2c. For a detailed description on how to disable DW_apb_i2c, refer to "Disabling DW_apb_i2c" Values: ■ 0x1 (ENABLED): I2C is enabled. ■ 0x0 (DISABLED): I2C is disabled. Value After Reset: 0x0 Exists: Always

7.5.2.29 C_STATUS

- Name: I2C STATUS Register
- Description: I2C Status Register

  This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

  When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:

  – Bits 1 and 2 are set to 1.

- Bits 3 and 10 are set to 0.

When the master or slave state machines goes to idle and ic_en = 0:

- Bits 5 and 6 are set to 0.

- Size: 32 bits
- Offset: 0x70
- Exists: Always

Bits	Name	Access	Description
31:12	RSVD_IC_STATUS_2	R	IC_STATUS Reserved bits - Read Only Exists: Always Volatile: True
11	SDA_STUCK_NOT_RECOVERED	R	This bit indicates that SDA stuck at low is not recovered after the recovery mechanism. In Slave mode, this register bit is not applicable. Values: ■ 0x1 (ACTIVE): SDA Stuck at low is recovered after recovery mechanism. ■ 0x0 (INACTIVE): SDA Stuck at low is not recovered after recovery mechanism. Value After Reset: 0x0 Exists: Always Volatile: True
10:7	RSVD_IC_STATUS_1	R	IC_STATUS Reserved bits - Read Only Exists: Always Volatile: True
6	SLV_ACTIVITY	R	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. ■ 0: Slave FSM is in IDLE state so the Slave part of DW_apb_i2c is not active. ■ 1: Slave FSM is not in IDLE state so the Slave part of DW_apb_i2c is active. Values: ■ 0x1 (ACTIVE): Slave not idle. ■ 0x0 (IDLE): Slave is idle. Value After Reset: 0x0 Exists: Always Volatile: True
5	MST_ACTIVITY	R	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bits	Name	Access	Description
			■ 0: Master FSM is in IDLE state so the Master part of DW_apb_i2c is not active. ■ 1: Master FSM is not in IDLE state so the Master part of DW_apb_i2c is active. Note: IC_STATUS[0]-that is, ACTIVITY bit-is the OR of SLV_ACTIVITY and MST_ACTIVITY bits. Values: ■ 0x1 (ACTIVE): Master not idle. ■ 0x0 (IDLE): Master is idle. Value After Reset: 0x0 Exists: Always Volatile: True
4	RFF	R	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. ■ 0: Receive FIFO is not full. ■ 1: Receive FIFO is full. Values: ■ 0x1 (FULL): Rx FIFO is full. ■ 0x0 (NOT_FULL): Rx FIFO not full. Value After Reset: 0x0 Exists: Always Volatile: True
3	RFNE	R	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. ■ 0: Receive FIFO is empty. ■ 1: Receive FIFO is not empty. Values: ■ 0x1 (NOT_EMPTY): Rx FIFO not empty. ■ 0x0 (EMPTY): Rx FIFO is empty. Value After Reset: 0x0 Exists: Always Volatile: True
2	TFE	R	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared.

Bits	Name	Access	Description
			This bit field does not request an interrupt. ■ 0: Transmit FIFO is not empty. ■ 1: Transmit FIFO is empty. Values: ■ 0x1 (EMPTY): Tx FIFO is empty. ■ 0x0 (NON_EMPTY): Tx FIFO not empty. Value After Reset: 0x1 Exists: Always Volatile: True
1	TFNF	R	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. ■ 0: Transmit FIFO is full. ■ 1: Transmit FIFO is not full. Values: ■ 0x1 (NOT_FULL): Tx FIFO not full. ■ 0x0 (FULL): Tx FIFO is full. Value After Reset: 0x1 Exists: Always Volatile: True
0	ACTIVITY	R	I2C Activity Status Values: ■ 0x1 (ACTIVE): I2C is active. ■ 0x0 (INACTIVE): I2C is idle. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.30 IC_TXFLR

- Name: I2C Transmit FIFO Level Register
- Description: I2C Transmit FIFO Level Register
  This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:
  - The I2C is disabled.
  - There is a transmit abort - that is, TX_ABRT bit is set in the IC_RAW_INTR_STAT register.
  - The slave bulk transmit mode is aborted.

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

- Size: 32 bits
- Offset: 0x74
- Exists: Always

Bits	Name	Access	Description
31:5	RSVD_TXFLR	R	TXFLR Register field Reserved bits - Read Only Exists: Always Volatile: True
4:0	TXFLR	R	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.31 IC_RXFLR

- Name: I2C Receive FIFO Level Register
- Description: I2C Receive FIFO Level Register

  This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever:

  - The I2C is disabled.
  - Whenever there is a transmit abort caused by any of the events tracked in IC_TX_ABRT_SOURCE.

  The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.
- Size: 32 bits
- Offset: 0x78
- Exists: Always

Bits	Name	Access	Description
31:5	RSVD_RXFLR	R	RXFLR Reserved bits - Read Only Exists: Always Volatile: True
4:0	RXFLR	R	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.32 IC_SDA_HOLD

- Name: I2C SDA Hold Time Length Register
- Description: I2C SDA Hold Time Length Register
  The bits [15:0] of this register are used to control the hold time of SDA during transmit in both slave and master mode (after SCL goes from high to low).
  The bits [23:16] of this register are used to extend the SDA transition (if any) whenever SCL is high in the receiver in either master or slave mode.
  Writes to this register succeed only when IC_ENABLE[0] = 0.
  The values in this register are in units of ic_clk period. The value programmed in IC_SDA_TX_HOLD must be greater than the minimum hold time in each mode one cycle in master mode, seven cycles in slave mode for the value to be implemented.
  The programmed SDA hold time during transmit (IC_SDA_TX_HOLD) cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in ic_clk cycles.
- Size: 32 bits
- Offset: 0x7c
- Exists: Always

Bits	Name	Access	Description
31:24	RSVD_IC_SDA_HOLD	R	IC_SDA_HOLD Reserved bits - Read Only Exists: Always
23:16	IC_SDA_RX_HOLD	R/W	Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a receiver. Value After Reset: 0x0 Exists: Always
15:0	IC_SDA_TX_HOLD	R/W	Sets the required SDA hold time in units of ic_clk period, when DW_apb_i2c acts as a transmitter. Value After Reset: 0x1 Exists: Always

7.5.2.33 IC_TX_ABRT_SOURCE

- Name: I2C Transmit Abort Source Register
- Description: I2C Transmit Abort Source Register
  This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5] = 1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]).

Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

- Size: 32 bits
- Offset: 0x80
- Exists: Always

Bits	Name	Access	Description
31:23	TX_FLUSH_CNT	R	This field indicates the number of Tx FIFO Data Commands which are flushed due to TX_ABRT interrupt. It is cleared whenever I2C is disabled. Role of DW_apb_i2c: Master-Transmitter or Slave-Transmitter Value After Reset: 0x0 Exists: Always Volatile: True
22:18	RSVD_IC_TX_ABRT_SOURCE	R	IC_TX_ABRT_SOURCE Reserved bits - Read Only Exists: Always Volatile: True
17	ABRT_SDA_STUCK_AT_LOW	R	This is a master-mode-only bit. Master detects the SDA Stuck at low for the IC_SDA_STUCK_AT_LOW_TIMEOUT value of ic_clks. Role of DW_apb_i2c: Master Values: ■ 0x1 (ACTIVE): This abort is generated because of Sda stuck at low for IC_SDA_STUCK_AT_LOW_TIMEOUT value of ic_clks. ■ 0x0 (INACTIVE): This abort is not generated. Value After Reset: 0x0 Exists: Always Volatile: True
16	ABRT_USER_ABRT	R	This is a master-mode-only bit. Master has detected the transfer abort (IC_ENABLE[1]). Role of DW_apb_i2c: Master-Transmitter Values: ■ 0x1 (ABRT_USER_ABRT_GENERATED): Transfer abort detected by master. ■ 0x0 (ABRT_USER_ABRT_VOID): Transfer abort detected by master- scenario not present.

Bits	Name	Access	Description
			Value After Reset: 0x0 Exists: Always Volatile: True
15	ABRT_SLVRD_INTX	R	1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Role of DW_apb_i2c: Slave-Transmitter Values: ■ 0x1 (ABRT_SLVRD_INTX_GENERATED): Slave trying to transmit to remote master in read mode. ■ 0x0 (ABRT_SLVRD_INTX_VOID): Slave trying to transmit to remote master in read mode- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
14	ABRT_SLV_ARBLOST	R	This field indicates that a Slave has lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then DW_apb_i2c no longer own the bus. Role of DW_apb_i2c: Slave-Transmitter Values: ■ 0x1 (ABRT_SLV_ARBLOST_GENERATED): Slave lost arbitration to remote master. ■ 0x0 (ABRT_SLV_ARBLOST_VOID): Slave lost arbitration to remote master- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
13	ABRT_SLVFLUSH_TXFIFO	R	This field specifies that the Slave has received a read command and some data exists in the TX FIFO, so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.

Bits	Name	Access	Description
			Role of DW_apb_i2c: Slave-Transmitter Values: ■ 0x1 (ABRT_SLVFLUSH_TXFIFO_GENERATED): Slave flushes existing data in TX-FIFO upon getting read command. ■ 0x0 (ABRT_SLVFLUSH_TXFIFO_VOID): Slave flushes existing data in TX-FIFO upon getting read command- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
12	ARB_LOST	R	This field specifies that the Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Role of DW_apb_i2c: Master-Transmitter or Slave Transmitter Values: ■ 0x1 (ABRT_LOST_GENERATED): Master or Slave Transmitter lost arbitration. ■ 0x0 (ABRT_LOST_VOID): Master or Slave-Transmitter lost arbitration- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
11	ABRT_MASTER_DIS	R	This field indicates that the User tries to initiate a Master operation with the Master mode disabled. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver Values: ■ 0x1 (ABRT_MASTER_DIS_GENERATED): User initiating master operation when MASTER disabled. ■ 0x0 (ABRT_MASTER_DIS_VOID): User initiating master operation when MASTER disabled- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True

Bits	Name	Access	Description
10	ABRT_10B_RD_NORSTRT	R	This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) =0) and the master sends a read command in 10-bit addressing mode. Role of DW_apb_i2c: Master-Receiver Values: ■ 0x1 (ABRT_10B_RD_GENERATED): Master trying to read in 10Bit addressing mode when RESTART disabled. ■ 0x0 (ABRT_10B_RD_VOID): Master not trying to read in 10Bit addressing mode when RESTART disabled. Value After Reset: 0x0 Exists: Always Volatile: True
9	ABRT_SBYTE_NORSTRT	R	To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5] = 1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets reasserted. When this field is set to 1, the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte. Role of DW_apb_i2c: Master Values: ■ 0x1 (ABRT_SBYTE_NORSTRT_GENERATED): User trying to send START byte when RESTART disabled. ■ 0x0 (ABRT_SBYTE_NORSTRT_VOID): User trying to send START byte when RESTART disabled- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
8	ABRT_HS_NORSTRT	R	This field indicates that the restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. Role of DW_apb_i2c: Master-Transmitter or Master

Bits	Name	Access	Description
			Receiver Values: ■ 0x1 (ABRT_HS_NORSTRT_GENERATED): User trying to switch Master to HS mode when RESTART disabled. ■ 0x0 (ABRT_HS_NORSTRT_VOID): User trying to switch Master to HS mode when RESTART disabled-scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
7	ABRT_SBYTE_ACKDET	R	This field indicates that the Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Role of DW_apb_i2c: Master Values: ■ 0x1 (ABRT_SBYTE_ACKDET_GENERATED): ACK detected for START byte. ■ 0x0 (ABRT_SBYTE_ACKDET_VOID): ACK detected for START byte- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
6	ABRT_HS_ACKDET	R	This field indicates that the Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Role of DW_apb_i2c: Master Values: ■ 0x1 (ABRT_HS_ACK_GENERATED): HS Master code ACKed in HS Mode. ■ 0x0 (ABRT_HS_ACK_VOID): HS Master code ACKed in HS Mode- scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
5	ABRT_GCALL_READ	R	This field indicates that DW_apb_i2c in the master mode has sent a General Call but the user programmed the byte following the General Call to be a read from

Bits	Name	Access	Description
			the bus (IC_DATA_CMD[9] is set to 1). Role of DW_apb_i2c: Master-Transmitter Values: ■ 0x1 (ABRT_GCALL_READ_GENERATED): GCALL is followed by read from bus. ■ 0x0 (ABRT_GCALL_READ_VOID): GCALL is followed by read from bus-scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
4	ABRT_GCALL_NOACK	R	This field indicates that DW_apb_i2c in master mode has sent a General Call and no slave on the bus acknowledged the General Call. Role of DW_apb_i2c: Master-Transmitter Values: ■ 0x1 (ABRT_GCALL_NOACK_GENERATED): GCALL not ACKed by any slave. ■ 0x0 (ABRT_GCALL_NOACK_VOID): GCALL not ACKed by any slave-scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
3	ABRT_TXDATA_NOACK	R	This field indicates the master-mode only bit. When the master receives an acknowledgement for the address, but when it sends data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Role of DW_apb_i2c: Master-Transmitter Values: ■ 0x1 (ABRT_TXDATA_NOACK_GENERATED): Transmitted data not ACKed by addressed slave. ■ 0x0 (ABRT_TXDATA_NOACK_VOID): Transmitted data non-ACKed by addressed slave-scenario not present. Value After Reset: 0x0 Exists: Always Volatile: True
2	ABRT_10ADDR2_NOACK	R	This field indicates that the Master is in 10-bit address

Bits	Name	Access	Description
			mode and that the second address byte of the 10-bit address was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master Receiver Values: ■ 0x1 (ACTIVE): Byte 2 of 10Bit Address not ACKed by any slave. ■ 0x0 (INACTIVE): This abort is not generated. Value After Reset: 0x0 Exists: Always Volatile: True
1	ABRT_10ADDR1_NOACK	R	This field indicates that the Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0 Role of DW_apb_i2c: Master-Transmitter or Master-Receiver Values: ■ 0x1 (ACTIVE): Byte 1 of 10Bit Address not ACKed by any slave. ■ 0x0 (INACTIVE): This abort is not generated. Exists: Always Volatile: True
0	ABRT_7B_ADDR_NOACK	R	This field indicates that the Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Role of DW_apb_i2c: Master-Transmitter or Master-Receiver Values: ■ 0x1 (ACTIVE): This abort is generated because of NOACK for 7-bit address. ■ 0x0 (INACTIVE): This abort is not generated. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.34 IC_DMA_CR

- Name: DMA Control Register

- Description: DMA Control Register
  This register is only valid when DW_apb_i2c is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register address will return zero. The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.
- Size: 32 bits
- Offset: 0x88
- Exists: Always

Bits	Name	Access	Description
31:2	RSVD_IC_DMA_CR_2_31	R	RSVD_IC_DMA_CR_2_31 Reserved bits - Read Only Exists: Always
1	TDMAE	R/W	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. Values: ■ 0x1 (ENABLED): Transmit FIFO DMA channel enabled. ■ 0x0 (DISABLED): transmit FIFO DMA channel disabled. Value After Reset: 0x0 Exists: Always
0	RDMAE	R/W	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. Values: ■ 0x1 (ENABLED): Receive FIFO DMA channel enabled. ■ 0x0 (DISABLED): Receive FIFO DMA channel disabled. Value After Reset: 0x0 Exists: Always

7.5.2.35 IC_DMA_TDLR

- Name: DMA Transmit Data Level Register
- Description: DMA Transmit Data Level Register
  This register is only valid when the DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.
- Size: 32 bits

- Offset: 0x8c
- Exists: Always

Bits	Name	Access	Description
31:4	RSVD_DMA_TDLR	R	DMA_TDLR Reserved bits - Read Only Exists: Always
3:0	DMATDL	R/W	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1. Value After Reset: 0x0 Exists: Always

7.5.2.36 IC_DMA_RDLR

- Name: DMA Receive Data Level Register
- Description: DMA Receive Data Level Register
  This register is only valid when DW_apb_i2c is configured with a set of DMA interface signals (IC_HAS_DMA = 1). When DW_apb_i2c is not configured for DMA operation, this register does not exist; writing to its address has no effect; reading from its address returns zero.
- Size: 32 bits
- Offset: 0x90
- Exists: Always

Bits	Name	Access	Description
31:4	RSVD_DMA_RDLR	R	DMA_RDLR Reserved bits - Read Only Exists: Always
3:0	DMARDL	R/W	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE = 1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO. Value After Reset: 0x0 Exists: Always

7.5.2.37 IC_SDA_SETUP

- Name: I2C SDA Setup Register
- Description: I2C SDA Setup Register
  This register controls the amount of time delay (in terms of number of ic_clk clock periods) introduced in the rising edge of SCL - relative to SDA changing - when DW_apb_i2c services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT (note 4) as detailed in the I2C Bus Specification. This register must be programmed with a value equal to or greater than 2.
  Writes to this register succeed only when IC_ENABLE[0] = 0.
  Note: The length of setup time is calculated using [(IC_SDA_SETUP - 1)*(ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11. The IC_SDA_SETUP register is only used by the DW_apb_i2c when operating as a slave transmitter.
- Size: 32 bits
- Offset: 0x94
- Exists: Always

Bits	Name	Access	Description
31:8	RSVD_IC_SDA_SETUP	R	IC_SDA_SETUP Reserved bits - Read Only Exists: Always
7:0	SDA_SETUP	R/W	SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10MHz, IC_SDA_SETUP should be programmed to a value of 11. IC_SDA_SETUP must be programmed with a minimum value of 2. Value After Reset: 0x64 Exists: Always

7.5.2.38 IC_ACK_GENERAL_CALL

- Name: I2C ACK General Call Register
- Description: I2C ACK General Call Register
  The register controls whether DW_apb_i2c responds with an ACK or NACK when it receives an I2C General Call address.
  This register is applicable only when the DW_apb_i2c is in slave mode.
- Size: 32 bits
- Offset: 0x98
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_IC_ACK_GEN_1_31	R	RSVD_IC_ACK_GEN_1_31 Reserved bits - Read Only

Bits	Name	Access	Description
			Exists: Always
0	ACK_GEN_CALL	R/W	ACK General Call. When set to 1, DW_apb_i2c responds with an ACK (by asserting ic_data_oe) when it receives a General Call. Otherwise, DW_apb_i2c responds with a NACK (by negating ic_data_oe). Values: ■ 0x1 (ENABLED): Generate ACK for a General Call. ■ 0x0 (DISABLED): Generate NACK for a General Call. Value After Reset: 0x1 Exists: Always

7.5.2.39 IC_ENABLE_STATUS

- Name: I2C Enable Status Register
- Description: I2C Enable Status Register
  The register is used to report the DW_apb_i2c hardware status when the IC_ENABLE[0] register is set from 1 to 0; that is, when DW_apb_i2c is disabled.
  If IC_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
  If IC_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as 0.
  Note: When IC_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the DW_apb_i2c depends on I2C bus activities.
- Size: 32 bits
- Offset: 0x9c
- Exists: Always

Bits	Name	Access	Description
31:3	RSVD_IC_ENABLE_STATUS	R	IC_ENABLE_STATUS Reserved bits - Read Only Exists: Always Volatile: True
2	SLV_RX_DATA_LOST	R	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting bit 0 of IC_ENABLE from 1 to 0. When read as 1, DW_apb_i2c is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a

Bits	Name	Access	Description
			chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0. Values: ■ 0x1 (ACTIVE): Slave RX Data is lost. ■ 0x0 (INACTIVE): Slave RX Data is not lost. Value After Reset: 0x0 Exists: Always Volatile: True
1	SLV_DISABLED_WHILE_BUSY	R	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting bit 0 of the IC_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the IC_ENABLE register while: DW_apb_i2c is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, DW_apb_i2c is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in DW_apb_i2c (IC_SAR register) OR if the transfer is completed before IC_ENABLE is set to 0 but has not taken effect. Note: If the remote I2C master terminates the transfer with a STOP condition before the DW_apb_i2c has a chance to NACK a transfer, and IC_ENABLE[0] has been set to 0, then this bit will also be set to 1. When read as 0, DW_apb_i2c is deemed to have been disabled when there is master activity, or when the I2C bus is idle. Note: The CPU can safely read this bit when IC_EN (bit 0) is read as 0. Values: ■ 0x1 (ACTIVE): Slave is disabled when it is active.

Bits	Name	Access	Description
			■ 0x0 (INACTIVE): Slave is disabled when it is idle. Value After Reset: 0x0 Exists: Always Volatile: True
0	IC_EN	R	ic_en Status. This bit always reflects the value driven on the output port ic_en. ■ When read as 1, DW_apb_i2c is deemed to be in an enabled state. ■ When read as 0, DW_apb_i2c is deemed completely inactive. Note: The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLV_RX_DATA_LOST (bit 2) and SLV_DISABLED_WHILE_BUSY (bit 1). Values: ■ 0x1 (ENABLED): I2C enabled. ■ 0x0 (DISABLED): I2C disabled. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.40 IC_FS_SPKLEN

- Name: I2C SS, FS or FM+ spike suppression limit
- Description: I2C SS, FS or FM+ spike suppression limit
  This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS, FS or FM+ modes. The relevant I2C requirement is tSP (table 4) as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.
- Size: 32 bits
- Offset: 0xa0
- Exists: Always

Bits	Name	Access	Description
31:8	RSVD_IC_FS_SPKLEN	R	IC_FS_SPKLEN Reserved bits - Read Only Exists: Always
7:0	IC_FS_SPKLEN	R/W	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the

Bits	Name	Access	Description
			longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set. For more information, refer to "Spike Suppression". Value After Reset: 0x1 Exists: Always

7.5.2.41 IC_HS_SPKLEN

- Name: I2C HS spike suppression limit register
- Description: I2C HS spike suppression limit register
  This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. The relevant I2C requirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1 and is implemented only if the component is configured to support HS mode; that is, if the IC_MAX_SPEED_MODE parameter is set to 3.
- Size: 32 bits
- Offset: 0xa4
- Exists: Always

Bits	Name	Access	Description
31:8	RSVD_IC_HS_SPKLEN	R	IC_HS_SPKLEN Reserved bits - Read Only Exists: Always
7:0	IC_HS_SPKLEN	R/W	This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that will be filtered out by the spike suppression logic; for more information, refer to "Spike Suppression". This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 1 being set. Value After Reset: 0x1

Bits	Name	Access	Description
			Exists: Always

7.5.2.42 IC_SCL_STUCK_AT_LOW_TIMEOUT

- Name: I2C SCL Stuck at Low Timeout register
- Description: I2C SCL Stuck at Low Timeout
  This register is used to store the duration, measured in ic_clk cycles, used to generate an interrupt (SCL_STUCK_AT_LOW) if SCL is held low for the IC_SCL_STUCK_LOW_TIMEOUT duration.
- Size: 32 bits
- Offset: 0xac
- Exists: Always

Bits	Name	Access	Description
31:0	IC_SCL_STUCK_LOW_TIMEOUT	R/W	DW_apb_i2c generate the interrupt to indicate SCL stuck at low (SCL_STUCK_AT_LOW) if it detects the SCL stuck at low for the IC_SCL_STUCK_LOW_TIMEOUT in units of ic_clk period. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE[0] register being set to 0. Writes at other times have no effect. Value After Reset: 0xFFFFFFFF Exists: Always

7.5.2.43 IC_SDA_STUCK_AT_LOW_TIMEOUT

- Name: I2C SDA Stuck at Low Timeout register
- Description: I2C SDA Stuck at Low Timeout
  This register is used to store the duration, measured in ic_clk cycles, used to recover the data (SDA) line through sending SCL pulses if SDA is held low for the mentioned duration.
- Size: 32 bits
- Offset: 0xb0
- Exists: Always

Bits	Name	Access	Description
31:0	IC_SDA_STUCK_LOW_TIMEOUT	R/W	DW_apb_i2c initiates the recovery of SDA line through enabling the SDA_STUCK_RECOVERY_EN (IC_ENABLE[3]) register bit, if it detects the SDA stuck at low for the IC_SDA_STUCK_LOW_TIMEOUT in units of ic_clk period. Value After Reset: 0xFFFFFFFF Exists: Always

7.5.2.44 IC_CLR_SCL_STUCK_DET

- Name: Clear SCL Stuck at Low Detect Interrupt Register
- Description: Clear SCL Stuck at Low Detect Interrupt Register
- Size: 32 bits
- Offset: 0xb4
- Exists: Always

Bits	Name	Access	Description
31:1	RSVD_CLR_SCL_STUCK_DET	R	CLR_SCL_STUCK_DET Reserved bits - Read Only Exists: Always Volatile: True
0	CLR_SCL_STUCK_DET	R	Read this register to clear the SCL_STUCT_AT_LOW interrupt (bit 15) of the IC_RAW_INTR_STAT register. Value After Reset: 0x0 Exists: Always Volatile: True

7.5.2.45 REG_TIMEOUT_RST

- Name: Register timeout counter reset value
- Description: This register keeps the timeout value of register timer counter. The reset value of the register is REG_TIMEOUT_VALUE. The default reset value can be further modified if HC_REG_TIMEOUT_VALUE = 0. The final programmed value (or the default reset value if not programmed) determines from what value the register timeout counter starts counting down. A zero on this counter will break the waited transaction with PSLVERR as high.
- Size: 32 bits
- Offset: 0xf0
- Exists: Always

Bits	Name	Access	Description
31:4	RSVD_REG_TIMEOUT_RST	R	Reserved bits - Read Only Exists: Always Volatile: True
3:0	REG_TIMEOUT_RST_ro	R	This field holds reset value of REG_TIMEOUT counter register. Value After Reset: REG_TIMEOUT_VALUE Exists: Always Volatile: True

7.5.2.46 IC_COMP_PARAM_1

- Name: Component Parameter Register 1
- Description: Component Parameter Register 1
  Note: This is a constant read-only register that contains encoded information about the component's parameter settings. The reset value depends on coreConsultant parameter(s).
- Size: 32 bits
- Offset: 0xf4
- Exists: Always

Bits	Name	Access	Description
31:24	RSVD_IC_COMP_PARAM_1	R	IC_COMP_PARAM_1 Reserved bits - Read Only Exists: Always
23:16	TX_BUFFER_DEPTH	R	The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter. ■ 0x00 = Reserved ■ 0x01 = 2 ■ 0x02 = 3 ■ ... ■ 0xFF = 256 Value After Reset: 0xF Exists: Always
15:8	RX_BUFFER_DEPTH	R	The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter. ■ 0x00: Reserved ■ 0x01: 2 ■ 0x02: 3 ■ ... ■ 0xFF: 256 Value After Reset: 0xF Exists: Always
7	ADD_ENCODED_PARAMS	R	The value of this register is derived from the IC_ ADD_ENCODED_PARAMS coreConsultant parameter. Reading 1 in this bit means that the capability of reading these encoded parameters via software has been included. Otherwise, the entire register is 0 regardless of the setting of any other parameters that are encoded in the bits.

Bits	Name	Access	Description
			Values: ■ 0x1 (ENABLED): Enables capability of reading encoded parameters. ■ 0x0 (DISBALED): Disables capability of reading encoded parameters. Value After Reset: 0x1 Exists: Always
6	HAS_DMA	R	The value of this register is derived from the IC_HAS_DMA coreConsultant parameter. Values: ■ 0x1 (ENABLED): DMA handshaking signals are enabled. ■ 0x0 (DISABLED): DMA handshaking signals are disabled. Value After Reset: 0x1 Exists: Always
5	INTR_IO	R	The value of this register is derived from the IC_INTR_IO coreConsultant parameter. Values: ■ 0x1 (COMBINED): COMBINED Interrupt outputs ■ 0x0 (INDIVIDUAL): INDIVIDUAL Interrupt outputs Value After Reset: 0x1 Exists: Always
4	HC_COUNT_VALUES	R	The value of this register is derived from the IC_HC_COUNT VALUES coreConsultant parameter. Values: ■ 0x1 (ENABLED): Hard code the count values for each mode. ■ 0x0 (DISABLED): Programmable count values for each mode. Value After Reset: 0x0 Exists: Always
3:2	MAX_SPEED_MODE	R	The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter. ■ 0x0: Reserved ■ 0x1: Standard ■ 0x2: Fast

Bits	Name	Access	Description
			■ 0x3: High Values: ■ 0x1 (STANDARD): IC MAX SPEED is STANDARD MODE. ■ 0x2 (FAST): IC MAX SPEED is FAST MODE. ■ 0x3 (HIGH): IC MAX SPEED is HIGH MODE. Value After Reset: 0x3 Exists: Always
1:0	APB_DATA_WIDTH	R	The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter. Values: ■ 0x0 (APB_08BITS): APB data bus width is 08 bits. ■ 0x1 (APB_16BITS): APB data bus width is 16 bits. ■ 0x2 (APB_32BITS): APB data bus width is 32 bits. ■ 0x3 (RESERVED): Reserved bits Value After Reset: 0x2 Exists: Always

7.5.2.47 IC_COMP_VERSION

- Name: I2C Component Version Register
- Description: I2C Component Version Register
- Size: 32 bits
- Offset: 0xf8
- Exists: Always

Bits	Name	Access	Description
31:0	IC_COMP_VERSION	R	Specific values for this register are described in the Releases Table in the DW_apb_i2c Release Notes. Value After Reset: 0x3230322A Exists: Always

7.5.2.48 IC_COMP_TYPE

- Name: I2C Component Type Register
- Description: I2C Component Type Register
- Size: 32 bits
- Offset: 0xfc
- Exists: Always

Bits	Name	Access	Description
31:0	IC_COMP_TYPE	R	Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters 'DW' followed by a 16-bit unsigned number. Value After Reset: 0x44570140 Exists: Always

8 UART

8.1 Overview

The UART is modeled after the industry-standard 16550. UART is used for serial communication with external devices. Data is written from the host device (CPU) to the UART through the APB bus, converted to a serial format and transmitted to the target device. The UART also receives serial data and stores it for readback by the host (CPU).

The UART contains registers for controlling character length, baud rate, parity generation/check, and interrupt generation. There are several types of UART priority interrupts that can cause the UART to be set, which in turn generates an interrupt. The control register enables/disables each interrupt type individually.

To reduce the time required by the UART for the host, the FIFO can be used to buffer the transmit and receive data. The host does not have to access the UART each time a byte of data is received.

The UART can be connected to the DMA controller via a dedicated channel to indicate when data can be read or when the Transmit FIFO is empty.

16750-compatible Auto Flow Control Mode improves system efficiency and reduces software load. When FIFO and Auto Flow Control are enabled, the serial data flow is automatically controlled by request send output (rts_n) and clear send input (cts_n).

8.2 Main Features

The UART supports the following features:

- There are 8 UART interface modules in the TH1520 chip, UART0~5, AUDUART and AOUART
- 9-bit serial data support
- False start bit detection signals
- Programmable fractional baud rate support
- Functionality based on the 16550 industry standard
- Multi-drop RS485 interface support
- IrDA 1.0 SIR mode support with up to 115.2Kbaud data of UART3 and AOUART
- Auto Flow Control mode of UART, as specified in the 16750 standard

8.3 Interface

Figure & Table 8-1 Pin description table

Pin Name	Direction	Width	Description
AOUART_RXD	IO	1	Serial data receive signal
AOUART_TXD	IO	1	Serial data send signal

Pin Name	Direction	Width	Description
AOUART_IR_IN	IO	1	Serial data receive signal in SIR mode
AOUART_IR_OUT	IO	1	Serial data send signal in SIR mode
UART[0~5]_RXD	IO	1	Serial data receive signal
UART[0~5]_TXD	IO	1	Serial data send signal
UART3_IR_IN	IO	1	Serial data receive signal in SIR mode
UART3_IR_OUT	IO	1	Serial data send signal in SIR mode
UART4_CTSN	IO	1	Flow control signal
UART4_RTSN	IO	1	Flow control signal

8.4 Function Description

Because the serial communication between the UART and a selected device is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. Utilizing these bits allows two devices to be synchronized. This structure of serial data–accompanied by start and stop bit is referred to as a character, as shown in Figure & Table 8-2.

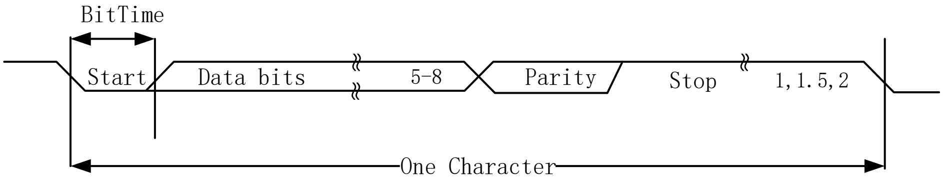

Figure & Table 8-2 UART serial data format

An additional parity bit can be added to the serial character. This bit appears after the last data bit and before the stop bits in the character structure in order to provide the UART with the ability to perform simple error checking on the received data.

When an interrupt occurs, the master accesses the IIR register. The following interrupt types can be enabled with the IER register:

- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in programmable THRE interrupt mode)
- Modem Status
- Busy Detect Indication

8.5 Usage

Programming Flow in RS485 Mode

- Full Duplex Mode (XFER_MODE = 0)

1. Program the TCR register to set the XFER_MODE (0), DE_POL (polarity of the 'de' signal) and RE_POL (polarity of the 're' signal).
2. Program the DE assertion and de-assertion timing in the DET register.
3. Program RE_EN and DE_EN registers to assert the 're' signal and 'de' signal respectively.
4. Perform the data transmission and reception.
5. Program RE_EN to de-assert the 're' signal.
6. 'The de' signal gets de-asserted based on TX FIFO empty. Program DE_EN to 0 if you do not want to transmit further.

- Software-Enabled Half Duplex Mode (XFER_MODE = 1)

1. Program the TCR register to set the XFER_MODE (1), DE_POL (polarity of the 'de' signal) and RE_POL (polarity of the 're' signal).
2. Program the DE assertion and de-assertion timing in the DET register.
3. Program the turnaround times in the TAT register.
4. Program RE_EN and DE_EN registers to assert the 're' signal and 'de' signal respectively.
5. Perform the data transmission/reception.
6. Program the RE_EN register to de-assert the 're' signal.
7. Program the DE_EN register to 0, before programming RE_EN to 1.

- Hardware enabled Half Duplex mode (XFER_MODE = 2)

1. Program the TCR register to set the XFER_MODE (2), DE_POL (polarity of the 'de' signal) and RE_POL (polarity of the 're' signal).
2. Program the DE assertion and de-assertion timing in the DET register.
3. Program the turnaround times in the TAT register.
4. Program RE_EN and DE_EN registers to enable the transmit and receive paths.
5. Perform the Data transmission/reception.
6. Once the 'RE_EN' and 'DE_EN' is programmed to 1, then by default the 're' signal is asserted and 'de' is de-asserted. When the software pushes the data into the TX FIFO and if there is no ongoing receive transfer, then the 're' signal is de-asserted and then the 'de' signal gets asserted until TX FIFO has data to be transmitted.
7. RE_EN and DE_EN still serves as the software overrides to decide when to shutdown transmit and receive paths.

8.6 Register Description

8.6.1 Register Memory Map

Register	Offset	Description	Section/Page
RBR	0x0	Receive Buffer Register	8.6.2.1/312
DLL	0x0	Divisor Latch (Low)	8.6.2.2/313
THR	0x0	Transmit Holding Register	8.6.2.3/313

Register	Offset	Description	Section/Page
DLH	0x4	Divisor Latch High (DLH) Register	8.6.2.4/314
IER	0x4	Interrupt Enable Register	8.6.2.5/315
FCR	0x8	FIFO Control Register	8.6.2.6/316
IIR	0x8	Interrupt Identification Register	8.6.2.7/319
LCR	0xc	Line Control Register	8.6.2.8/320
MCR	0x10	Modem Control Register	8.6.2.9/322
LSR	0x14	Line Status Register	8.6.2.10/325
MSR	0x18	Modem Status Register	8.6.2.11/330
SCR	0x1c	Scratchpad Register	8.6.2.12/333
LPDLL	0x20	Low Power Divisor Latch Low Register	8.6.2.13/333
LPDLH	0x24	Low Power Divisor Latch High Register	8.6.2.14/334
SRBRn (for n = 0; n <= 15)	0x30 + n*0x4	Shadow Receive Buffer Register	8.6.2.15/335
STHRn (for n = 0; n <= 15)	0x30 + n*0x4	Shadow Transmit Holding Register	8.6.2.16/335
FAR	0x70	FIFO Access Register	8.6.2.17/336
TFR	0x74	Transmit FIFO Read	8.6.2.18/336
RFW	0x78	Receive FIFO Write	8.6.2.19/337
USR	0x7c	UART Status Register	8.6.2.20/338
TFL	0x80	Transmit FIFO Level	8.6.2.21/340
RFL	0x84	Receive FIFO Level	8.6.2.22/340
SRR	0x88	Software Reset Register	8.6.2.23/340
SRTS	0x8c	Shadow Request to Send	8.6.2.24/341
SBCR	0x90	Shadow Break Control Register	8.6.2.25/342
SDMAM	0x94	Shadow DMA Mode Register	8.6.2.26/343
SFE	0x98	Shadow FIFO Enable Register	8.6.2.27/343
SRT	0x9c	Shadow RCVR Trigger Register	8.6.2.28/344
STET	0xa0	Shadow TX Empty Trigger Register	8.6.2.29/345
HTX	0xa4	Halt TX	8.6.2.30/345

Register	Offset	Description	Section/Page
DMASA	0xa8	DMA Software Acknowledge Register	8.6.2.31/346
TCR	0xac	Transceiver Control Register	8.6.2.32/346
DE_EN	0xb0	Driver Output Enable Register	8.6.2.33/348
RE_EN	0xb4	Receiver Output Enable Register	8.6.2.34/348
DET	0xb8	Driver Output Enable Timing Register (DET)	8.6.2.35/348
TAT	0xbc	TurnAround Timing Register	8.6.2.36/349
DLF	0xc0	Divisor Latch Fraction Register	8.6.2.37/350
RAR	0xc4	Receive Address Register	8.6.2.38/350
TAR	0xc8	Transmit Address Register	8.6.2.39/351
LCR_EXT	0xcc	Line Extended Control Register	8.6.2.40/351
CPR	0xf4	Component Parameter Register	8.6.2.41/353
UCV	0xf8	UART Component Version	8.6.2.42/355
CTR	0xfc	Component Type Register	8.6.2.43/356

8.6.2 Register and Field Description

8.6.2.1 RBR

- Name: Receive Buffer Register
- Description: Receive Buffer Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.
- Offset: 0x0

Bits	Field Name	Access	Description
31:8	RSVD_RBR	R	RBR 31to9 Reserved bits read as 0. Value After Reset: 0x0
7:0	RBR	R	Receive Buffer Register This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be

Bits	Field Name	Access	Description
			overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an overrun error occurs. Value After Reset: 0x0

8.6.2.2 DLL

- Name: Divisor Latch (Low)
- Offset: 0x0

Bits	Field Name	Access	Description
31:8	RSVD_DLL_31to8	R	DLL 31to8 Reserved bits read as 0.
7:0	DLL	R/W	Divisor Latch (Low) This register makes up the lower 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock frequency)/(16*divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications will occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data. Value After Reset: 0x0

8.6.2.3 THR

- Name: Transmit Holding Register
- Description: Transmit Holding Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.
- Offset: 0x0

Bits	Field Name	Access	Description
32:9	RSVD_THR	R	THR 31to9 Reserved bits read as 0.

Bits	Field Name	Access	Description
8:0	THR	W	Transmit Holding Register. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default = 16) is determined by the value of FIFO Depth that is set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. Value After Reset: 0x0

8.6.2.4 DLH

- Name: Divisor Latch High
- Description: Divisor Latch High (DLH) Register. If UART_16550_COMPATIBLE = No, then this register can be accessed only when the DLAB bit (LCR[7]) is set and the UART is not busy, that is, USR[0] is 0; otherwise this register can be accessed only when the DLAB bit (LCR[7]) is set.
- Offset: 0x4

Bits	Field Name	Access	Description
31:8	RSVD_DLH	R	DLH 31to8 Reserved bits read as zero 0.
7:0	dlh	R/W	Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock frequency)/(16*divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications will occur. Also, once the DLH is

Bits	Field Name	Access	Description
			set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data. Value After Reset: 0x0

8.6.2.5 IER

- Name: Interrupt Enable Register
- Description: Interrupt Enable Register. This register can be accessed only when the DLAB bit (LCR[7]) is cleared.
- Offset: 0x4

Bits	Field Name	Access	Description
31:8	RSVD_IER_31to8	R	IER 31to8 Reserved bits read as zero 0.
7	PTIME	RW	Programmable THRE Interrupt Mode Enable. Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. Values: ■ 0x0 (DISABLED): Disable Programmable THRE Interrupt Mode. ■ 0x1 (ENABLED): Enable Programmable THRE Interrupt Mode. Value After Reset: 0x0
6:5	RSVD_IER_6to5	R	IER 6to5 Reserved bits read as 0. Value After Reset: 0x0
4	ELCOLR	RO	Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register. This is applicable only for Overrun Error, Parity Error, Framing Error, and Break Interrupt status bits. 0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register. 1 = LSR status bits are cleared only on reading the LSR register. Writeable only when LSR_STATUS_CLEAR == Enabled, always readable. Values: ■ 0x0 (DISABLED): Disable ALC. ■ 0x1 (ENABLED): Enable ALC. Value After Reset: 0x0

Bits	Field Name	Access	Description
3	EDSSI	R/W	Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. Values: ■ 0x0 (DISABLED): Disable Modem Status Interrupt. ■ 0x1 (ENABLED): Enable Modem Status Interrupt. Value After Reset: 0x0
2	ELSI	R/W	Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. Values: ■ 0x0 (DISABLED): Disable Receiver Line Status Interrupt. ■ 0x1 (ENABLED): Enable Receiver Line Status Interrupt. Value After Reset: 0x0
1	ETBEI	R/W	Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. Values: ■ 0x0 (DISABLED): Disable Transmit empty interrupt. ■ 0x1 (ENABLED): Enable Transmit empty interrupt. Value After Reset: 0x0
0	ERBFI	R/W	Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. Values: ■ 0x0 (DISABLED): Disable Receive data Interrupt. ■ 0x1 (ENABLED): Enable Receive data Interrupt. Value After Reset: 0x0

8.6.2.6 FCR

- Name: FIFO Control Register
- Offset: 0x8

Bits	Field Name	Access	Description
31:8	RSVD_FCR_31to8	R	FCR 31to8 Reserved bits read as 0.
7:6	RT	W	RCVR Trigger (or RT). This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will be generated. In auto flow control mode, it is used to determine when the rts_n signal will be de-asserted only when RTC_FCT is disabled. It also determines when the dma_rx_req_n signal will be asserted when in certain modes of operation. For details on DMA support, refer to 'DMA Support' section of data book. Values: ■ 0x0 (FIFO_CHAR_1): 1 character in FIFO ■ 0x1 (FIFO_QUARTER_FULL): FIFO 1/4 full ■ 0x2 (FIFO_HALF_FULL): FIFO 1/2 full ■ 0x3 (FIFO_FULL_2): FIFO 2 less than full Value After Reset: 0x0
5:4	TET	W	TX Empty Trigger (or TET). Writes will have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts will be generated when the mode is active. It also determines when the dma_tx_req_n signal will be asserted when in certain modes of operation. For details on DMA support, refer to 'DMA Support' section of data book. Values: ■ 0x0 (FIFO_EMPTY): FIFO Empty ■ 0x1 (FIFO_CHAR_2): 2 characters in FIFO ■ 0x2 (FIFO_QUARTER_FULL): FIFO 1/4 full ■ 0x3 (FIFO_HALF_FULL): FIFO 1/2 full Value After Reset: 0x0
3	DMAM	W	DMA Mode (or DMAM). This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). For details on DMA support, refer to 'DMA Support' section of data book. Values: ■ 0x0 (MODE0): Mode 0 ■ 0x1 (MODE1): Mode 1

Bits	Field Name	Access	Description
			Value After Reset: 0x0
2	XFIFOR	W	XMIT FIFO Reset (or XFIFOR). This resets the control portion of the transmit FIFO and treats the FIFO as empty. This will also de-assert the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Values: ■ 0x1 (RESET): Transmit FIFO reset Value After Reset: 0x0
3	DMAM	W	DMA Mode (or DMAM). This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). For details on DMA support, refer to 'DMA Support' section of data book. Values: ■ 0x0 (MODE0): Mode 0 ■ 0x1 (MODE1): Mode 1 Value After Reset: 0x0
2	XFIFOR	W	XMIT FIFO Reset (or XFIFOR). This resets the control portion of the transmit FIFO and treats the FIFO as empty. This will also de-assert the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Values: ■ 0x1 (RESET): Transmit FIFO reset Value After Reset: 0x0
1	RFIFOR	W	RCVR FIFO Reset (or RFIFOR). This resets the control portion of the receive FIFO and treats the FIFO as empty. This will also de-assert the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Values: ■ 0x1 (RESET): Receive FIFO reset

Bits	Field Name	Access	Description
			Value After Reset: 0x0
0	FIFOE	W	FIFO Enable (or FIFOE). This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. Values: ■ 0x0 (DISABLED): FIFO disabled. ■ 0x1 (ENABLED): FIFO enabled. Value After Reset: 0x0

8.6.2.7 IIR

- Name: Interrupt Identification Register
- Description: Interrupt Identification Register
- Offset: 0x8

Bits	Field Name	Access	Description
31:8	RSVD_IIR_31to8	R	IIR 31to8 Reserved bits read as 0.
7:6	FIFOSE	R	FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled. Values: ■ 0x0 (DISABLED): FIFOs are disabled. ■ 0x3 (ENABLED): FIFOs are enabled. Value After Reset: 0x0
5:4	RSVD_IIR_5to4	R	IIR 5to4 Reserved bits read as 0. Value After Reset: 0x0
3:0	IID	R	Interrupt ID (or IID). This indicates the highest priority pending interrupt which can be one of the following types specified in Values. Note: An interrupt of type 0111 (busy detect) will never get indicated if UART_16550_COMPATIBLE == YES in coreConsultant. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt. Values: ■ 0x0 (MODEM_STATUS): Modem status ■ 0x1 (NO_INTERRUPT_PENDING): No interrupt

Bits	Field Name	Access	Description
			pending ■ 0x2 (THR_EMPTY): THR empty ■ 0x4 (RECEIVED_DATA_AVAILABLE): Received data available ■ 0x6 (RECEIVER_LINE_STATUS): Receiver line status ■ 0x7 (BUSY_DETECT): Busy detect ■ 0xc (CHARACTER_TIMEOUT): Character timeout Value After Reset: 0x1

8.6.2.8 LCR

- Name: Line Control Register
- Description: Line Control Register
- Offset: 0xc

Bits	Field Name	Access	Description
31:8	RSVD_LCR_31to8	R	LCR 31to8 Reserved bits read as 0.
7	DLAB	R/W	Divisor Latch Access Bit If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. Values: ■ 0x0 (DISABLED): Divisor Latch register is writable only when UART Not BUSY. ■ 0x1 (ENABLED): Divisor Latch register is always readable and writable. Value After Reset: 0x0
6	BC	R/W	Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally

Bits	Field Name	Access	Description
			looped back to the receiver and the sir_out_n line is forced low. Values: ■ 0x0 (DISABLED): Serial output is released for data transmission. ■ 0x1 (ENABLED): Serial output is forced to spacing state. Value After Reset: 0x0
5	SP	R/W	Stick Parity If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled. Values: ■ 0x0 (DISABLED): Stick parity disabled. ■ 0x1 (ENABLED): Stick parity enabled. Value After Reset: 0x0
4	EPS	R/W	Even Parity Select If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked. Values: ■ 0x0 (ODD_PARITY): An odd parity is transmitted or checked. ■ 0x1 (EVEN_PARITY): An even parity is transmitted or checked. Value After Reset: 0x0
3	PEN	R/W	Parity Enable If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This bit is used to enable and disable parity generation and detection

Bits	Field Name	Access	Description
			in transmitted and received serial character respectively. Values: ■ 0x0 (DISABLED): Disable parity. ■ 0x1 (ENABLED): Enable parity. Value After Reset: 0x0
2	STOP	R/W	Number of stop bits If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit. Values: ■ 0x0 (STOP_1BIT): 1 stop bit ■ 0x1 (STOP_1_5BIT_OR_2BIT): 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit Value After Reset: 0x0
1:0	DLS	R/W	Data Length Select (or CLS as used in legacy) If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive. Values: ■ 0x0 (CHAR_5BITS): 5 data bits per character ■ 0x1 (CHAR_6BITS): 6 data bits per character ■ 0x2 (CHAR_7BITS): 7 data bits per character ■ 0x3 (CHAR_8BITS): 8 data bits per character Value After Reset: 0x0

8.6.2.9 MCR

- Name: Modem Control Register

- Description: Modem Control Register
- Offset: 0x10

Bits	Field Name	Access	Description
31:7	RSVD_MCR_31to7	R	MCR 31to7 Reserved bits read as 0.
6	SIRE	R/W	SIR Mode Enable Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in section 'IrDA 1.0 SIR Protocol' in the databook. Note: To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register. For details of the recommended programming sequence, refer to 'Programing Examples' section of data book. Values: ■ 0x0 (DISABLED): IrDA SIR Mode disabled. ■ 0x1 (ENABLED): IrDA SIR Mode enabled. Value After Reset: 0x0
5	AFCE	R/W	Auto Flow Control Enable Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in section 'Auto Flow Control' in data book. Values: ■ 0x0 (DISABLED): Auto Flow Control Mode disabled. ■ 0x1 (ENABLED): Auto Flow Control Mode enabled. Value After Reset: 0x0
4	LoopBack	R/W	LoopBack Bit This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n

Bits	Field Name	Access	Description
			line is held low, while serial data output is inverted and looped back to the sir_in line. Values: ■ 0x0 (DISABLED): Loopback mode disabled. ■ 0x1 (ENABLED): Loopback mode enabled. Value After Reset: 0x0
3	OUT2	R/W	OUT2 This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. Values: ■ 0x0 (OUT2_0): out2_n de-asserted (logic 1) ■ 0x1 (OUT2_1): out2_n asserted (logic 0) Value After Reset: 0x0
2	OUT1	R/W	OUT1 This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. Values: ■ 0x0 (OUT1_0): out1_n de-asserted (logic 1) ■ 0x1 (OUT1_1): out1_n asserted (logic 0) Value After Reset: 0x0
1	RTS	R/W	Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enabled (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive

Bits	Field Name	Access	Description
			high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Values: ■ 0x0 (INACTIVE): Request to Send rts_n de-asserted (logic 1) ■ 0x1 (ACTIVE): Request to Send rts_n asserted (logic 0) Value After Reset: 0x0
0	DTR	R/W	Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Values: ■ 0x0 (INACTIVE): dtr_n de-asserted (logic1) ■ 0x1 (ACTIVE): dtr_n asserted (logic 0) Value After Reset: 0x0

8.6.2.10 LSR

- Name: Line Status Register
- Description: Line Status Register
- Offset: 0x14

Bits	Field Name	Access	Description
31:9	RSVD_LSR_31to9	R	LSR 31to9 Reserved bits read as 0.
8	ADDR_RCVD	R	Address Received Bit If 9Bit data mode (LCR_EXT[0] = 1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. ■ 1: Indicates the character is address.

Bits	Field Name	Access	Description
			■ 0: Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: Users needs to ensure that interrupt gets cleared (reading the LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupts. Value After Reset: 0x0
7	RFE	R	Receiver FIFO Error bit This bit is only relevant when FIFO_MODE != NONE and FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO. Values: ■ 0x0 (NO_RX_FIFO_ERROR): No error in RX FIFO ■ 0x1 (RX_FIFO_ERROR): Error in RX FIFO Value After Reset: 0x0
6	TEMT	R	Transmitter Empty bit If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Values: ■ 0x0 (DISABLED): Transmitter not empty ■ 0x1 (ENABLED): Transmitter empty Value After Reset: 0x1
5	THRE	R	Transmit Holding Register Empty bit If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty.

Bits	Field Name	Access	Description
			This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. Programmable THRE interrupt mode operation is described in detail in section 'Programmable THRE Interrupt' in data book. Values: ■ 0x0 (DISABLED): THRE interrupt control is disabled. ■ 0x1 (ENABLED): THRE interrupt control is enabled. Value After Reset: 0x1
4	BI	R	Break Interrupt bit This is used to indicate the detection of a break sequence on the serial input data. If in UART mode, it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode, it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR == 1) or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR == 0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.

Bits	Field Name	Access	Description
			Values: ■ 0x0 (NO_BREAK): No break sequence detected ■ 0x1 (BREAK): Break sequence detected Value After Reset: 0x0
3	FE	R	Framing Error bit This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART will try to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR == 1) or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR == 0). Values: ■ 0x0 (NO_FRAMING_ERROR): No framing error ■ 0x1 (FRAMING_ERROR): Framing error Value After Reset: 0x0
2	PE	R	Parity Error bit This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this

Bits	Field Name	Access	Description
			situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3] = 1) and the parity is set to odd (LCR[4] = 0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR == 1) or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR == 0). Values: ■ 0x0 (NO_PARITY_ERROR): No parity error ■ 0x1 (PARITY_ERROR): Parity error Value After Reset: 0x0
1	OE	R	Overrun error bit This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR == 1) or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR == 0). Values: ■ 0x0 (NO_OVER_RUN_ERROR): No overrun error ■ 0x1 (OVER_RUN_ERROR): Overrun error Value After Reset: 0x0
0	DR	R	Data Ready bit This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode. Values: ■ 0x0 (NOT_READY): Data not ready ■ 0x1 (READY): Data ready Value After Reset: 0x0

8.6.2.11 MSR

- Name: Modem Status Register
- Description: Whenever bit 0, 1, 2 or 3 is set to logic one, to indicate a change on the modem control inputs, a modem status interrupt will be generated if enabled via the IER regardless of when the change occurred. The bits (bits 0, 1, 3) can be set after a reset-even though their respective modem signals are inactive-because the synchronized version of the modem signals have a reset value of 0 and change to value 1 after reset. To prevent unwanted interrupts due to this change, a read of the MSR register can be performed after reset.
- Offset: 0x18

Bits	Field Name	Access	Description
31:8	RSVD_MSR_31to8	R	MSR 31to8 Reserved bits read as 0.
7	DCD	R	Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted, it is an indication that the carrier has been detected by the modem or data set. In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Values: ■ 0x0 (DEASSERTED): dcd_n input is de-asserted (logic 1). ■ 0x1 (ASSERTED): dcd_n input is asserted (logic 0). Value After Reset: 0x0
6	RI	R	Ring Indicator This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted, it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Values: ■ 0x0 (DEASSERTED): ri_n input is de-asserted (logic 1). ■ 0x1 (ASSERTED): ri_n input is asserted (logic 0). Value After Reset: 0x0

Bits	Field Name	Access	Description
5	DSR	R	Data Set Ready This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Values: ■ 0x0 (DEASSERTED): dsr_n input is de-asserted (logic 1). ■ 0x1 (ASSERTED): dsr_n input is asserted (logic 0). Value After Reset: 0x0
4	CTS	R	Clear to Send This is used to indicate the current state of the modem control line cts_n. That is, this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with the UART. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS). Values: ■ 0x0 (DEASSERTED): cts_n input is de-asserted (logic 1). ■ 0x1 (ASSERTED): cts_n input is asserted (logic 0). Value After Reset: 0x0
3	DDCD	R	Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted. Values: ■ 0x0 (NO_CHANGE): No change on dcd_n since last read of MSR ■ 0x1 (CHANGE): Change on dcd_n since last read of

Bits	Field Name	Access	Description
			MSR Value After Reset: 0x0
2	TERI	R	Trailing Edge of Ring Indicator This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Values: ■ 0x0 (NO_CHANGE): No change on ri_n since last read of MSR ■ 0x1 (CHANGE): Change on ri_n since last read of MSR Value After Reset: 0x0
1	DDSR	R	Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted. Values: ■ 0x0 (NO_CHANGE): No change on dsr_n since last read of MSR ■ 0x1 (CHANGE): Change on dsr_n since last read of MSR Value After Reset: 0x0
0	DCTS	R	Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset

Bits	Field Name	Access	Description
			is removed if the cts_n signal remains asserted. Values: ■ 0x0 (NO_CHANGE): No change on cts_n since last read of MSR ■ 0x1 (CHANGE): Change on cts_n since last read of MSR Value After Reset: 0x0

8.6.2.12 SCR

- Name: Scratchpad Register
- Description: Scratchpad Register
- Offset: 0x1c

Bits	Field Name	Access	Description
31:8	RSVD_SCR_31to8	R	SCR 31to8 Reserved bits read as 0.
7:0	SCR	R/W	This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART. Value After Reset: 0x0

8.6.2.13 LPDLL

- Name: Low Power Divisor Latch Low
- Description: Low Power Divisor Latch Low Register
- Offset: 0x20

Bits	Field Name	Access	Description
31:8	RSVD_LPDLL_31to8	R	LPDLL 31to8 Reserved bits read as 0.
7:0	LPDLL	R/W	This register makes up the lower 8-bits of a 16-bit, read/write, Low Power Divisor Latch register that contains the baud rate divisor for the UART which must give a baud rate of 115.2K. This is required for SIR Low Power (minimum pulse width) detection at the receiver. The output low power baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: Low power baud rate = (serial clock frequency)/(16*divisor) Therefore a divisor must be selected to give a baud rate

Bits	Field Name	Access	Description
			of 115.2K. Note: When the Low Power Divisor Latch Registers (LPDLL and LPDLH) are set to zero, the low power baud clock is disabled and no low power pulse detection (or any pulse detection for that matter) will occur at the receiver. Also, once the LPDLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data. Value After Reset: 0x0

8.6.2.14 LPDLH

- Name: Low Power Divisor Latch High
- Description: Low Power Divisor Latch High Register
- Offset: 0x24

Bits	Field Name	Access	Description
31:8	RSVD_LPDLH_31to8	R	LPDLH 31to8 Reserved bits read as 0.
7:0	LPDLH	R/W	This register makes up the upper 8-bits of a 16-bit, read/write, Low Power Divisor Latch register that contains the baud rate divisor for the UART which must give a baud rate of 115.2K. This is required for SIR Low Power (minimum pulse width) detection at the receiver. The output low power baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: Low power baud rate = (serial clock frequency)/ (16*divisor) Therefore a divisor must be selected to give a baud rate of 115.2K. Note: When the Low Power Divisor Latch Registers (LPDLL and LPDLH) are set to zero, the low power baud clock is disabled and no low power pulse detection (or any pulse detection for that matter) will occur at the receiver. Also, once the LPDLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data. Value After Reset: 0x0

8.6.2.15 SRBRn

- Name: Shadow Receive Buffer Register
- Offset: 0x30 + n*0x4

Bits	Field Name	Access	Description
31:9	RSVD_SRBRn	R	SRBR0 31 to 9 Reserved bits read as 0.
8:0	SRBRn	R	Shadow Receive Buffer Register n. This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Value After Reset: 0x0

8.6.2.16 STHRn

- Name: Shadow Transmit Holding Register
- Offset: 0x30 + n*0x4

Bits	Field Name	Access	Description
31:9	RSVD_STHRn	R	STHRn 31 to 9 Reserved bits read as 0.
8:0	STHRn	W	Shadow Transmit Holding Register n. This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.

Bits	Field Name	Access	Description
			If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default = 16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. Value After Reset: 0x0

8.6.2.17 FAR

- Name: FIFO Access Register
- Description: FIFO Access Register
- Offset: 0x70

Bits	Field Name	Access	Description
31:1	RSVD_FAR_31to1	R	FAR 31to1 Reserved bits read as 0.
0	FAR	R/W	Writes will have no effect when FIFO_ACCESS == No, always readable. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled, it allows the RBR to be written by the master and the THR to be read by the master. Note that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Values: ■ 0x0 (DISABLED): FIFO access mode disabled. ■ 0x1 (ENABLED): FIFO access mode enabled. Value After Reset: 0x0

8.6.2.18 TFR

- Name: Transmit FIFO Read

- Offset: 0x74

Bits	Field Name	Access	Description
31:8	RSVD_TFR_31to8	R	TFR 31to8 Reserved bits read as 0.
7:0	TFR	R	Transmit FIFO Read These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Value After Reset: 0x0

8.6.2.19 RFW

- Name: Receive FIFO Write
- Offset: 0x78

Bits	Field Name	Access	Description
31:10	RSVD_RFW_31to10	R	RFW 31to10 Reserved bits read as 0.
9	RFFE	W	Receive FIFO Framing Error These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. Values: ■ 0x0 (DISABLED): Frame error disabled. ■ 0x1 (ENABLED): Frame error enabled. Value After Reset: 0x0
8	RFPE	W	Receive FIFO Parity Error These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to

Bits	Field Name	Access	Description
			the RBR. Values: ■ 0x0 (DISABLED): Parity error disabled. ■ 0x1 (ENABLED): Parity error enabled. Value After Reset: 0x0
7:0	RFWD	W	Receive FIFO Write Data These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Value After Reset: 0x0

8.6.2.20 USR

- Name: UART Status register
- Description: UART Status register
- Offset: 0x7c

Bits	Field Name	Access	Description
31:5	RSVD_USR_31to5	R	USR 31to5 Reserved bits read as 0.
4	RFF	R	Receive FIFO Full This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full. Values: ■ 0x0 (NOT_FULL): Receive FIFO not full ■ 0x1 (FULL): Receive FIFO full Value After Reset: 0x0
3	RFNE	R	Receive FIFO Not Empty This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty. Values:

Bits	Field Name	Access	Description
			■ 0x0 (EMPTY): Receive FIFO is empty. ■ 0x1 (NOT_EMPTY): Receive FIFO is not empty. Value After Reset: 0x0
2	TFE	R	Transmit FIFO Empty This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty. Values: ■ 0x0 (NOT_EMPTY): Transmit FIFO is not empty. ■ 0x1 (EMPTY): Transmit FIFO is empty. Value After Reset: 0x1
1	TFNF	R	Transmit FIFO Not Full This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full. Values: ■ 0x0 (FULL): Transmit FIFO is full. ■ 0x1 (NOT_FULL): Transmit FIFO is not full. Value After Reset: 0x1
0	BUSY	R	UART Busy This bit is only valid when UART_16550_COMPATIBLE == NO. This indicates that a serial transfer is in progress, when cleared indicates that the UART is idle or inactive. This bit will be set to 1 (busy) under any of the following conditions: Transmission in progress on serial interface Transmit data present in THR, when FIFO access mode is not being used (FAR = 0) and the baud divisor is non-zero ({DLH, DLL} does not equal 0) when the divisor latch access bit is 0 (LCR.DLAB = 0) Reception in progress on the interface Receive data present in RBR, when FIFO access mode is not being used (FAR = 0). Note: It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if UART has no data in the THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the UART.

Bits	Field Name	Access	Description
			This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit will also be delayed by several cycles of the slower clock. Values: ■ 0x0 (IDLE): UARTt is idle or inactive. ■ 0x1 (BUSY): UART is busy (actively transferring data). Value After Reset: 0x0

8.6.2.21 TFL

- Name: Transmit FIFO Level
- Offset: 0x80

Bits	Field Name	Access	Description
31:5	RSVD_TFL_31toADDR_WIDTH	R	TFL 31 to 5 Reserved bits read as 0.
4:0	tfl	R	Transmit FIFO Level This indicates the number of data entries in the transmit FIFO. Value After Reset: 0x0

8.6.2.22 RFL

- Name: RFL
- Offset: 0x84

Bits	Field Name	Access	Description
31:5	RSVD_RFL_31toADDR_WIDTH	R	RFL 31 to 5 Reserved bits read as 0.
4:0	rfl	R	Receive FIFO Level. This indicates the number of data entries in the receive FIFO. Value After Reset: 0x0

8.6.2.23 SRR

- Name: Software Reset Register
- Offset: 0x88

Bits	Field Name	Access	Description
31:3	RSVD_SRR_31to3	R	SRR 31to3 Reserved bits read as 0.
2	XFR	W	XMIT FIFO Reset Writes will have no effect when FIFO_MODE == NONE. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This will also de-assert the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA = YES). Note that this bit is 'self-clearing', it is not necessary to clear this bit. Value After Reset: 0x0
1	RFR	W	RCVR FIFO Reset Writes will have no effect when FIFO_MODE == NONE. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. This will also de-assert the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing', it is not necessary to clear this bit. Value After Reset: 0x0
0	UR	W	UART Reset This asynchronously resets the UART and synchronously removes the reset assertion. For a two clock implementation, both pclk and sclk domains will be reset. Values: ■ 0x0 (NO_RESET): No UART reset ■ 0x1 (RESET): UART reset Value After Reset: 0x0

8.6.2.24 SRTS

- Name: Shadow Request to Send
- Offset: 0x8c

Bits	Field Name	Access	Description
31:1	RSVD_SRTS_31to1	R	SRTS 31to1 Reserved bits read as 0.
0	SRTS	R/W	Shadow Request to Send This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read modify write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enabled (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold) only when RTC Flow Trigger is disabled; otherwise it is gated by the receiver FIFO almost-full trigger, where 'almost full' refers to two available slots in the FIFO (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Values: ■ 0x0 (DEASSERTED): Shadow Request to Send uart_rts_n logic1 ■ 0x1 (ASSERTED): Shadow Request to Send uart_rts_n logic0 Value After Reset: 0x0

8.6.2.25 SBCR

- Name: Shadow Break Control Register
- Offset: 0x90

Bits	Field Name	Access	Description
31:1	RSVD_SBCR_31to1	R	SBCR 31to1 Reserved bits read as 0.
0	SBCB	R/W	Shadow Break Control Bit This is a shadow register for the Break bit (LCR[6]), this

Bits	Field Name	Access	Description
			can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one, the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver. Values: ■ 0x0 (NO_BREAK): No spacing on serial output ■ 0x1 (BREAK): Serial output forced to the spacing Value After Reset: 0x0

8.6.2.26 SDMAM

- Name: Shadow DMA Mode Register
- Offset: 0x94

Bits	Field Name	Access	Description
31:1	RSVD_SDMAM_31to1	R	SDMAM 31to1 Reserved bits read as 0.
0	SDMAM	R/W	Shadow DMA Mode This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). See section 5.9 on page 54 for details on DMA support. Values: ■ 0x0 (MODE_0): Mode 0 ■ 0x1 (MODE_1): Mode 1 Value After Reset: 0x0

8.6.2.27 SFE

- Name: Shadow FIFO Enable Register

- Offset: 0x98

Bits	Field Name	Access	Description
31:1	RSVD_SFE_31to1	R	SFE 31to1 Reserved bits read as 0.
0	SFE	R/W	Shadow FIFO Enable This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs will be reset. Values: ■ 0x0 (DISABLED): FIFOs are disabled. ■ 0x1 (ENABLED): FIFOs are enabled. Value After Reset: 0x0

8.6.2.28 SRT

- Name: Shadow RCVR Trigger Register
- Size: 32 bits
- Offset: 0x9c

Bits	Field Name	Access	Description
31:2	RSVD_SRT_31to2	R	SRT 31to2 Reserved bits read as 0.
1:0	SRT	R/W	Shadow RCVR Trigger This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will be generated. It also determines when the dma_rx_req_n signal will be asserted when DMA Mode (FCR[3]) is set to one. Values: ■ 0x0 (FIFO_CHAR_1): 1 character in FIFO ■ 0x1 (FIFO_QUARTER_FULL): FIFO 1/4 full

Bits	Field Name	Access	Description
			■ 0x2 (FIFO_HALF_FULL): FIFO 1/2 full ■ 0x3 (FIFO_FULL_2): FIFO 2 less than full Value After Reset: 0x0

8.6.2.29 STET

- Name: Shadow TX Empty Trigger Register
- Offset: 0xa0

Bits	Field Name	Access	Description
31:2	RSVD_STET_31to2	R	STET 31to2 Reserved bits read as 0.
1:0	STET	R/W	Shadow TX Empty Trigger This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. Writes will have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts will be generated when the mode is active. Values: ■ 0x0 (FIFO_EMPTY): FIFO empty ■ 0x1 (FIFO_CHAR_2): 2 characters in FIFO ■ 0x2 (FIFO_QUARTER_FULL): FIFO 1/4 full ■ 0x3 (FIFO_HALF_FULL): FIFO 1/2 full Value After Reset: 0x0

8.6.2.30 HTX

- Name: Halt TX
- Description: Halt TX
- Offset: 0xa4

Bits	Field Name	Access	Description
31:1	RSVD_HTX_31to1	R	HTX 31to1 Reserved bits read as 0.
0	HTX	R/W	Halt TX Writes will have no effect when FIFO_MODE == NONE, always readable. This register is used to halt transmissions for testing, so that the transmit FIFO can

Bits	Field Name	Access	Description
			be filled by the master when FIFOs are implemented and enabled. Note, if FIFOs are implemented and not enabled, the setting of the halt TX register will have no effect on operation. Values: ■ 0x0 (DISABLED): Halt Transmission disabled. ■ 0x1 (ENABLED): Halt Transmission enabled. Value After Reset: 0x0

8.6.2.31 DMASA

- Name: DMA Software Acknowledge Register
- Description: DMA Software Acknowledge Register
- Offset: 0xa8

Bits	Field Name	Access	Description
31:1	RSVD_DMASA_31to1	R	DMASA 31to1 Reserved bits read as 0.
0	DMASA	W	DMA Software Acknowledge Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This will cause the TX request, TX single, RX request and RX single signals to deassert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit. Values: ■ 0x1 (SOFT_ACK): DMA software acknowledge Value After Reset: 0x0

8.6.2.32 TCR

- Name: Transceiver Control Register
- Description: This register is used to enable or disable RS485 mode and also control the polarity values for Driver enable (de) and Receiver Enable (re) signals.
- Offset: 0xac

Bits	Field Name	Access	Description
31:5	RSVD_TCR_31to5	R	TCR 31to5 Reserved bits read as 0.

Bits	Field Name	Access	Description
4:3	XFER_MODE	R/W	Transfer Mode ■ 0: In this mode, transmit and receive can happen simultaneously. The user can enable DE_EN, RE_EN at any point of time. Turn around timing as programmed in the TAT register is not applicable in this mode. ■ 1: In this mode, DE and RE are mutually exclusive. Either DE or RE only one of them is expected to be enabled through programming. Hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. For transmission, hardware will wait if it is in middle of receiving any transfer, before it starts transmitting. ■ 2: In this mode, DE and RE are mutually exclusive. Once DE_EN/RE_EN is programed - by default 're' will be enabled and UART controller will be ready to receive. If the user programs the TX FIFO with the data, then UART after ensuring no receive is in progress, disable 're' and enable the 'de' signal. Once the TX FIFO becomes empty, the ‘re’ signal gets enabled and the 'de' signal will be disabled. In this mode of operation, hardware will consider the Turn Around timings which are programmed in the TAT register while switching from RE to DE or DE to RE. In this mode, 'de' and 're' signals are strictly complementary to each other. Value After Reset: 0x0
2	DE_POL	R/W	Driver Enable Polarity ■ 1: DE signal is active high. ■ 0: DE signal is active low. Value After Reset: UART_DE_POL
1	RE_POL	R/W	Receiver Enable Polarity ■ 1: RE signal is active high. ■ 0: RE signal is active low. Value After Reset: UART_RE_POL
0	RS485_EN	R/W	RS485 Transfer Enable ■ 0: In this mode, the transfers are still in the RS232 mode. All other fields in this register are reserved and registers DE_EN/RE_EN/TAT are also reserved.

Bits	Field Name	Access	Description
			■ 1: In this mode, the transfers will happen in RS485 mode. All other fields of this register are applicable. Value After Reset: 0x0

8.6.2.33 DE_EN

- Name: Driver Output Enable Register
- Description: The Driver Output Enable Register (DE_EN) is used to control the assertion and deassertion of the DE signal.
- Offset: 0xb0

Bits	Field Name	Access	Description
31:1	RSVD_DE_EN_31to1	R	DE_EN 31to1 Reserved bits read as 0.
0	DE_Enable	R/W	DE Enable control The 'DE Enable' register bit is used to control assertion and de-assertion of the 'de' signal. ■ 0: De-assert the 'de' signal. ■ 1: Assert the 'de' signal. Value After Reset: 0x0

8.6.2.34 RE_EN

- Name: Receiver Output Enable Register
- Description: The Receiver Output Enable Register (RE_EN) is used to control the assertion and deassertion of the RE signal.
- Offset: 0xb4

Bits	Field Name	Access	Description
31:1	RSVD_RE_EN_31to1	R	RE_EN 31to1 Reserved bits read as 0.
0	RE_Enable	R/W	RE Enable control The 'RE Enable' register bit is used to control assertion and de-assertion of the 're' signal. ■ 0: De-assert the 're' signal. ■ 1: Assert the 're' signal. Value After Reset: 0x0

8.6.2.35 DET

- Name: Driver Output Enable Timing Register

- Description: The Driver Output Enable Timing Register (DET) is used to control the DE assertion and de-assertion timings of the 'de' signal.
- Offset: 0xb8

Bits	Field Name	Access	Description
31:24	RSVD_DE_DEAT_31to24	R	DET 31to24 Reserved bits read as 0.
23:16	DE_De-assertion_Time	R/W	Driver Enable de-assertion time This field controls the amount of time (in terms of number of serial clock periods) between the end of stop bit on the sout to the falling edge of Driver output enable signal. Value After Reset: 0x0
15:8	RSVD_DE_AT_15to8	R	DET 15to8 Reserved bits read as 0. Value After Reset: 0x0
7:0	DE_Assertion_Time	R/W	Driver Enable assertion time This field controls the amount of time (in terms of number of serial clock periods) between the assertion of rising edge of Driver output enable signal to serial transmit enable. Any data in transmit buffer, will start on serial output (sout) after the transmit enable. Value After Reset: 0x0

8.6.2.36 TAT

- Name: TurnAround Timing Register
- Description: The TurnAround Timing Register (TAT) is used to hold the turnaround time between switching of the 're' and 'de' signals.
- Offset: 0xbc

Bits	Field Name	Access	Description
31:16	RE_to_DE	R/W	Receiver Enable to Driver Enable TurnAround time Turnaround time (in terms of serial clock) for RE deassertion to DE assertion. Note: ■ If the DE assertion time in the DET register is 0, then the actual value is the programmed value + 3. ■ If the DE assertion time in the DET register is 1, then the actual value is the programmed value + 2. ■ If the DE assertion time in the DET register is greater than 1, then the actual value is the programmed value + 1.

Bits	Field Name	Access	Description
			Value After Reset: 0x0
15:0	DE_to_RE	R/W	Driver Enable to Receiver Enable TurnAround time Turnaround time (in terms of serial clock) for DE deassertion to RE assertion. Note: The actual time is the programmed value + 1. Value After Reset: 0x0

8.6.2.37 DLF

- Name: Divisor Latch Fraction Register
- Offset: 0xc0

Bits	Field Name	Access	Description
31:4	RSVD_DLF	R	DLF 31 to4 Reserved bits read as 0.
3:0	DLF	R/W	Fractional part of divisor The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE). Value After Reset: 0x0

8.6.2.38 RAR

- Name: Receive Address Register
- Description: Receive Address Register
- Offset: 0xc4

Bits	Field Name	Access	Description
31:8	RSVD_RAR_31to8	R	RAR 31to8 Reserved bits read as 0.
7:0	RAR	R/W	This is an address matching register during receive mode. If the 9th bit is set in the incoming character, then the remaining 8-bits will be checked against this register value. If the match happens, then subsequent characters with 9th bit set to 0 will be treated as data byte until the next address byte is received. Note: This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. If UART_16550_COMPATIBLE is configured to 0, then

Bits	Field Name	Access	Description
			RAR should be programmed only when UART is not busy. If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress. Value After Reset: 0x0

8.6.2.39 TAR

- Name: Transmit Address Register
- Description: Transmit Address Register
- Offset: 0xc8

Bits	Field Name	Access	Description
31:8	RSVD_TAR_31to8	R	TAR 31to8 Reserved bits read as 0.
7:0	TAR	R/W	This is an address matching register during transmit mode. If DLS_E (LCR_EXT[0]) bit is enabled, then UART will send the 9-bit character with 9th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1. Note: ■ This register is used only to send the address. The normal data should be sent by programming the THR register. ■ Once the address is started to send on the UART serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware. Value After Reset: 0x0

8.6.2.40 LCR_EXT

- Name: Line Extended Control Register
- Description: Line Extended Control Register
- Size: 32 bits
- Offset: 0xcc

Bits	Field Name	Access	Description
31:4	RSVD_LCR_EXT	R	LCR_EXT 31to4 Reserved bits read as 0.
3	TRANSMIT_MODE	R/W	Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers.

Bits	Field Name	Access	Description
			■ 1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide. The user needs to ensure that the THR/STHR register is written correctly for address/data. Address: 9th bit is set to 1, Data: 9th bit is set to 0. Note: Transmit address register (TAR) is not applicable in this mode of operation. ■ 0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide. The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register. SEND_ADDR bit is used as a control knob to indicate the UART on when to send the address. Value After Reset: 0x0
2	SEND_ADDR	R/W	Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode. ■ 1: 9-bit character will be transmitted with 9th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'. ■ 0: 9-bit character will be transmitted with 9th bit set to 0 and the remaining 8-bits will be taken from the TX FIFO which is programmed through 8-bit wide THR/STHR register. Note: 1. This bit is auto-cleared by the hardware, after sending out the address character. User is not expected to program this bit to 0. 2. This field is applicable only when DLS_E bit is set to 1 and TRANSMIT_MODE is set to 0. Value After Reset: 0x0
1	ADDR_MATCH	R/W	Address Match Mode. This bit is used to enable the address match feature during receive. ■ 1: Address match mode. UART will wait until the incoming character with 9th bit set to 1, and further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then subsequent characters will be treated as valid data and UART starts receiving

Bits	Field Name	Access	Description
			data. ■ 0: Normal mode. UART will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO. User is responsible to read the data and differentiate b/n address and data. Note: This field is applicable only when DLS_E is set to 1. Value After Reset: 0x0
0	DLS_E	R/W	Extension for DLS. This bit is used to enable 9-bit data for transmit and receive transfers. Value After Reset: 0x0

8.6.2.41 CPR

- Name: Component Parameter Register
- Description: Component Parameter Register
- Offset: 0xf4

Bits	Field Name	Access	Description
31:24	RSVD_CPR_31to24	R	CPR 31to24 Reserved bits read as 0.
23:16	FIFO_MODE	R	Encoding of FIFO_MODE configuration parameter value Values: ■ 0x0 (FIFO_MODE_0): FIFO mode is 0. ■ 0x1 (FIFO_MODE_16): FIFO mode is 16. ■ 0x2 (FIFO_MODE_32): FIFO mode is 32. ■ 0x4 (FIFO_MODE_64): FIFO mode is 64. ■ 0x8 (FIFO_MODE_128): FIFO mode is 128. ■ 0x10 (FIFO_MODE_256): FIFO mode is 256. ■ 0x20 (FIFO_MODE_512): FIFO mode is 512. ■ 0x40 (FIFO_MODE_1024): FIFO mode is 1024. ■ 0x80 (FIFO_MODE_2048): FIFO mode is 2048. Value After Reset: UART_ENCODED_FIFO_MODE
15:14	RSVD_CPR_15to14	R	CPR 15to14 Reserved bits read as 0. Value After Reset: 0x0
13	DMA_EXTRA	R	Encoding of DMA_EXTRA configuration parameter value Values:

Bits	Field Name	Access	Description
			■ 0x0 (DISABLED): DMA_EXTRA disabled. ■ 0x1 (ENABLED): DMA_EXTRA enabled. Value After Reset: DMA_EXTRA
12	UART_ADD_ENCODED_PARAMS	R	Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value Values: ■ 0x0 (DISABLED): UART_ADD_ENCODED_PARAMS disabled. ■ 0x1 (ENABLED): UART_ADD_ENCODED_PARAMS enabled. Value After Reset: UART_ADD_ENCODED_PARAMS
11	SHADOW	R	Encoding of SHADOW configuration parameter value Values: ■ 0x0 (DISABLED): SHADOW disabled. ■ 0x1 (ENABLED): SHADOW enabled. Value After Reset: SHADOW
10	FIFO_STAT	R	Encoding of FIFO_STAT configuration parameter value Values: ■ 0x0 (DISABLED): FIFO_STAT disabled. ■ 0x1 (ENABLED): FIFO_STAT enabled. Value After Reset: FIFO_STAT
9	FIFO_ACCESS	R	Encoding of FIFO_ACCESS configuration parameter value Values: ■ 0x0 (DISABLED): FIFO_ACCESS disabled. ■ 0x1 (ENABLED): FIFO ACCESS enabled. Value After Reset: FIFO_ACCESS
8	ADDITIONAL_FEAT	R	Encoding of ADDITIONAL_FEATURES configuration parameter value Values: ■ 0x0 (DISABLED): Additional features disabled. ■ 0x1 (ENABLED): Additional features enabled. Value After Reset: ADDITIONAL_FEATURES
7	SIR_LP_MODE	R	Encoding of SIR_LP_MODE configuration parameter value Values:

Bits	Field Name	Access	Description
			■ 0x0 (DISABLED): SIR_LP mode disabled. ■ 0x1 (ENABLED): SIR_LP mode enabled. Value After Reset: SIR_LP_MODE
6	SIR_MODE	R	Encoding of SIR_MODE configuration parameter value Values: ■ 0x0 (DISABLED): SIR mode disabled. ■ 0x1 (ENABLED): SIR mode enabled. Value After Reset: SIR_MODE
5	THRE_MODE	R	Encoding of THRE_MODE configuration parameter value Values: ■ 0x0 (DISABLED): THRE mode disabled. ■ 0x1 (ENABLED): THRE mode enabled. Value After Reset: THRE_MODE_RST
4	AFCE_MODE	R	Encoding of AFCE_MODE configuration parameter value Values: ■ 0x0 (DISABLED): AFCE mode disabled. ■ 0x1 (ENABLED): AFCE mode enabled. Value After Reset: AFCE_MODE
3:2	RSVD_CPR_3to2	R	CPR 3to2 Reserved bits read as 0. Value After Reset: 0x0
1:0	APB_DATA_WIDTH	R	Encoding of APB_DATA_WIDTH configuration parameter value Values: ■ 0x0 (APB_8BITS): APB data width is 8 bits. ■ 0x1 (APB_16BITS): APB data width is 16 bits. ■ 0x2 (APB_32BITS): APB data width is 32 bits. Value After Reset: UART_ENCODED_APB_WIDTH

8.6.2.42 UCV

- Name: UART Component Version
- Offset: 0xf8

Bits	Field Name	Access	Description
31:0	UART_Component_Version	R	ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*. Value After Reset: UART_COMP_VERSION

8.6.2.43 CTR

- Name: Component Type Register
- Offset: 0xfc

Bits	Field Name	Access	Description
31:0	Peripheral_ID	R	This register contains the peripherals identification code.

9 GPIO

9.1 Overview

There are six groups of GPIOs in the TH1520 chip, of which two groups are in the AON power domain, named AOGPIO and GPIO4; four groups in the AP power domain, named GPIO0, GPIO1, GPIO2 and GPIO3. Each group has 32 multi-function I/O port pins. Each port can be easily configured by software to meet various system configuration and design requirements. The function of each pin to be used must be defined before starting the main program. If the multiplexing function on the pin is not used, the pin can be configured as an I/O port. Before pin configuration, the initial pin state should be configured carefully to avoid some problems.

9.2 Main Features

The GPIO supports the following features:

- There are six groups of identical GPIOs in the TH1520 chip
  - Two groups are in the AON power domain, named AOGPIO and GPIO4
  - Four groups are in the AP power domain, named GPIO0, GPIO1, GPIO2 and GPIO3
- Each group has 32 independently configurable signals
- Separate data registers and data direction registers for each signal
- Independently controllable signal bits
- Configurable interrupt mode and generate single interrupt
- GPIO Component Type register
- GPIO Component Version register
- Configurable reset values on output signals

9.3 Interface

Figure & Table 9-1 Pin description table

Pin Name	Direction	Width	Description
GPIO0_[0~31]	IO	1	GPIO0 PAD pin name
GPIO1_[0~31]	IO	1	GPIO1 PAD pin name
GPIO2_[0~31]	IO	1	GPIO2 PAD pin name
GPIO3_[0~31]	IO	1	GPIO3 PAD pin name

9.4 Function Description

The GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.
GPIO I/O port can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable. The interrupts can be masked by programming the gpio_intmask register. The interrupt status can be read before masking (called raw status) and after masking. The interrupts are also combined into a single interrupt output signal, which has the same polarity as the individual interrupts. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.

9.5 Usage

- Configure the GPIO output:

1. Configure GPIO.gpio_swporta_ctl.gpio_swporta_ctl[0] = 1'b1, configure GPIO[0] to use software mode.
2. Configure GPIO.gpio_swporta_ddr.gpio_swporta_ddr[0] = 1'b1, configure GPIO[0] to input directly.
3. Configure GPIO.gpio_swporta_dr.gpio_swporta_dr[0] = 1'b1, write data 1'b1 to GPIO.
4. Monitor PAD GPIO[0] == 1.

- Configure the GPIO input:

1. Configure GPIO.gpio_swporta_ctl.gpio_swporta_ctl[0] = 1'b1, configure GPIO[0] to use software mode.
2. Configure GPIO.gpio_swporta_ddr.gpio_swporta_ddr[0] = 1'b0, configure GPIO[0] to input directly.
3. Tie PAD GPIO[0] to 1.
4. Read GPIO port A External port register, port A external port register[0] == 1, check whether GPIO[0] = 1.

9.6 Register Description

9.6.1 Register Memory Map

Name	Offset	Description	Chapter/Page
GPIO_SWPORTA_DR	0x0	Port A data register Reset value: 0x0	9.6.2.1/359
GPIO_SWPORTA_DDR	0x4	Port A data direction register Reset value: 0x0	9.6.2.2/360
GPIO_INTEN	0x30	Interrupt enable register	9.6.2.3/360

Name	Offset	Description	Chapter/Page
		Reset value: 0x0	
GPIO_INTMASK	0x34	Interrupt mask register Reset value: 0x0	9.6.2.4/360
GPIO_INTTYPE_LEVEL	0x38	Interrupt level Reset value: 0x0	9.6.2.5/360
GPIO_INT_POLARITY	0x3C	Interrupt polarity Reset value: 0x0	9.6.2.6/361
GPIO_INTSTATUS	0x40	Interrupt status Reset value: 0x0	9.6.2.7/361
GPIO_RAW_INTSTATUS	0x44	Raw interrupt status Reset value: 0x0	9.6.2.8/361
GPIO_PORTA_EOI	0x4C	Port A clear interrupt register Reset value: 0x0	9.6.2.9/361
GPIO_EXT_PORTA	0x50	External port A register Reset value: 0x0	9.6.2.10/361
GPIO_LS_SYNC	0x60	Synchronization level Reset value: 0x0	9.6.2.11/362
GPIO_ID_CODE	0x64	GPIO ID code Reset value: 0x0	9.6.2.12/362
GPIO_VER_ID_CODE	0x6C	GPIO component version Reset value: 0x0	9.6.2.13/362
GPIO_CONFIG_REG2	0x70	GPIO configuration register 2 Reset value: 0x0	9.6.2.14/362
GPIO_CONFIG_REG1	0x74	GPIO configuration register 1 Reset value: 0x0	9.6.2.15/363

9.6.2 Register and Field Description

9.6.2.1 GPIO_SWPORTA_DR

- Name: GPIO_SWPORTA_DR
- Address Offset: 0x00
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_SWPORTA_DR	R/W	Port A data register

9.6.2.2 GPIO_SWPORTA_DDR

- Name: GPIO_SWPORTA_DDR
- Address Offset: 0x04
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_SWPORTA_DDR	R/W	Port A data direction register

9.6.2.3 GPIO_INTEN

- Name: GPIO_INTEN
- Address Offset: 0x30
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_INTEN	R/W	Interrupt enable register

9.6.2.4 GPIO_INTMASK

- Name: GPIO_INTMASK
- Address Offset: 0x34
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_INTMASK	R/W	Interrupt mask register

9.6.2.5 GPIO_INTTYPE_LEVEL

- Name: GPIO_INTTYPE_LEVEL
- Address Offset: 0x38
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_INTTYPE_LEVEL	R/W	Interrupt level. Controls the type of interrupt that can occur on Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to be level-sensitive; otherwise, it is edge-sensitive.

9.6.2.6 GPIO_INT_POLARITY

- Name: GPIO_INT_POLARITY
- Address Offset: 0x3C
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_INT_POLARITY	R/W	Interrupt level Interrupt polarity. Controls the polarity of edge or level sensitivity that can occur on input of Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to falling-edge or active-low sensitive; otherwise, it is rising-edge or active-high sensitive.

9.6.2.7 GPIO_INTSTATUS

- Name: GPIO_INTSTATUS
- Address Offset: 0x40
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_INTSTATUS	RO	Interrupt status

9.6.2.8 GPIO_RAW_INTSTATUS

- Name: GPIO_RAW_INTSTATUS
- Address Offset: 0x44
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_RAW_INTSTATUS	RO	Raw interrupt status

9.6.2.9 GPIO_PORTA_EOI

- Name: GPIO_PORTA_EOI
- Address Offset: 0x4C
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_PORTA_EOI	WO	Port A clear interrupt register

9.6.2.10 GPIO_EXT_PORTA

- Name: GPIO_EXT_PORTA

- Address Offset: 0x50
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_EXT_PORTA	RO	External port A register

9.6.2.11 GPIO_LS_SYNC

- Name: GPIO_LS_SYNC
- Address Offset: 0x60
- Default Value: 0x0

Bits	Field Name	Access	Description
31:1	RSVD_GPIO_LS_SYNC		
0	GPIO_LS_SYNC	R/W	Writing a 1 to this register results in all level-sensitive interrupts being synchronized to pclk_intr.

9.6.2.12 GPIO_ID_CODE

- Name: GPIO_ID_CODE
- Address Offset: 0x64
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_ID_CODE	RO	GPIO ID code

9.6.2.13 GPIO_VER_ID_CODE

- Name: GPIO_VER_ID_CODE
- Address Offset: 0x6C
- Default Value: 0x0

Bits	Field Name	Access	Description
31:0	GPIO_VER_ID_CODE	RO	GPIO component version

9.6.2.14 GPIO_CONFIG_REG2

- Name: GPIO_CONFIG_REG2
- Address Offset: 0x70
- Default Value: 0x0

Bits	Field Name	Access	Description
31:20	RSVD_GPIO_CONFIG_REG2	RO	Reserved

Bits	Field Name	Access	Description
19:15	ENCODED_ID_PWIDTH_D	RO	Reserved
14:10	ENCODED_ID_PWIDTH_C	RO	Reserved
9:5	ENCODED_ID_PWIDTH_B	RO	Reserved
4:0	ENCODED_ID_PWIDTH_A	RO	The value of this register is equal to GPIO_PWIDTH_A-1.

9.6.2.15 GPIO_CONFIG_REG1

- Name: GPIO_CONFIG_REG1
- Address Offset: 0x74
- Default Value: 0x0

Bits	Field Name	Access	Description
31:22	RSVD_GPIO_CONFIG_REG1	RO	RSVD_GPIO_CONFIG_REG1 Reserved bits - read as zero.
21	INTERRUPT_BOTH_EDGE_TYPE	RO	The value of this register is derived from the GPIO_INT_BOTH_EDGE configuration parameter.
20:16	ENCODED_ID_WIDTH	RO	The value of this register is derived from the GPIO_ID_WIDTH configuration parameter.
15	GPIO_ID	RO	The value of this register is derived from the GPIO_ID configuration parameter.
14	ADD_ENCODED_PARAMS	RO	The value of this register is derived from the GPIO _ADD_ENCODED_PARAMS configuration parameter.
13	DEBOUNCE	RO	The value of this register is derived from the GPIO_DEBOUNCE configuration parameter.
12	PORTA_INTR	RO	The value of this register is derived from the GPIO_PORTA_INTR configuration parameter.
11	HW_PORTD	RO	Reserved
10	HW_PORTC	RO	Reserved
9	HW_PORTB	RO	Reserved
8	HW_PORTA	RO	The value of this register is derived from the GPIO_HW_PORTA configuration parameter.
7	PORTD_SINGLE_CTL	RO	Reserved
6	PORTC_SINGLE_CTL	RO	Reserved
5	PORTB_SINGLE_CTL	RO	Reserved
4	PORTA_SINGLE_CTL	RO	The value of this register is derived from the

Bits	Field Name	Access	Description
			GPIO_PORTA_SINGLE_CTL configuration parameter.
3:2	NUM_PORTS	RO	The value of this register is derived from the GPIO_NUM_PORT configuration parameter.
1:0	APB_DATA_WIDTH	RO	The value of this register is derived from the GPIO_APB_DATA_WIDTH configuration parameter.