Q3. (15 marks)
Here is a series of 4 bit address references given as word addresses in both decimal and binary.

Dec Addr	0	1	2	3	0	1	6	8	0	10	2	3	1	0
Binary	0000	0001	0010	0011	0000	0001	0110	1000	0000	1010	0010	0011	0001	0000

Below are four different 8-word caches. For each cache type, assuming the cache is initially empty, show the final contents of the cache. In the table at the bottom, show how many cache hits and misses there are for each type of cache. Write your solution in the tables below, assuming the above word address are 4-bit binary numbers. You should write the binary form of the tag in the tables indicating how many bits are in the tag field and index field. Also, the data column would be M[3], for data at memory address 3, M[8] for data at memory address 8.
You must use a LRU (least recently used) replacement scheme for bumping out entries in the cache when necessary. When inserting an element into the cache, if there are multiple empty slots for that index, you should put the new element in the left-most empty slot.

Direct-Mapped Cache

Index	Tag	Data
000	0	M[0]
001	0	M[1]
010	0	M[2]
011	0	M[3]
100		
101		
110	0	M[6]
111		

Two-Way Set Associative

Index	Tag	Data	Tag	Data
00	00	M[0]	10	M[8]
01	00	M[1]		
10	00	M[2]	01	M[6]
11	00	M[3]		

Four -Way Set Associative

Index	Tag	Data	Tag	Data	Tag	Data	Tag	Data
0	000	M[0]	101	M[2]	011	M[6]	100	M[8]
1	000	M[1]	001	M[3]				

Fully Associative

Tag	Data	Tag	Data	Tag	Data	Tag	Data	Tag	Data	Tag	Data	Tag	Data	Tag	Data
0000	M[0]	0001	M[1]	0010	M[2]	0011	M[3]	0110	M[6]	1000	M[8]	1010	M[10]		

Set	Hits	Misses
One-way (Direct-mapped)	5	9
Two-way	6	8
Four-way	6	8
Fully Associative	7	7