1. (6 marks) For 4 inputs A, B, C, D, fill in the truth table for the function F that is 1 when the binary number ABCD is a digit in your student ID. For example, if your student number was 20340259, the rows 0000, 0010, 0011, 0100, 0101, and 1001 should be 1, while the other entries should be 0.
Your solution depends on your student number.

Your Student number 20600787 (2 marks)

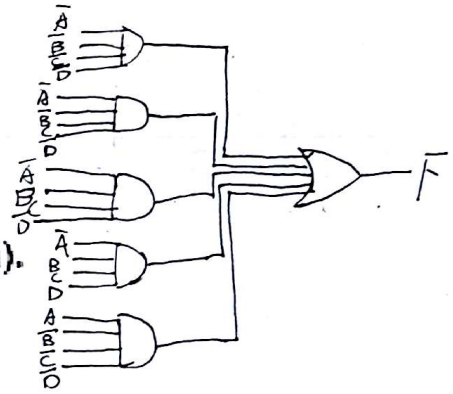
A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

A	B	C	D	F
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

a) (2 marks) Sum of Products Notation:

$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D}$

b) (2 marks) Circuit implementing F from part(a).



2. (4 marks)
(a)(2 marks) Re-write the following table (On the left) using *Don't Cares* where possible for output F only.

A	B	C	F	G
0	0	0	1	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0

A	B	C	F
X	0	X	1
X	1	X	X
1	X	X	1

(b)(2 mark) Give a simplified output equation for outputs F and G, using the inputs A, B, C as necessary. You may simplify by inspection. Your output equations should be in reduced form.

$F = \bar{A}B\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + ABC = \bar{A}\bar{B}(\bar{C}+C) + A\bar{B}(\bar{C}+C) + AB(\bar{C}+C)$

$= \bar{A}\bar{B} + A\bar{B} + AB$

$= (\bar{A}+A)\bar{B} + AB = \bar{B} + AB$

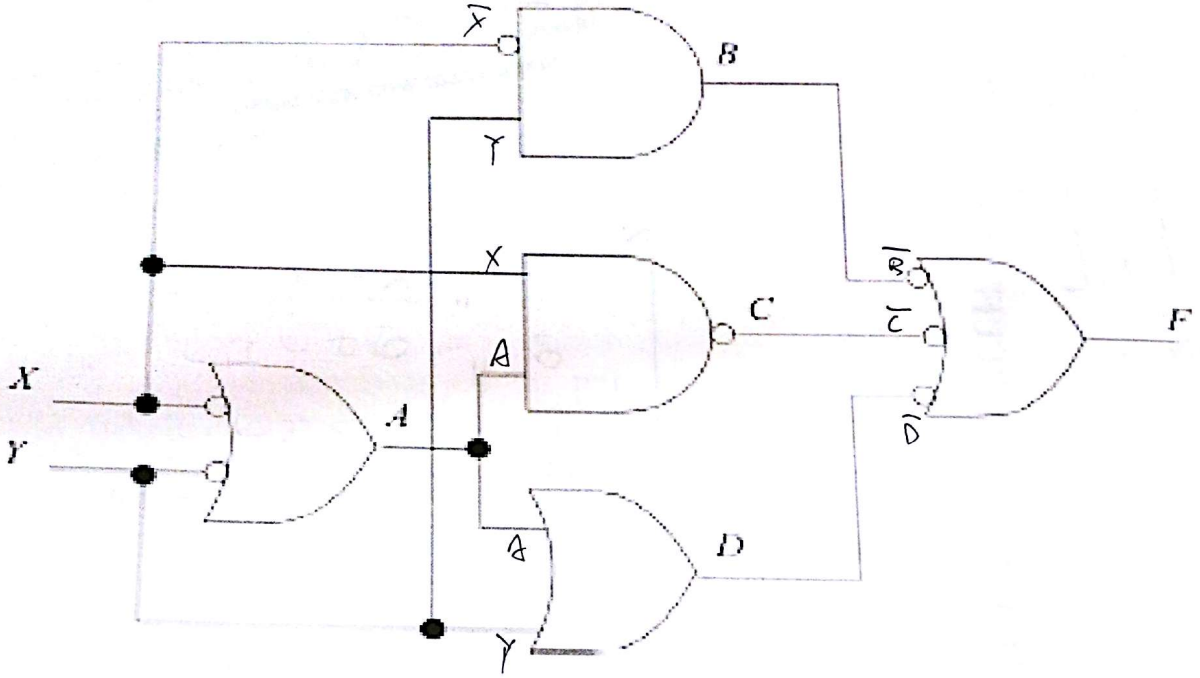
$G = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$

$= (\bar{A}\bar{B} + \bar{A}B + A\bar{B} + AB)\bar{C}$

$= (\bar{A}+A)\bar{C}$

$= \bar{C}$

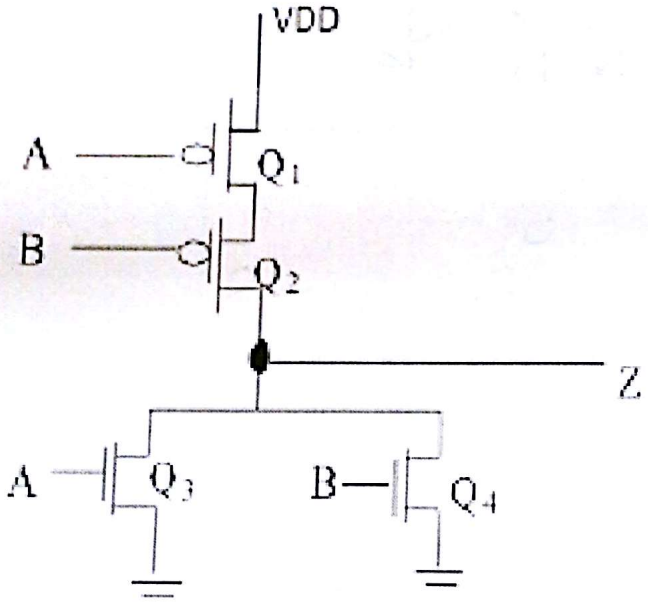
3. (5 marks) Complete the truth table for F in the following circuit, giving the truth table values for the internal signals A, B, and C and D as intermediate steps.



X	Y	A	B	C	D	F
0	0	1	0	1	1	1
0	1	1	1	1	1	0
1	0	1	0	0	1	1
1	1	0	0	1	1	1

4.(6 marks) You are given a circuit implemented with transistors in the diagram below. Analyze this circuit for all internal resistances Q_1 to Q_4, and state the final output of the circuit Z. The output Z may be 0, 1, or float '-'. The transistors Q1, Q2, Q3, Q4 should be High or Low (or 'H' or 'L').

TRANSISTOR CIRCUIT

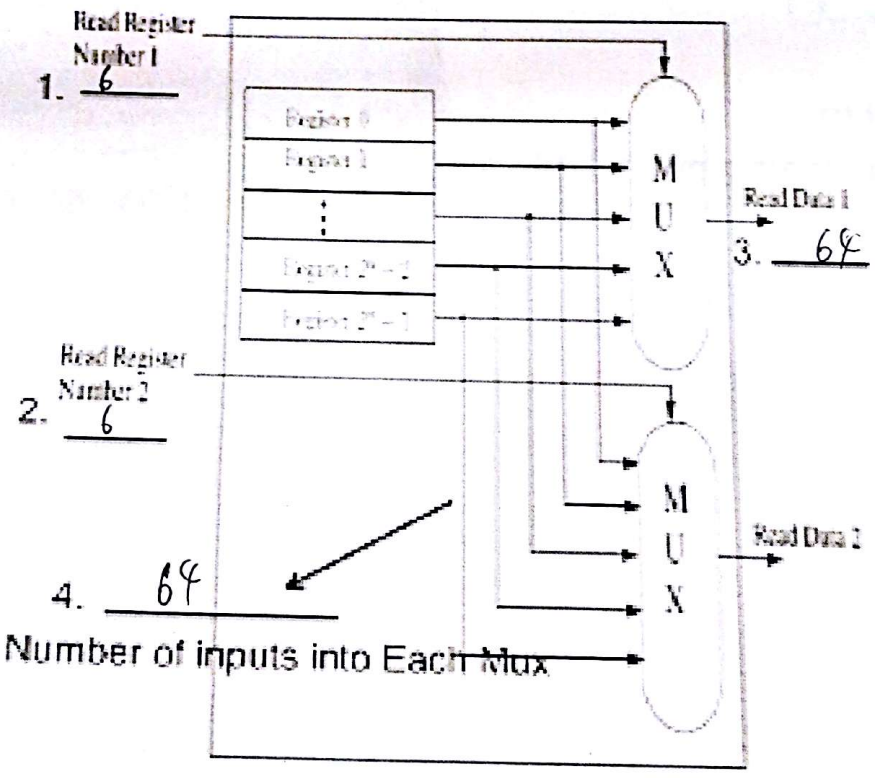


A	B	Q_1	Q_2	Q_3	Q_4	Z
0	0	L	L	H	H	1
0	1	L	H	H	L	0
1	0	H	L	L	H	0
1	1	H	H	L	L	0

5. (6 marks) Suppose we have a Register File that contains 64 registers. Each registers stores 32 bits of data. We would like to add a new MIPS instruction : adds $3, $4, $5, $6 : adds $rd, $rs, $rt, $rv

This instruction reads the contents of 3 registers ($rs, $rt, $rv) and places the result in one single destination register $rd. For this instruction we need to allow a read operation from the Register File for 3 registers in parallel.

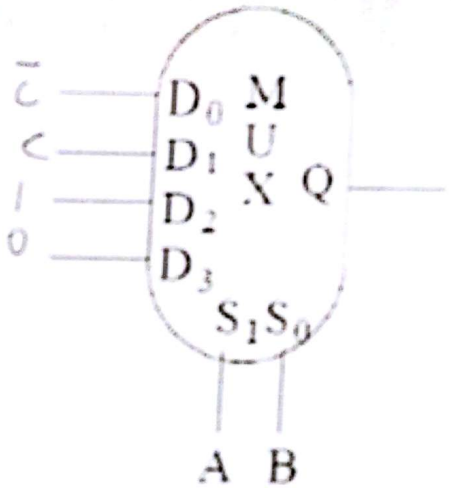
Label the inputs and *draw in any additional components* necessary to the Register File below inorder to implement this new configuration for the adds instruction. The labels from 1-3 should state the number of bits on the input/output and label number 4 should state how many inputs into each multiplexor in order to implement this new configuration.



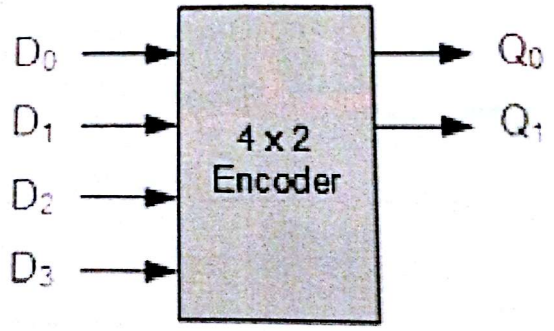
6. (4 marks) In the Diagram below is a 4-1 multiplexor with its select lines tied to A and B. Suppose we want to implement the following function using this multiplexor:

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Label the inputs D_0, D_1, D_2, and D_3 so that the output Q is as given by the truth table equal to F. The labels you use may be, C, $\bar{C}$, 0 or 1. The inputs A, and B are already tied to the select lines, S_0 and S_1.



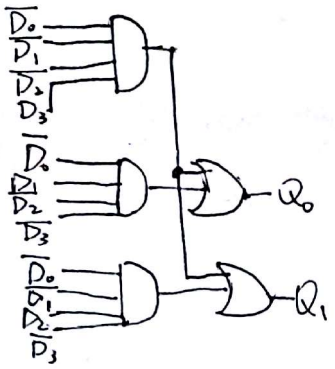
7.(5 marks) A binary Encoder works the *opposite* of a decoder. It performs the inverse of the decoder, having 2^n inputs and n outputs. In a *simple* binary encoder, only one input line may be asserted at any time. The output lines are the binary representation of the input. Therefore if D_0 is 1, the outputs on both Q_0 and Q_1 will be 0.



Fill in the rest of the truth table *and* draw the internal circuit for a 4x2 Encoder. In the case where all of the inputs to the encoder are 0, we do not care about the outputs (ie. this in an irrelevant option)

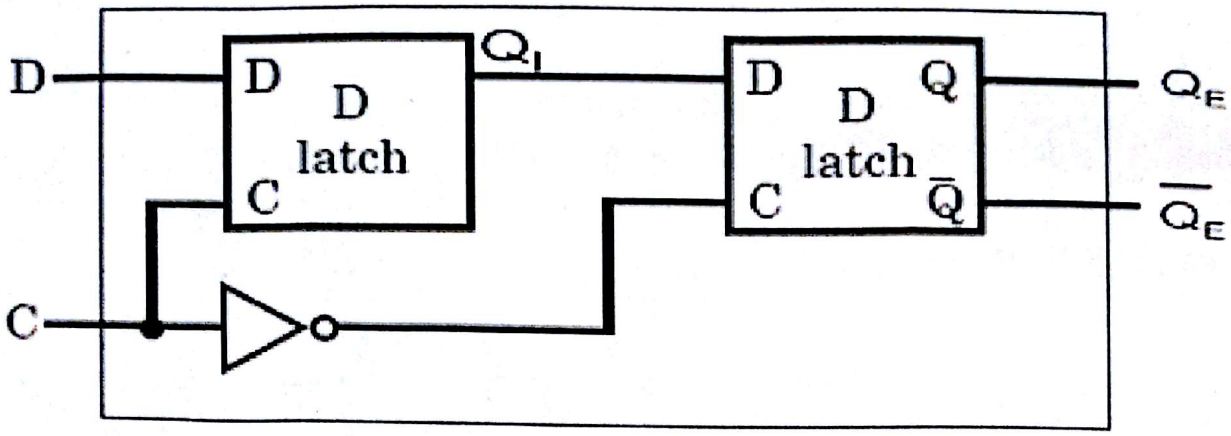
(a) (2 marks)

D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	0	–	–
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



b) (3 marks) Circuit for Encoder for both outputs:

8. (4 marks) Examine the D flip flop below:



In the figure below are traces of the D and C inputs to this latch. Draw in the traces of the signals Q_I and Q_E.