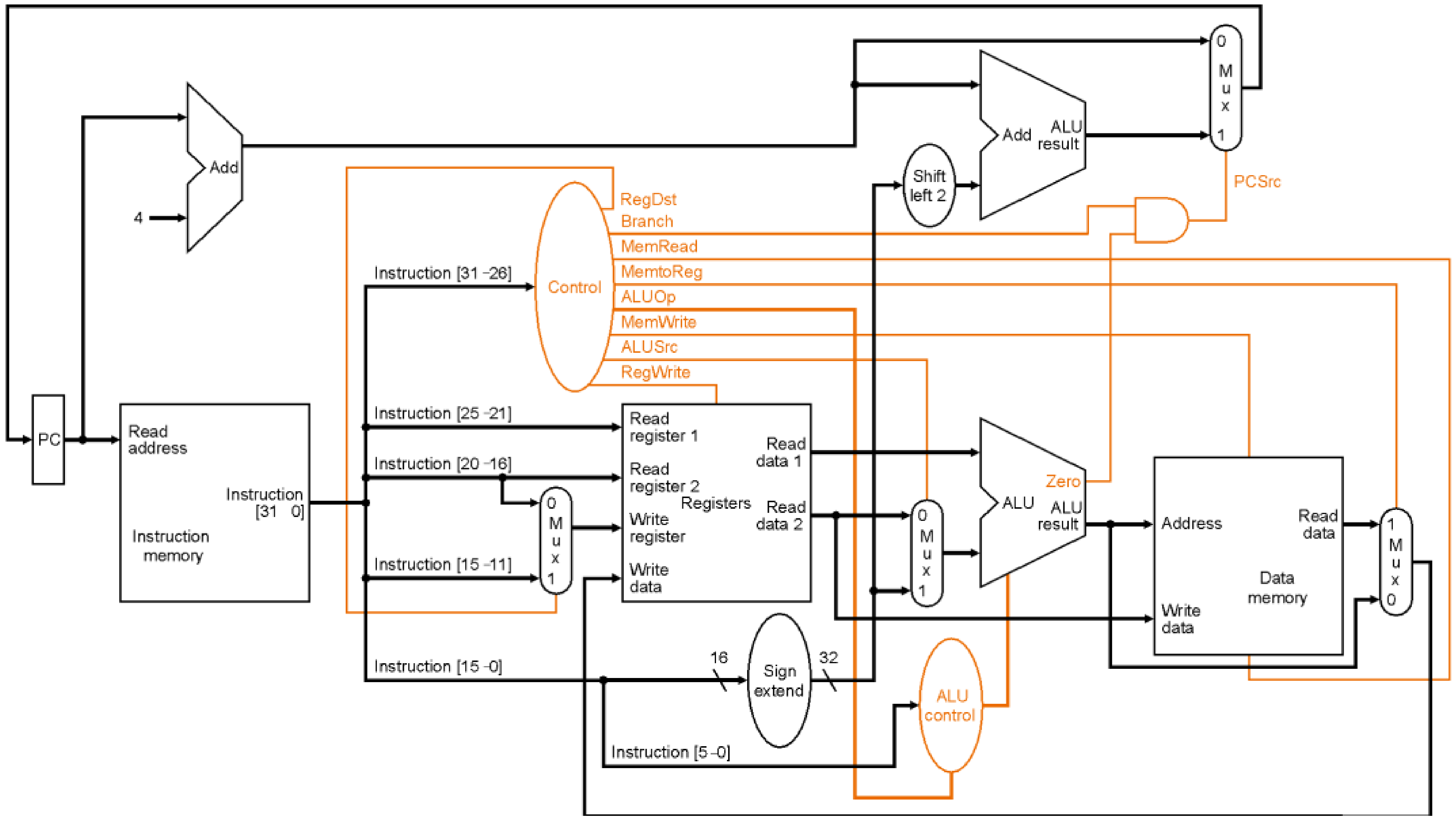
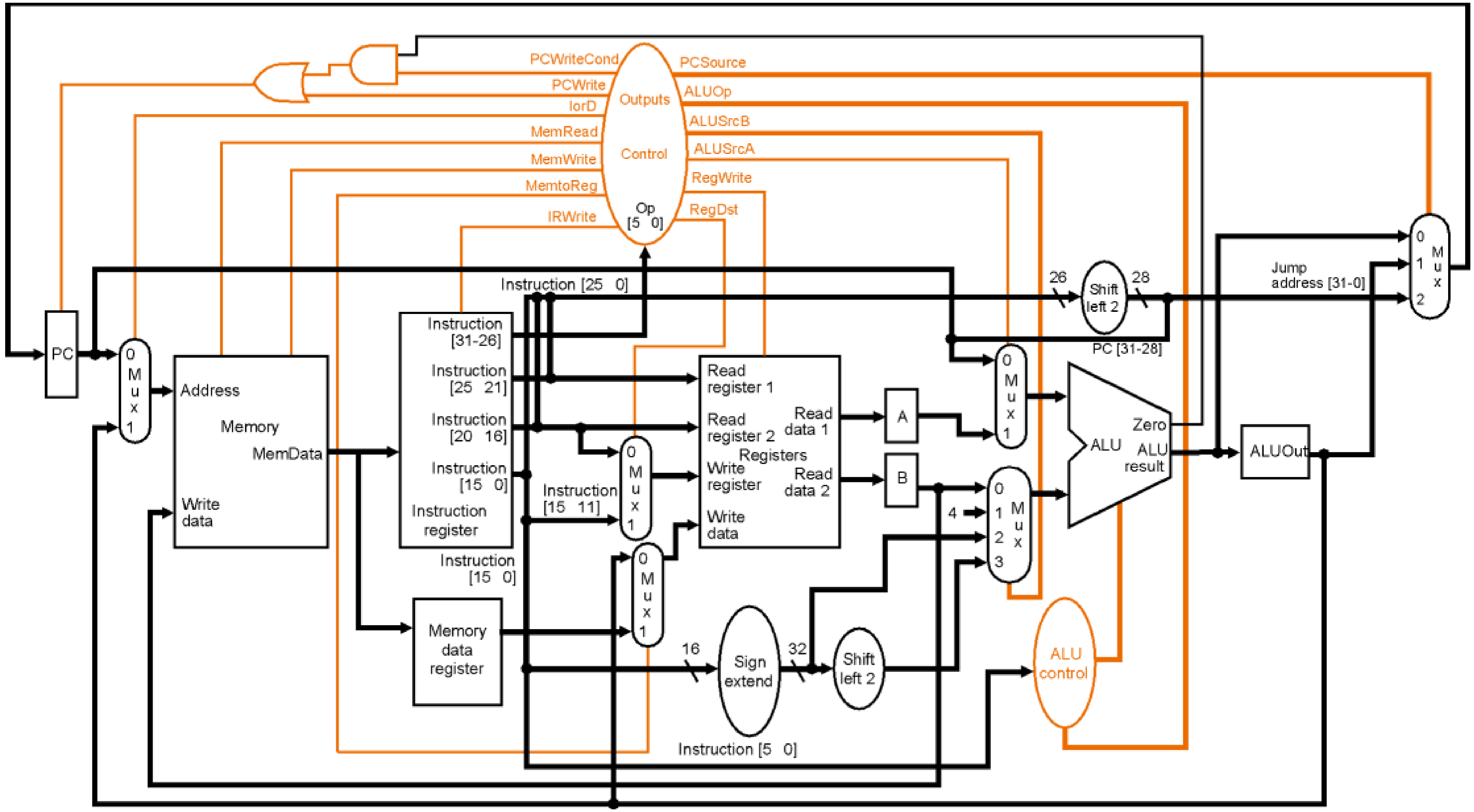
Pipelined CPU

Jason Mars

Evolution of Our CPU: Single Cycle



Evolution of Our CPU: Multi Cycle



Instruction Latencies and Throughput

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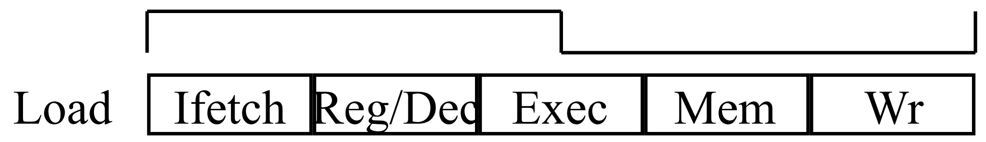
•Single-Cycle CPU



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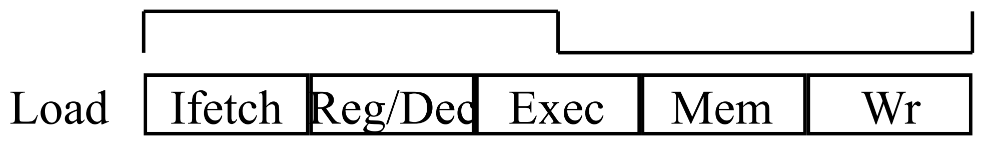
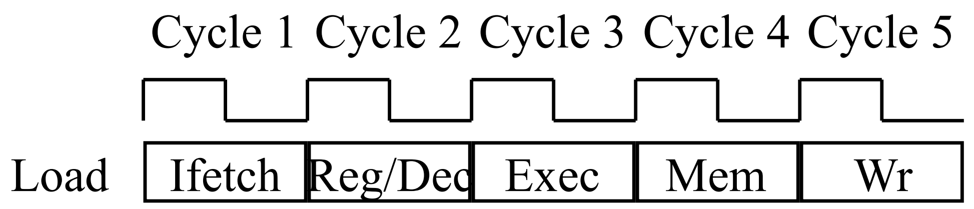


•Multiple Cycle CPU



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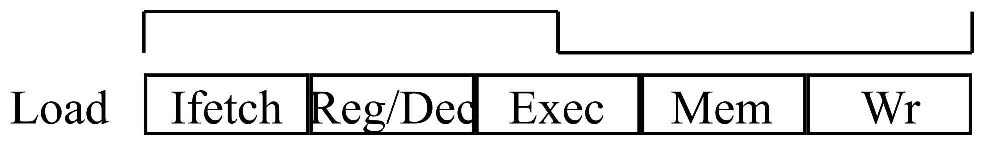

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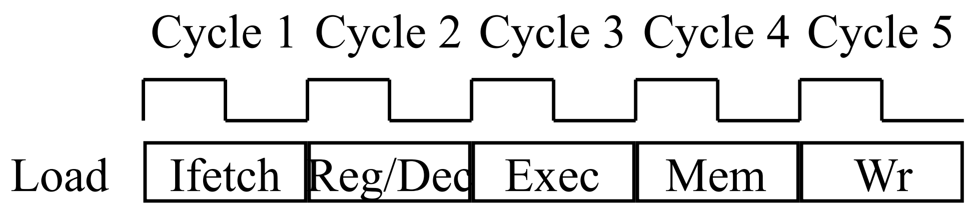
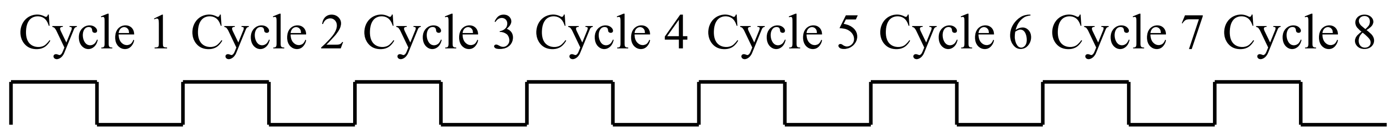


•Pipelined CPU



Instruction Latencies and Throughput

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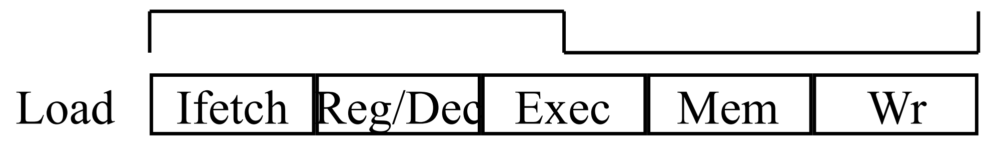
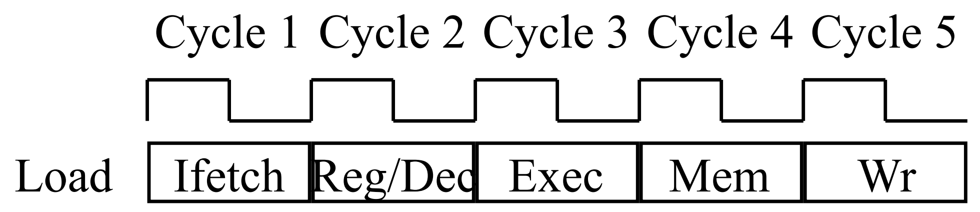
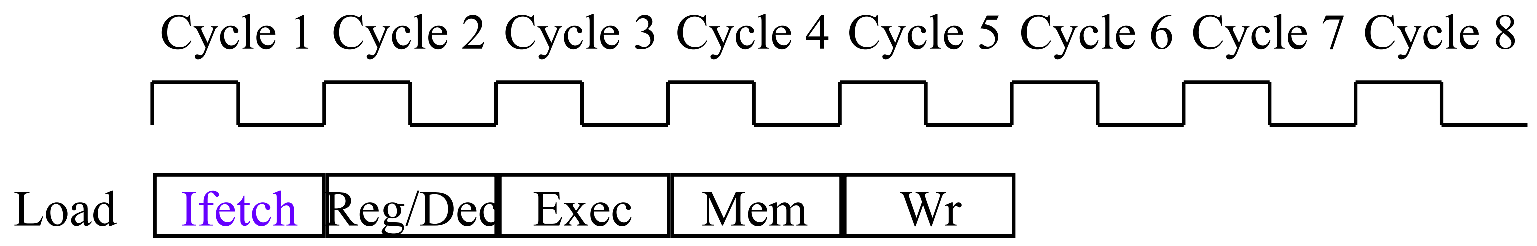


- **Multiple Cycle CPU**



- **Pipelined CPU**



Instruction Latencies and Throughput

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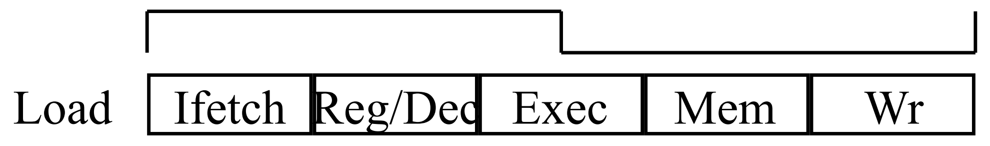

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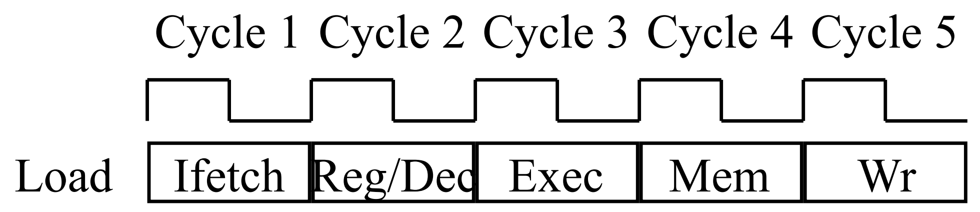

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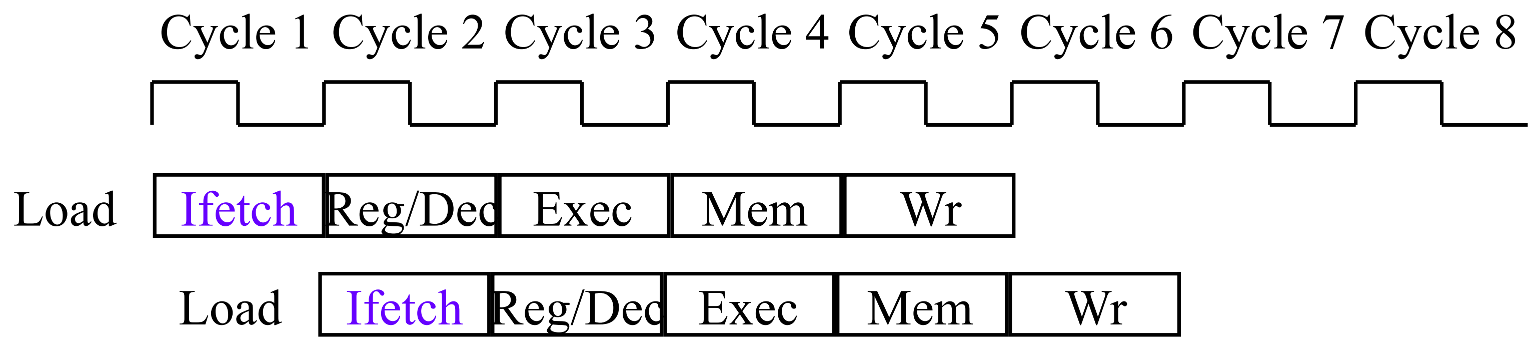

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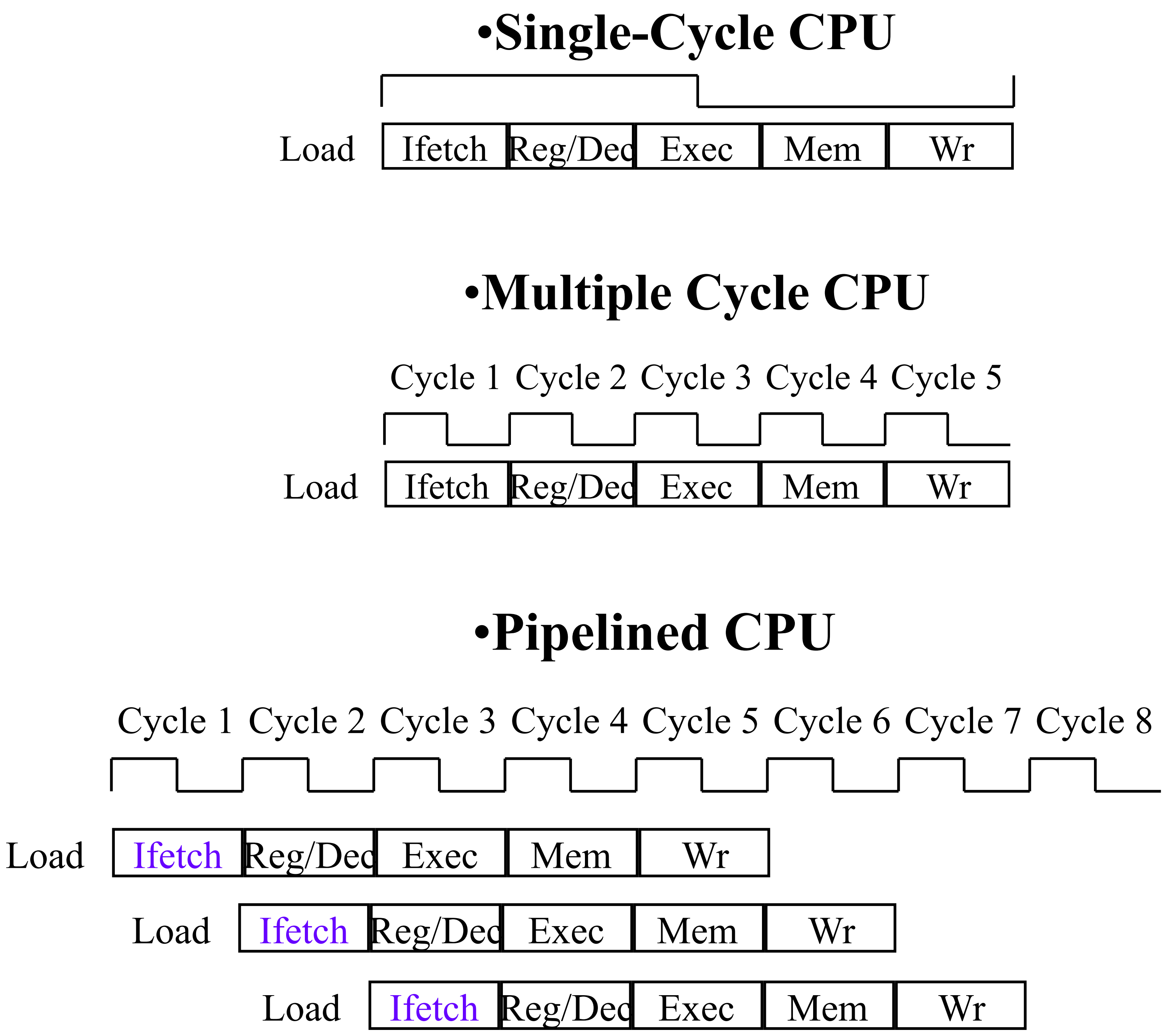

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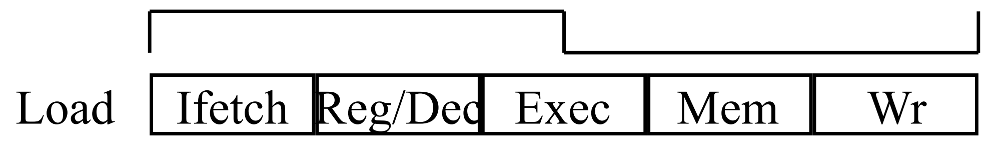

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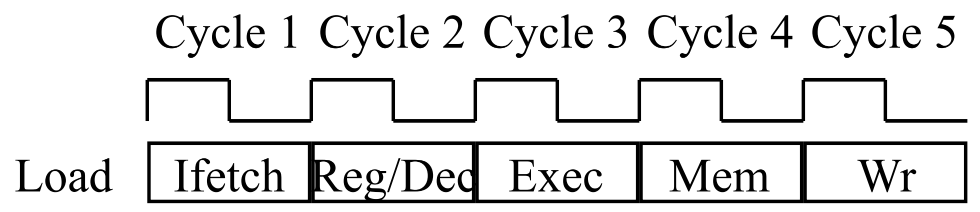

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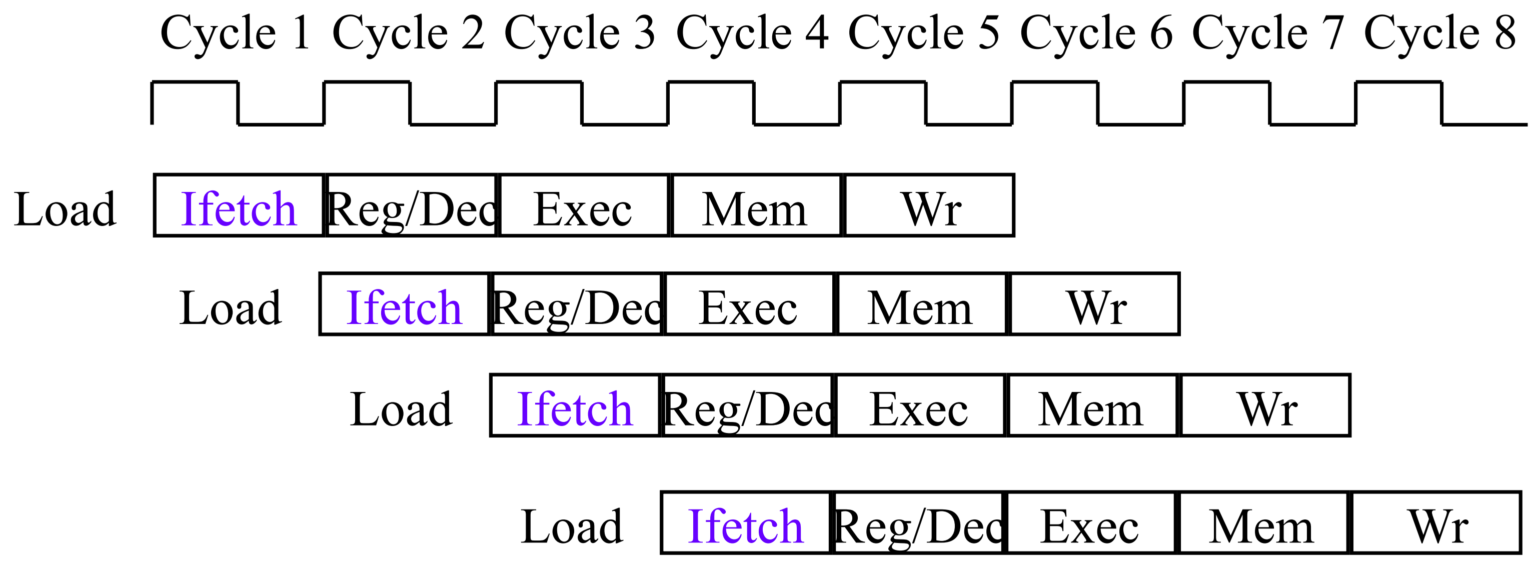

Pipelining Advantages

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- Higher maximum throughput

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- Higher utilization of CPU resources

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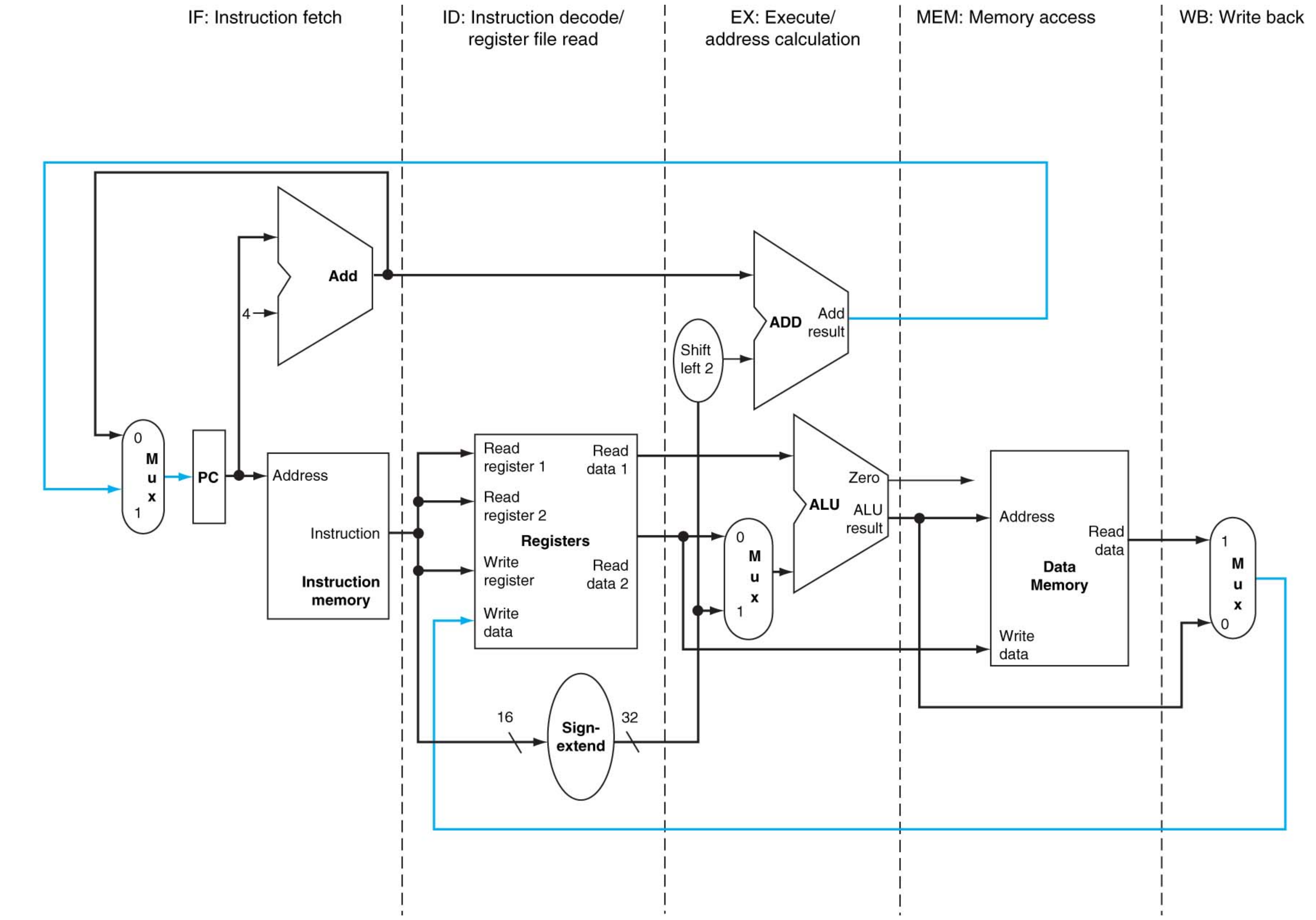
Pipelining Advantages

- Higher maximum throughput
- Higher utilization of CPU resources
- But, more complicated datapath, more complex control

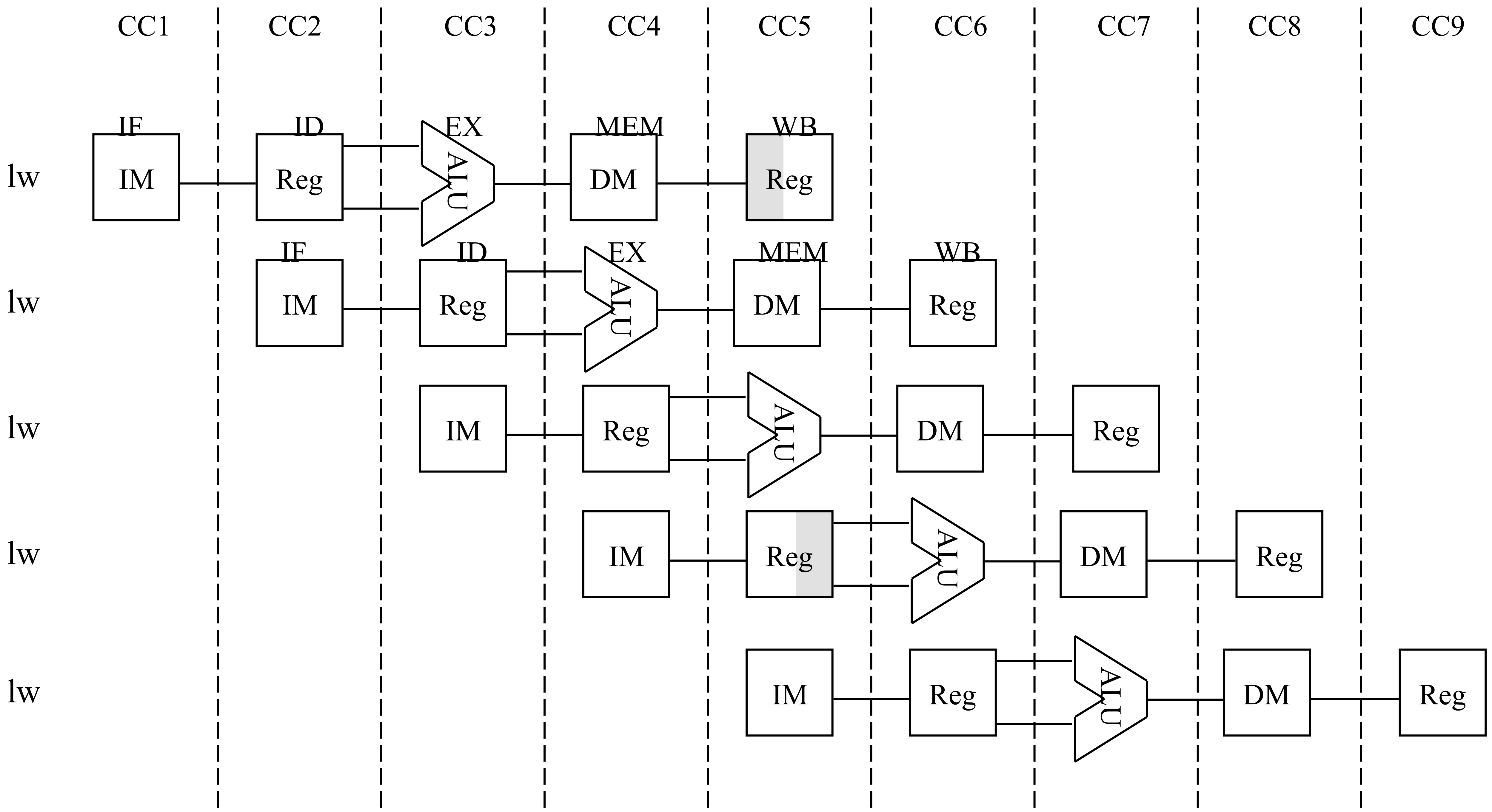
A Pipelined Datapath

- IF: Instruction fetch
- ID: Instruction decode and register fetch
- EX: Execution and effective address calculation
- MEM: Memory access
- WB: Write back

A Rough View of the Datapath



Execution in Pipelined Datapath



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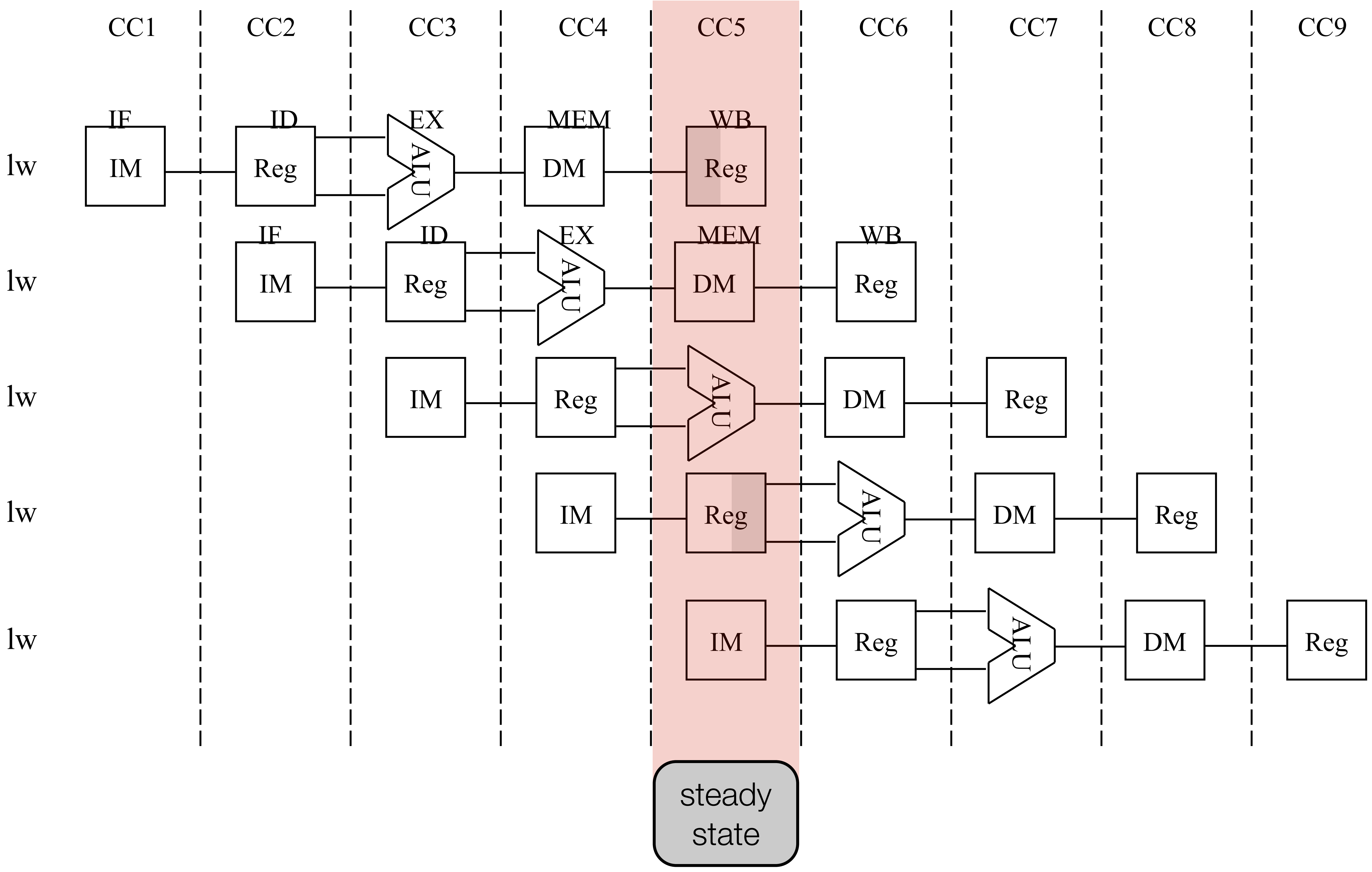
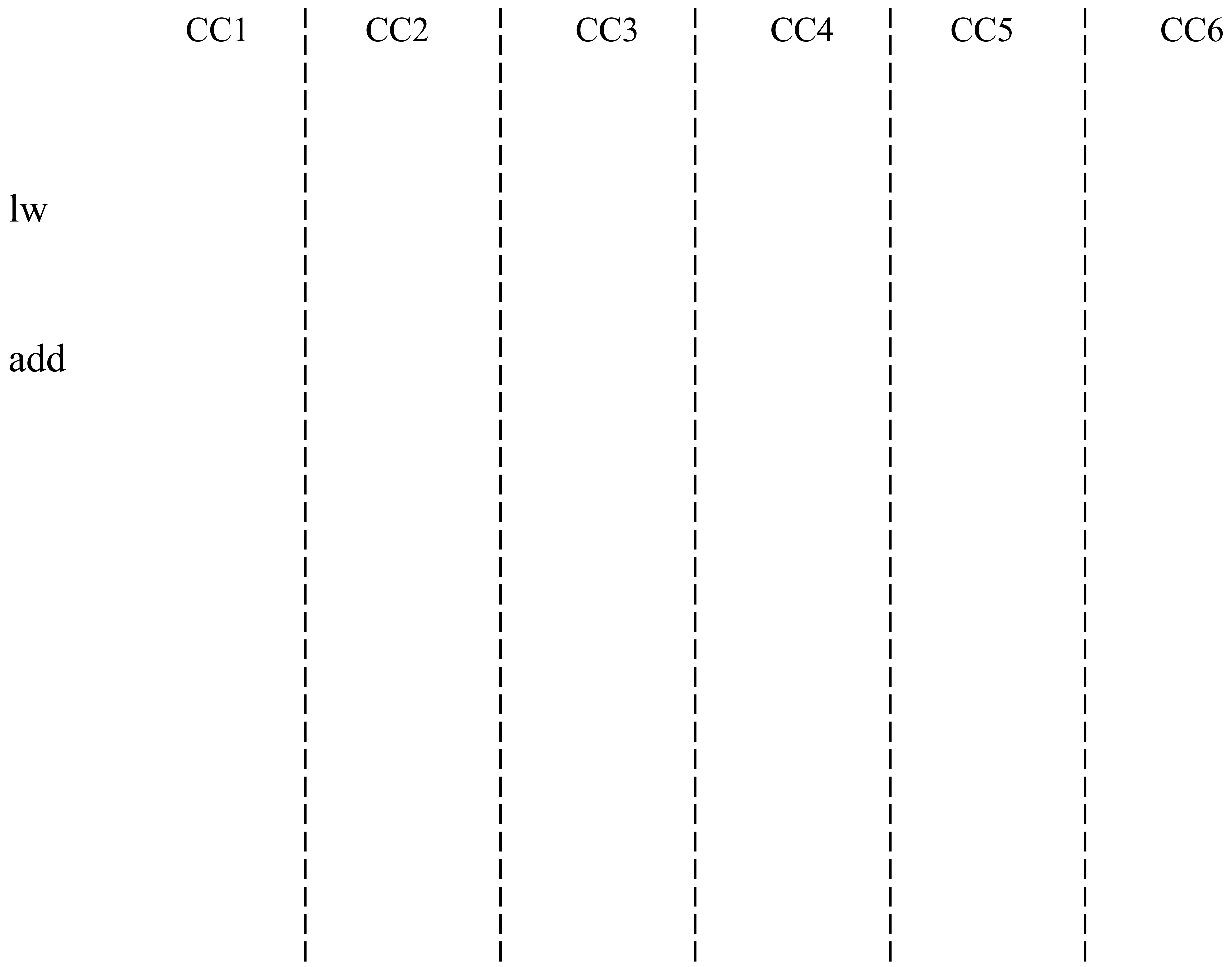


Mixed Instructions in the Pipeline



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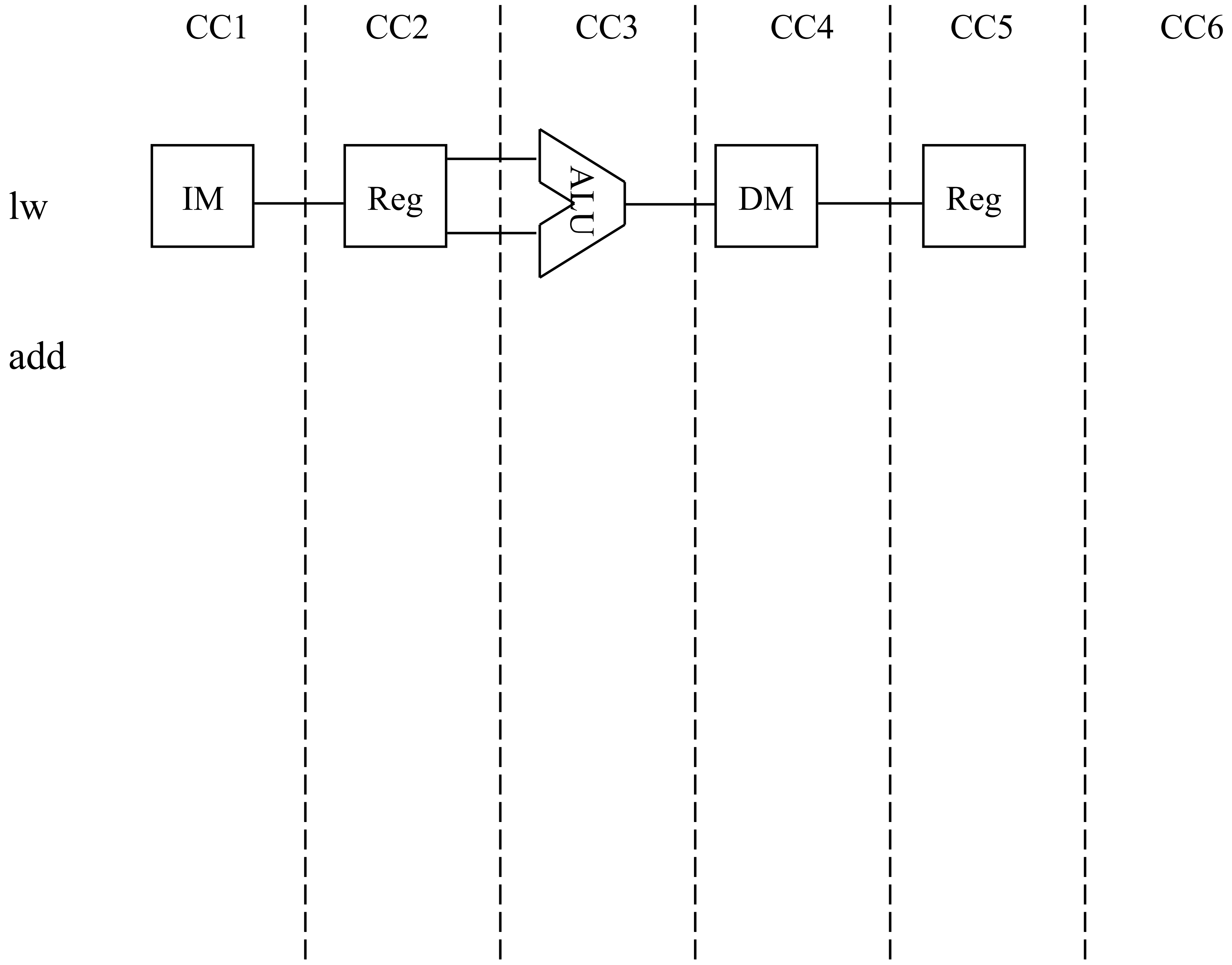

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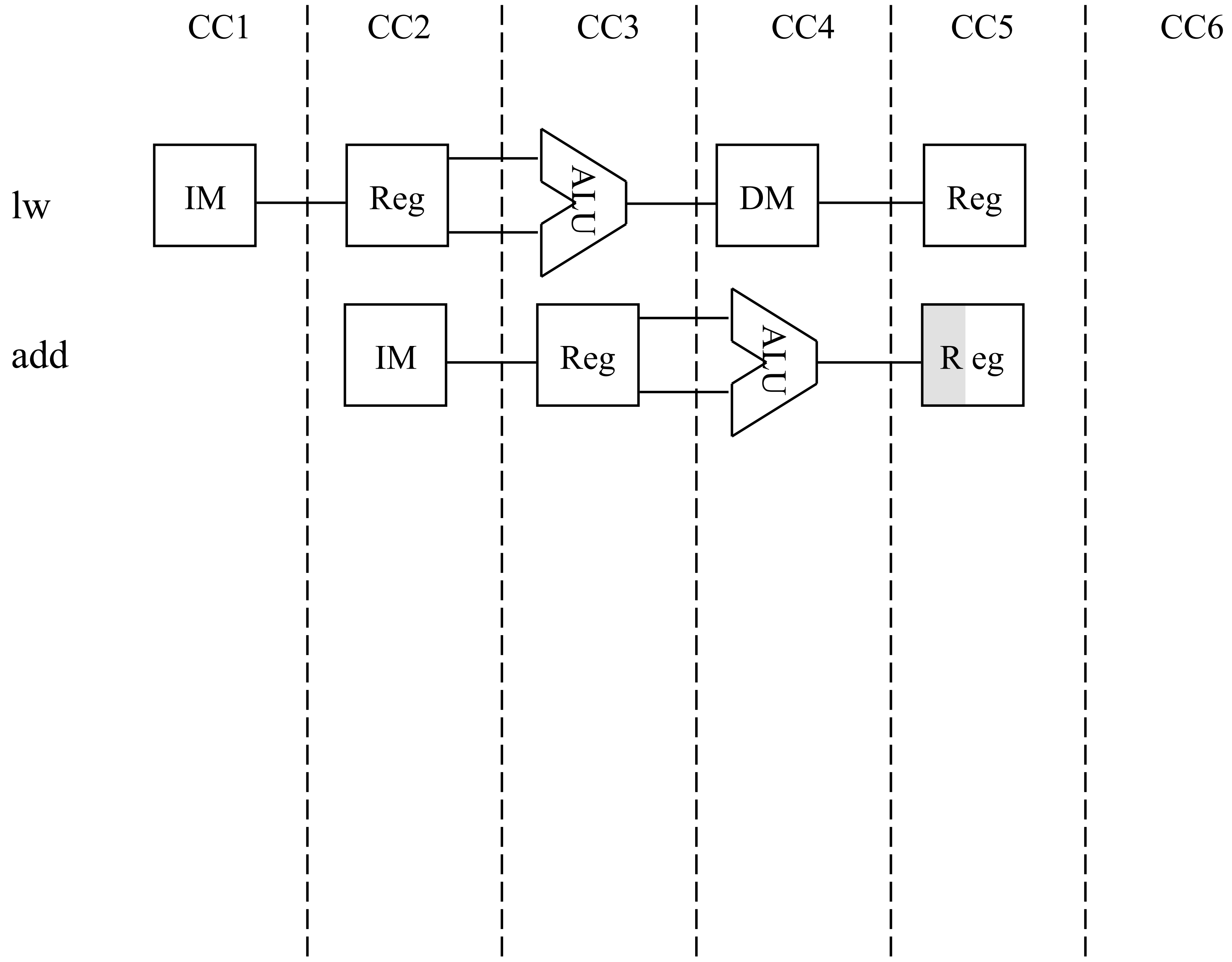

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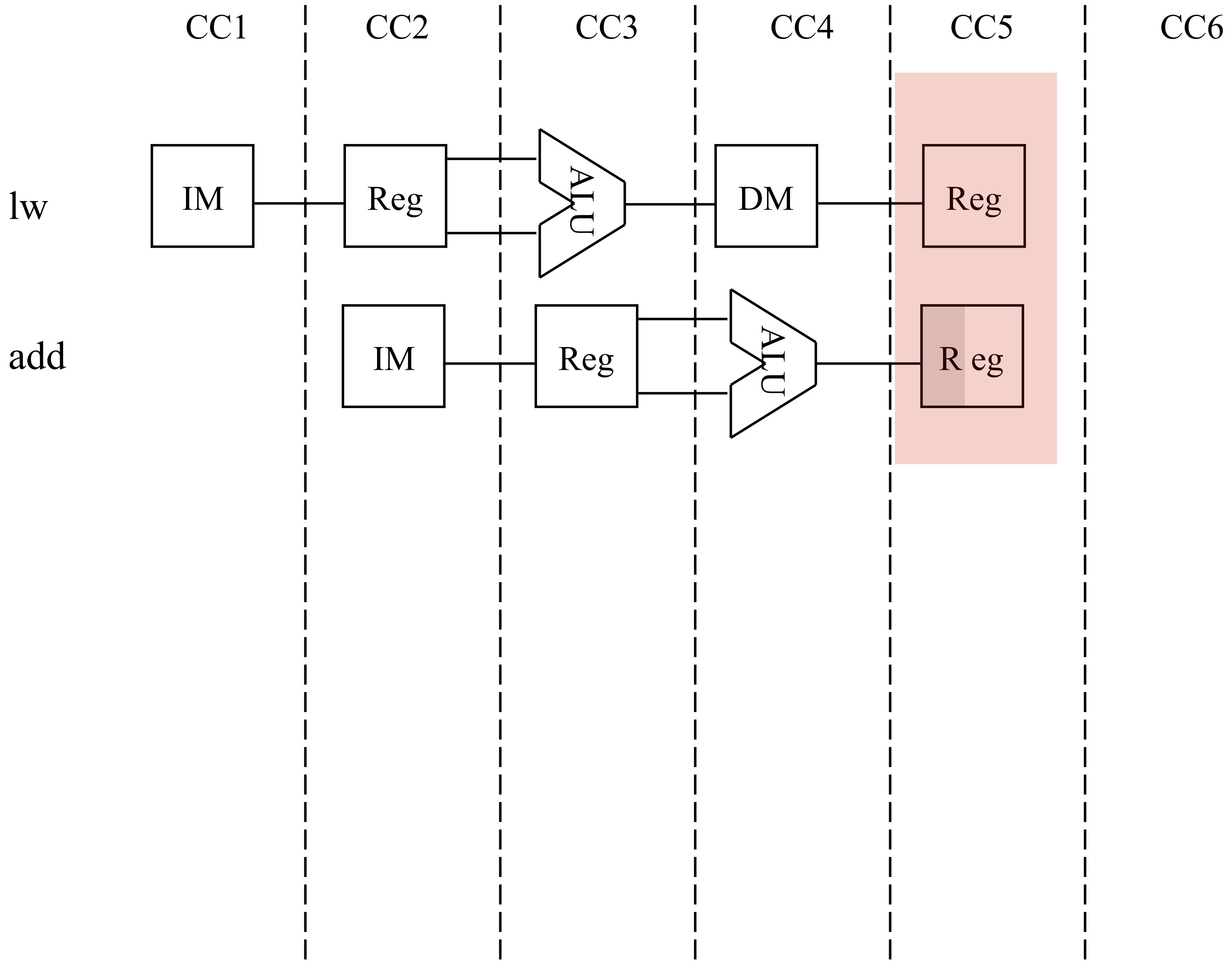
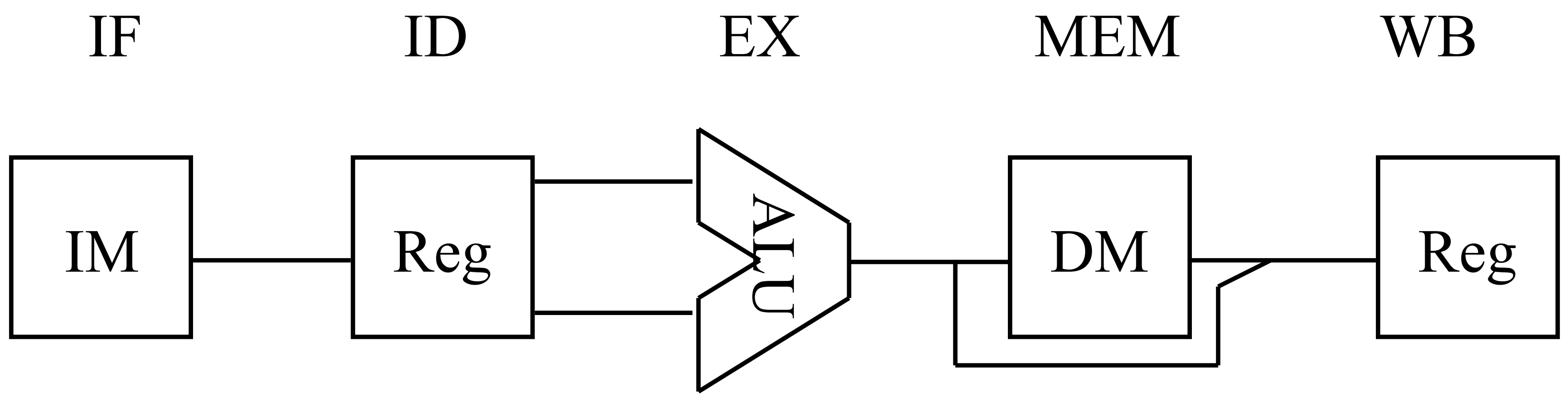


Pipeline Principles

- All instructions that share a pipeline should have the same stages in the same order.
    - therefore, add does nothing during Mem stage
    - sw does nothing during WB stage
- All intermediate values must be latched each cycle.
- There is no functional block reuse



Pipelined Datapath

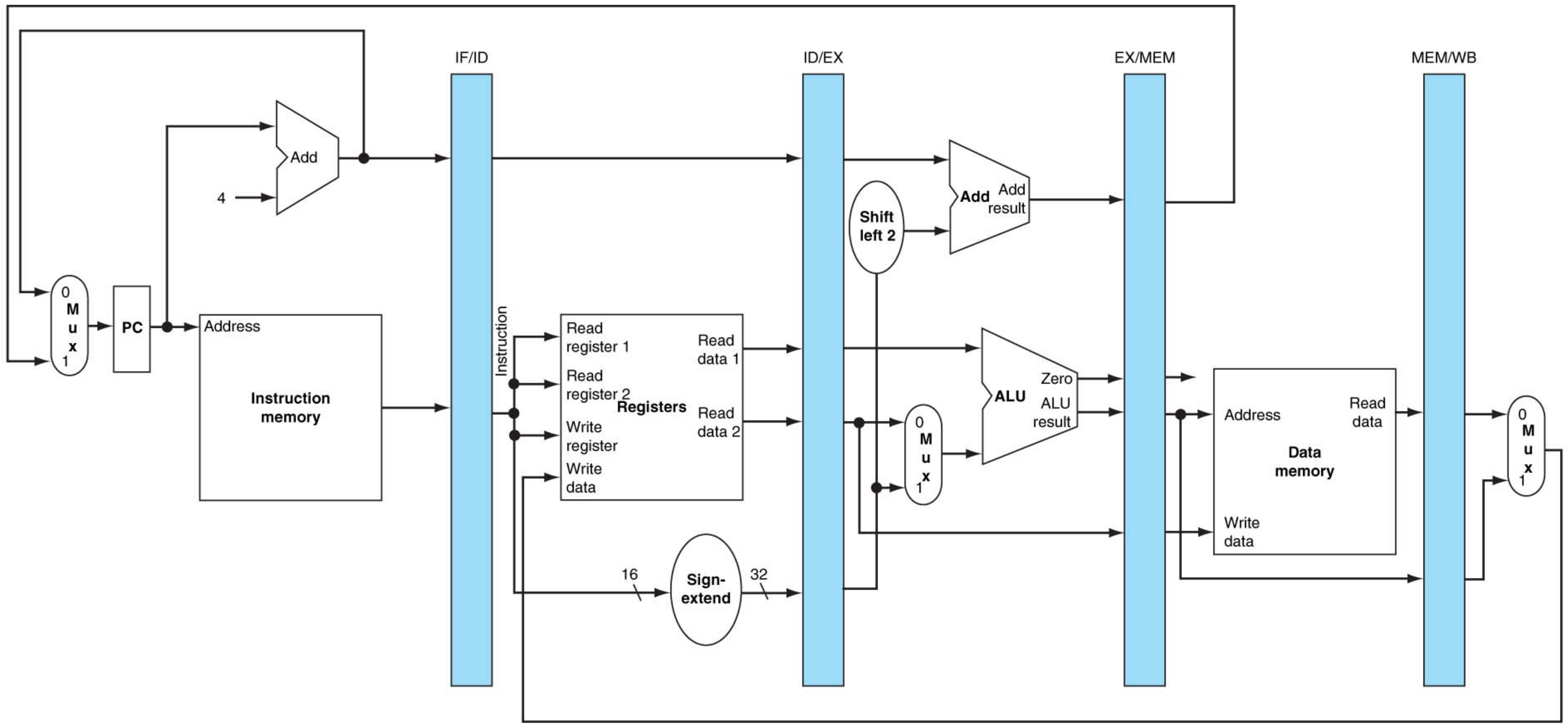
Instruction Fetch

Decode /
Reg. Fetch

Execute

Memory

Write-back



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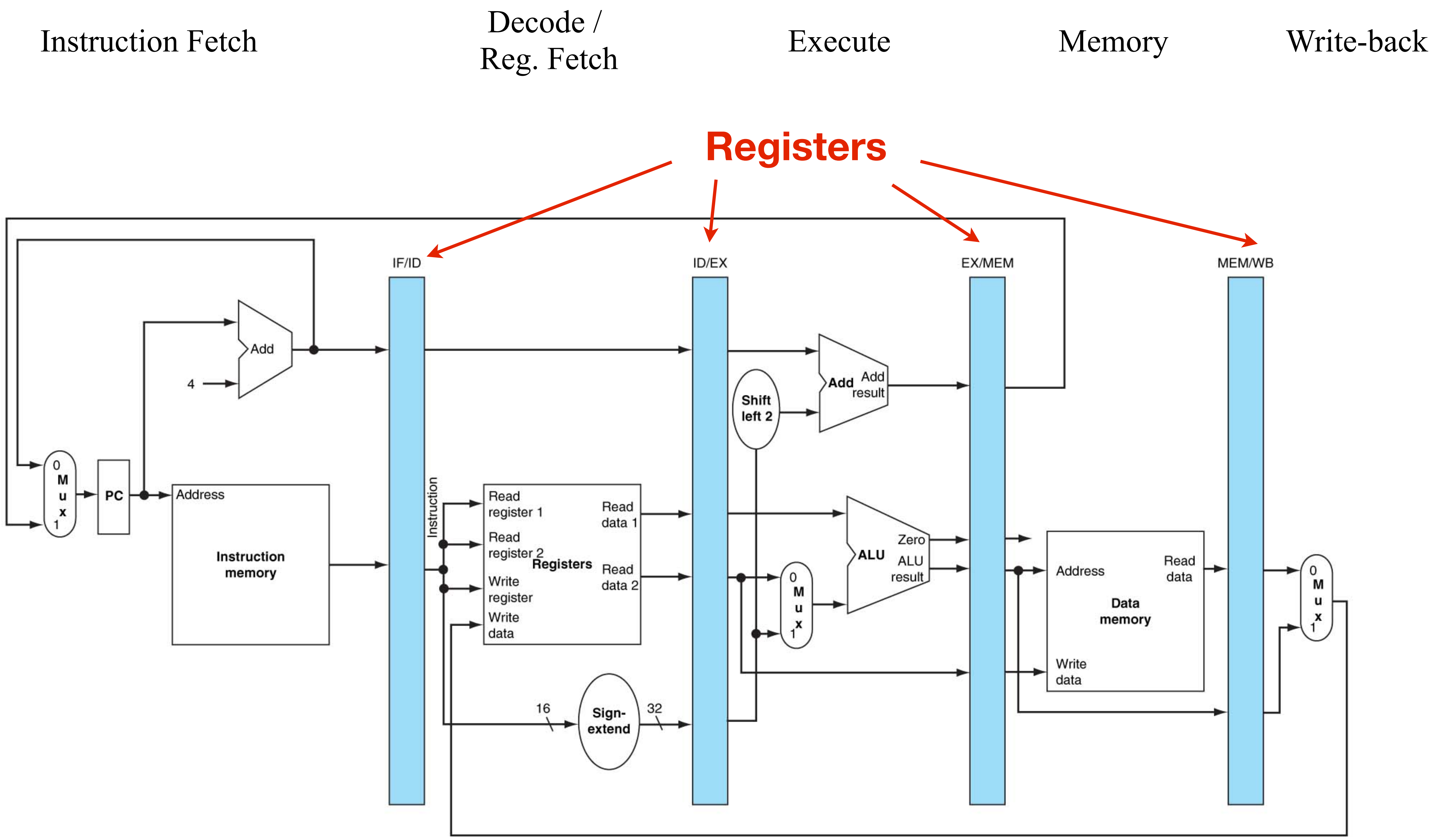

Pipeline In Execution

Instruction Fetch

Decode /
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Execute

Memory

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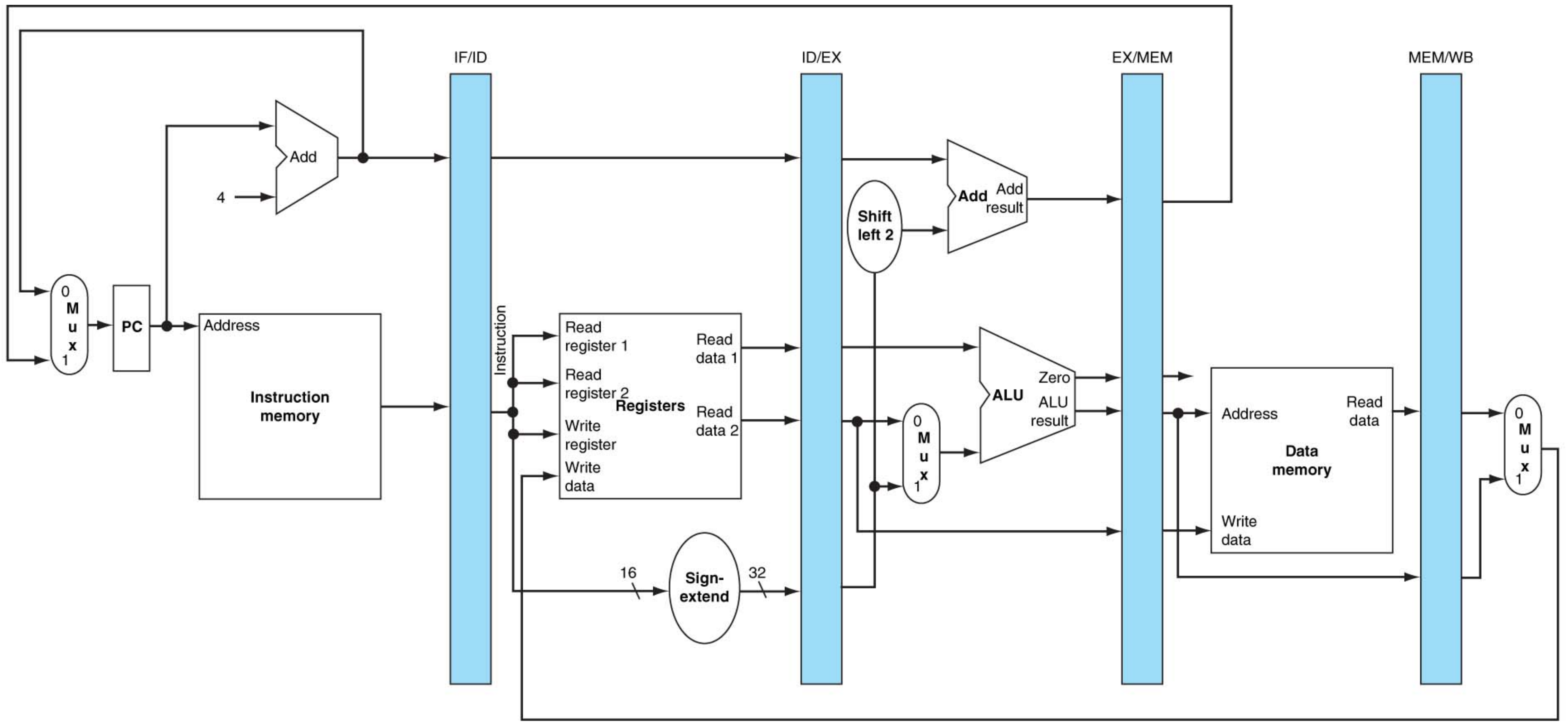

Pipeline In Execution

Instruction Fetch

Decode /
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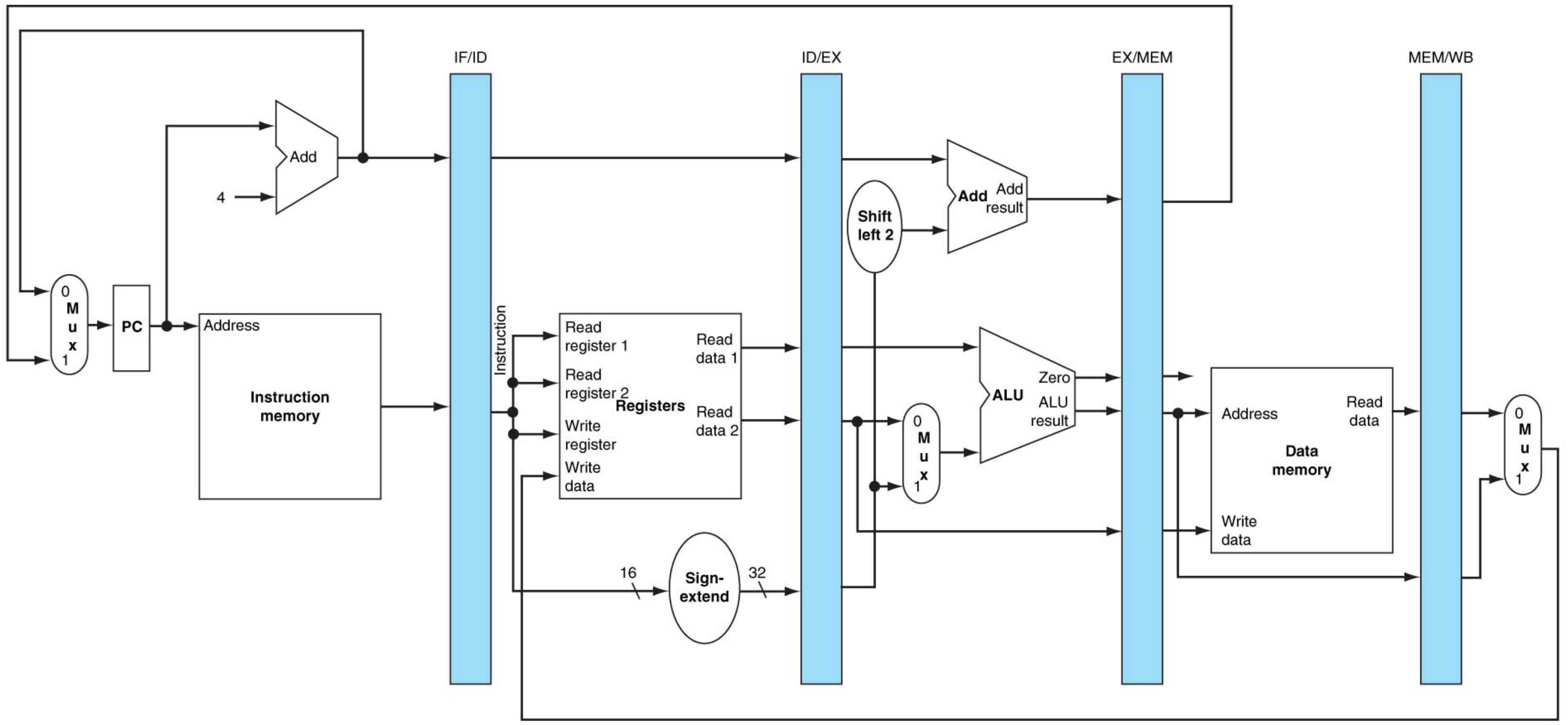
Execute

Memory

Write-back

add $10, $1, $2



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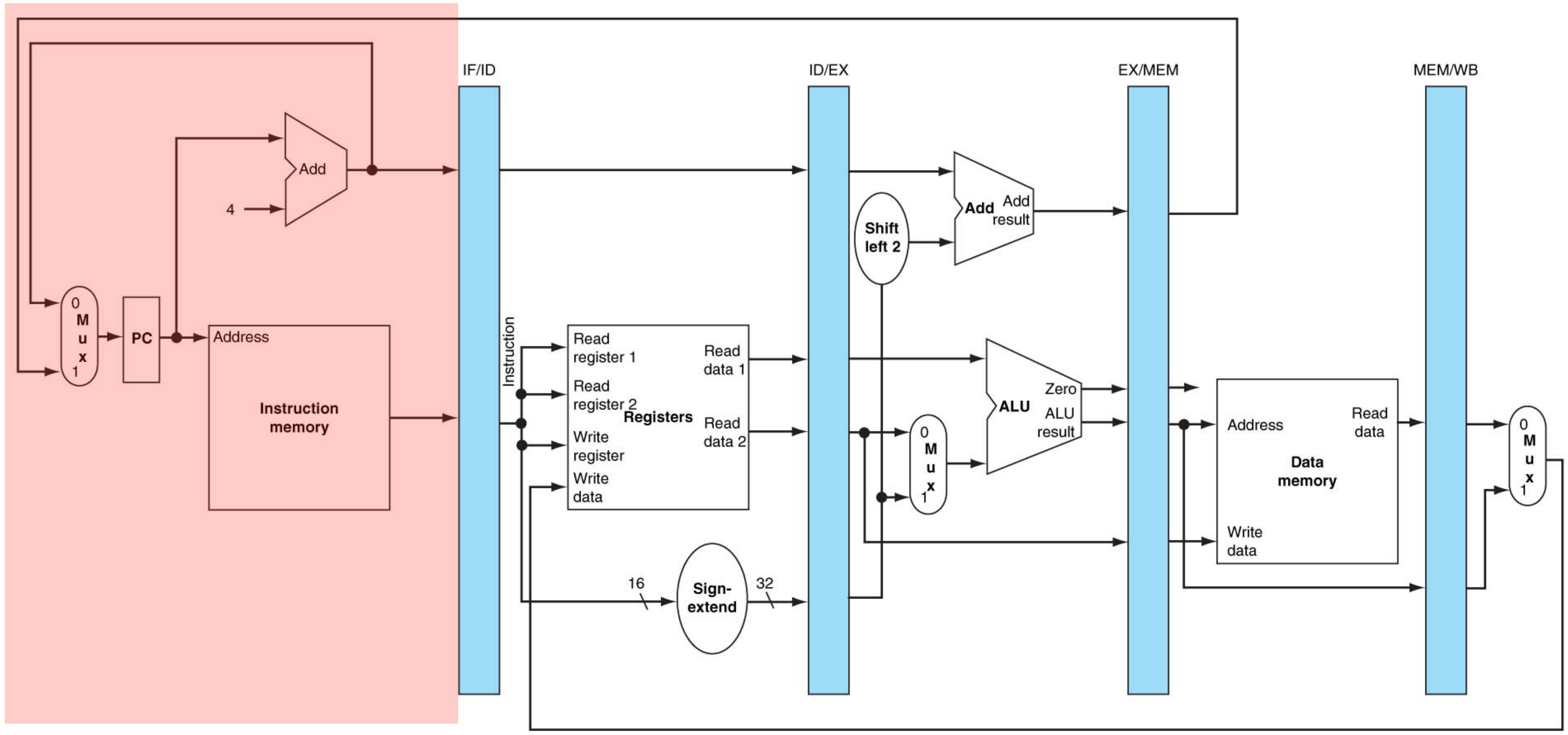

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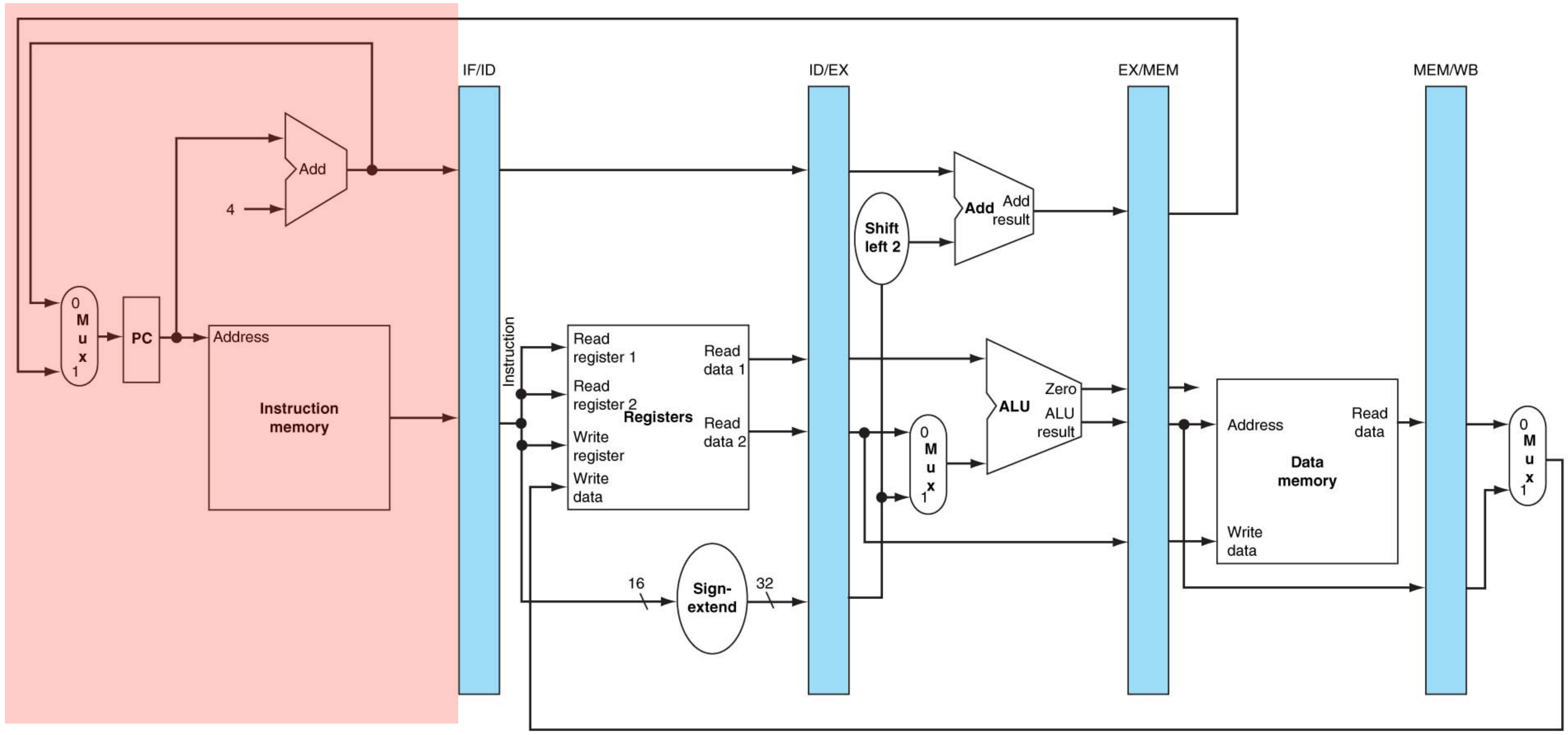


Pipeline In Execution

Instruction Fetch

Decode / Reg. Fetch

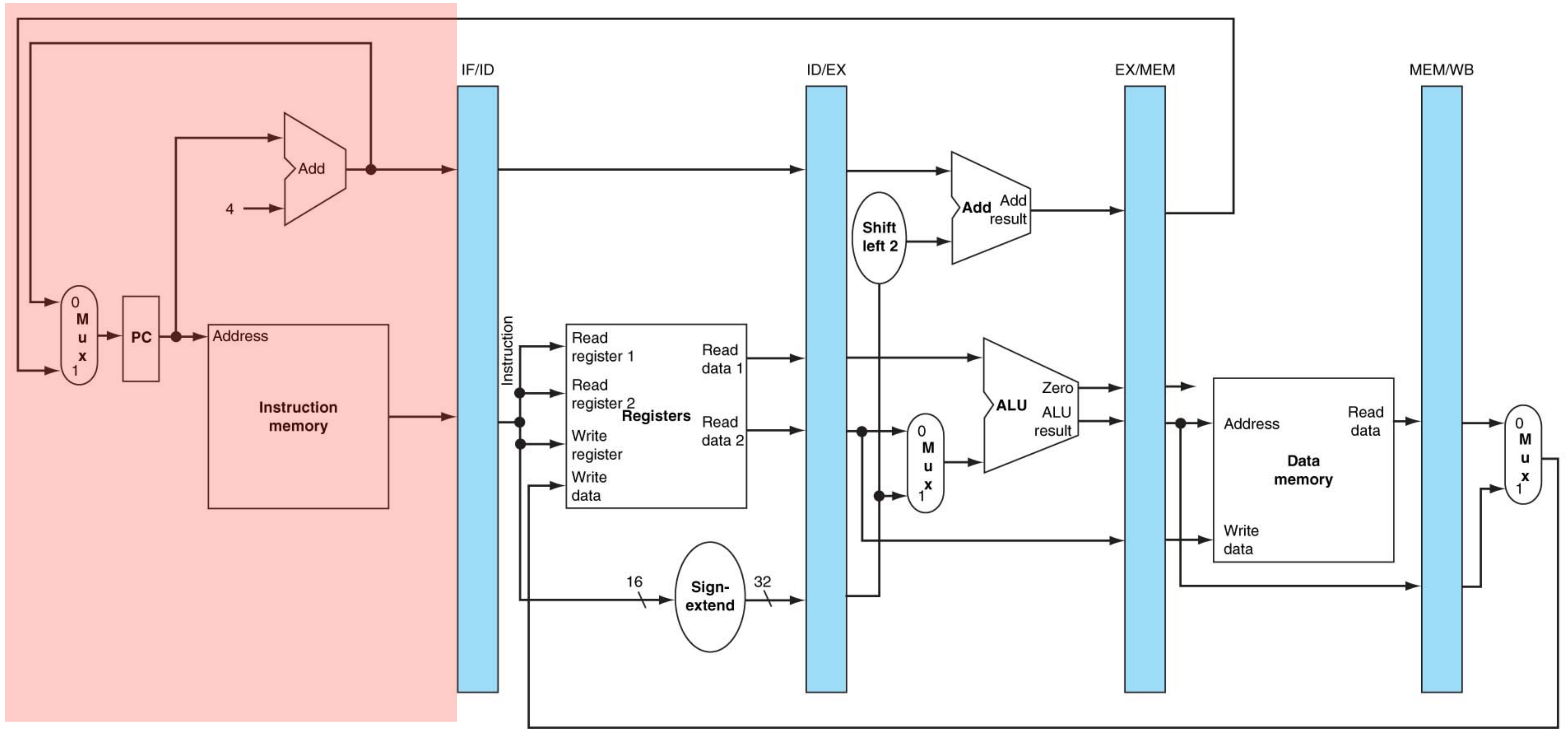
Execute

Memory

Write-back

lw $12, 1000($4)

add $10, $1, $2



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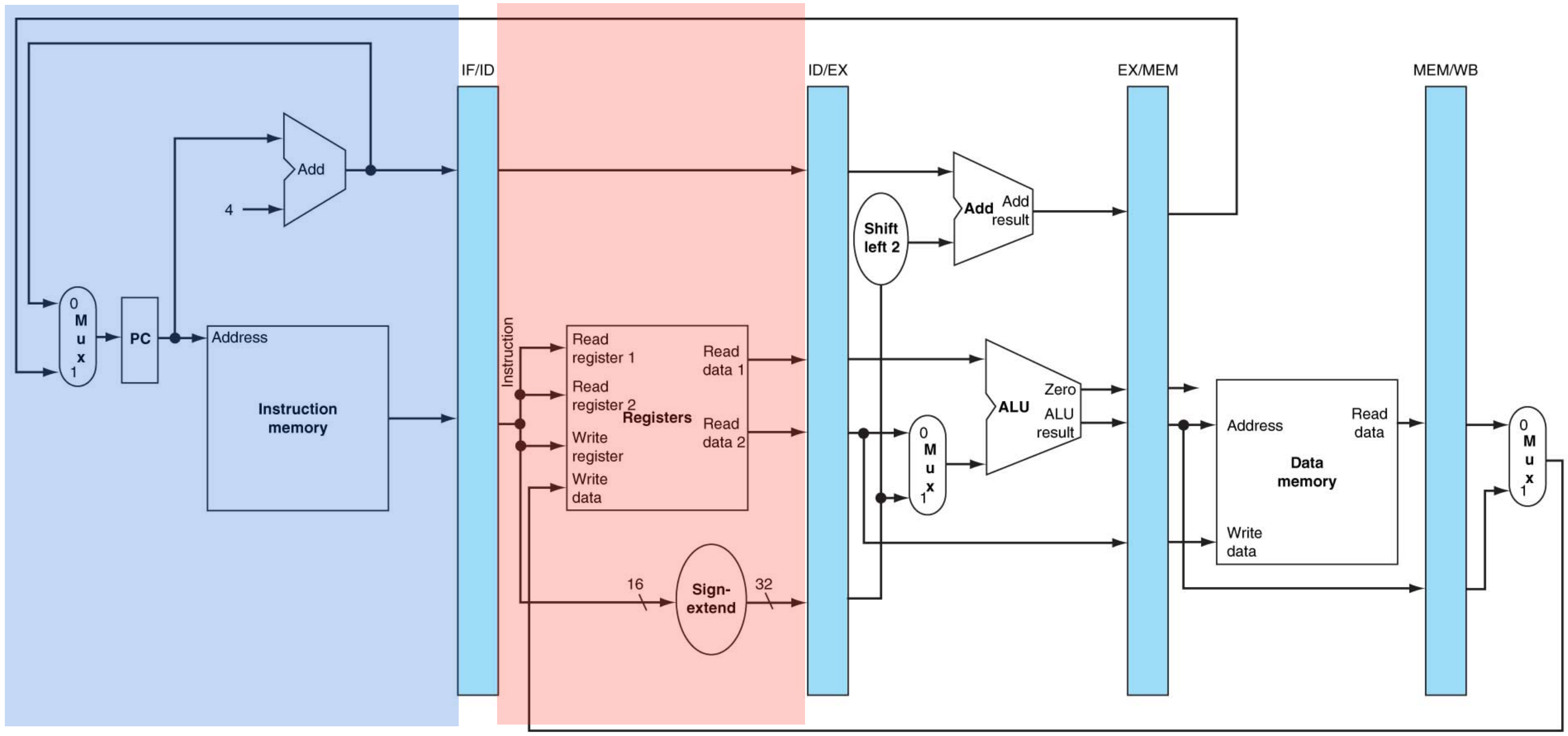

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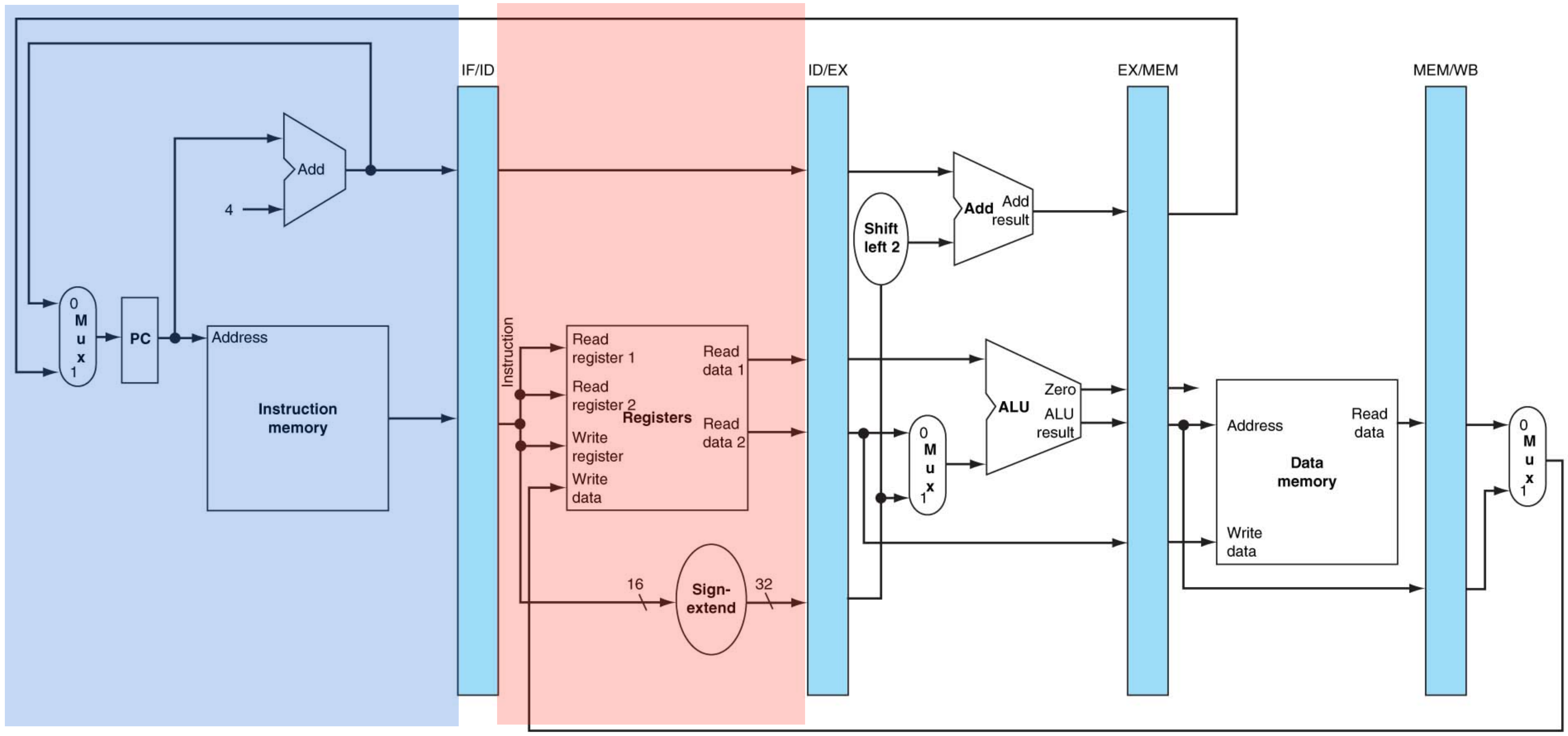
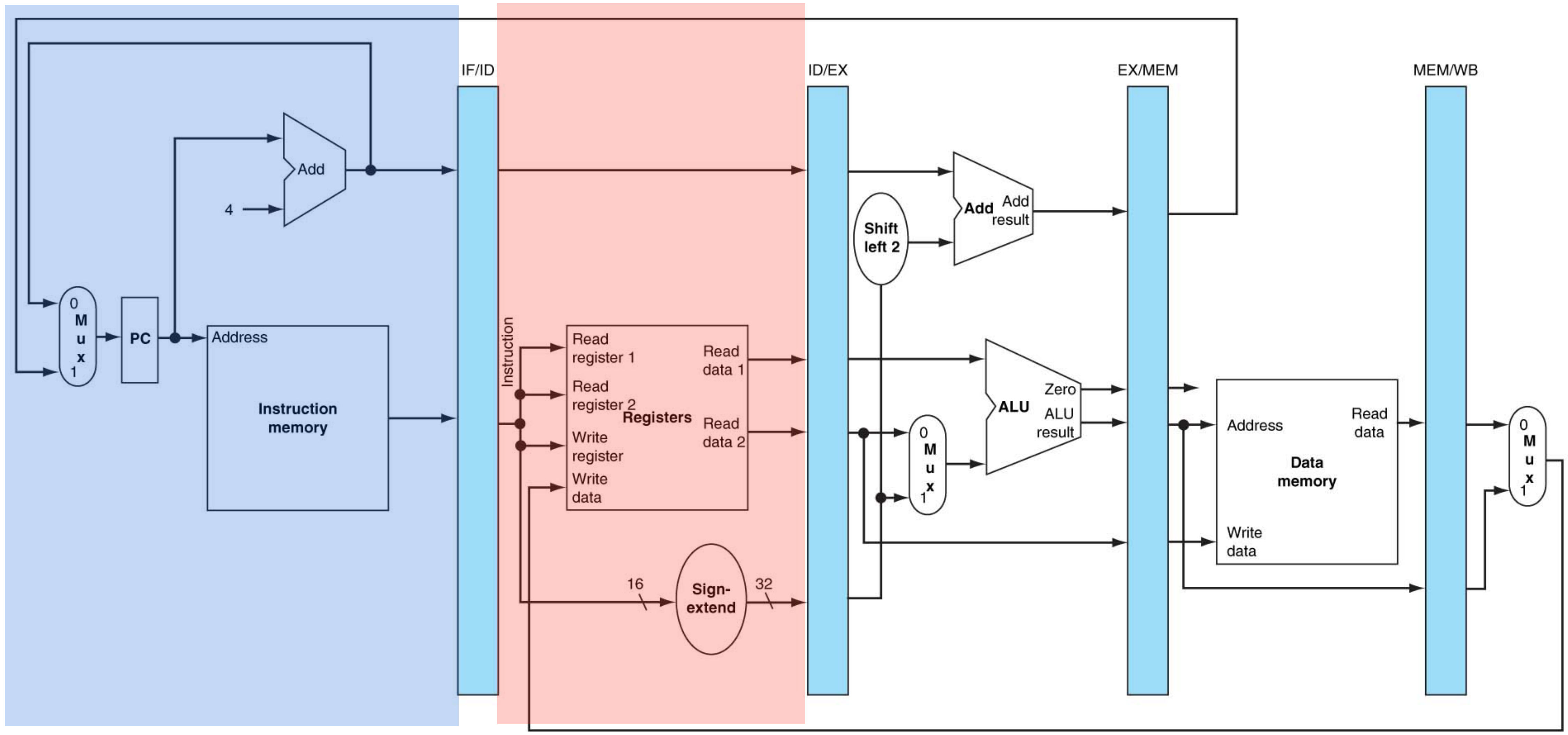


Pipeline In Execution

Instruction Fetch | Decode / Reg. Fetch | Execute | Memory | Write-back

sub $15, $4, $1 | lw $12, 1000($4) | add $10, $1, $2



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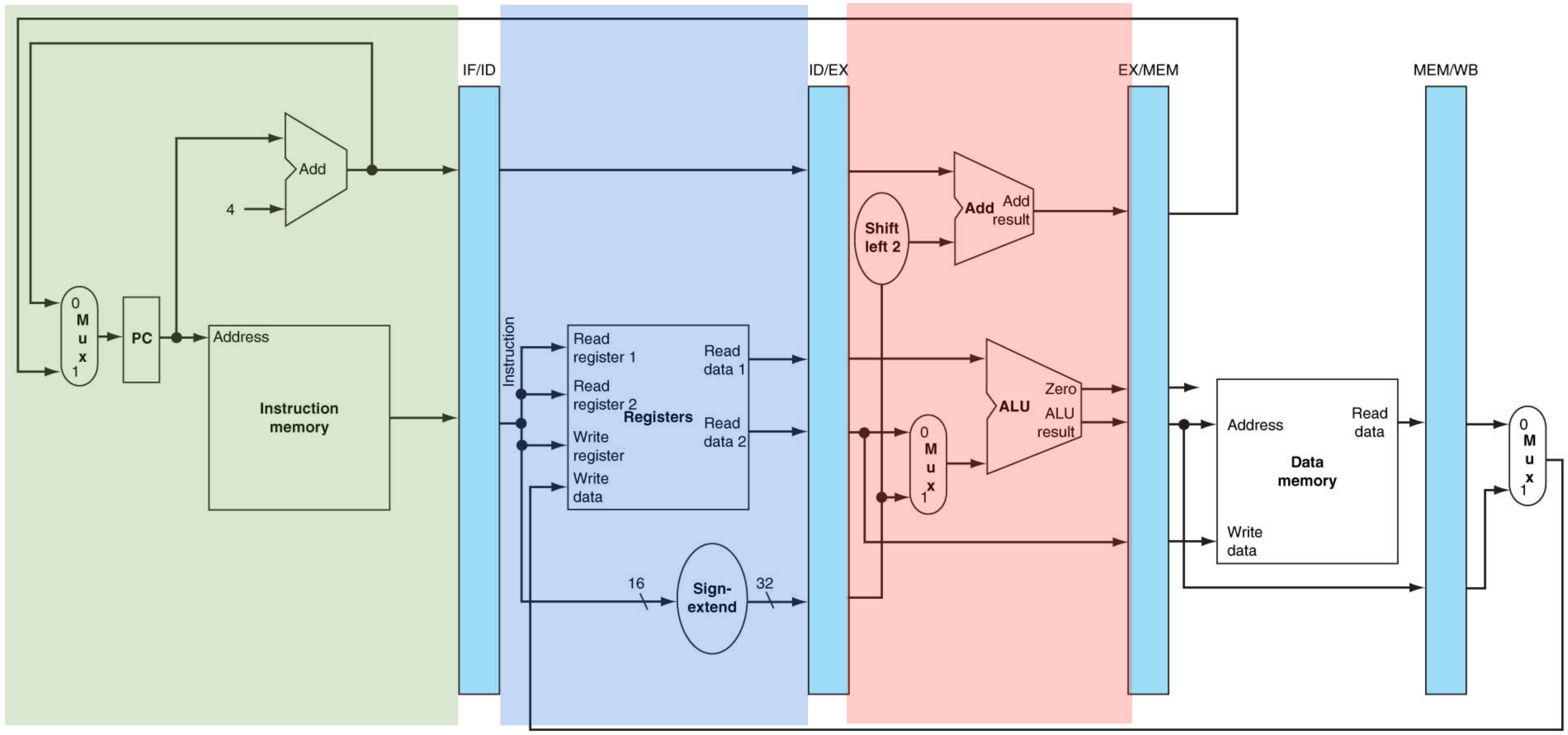

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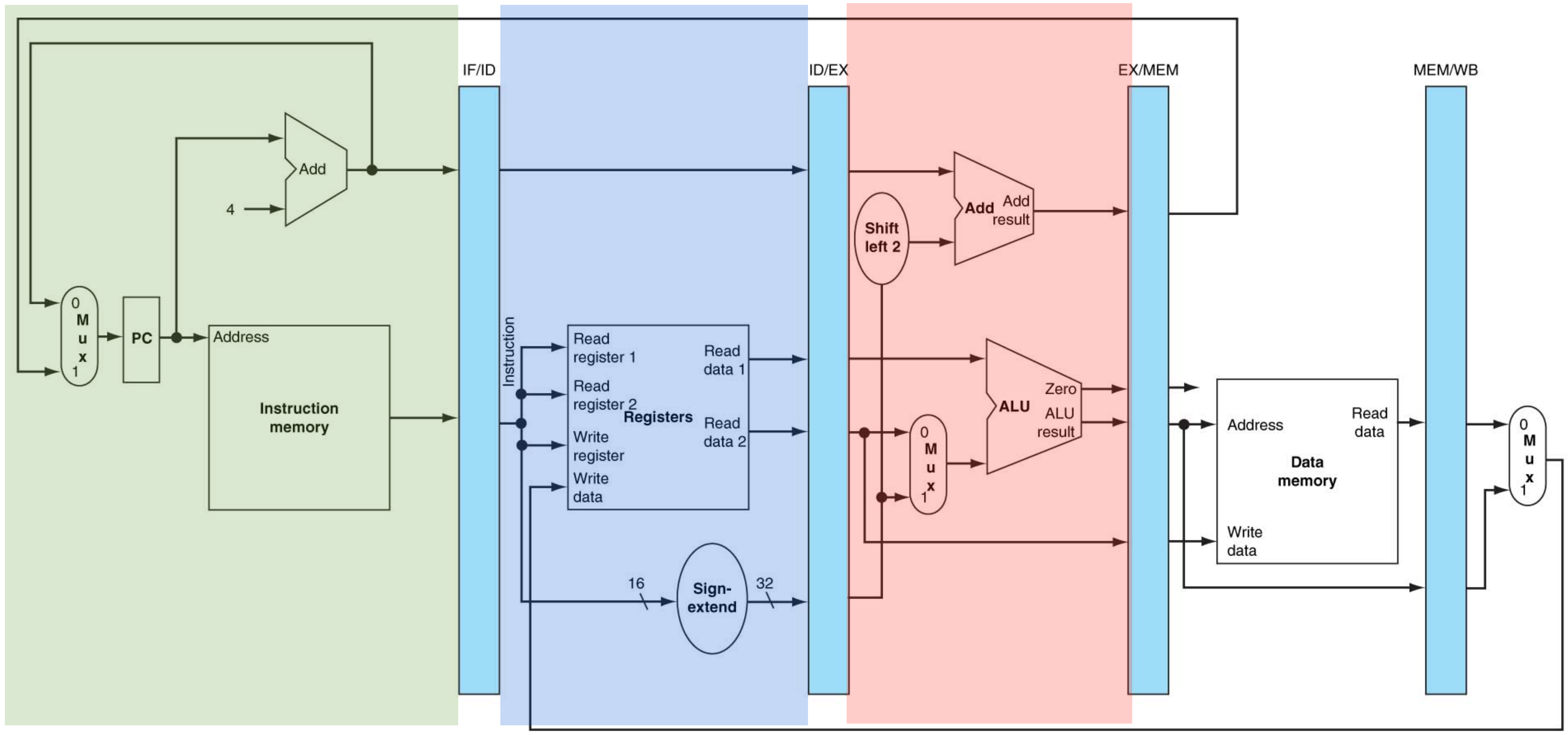

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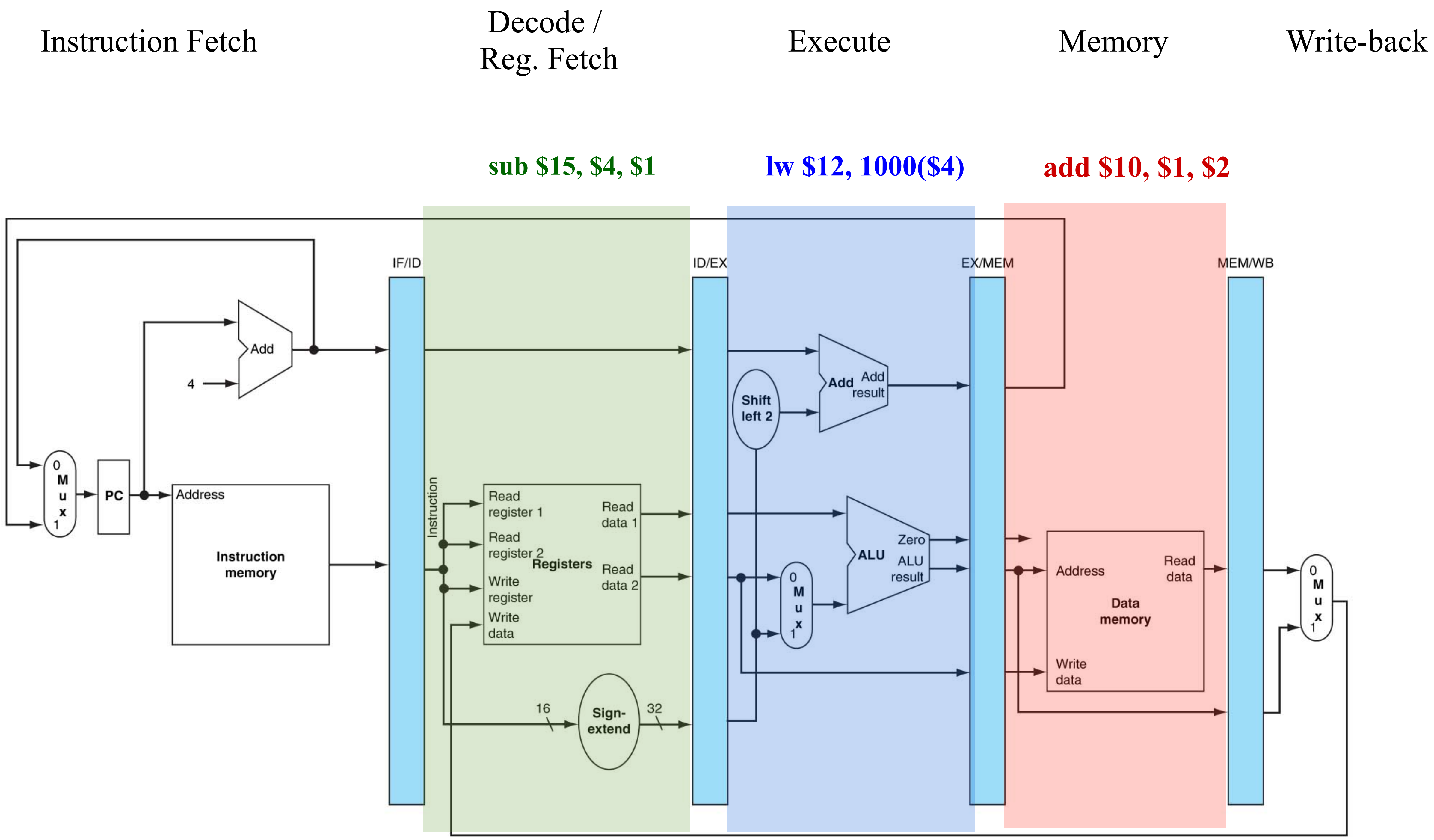

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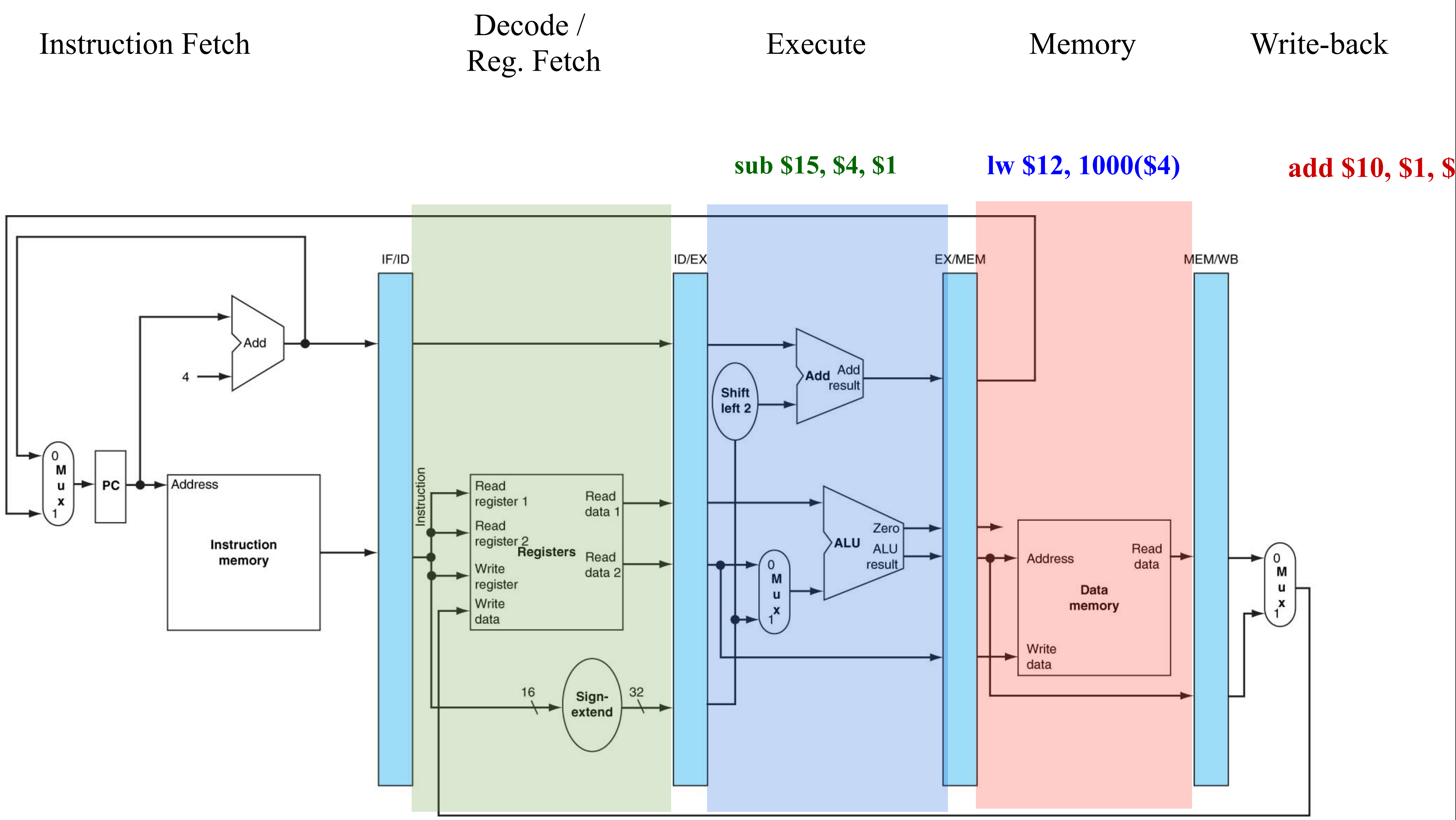

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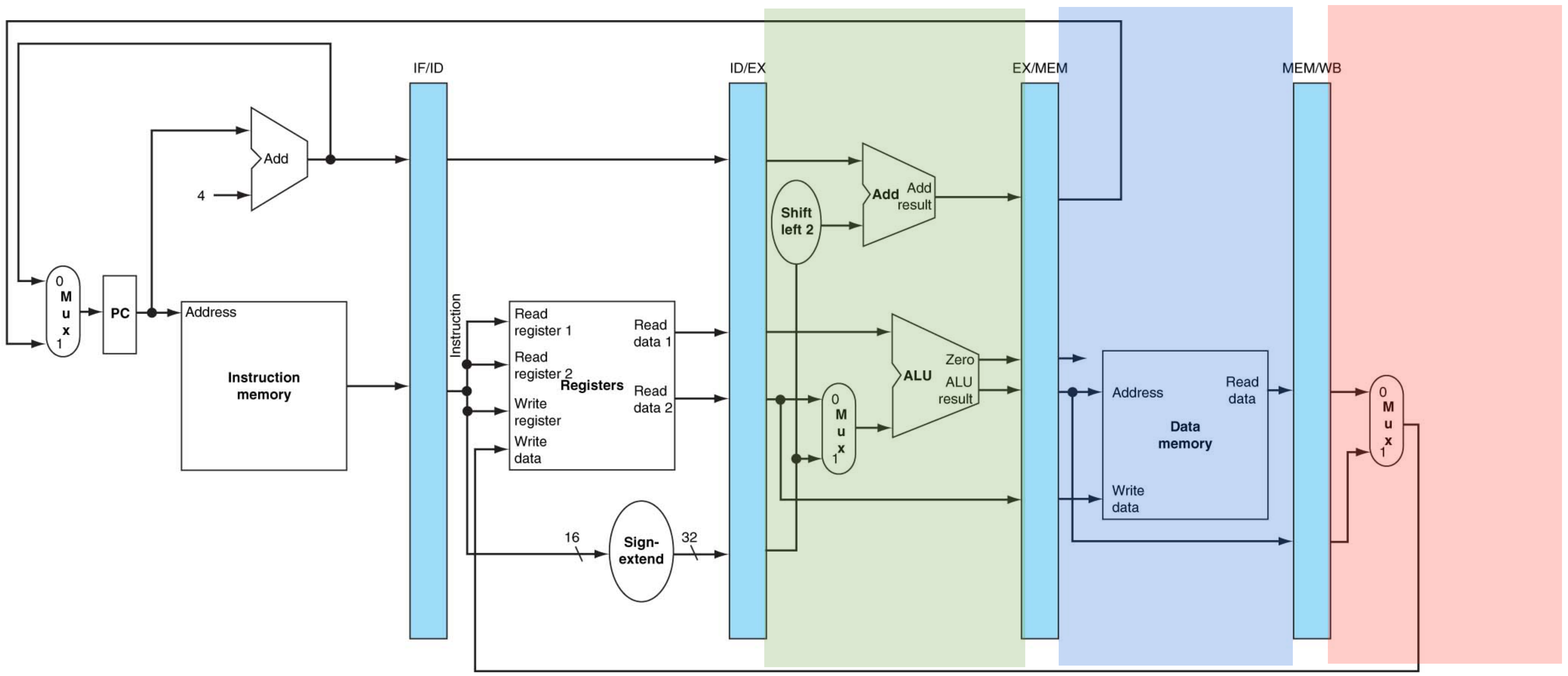

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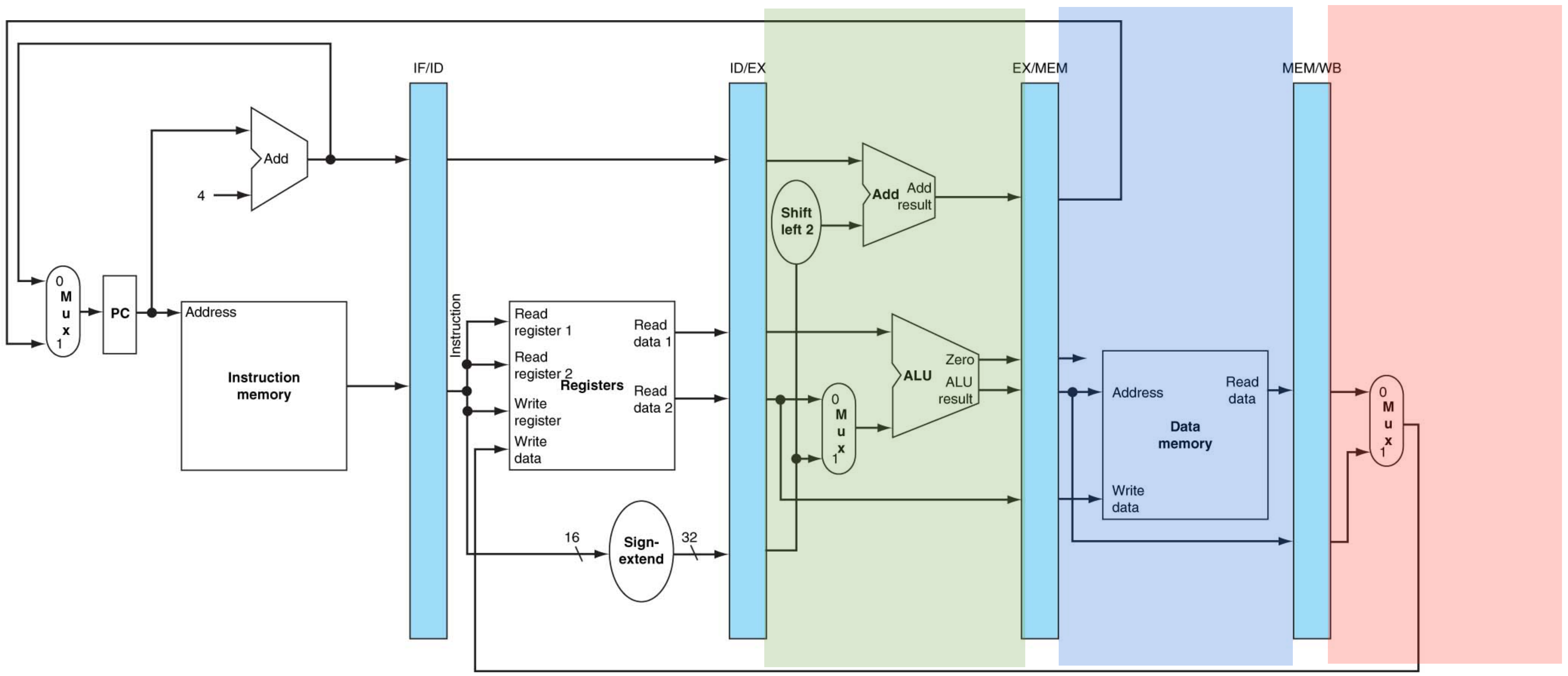

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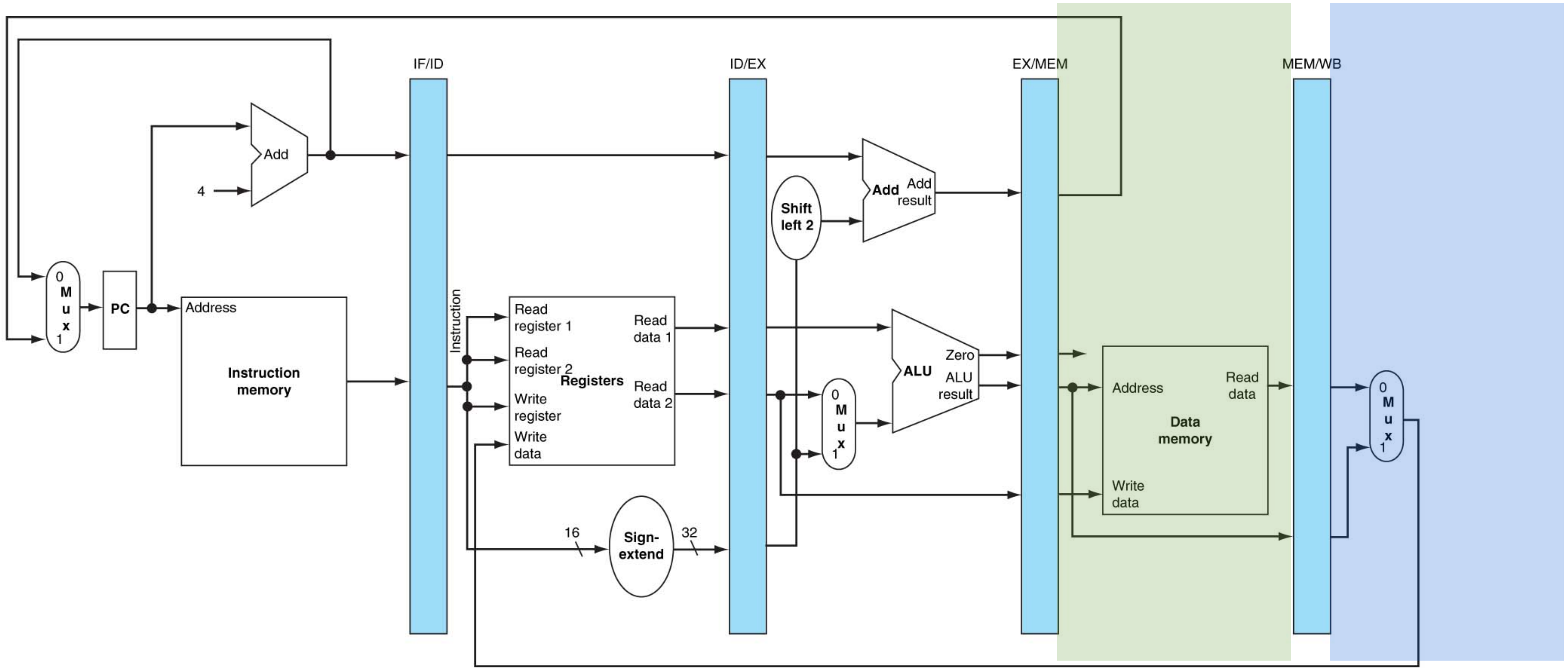

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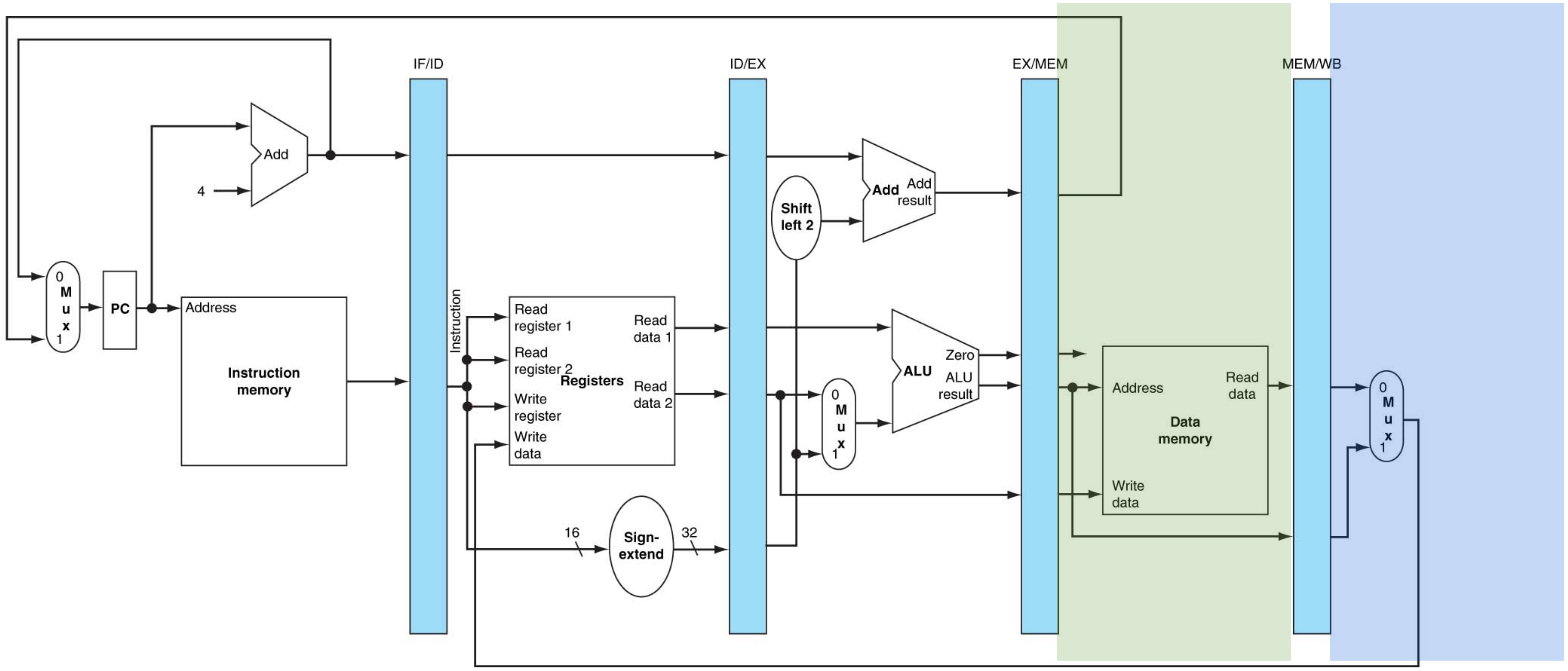

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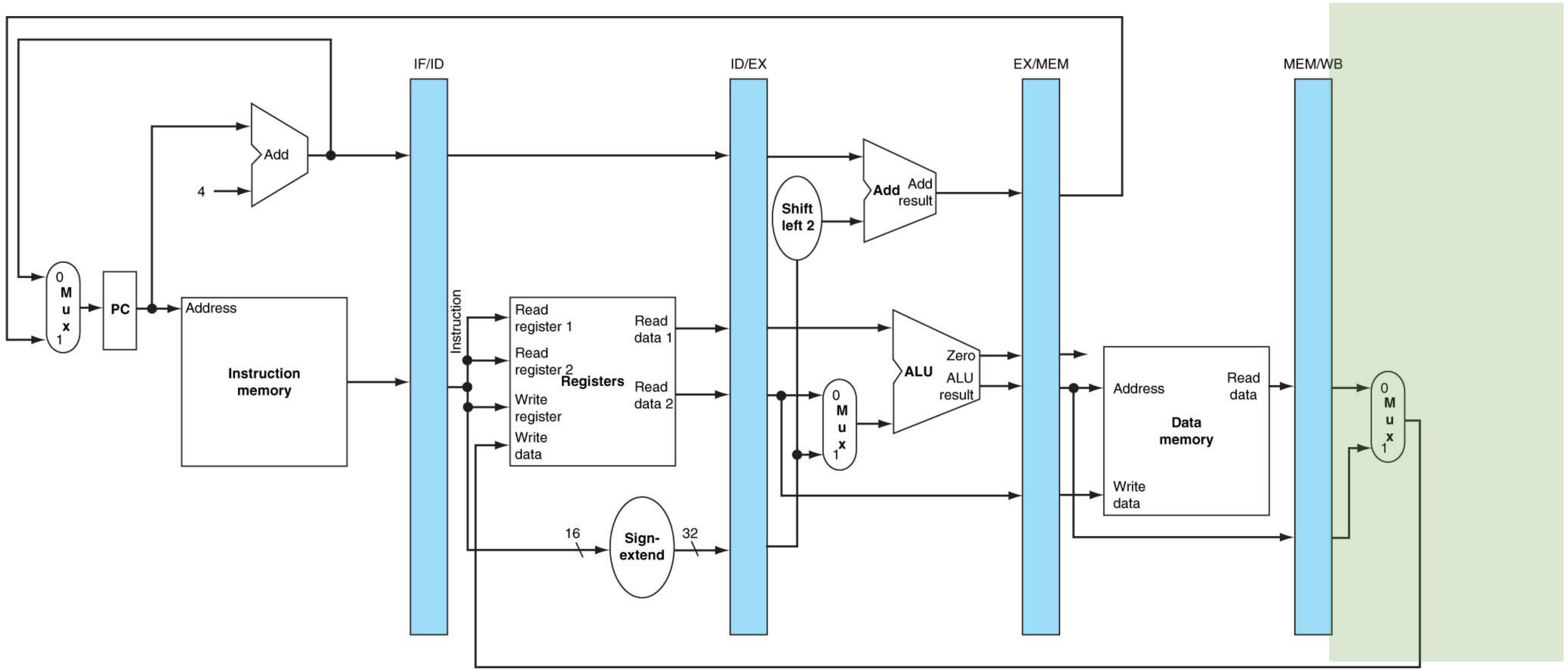

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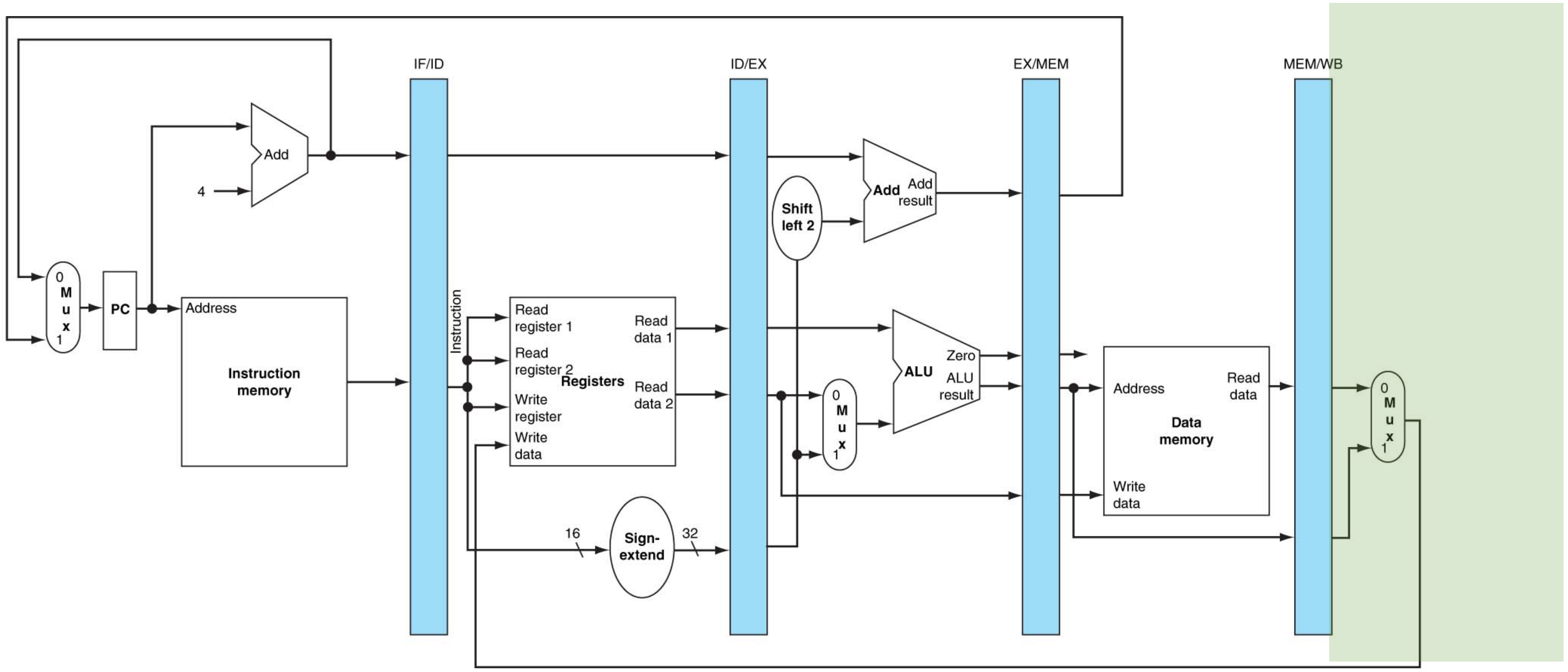

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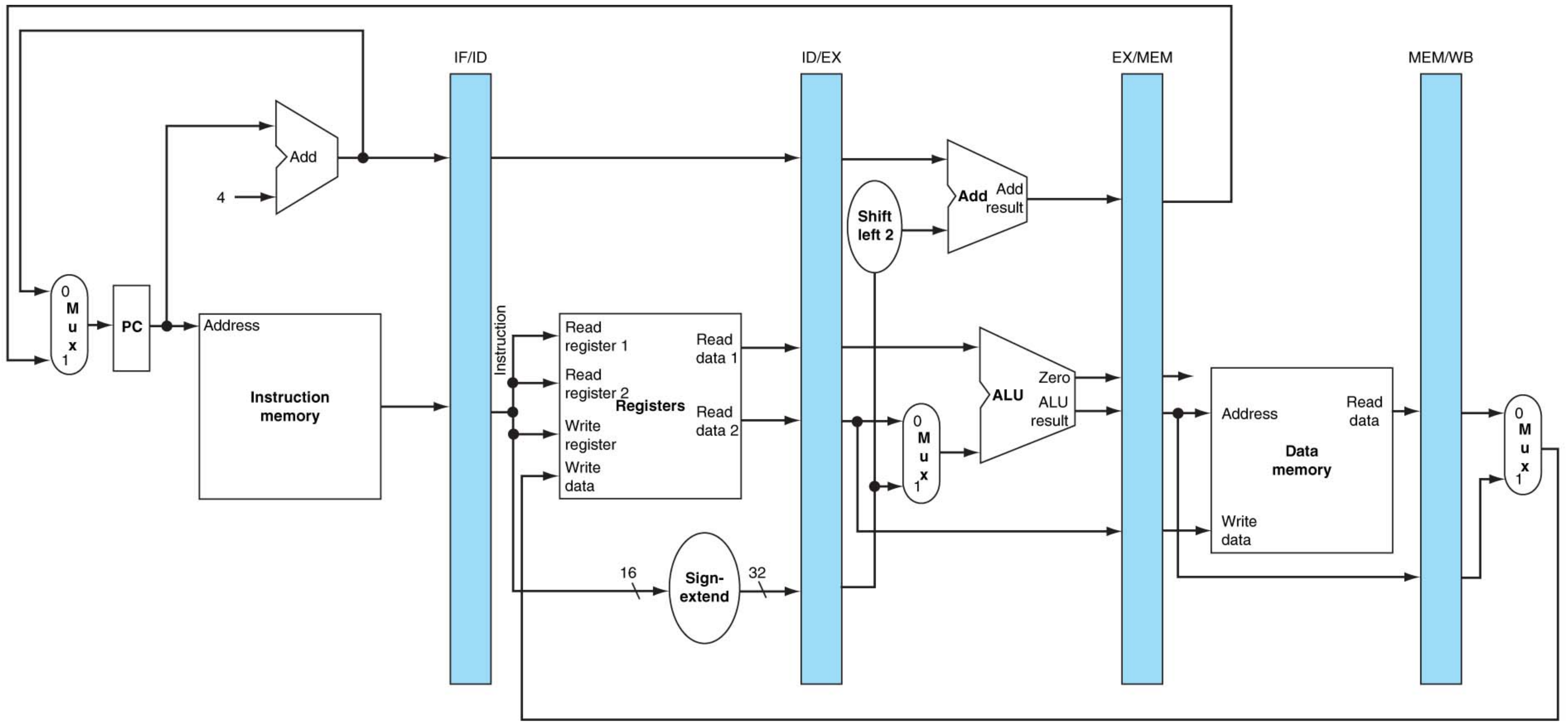
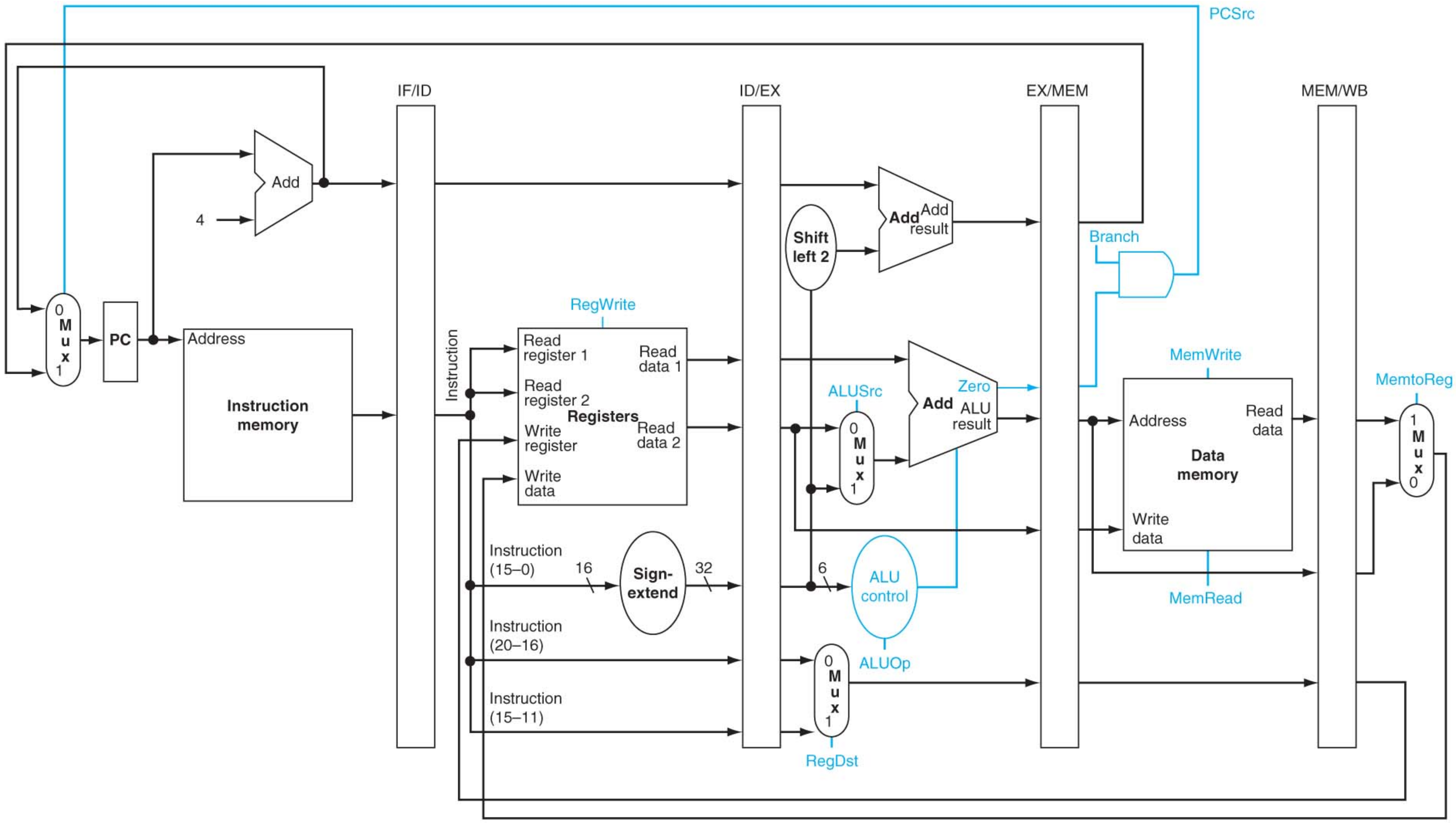


Pipeline with Controls



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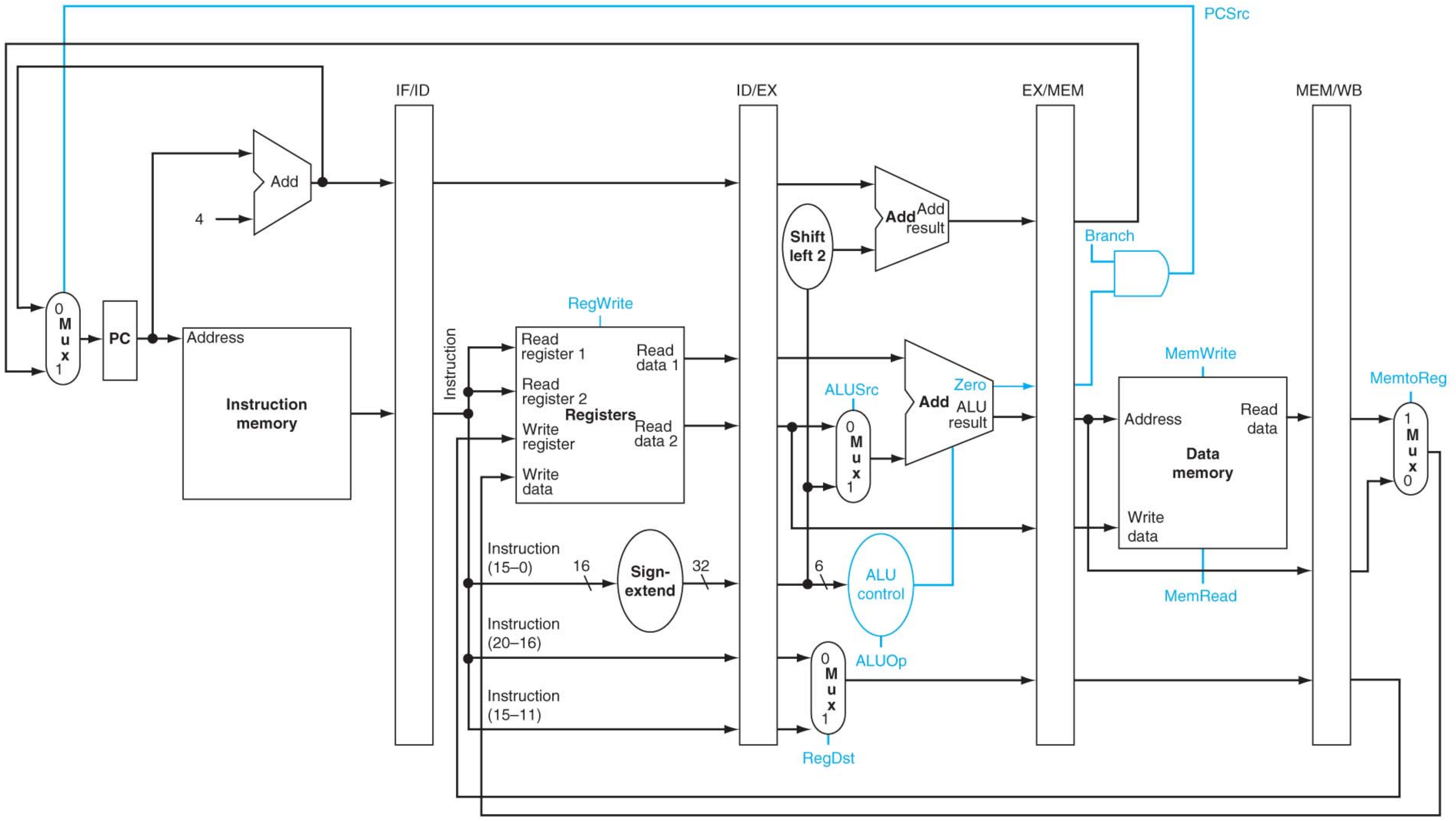
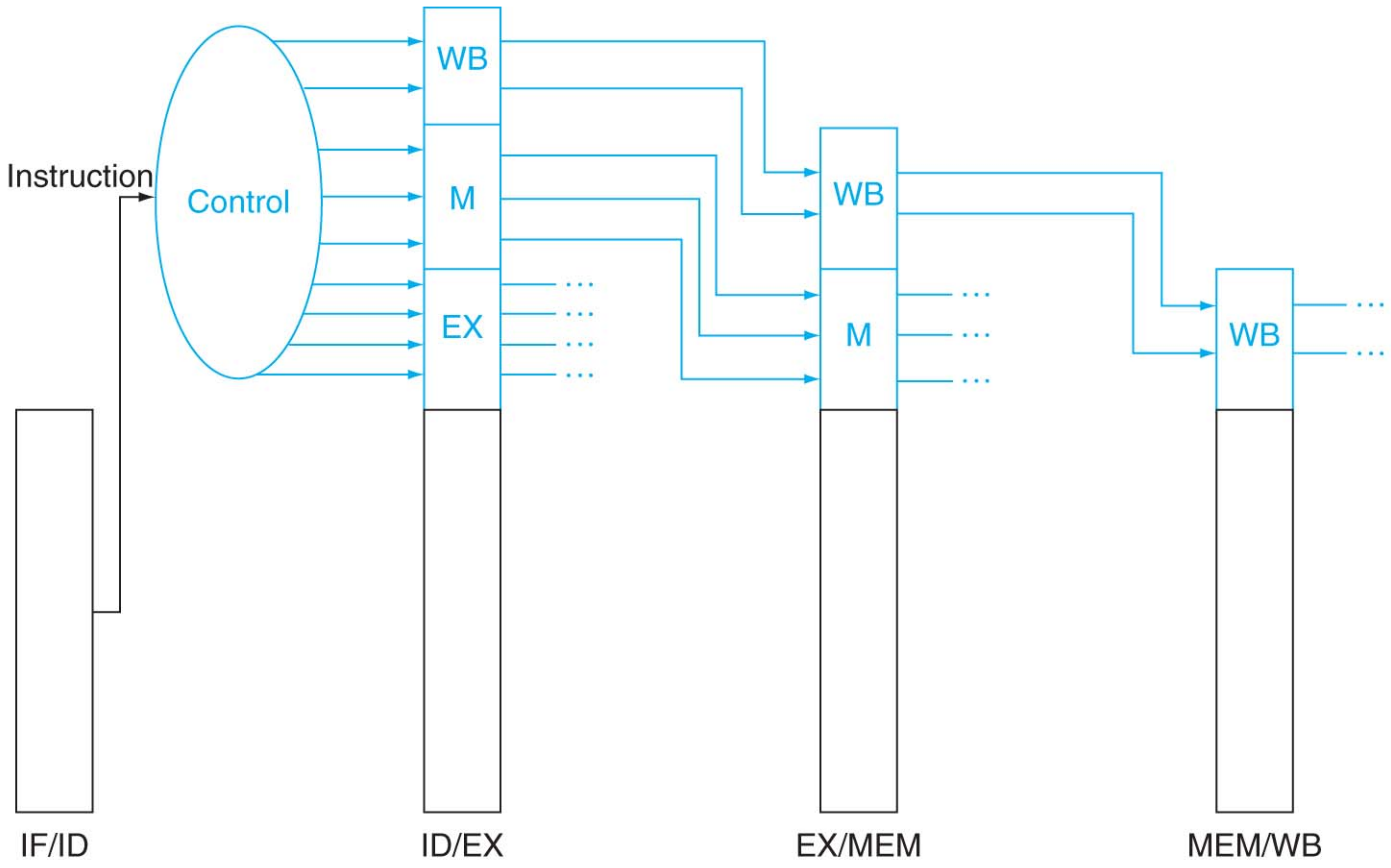


But...

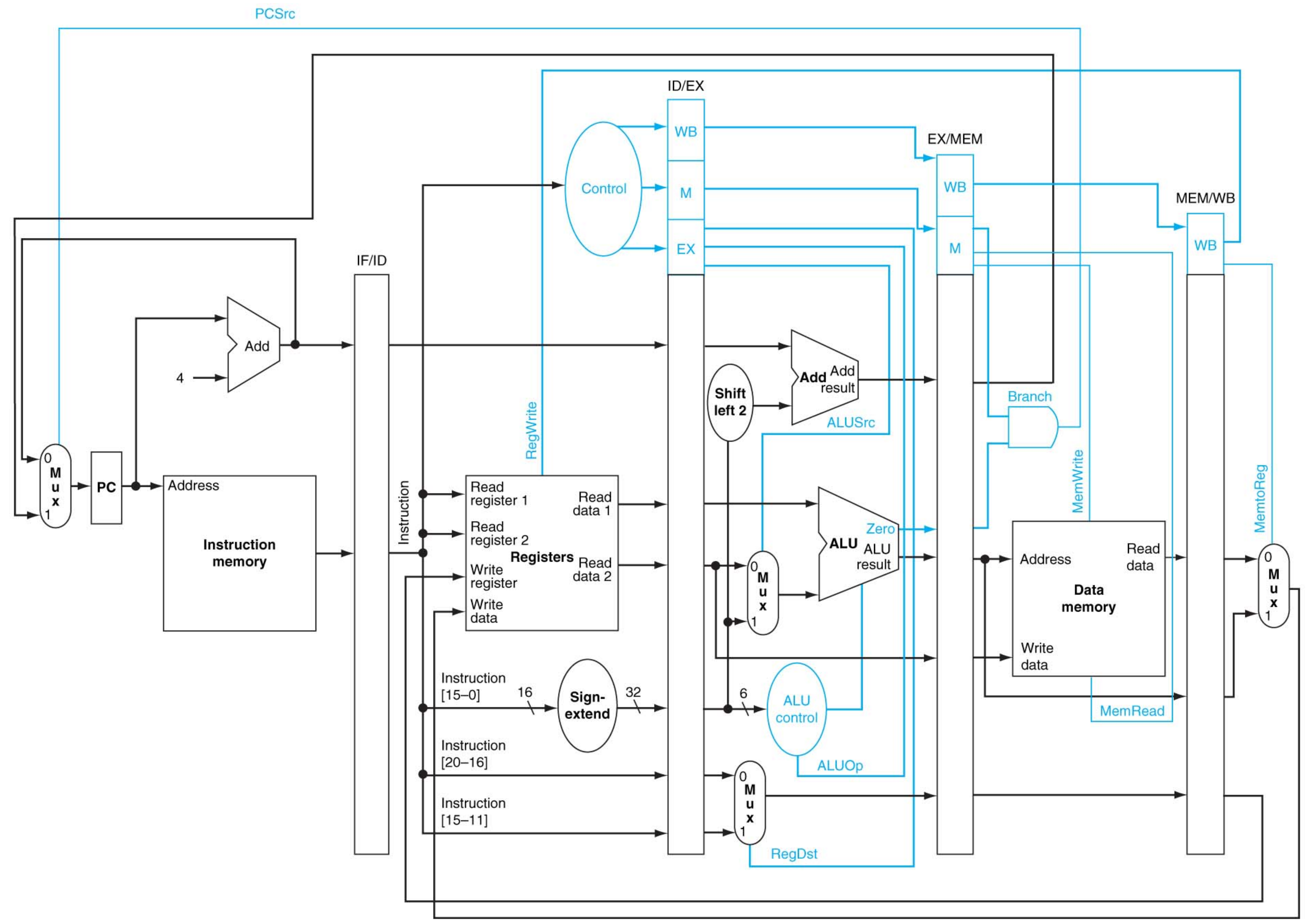
Pipeline Control

- FSM not really appropriate.
- Combinational logic!
    - signals generated once, but follow instruction through the pipeline

Pipeline Control



Pipeline with Control Logic



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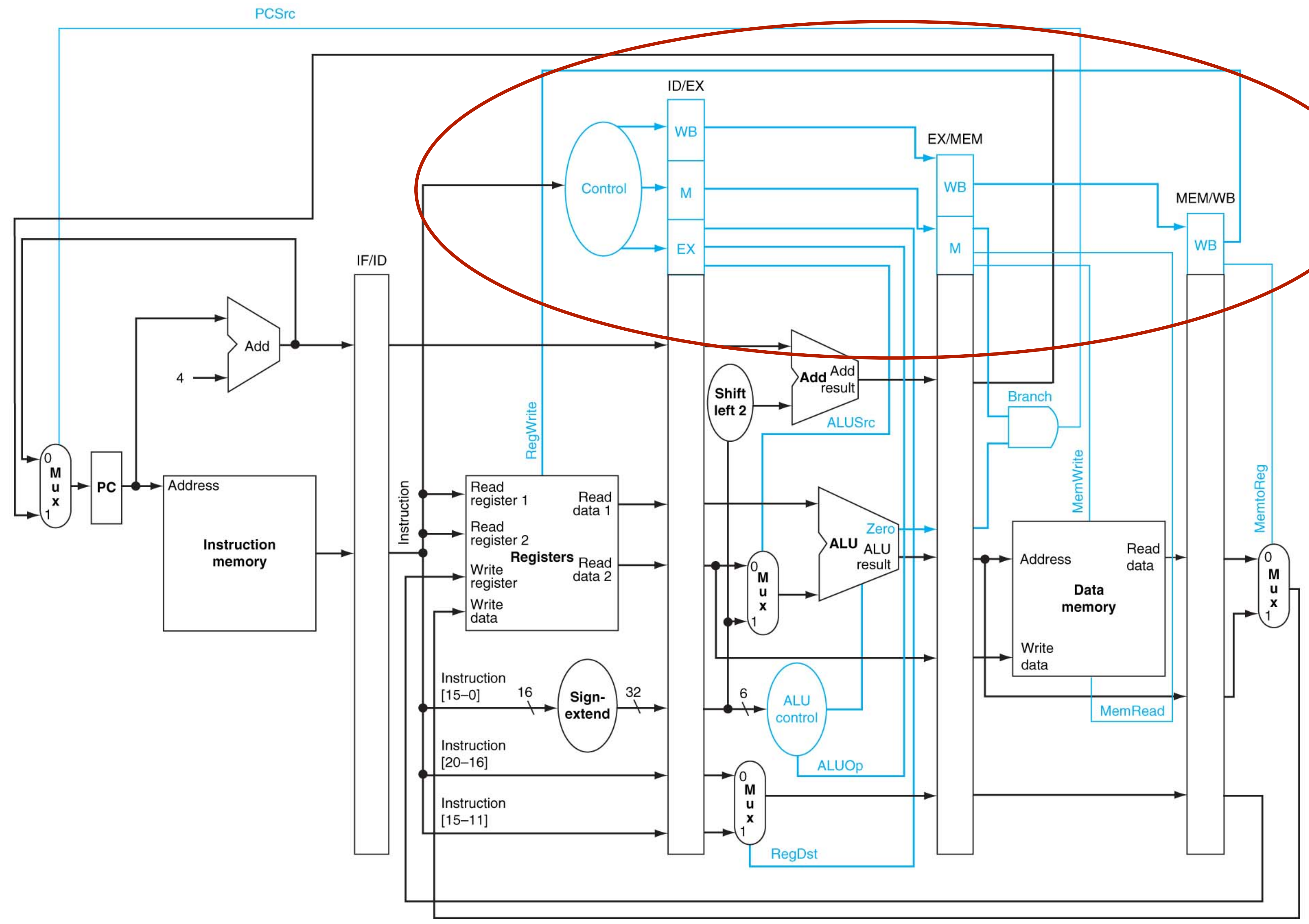

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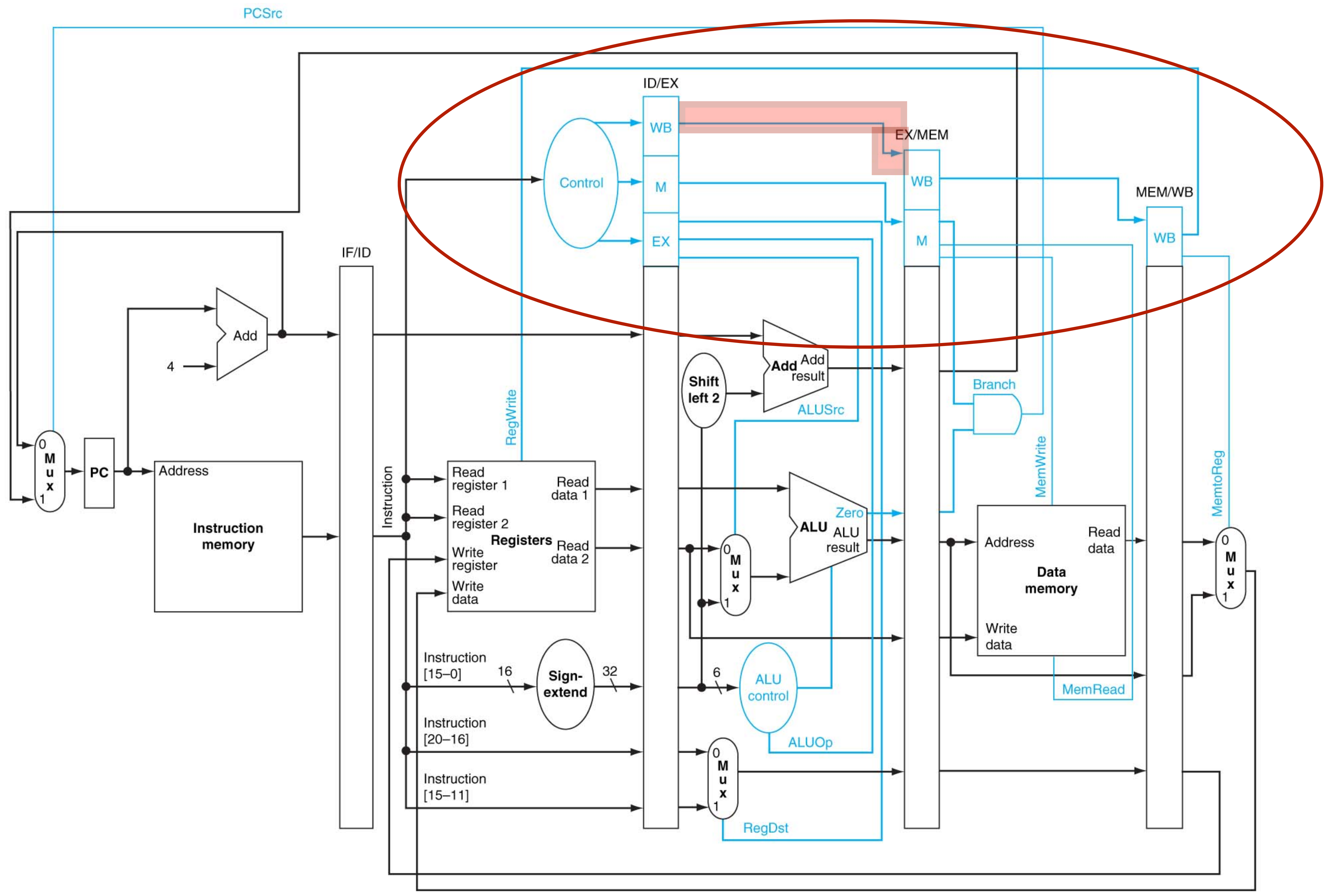

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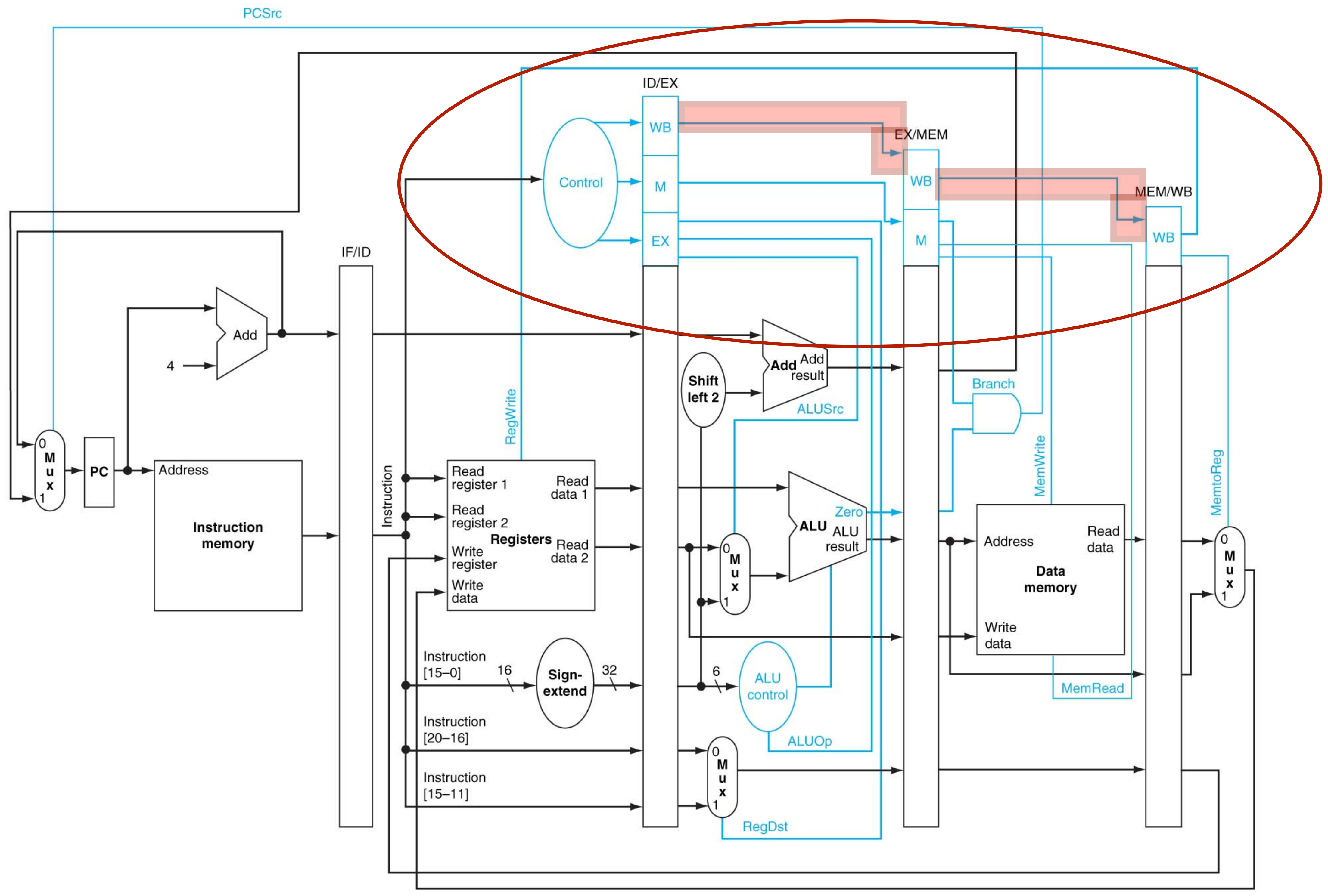

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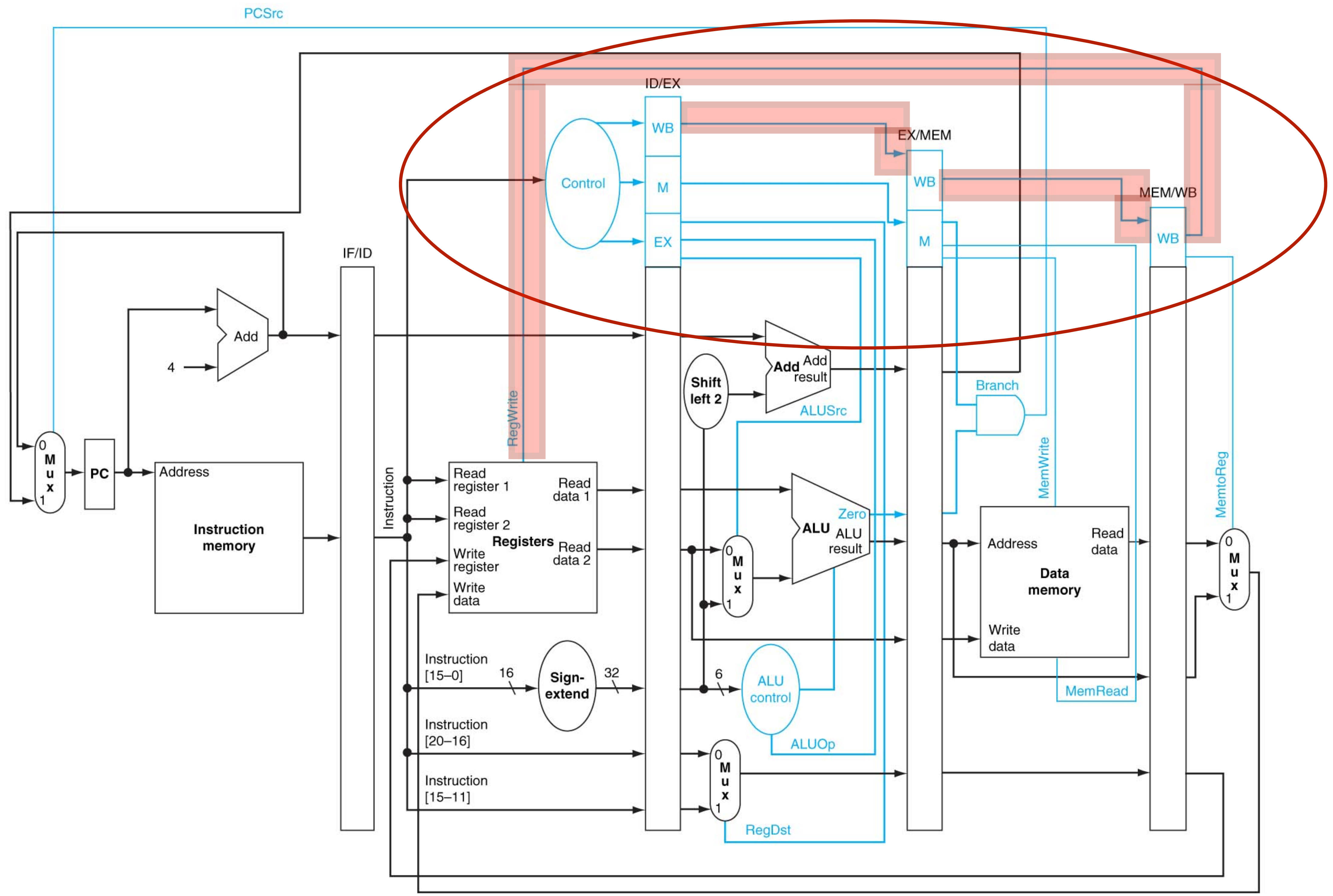
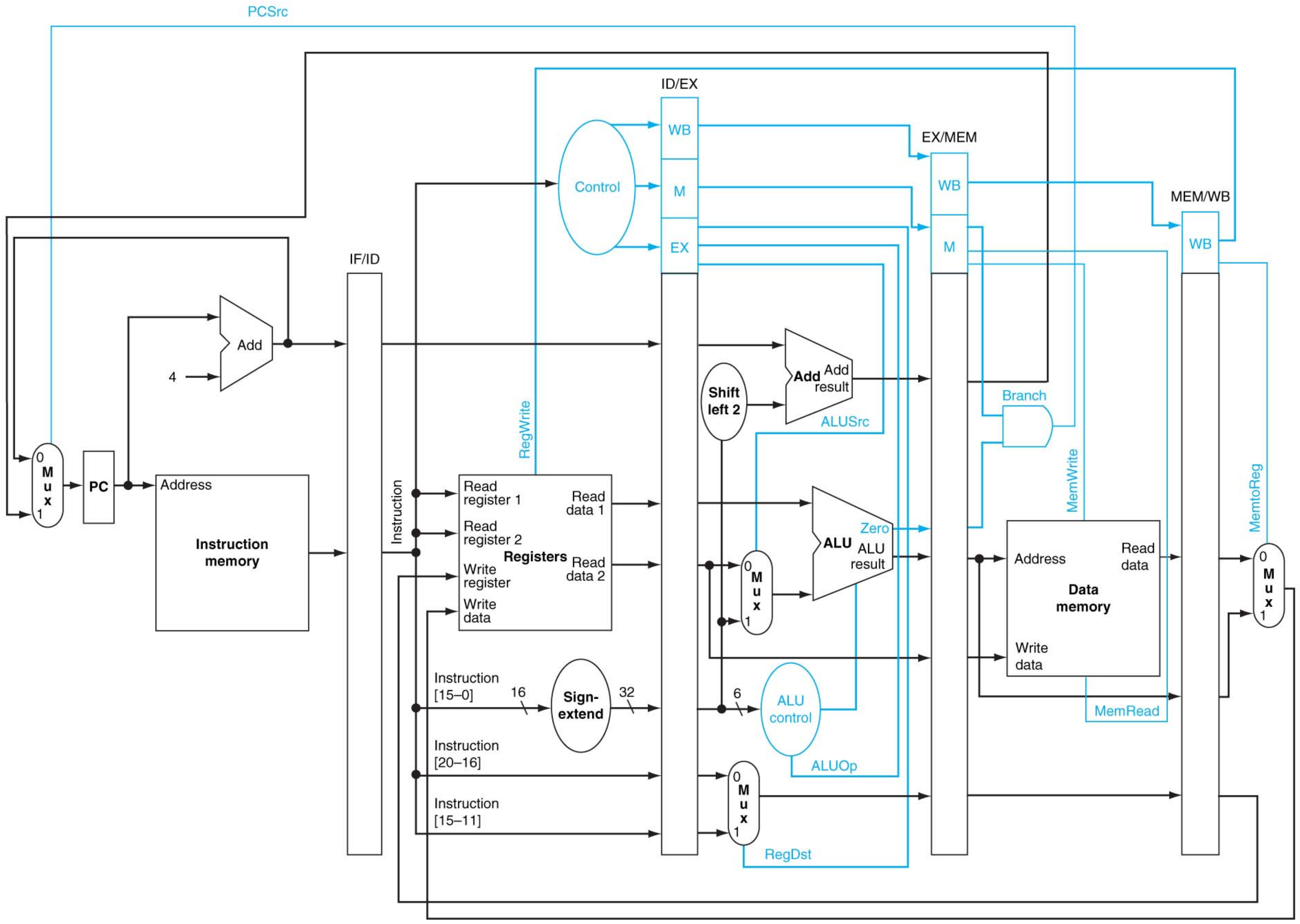


Pipeline Control Signals

	Execution Stage Control Lines				Memory Stage Control Lines			Write Back Stage Control Lines	
Instruction	RegDst	ALUOp1	ALUOp0	ALUSrc	Branch	MemRead	MemWrite	RegWrite	MemtoReg
R-Format	1	1	0	0	0	0	0	1	0
lw	0	0	0	1	0	1	0	1	1
sw	x	0	0	1	0	0	1	0	x
beq	x	0	1	0	1	0	0	0	x

Guess the Signal



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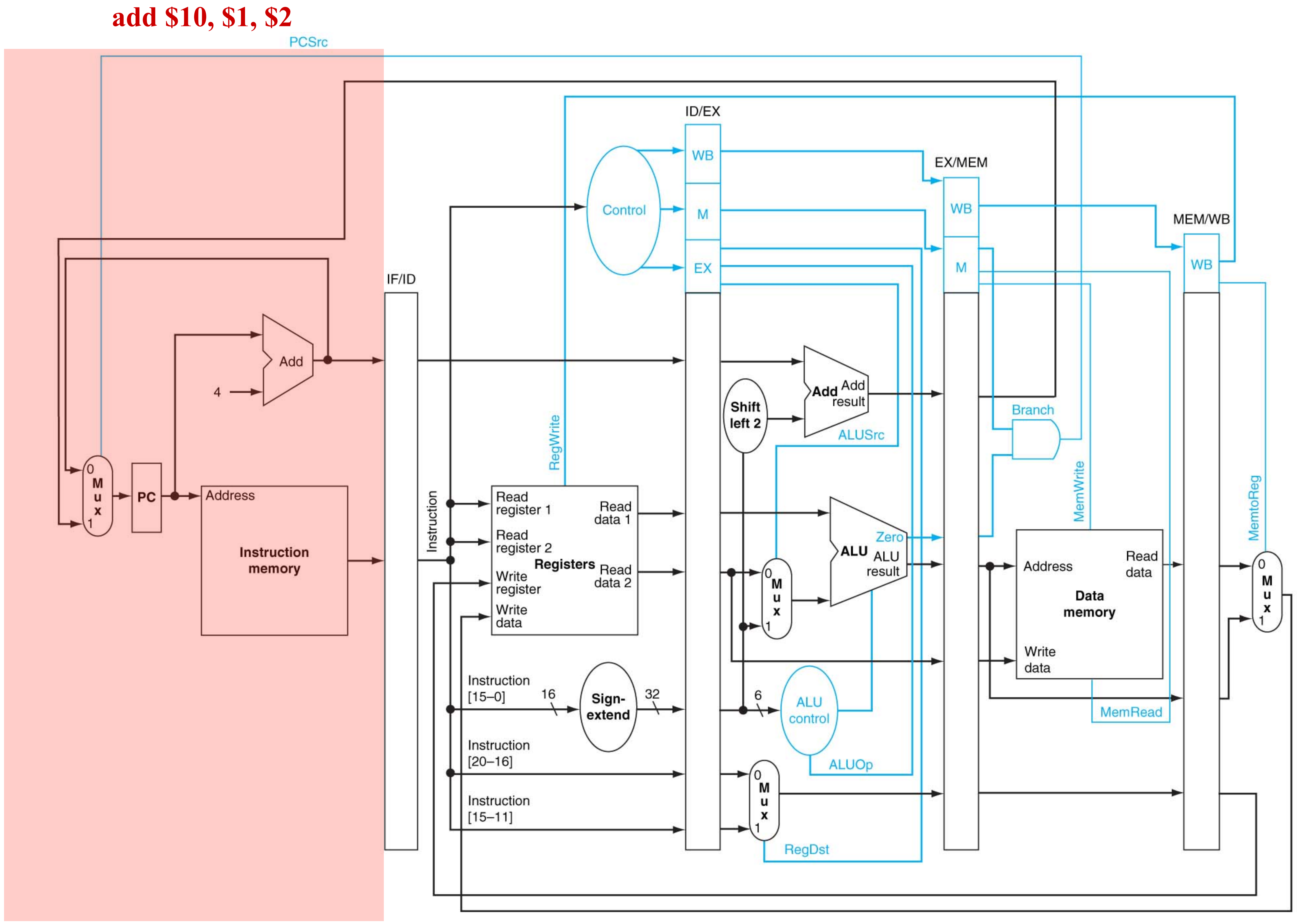

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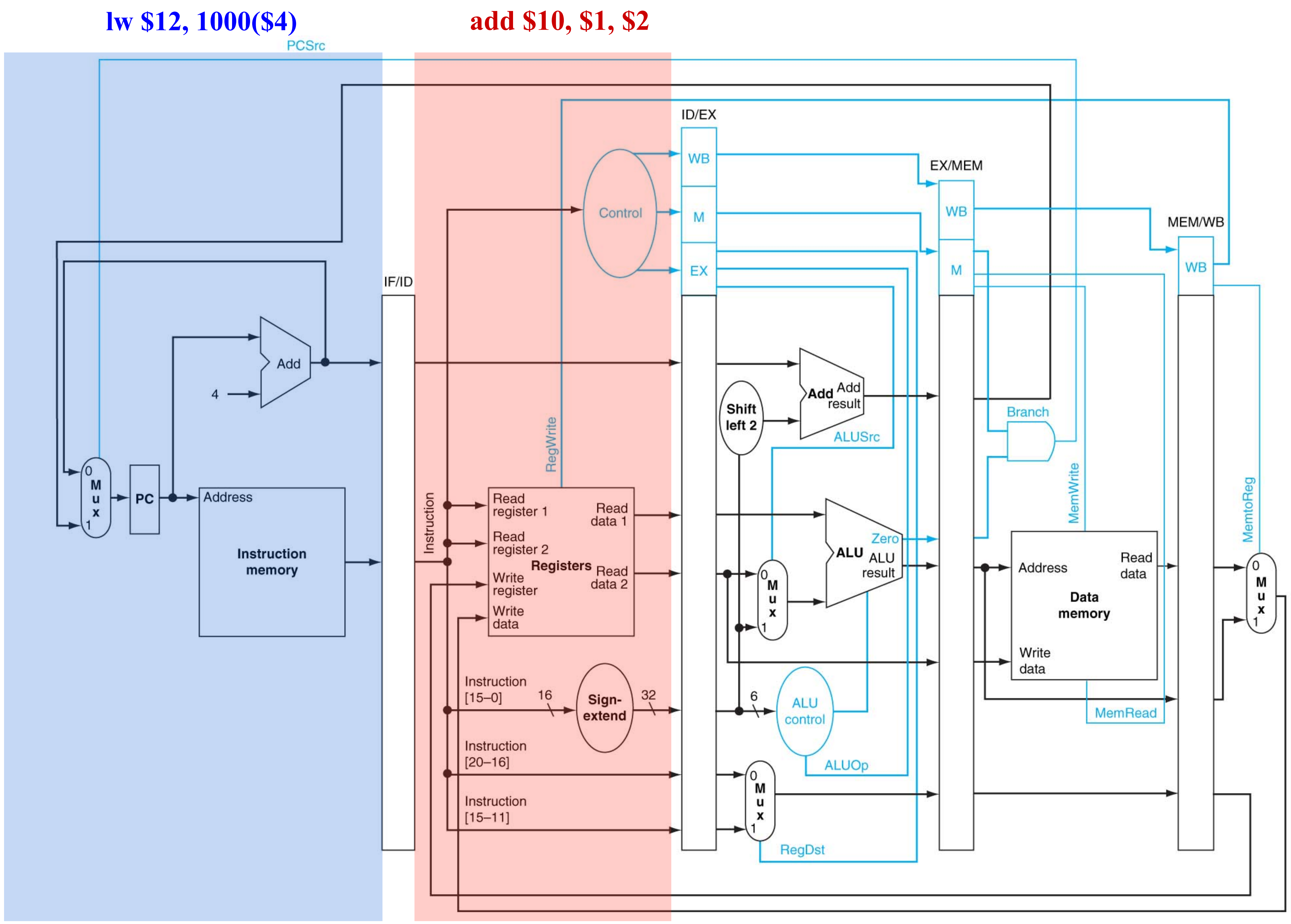

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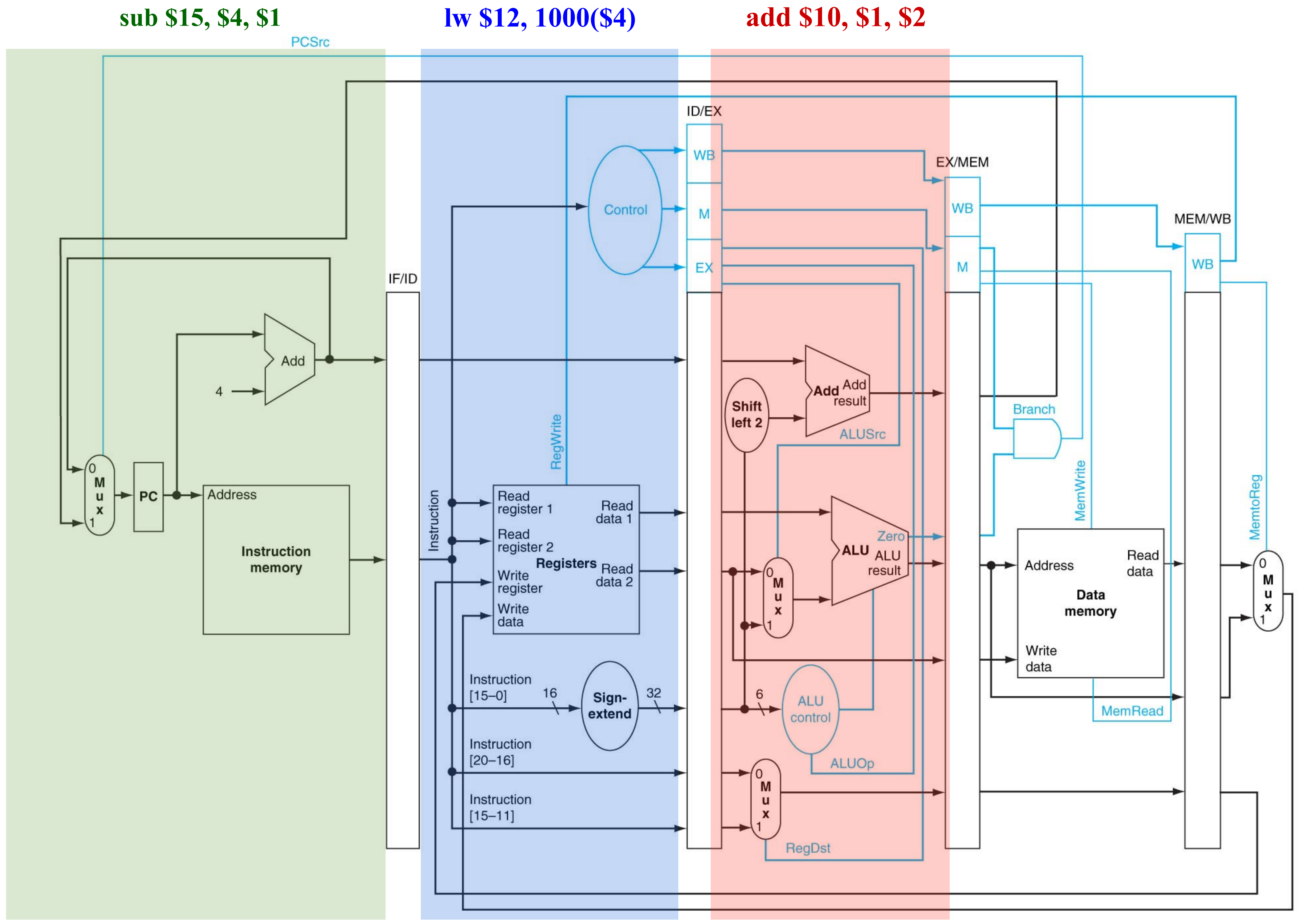

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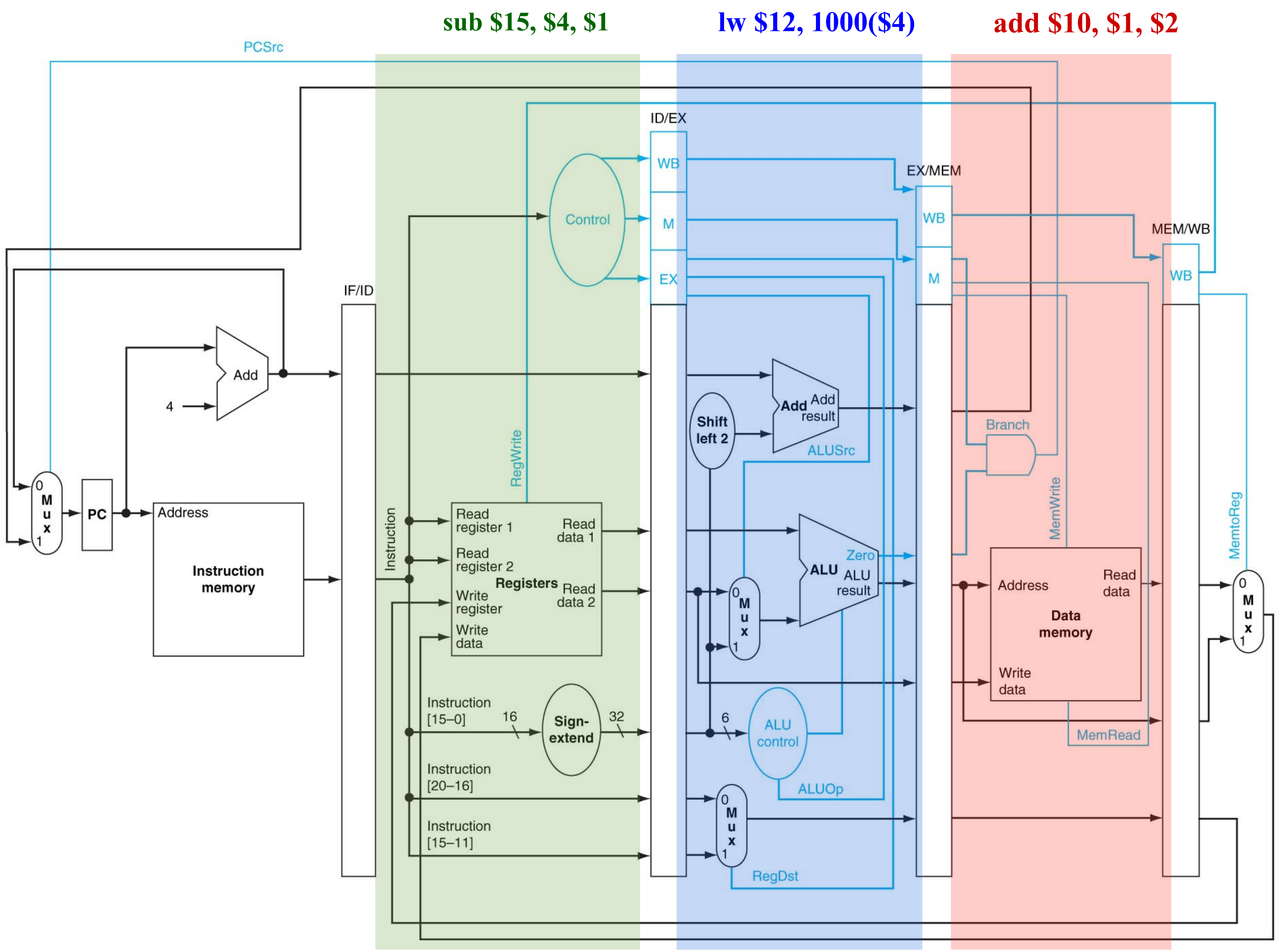

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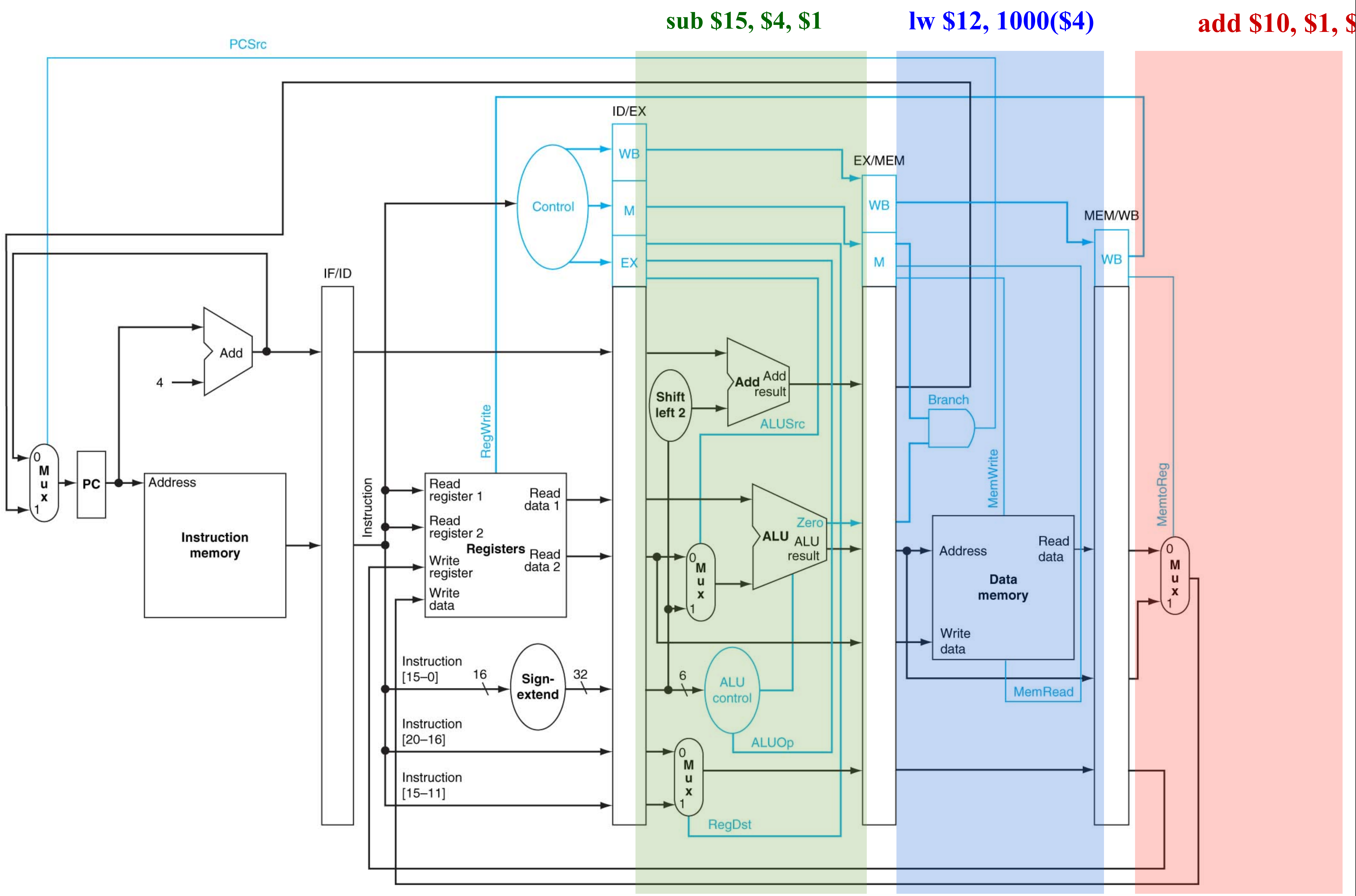

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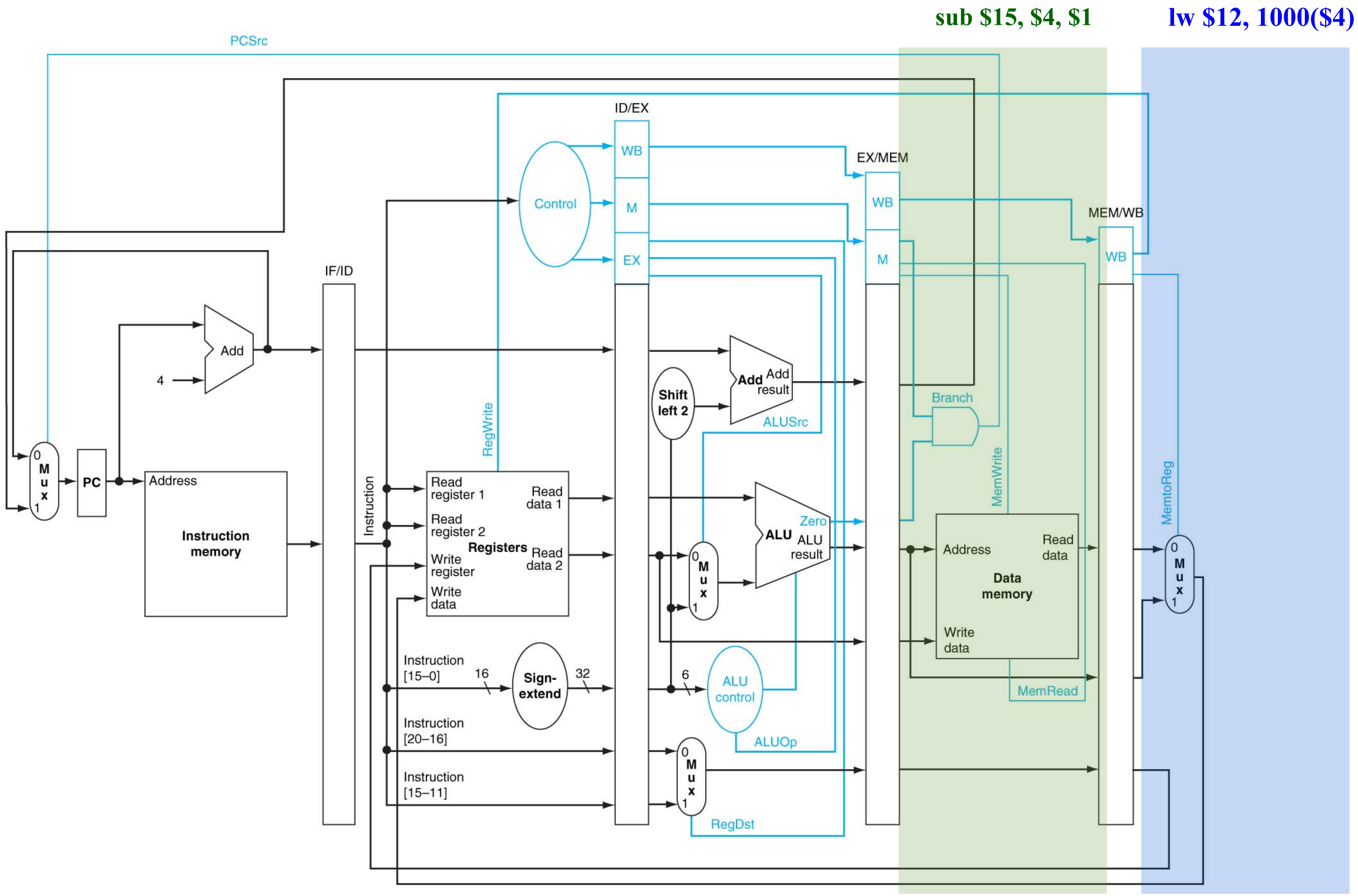
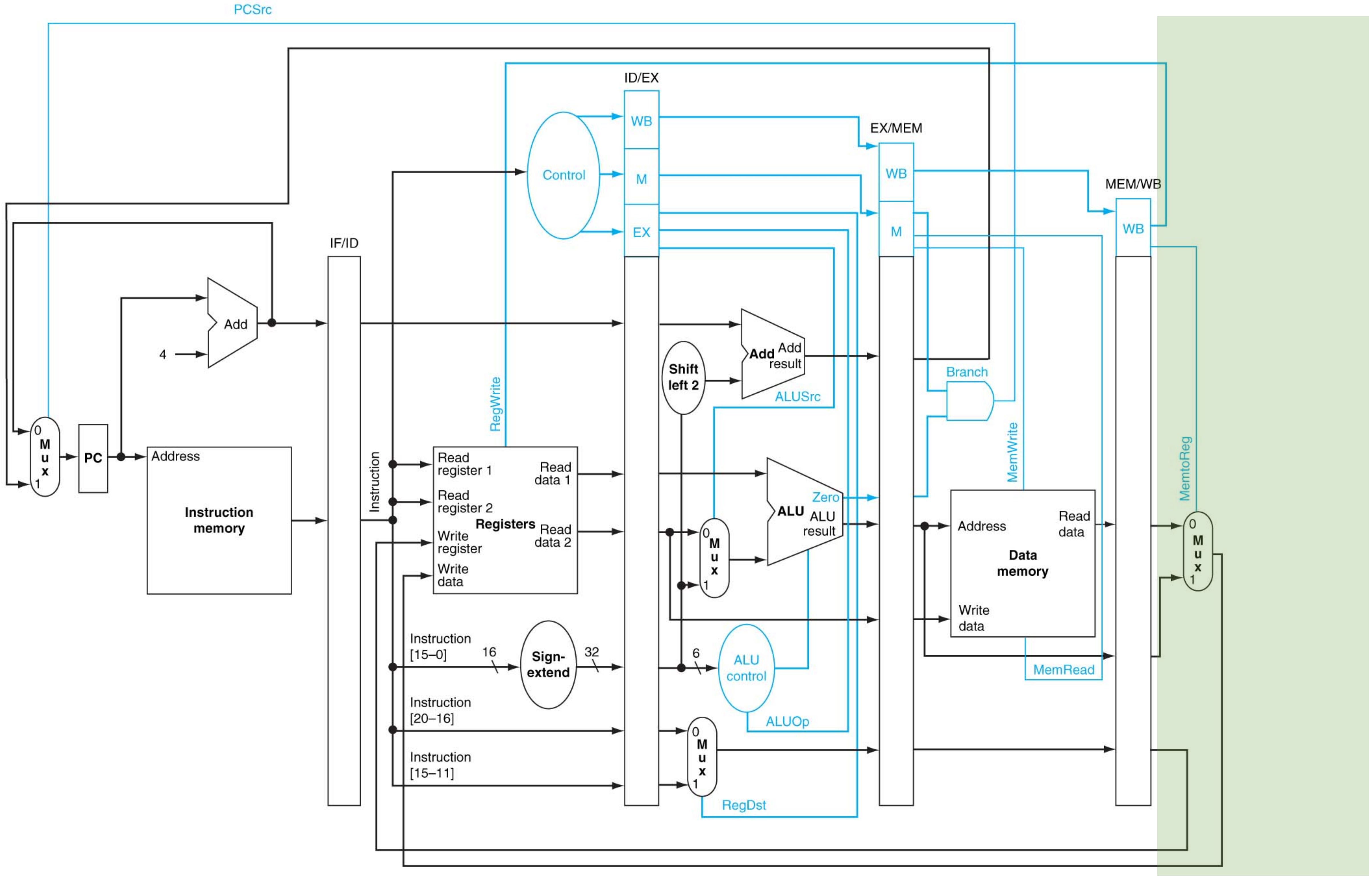


Guess the Signal

sub $15, $4, $1



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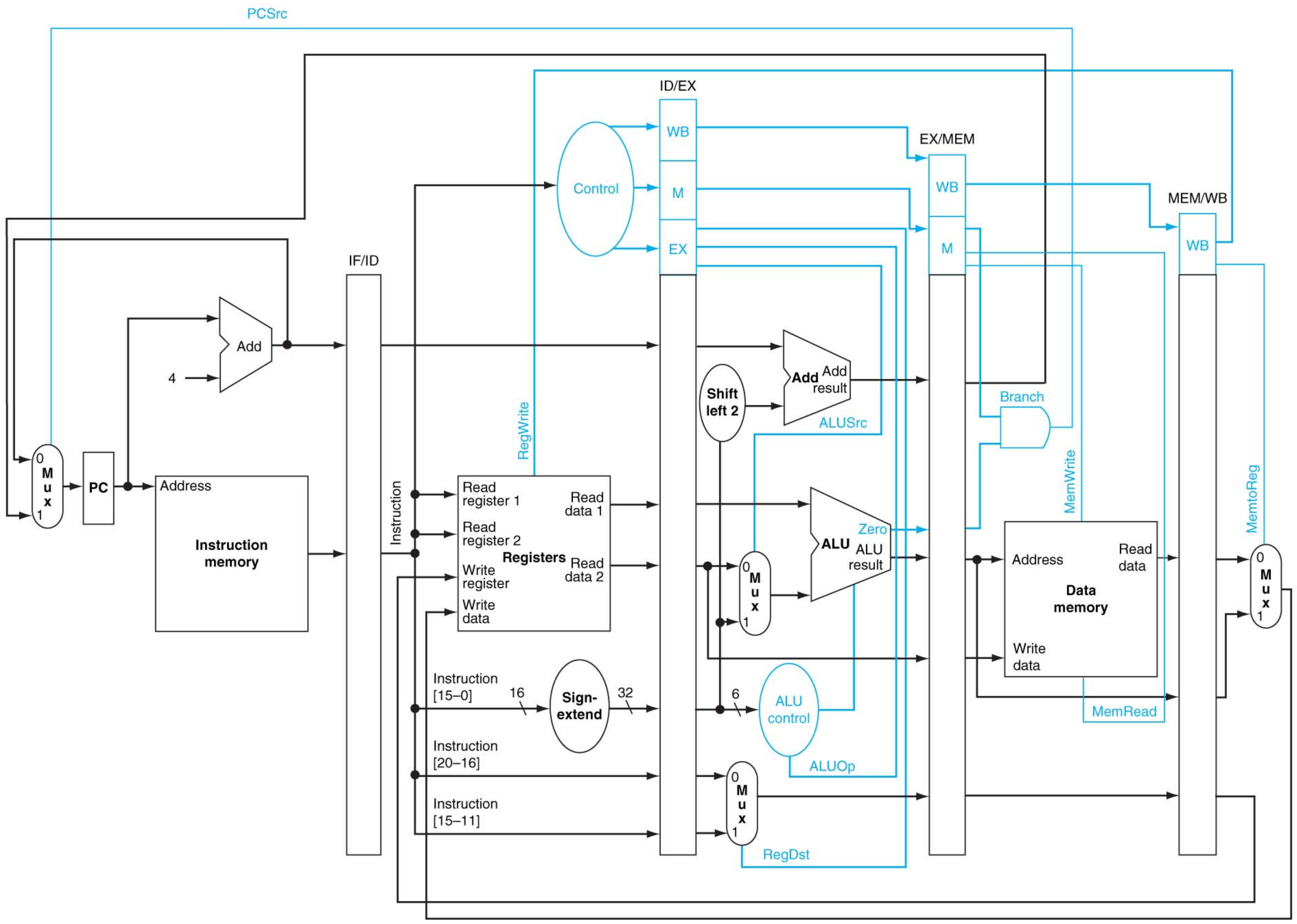
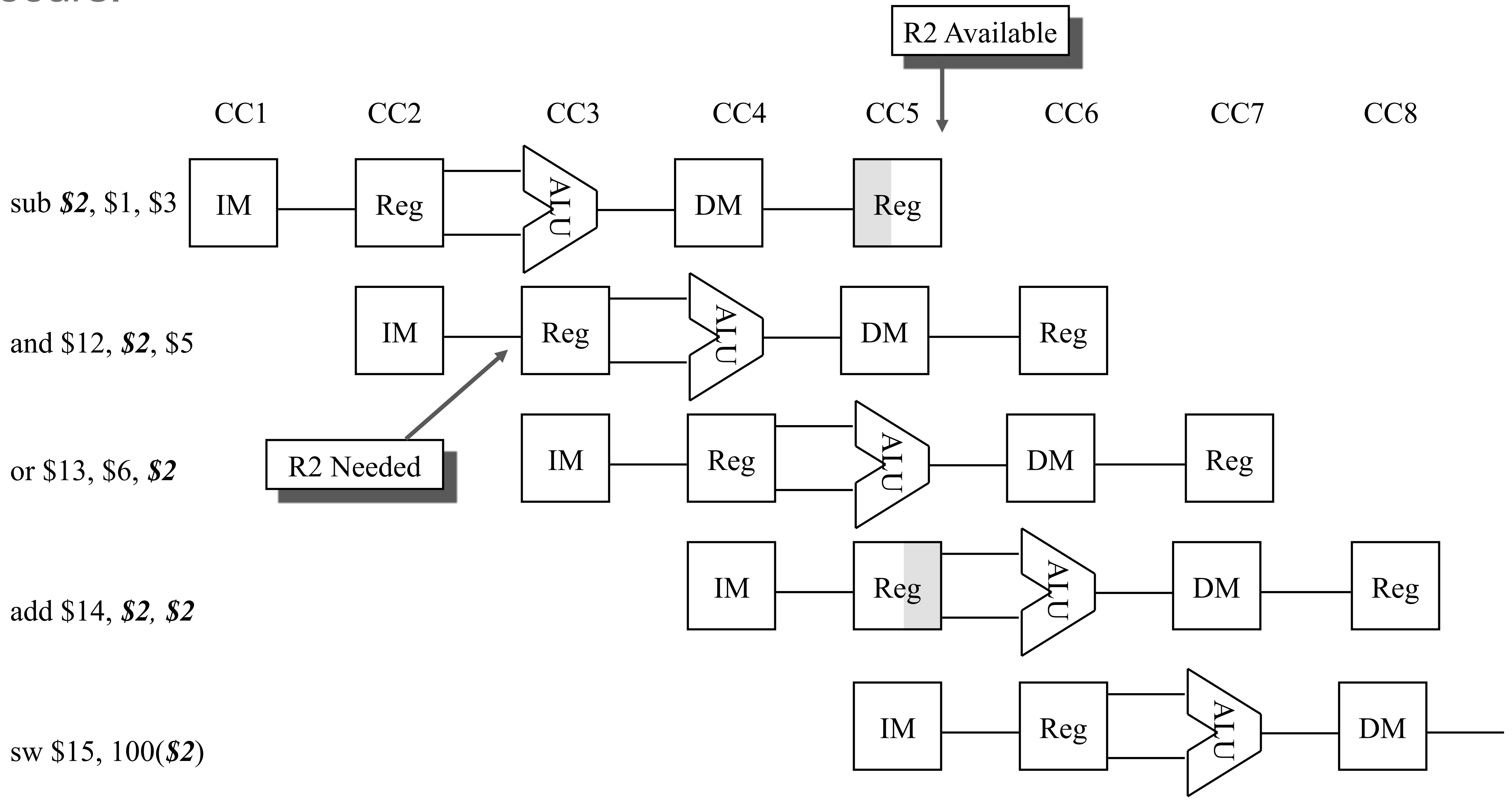


Data Hazards

- When a result is needed in the pipeline before it is available, a “data hazard” occurs.



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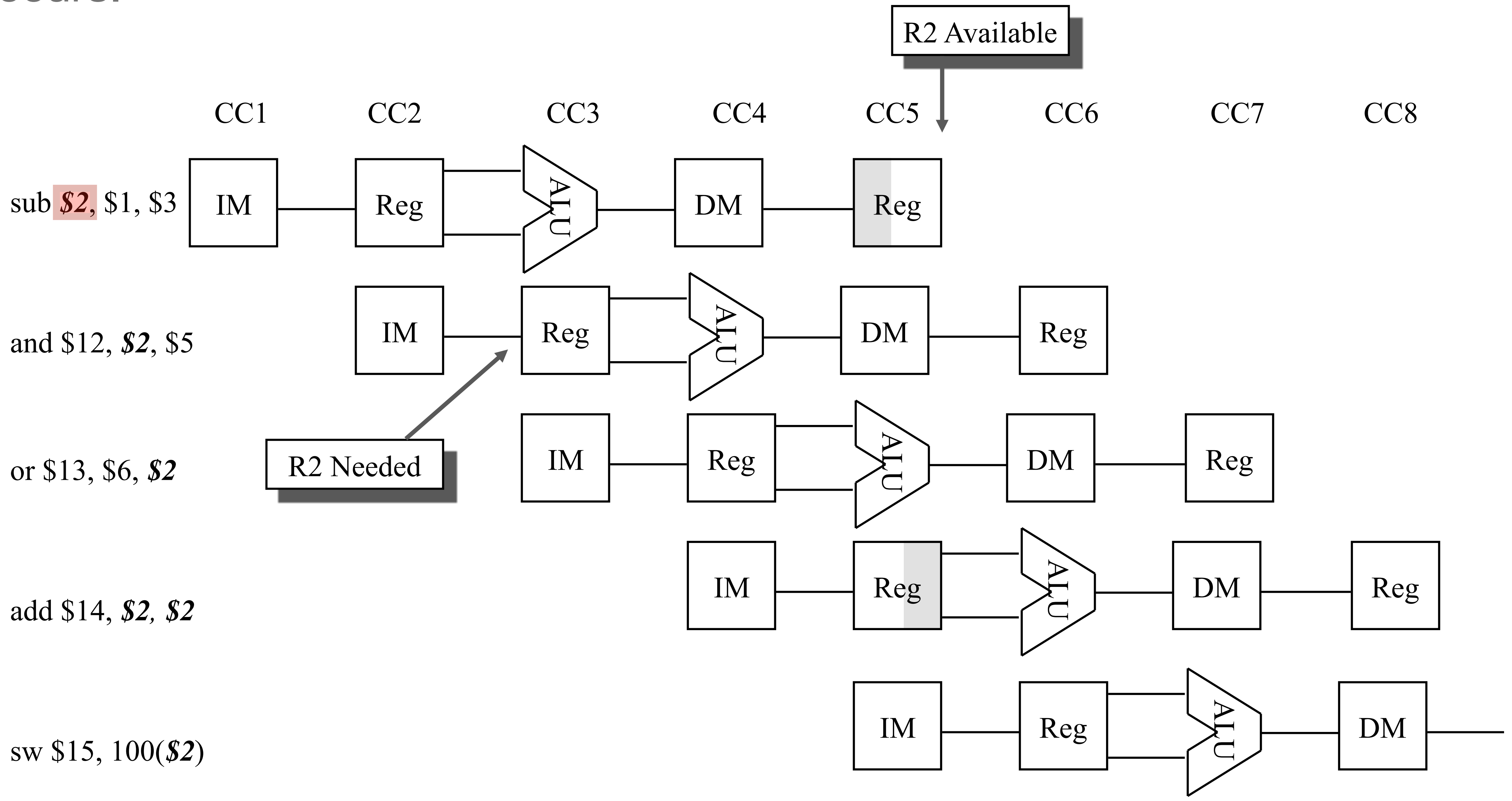

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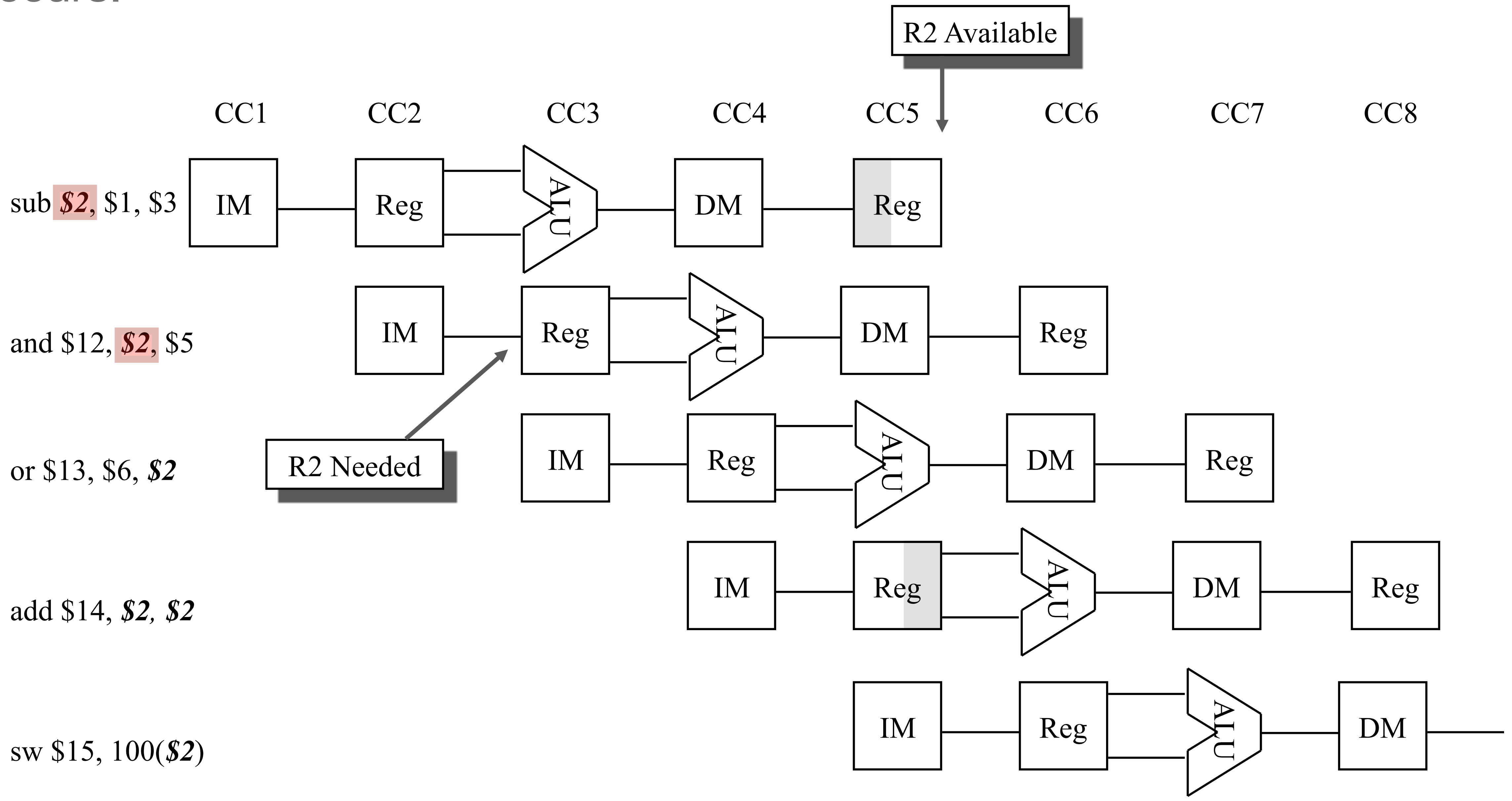

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- Pipelining creates potential hazards.