

# Systems and Networking I

Applied Computer Science and Artificial Intelligence  
2023-2024

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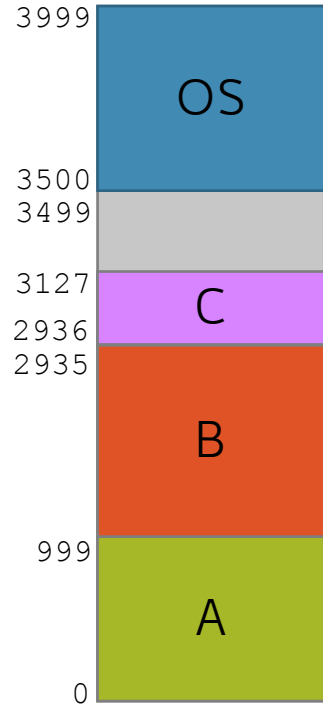
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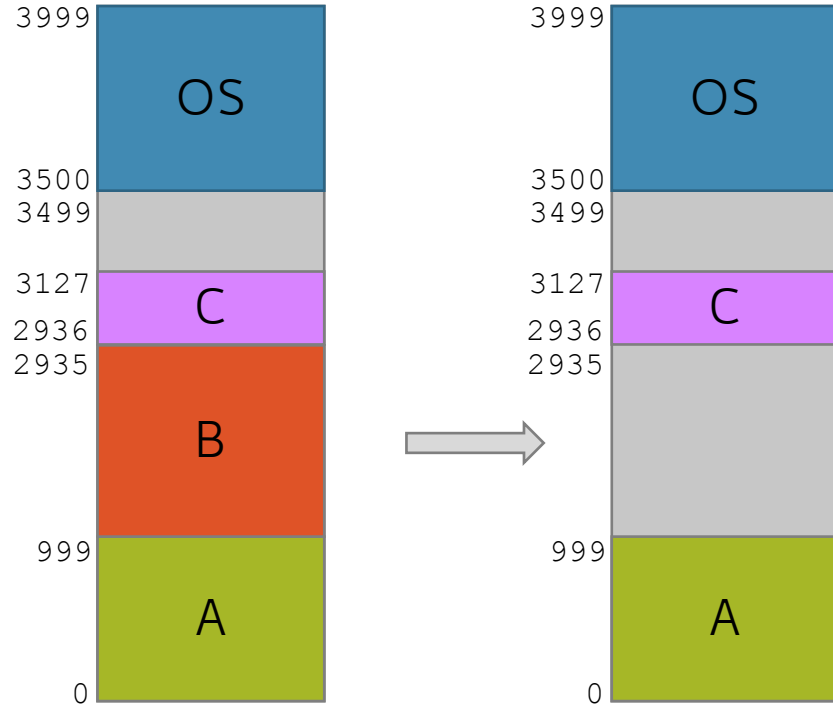
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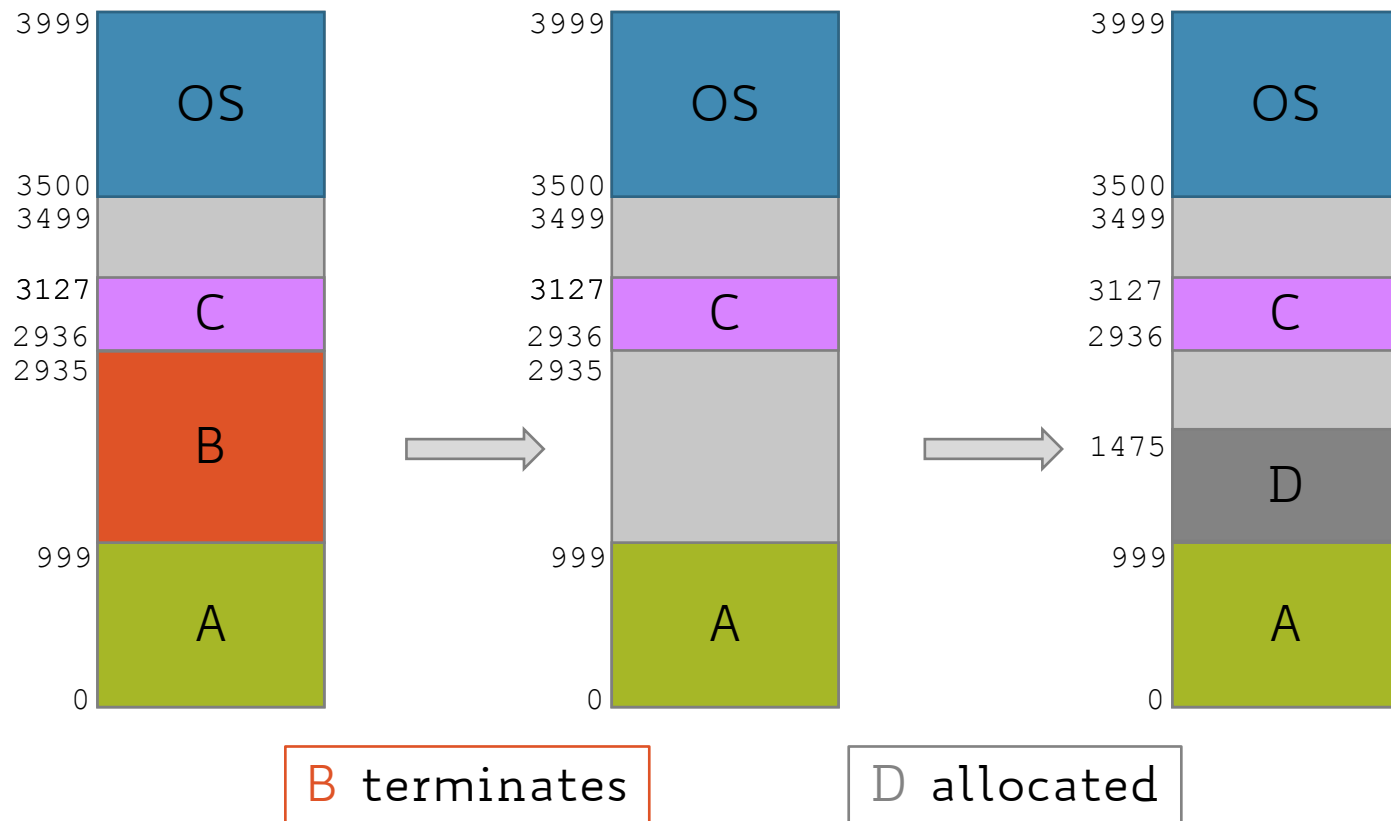
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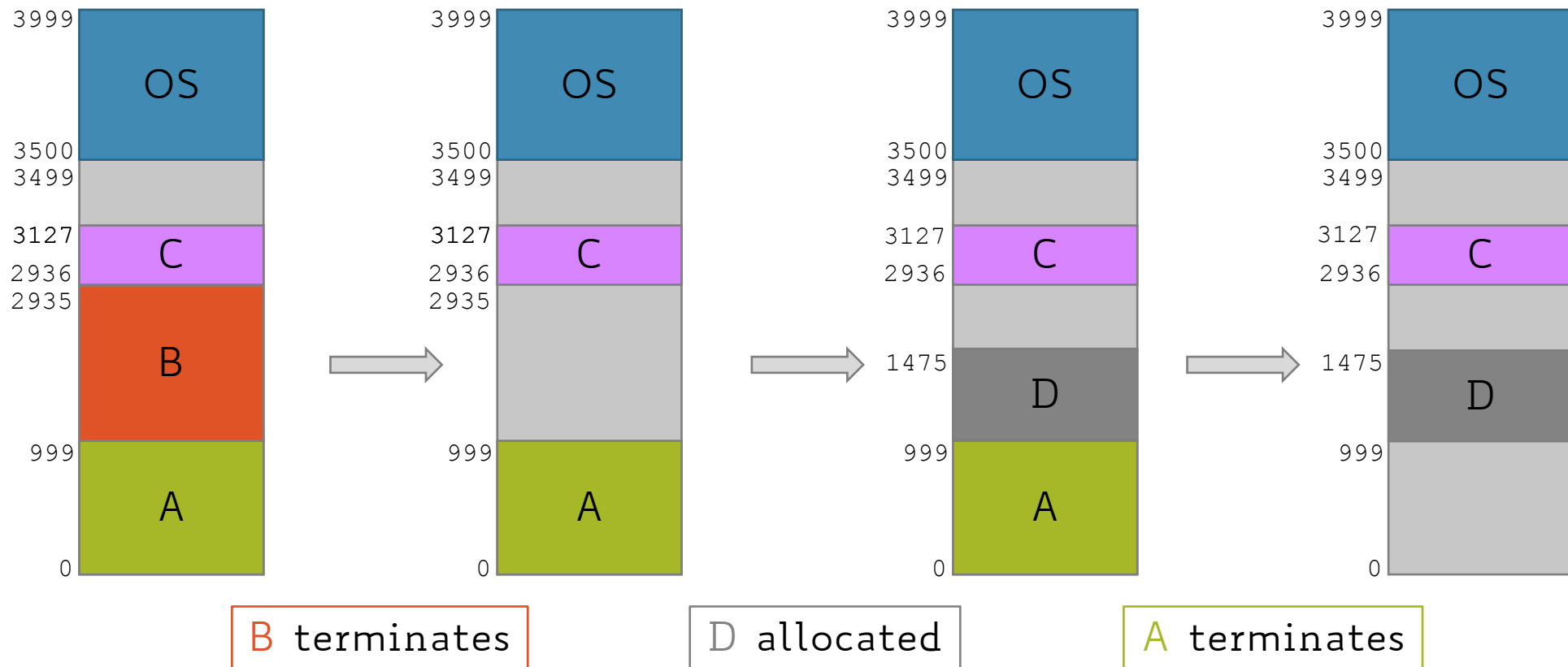
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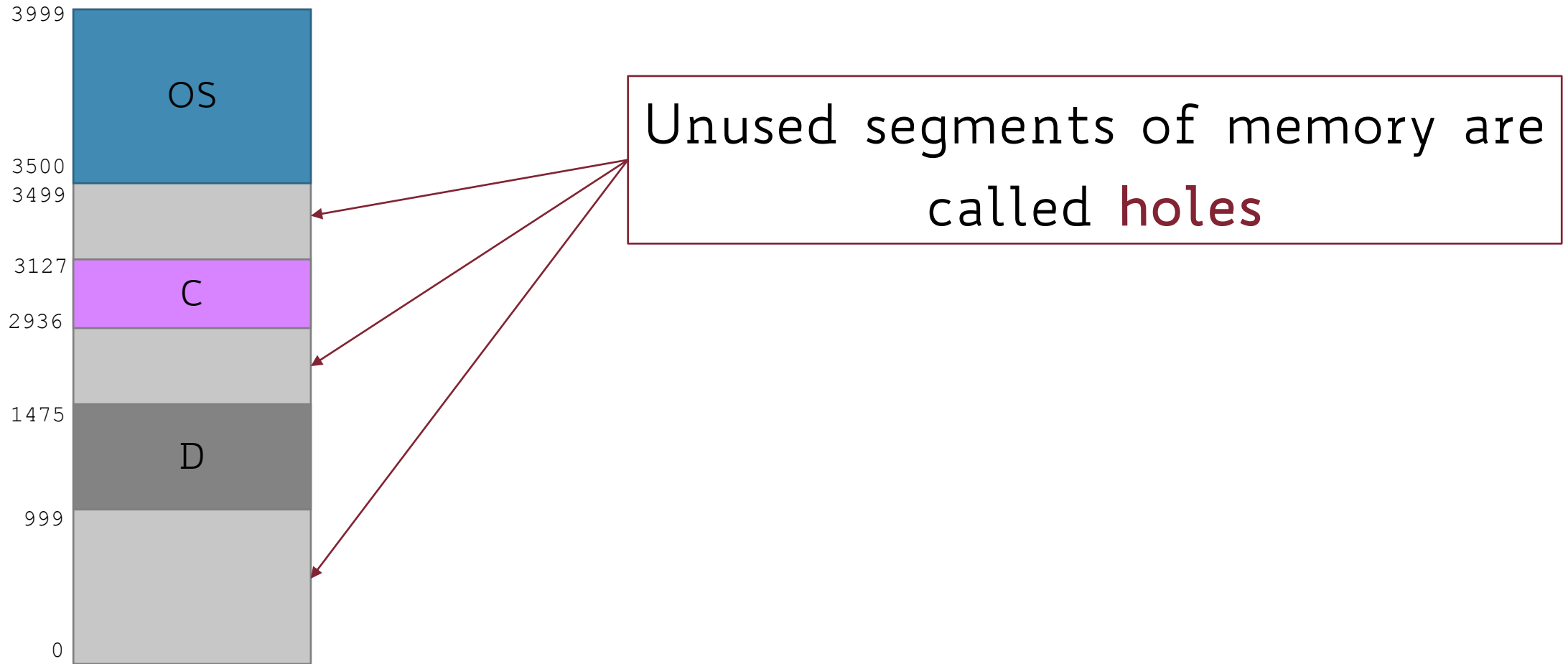


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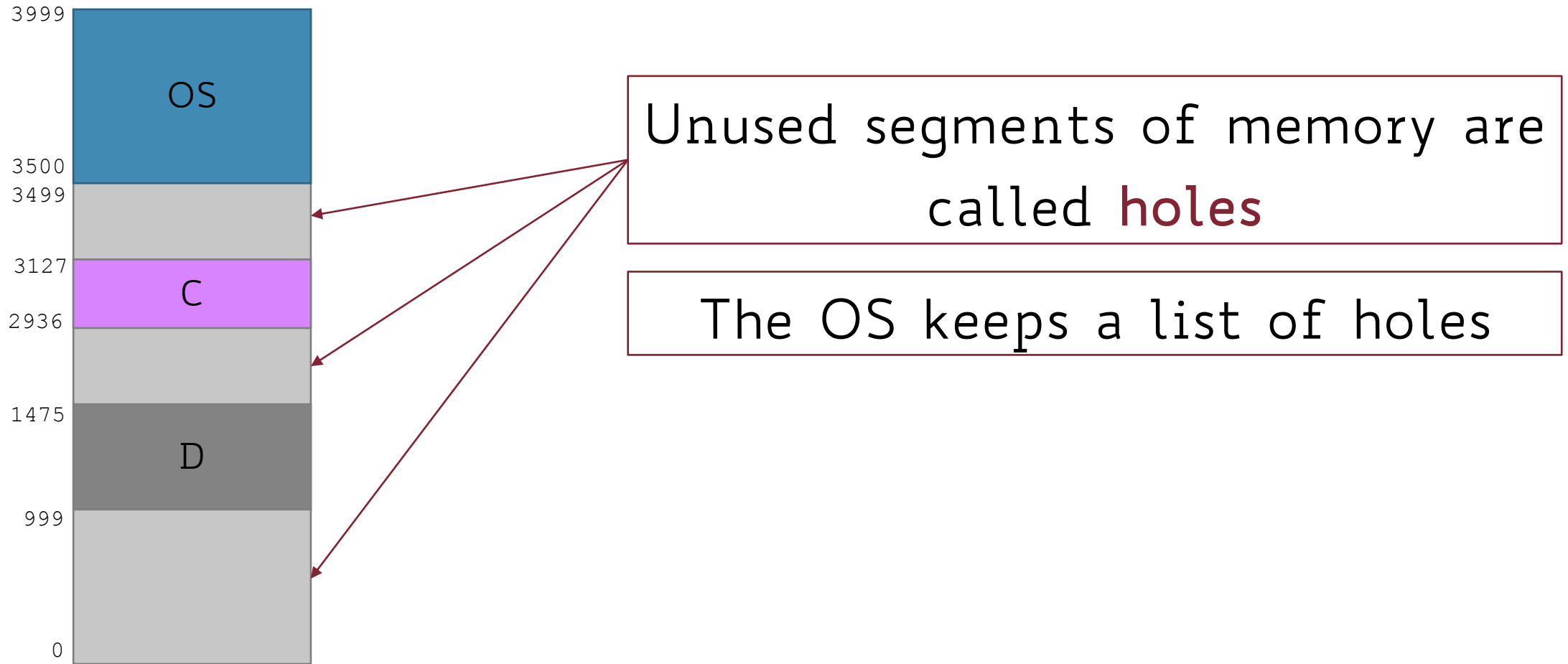
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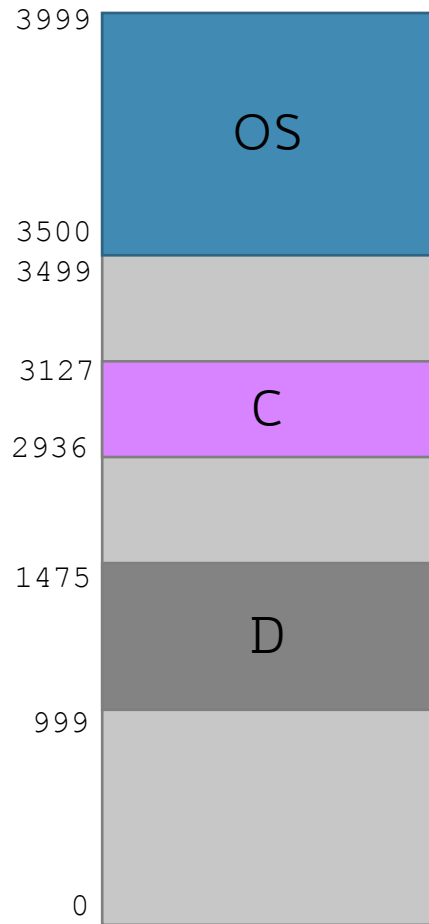
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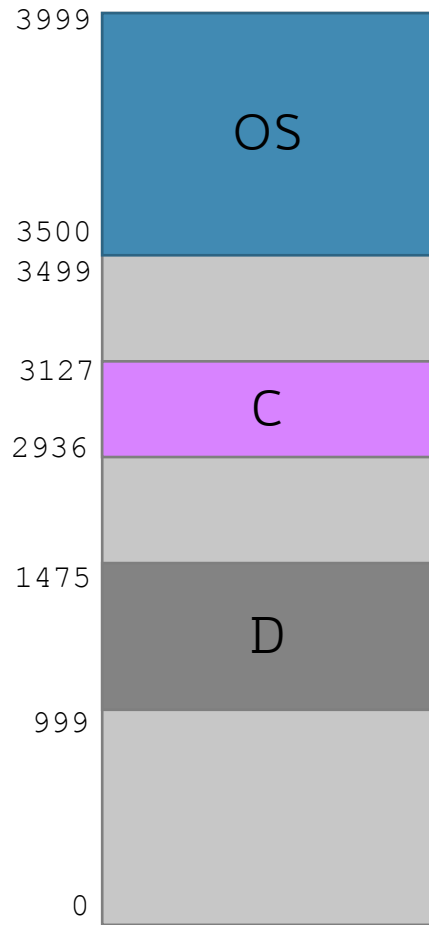


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**How?**

# Memory Allocation Policies: First-Fit

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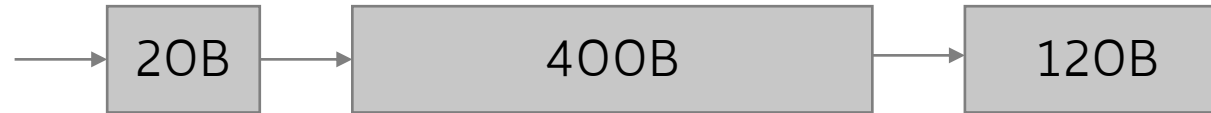
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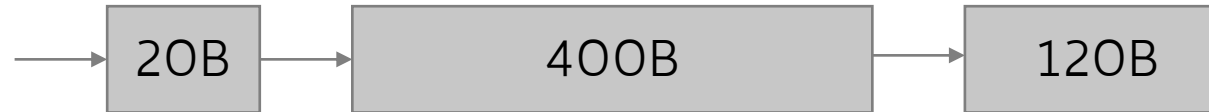
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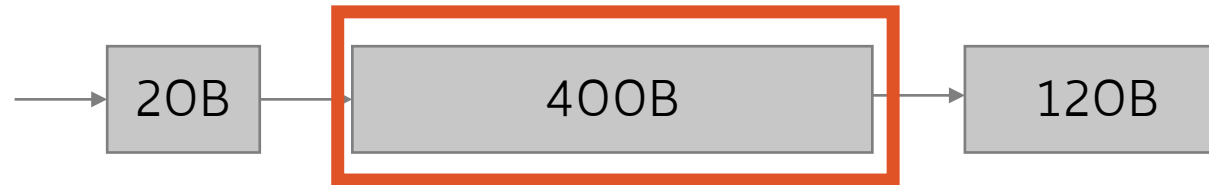
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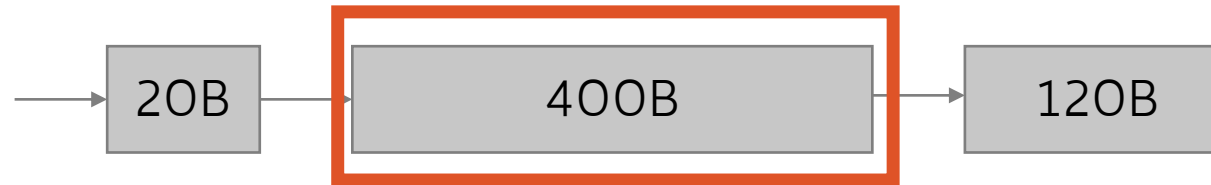
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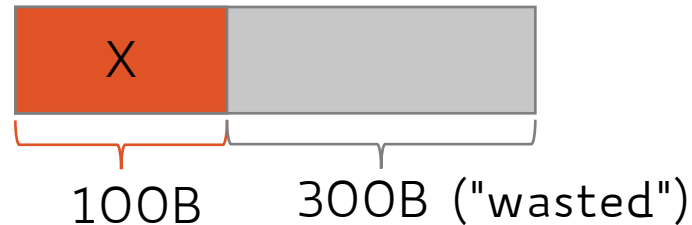
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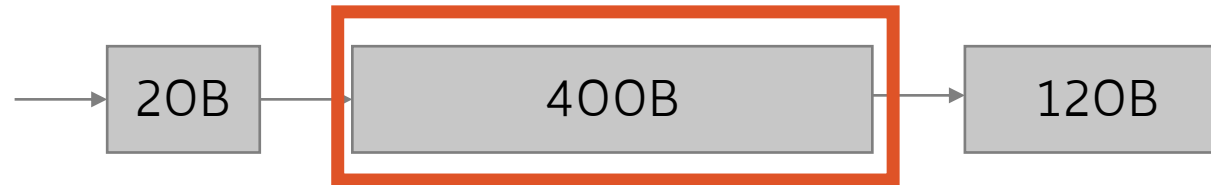


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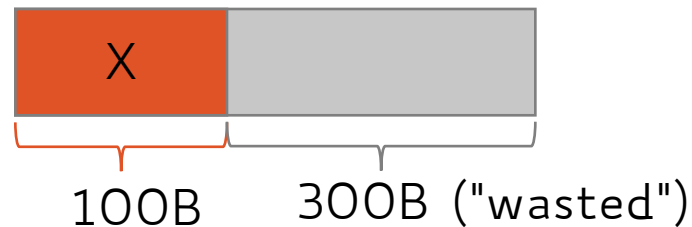


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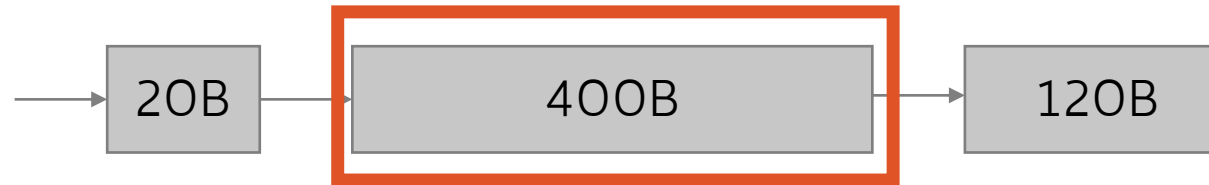
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We will not be able to satisfy this request even if theoretically we could



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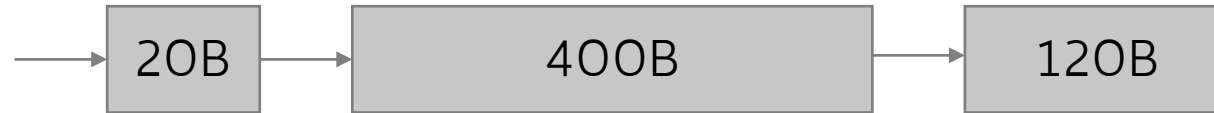
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Binary Search Tree (BST)

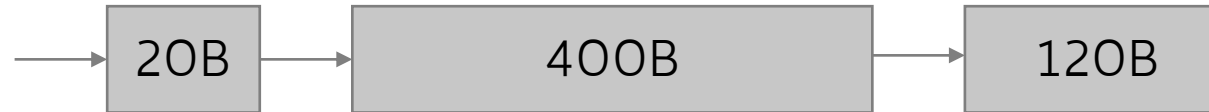
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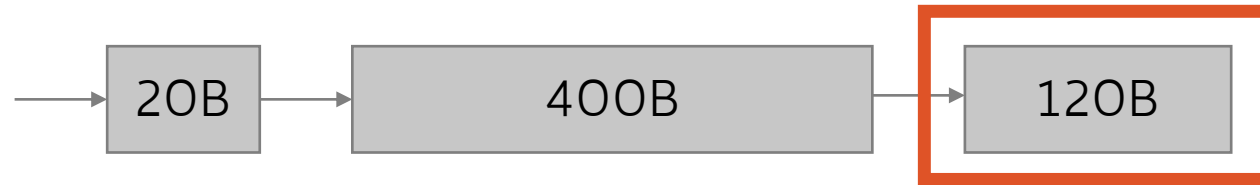


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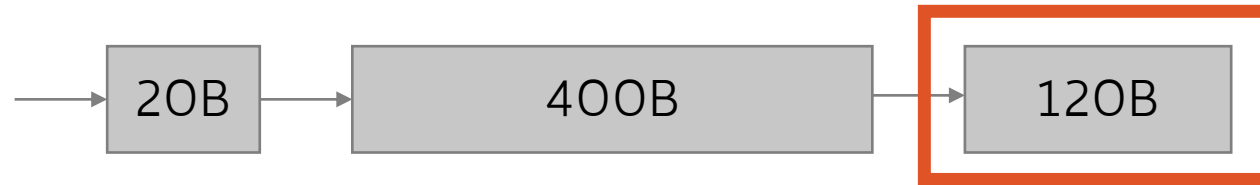
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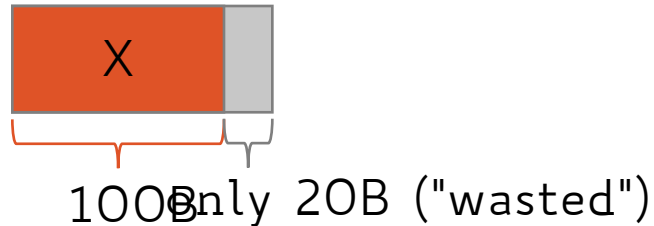
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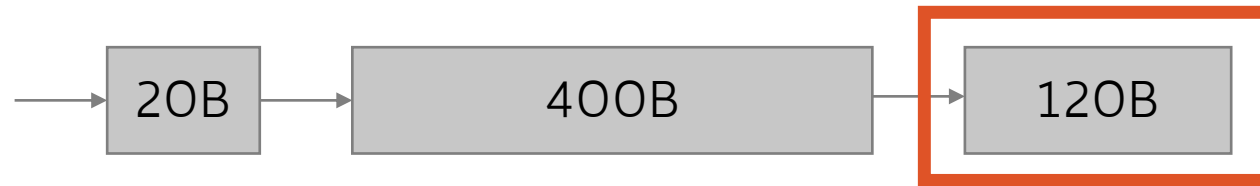


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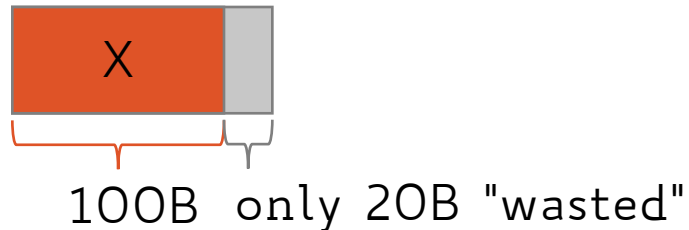


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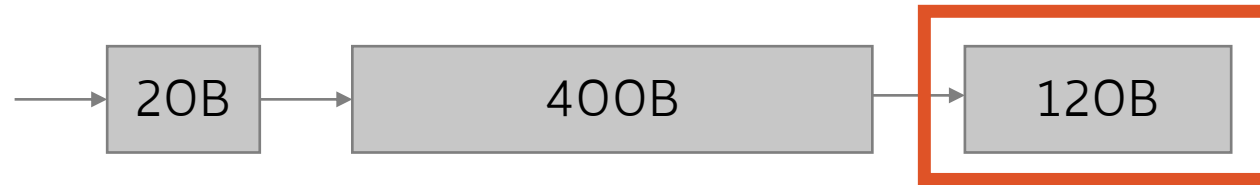
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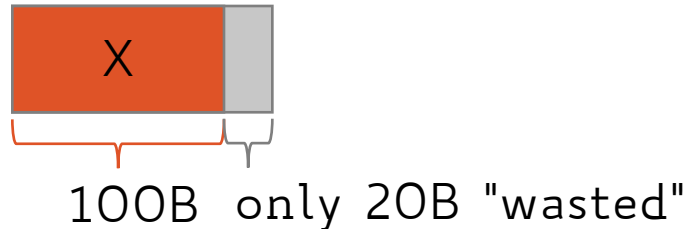
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We can now assign it the second available hole segment (400B)

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```
graph TD; A[Problem] --> B[External Fragmentation]; A --> C[Internal Fragmentation];
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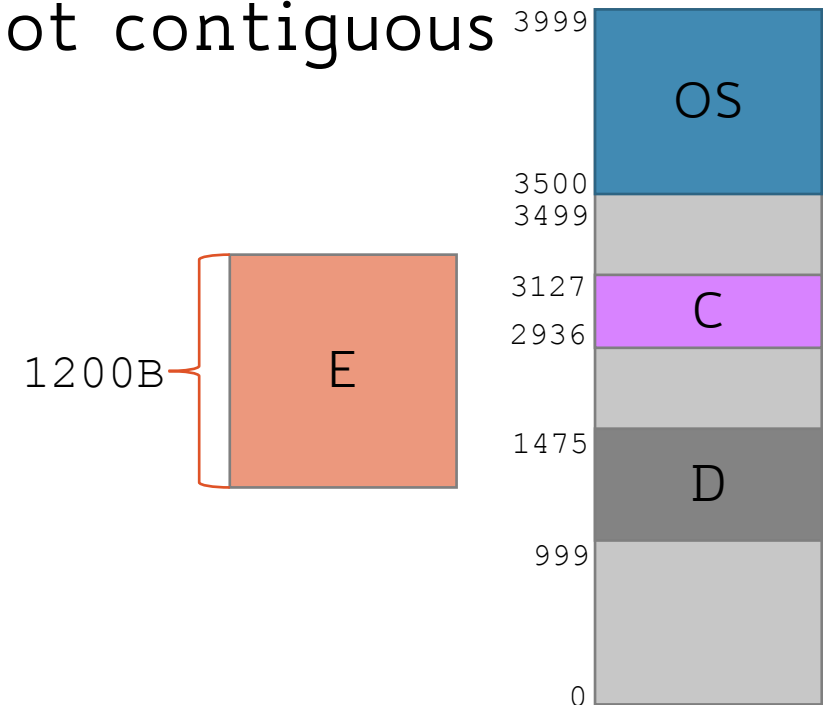
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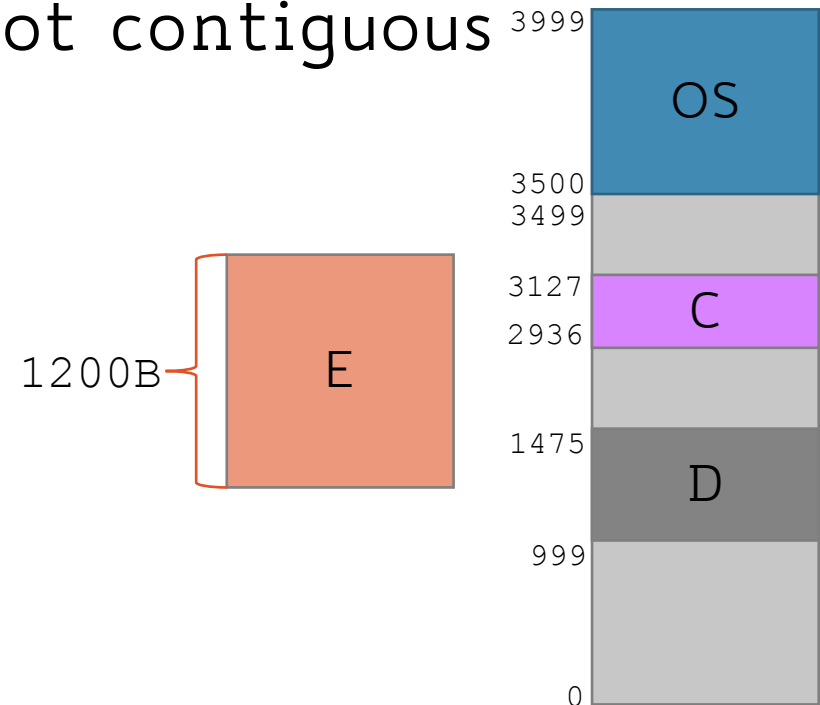


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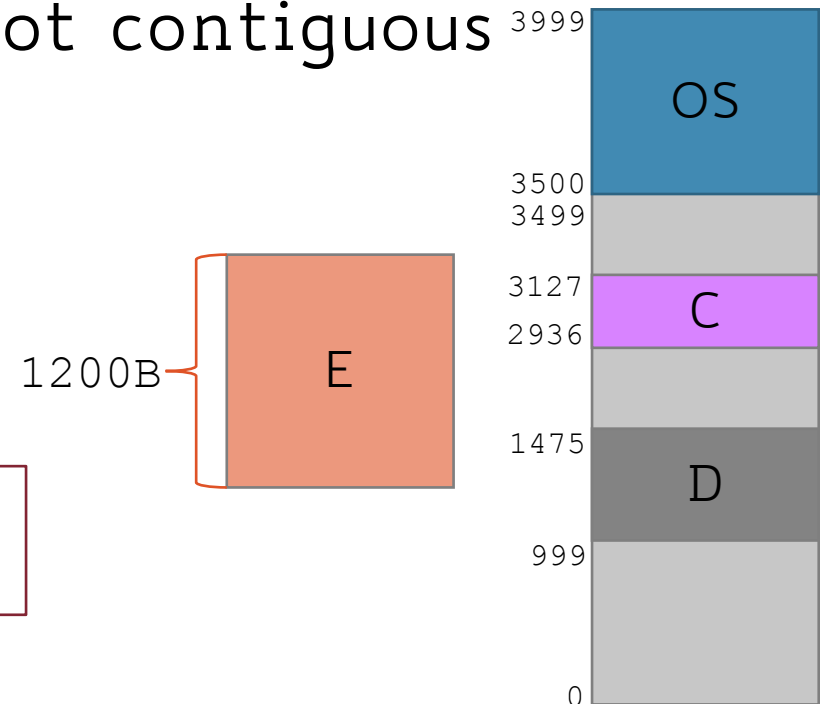
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Goal:

Allocation policy that minimizes wasted space!





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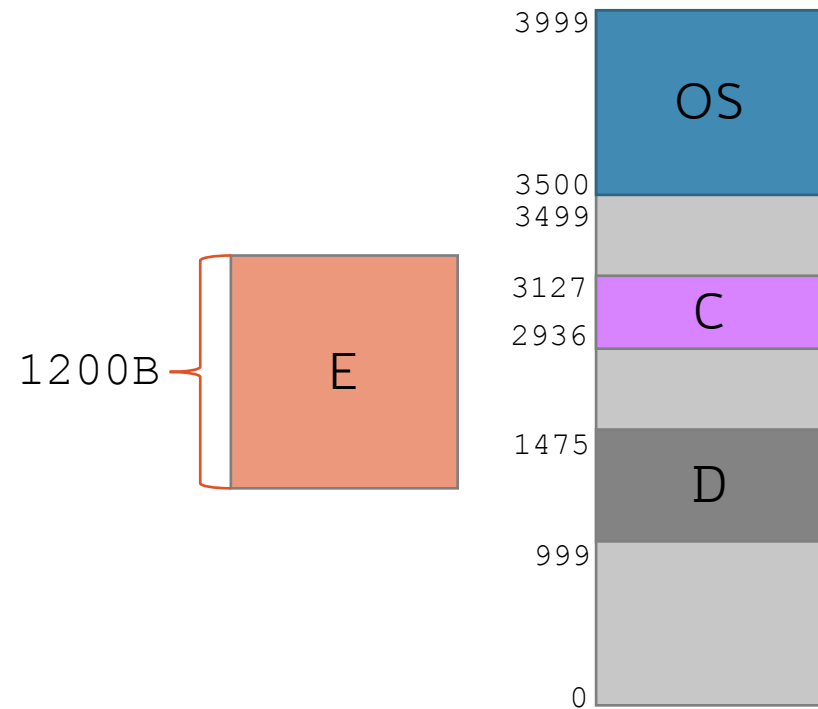
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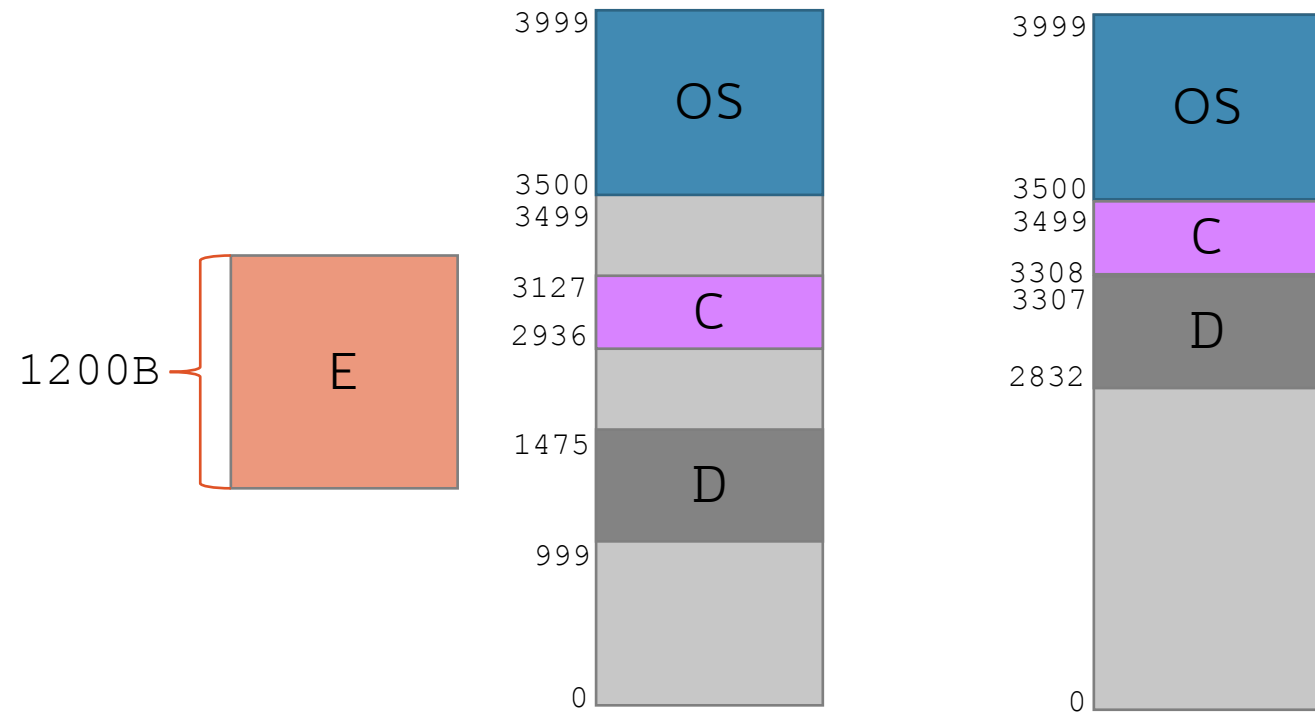
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- It may be much more efficient to allocate the process the whole block (and waste 2B) rather than keep track of a tiny 2B hole

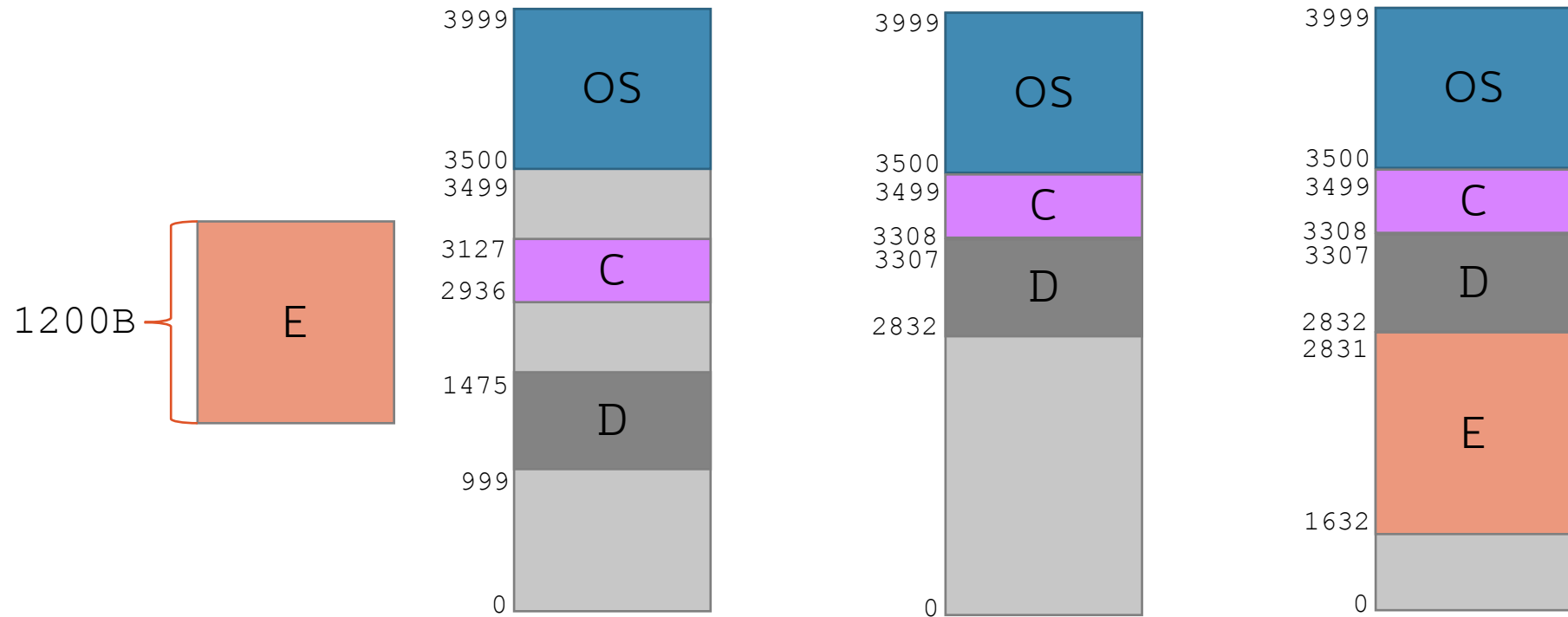
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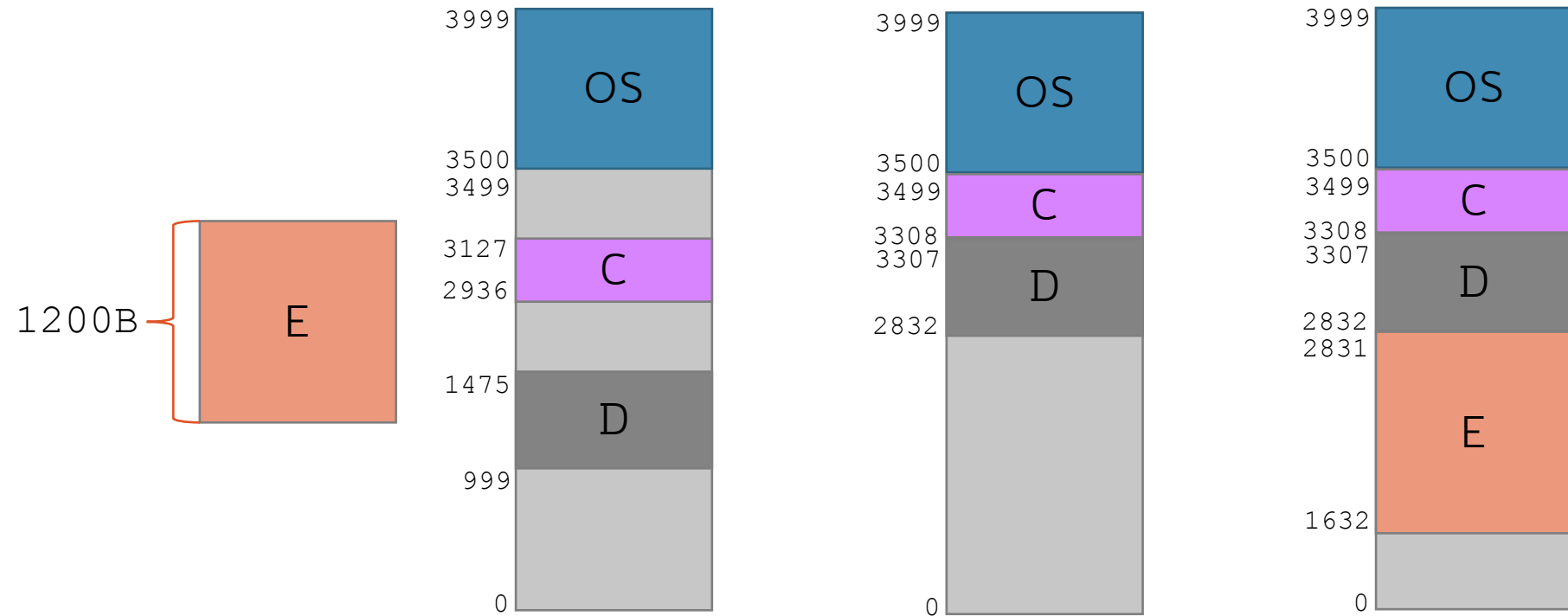
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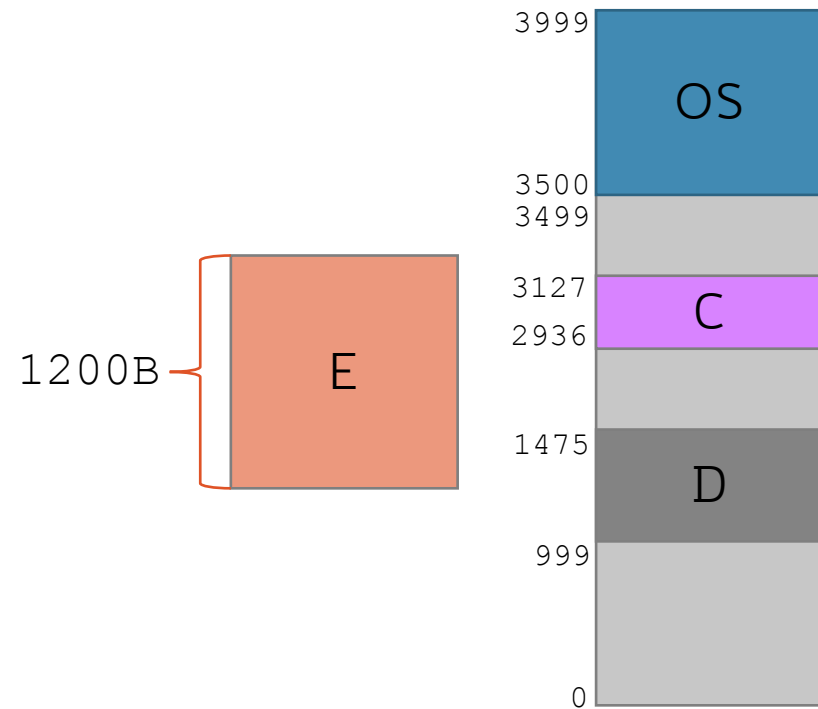


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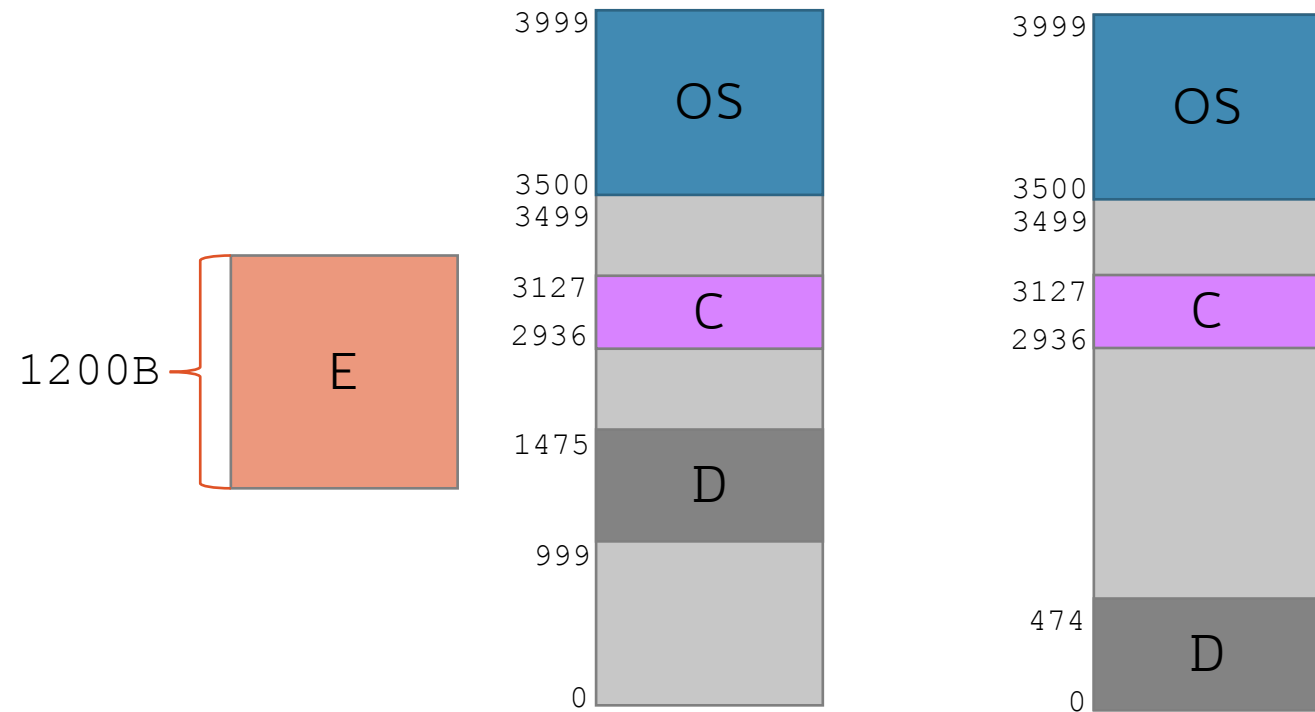
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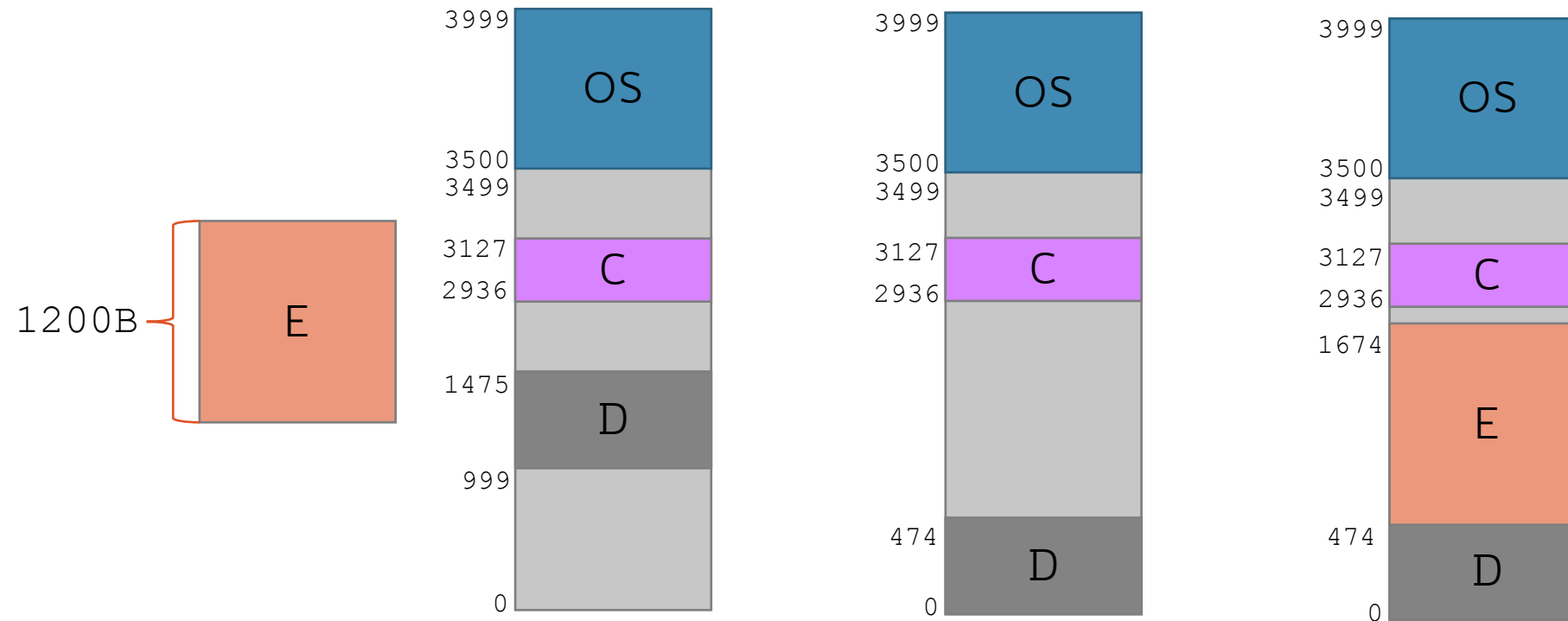




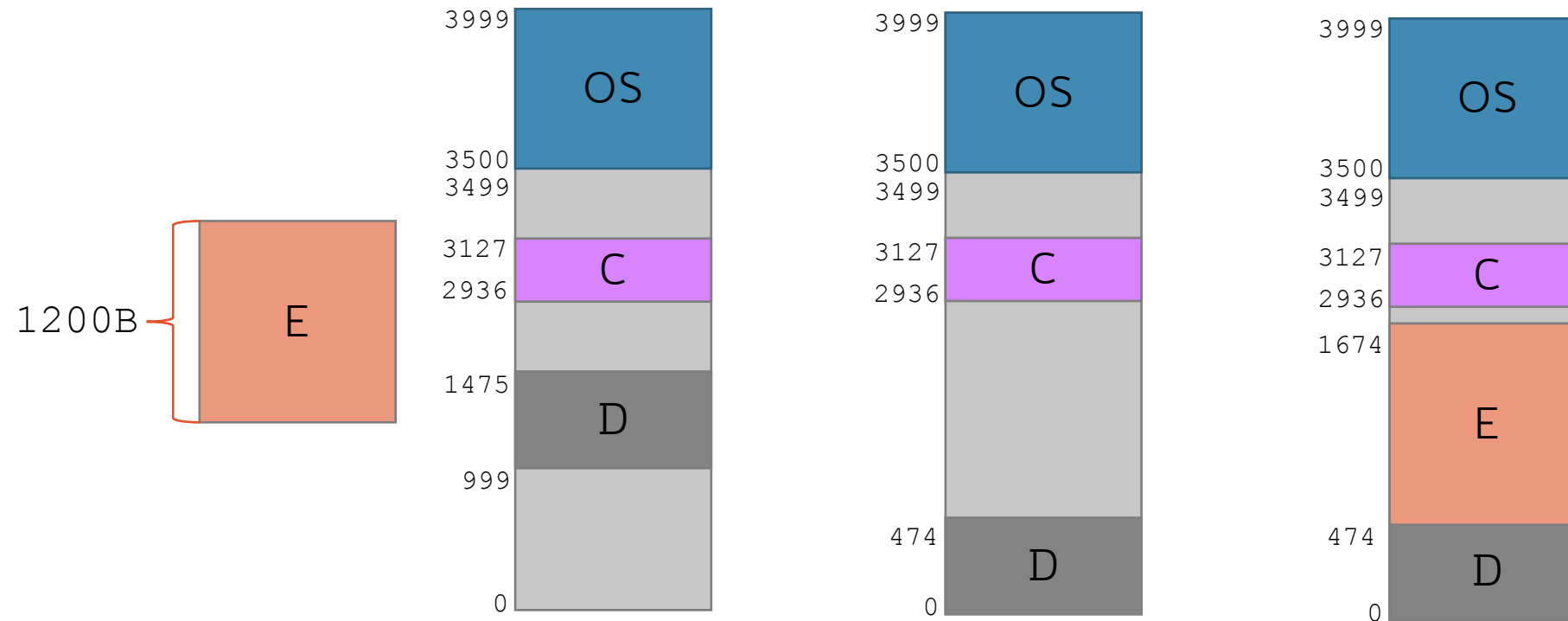
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Still some holes left but only one process is moved (D) rather than two

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- That process can be "swapped out" from memory to disk to make room for other processes

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- Using swapping, fragmentation can be tackled easily
  - Just run compaction before swapping-in a process

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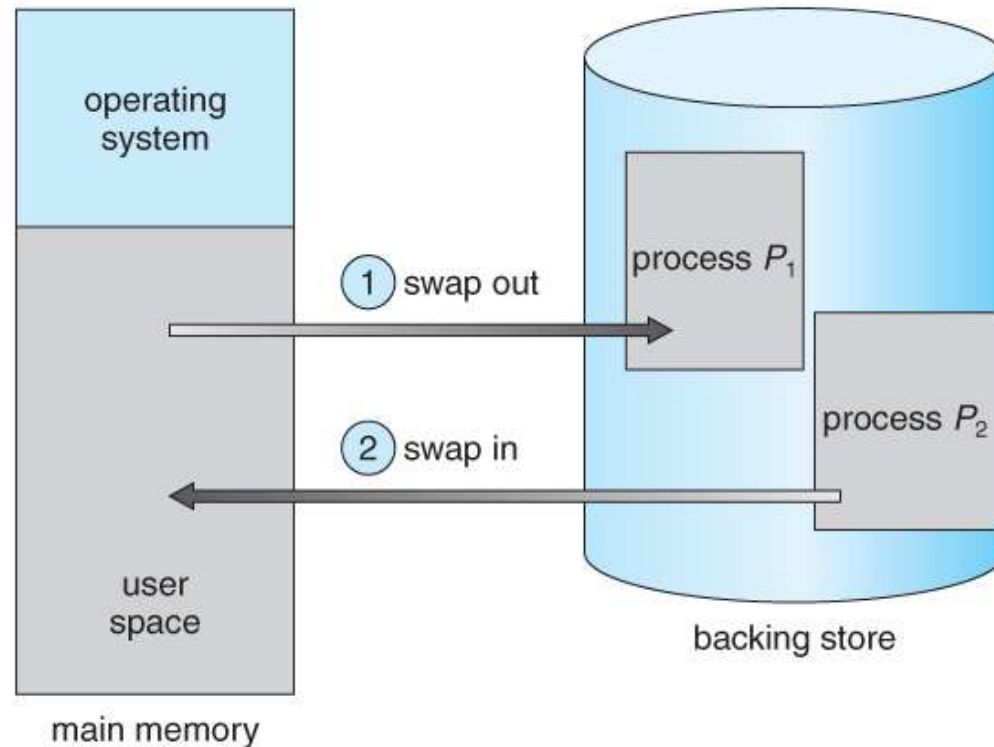
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- Time slice is usually way smaller than that!

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Most modern OSs no longer use swapping, because it is too slow and there are faster alternatives available (e.g., **paging**)



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- Process entirely loaded
  - Swapping helps but it may be too inefficient

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## 90/10 Rule

Processes spend **90%** of their time accessing only **10%** of their allocated memory space

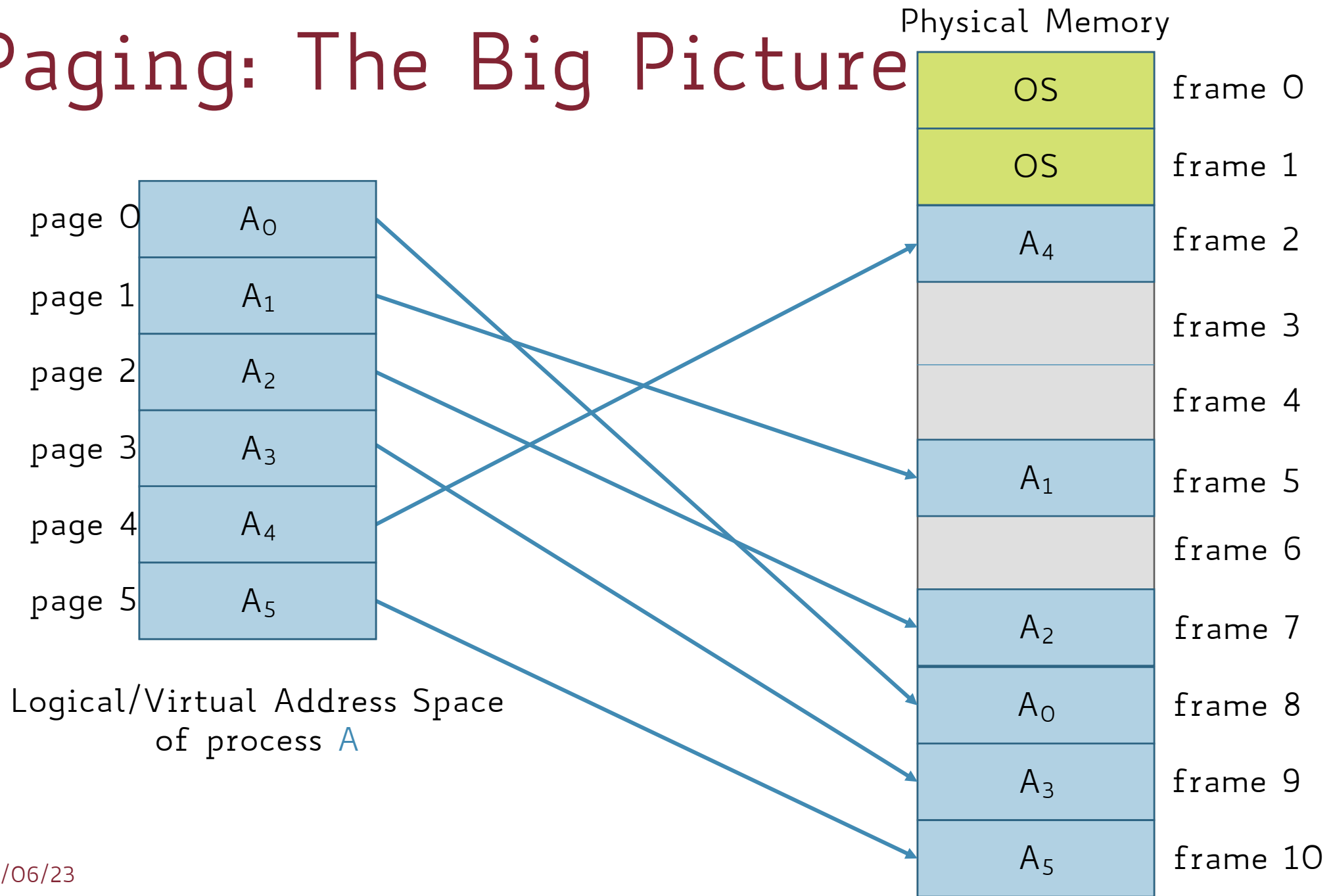


# Paging: The Big Picture

page 0	$A_0$
page 1	$A_1$
page 2	$A_2$
page 3	$A_3$
page 4	$A_4$
page 5	$A_5$

Logical/Virtual Address Space  
of process  $A$

# Paging: The Big Picture



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  - Remember, memory addresses are referenced all the time
- OS needs dedicated support for doing it → **Page Table**

# Page Table: Mapping Pages to Frames

0	A <sub>0</sub>
1	A <sub>1</sub>
2	A <sub>2</sub>
3	A <sub>3</sub>
4	A <sub>4</sub>
5	A <sub>5</sub>

OS	0
OS	1
A <sub>4</sub>	2
	3
	4
A <sub>1</sub>	5
	6
A <sub>2</sub>	7
A <sub>0</sub>	8
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# Page Table: Mapping Pages to Frames

Lookup table to retrieve what frame a page is stored in

0	A <sub>0</sub>
1	A <sub>1</sub>
2	A <sub>2</sub>
3	A <sub>3</sub>
4	A <sub>4</sub>
5	A <sub>5</sub>

Page	Frame
0	8
1	5
2	7
3	9
4	2
5	10

OS	0
OS	1
A <sub>4</sub>	2
	3
	4
A <sub>1</sub>	5
	6
A <sub>2</sub>	7
A <sub>0</sub>	8
A <sub>3</sub>	9
A <sub>5</sub>	10

# Page Table: Mapping Pages to Frames

Lookup table to retrieve what frame a page is stored in

0	A <sub>0</sub>	Page	Frame	OS	0
1	A <sub>1</sub>	0	8	OS	1
2	A <sub>2</sub>	1	5	A <sub>4</sub>	2
3	A <sub>3</sub>	2	7		3
4	A <sub>4</sub>	3	9		4
5	A <sub>5</sub>	4	2	A <sub>1</sub>	5
		5	10		6
				A <sub>2</sub>	7
				A <sub>0</sub>	8
				A <sub>3</sub>	9
				A <sub>5</sub>	10

We have assumed **all** pages of a process are mapped to physical frames, but this is not always the case



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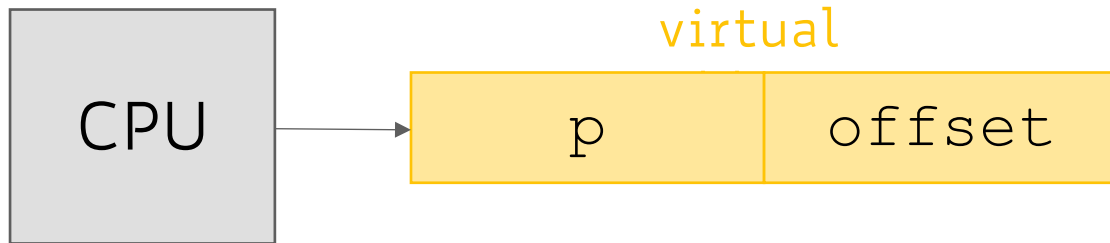
# Page Table: Virtual to Physical Address

- Processes use virtual (logical) addresses to refer to memory (not page number!)
- Virtual (logical) address space is still contiguous starting from 0
- Page table must ultimately translate virtual address to physical address

# Page Table: Virtual to Physical Address

virtual address consists of 2 parts:

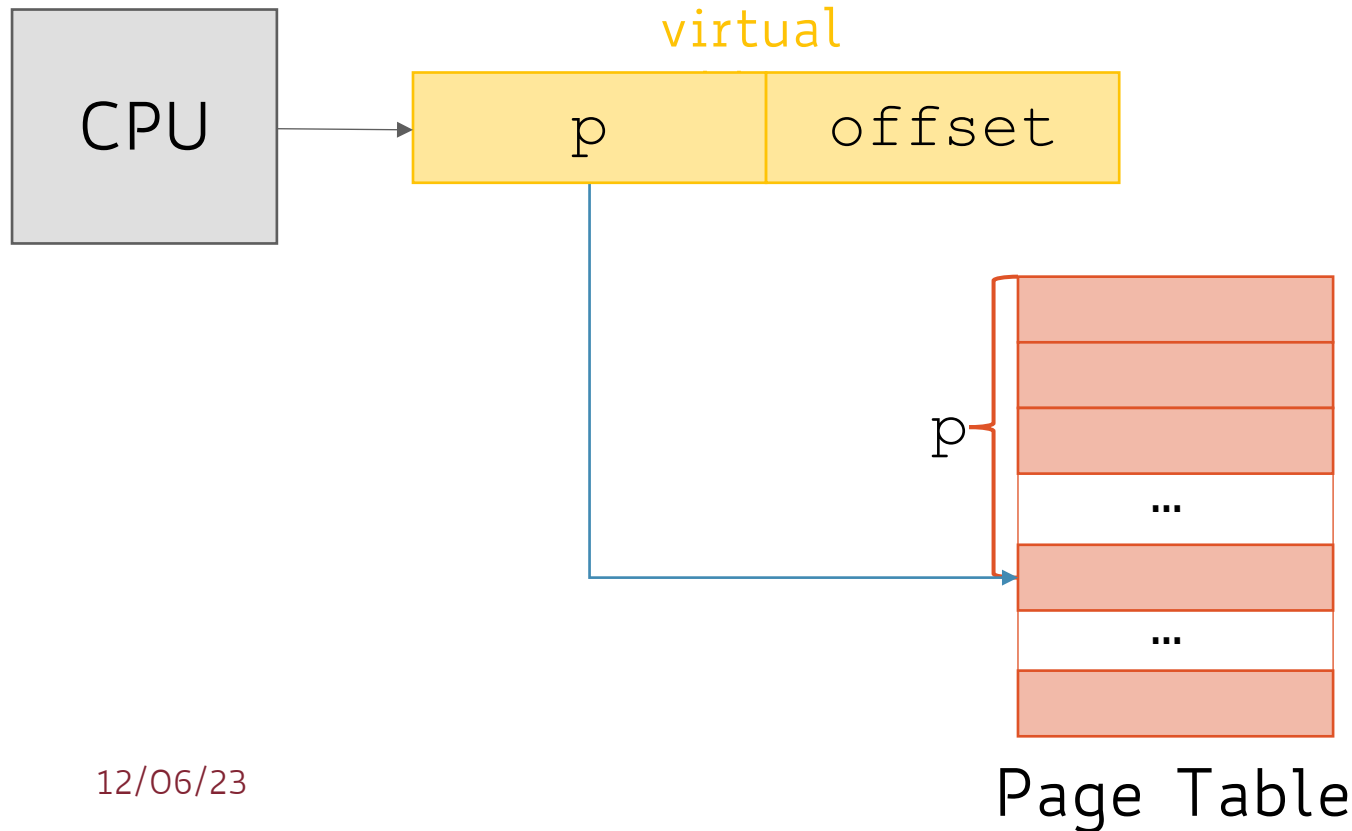
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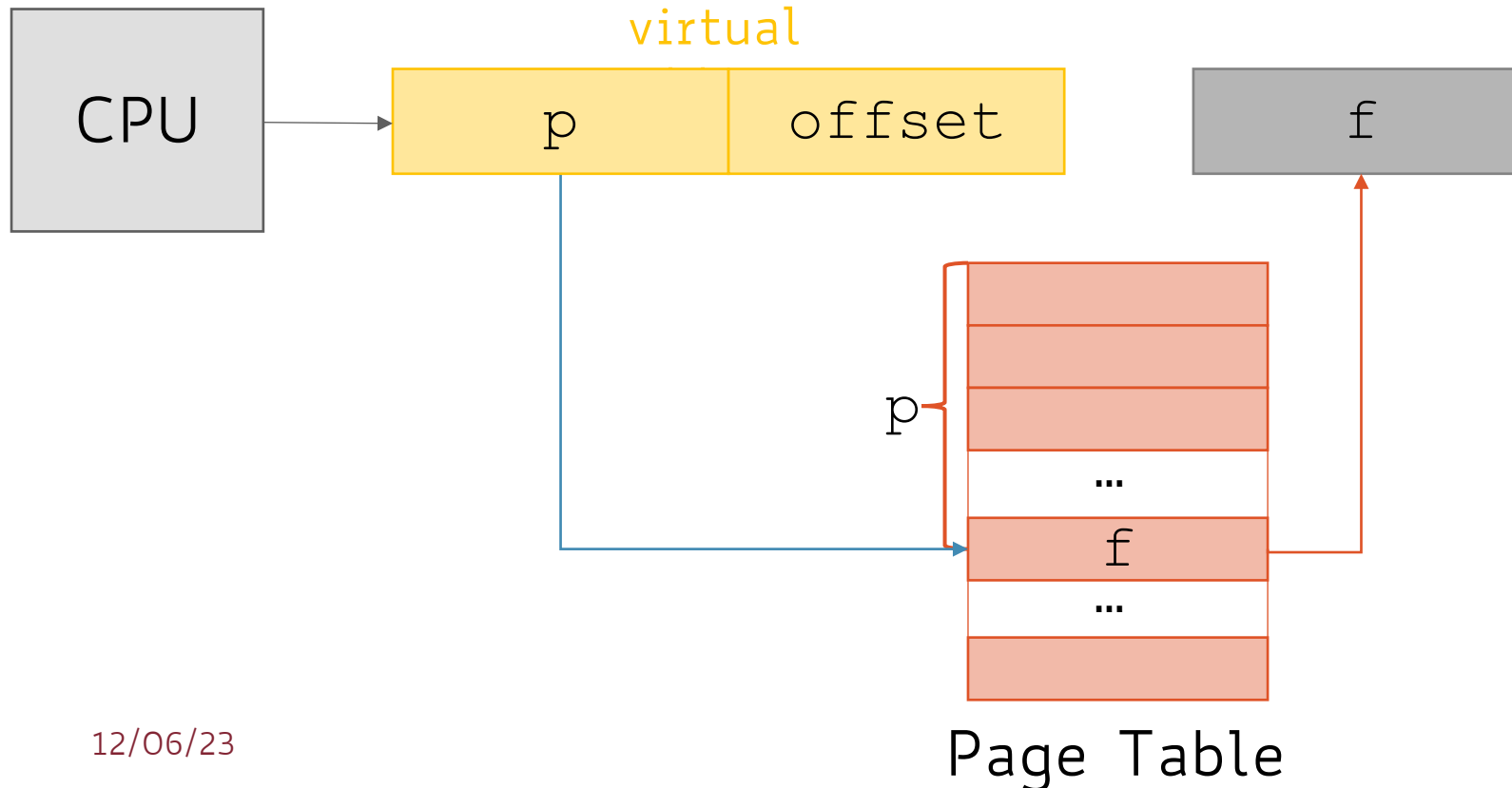
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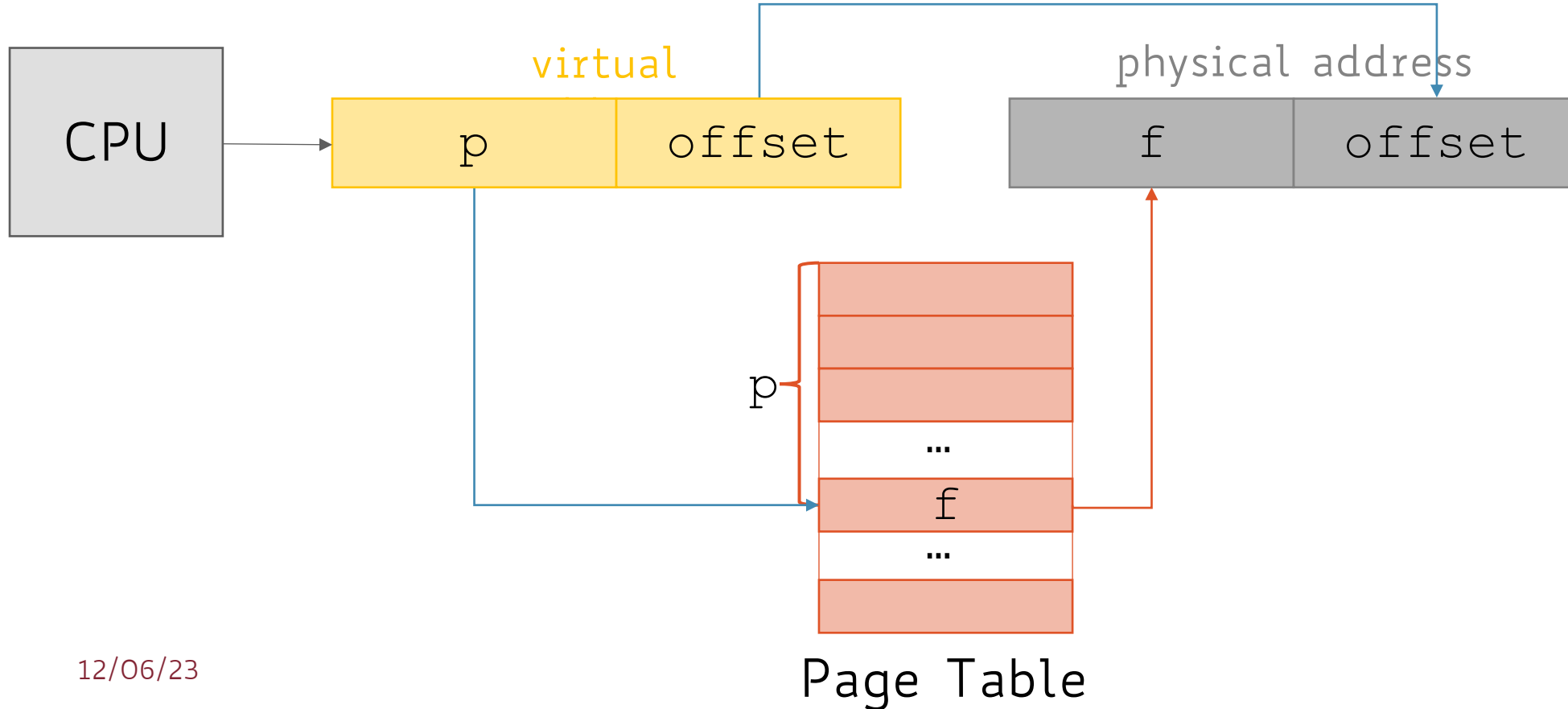
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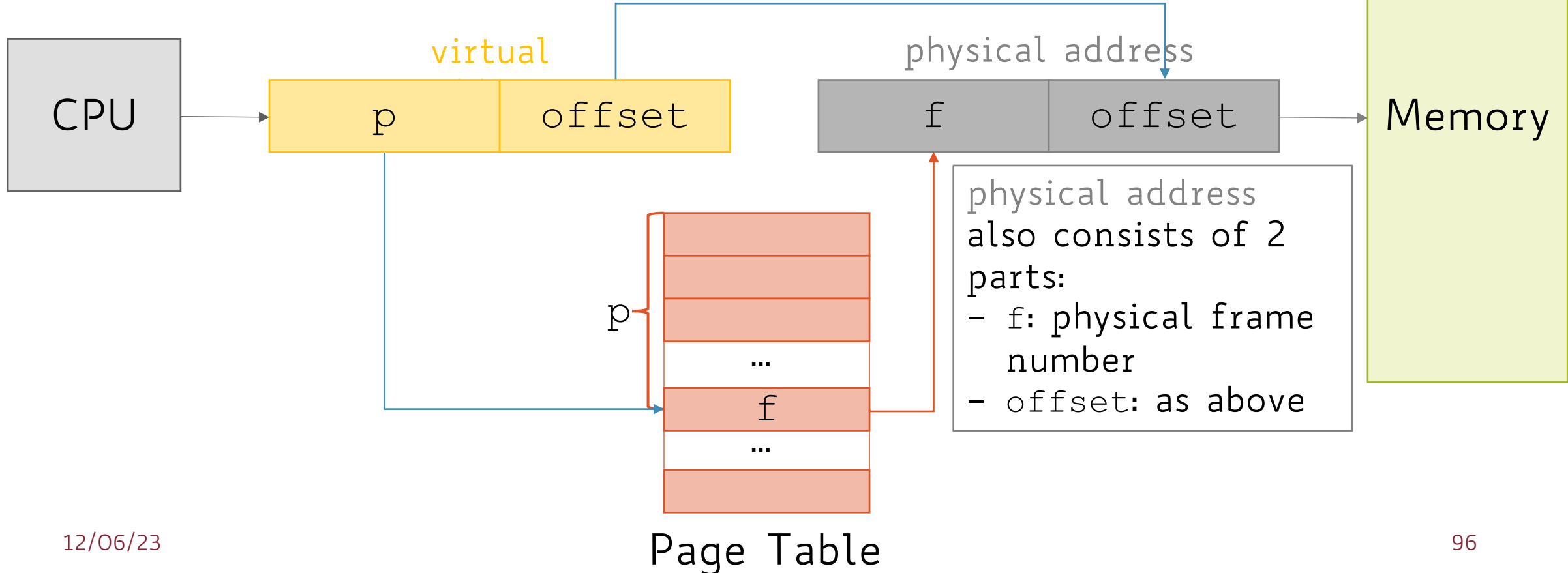
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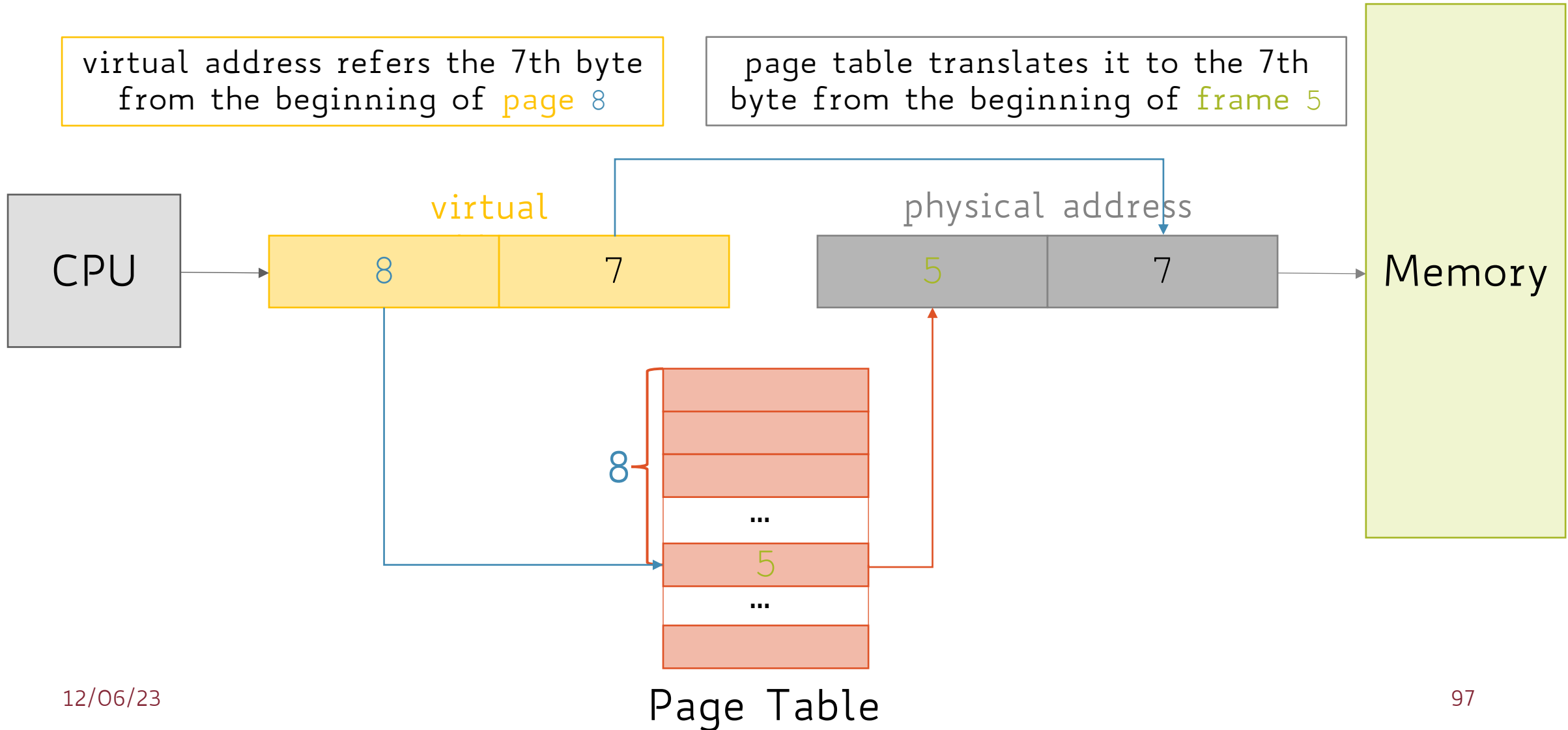




# Page Table: Example of Address Translation

virtual address refers the 7th byte from the beginning of **page 8**

page table translates it to the 7th byte from the beginning of **frame 5**



# Paging as Dynamic Relocation

- Paging is an advanced form of dynamic relocation
- Each virtual address is bound by the page table to a physical address
- Page table can be seen just as a set of base (relocation) registers, one for each frame
- Mapping is invisible to the user process: the OS maintains the page table and translation happens in hardware (via the MMU)
- Protection is provided similarly to dynamic relocation (limit register)

# Paging: Steps

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3. Combine  $f$  with **offset** to obtain the physical address  $y$

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Address translation requires a **div** and a **mod** operation

# Paging: Implementation Details

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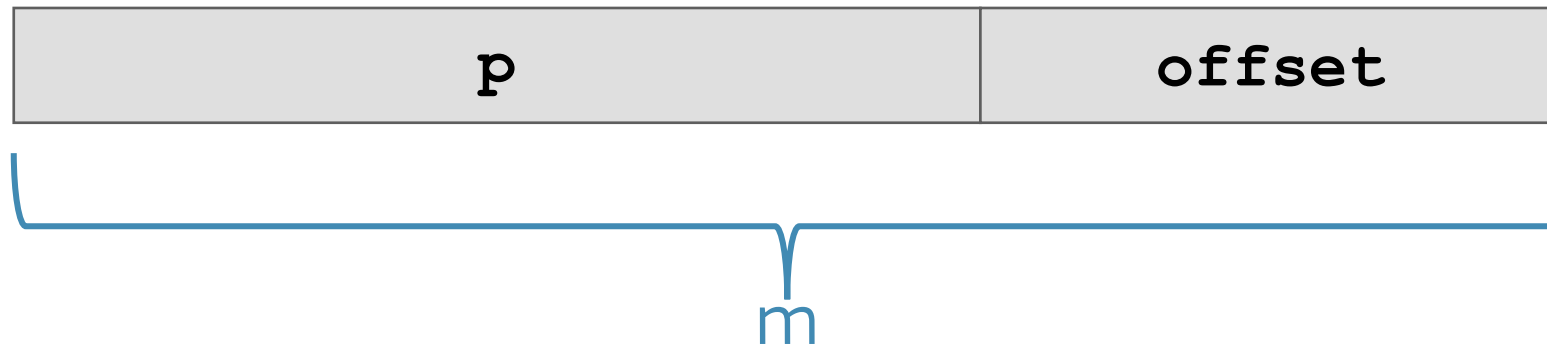
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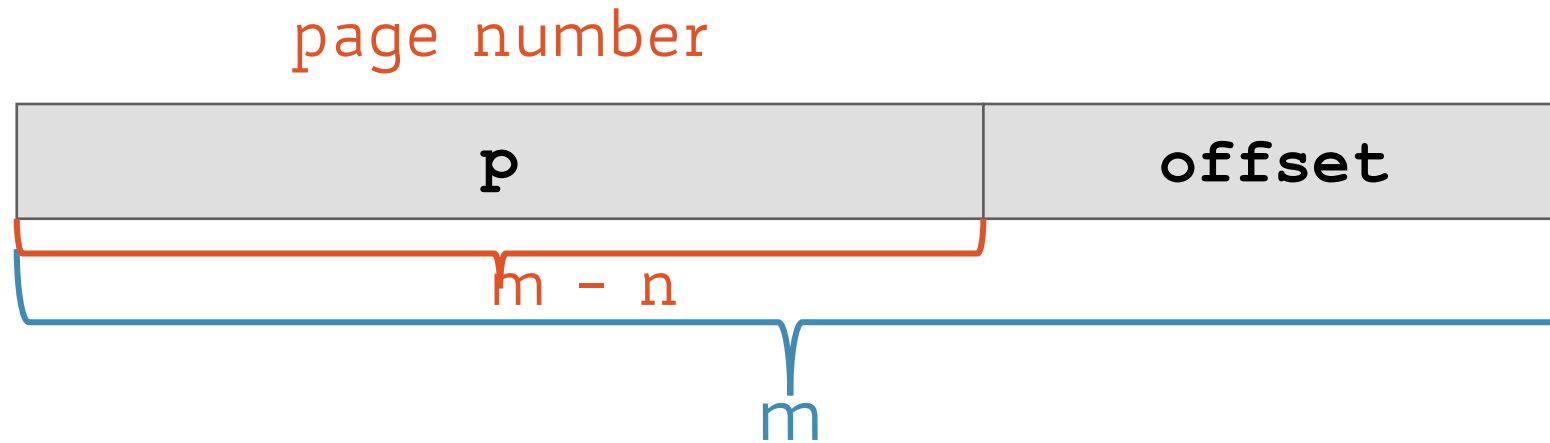
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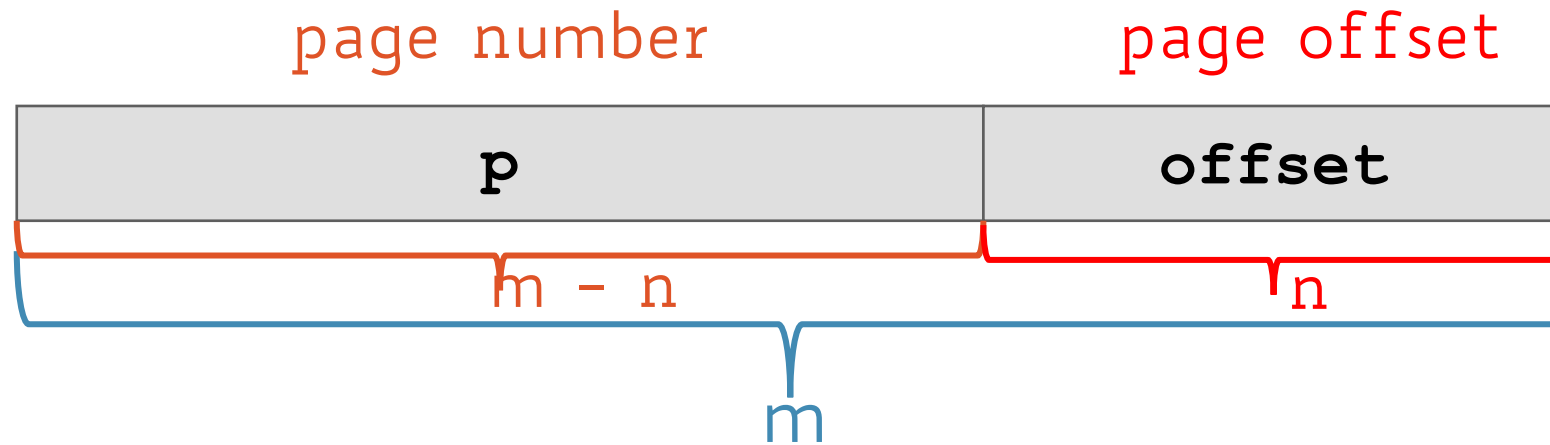
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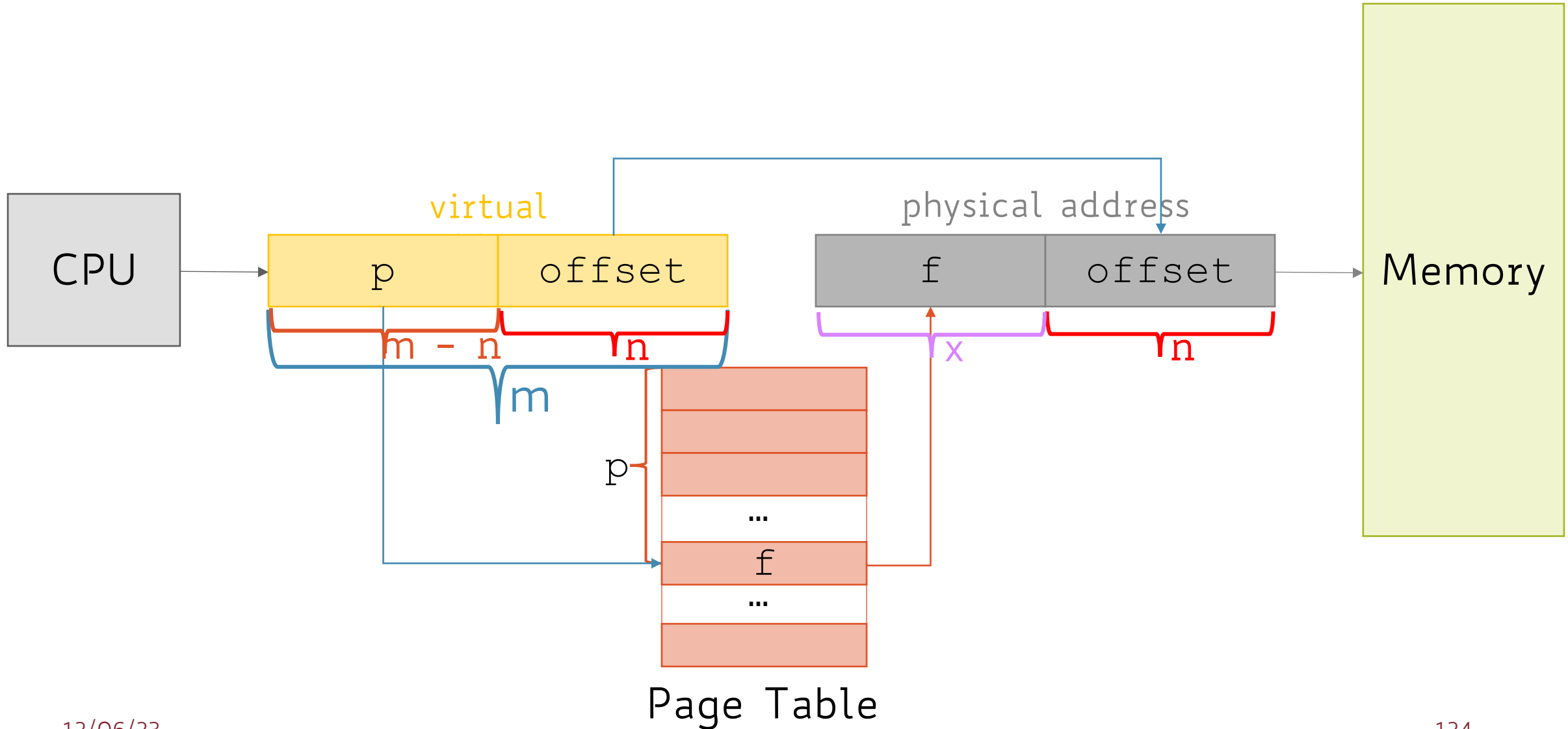
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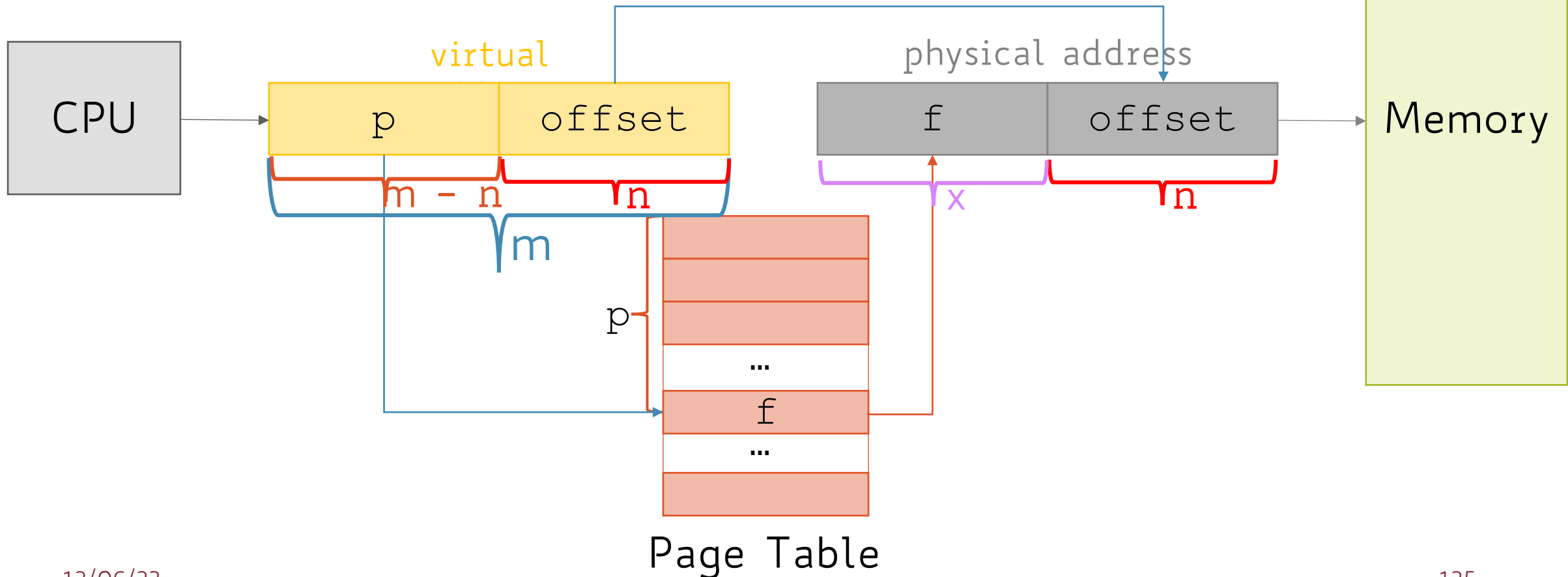
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## NOTE

$m-n$  doesn't necessarily have to be equal to  $x$



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- Typical values of virtual address size is  $m = 32$  or  $64$  bits
  - The virtual address space is  $2^{32} = 4\text{GiB}$  or  $2^{64} = 16\text{EiB}$

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  - Each page/frame is  $2^{12} = 4\text{KiB}$
- Assuming  $m = 32$  bits, there are  $2^{m-n} = 2^{20} = \sim 1\text{M}$  pages/frames
  - The page table has  $2^{20}$  entries (i.e., one for each page/frame)



# Paging: Practical Example

Suppose we have a virtual memory and a physical memory, both of size  $M = 1024\text{B}$  (1KiB)

Q1

How many bits are needed for a virtual/physical address (assuming single-byte addressing)

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R1

10 bits to address  $M = 1024$  bytes (both for virtual and physical address)

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$T = M / S = 1024 \text{ memory bytes} / 16 \text{ bytes per page} = 64 \text{ pages}$

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Our logical address is made of  $m = 10$  bits  
 $n = 4$  bits are used to represent the  $offset$ , as each page/frame is  $S = 16$  bytes  
 $m - n = 6$  bits are used to represent page number  $p$ , as there are  $T = 64$  pages

# Paging: Practical Example

Q4

Translate the virtual address  $x = 42$ , assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

# Paging: Practical Example

Q4

Translate the virtual address  $x = 42$ , assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

R4

$$p = x \text{ div } S = 42 \text{ div } 16 = 2$$



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R4

$$p = x \text{ div } S = 42 \text{ div } 16 = 2$$

$$\text{offset} = x \text{ mod } S = 42 \text{ mod } 16 = 10$$

10th byte from the beginning of frame 37

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Modern computers however operate natively on multiple of bytes (i.e., words) rather than single-byte. Typical values of word length is: 16, 32 or 64 bits.

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R1

8 bits to address  $M = 1024/4 = 256$  4-byte words

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What is  $p$  and `offset` (i.e., how many bits for  $p$  and `offset`?)

R3

Our logical address is now made of  $m = 8$  bits  
 $n = 2$  bits are used to represent the `offset`, as each page/frame is:  
 $S = 16$  bytes =  $4 * 4$ -byte words  
 $m - n = 6$  bits are used to represent page number  $p$ , as there are still  
 $T = 64$  pages

# Paging: Practical Example 2

Q4

Translate the virtual address  $x = 7$ , assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

# Paging: Practical Example 2

Q4

Translate the virtual address  $x = 7$ , assuming the following page table

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...	..
63	29

Remember: now virtual address refers to a 4-byte word!

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Translate the virtual address  $x = 7$ , assuming the following page table

page	frame
0	12
1	5
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$S = 16 \text{ bytes} = 4 * 4\text{-byte}$   
**words**

Must be expressed in terms  
of number of words

R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

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Q4

Translate the virtual address  $x = 7$ , assuming the following page table

page	frame
0	12
1	5
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...	..
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R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

$$\text{offset} = x \text{ mod } S = 7 \text{ mod } 4 = 3$$

3rd word from the beginning of frame 5

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- Trade-off solution: **Translation Look-aside Buffer (TLB)**, namely a cache!

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- Several chunks of memory transferred from main memory to the cache
- Access individual memory locations one at a time from the cache rather than from memory directly

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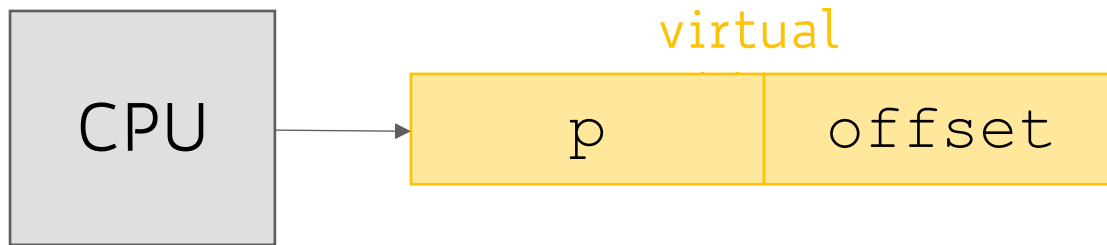
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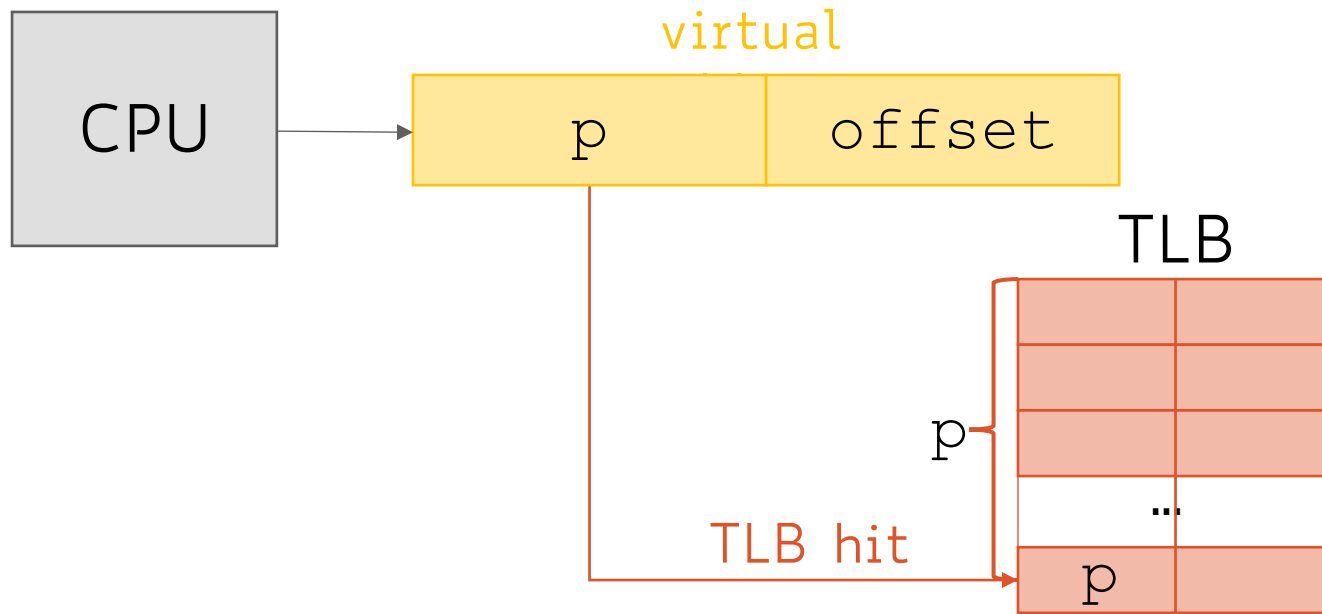
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- Typical TLB sizes range from 8 to 2048 entries

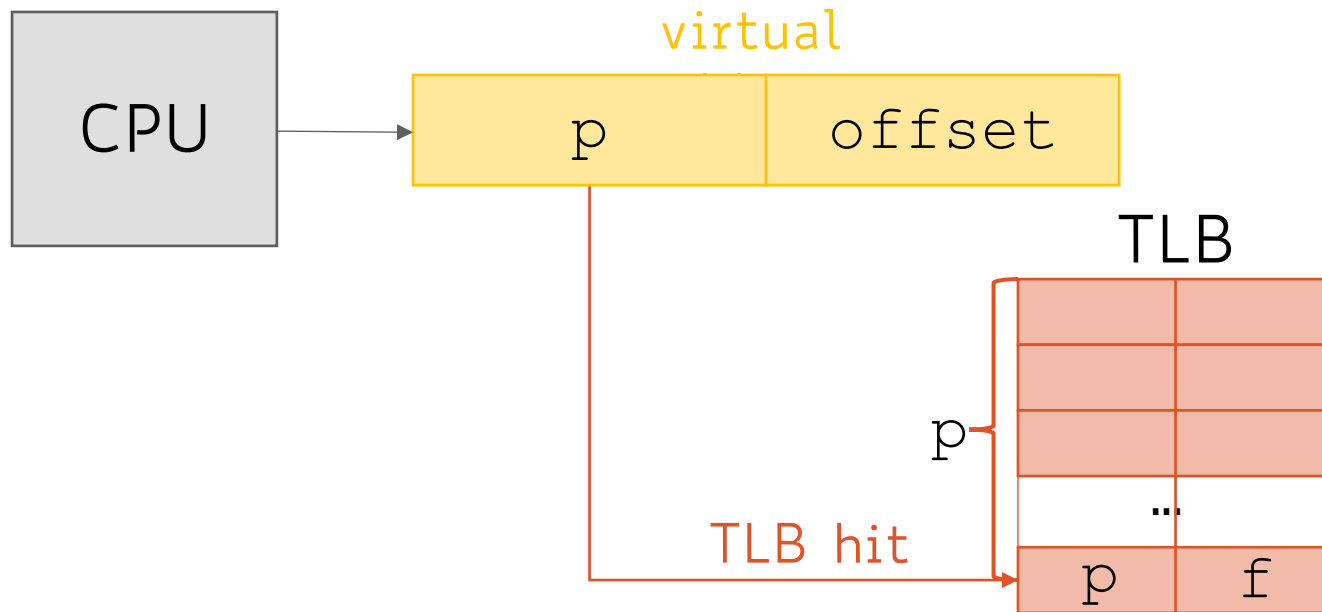
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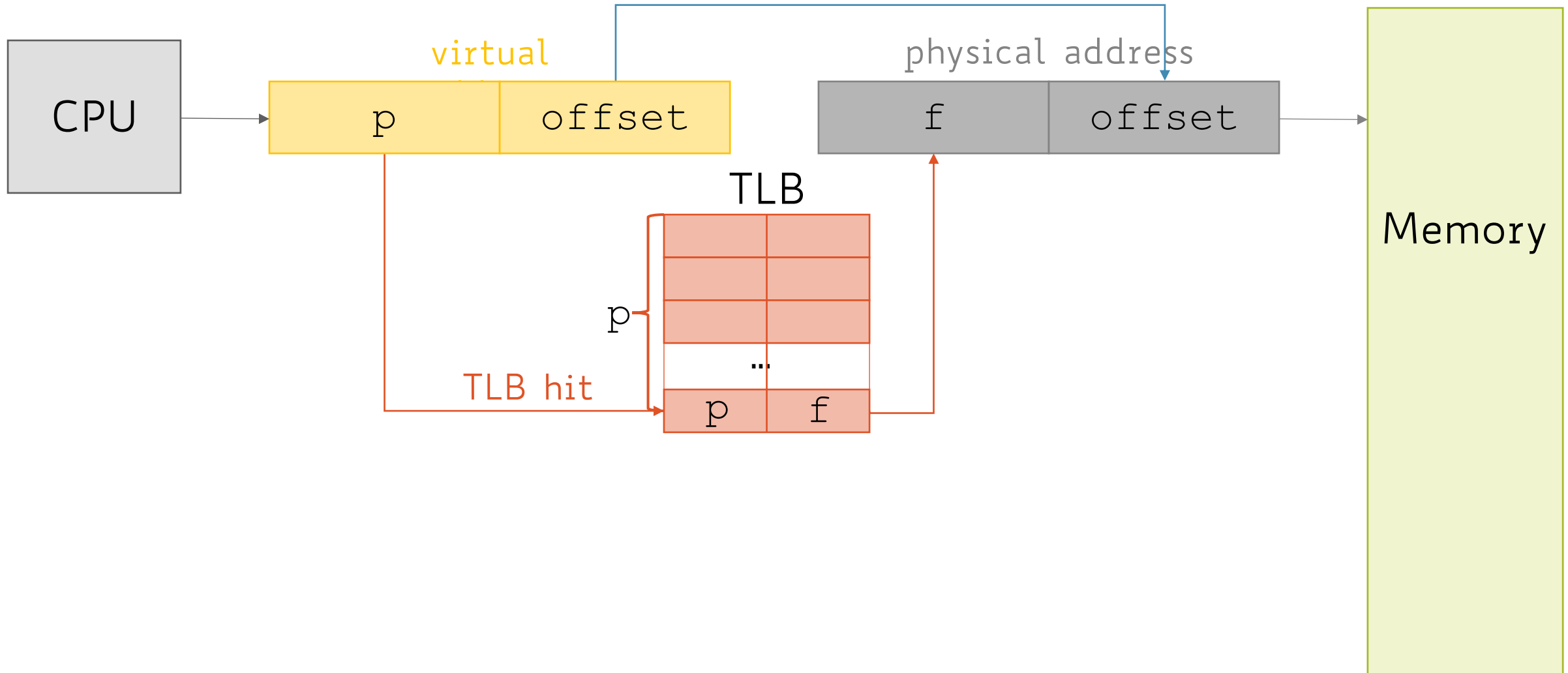
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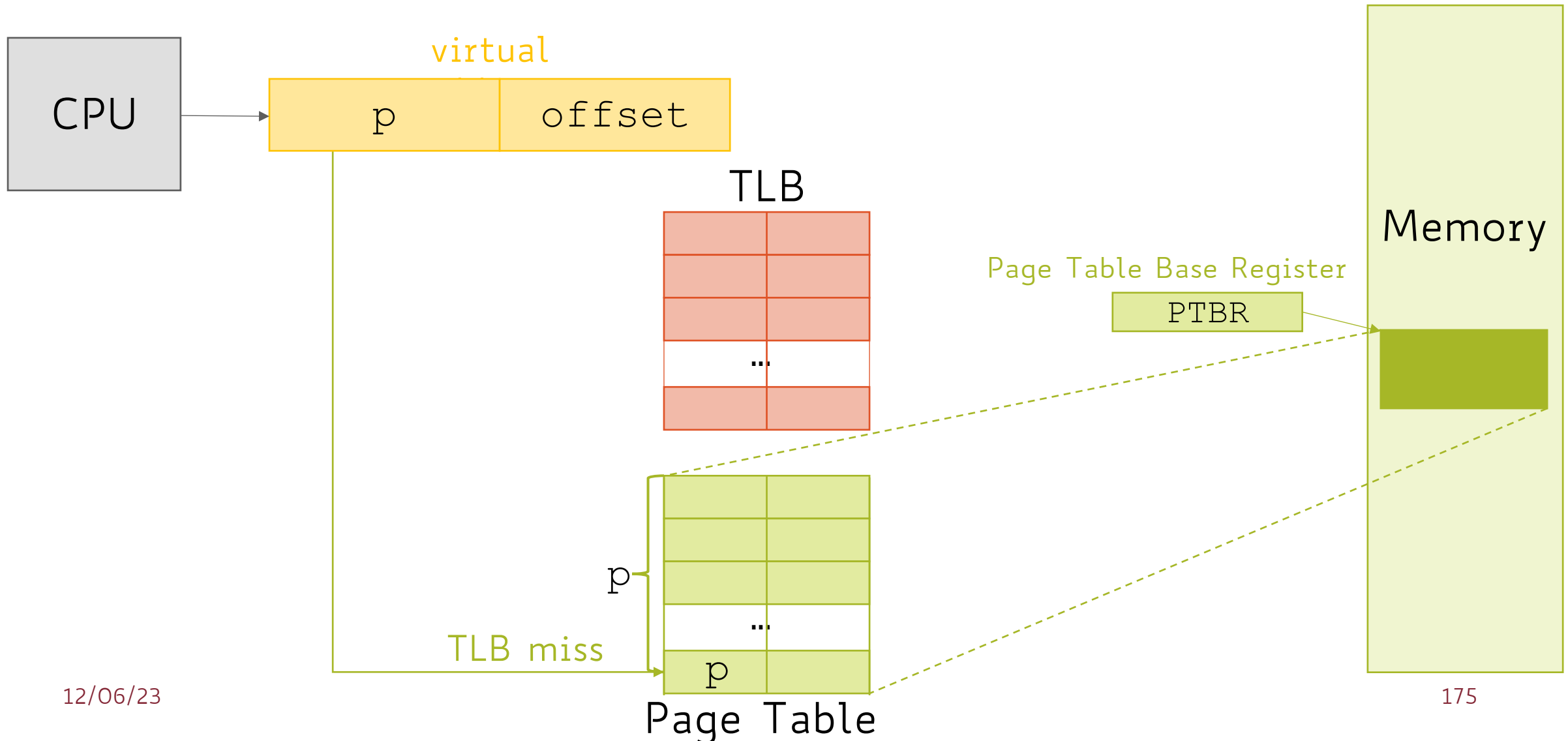
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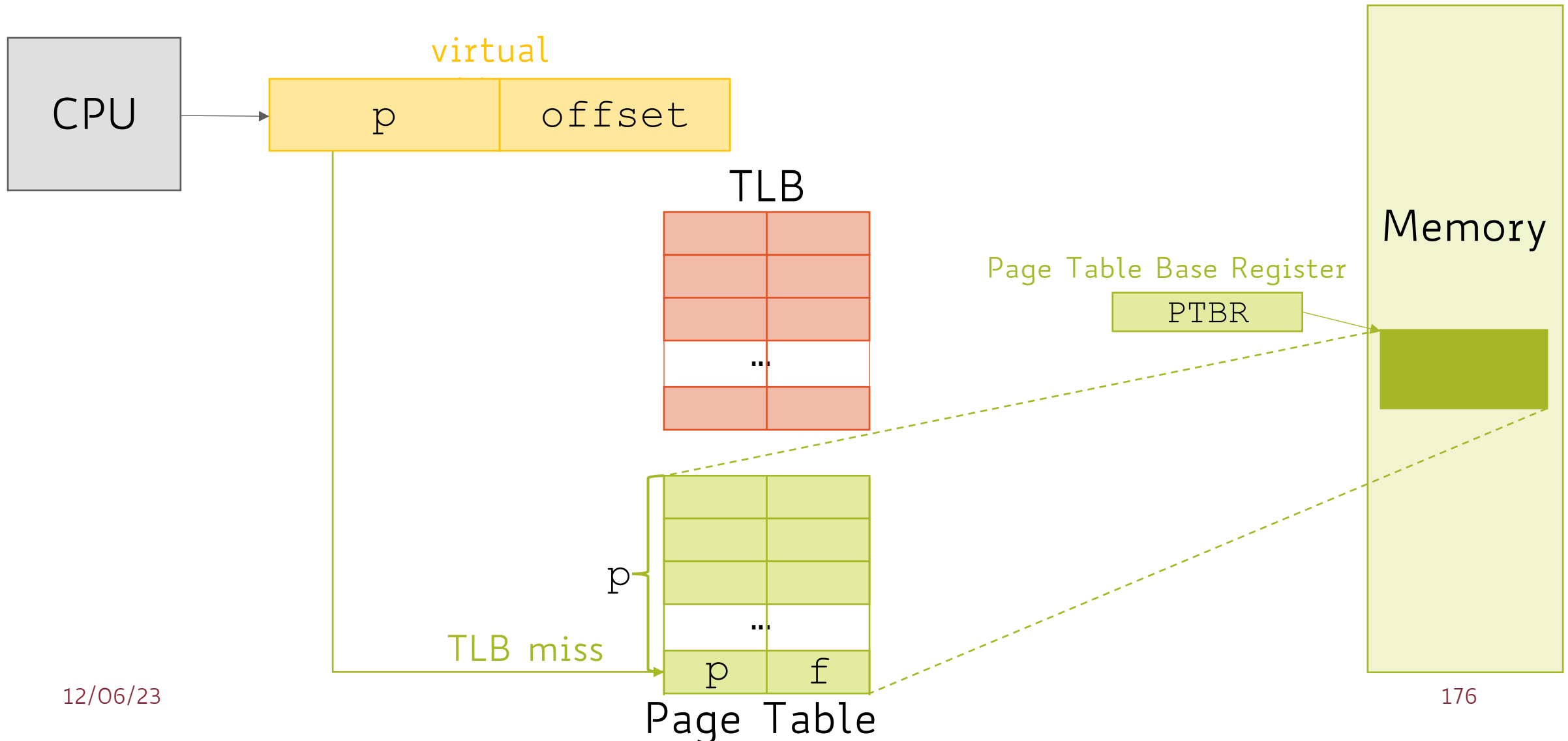
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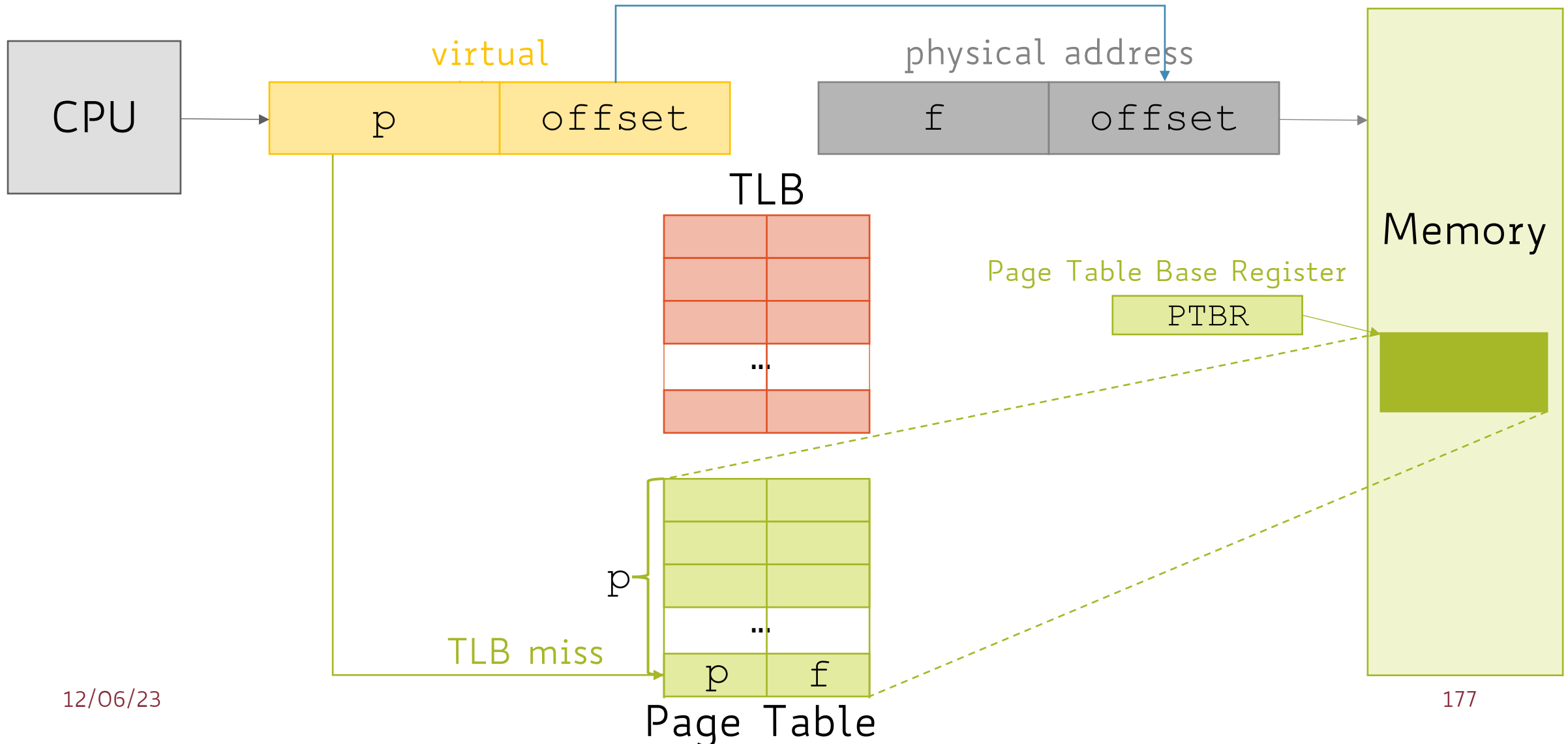


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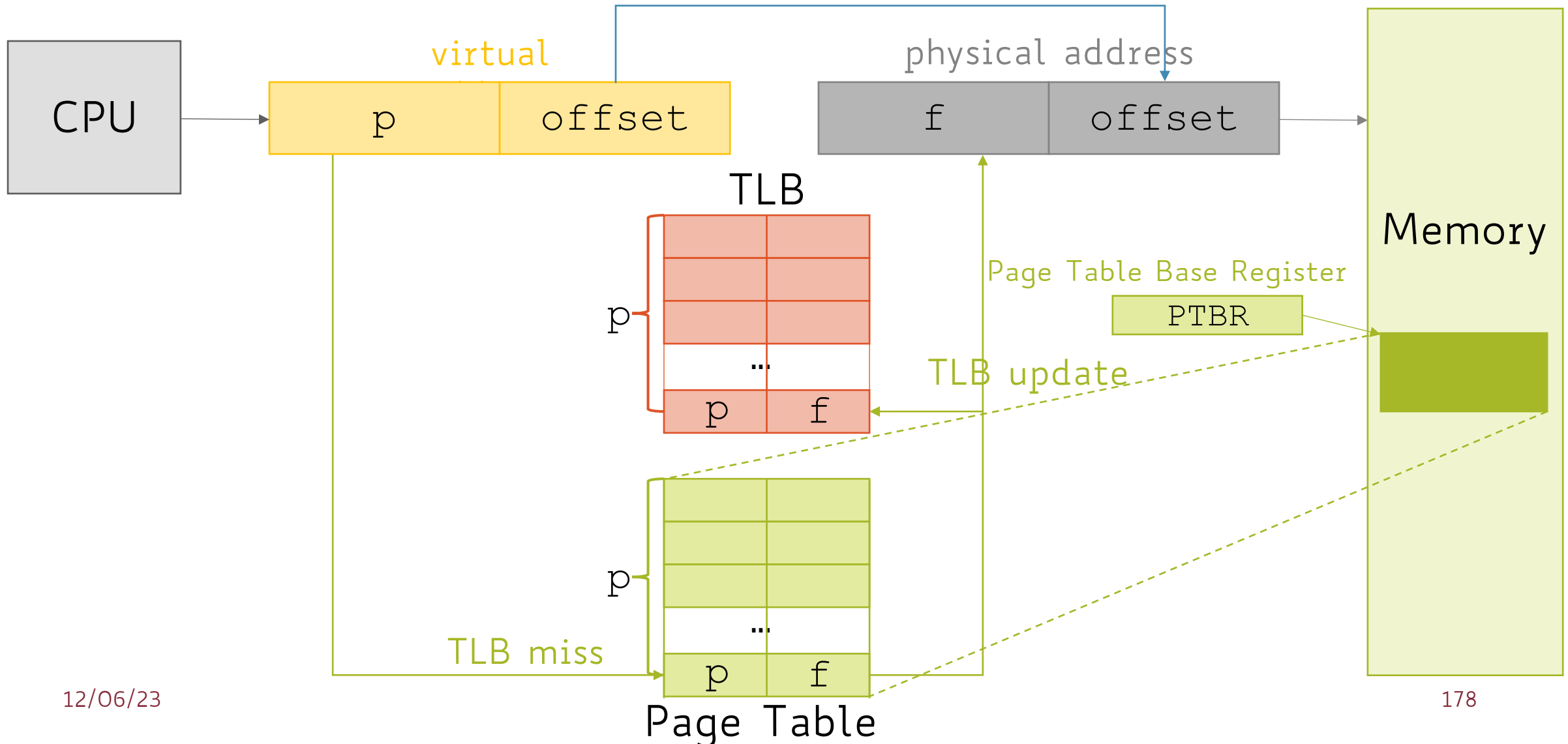




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- **2 setups:**
  - **basic:** at each context switch the content of the TLB is fully flushed and cleaned (cold-start → the first accesses will generate all TLB misses)
  - **advanced:** TLB entries dumped and restored within the PCB or adding a so-called process context ID (PCID) to each entry (the CPU will use a TLB entry iff the PCID of that entry corresponds to the ID of the running process)



# Memory Access Cost

$t_{MA}$  = physical memory access time

$t_{TLB}$  = lookup time on the TLB cache

(NOTE:  $t_{TLB} \ll t_{MA}$ )

$p$  = probability of TLB cache hit (i.e., *hit ratio*)

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The larger the TLB the higher the probability  $p$  of hit ratio, thereby decreasing the average memory access cost

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- Each memory reference can be checked to ensure it is accessing the memory in the appropriate mode
- Valid/invalid bits can be added to "mask off" entries in the page table that are not in use by the current process

# Additional Protection

- Valid/Invalid bits cannot block all illegal memory accesses, due to the internal fragmentation

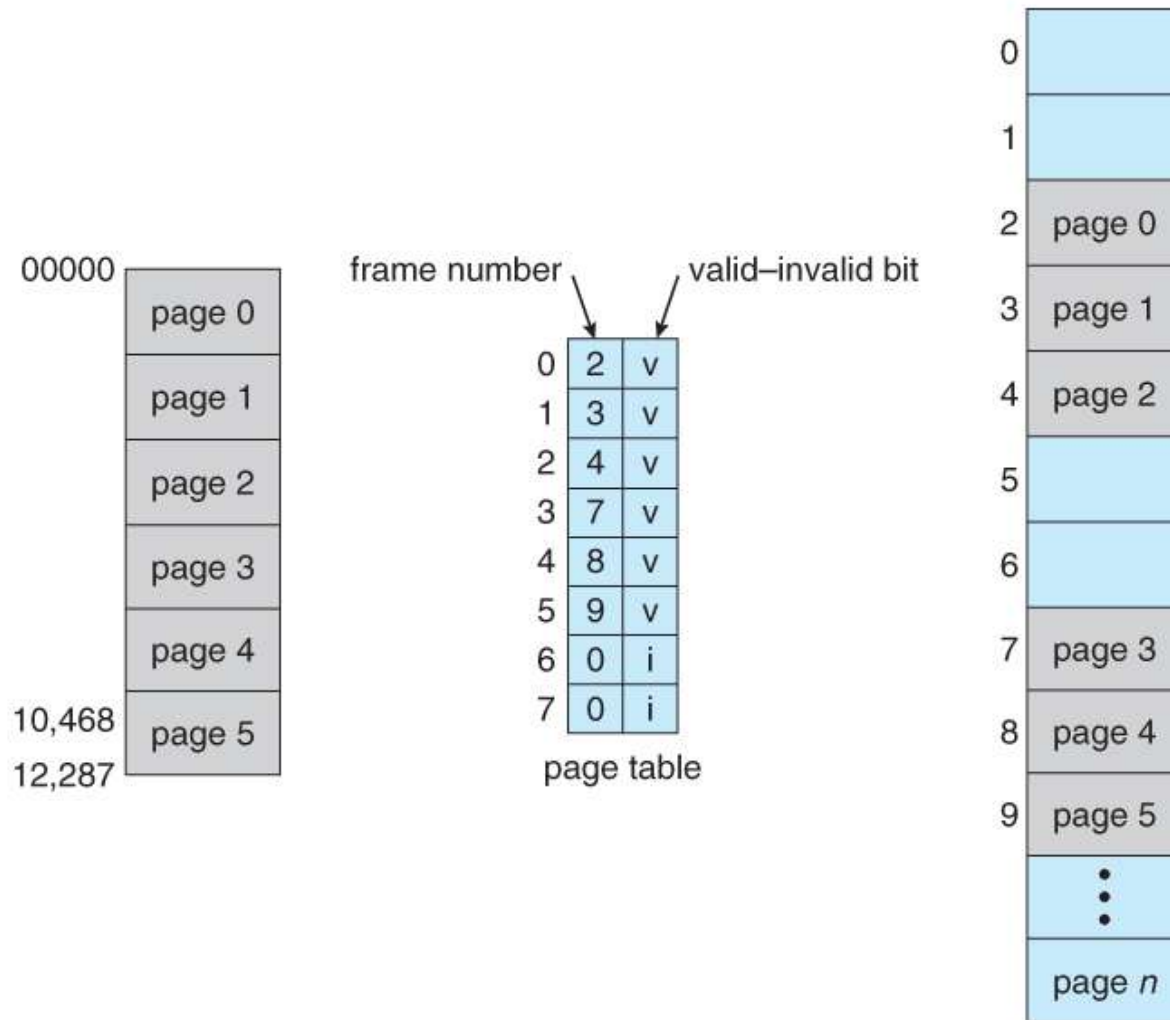
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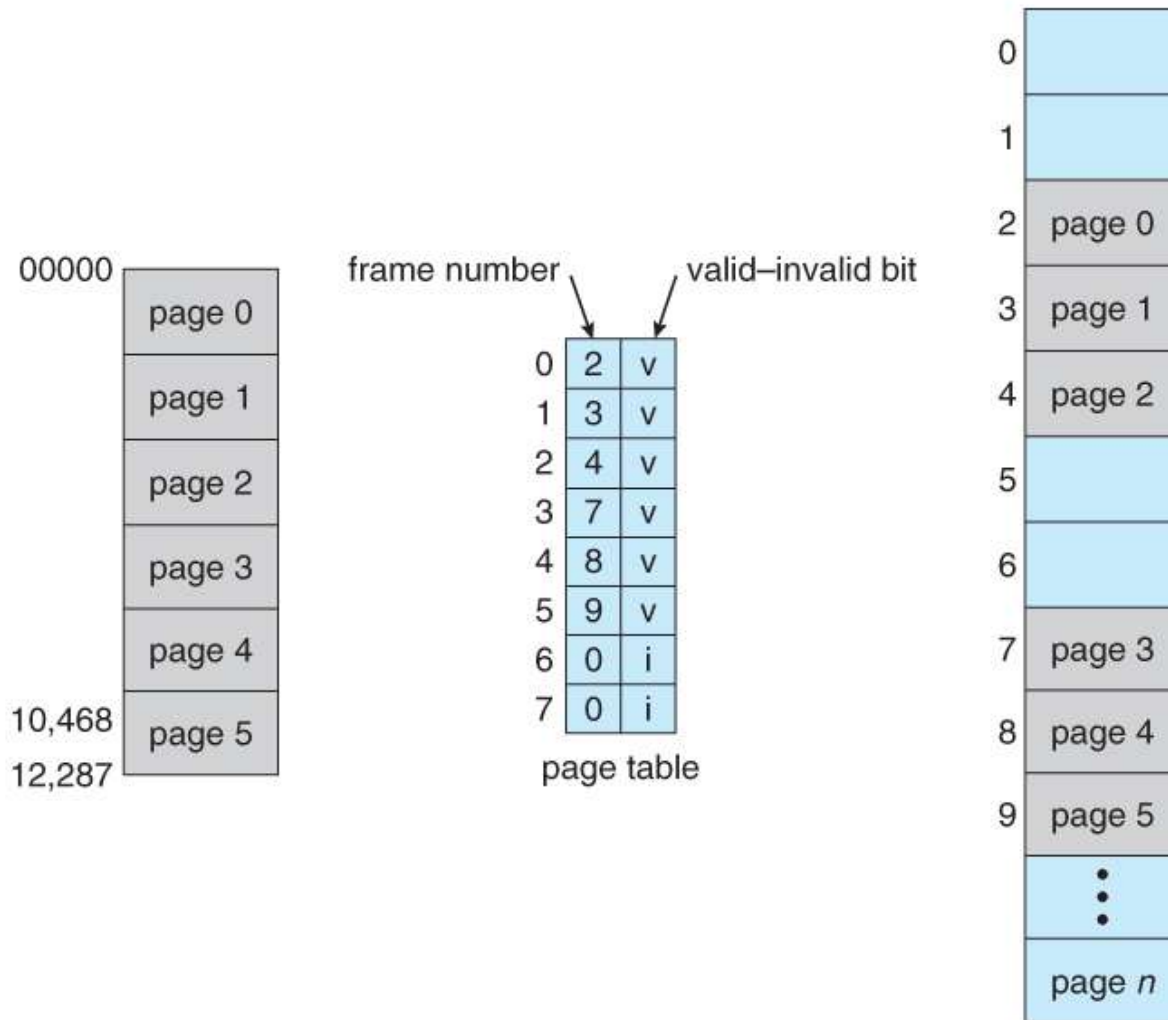
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- Many processes do not use all of the page table entries available, particularly in modern systems with very large potential page tables
- Some systems use a page-table length register (PTLR) to specify the length of the page table

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any entry whose invalid bit is set will be discarded (and updated)

# Memory Initialization

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5. As process runs, OS loads TLB missed entries possibly replacing existing entries if TLB is full

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  - Possibly a copy of the TLB entries
- On a context switch:
  - Copy the PTBR value to the PCB
  - Copy the TLB to the PCB (optional)
  - Flush the TLB (if TLB is not saved to/restored from the PCB)
  - Restore the PTBR (i.e., with the value of the new running process)
  - Restore the TLB (if it was previously saved)

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- Memory doesn't have to be contiguous anymore!
- Just duplicate page entries of different processes to the same page frames (both for code and data)

# Sharing Pages

- Only if code is **reentrant!**

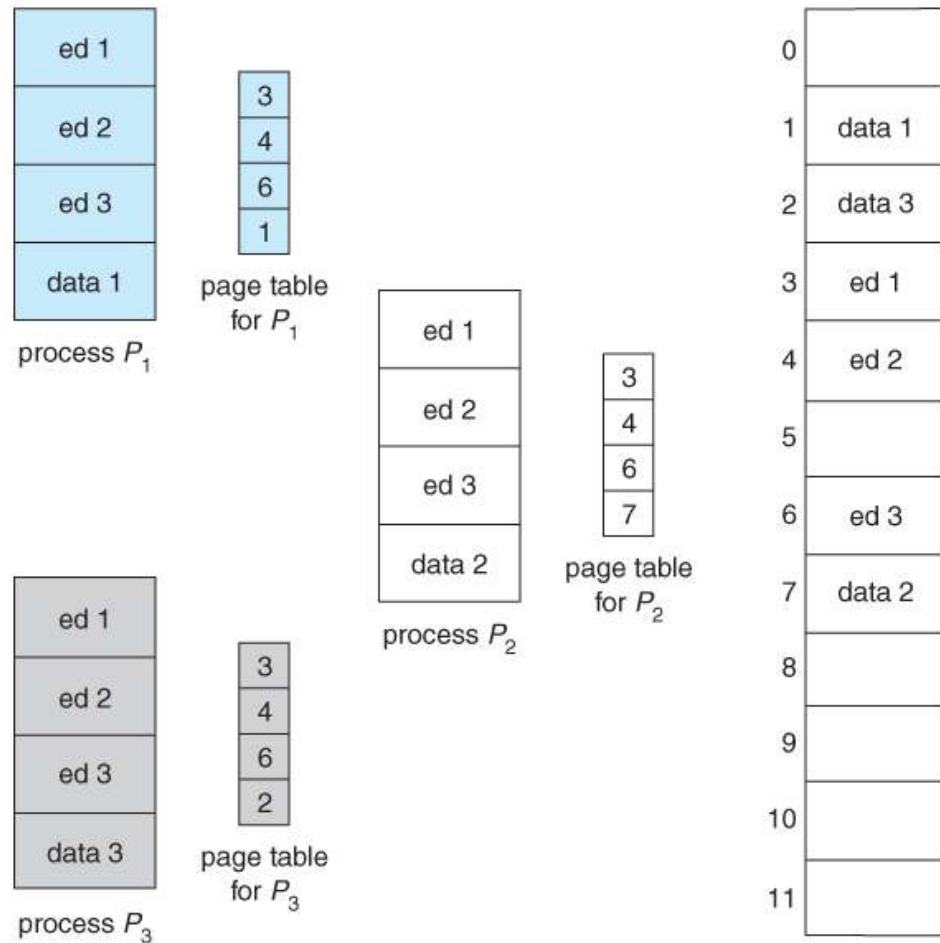
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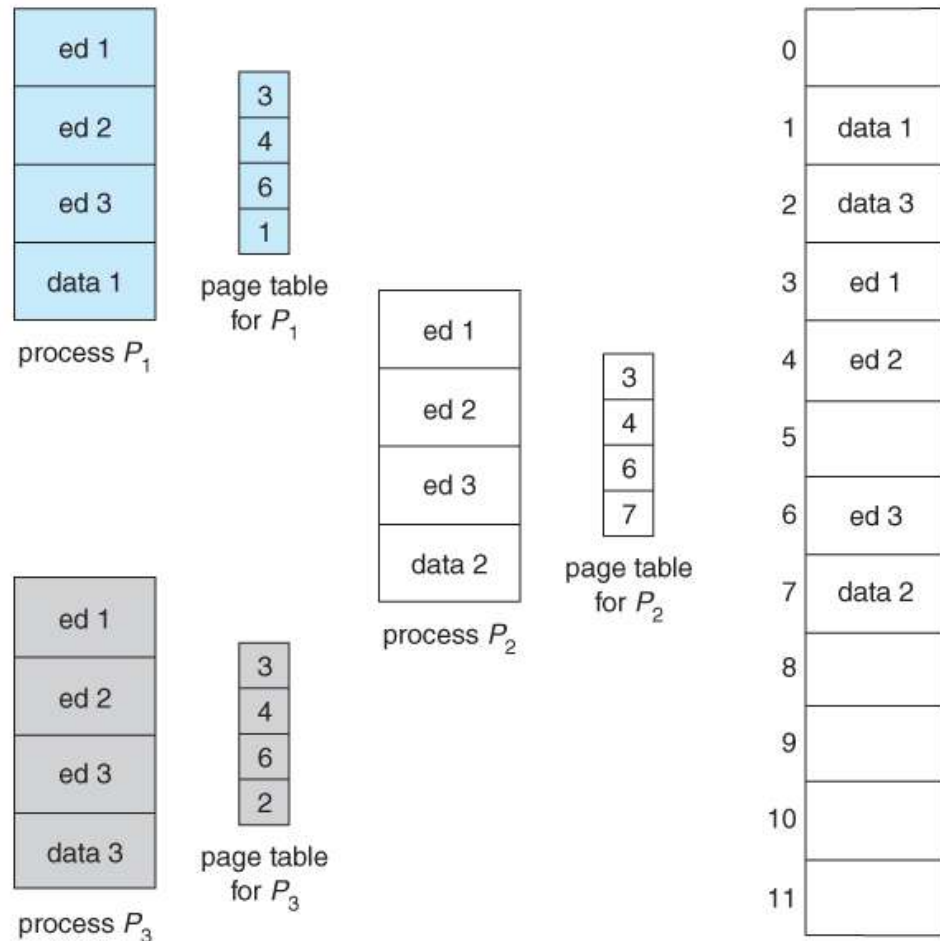
- Only if code is **reentrant!**
- It does not write to or change the code (i.e., it is non self-modifying)
- The code can be shared by multiple processes, as long as each has their own copy of the data and registers, including the instruction register

# Sharing Pages: Example



3 user processes are using the editor program ed

# Sharing Pages: Example



3 user processes are using the editor program ed

Only a single copy of the code of ed is actually loaded in main memory

# Paging: Summary

- A big improvement over **relocation**
- Eliminates the problem of external fragmentation and therefore the need for compaction
- Allows code sharing among processes, reducing memory footprint
- Enables processes to run when they are partially loaded

# Paging: Summary

- However, paging comes with its costs...
- Virtual/Physical address translation may be time consuming
- Hardware support like TLB cache is needed to make it efficient enough
- OS has to be inevitably more complex