Systems and Networking – Unit 1

B.Sc. in Applied Computer Science and Artificial Intelligence

2022-2023

SAPIENZA
UNIVERSITÀ DI ROMA

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A Quick Step Back: Segmentation

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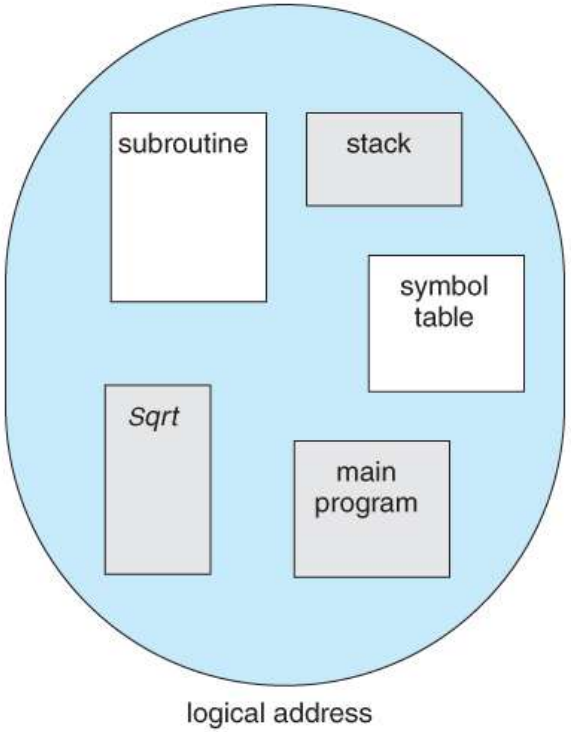
- Rather they think of memory divided in multiple segments, each dedicated to a specific use, such as code, data, stack, heap, etc.
- Memory segmentation supports this view by providing addresses with a segment number (mapped to a segment base address) and an offset from the beginning of that segment

Segmentation: Example

A C compiler generating 5 segments for the user code, library code, global (static) variables, the stack, and the heap



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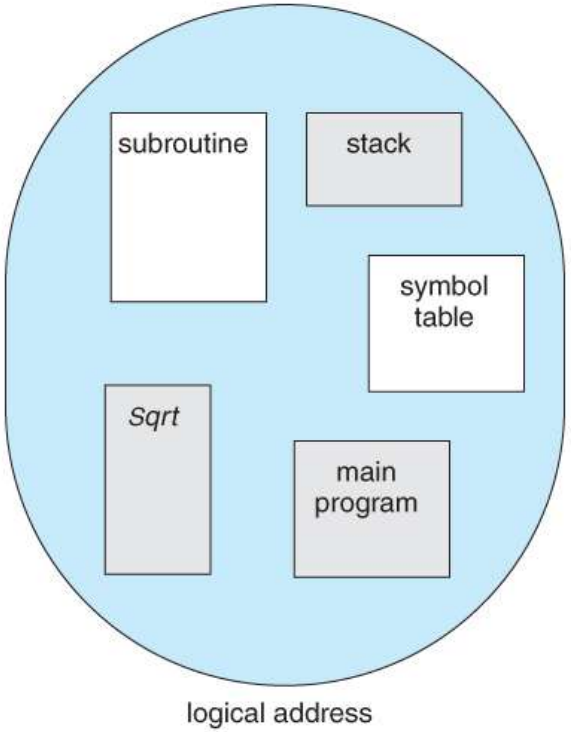
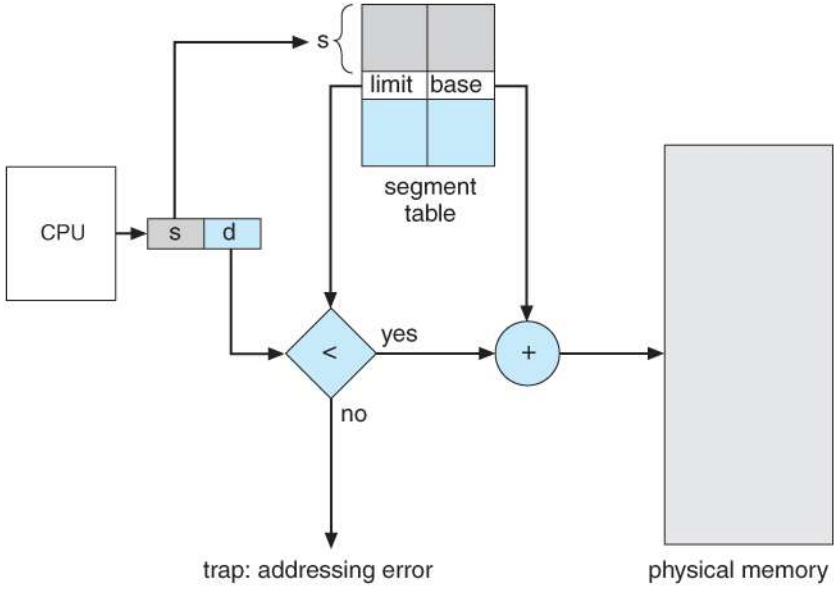


The compiler generates addresses identifying segments and offset in those

Segmentation Hardware

A segment table maps segment-offset addresses to physical addresses, and simultaneously checks for invalid addresses, using a system similar to the page tables and relocation base registers discussed previously



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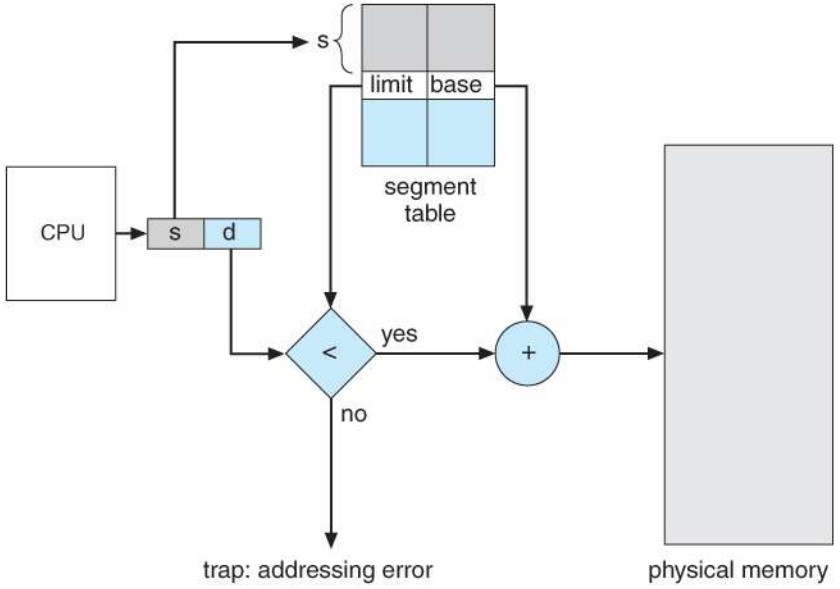

Note that we came back to the assumption that each segment is kept in contiguous memory and may be of different size…

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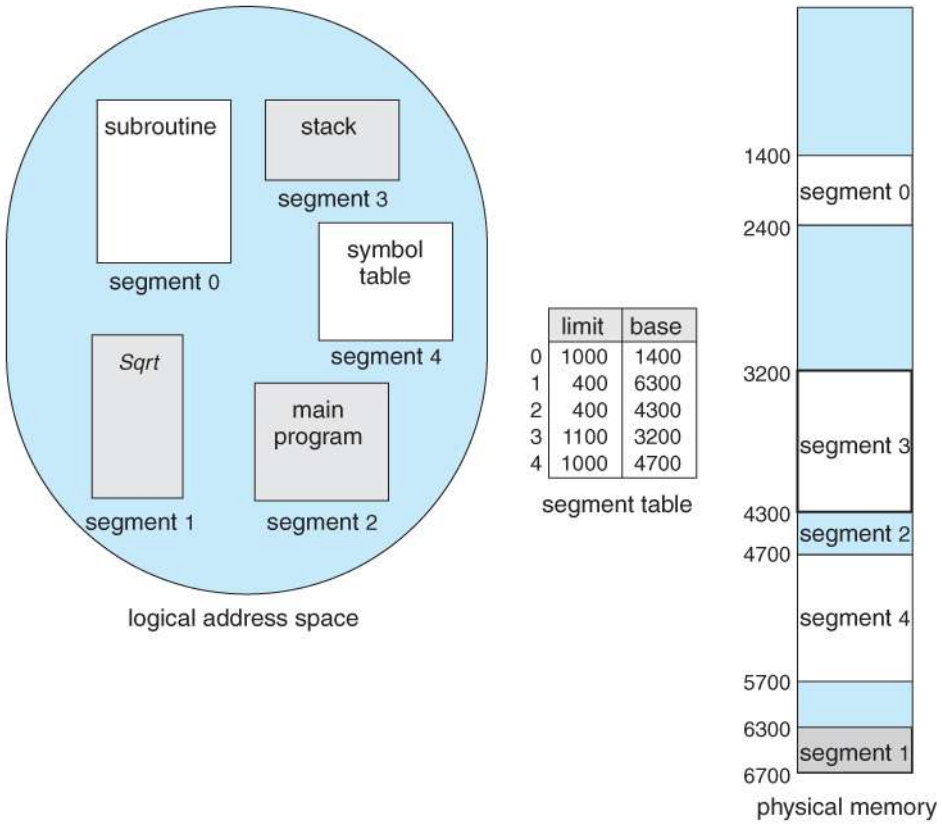

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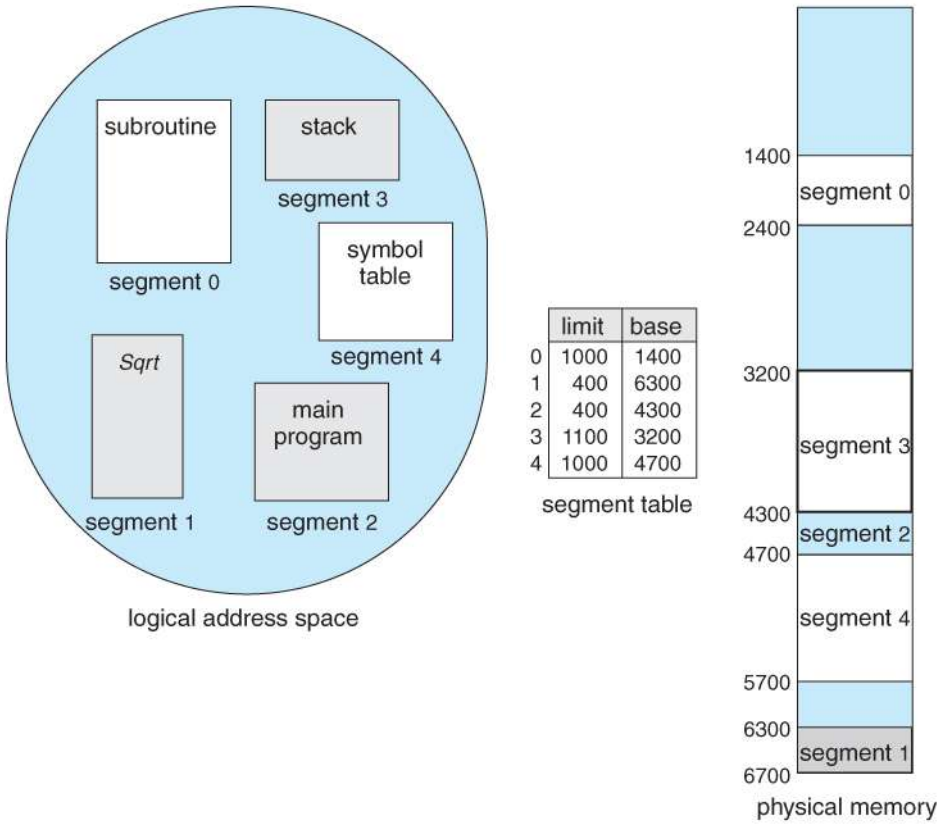

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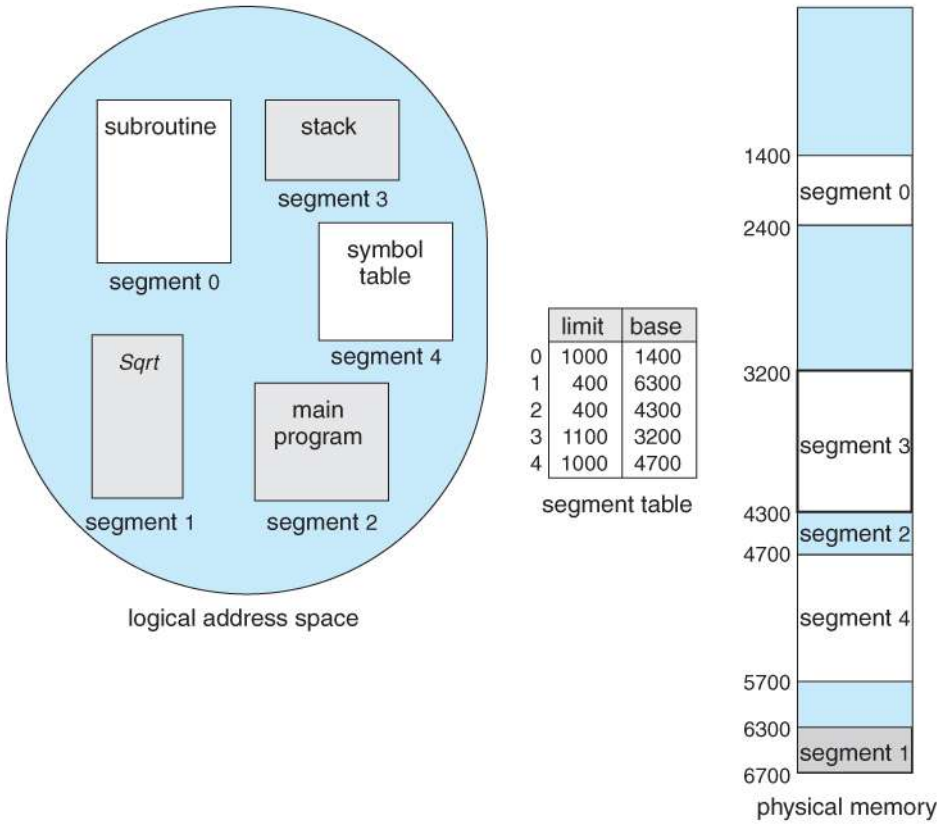

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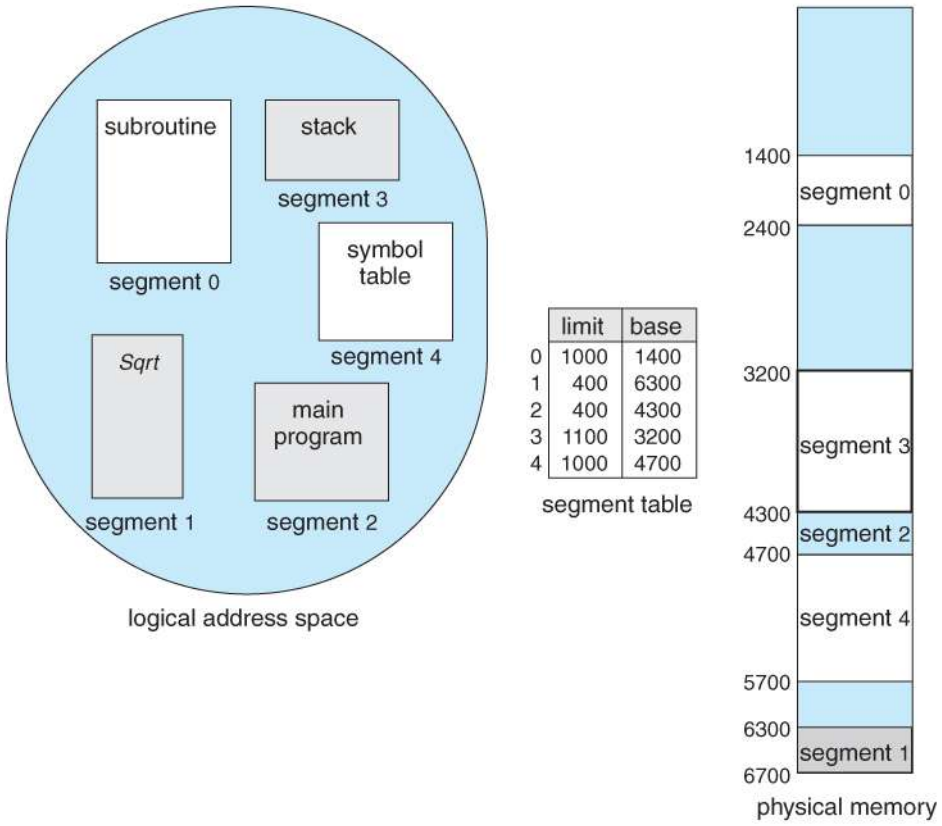

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Segment Table, instead, must store a very limited amount of segments per process (3÷5)

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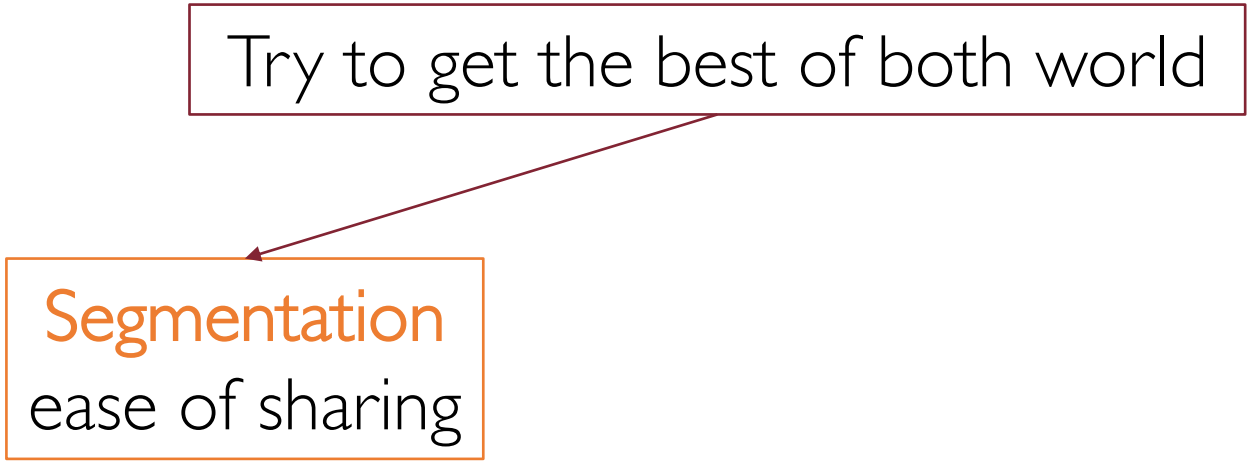
- Additional HW (like TLB cache) might be needed if programs use many logical segments

Combine Segmentation with Paging

Try to get the best of both world

Combine Segmentation with Paging



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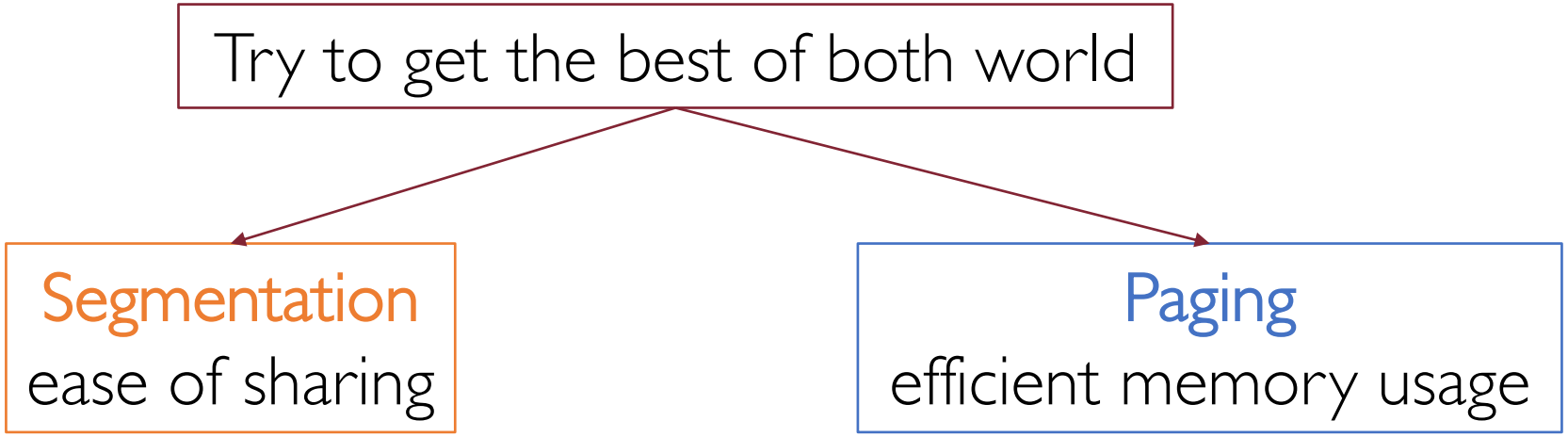

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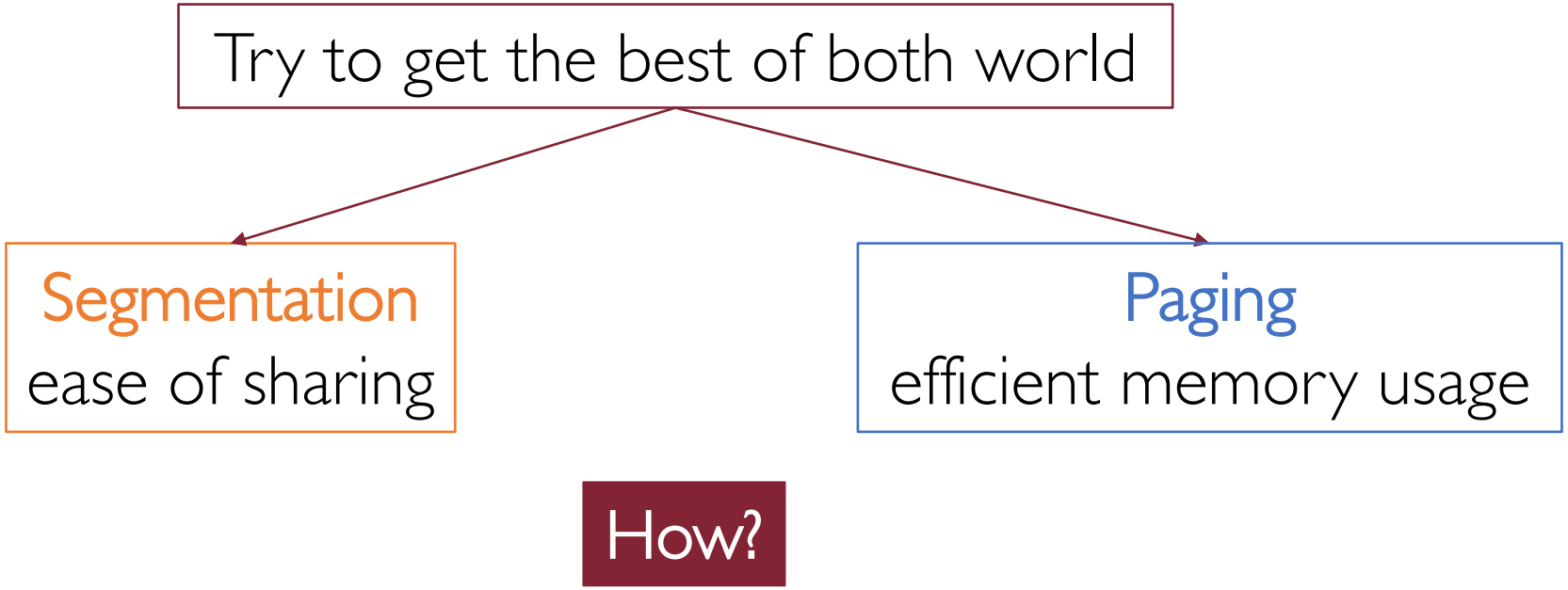

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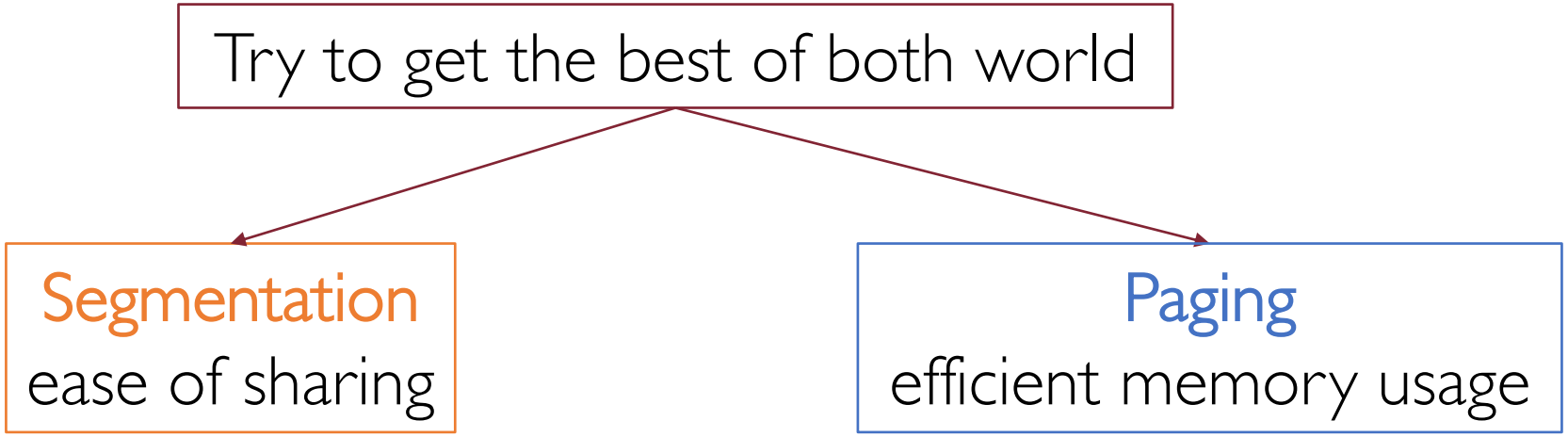

Apply paging to segments!

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Map a logical segment onto multiple page frames

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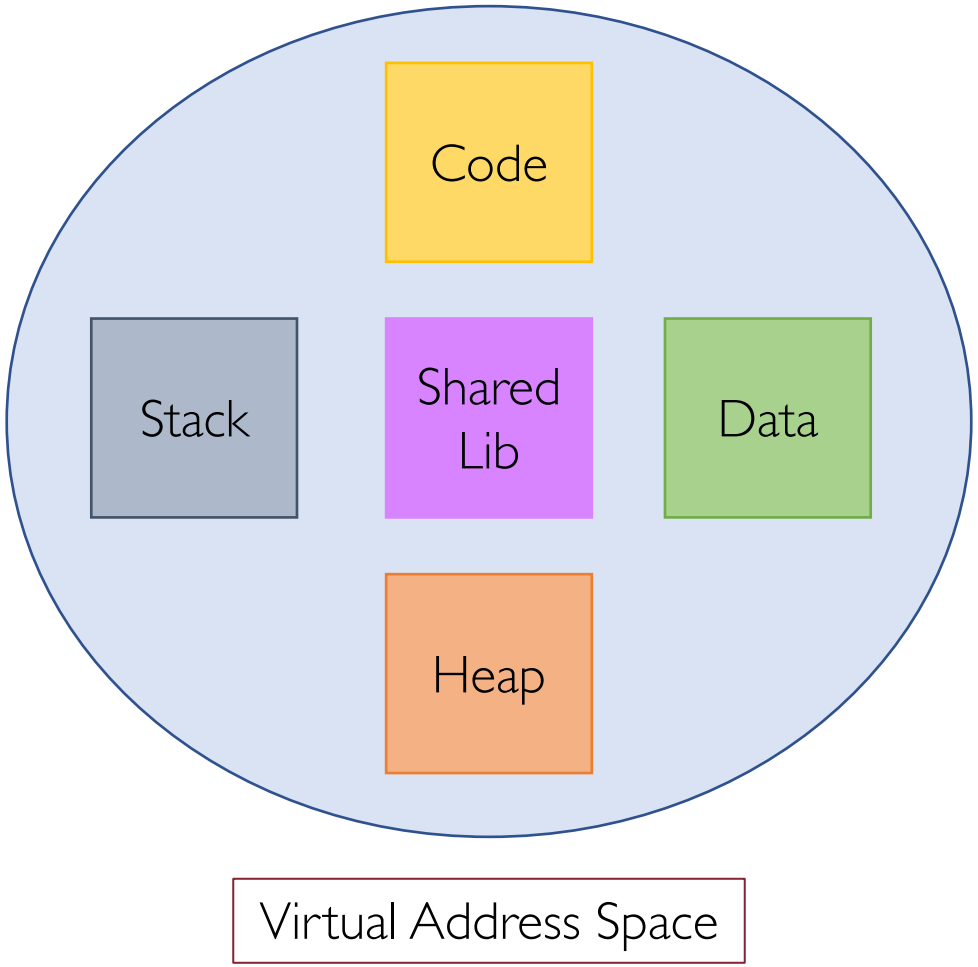

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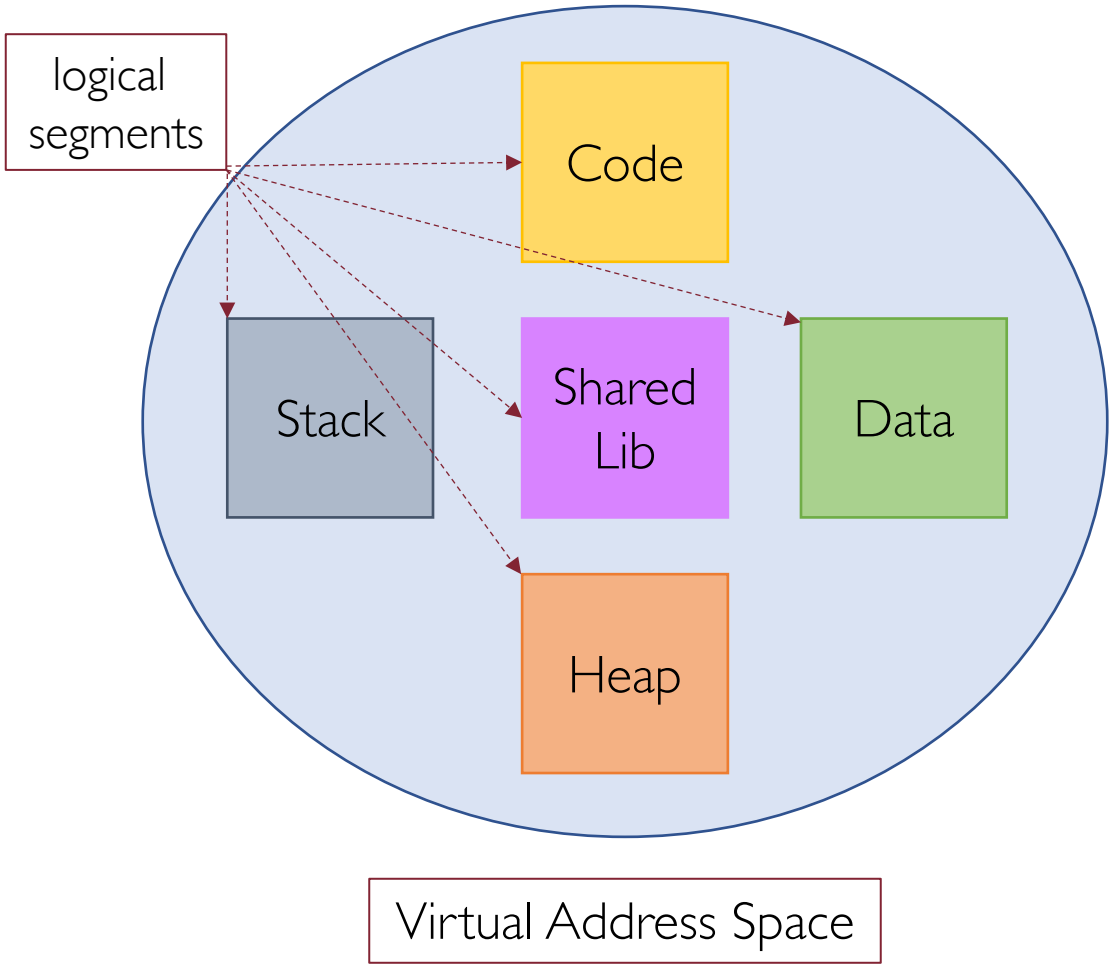

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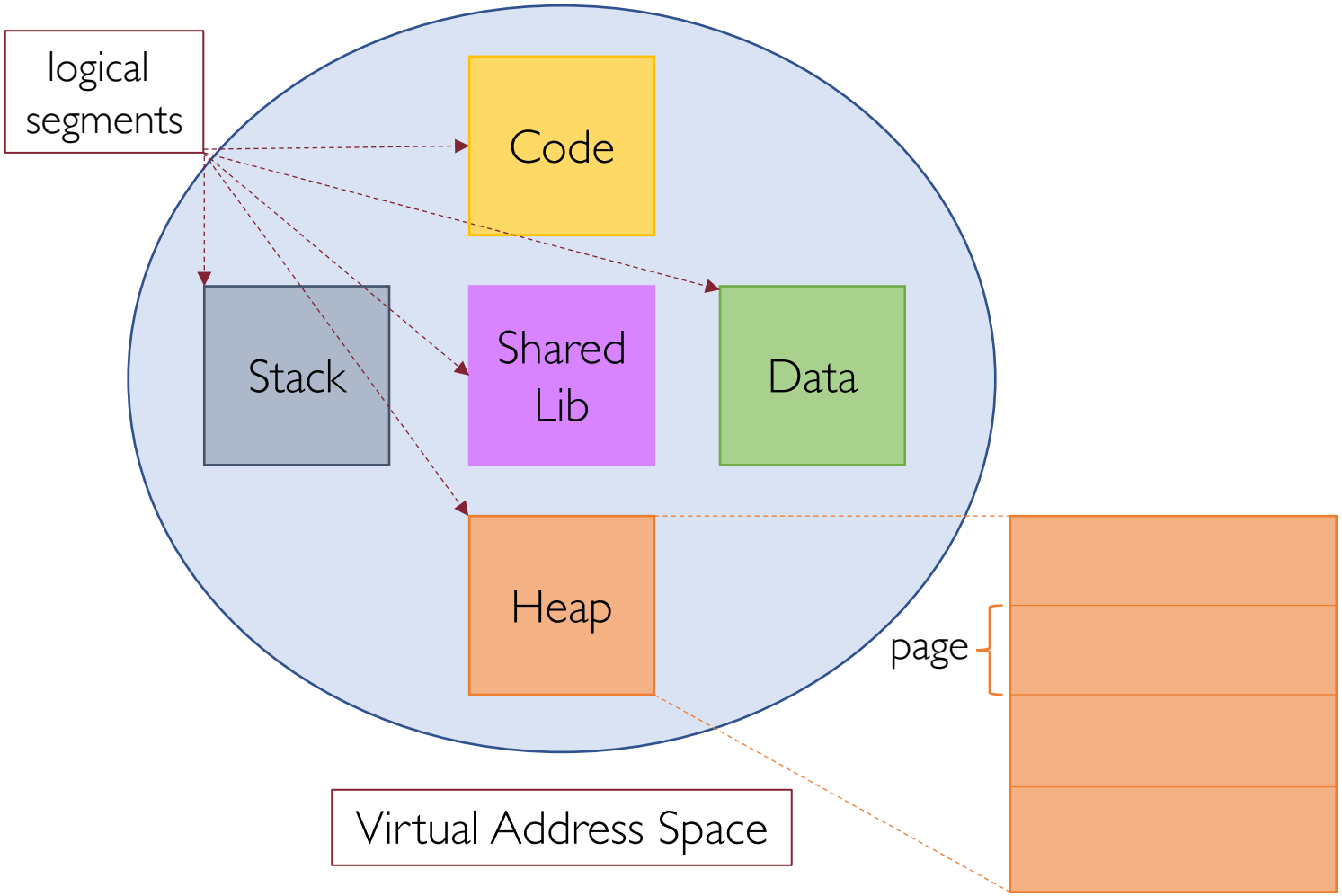

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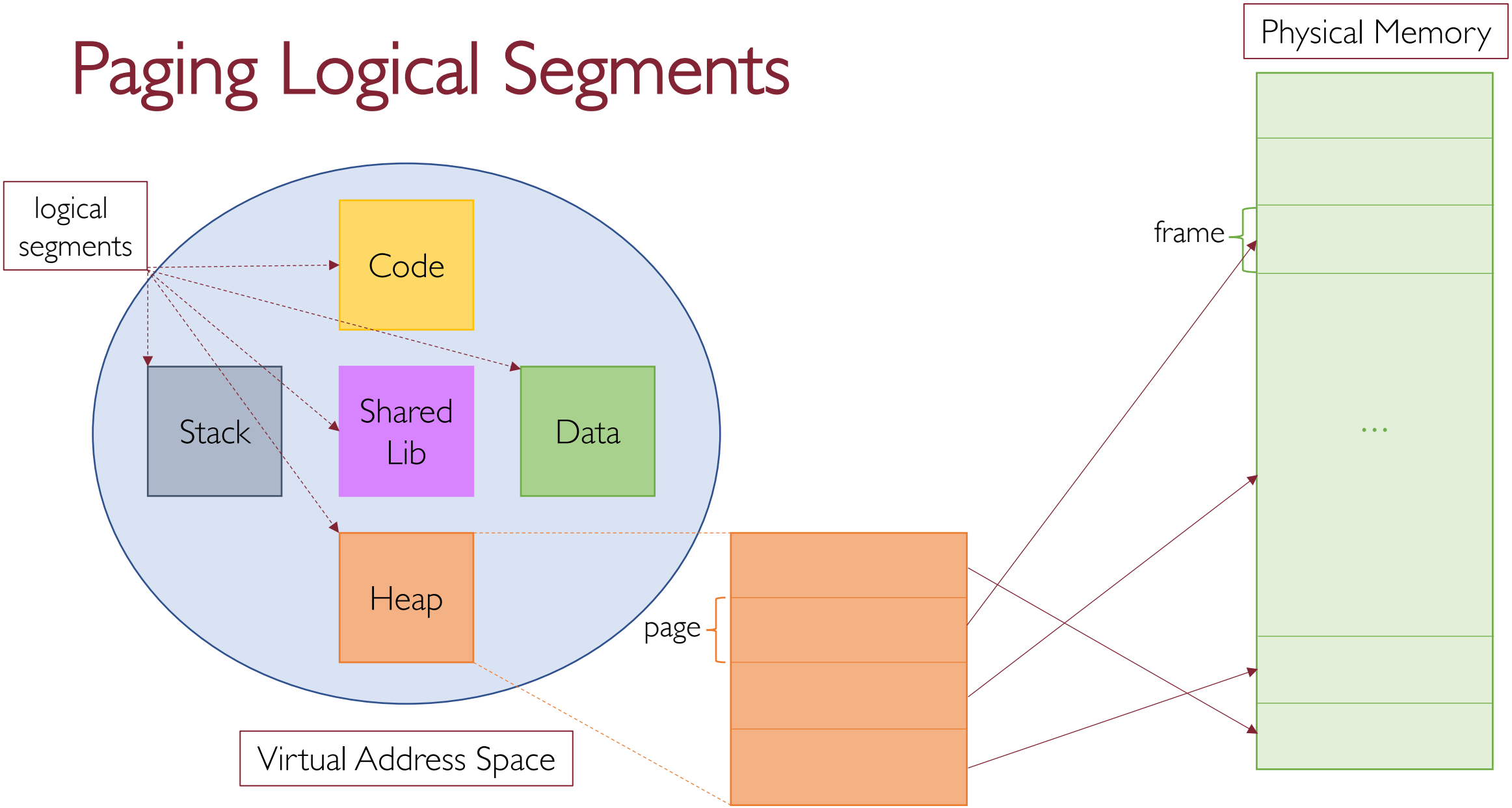

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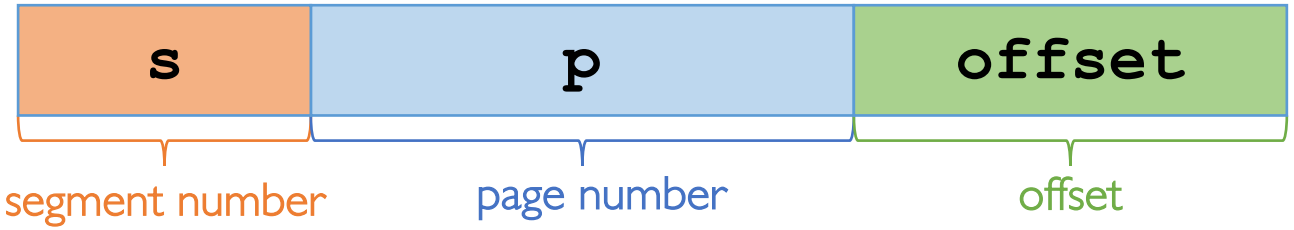

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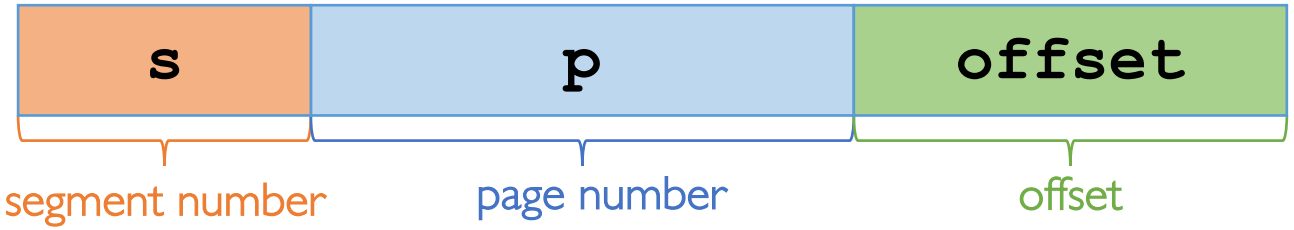

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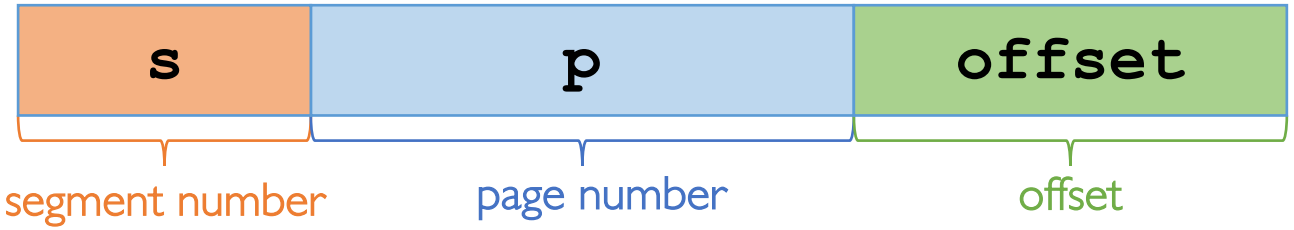

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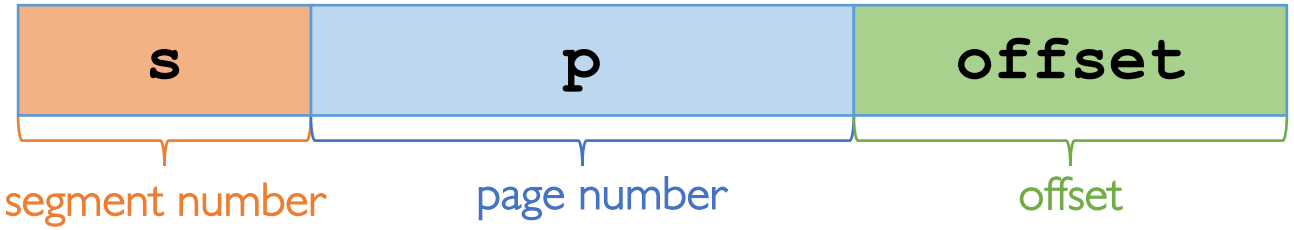

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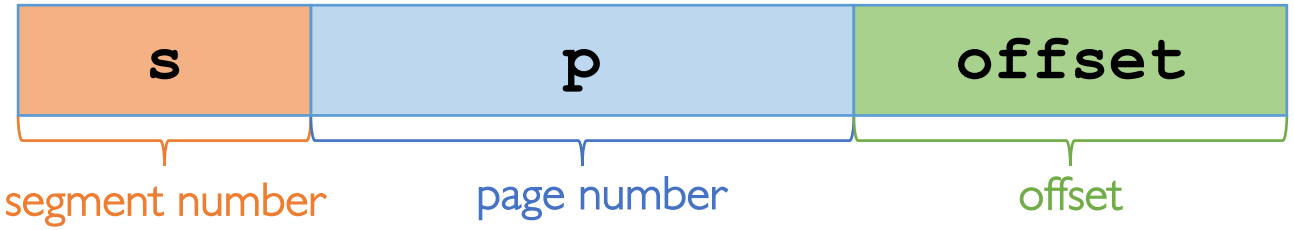

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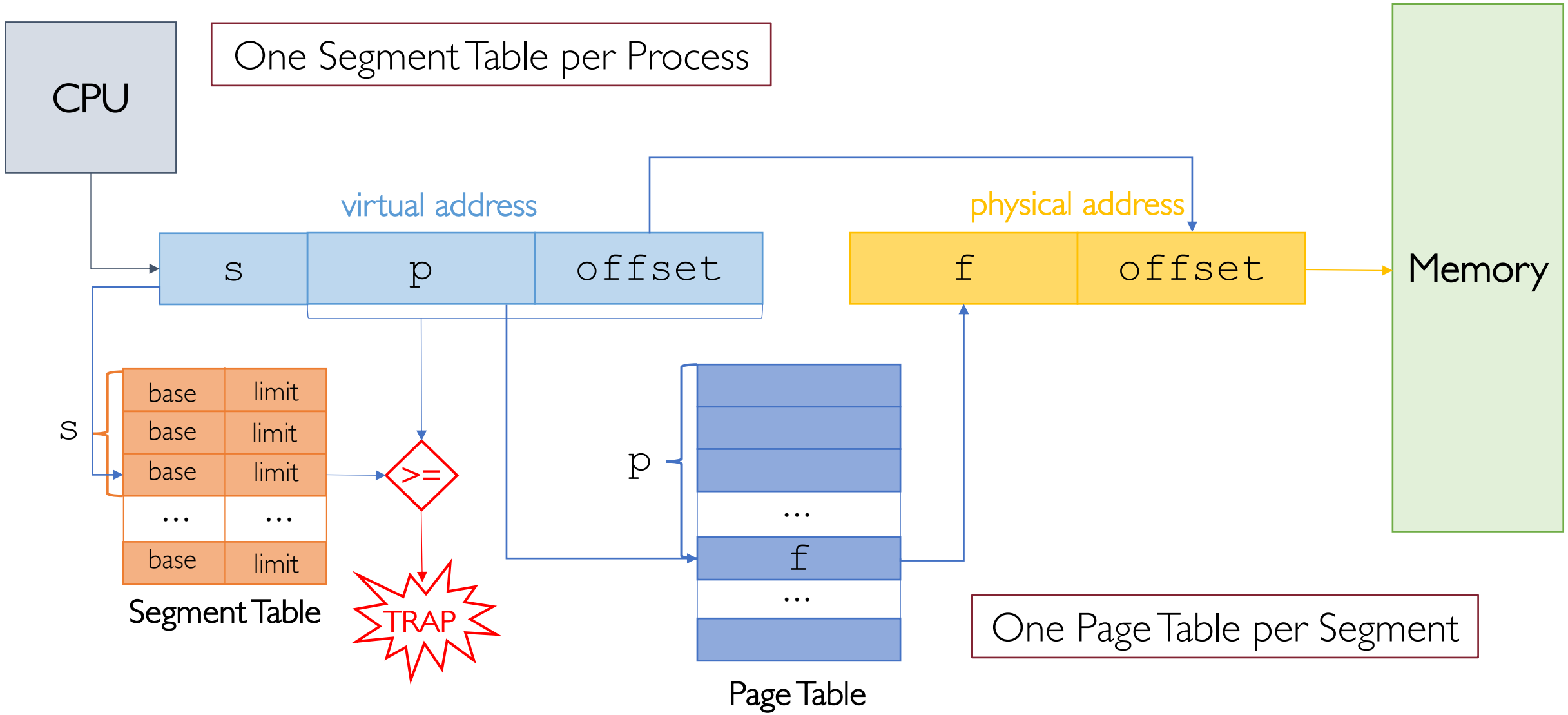

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Slower but more flexible

Segmented Paging Hardware: Practical Example 3

Suppose a physical memory of 1024 addressable words (assuming 1 word = 1 byte)

Frame size is 64 words (i.e., 64 bytes)

Page table size (i.e., number of entries) is thus 1024 bytes/64 bytes per frame = 16

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3 bits to address 8 logical segments (s)

4 bits to address 16 entries of the page table

6 bits to address 64 individual words (i.e., bytes) within each page

13 bits (virtual address) vs. 10 bits (physical address)

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- Even more flexible!

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More advanced paging structures are needed!

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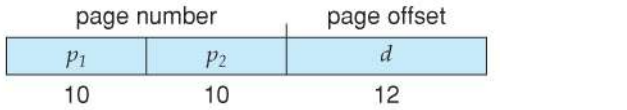

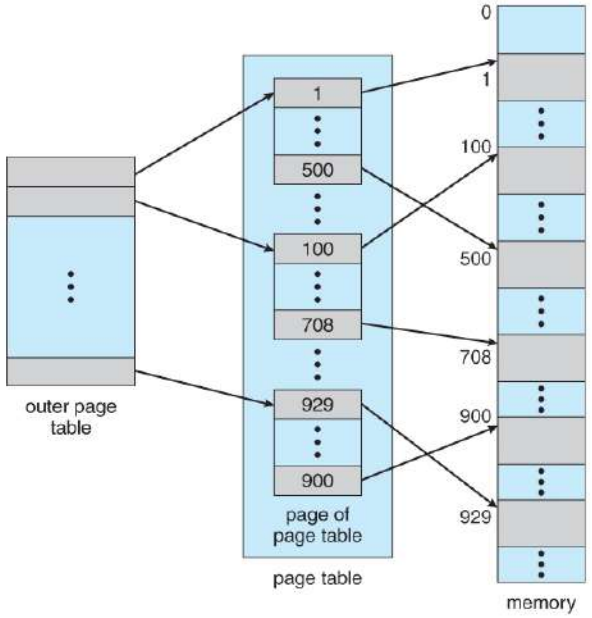

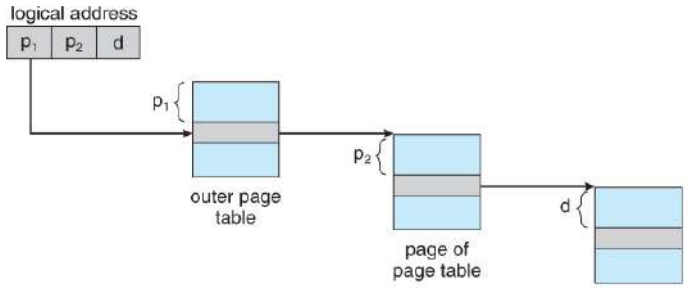

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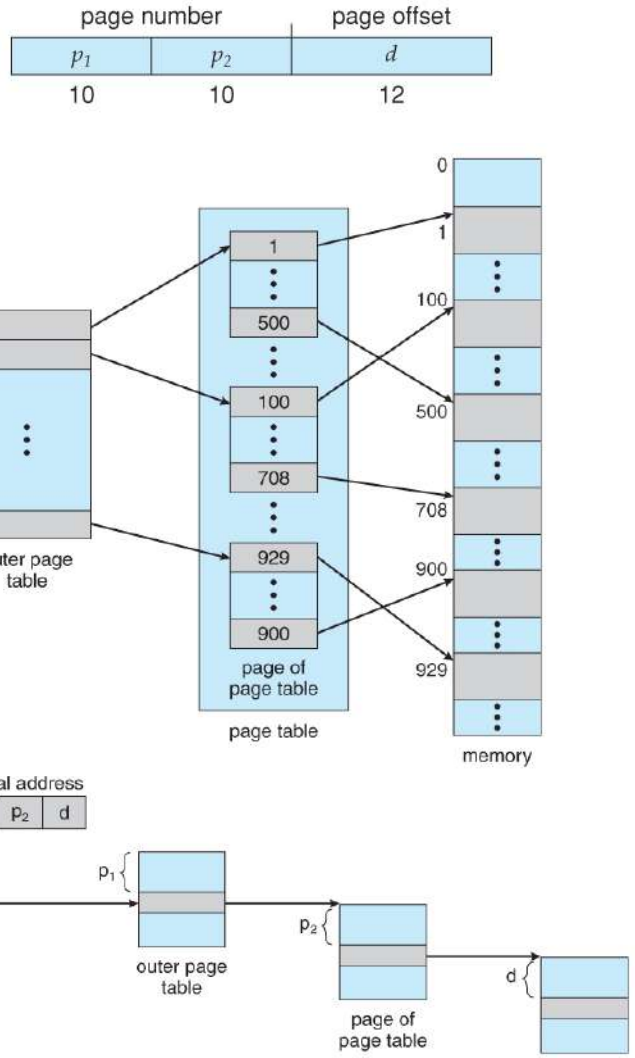

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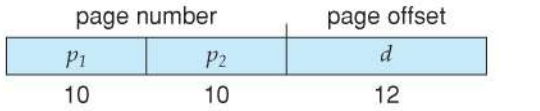

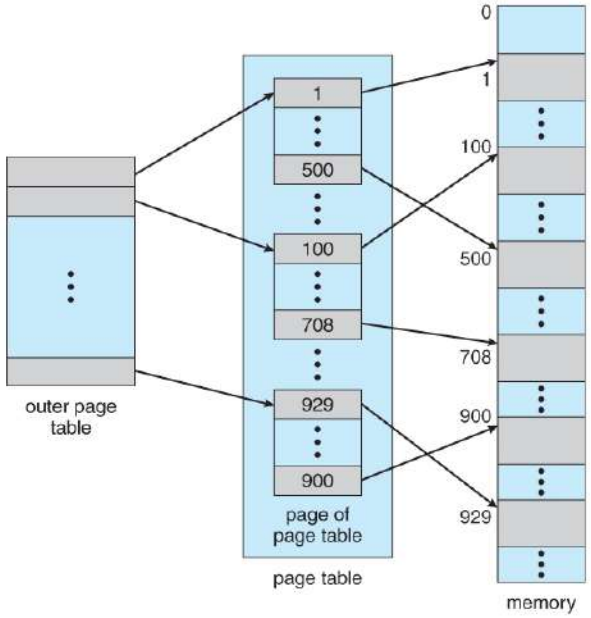

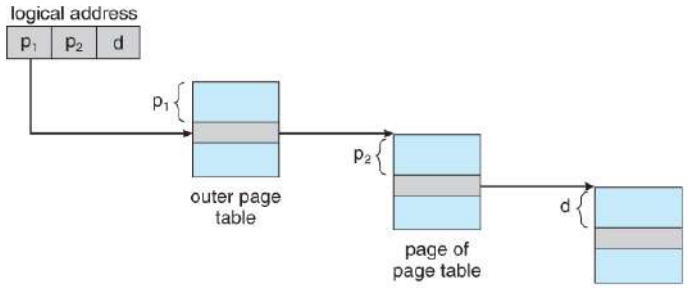

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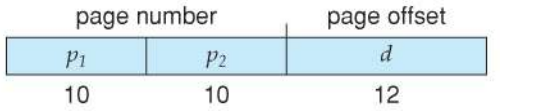

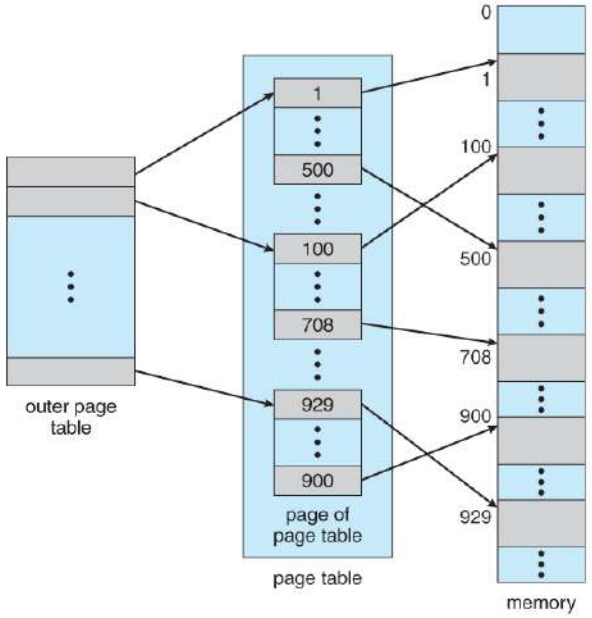

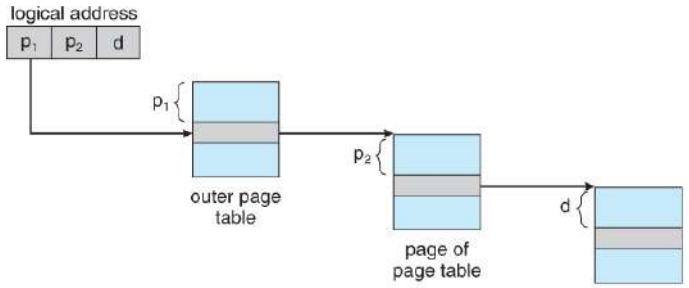

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The second 10 bits finds a specific entry in that inner page table, which maps to a frame in physical memory

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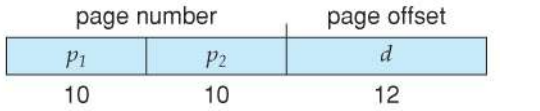
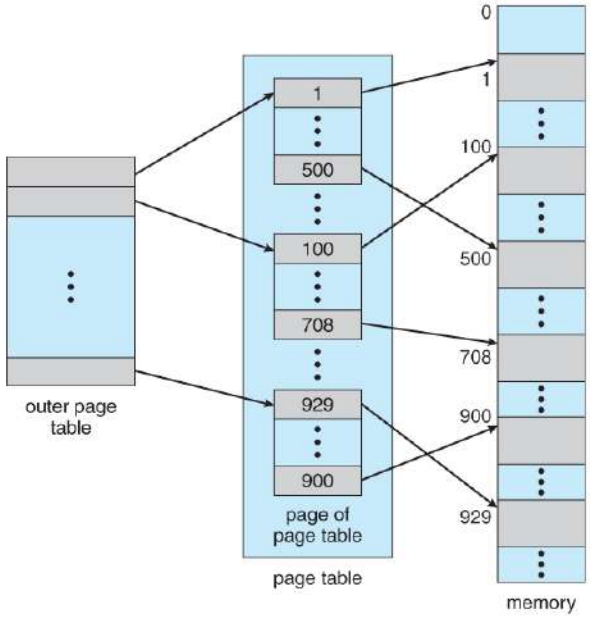
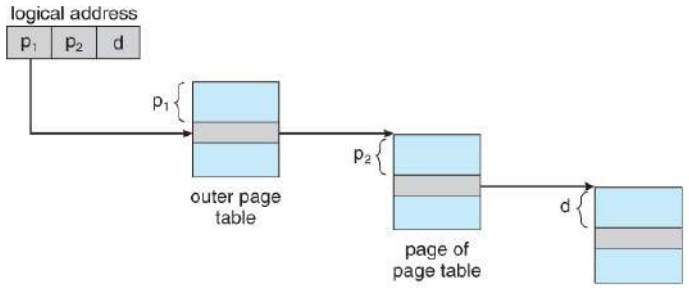






Let's page the page table!

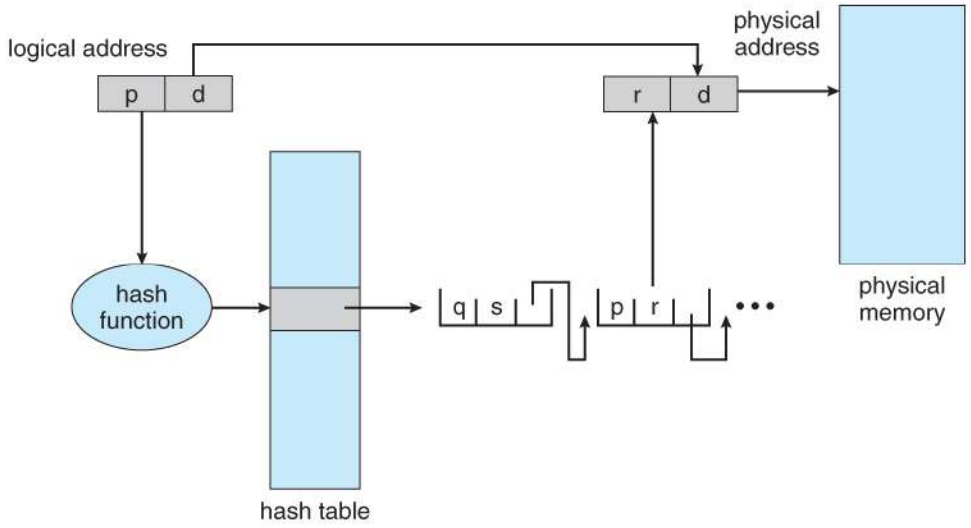
20-bit page number broken into 2 10-bit page numbers

The most significant 10 bits represent an entry in the outer page table, used to find one page of the inner page table

The second 10 bits finds a specific entry in that inner page table, which maps to a frame in physical memory

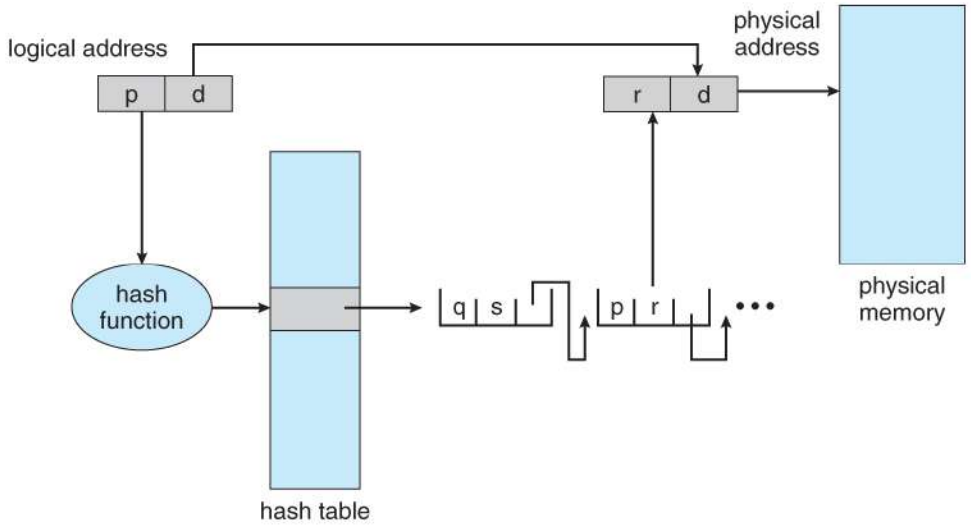
The remaining 12 bits of the 32-bit logical address are still the offset within the 4KiB frame

Advanced Paging: Hashed Page Table



Use hash tables to store highly sparse page tables

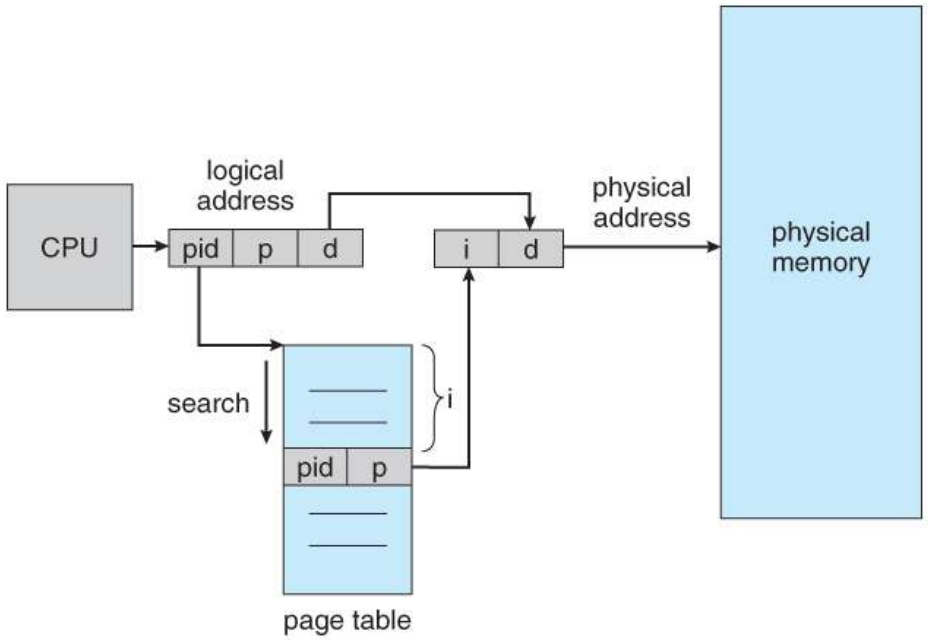
Advanced Paging: Hashed Page Table



Use hash tables to store highly sparse page tables

Indexing via hash function rather than integers

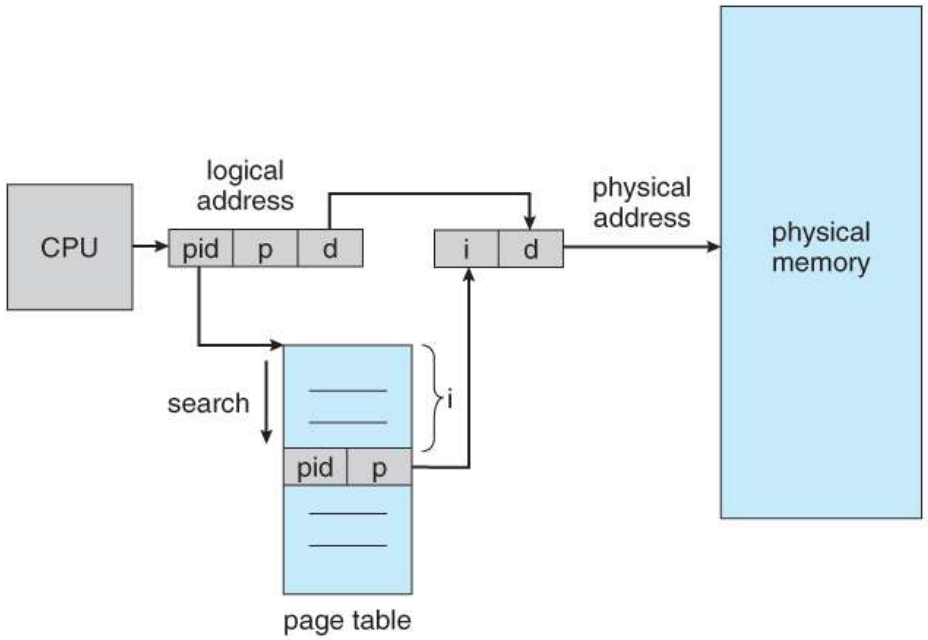
Advanced Paging: Inverted Page Table



An inverted page table lists all of the frames currently loaded in memory, for all processes

Instead of a table listing all of the pages for a particular process

Advanced Paging: Inverted Page Table



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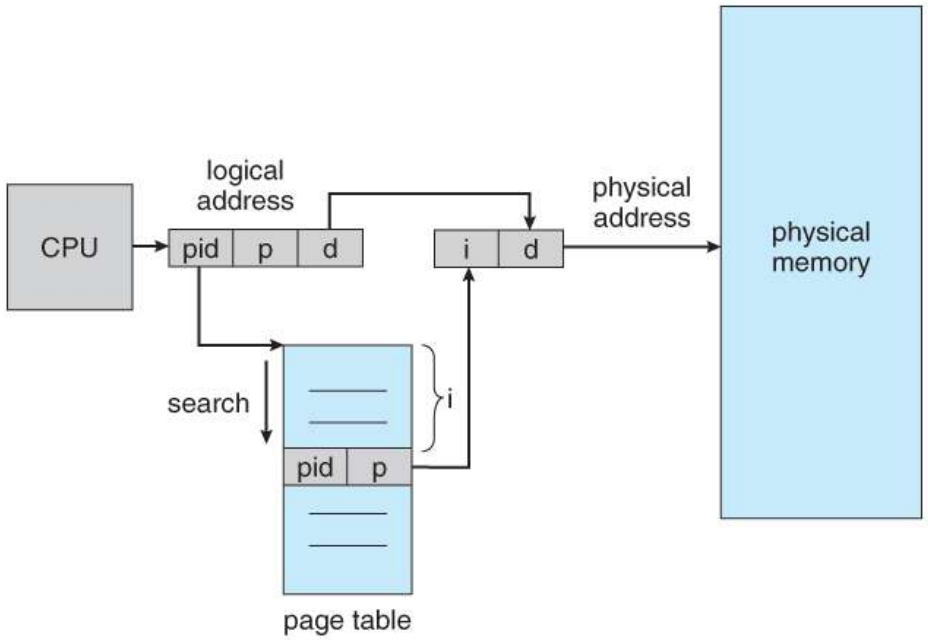
Hashing the table can help speedup the search process

Advanced Paging: Inverted Page Table



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Instead of a table listing all of the pages for a particular process

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Inverted page tables do not easily allow mapping multiple logical pages to a common physical frame (page sharing)

Each frame is mapped to *exactly* one process

Summary

- Relocation using base and limit registers
  - Simple yet inflexible

Summary

- Relocation using base and limit registers
  - Simple yet inflexible
- Segmentation
  - Compiler's logical view of memory presented to the OS
  - Segment tables tend to be small enough to be stored in registers
  - Contiguous memory allocation is expensive and complicated (first-fit, best-fit, or worst-fit)
  - Compaction is needed to solve external fragmentation

Summary

- Paging
  - Simplifies memory allocation by relaxing contiguous assumption
  - Each logical page can be allocated to any physical frame
  - Page tables can be extremely large

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- Paging
  - Simplifies memory allocation by relaxing contiguous assumption
  - Each logical page can be allocated to any physical frame
  - Page tables can be extremely large
- Segmentation + Paging
  - Only need to allocate as many page table entries an needed
  - Sharing either at the segment or at the page level
  - Might increase internal fragmentation over pure paging
  - 2 lookups per memory reference are needed