
STM32
CubeMX

1. Description

1.1. Project

Project Name	G431RB_Air_Quality
Board Name	NUCLEO-G431RB
Generated with:	STM32CubeMX 6.4.0
Date	02/16/2022

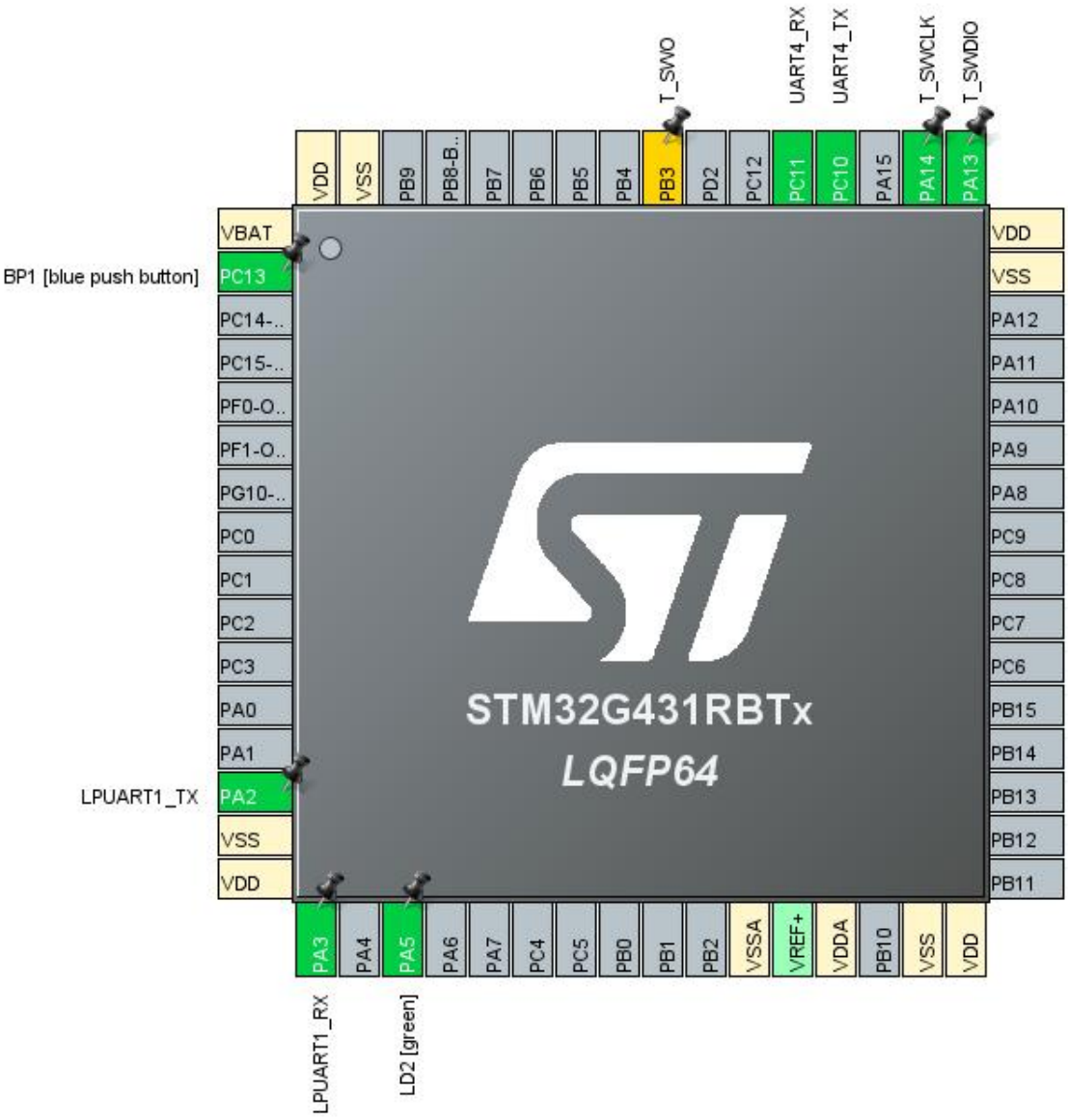
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G431RBTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration



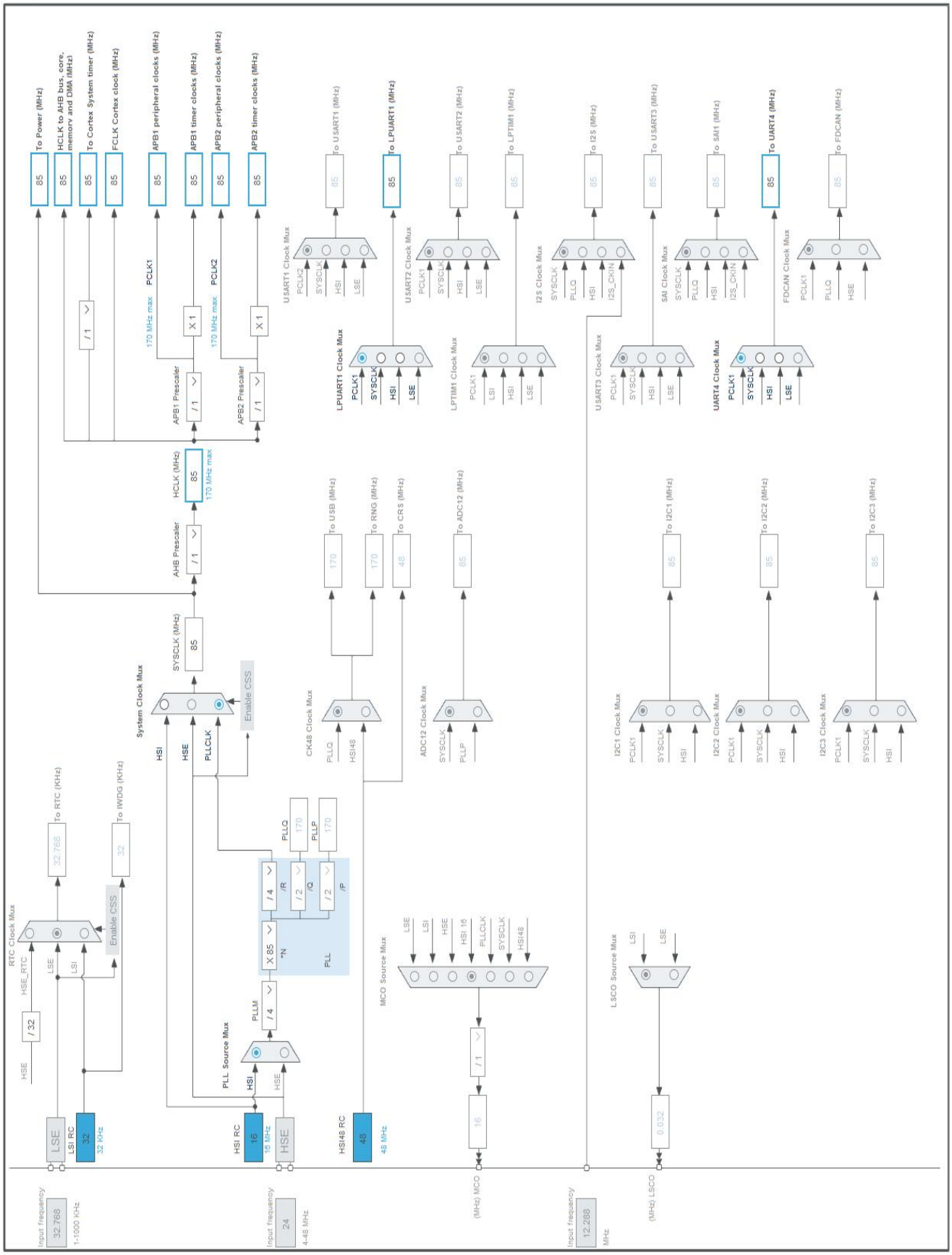
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	BP1 [blue push button]
14	PA2	I/O	LPUART1_TX	LPUART1_TX
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	LPUART1_RX	LPUART1_RX
19	PA5 *	I/O	GPIO_Output	LD2 [green]
27	VSSA	Power		
29	VDDA	Power		
31	VSS	Power		
32	VDD	Power		
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
50	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
52	PC10	I/O	UART4_TX	UART4_TX
53	PC11	I/O	UART4_RX	UART4_RX
56	PB3 **	I/O	SYS_JTDO-SWO	T_SWO
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	G431RB_Air_Quality
Project Folder	D:\GitDepots\G431RB_Air_Quality
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM1_Init	TIM1
4	MX_LPUART1_UART_Init	LPUART1
5	MX_UART4_Init	UART4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
MCU	STM32G431RBTx
Datasheet	DS12589_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

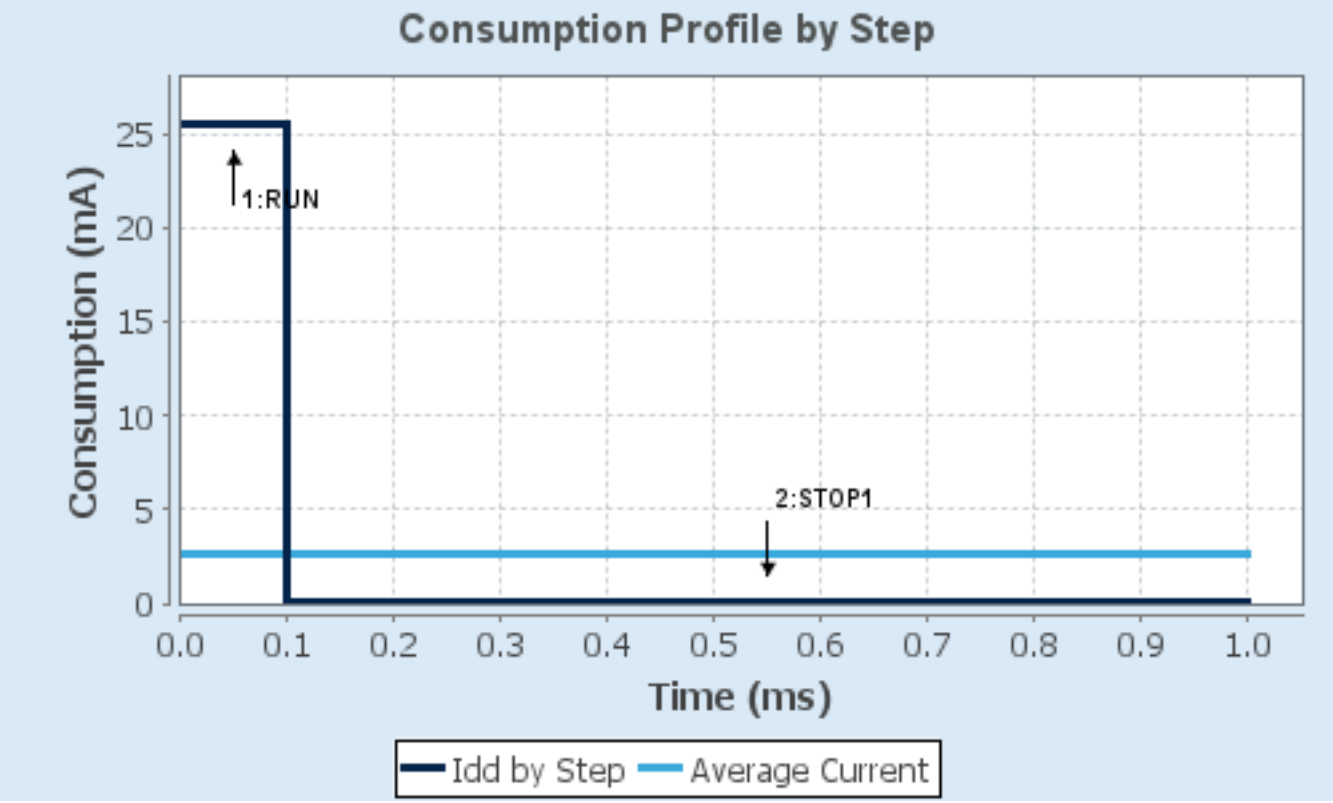
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	25.5 mA	59 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	125.03	129.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.6 mA
Battery Life	1 month, 23 days, 22 hours	Average DMIPS	212.5 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
25
20
15
10
5
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. LPUART1

Mode: Asynchronous

7.1.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.2. RCC

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100

LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.4. TIM1

Clock Source : Internal Clock

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**5000-1 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**8500-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

7.5. UART4

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None

Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	**half full configuration ***
Rxfifo Threshold	**half full configuration ***

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_TX
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_RX
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	T_SWCLK
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART4_TX
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART4_RX
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	T_SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	BP1 [blue push button]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green]

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 break interrupt and TIM15 global interrupt	true	0	0
TIM1 update interrupt and TIM16 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
UART4 global interrupt / UART4 wake-up interrupt through EXTI line 34	true	0	0
LPUART1 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 break interrupt and TIM15 global	false	true	true

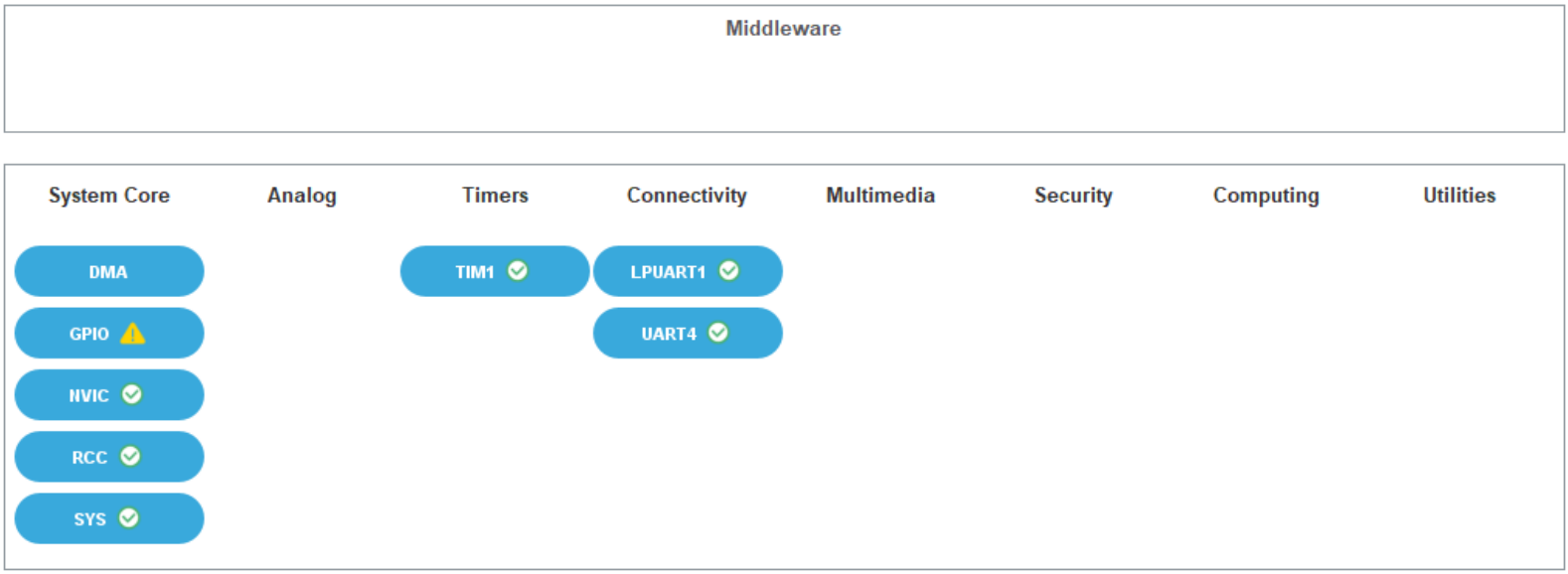
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
interrupt			
TIM1 update interrupt and TIM16 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
UART4 global interrupt / UART4 wake-up interrupt through EXTI line 34	false	true	true
LPUART1 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00507199.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00355726.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00502298.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442716.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442720.pdf

Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00605707.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00610467.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625282.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf