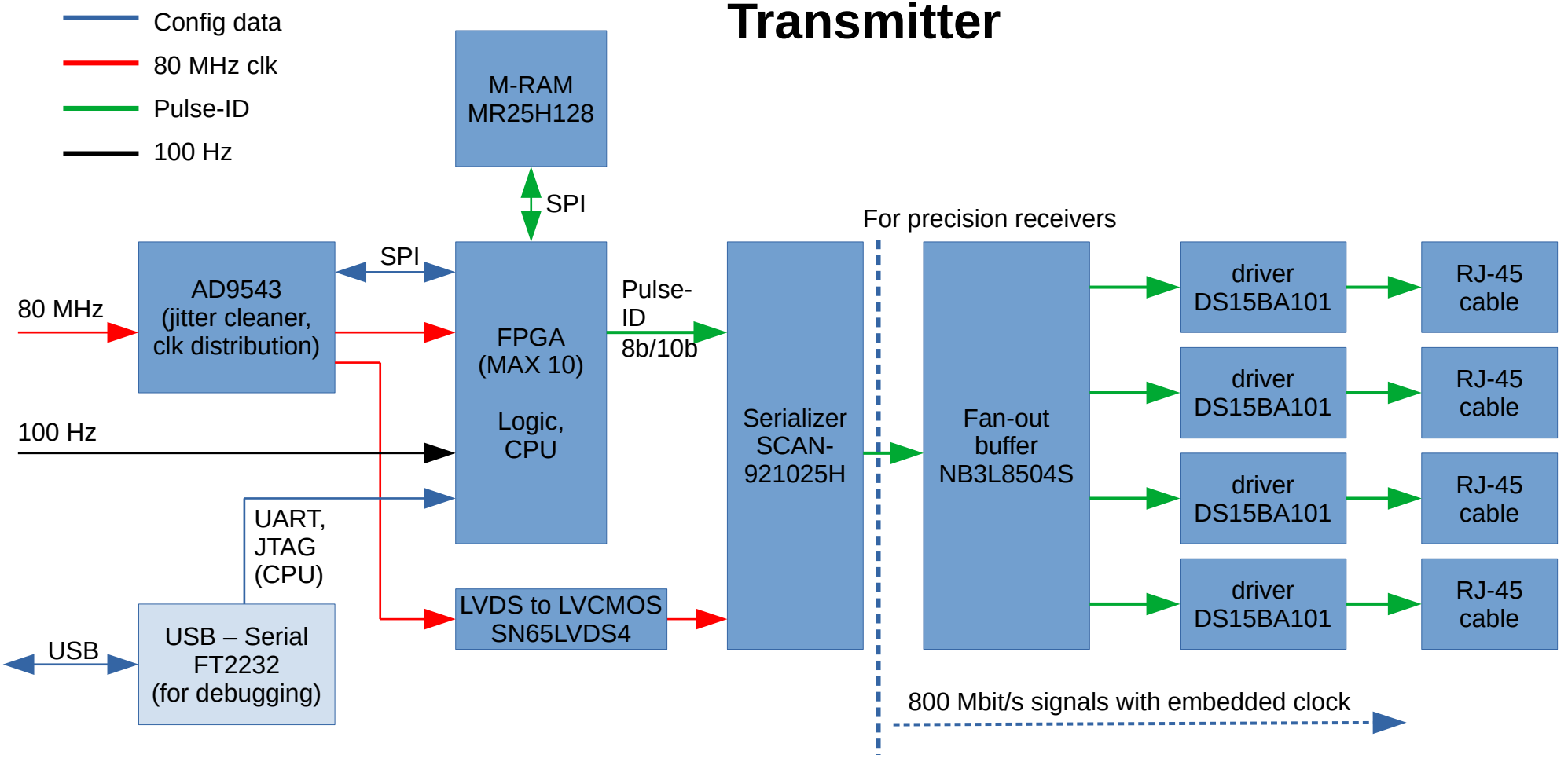
Block schematic

Low jitter time distribution system,
Y. Acremann, 2.2.2021

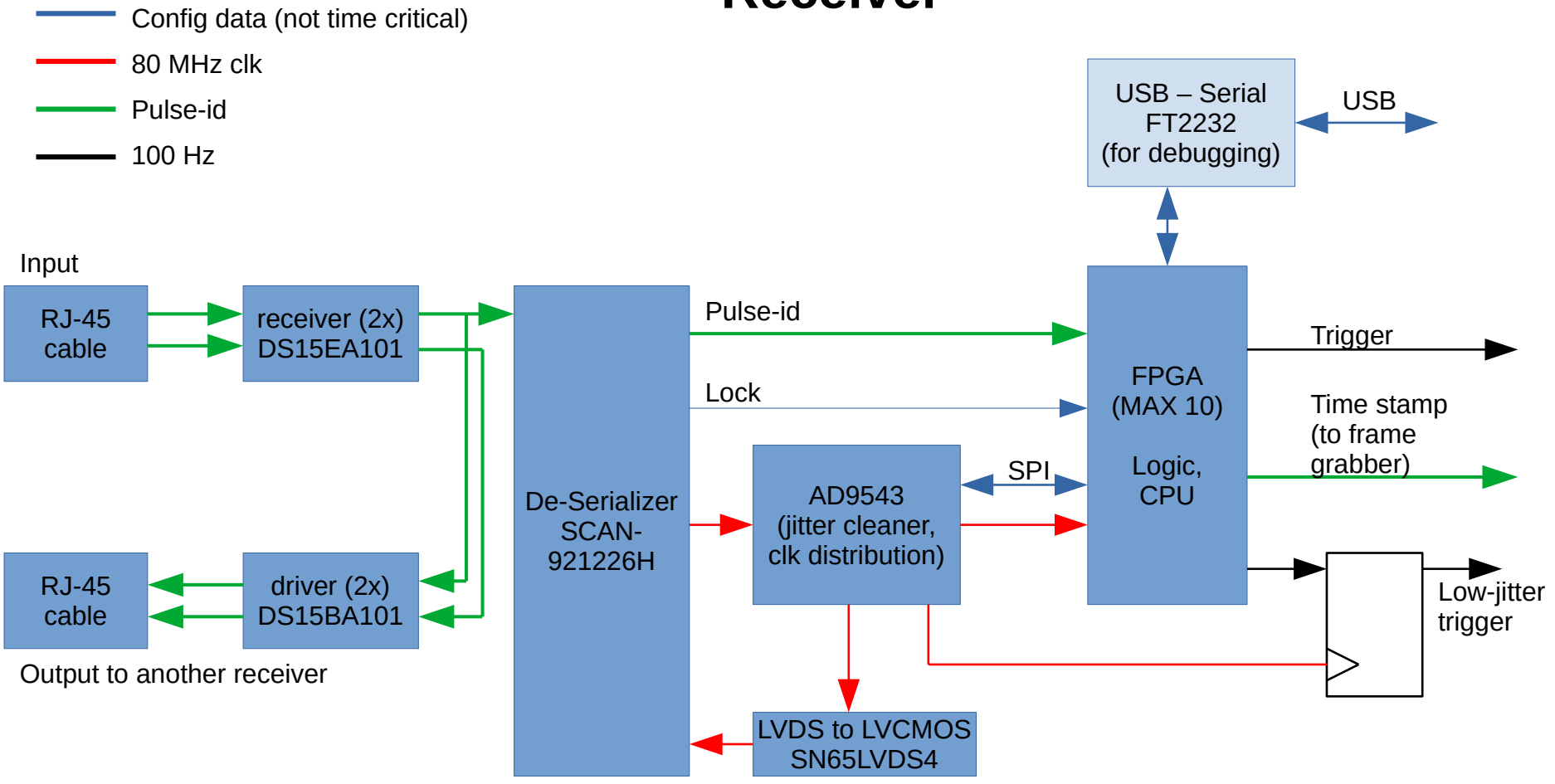
Transmitter



Concept

- Bit clock synchronized to the oscillator (80 MHz) for precision timing (estimate: 10 ps jitter)
- Jitter cleaner to get very clean clock signals from 80 MHz clock
- FPGA:
  - Counting of 100 Hz pulses (pulse-ID)
  - Control of the serializer and M-RAM
  - CPU for configuration of the jitter cleaner
- M-RAM: Stores the last pulse-ID (restore after power-loss)
- Distribution: RJ-45 cabes, max. length: 70m
- Encoding:
  - For simple receivers: 10 Mbit/s 8b/10b encoded data => jitter: 100 ns
  - For precision receivers: 800 Mbit/s 8b/10b encoded data (+ start bit)

Receiver


Config data (not time critical)
80 MHz clk
Pulse-id
100 Hz
USB – Serial
FT2232
(for debugging)
USB
Input
RJ-45
cable
receiver (2x)
DS15EA101
De-Serializer
SCAN-
921226H
Pulse-id
Lock
FPGA
(MAX 10)
Logic,
CPU
Trigger
Time stamp
(to frame
grabber)
SPI
AD9543
(jitter cleaner,
clk distribution)
RJ-45
cable
driver (2x)
DS15BA101
Output to another receiver
Low-jitter
trigger
LVDS to LVCMOS
SN65LVDS4

Additional features: Receiver

- Power over the RJ-45 cable to the receivers
- Trigger outputs:
  - Several independent outputs
  - Low jitter
  - Time steps in 1/(80 MHz)
- Output connector to connect another receiver