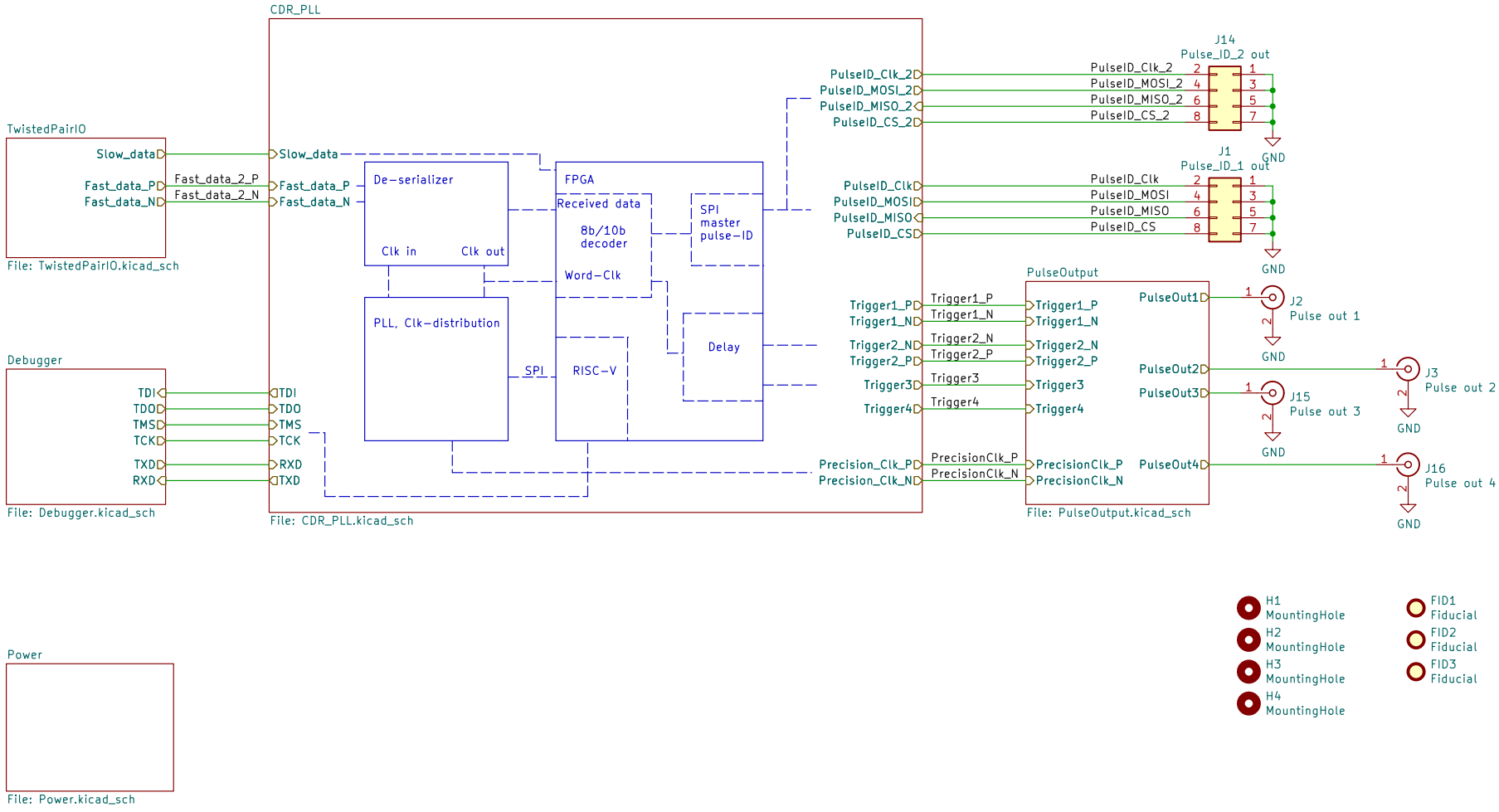
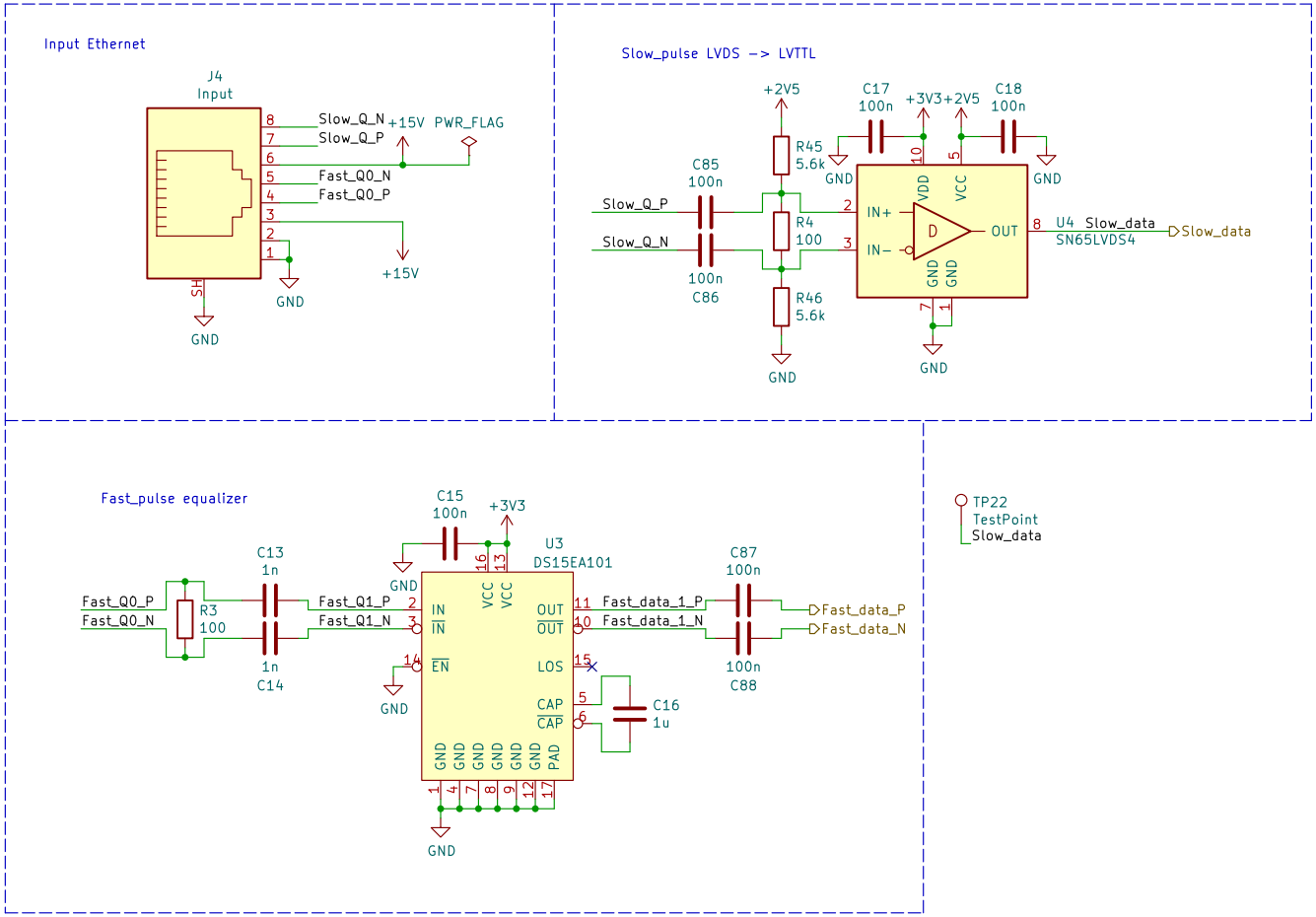
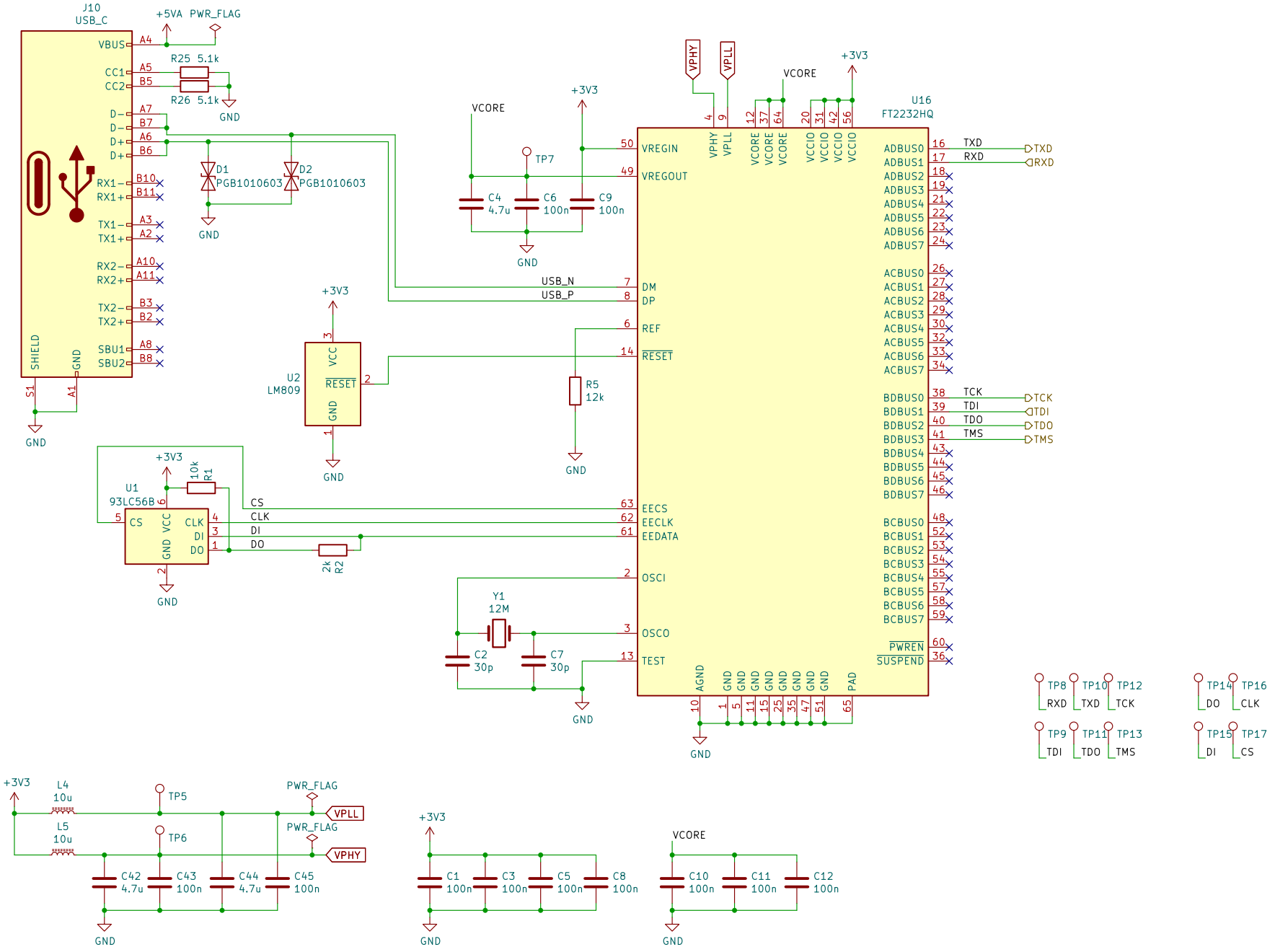
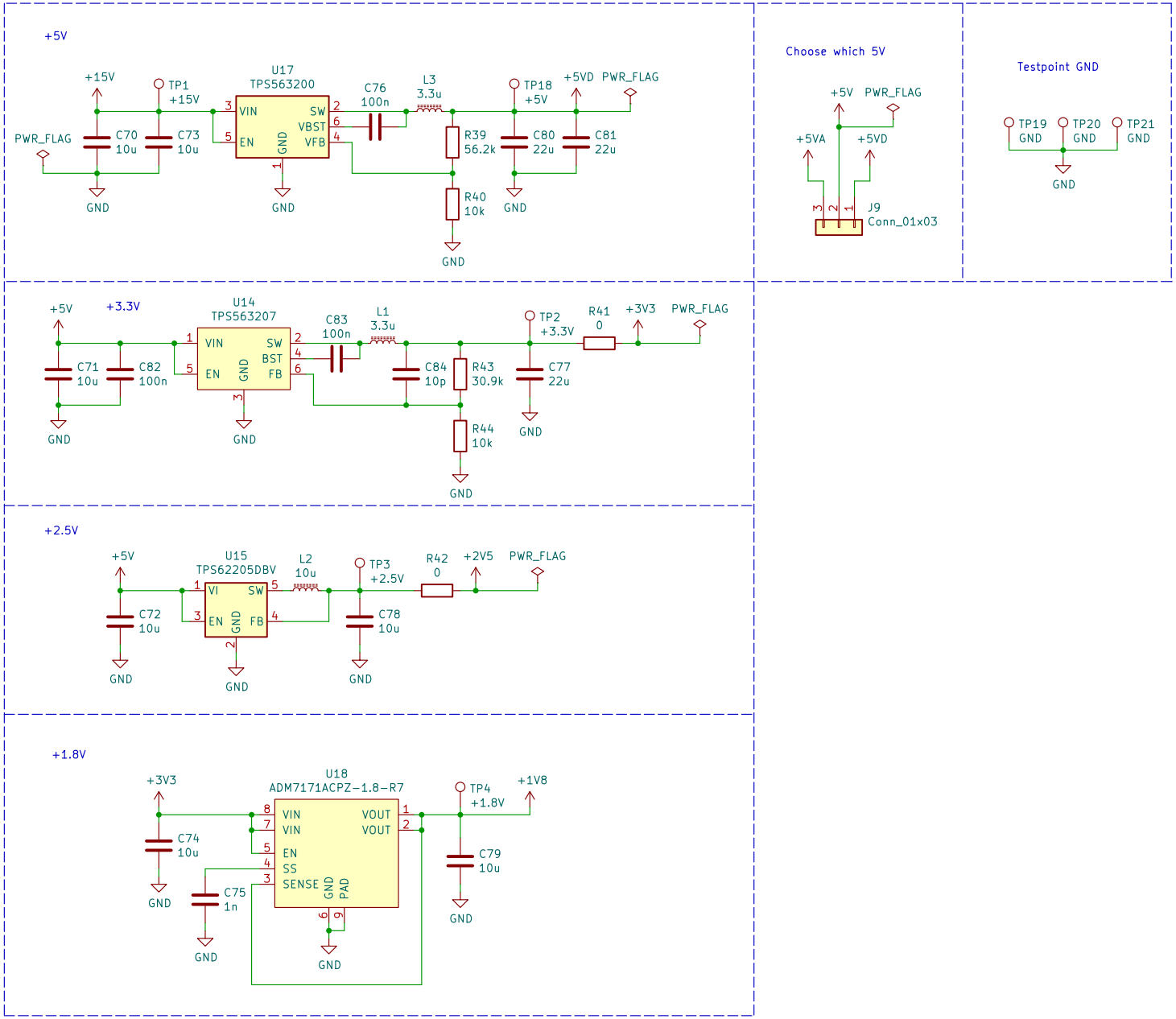
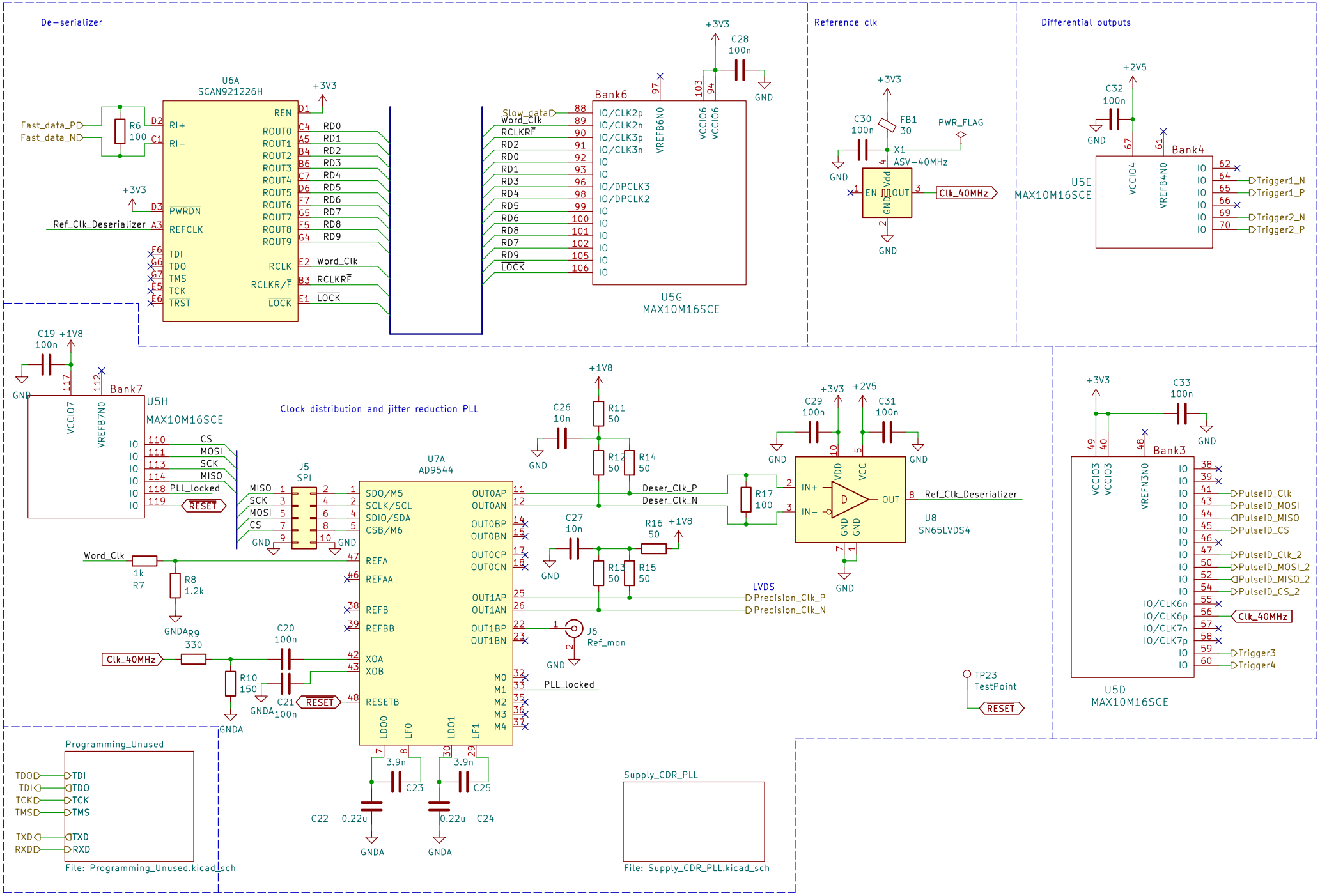
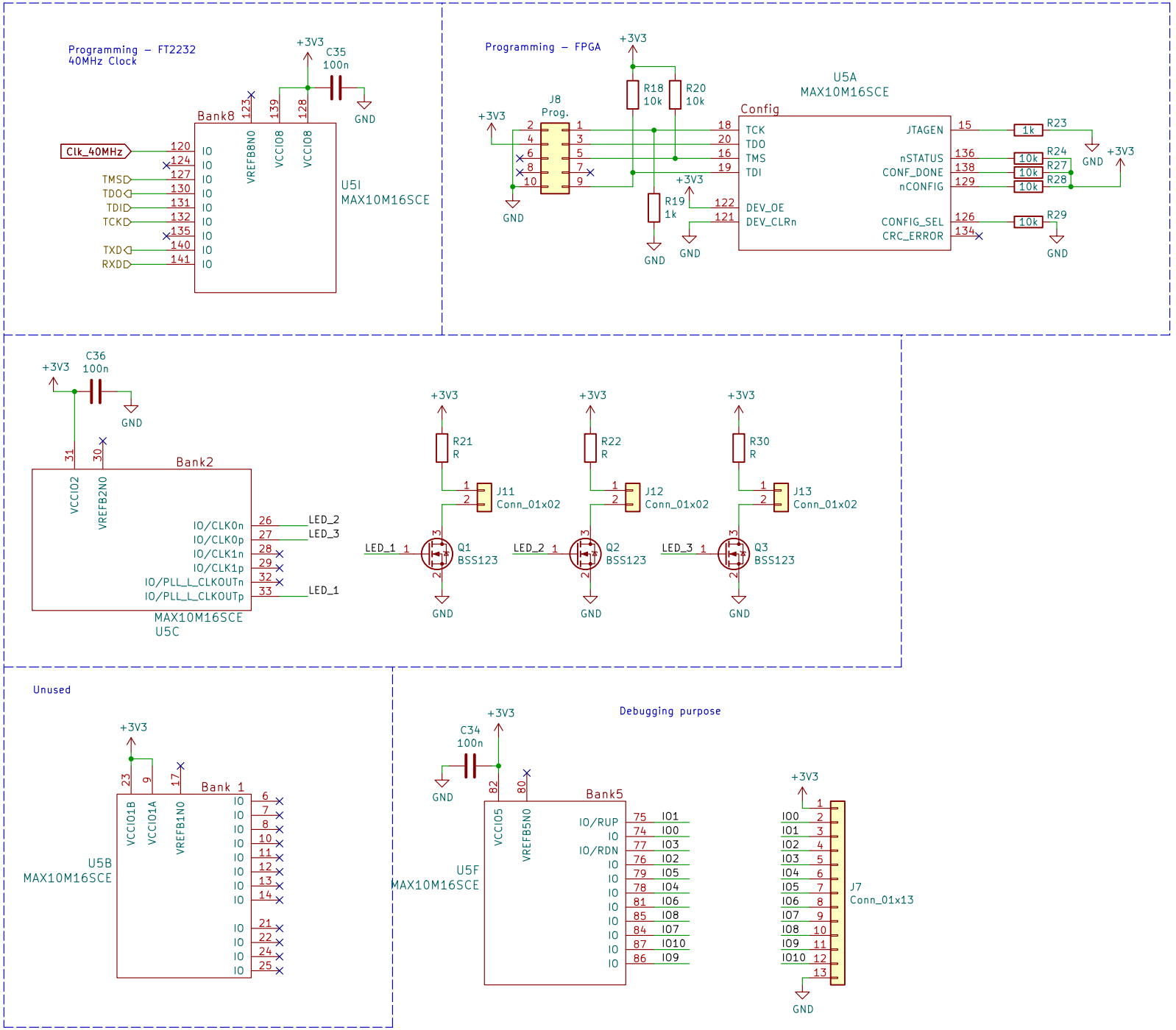

CDR_PLL
TwistedPairIO
Slow_data
Fast_data_P
Fast_data_N
Fast_data_2_P
Fast_data_2_N
File: TwistedPairIO.kicad_sch
Debugger
TDI
TDO
TMS
TCK
TXD
RXD
File: Debugger.kicad_sch
De-serializer
Clk in
Clk out
PLL, Clk-distribution
SPI
FPGA
Received data
8b/10b decoder
Word-Clk
RISC-V
SPI master pulse-ID
Delay
Precision_Clk_P
Precision_Clk_N
File: CDR_PLL.kicad_sch
PulseID_Clk_2
PulseID_MOSI_2
PulseID_MISO_2
PulseID_CS_2
PulseID_Clk
PulseID_MOSI
PulseID_MISO
PulseID_CS
Trigger1_P
Trigger1_N
Trigger2_N
Trigger2_P
Trigger3
Trigger4
PulseOutput
PulseOut1
PulseOut2
PulseOut3
PulseOut4
File: PulseOutput.kicad_sch
J14
Pulse_ID_2 out
J1
Pulse_ID_1 out
J2
Pulse out 1
J3
Pulse out 2
J15
Pulse out 3
J16
Pulse out 4
GND
Power
File: Power.kicad_sch
H1
MountingHole
H2
MountingHole
H3
MountingHole
H4
MountingHole
FID1
Fiducial
FID2
Fiducial
FID3
Fiducial

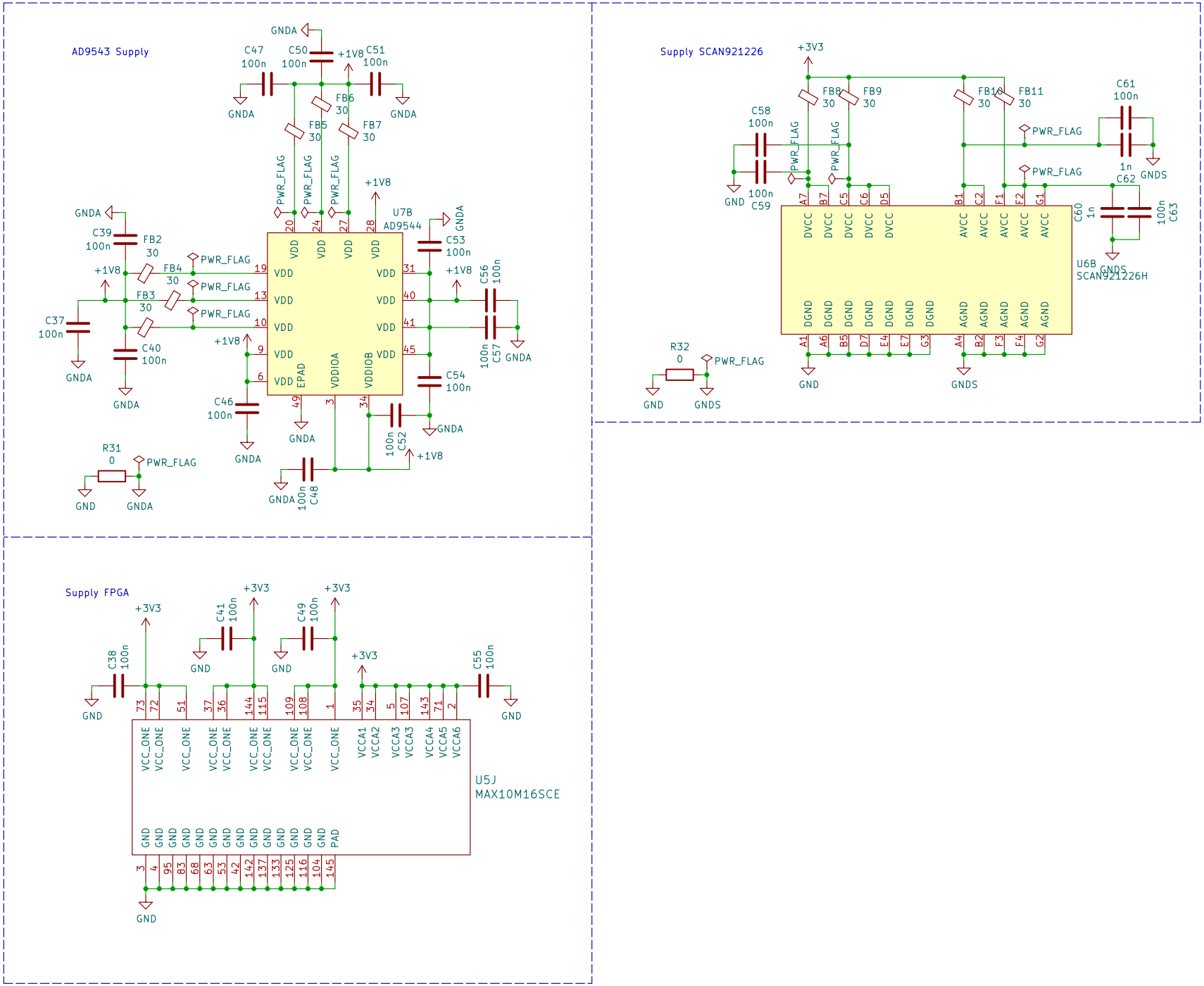

Input Ethernet
J4
Input
8
7
6
5
4
3
2
1
SH
Slow_Q_N
Slow_Q_P
Fast_Q0_N
Fast_Q0_P
+15V
PWR_FLAG
+15V
GND
GND
Slow_pulse LVDS -> LVTTL
+2V5
C17
100n
+3V3
+2V5
C18
100n
R45
5.6k
GND
GND
C85
100n
Slow_Q_P
Slow_Q_N
100n
C86
R4
100
R46
5.6k
GND
IN+
IN−
VDD
VCC
D
OUT
GND
GND
2
3
10
5
8
7
1
U4 Slow_data
SN65LVDS4
Slow_data
GND
Fast_pulse equalizer
C15
100n
+3V3
U3
DS15EA101
C13
1n
Fast_Q0_P
Fast_Q0_N
R3
100
1n
C14
GND
Fast_Q1_P
Fast_Q1_N
IN
IN
EN
VCC
VCC
16
13
2
3
14
GND
OUT
OUT
LOS
CAP
CAP
11
10
15
5
6
Fast_data_1_P
Fast_data_1_N
C16
1u
C87
100n
100n
C88
Fast_data_P
Fast_data_N
GND
GND
GND
GND
GND
GND
PAD
1
4
7
8
9
12
17
GND
TP22
TestPoint
Slow_data


J10
USB_C
+5VA
PWR_FLAG
VBUS
CC1
CC2
R25 5.1k
R26 5.1k
GND
D−
D+
RX1−
RX1+
TX1−
TX1+
RX2−
RX2+
TX2−
TX2+
SBU1
SBU2
SHIELD
S1
D1
PGB1010603
D2
PGB1010603
U2
LM809
VCC
RESET
GND
+3V3
U1
93LC56B
CS
CLK
DI
DO
10k
R1
2k
R2
VCORE
TP7
C4
4.7u
C6
100n
C9
100n
VPHY
VPLL
U16
FT2232HQ
VREGIN
VREGOUT
DM
DP
USB_N
USB_P
REF
RESET
R5
12k
EECS
EECLK
EEDATA
OSCI
OSCO
TEST
Y1
12M
C2
30p
C7
30p
AGND
PAD
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
PWREN
SUSPEND
TXD
RXD
TCK
TDI
TDO
TMS
TP8
TP10
TP12
TP14
TP16
TP9
TP11
TP13
TP15
TP17
L4
10u
L5
10u
TP5
TP6
C42
4.7u
C43
100n
C44
4.7u
C45
100n
C1
100n
C3
100n
C5
100n
C8
100n
C10
100n
C11
100n
C12
100n


+5V
+15V
TP1
+15V
U17
TPS563200
C76
100n
L3
3.3u
TP18
+5V
+5VD
PWR_FLAG
PWR_FLAG
C70
10u
C73
10u
VIN
SW
VBST
EN
GND
VFB
R39
56.2k
C80
22u
C81
22u
GND
GND
R40
10k
GND
GND
Choose which 5V
+5V
PWR_FLAG
+5VA
+5VD
J9
Conn_01x03
Testpoint GND
TP19
GND
TP20
GND
TP21
GND
GND
+5V
+3.3V
U14
TPS563207
C83
100n
L1
3.3u
TP2
+3.3V
R41
0
+3V3
PWR_FLAG
C71
10u
C82
100n
VIN
SW
BST
EN
GND
FB
C84
10p
R43
30.9k
C77
22u
GND
GND
R44
10k
GND
GND
+2.5V
+5V
U15
TPS62205DBV
L2
10u
TP3
+2.5V
R42
0
+2V5
PWR_FLAG
C72
10u
VI
SW
EN
GND
FB
C78
10u
GND
GND
GND
+1.8V
+3V3
U18
ADM7171ACPZ-1.8-R7
TP4
+1.8V
+1V8
C74
10u
VIN
VIN
VOUT
VOUT
EN
SS
SENSE
GND
PAD
C79
10u
GND
C75
1n
GND
GND
GND


De-serializer
U6A
SCAN921226H
+3V3
Fast_data_PD
Fast_data_ND
R6
100
RI+
RI-
REN
ROUT0
ROUT1
ROUT2
ROUT3
ROUT4
ROUT5
ROUT6
ROUT7
ROUT8
ROUT9
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RD8
RD9
PWRDN
REFCLK
Ref_Clk_Deserializer
TDI
TDO
TMS
TCK
TRST
RCLK
RCLKR/F
LOCK
Word_Clk
RCLKRF
LOCK
Slow_data
Word_Clk
RCLKRF
RD2
RD0
RD1
RD3
RD4
RD5
RD6
RD8
RD7
RD9
LOCK
Bank6
IO/CLK2p
IO/CLK2n
IO/CLK3p
IO/CLK3n
VREFB6N0
VCCIO6
VCCIO6
C28
100n
GND
U5G
MAX10M16SCE
Reference clk
C30
100n
FB1
30
PWR_FLAG
X1
ASV-40MHz
EN
GND
Vdd
OUT
Clk_40MHz
Differential outputs
+2V5
C32
100n
Bank4
VCCIO4
VREFB4N0
U5E
MAX10M16SCE
Trigger1_N
Trigger1_P
Trigger2_N
Trigger2_P
C19
100n
+1V8
Bank7
VCCIO7
VREFB7N0
U5H
MAX10M16SCE
CS
MOSI
SCK
MISO
PLL_locked
RESET
Clock distribution and jitter reduction PLL
J5
SPI
U7A
AD9544
SDO/M5
SCLK/SCL
SDIO/SDA
CSB/M6
REFA
REFAA
REFB
REFBB
XOA
XOB
RESETB
LDO0
LF0
LDO1
LF1
OUT0AP
OUT0AN
OUT0BP
OUT0BN
OUT0CP
OUT0CN
OUT1AP
OUT1AN
OUT1BP
OUT1BN
M0
M1
M2
M3
M4
Deser_Clk_P
Deser_Clk_N
LVDS
Precision_Clk_P
Precision_Clk_N
PLL_locked
Word_Clk
1k
R7
R8
1.2k
R9
330
R10
150
C20
100n
C21
100n
C22
0.22u
C23
3.9n
C24
0.22u
C25
3.9n
C26
10n
C27
10n
R11
50
R12
50
R13
50
R14
50
R15
50
R16
50
R17
100
C29
100n
C31
100n
U8
SN65LVDS4
Ref_Clk_Deserializer
J6
Ref_mon
TP23
TestPoint
+3V3
+2V5
C33
100n
Bank3
VCCIO3
VCCIO3
VREFN3N0
U5D
MAX10M16SCE
PulseID_Clk
PulseID_MOSI
PulseID_MISO
PulseID_CS
PulseID_Clk_2
PulseID_MOSI_2
PulseID_MISO_2
PulseID_CS_2
IO/CLK6n
IO/CLK6p
IO/CLK7n
IO/CLK7p
Clk_40MHz
Trigger3
Trigger4
Programming_Unused
TDO
TDI
TCK
TMS
TXD
RXD
File: Programming_Unused.kicad_sch
Supply_CDR_PLL
File: Supply_CDR_PLL.kicad_sch


Programming – FT2232
40MHz Clock
+3V3
C35
100n
GND
Bank8
123
139
128
VREFB8N0
VCCIO8
VCCIO8
Clk_40MHz
120
124
127
130
131
132
135
140
141
TMS
TDO
TDI
TCK
TXD
RXD
IO
U5I
MAX10M16SCE
Programming – FPGA
+3V3
R18
10k
R20
10k
J8
Prog.
2
4
6
8
10
1
3
5
7
9
18
20
16
19
TCK
TDO
TMS
TDI
GND
+3V3
R19
1k
122
121
DEV_OE
DEV_CLRn
GND
U5A
MAX10M16SCE
Config
JTAGEN
15
1k
R23
nSTATUS
136
10k
R24
CONF_DONE
138
10k
R27
nCONFIG
129
10k
R28
CONFIG_SEL
126
10k
R29
CRC_ERROR
134
GND
+3V3
C36
100n
GND
31
30
Bank2
VCCIO2
VREFB2N0
IO/CLK0n
IO/CLK0p
IO/CLK1n
IO/CLK1p
IO/PLL_L_CLKOUTn
IO/PLL_L_CLKOUTp
26
27
28
29
32
33
LED_2
LED_3
LED_1
MAX10M16SCE
U5C
+3V3
R21
R
J11
Conn_01x02
LED_1
Q1
BSS123
GND
+3V3
R22
R
J12
Conn_01x02
LED_2
Q2
BSS123
GND
+3V3
R30
R
J13
Conn_01x02
LED_3
Q3
BSS123
GND
Unused
+3V3
23
9
17
Bank 1
VCCIO1B
VCCIO1A
VREFB1N0
IO
6
7
8
10
11
12
13
14
21
22
24
25
U5B
MAX10M16SCE
Debugging purpose
+3V3
C34
100n
GND
82
80
Bank5
VCCIO5
VREFB5N0
IO/RUP
IO/RDN
IO
75
74
77
76
79
78
81
85
84
87
86
IO1
IO0
IO3
IO2
IO5
IO4
IO6
IO8
IO7
IO10
IO9
U5F
MAX10M16SCE
+3V3
1
IO0
2
IO1
3
IO2
4
IO3
5
IO4
6
IO5
7
IO6
8
IO7
9
IO8
10
IO9
11
IO10
12
13
J7
Conn_01x13
GND


AD9543 Supply
GNDA
C47
100n
C50
100n
+1V8
C51
100n
FB6
30
FB5
30
FB7
30
PWR_FLAG
U7B
AD9544
C53
100n
C56
100n
C57
100n
C54
100n
C52
100n
C48
100n
C46
100n
C39
100n
FB2
30
FB4
30
FB3
30
C37
100n
C40
100n
R31
0
GND
Supply SCAN921226
+3V3
FB8
30
FB9
30
FB10
30
FB11
30
C58
100n
C59
100n
C61
100n
1n
C62
100n
C63
C60
1n
GNDS
U6B
SCAN921226H
DVCC
AVCC
DGND
AGND
R32
0
Supply FPGA
C38
100n
C41
100n
C49
100n
C55
100n
U5J
MAX10M16SCE
VCC_ONE
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
VCCA6
PAD

D-Flipflop: NB7V52MMNG
Output driver: SN65LVDS4 (MC100EPT21)
Fan-out buffer für den Clock: NB3L8504S

Idee: Precision_clk mit NB3L8504S an zwei NB7V52MMNG verteilen (als clk)
D vom FPGA
Q mit MC100EPT21 in LVCMOS umwandeln