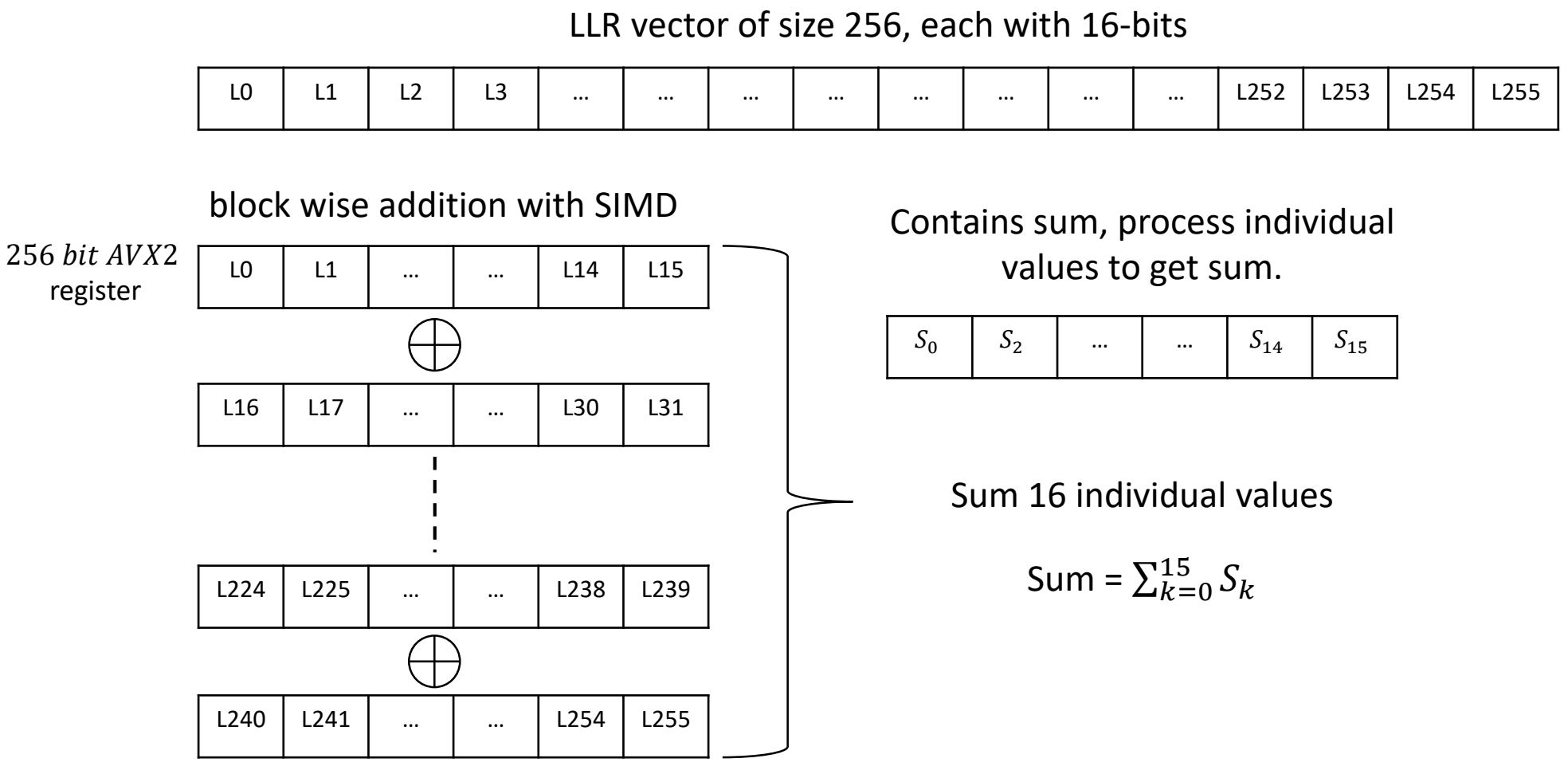
LLR vector of size 256, each with 16-bits
L0 L1 L2 L3 … … … … … … … … L252 L253 L254 L255
block wise addition with SIMD
256 bit AVX2 register
L0 L1 … … L14 L15
L16 L17 … … L30 L31
L224 L225 … … L238 L239
L240 L241 … … L254 L255
Contains sum, process individual values to get sum.
S_0 S_2 … … S_{14} S_{15}
Sum 16 individual values
Sum = $\sum_{k=0}^{15} S_k$