

LLR vector of size 256, each with 16-bits

L0	L1	L2	L3	L252	L253	L254	L255
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block wise addition with SIMD

256 bit AVX2
register

L0	L1	L14	L15
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L16	L17	L30	L31
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L224	L225	L238	L239
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L240	L241	L254	L255
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Contains sum, process individual
values to get sum.

S_0	S_2	S_{14}	S_{15}
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Sum 16 individual values

$$\text{Sum} = \sum_{k=0}^{15} S_k$$