

Real-time and high accuracy frequency measurements for intermediate frequency narrowband signals

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Real-time and accurate measurements of intermediate frequency signals based on microprocessors are difficult due to the computational complexity and limited time constraints. In this paper, a fast and precise methodology based on the sigma-delta modulator is designed and implemented by first generating the twiddle factors using the designed recursive scheme. This scheme requires zero times of multiplications and only half amounts of addition operations by using the discrete Fourier transform (DFT) and the combination of the Rife algorithm and Fourier coefficient interpolation as compared with conventional methods such as DFT and Fast Fourier Transform. Experimentally, when the sampling frequency is 10 MHz, the real-time frequency measurements with intermediate frequency and narrowband signals have a measurement mean squared error of ± 2.4 Hz. Furthermore, a single measurement of the whole system only requires approximately 0.3 s to achieve fast iteration, high precision, and less calculation time. Published by AIP Publishing. <https://doi.org/10.1063/1.5010142>

I. INTRODUCTION

The intermediate frequency signals bridging between the baseband and radio-frequency have been keys for many applications such that frequency measurements of these narrowband signals have attracted great interests in various fields such as microelectromechanical system (MEMS), electric power systems, and telecommunication system.^{1–3} Using the Fast Fourier Transform (FFT), most research has focused on the accuracy of the frequency measurements but ignored the speed and efficiency.⁴ For instance, radar intermediate frequency signals usually utilize high-precision frequency measurement methods to improve the accuracy, such as maximum likelihood method and the Multiple Signal Classification (MUSIC) method,^{5–7} but most of them require complex calculations with a long processing time. In the resonance dew point sensor systems, frequency changes are used to identify environmental humidity.^{8–11} Therefore, rapid and accurate frequency measurement is important and the multi-bit analog-to-digital converter (ADC) is widely utilized. When the number of bits of the ADC is high, the resulting accuracy is also high using the frequency measurement algorithm in a Field Programmable Gate Array (FPGA). For frequency-based methods such as FFT, the speed and accuracy will be limited by the large data. Using the high-precision frequency estimation, the speed of the frequency estimation will be worse due to the large and complex calculations. Using the Digital Signal Processing (DSP) and embedded computer system, the requirements of frequency measurement are even more stronger. At present, there are many frequency measurement algorithms and the discrete Fourier transform (DFT) is especially suitable for the frequency estimations for high measurement accuracy and strong

anti-interference ability.¹² However, the storage problem and operation speed have limited the measurement accuracy.

In this paper, a fast frequency measurement method based on DFT is proposed for intermediate frequency signals. The main features of the proposed measurement system include the following: (1) utilizing the sigma-delta modulator to achieve the 1 bit digital signal; (2) designing the DFT fast algorithm based on the sigma-delta modulator with zero multiplication and half addition; (3) using the twiddle factor generation method to solve the problems of storage capacity and the computation time; and (4) implementing the fine frequency measurement by combining the Rife algorithm and the Fourier coefficient interpolation method to further improve the accuracy and reduce the DFT points. Figure 1 shows the flow chart of the proposed frequency measurement method. By utilizing the characteristics of the sigma-delta modulator, the long-point DFT and twiddle factor storage can be realized rapidly in the microprocessor. The proposed method is realized through hardware implementations and experiments.

II. MEASUREMENT PRINCIPLE

A. Sigma-delta modulator

The frequency resolution of the DFT can be defined as the characterized minimum frequency interval f_0 on the frequency axis, which is related to the sampling points N and sampling frequency f_s . The relationship of these three parameters can be expressed as

$$f_0 = \frac{f_s}{N} = \frac{1}{Nt_s} = \frac{1}{T}, \quad (1)$$

where t_s is the sampling interval and T is the length of the analog signal before sampling. From Eq. (1), it is obvious that the longer the signal length, the higher the frequency resolution is.

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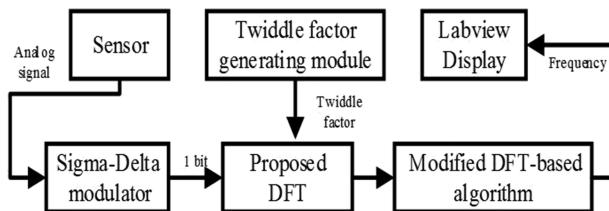
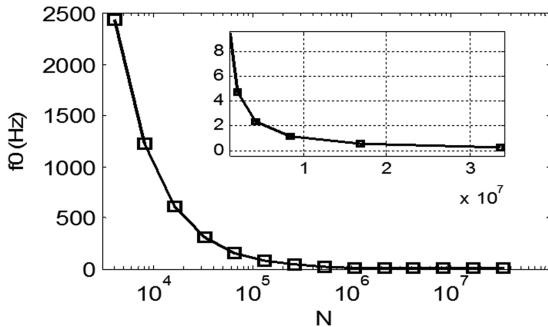


FIG. 1. The flow chart of the proposed frequency measurement scheme.

FIG. 2. The frequency resolution varies with N of the DFT.

When the sampling frequency is 10 MHz, the f_0 versus N plot is shown in Fig. 2. Without the consideration of the integer sampling period, we can conclude from the figure that the frequency resolution gradually improves as N increases. For example, when f_0 is 610.35 Hz, N is 16 384. Furthermore, only when N is greater than 16 777 216, the frequency resolution is less than 1 Hz.

To better understand the required calculation and storage, an FFT with 16 777 216 points is used to achieve the frequency resolution with detailed parameters shown in Table I. The twiddle factor is denoted in Eq. (2), where k is the frequency point and n is the signal sequence number. If k is 1, and n is 1 and 2, the real parts of the twiddle factor are 0.999 999 999 999 93 and 0.999 999 999 999 719, respectively,

$$W_N^{kn} = \cos\left(\frac{2\pi}{N} * k * n\right) - j \sin\left(\frac{2\pi}{N} * k * n\right). \quad (2)$$

The FPGA is used to calculate the FFT, and the twiddle factors are required for storages. On the one hand, the difference of the adjacent twiddle factor is very small (the minimum is in the order of 10^{-13}), and the calculation type of FPGA is fixed-point. Therefore, if the storage accuracy of the twiddle factor should reach 10^{-13} , the stored bits of the twiddle factor must be at least 64 bits. Furthermore, for the narrowband intermediate frequency signals, the 16-bit ADC is used for the analog-to-digital conversion; the output of the ADC is a 16-bit digital signal. Thus, the calculation of the 16-bit

TABLE I. The calculation and twiddle factor storage of FFT with 16 777 216 points.

| Algorithm | Complex multiplication/times | Complex addition/times | Twiddle factor storage |
|-----------|------------------------------|------------------------|------------------------|
| FFT | 402 653 184 | 201 326 592 | 16 777 216 |

digital signal and 64-bit twiddle factor is inevitable. In other words, more storage space and complicate calculation will be required. Furthermore, the FPGA will overflow to cause unsatisfactory accuracy. On the other hand, the storage of twiddle factors in Table I is 16 777 216, which will occupy the storage space of $16 777 216 \times 64 \approx 134$ Mbyte and it is unrealistic for the FPGA to store these twiddle factors and make the real-time computing unachievable.

The FFT is based on butterfly calculations, and each level requires $N/2$ times complex multiplications and N times complex additions. If it is implemented in the DSP, the calculation type is floating and the amount is large. Meanwhile, the twiddle factors occupy plenty of storage space. For instance, the RAM of TMS320C6748 can only store 128 Kbyte, which is used in the proposed hardware system. As such it is evident that the storage in Table I is unachievable for the DSP. We can extend the storage of DSP using the external memory, but this will be difficult for the real-time computing due to large time requirement.

As such, a high-precision and real-time frequency measurement for a narrowband intermediate frequency signal cannot be realized in the microprocessor by the conventional multi-bit ADC and the FFT. To solve these problems, the sigma-delta modulator is implemented to achieve the analog-to-digital conversion and the 1-bit output coding of the sigma-delta modulator is applied to design the back-end frequency measurement algorithms.

The mechanism of the sigma-delta modulator for quantization and coding is shown in Fig. 3. It is observed that σ is the quantization step, and $f(t)$ and $f'(t)$ are the input signal and estimated value of the signal, respectively. When the relationship between $f(t)$ and $f'(t)$ is $f(t) > f'(t)$, the output of the sigma-delta modulator is 1. Conversely, the output is 0. The process of the modulator is equivalent to the error signal $f(t) - f'(t)$, and the reconstruction of the original waveform $f(t)$ can be achieved by low-pass filtering for $f'(t)$, while the waveform of $f'(t)$ can be reconstruct by integrating the digital signal of sigma-delta modulator outputs.^{13,14} In brief, the 0, 1 coding of the sigma-delta modulator carries all information for the input analog signals. Therefore, the analog-to-digital conversion module of the proposed frequency measurement system can be obtained by directly analyzing the 0, 1 coding results to improve the speed of the analog-to-digital conversion process by omitting the filter module.

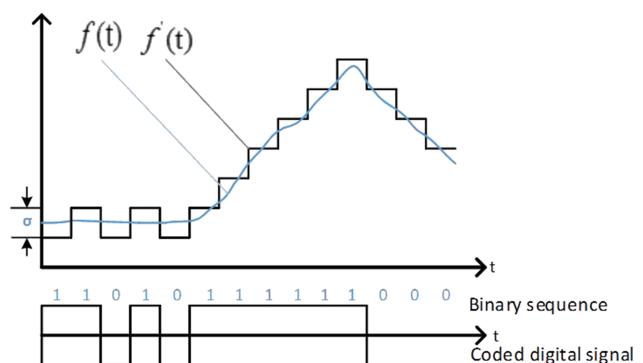


FIG. 3. The coding scheme of the sigma-delta modulator.

B. DFT based on sigma-delta modulator

Since our application is narrowband signals within a small frequency range from f_1 to f_2 , the spectral peak can be searched within the range based on Eqs. (3) and (4) when the DFT point number N is set and k_1' and k_2' are rounded to k_1 and k_2 . The frequency to be measured can be obtained by searching the peak of the DFT values between k_1 and k_2 . By analyzing Eqs. (3) and (4), it is observed that the amount of data between k_1 and k_2 is less with the prerequisite of high sampling frequency f_s and small difference between f_2 and f_1 . Therefore, one can directly use DFT to calculate the amplitude-frequency between k_1 and k_2 . For the narrowband signal with different starting frequency f_1 and small range, the starting frequency k_1 and the stop frequency k_2 can be first calculated by Eqs. (3) and (4). Next, the amplitude-frequency result is obtained by DFT,

$$k'_1 = f_1 N / f_s, \quad (3)$$

$$k'_2 = f_2 N / f_s. \quad (4)$$

Equation (5) shows the calculating theory of DFT, and the calculation of an $X(k)$ function usually requires N times complex multiplications and $N - 1$ times additions.¹⁵ Based on the characteristics of 0, 1 output from the sigma-delta modulator, the corresponding DFT algorithm is designed. First, the output signals of the sigma-delta modulator are evaluated. If the output signal is 1, the twiddle factor is directly added to $X(k)$, which can drastically decrease the calculation time by omitting the multiplications between the signal to be measured $x(n)$ and the twiddle factor in Eq. (5). If the output signal is 0, the calculation in Eq. (5) can be skipped. Especially, the multiplication is not required by using the proposed method, which is significant for the embedded systems to save large amounts of computing time and storage space. Known from the periodicity of the sinusoidal signal, half of the output $x(n)$ of the sigma-delta modulator will be 0. As such, if the length of the signal to be measured is N , the calculation of an $X(k)$ function only needs about $N/2 - 1$ times complex additions by the proposed DFT, while the traditional DFT requires N times complex multiplications and $N - 1$ times complex addition,

$$X(k) = \sum_{n=0}^{N-1} x(n) \exp\left(-j \frac{2\pi}{N} kn\right). \quad (5)$$

The storage of the twiddle factor in Table I shows that the storage difficulty is still significant when the length N of DFT is big. From the definition of the twiddle factor in Eq. (2), it includes both the real part and the imaginary part, which are both required to calculate from the sine and cosine functions. Therefore, if we directly calculate the twiddle factor during the calculation of the DFT, the computation time could be too large to meet the real-time performance requirement, and it will be a great pressure for the storage space requirement if the twiddle factor is stored before the DFT calculations. Meanwhile, the real-time performance will be limited by the time required in invoking the twiddle factors for the DFT. To solve these problems, an algorithm is proposed to reduce the storage space.

The real part of the twiddle factor is calculated as $\cos(2\pi kn/N)$, and each amplitude $X(k)$ is calculated by the multiplication of N points of twiddle factors and input $x(n)$ as described in Eq. (5), where n is $0, 1, 2, 3, \dots, N - 1$. From the characteristics of the sine and cosine function, one can derive the following functions:

$$\begin{aligned} \cos\left(\frac{2\pi}{N} k(n + \Delta n)\right) &= \cos\left(\frac{2\pi}{N} kn\right) \cos\left(\frac{2\pi}{N} k\Delta n\right) \\ &\quad - \sin\left(\frac{2\pi}{N} kn\right) \sin\left(\frac{2\pi}{N} k\Delta n\right), \end{aligned} \quad (6)$$

$$\begin{aligned} \sin\left(\frac{2\pi}{N} k(n + \Delta n)\right) &= \cos\left(\frac{2\pi}{N} kn\right) \sin\left(\frac{2\pi}{N} k\Delta n\right) \\ &\quad + \sin\left(\frac{2\pi}{N} kn\right) \cos\left(\frac{2\pi}{N} k\Delta n\right). \end{aligned} \quad (7)$$

By combining both equations, the following is derived:

$$\begin{bmatrix} W_r(n) \\ W_i(n) \end{bmatrix} = \begin{bmatrix} \cos\left(\frac{2\pi}{N} k\Delta n\right) - \sin\left(\frac{2\pi}{N} k\Delta n\right) \\ \sin\left(\frac{2\pi}{N} k\Delta n\right) \cos\left(\frac{2\pi}{N} k\Delta n\right) \end{bmatrix} \begin{bmatrix} W_r(n-1) \\ W_i(n-1) \end{bmatrix}. \quad (8)$$

Equation (8) can be written as

$$\begin{bmatrix} W_r(n) \\ W_i(n) \end{bmatrix} = \cos\left(\frac{2\pi}{N} k\Delta n\right) \begin{bmatrix} 1 & -\tan\left(\frac{2\pi}{N} k\Delta n\right) \\ \tan\left(\frac{2\pi}{N} k\Delta n\right) & 1 \end{bmatrix} \times \begin{bmatrix} W_r(n-1) \\ W_i(n-1) \end{bmatrix}, \quad (9)$$

where $W_r(n)$ and $W_i(n)$ indicate the real part and imaginary part of the twiddle factor when the frequency point is k . From Eqs. (6) and (7), with given parameters of n , k , and $\Delta n = 1$, every twiddle factor $W_r(n)$ and $W_i(n)$ can be deduced from twiddle factor $W_r(n-1)$ and $W_i(n-1)$ by four times of multiplications and two times of additions. The multiplication times are further reduced from four to three in Eq. (9) with only the real-valued operations. Therefore, the proposed twiddle factor generation method can improve the calculation speed as compared with the original calculations of the cosine and sine functions.

Based on the above proposed twiddle factor generating and DFT algorithm, the flow chart of the calculating algorithm is illustrated in Fig. 4 and implemented in DSP using C language. The twiddle factor is first calculated, where *delta_cos* and *delta_tan* are $\cos(2\pi k \Delta n / M)$ and $\tan(2\pi k \Delta n / M)$ with $\Delta n = 1$. It is worth mentioning that instead of calculating all twiddle factors in FFT, we only need to calculate the real and imaginary parts of the twiddle factors *W_cos* and *W_sin* for the required $X(k)$. In other words, if M points of DFT are required, the proposed twiddle factor algorithm only needs to store M *delta_cos* and *delta_tan* to greatly decrease the storage of the twiddle factors and the calculation time. As such, the total amount of calculation for an amplitude-frequency $X(k)$ function is $3N$ real multipliers, $2N$ real additions, and $N/2$ complex additions.

C. Modified DFT-based algorithm

To further improve the accuracy, a frequency estimation algorithm based on DFT is proposed to reduce the pressure of the real-time frequency measurement from the DFT module.

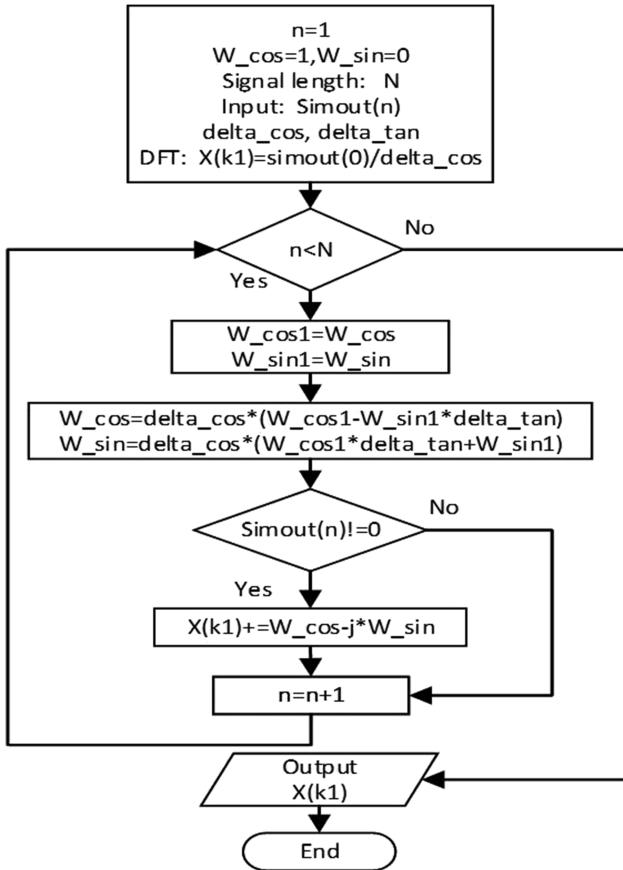


FIG. 4. The flow chart of the twiddle factor generating and DFT calculation.

Among the frequency estimation methods based on the DFT, the Fourier coefficient interpolation iterative method is a high-precision method but requires complex calculations¹⁶ while the choice of the initial iteration value δ can impact the number and accuracy of iterations. The Rife algorithm is another high-precision frequency measurement method based on DFT with simplified calculations and lower accuracy as compared with the Fourier coefficient interpolation algorithm. Here, the two algorithms are combined. The Fourier coefficient interpolation iterative algorithm generally requires two iterations to achieve better frequency estimation accuracy, and each iteration has to calculate the amplitude of X_p after the frequency shift. The signal length N to be measured is large, and the iterative accuracy relies strongly on the initial value δ . Therefore, the proposed algorithm first estimates the δ value using the Rife algorithm for minimum calculations, and the frequency estimation accuracy is further improved through another iteration by the Fourier coefficient interpolation. The frequency peak $X(k_0)$ is calculated and the second amplitude $X(k_0 + r)$ near k_0 is searched from the frequency peak of DFT, and the signal length N of the sigma-delta modulator output is fixed. The parameter r in Eq. (10) is 1 or -1 . The Rife algorithm is used to calculate δ_0 as

$$\delta_0 = r \frac{X(k_0 + r)}{X(k_0) + X(k_0 + r)}. \quad (10)$$

Next, we use Eq. (11) to calculate $X_{0.5}$ and $X_{-0.5}$ according to the proposed DFT method based on the sigma-delta modulator,

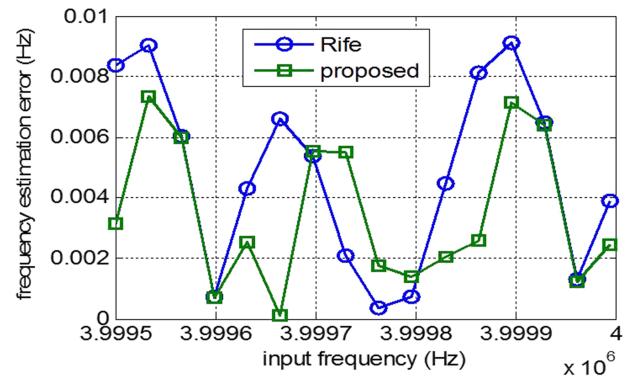


FIG. 5. The error comparisons for the ideal sinusoidal signal by the proposed and Rife algorithms.

which is on the side of the spectral peak $k_0 + \delta_0$,

$$X_p = \sum_{n=0}^{N-1} x(n) \exp[-j \frac{2\pi}{N} (k_0 + \delta_0 + p)n], \quad p = \pm 0.5. \quad (11)$$

Equation (11) is used to obtain final δ_1 and frequency estimation value f as

$$\delta_1 = \delta_0 + 0.5 * \text{real}\left\{\frac{X_{0.5} + X_{-0.5}}{X_{0.5} - X_{-0.5}}\right\}, \quad (12)$$

$$f = (k_0 + \delta_1) \frac{f_s}{N}. \quad (13)$$

To visualize the characteristics and effects of the proposed frequency measurement method, we calculate the ideal sinusoidal signal and the sinusoidal signal with the Gaussian white noise, with signal-to-noise ratio (SNR) of 0 dB and -10 dB with a signal sampling frequency of 12 MHz. The Gauss white noise is chosen because the noise of the modulator is white noise. The frequencies of sinusoidal signals are several groups that range from 3 999 500 Hz to 4 MHz, and the frequency estimation errors are shown in Figs. 5–7, where the errors are defined as the differences between input and measured values. Furthermore, the proposed method is compared with the Rife algorithm.

It is found that the low SNR results in poor accuracy. Figure 5 indicates that the estimation errors of those two methods are both excellent with the 0.01 Hz maximum frequency

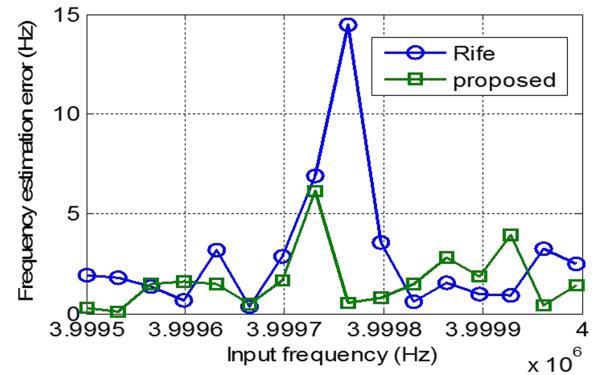


FIG. 6. The error comparisons for the sinusoidal signal with noise for the proposed and Rife algorithms when the SNR is 0 dB.

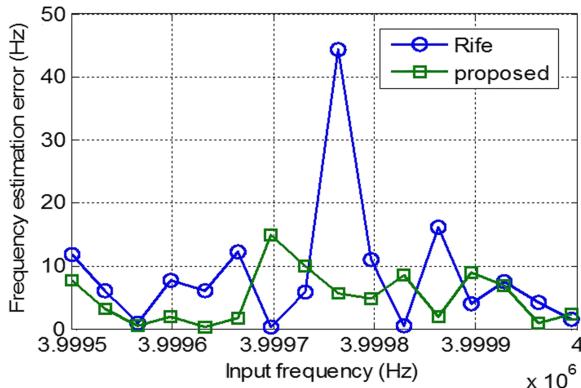


FIG. 7. The error comparisons for the sinusoidal signal with noise by the proposed and Rife algorithms when the SNR is -10 dB.

measurement error. On the other hand, the measured errors for the sinusoidal signal with noise (in Figs. 6 and 7) are worse than the ideal signal. Furthermore, the proposed algorithm has a large attenuation at the highest frequency error of the Rife algorithm.

III. HARDWARE IMPLEMENTATION AND PERFORMANCE EVALUATION

A. System construction

The experimental setup is shown in Fig. 8 with four main parts: sensor, sigma-delta modulator circuit, FPGA part, and DSP.

The sensor provides the analog signals to be measured focusing on the narrowband intermediate frequency signals with small frequency ranges. The sigma-delta modulator circuit is applied to convert the analog signals to the tractable digital signals, which consists of a one-stage amplifier, a low-pass filter, and a modulator chip ADS1202 by ADI, Inc., which achieves the digital isolation by the iCoupler technology with the resolution, input voltage, and output voltage as 16 bits, 3.5 V, and 3.3 V, respectively. The input range is from -250 to 250 mV, and the internal and external clock are 10 MHz and 12 MHz, respectively. The modulator output is the 1-bit serial code, which has unsatisfactory transmission efficiency. However, the proposed system transforms the serial code to 16 bits parallel code in the FPGA to enter the asynchronous

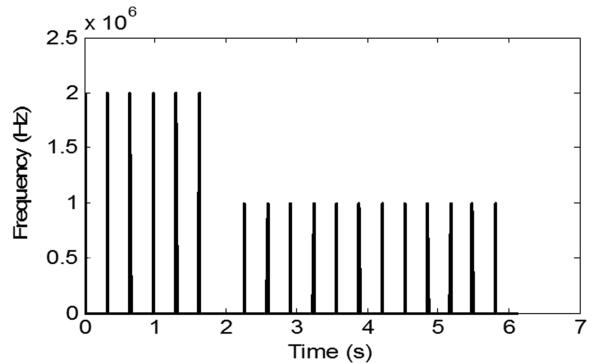


FIG. 9. The measured frequency with respect to time.

first in, first out (FIFO) for communicating with the DSP, having a Harvard structure to acquire high-speed computing ability. The External Memory Interface (EMIFA) is a high speed data interface between FPGA and DSP. The mission of the DSP is to achieve the proposed frequency measurement algorithms. It has the pipelining technique, multiplication and cumulative structure, and powerful DSP instructions, which are especially suitable for the complex and floating-point operations.

B. Results and discussion

The sensor is replaced by the direct digital synthesizer (DDS) to generate an ideal signal. The sigma-delta modulator uses 10 MHz internal clock to provide the sampling frequency for analog-to-digital conversion. The sinusoidal signals with different frequencies and 200 mV fixed amplitude are taken as the input signals of the frequency measurement system, and the final measured frequency calculated in DSP is uploaded to a personal computer (PC) to display the measurement results. The change of the measured frequency over time is shown in Fig. 9 with the frequency of input signals varying from 1 999 500 Hz to 2 MHz from 0 to 2 s, while the frequency of input signal varies from 999 500 Hz to 1 MHz from 2 to 6 s. The input signal length of the measurement system is 32 768, and the point of DFT is 524 288. Deduced by Eqs. (3) and (4), the number of the frequency points to be calculated is 28. It is obvious that the proposed frequency measurement system can achieve the real-time frequency measurement requirements from the measurement results in Fig. 9. The proposed scheme

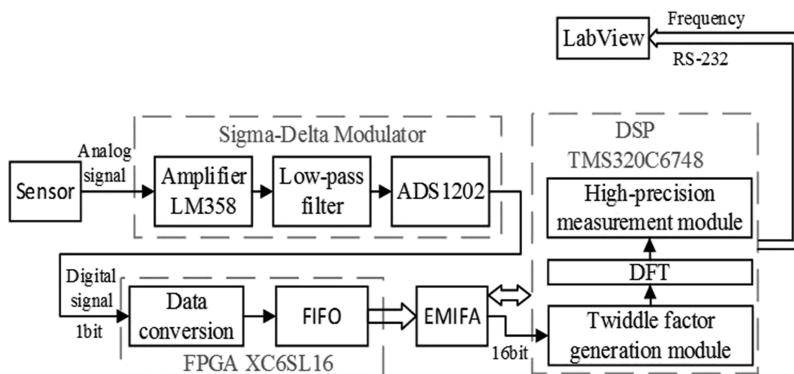


FIG. 8. Schematic of the proposed frequency measurement system setup.

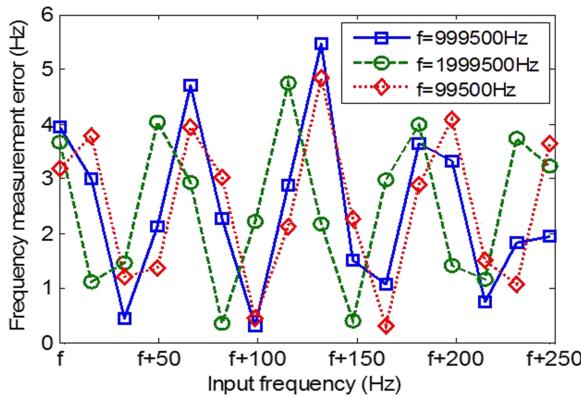


FIG. 10. The frequency measurement errors of the proposed measurement system with respect to the input frequency. The three curves are the errors with different starting frequencies of 999 500 (blue), 1 999 500 (green), and 99 500 (red), respectively.

can refresh the measured frequency three times in 1 s or 0.3 s per measurement. Furthermore, from the two frequency measurement results in Fig. 9, when the center frequency of the input signal changes, the measurement system can fast track the input signal. Hence, it implies that the proposed scheme can measure narrowband intermediate frequency signals with different center frequencies.

Figure 10 shows the change of the measured frequency error over the input frequency, while the input of the measurement system is the sinusoidal signals with different frequencies. Since the proposed measurement scheme is mainly suitable for narrowband intermediate frequency signals with small ranges, we test the signals with different center frequencies. In Fig. 10, different curves are the change of frequency errors with three different starting input frequencies. It is worth noting that the frequency error is the difference between the frequency measurement value and the true value of the signal generator, and each frequency error in Fig. 10 is the mean squared error (MSE) value of ten groups of frequency error values measured at the corresponding input frequency. For example, the blue solid curve is the difference between the measured frequency of the proposed system and the actual frequency, where the frequency of sinusoidal inputs ranges from 999 500 Hz to 1 MHz. By comparing these error curves of different starting frequencies of 999 500, 1 999 500, and 99 500 Hz, the MSEs are 2.451 34, 2.474 84, and 2.478 83 Hz, respectively. Furthermore, the measurement errors by the proposed scheme are stable among different starting frequency signals. For example, the blue solid curve has the starting frequency of 999 500 Hz and the MSE is 2.451 341 Hz. As the input frequency varies from 999 500 to 1 MHz, the maximum and minimum frequency MSEs are

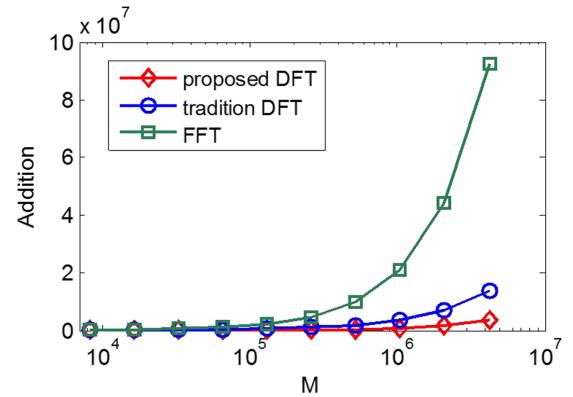


FIG. 11. Addition calculation varies with DFT points M.

5.6 Hz and 0.2 Hz, respectively. These errors are negligible as the signal frequency is more than 1 MHz. Hence, the measured results validate that the proposed frequency measurement scheme can achieve both high speed and measurement accuracy.

To verify the advantages of the proposed frequency measurement system in calculation speed and storage, results from the traditional DFT and FFT are compared as shown in Table II, where $\text{Int}(500 \times M/f_s)$ means to be rounded to $500 \times M/f_s$, which can calculate the number of the required frequency points. The starting frequency f_1 can be an arbitrary value, and the frequency range is fixed to 500 Hz. The outputs of the sigma-delta modulator are 1-bit data, whose sampling frequency is 10 MHz. The points of DFT are M to process N output points of the sigma-delta modulator.

As shown in Table II, the multiplication calculation of the proposed scheme is zero, which greatly decreases the amount of computational complexity. Moreover, the twiddle factor storage of the proposed scheme is approximately 1/20 000 of those using traditional schemes. The variation of addition calculations of the three methods with M DFT points is plotted in Fig. 11. It indicates that with the increase of the number of DFT points, the proposed scheme requires much less computation time as compared to those of traditional DFT and FFT methods.

IV. CONCLUSION

In this paper, we have proposed and demonstrated a new real-time frequency measurement scheme based on the sigma-delta modulator for intermediate frequency narrowband signals using three main parts: a sigma-delta modulator circuit for analog-to-digital conversion, an FPGA for data conversion and transmission, and a DSP for frequency measurement

TABLE II. The calculation and storage of different algorithms.

| Algorithm | Multiplication | Addition/subtraction | Twiddle factor storage |
|-----------------|--|---|---|
| Proposed DFT | 0 | $\text{Int}(500 \times M/f_s) \times N/2$ | $\text{Int}(500 \times M/f_s) \times 2$ |
| Traditional DFT | $\text{Int}(500 \times M/f_s) \times 2N$ | $\text{Int}(500 \times M/f_s) \times 2N$ | $2M$ |
| FFT | $M/2 \times \log 2M$ | $M \times \log 2M$ | $2M$ |

operations. Measured results show that when the sampling frequency is 10 MHz, the real-time frequency measurement MSE of ± 2.4 Hz has been achieved with different input intermediate frequencies. Furthermore, a single measurement of the whole system requires only about 0.3 s. The calculation speed and storage of the proposed scheme have been analyzed. Results showed that the calculation of the proposed scheme requires no multiplications and only needs minimum addition calculations, and the storage of twiddle factor is greatly reduced. As such, the proposed frequency measurement scheme could find potential applications in the real-time frequency measurement for intermediate frequency narrowband signals.

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