COMPUTER ARCHITECTURE AND ORGANIZATION

Tutorial 01

Exercise 1:

a/ - How many bits of information can be transmitted simultaneously on a power line?

- How can we transmit 4 bits simultaneously?
- Given an 8-bit data bus, what is the smallest binary number that can be represented on it? And the largest? Give these numbers in base 2, 10, and 16.
- Given a 2-bit address bus, how many different addresses can be represented? And for a 20- bit bus?

b/- What is the addressable space for a 16-bit processor with 32-bit addresses?

- How many address pins are there on a 1 MB memory module (8-bit words)?

c/- In a Von Neumann architecture: where is the data stored? Where are the programs stored?

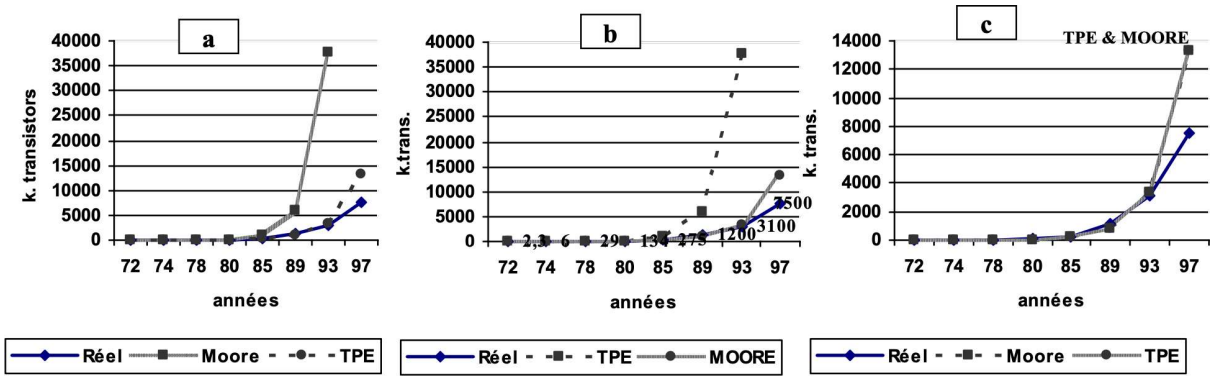
d/- In a Harvard architecture: where is the data stored? Where are the programs stored?

e/- How does the CPU know where the next instruction to execute is located?

Exercise 2:

a/- Complete and comment on the following table:

Year	1971	1979	1982	1985	1989	1993
Processor	4004	8088	80286	80386	I486	Pentium
Real number of transistors	2300	29000	134000	275000	1200000	3300000
Number of transistors according to Moore's method						
Number of transistors according to TPE method						



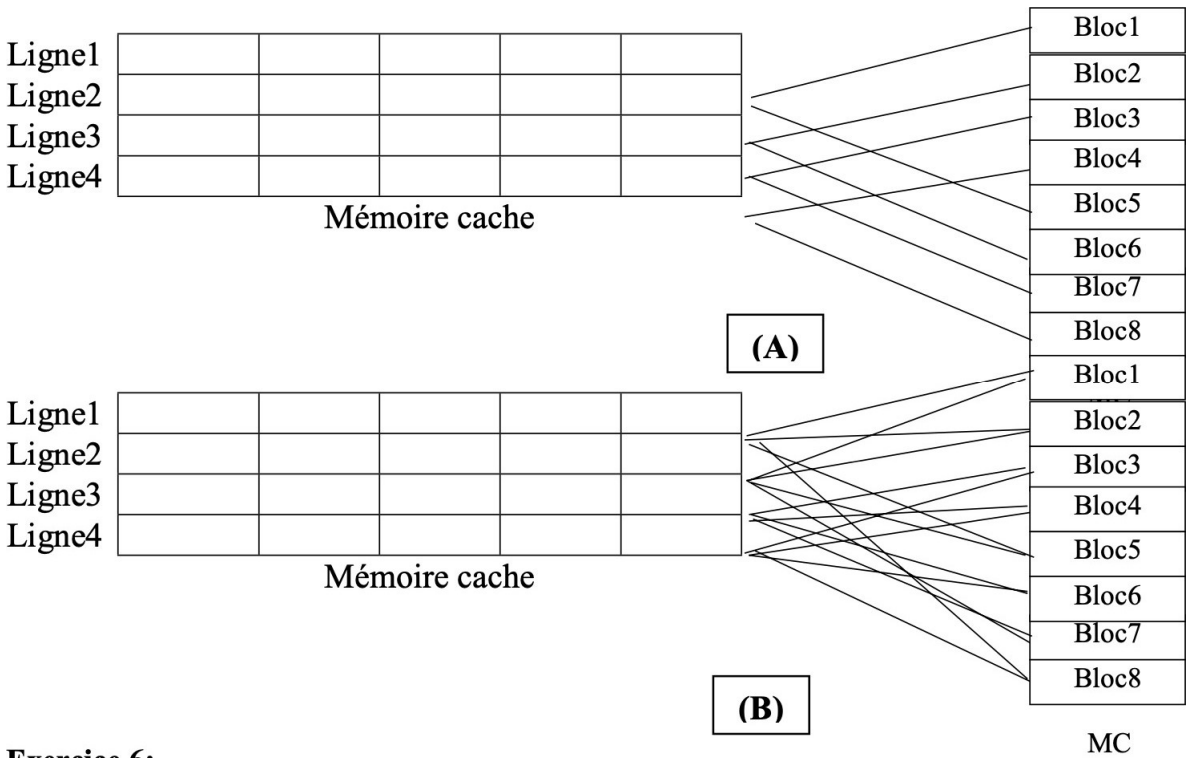
b/- Which of the three figures (a), (b), (c) is the most accurate? Justify.

Exercise 3:

Consider the part of MC with the addresses: i, i+1, i+2, i+3, i+4 (with i>0). Using the ASCII code table, represent the data "HELLO" in this part of memory using both big-endian and little-endian methods.

Exercise 4:

For each of the two cache configurations (A), (B), indicate its organization (Direct-mapped, N-way set associative, or fully associative). If the organization is N-way set associative, give N.



Exercise 5:

The secondary caches of the i486 operate with a line size of 128 bits and a cache size of 256 KB. The job of the cache controller is to map each address unambiguously to one of the "n" cache lines. The lower "x" bits of the address will form the cache line, but instead of using bits 0 to x-1, bits 4 to x+3 are used. Bits 0 to 3 of the address are used to calculate the offset within each line ➔ bits 0 to 3 serve as the index in the line, and bits 4 to x+3 serve as the index in the pool of cache lines. The 14 rest of the address bits "18 to t-1" are not all stored in the cache line tag; most often, only 8 bits are stored (TAG).

Questions:

a/- Calculate t, x, and n.

b/- What is the size of the memory (MC) managed by the cache?

c/- Can two consecutive addresses be loaded into such a cache? What effect does this organization have on the ratio of cache hits to cache misses?

Exercise 6:

A central memory (MC) is connected to a processor (P) via a 32-wire system bus. The command bus is 2 wires wide. The data bus allows a transfer rate (throughput) of 16 GB/s. The machine is clocked by a signal with a frequency of 1 GHz. One memory word = 1 byte.

Question: What is the size of MC? Justify your answer.

Exercise 7:

- In 1999, Intel introduced its 32-bit Pentium III processor (code-named **Coppermine**). A year later (in 2000), it released its 64-bit Pentium IV processor.
- On AMD's side, the **Thunderbird** (32-bit processor) was released in 2000, and the **Athlon XP** (code-named **Barton**, 64-bit processor) came out the following year.
- The Pentium IV had a small L1 data cache of 8 KB, which is exactly half the size of the L1 data cache of the Pentium III (16 KB).
- The inclusive L2 cache of the Pentium III has a 256-bit data path, while the inclusive L2 cache of the Pentium IV has a 512-bit data path. Both caches are 8-way associative and have a size of 256 KB.
- The cache architecture of the AMD Athlon XP processor includes a 128 KB L1 cache and a 512 KB exclusive L2 cache, which is 16-way associative and uses a 64-bit data path, the same as the Thunderbird. The L2 cache of the Thunderbird is also 256 KB and 16-way associative.
- All four processors (Pentium III, Pentium IV, Athlon XP, and Thunderbird) operated at a clock frequency of 1.5 GHz. Their caches are clocked at half of that frequency.

Questions:

1. Compare the latency and throughput of the caches of the two Intel processors (Pentium III and Pentium IV).
2. Compare the throughput of the caches of the two AMD processors (Thunderbird and Athlon XP).
3. Compare the performance of the caches of the Thunderbird and Pentium IV processors (throughput, available space, cache hit rate). Comment.

Exercise 8:

The university has funded a project for a group of computer engineering students who want to design and build a simple computer.

The total budget for this project is 50,000 DA. The student group must manage two types of budgets: the transistor budget and the power budget. The average cost of a transistor in Algeria is 2 DA, and that of a capacitor is 50 cents (0.5 DA).

After conducting a design and implementation study for the project, it was decided to allocate:

- 4,096 DA for the construction of a small cache memory that is not integrated into the processor,
- 10,240 DA for the main memory (MC),
- 40% of the budget (i.e., 20,000 DA) for the 8-bit processor,
- and the remainder for other components.

The student group decided to create a cache with a line length of 2 bytes and a memory word of 1 byte. The main memory is divided into N blocks, where N corresponds to the number of cache lines.

Questions:

- What is the size, in bytes, of the cache built with this budget? Justify your answer.
- What is the size, in bytes, of the main memory built with this budget? Justify your answer.
- What is the size, in bytes, of a memory block?
- What is the width of the address bus? Justify your answer.
- What internal data organization should be adopted for the cache, and why?

Exercise 9 :

At the high end of processor technology, we find two powerful models: **AMD Ryzen 9** and **Intel Core i9**, specifically the **Intel Core i9-13900K** released in October 2023 and the **AMD Ryzen 9 7950X** launched in January 2023.
Both processors are 64-bit models with the following characteristics (for the purpose of this exercise, some information has been modified):

	Intel Core i9-14900K	AMD Ryzen 9 7950X3D
Cache L1	~2MO	1 Mo
Cache L2	32 Mo (data cache) 16 way-set associative	16 Mo (data cache) 16 way-set associative
Cache L3	36 Mo	128 Mo
System Clock frequency	3,2 GHz	4,2 GHz
Bus frequency	2.8 GHz	2.6 GHz
Data bus bandwidth	11.2 GB/s	10.4 GB/s
System bus width	74	73
Control bus width	4	4

Questions:

Assuming that one memory word = 1 byte (1 B) and the size of a line cache (for both processors) is 32 bytes:

1. Determine the size of main memory. Justify your answer.
2. Determine the number of cache L2 sets for Intel processor. Justify your answer.
3. Compare the L3 caches of the two processors (in terms of latency and hit ratio).