



1. Description

1.1. Project

Project Name	cevizlibag_flight_controller
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	08/20/2025

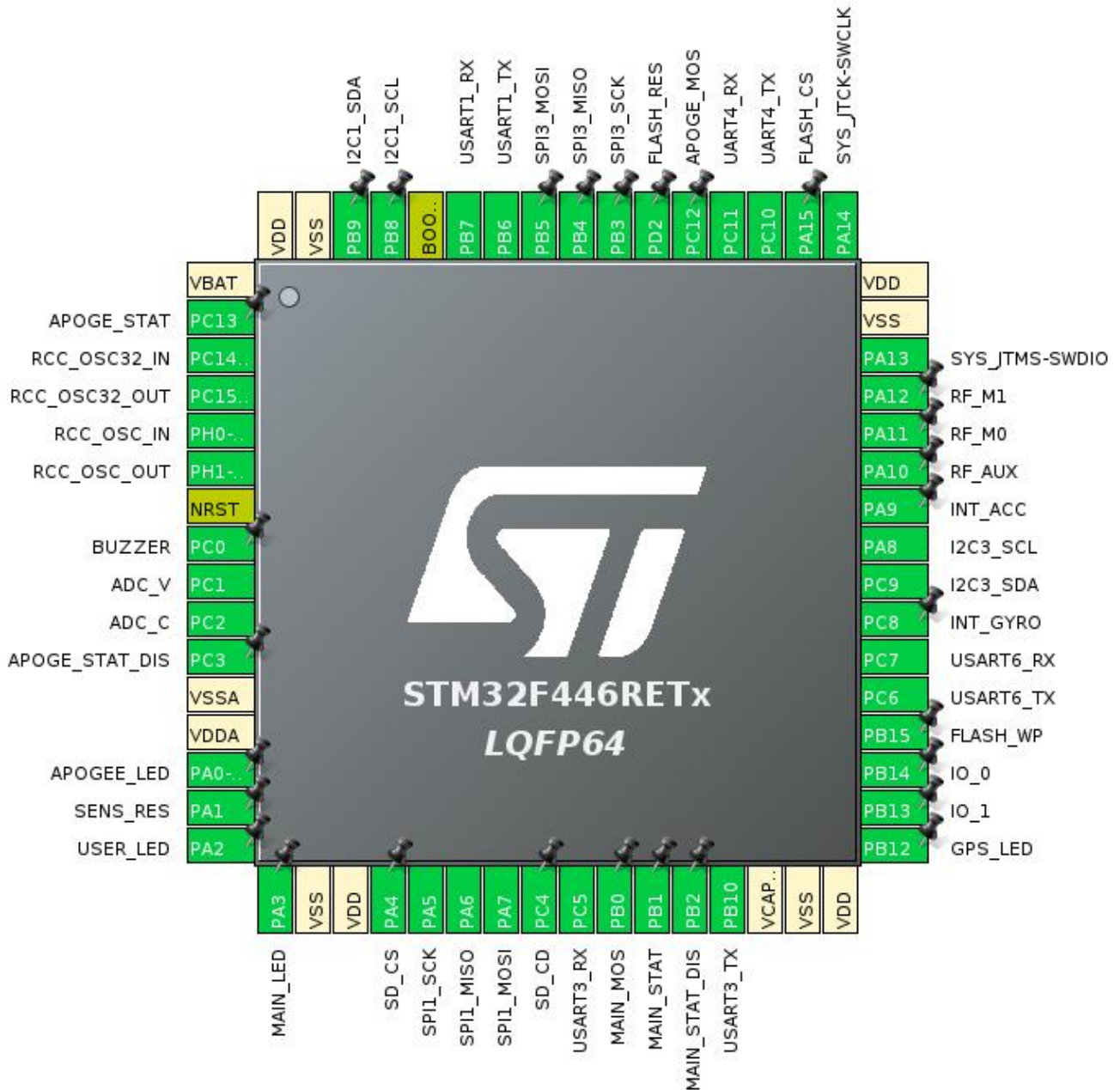
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Input	APOGE_STAT
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	BUZZER
9	PC1	I/O	ADC1_IN11	ADC_V
10	PC2	I/O	ADC2_IN12	ADC_C
11	PC3 *	I/O	GPIO_Output	APOGE_STAT_DIS
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP *	I/O	GPIO_Output	APOGEE_LED
15	PA1 *	I/O	GPIO_Output	SENS_RES
16	PA2 *	I/O	GPIO_Output	USER_LED
17	PA3 *	I/O	GPIO_Output	MAIN_LED
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	SD_CS
21	PA5	I/O	SPI1_SCK	
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
24	PC4 *	I/O	GPIO_Input	SD_CD
25	PC5	I/O	USART3_RX	
26	PB0 *	I/O	GPIO_Output	MAIN_MOS
27	PB1 *	I/O	GPIO_Input	MAIN_STAT
28	PB2 *	I/O	GPIO_Output	MAIN_STAT_DIS
29	PB10	I/O	USART3_TX	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Input	GPS_LED
34	PB13 *	I/O	GPIO_Output	IO_1
35	PB14 *	I/O	GPIO_Output	IO_0
36	PB15 *	I/O	GPIO_Input	FLASH_WP

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PC6	I/O	USART6_TX	
38	PC7	I/O	USART6_RX	
39	PC8	I/O	GPIO_EXTI8	INT_GYRO
40	PC9	I/O	I2C3_SDA	
41	PA8	I/O	I2C3_SCL	
42	PA9	I/O	GPIO_EXTI9	INT_ACC
43	PA10 *	I/O	GPIO_Input	RF_AUX
44	PA11 *	I/O	GPIO_Output	RF_M0
45	PA12 *	I/O	GPIO_Output	RF_M1
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15 *	I/O	GPIO_Output	FLASH_CS
51	PC10	I/O	UART4_TX	
52	PC11	I/O	UART4_RX	
53	PC12 *	I/O	GPIO_Output	APOGE_MOS
54	PD2 *	I/O	GPIO_Output	FLASH_RES
55	PB3	I/O	SPI3_SCK	
56	PB4	I/O	SPI3_MISO	
57	PB5	I/O	SPI3_MOSI	
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

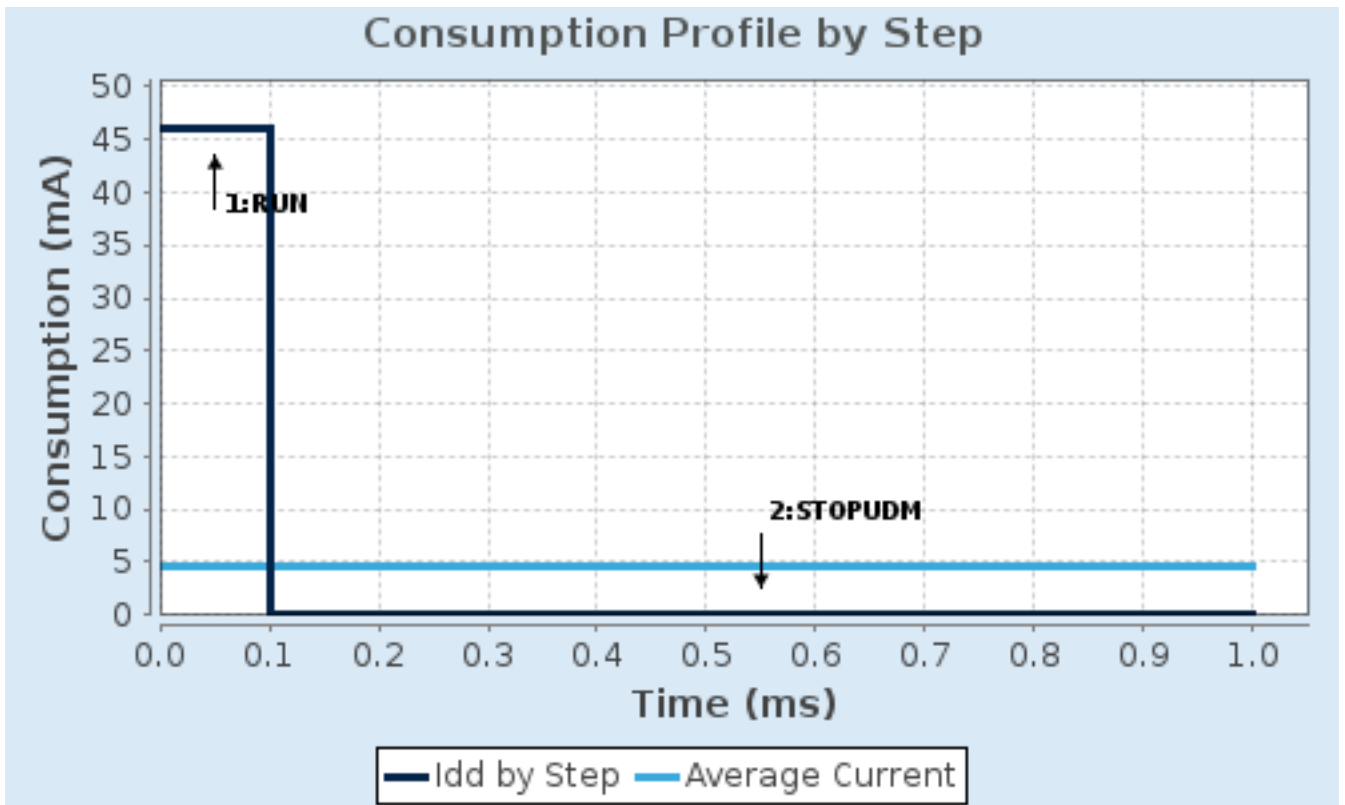
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/P REFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 μ A
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	cevizlibag_flight_controller
Project Folder	/home/yahya/STM32CubeIDE/workspace_1.19.0/cevizlibag_flight_controller
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	Yes
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_I2C1_Init	I2C1
5	MX_I2C3_Init	I2C3
6	MX_SPI1_Init	SPI1
7	MX_SPI3_Init	SPI3
8	MX_UART4_Init	UART4
9	MX_USART1_UART_Init	USART1
10	MX_USART3_UART_Init	USART3
11	MX_USART6_UART_Init	USART6

Rank	Function Name	Peripheral Instance Name
12	MX_RTC_Init	RTC
13	MX_TIM3_Init	TIM3
14	MX_TIM4_Init	TIM4
15	MX_TIM5_Init	TIM5
16	MX_TIM6_Init	TIM6
17	MX_TIM9_Init	TIM9
18	MX_ADC1_Init	ADC1
19	MX_ADC2_Init	ADC2

3. Peripherals and Middlewares Configuration

3.1. ADC1

mode: IN11

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 11

Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

3.2. ADC2

mode: IN12

3.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 12
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0
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WatchDog:

Enable Analog WatchDog Mode	false
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3.3. I2C1

I2C: I2C

3.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

3.4. I2C3

I2C: I2C

3.4.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
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I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

3.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

3.6. RTC

mode: Activate Clock Source

3.6.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

3.7. SPI1

Mode: Full-Duplex Master

3.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	45.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

3.8. SPI3

Mode: Full-Duplex Master

3.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	22.5 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

3.9. SYS

Debug: Serial Wire

Timebase Source: SysTick

3.10. TIM3

Clock Source : Internal Clock

3.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

3.11. TIM4

mode: Clock Source

3.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

3.12. TIM5

mode: Clock Source

3.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8999 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	99 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

3.13. TIM6

mode: Activated

3.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9 *
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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3.14. TIM9

mode: Clock Source

3.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8999 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	3999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Enable *

3.15. UART4

Mode: Asynchronous

3.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

3.16. USART1

Mode: Asynchronous

3.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

3.17. USART3

Mode: Asynchronous

3.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None

Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

3.18. USART6

Mode: Asynchronous

3.18.1. Parameter Settings:

Basic Parameters:

Baud Rate **9600 ***

Word Length 8 Bits (including Parity)

Parity None

Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	ADC_V
ADC2	PC2	ADC2_IN12	Analog mode	No pull-up and no pull-down	n/a	ADC_C
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI3	PB3	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB4	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB5	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					Very High *	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART3	PC5	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	APOGE_STAT
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUZZER
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	APOGE_STAT_DIS
	PA0-WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	APOGEE_LED
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SENS_RES
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USER_LED
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MAIN_LED
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD_CS
	PC4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SD_CD
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MAIN_MOS
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MAIN_STAT
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MAIN_STAT_DIS
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPS_LED
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IO_1
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IO_0
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FLASH_WP
	PC8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	INT_GYRO
	PA9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	INT_ACC
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RF_AUX
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RF_M0
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RF_M1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FLASH_CS
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	APOGE_MOS
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FLASH_RES

4.2. DMA configuration

DMA request	Stream	Direction	Priority
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream1 global interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
TIM1 break interrupt and TIM9 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
USART3 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
UART4 global interrupt	true	0	0
TIM6 global interrupt and DAC1, DAC2 underrun error interrupts	true	0	0
DMA2 stream1 global interrupt	true	0	0
USART6 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
USART1 global interrupt	unused		
SPI3 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream1 global interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM1 break interrupt and TIM9 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM5 global interrupt	false	true	true
UART4 global interrupt	false	true	true
TIM6 global interrupt and DAC1, DAC2 underrun error interrupts	false	true	true
DMA2 stream1 global interrupt	false	true	true
USART6 global interrupt	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f446_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f446_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f4-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf
Security Bulletin	https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2945-stm8s-and-stm32-mcus-a-consistent-832bit-product-line-for-painless-migration-

stmicroelectronics.pdf

- Application Notes https://www.st.com/resource/en/application_note/an3070-managing-the-driver-enable-signal-for-rs485-and-iolink-communications-with-the-stm32s-usart-stmicroelectronics.pdf
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