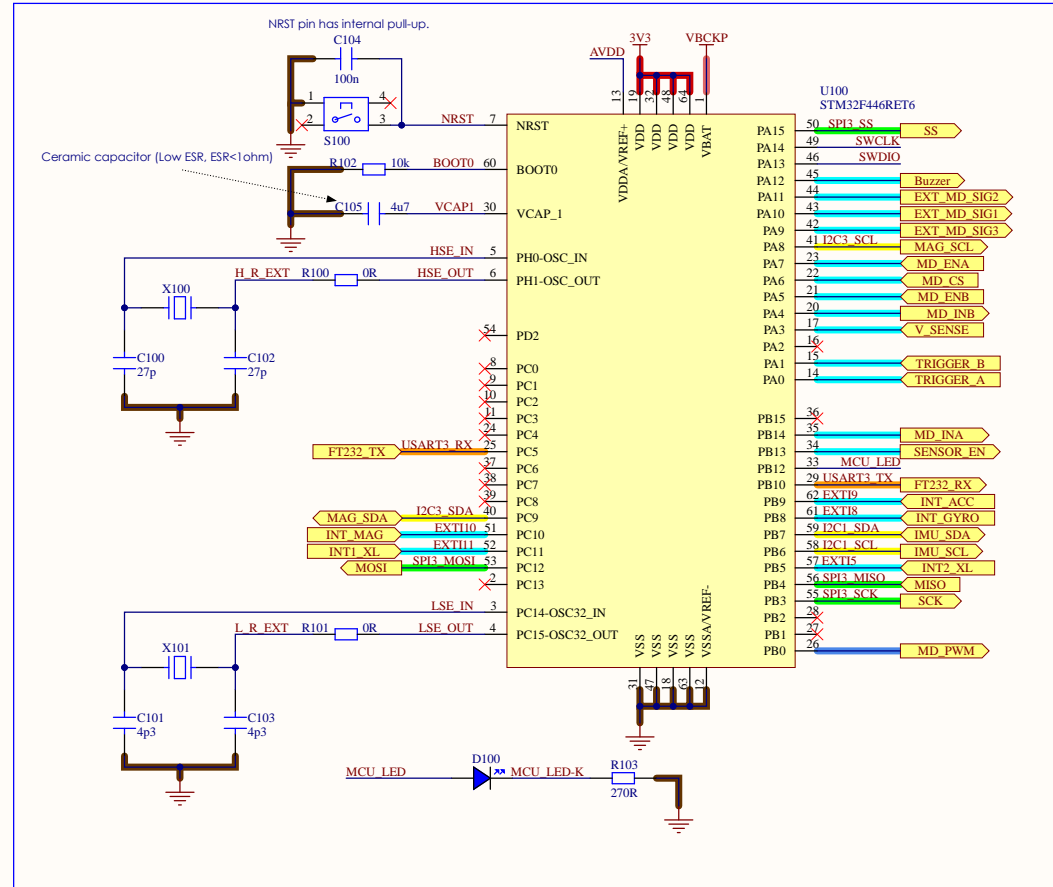
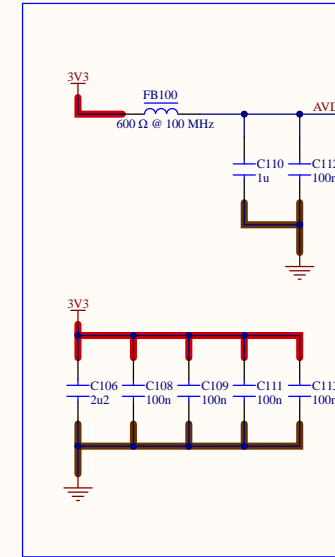


Project: RWHardware.PrjPcb			
Document: Main.SchDoc			
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Designed by: Recep Sağlam			Date: 5.05.2025
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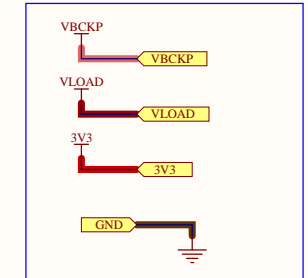
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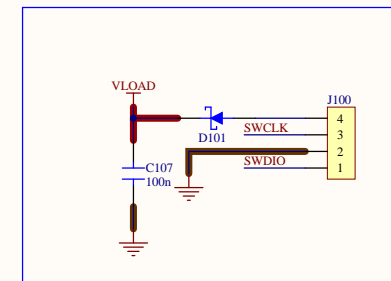
Decoupling Capacitors



Global Ports



ST-LINK V2 Connector



[illegible][illegible]

Phase A Input

Phase B Input

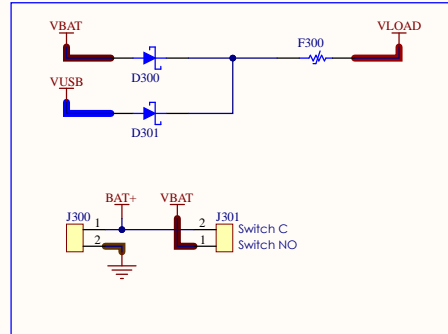
TRIGGER A

TRIGGER B

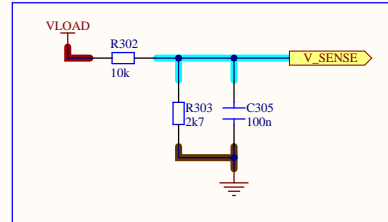
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Figure 1: Schematic diagram of the proposed 12T12R12C architecture. The diagram shows a 3x3 array of crossbar units. Each unit consists of a 3T1R1C1 sub-unit and a 3T1R1C1 sub-unit. The top 3T1R1C1 sub-unit has inputs EXT MD SR0, EXT MD SR2, and EXT MD SR3, and outputs 3, 2, and 1. The bottom 3T1R1C1 sub-unit has inputs Phase B Input1, MD OUTB, and MD OUTA, and outputs 3, 2, and 1. The array is connected to a 12T12R12C architecture, which is a 12x12 crossbar array with 12T12R12C architecture at the bottom.

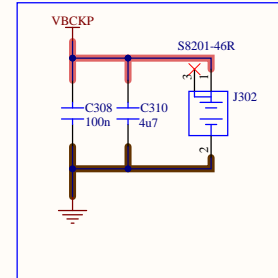
Battery and Switch Connector



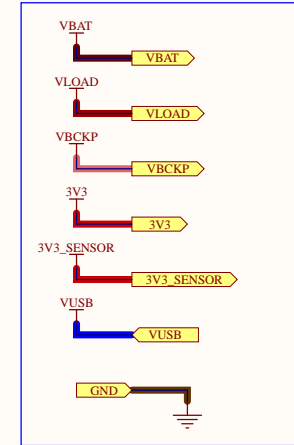
Voltage Sense



Backup Battery



Global Ports



MIC5205-3.3YM5-TR 3V3 Regulator

