Team6_Tests

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Table of Contents

1. AccelPdl

Test File Options

Close open figures	true
Store MATLAB figures	false
Generate report	false

1.1. New Test Suite 1

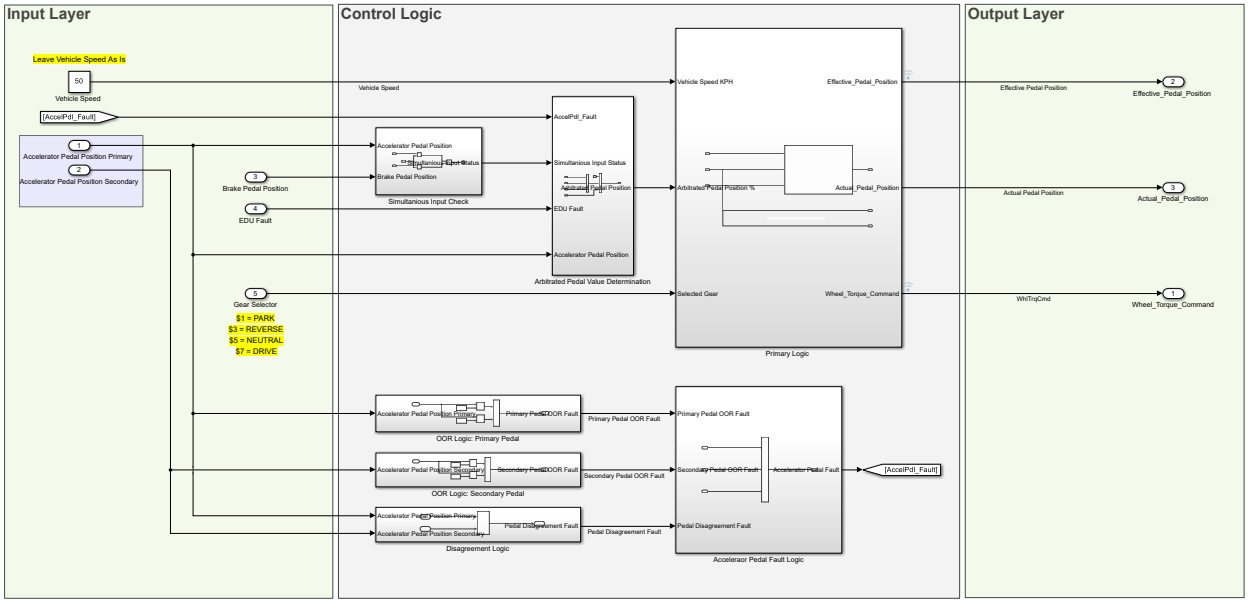
1.1.1. AP1-1_ArbitratedPdlPos0

Test Details

Requirements	• Description: AP 1 If any of the following situations occur, the arbitrated pedal position must be 0. Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Test Arbitrated Position = 0	At any point of time, whenever **SilmInputStatus == logical(1) | EDUfault == logical(1) | AccelPdl_Fault == logical(1)** is true then, with no delay, **ArbitPedalPos == 0** must be true	

Symbols

Symbol	Scope	Metadata
AccelPedalPos	Signal	Name: Accelerator Pedal Position Primary :1 Path: AccelPdl/Accelerator Pedal Position Primary

Symbol	Scope	Metadata
		Port Index: 1 Field/Element:
BrakePedalPos	Signal	Name: Brake Pedal Position:1 Path: AccelPdl/Brake Pedal Position Port Index: 1 Field/Element:
SilmInputStatus	Signal	Name: AND:1 Path: AccelPdl/Simultanious Input Check/AND Port Index: 1 Field/Element:
EDUfault	Signal	Name: EDU Fault:1 Path: AccelPdl/EDU Fault

Symbol	Scope	Metadata
		Port Index: 1 Field/Element:
AccelPdl_Fault	Signal	Name: From:1 Path: AccelPdl/From Port Index: 1 Field/Element:
ArbitPedalPos	Signal	Name: Arbitrated Pedal Position Path: AccelPdl/Arbitrated Pedal Value Determination/Switch Port Index: 1 Field/Element:

1.1.2. AP2-2_ArbitratedPdlPosEqualToPrimary

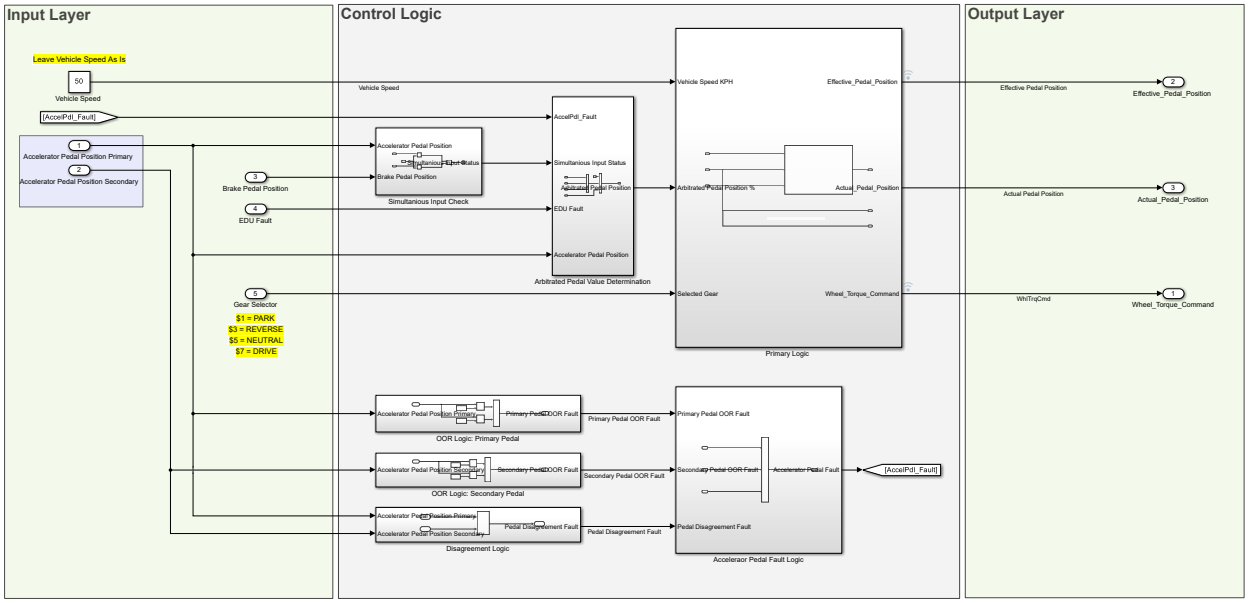
Test Details

Requirements	• Description: AP 2 If none of these situations occur, the Arbitrated Pedal Position must be equal to Ac-

	celerator Pedal Position Primary. Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Test	At any point of time, whenever **SimultaneousInputStatus == logical(0) & EDUFault == logical(0) & AccelPdlFault == logical(0)** is true then, with no delay, **ArbitratedPedalPosition == AcceleratorPrimaryPedalPos** must be true	

Symbols

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td>Simultaneou-
sInputStatus</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Simultanious Input Check:1</td></tr>
<tr><td>Path</td><td>AccelPdl/Simultanious Input Check</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
<tr><td>AccelPdlFault</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>From:1</td></tr>
<tr><td>Path</td><td>AccelPdl/From</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
<tr><td>EDUFault</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>EDU Fault:1</td></tr>
<tr><td>Path</td><td>AccelPdl/EDU Fault</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
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</table>

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td>ArbitratedPedalPosition</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Arbitrated Pedal Position</td></tr>
<tr><td>Path</td><td>AccelPdl/Arbitrated Pedal Value Determination/Switch</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
<tr><td>AcceleratorPrimaryPedalPos</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Accelerator Pedal Position Primary :1</td></tr>
<tr><td>Path</td><td>AccelPdl/Accelerator Pedal Position Primary</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
</table>

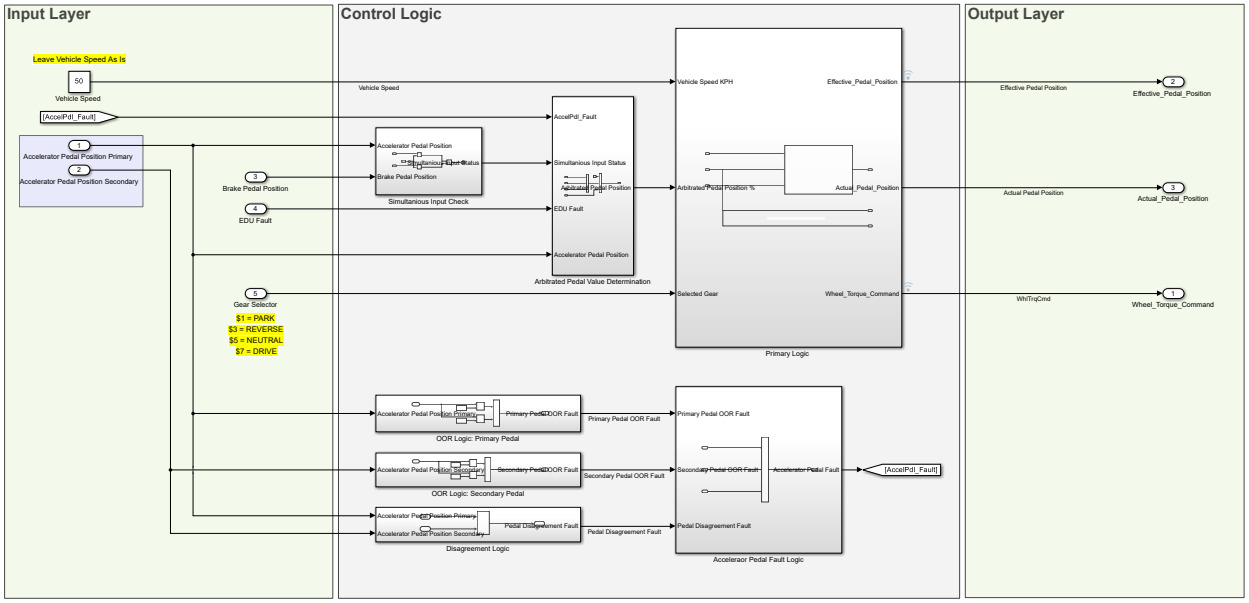
1.1.3. AP3-3_EffAndActualPdlPosEqualToArbPdlPos

Test Details

Requirements	• Description: AP 3 Effective Pedal Position and Actual Pedal Position Must Always Equal Arbitrated Pedal Position Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	EffectivePedalPos = ArbitratedPedalPos	At any point of time, **EffectivePedalPos == ArbitratedPedalPos** must be true	
True	ActualPedalPos = ArbitratedPedalPos	At any point of time, **ActualPedalPos == ArbitratedPedalPos** must be true	

Symbols

Symbol	Scope	Metadata
EffectivePedalPos	Signal	Name: Effective Pedal Position Path: AccelPdl/Primary Logic

Symbol	Scope	Metadata
		Port Index: 1 Field/Element:
ArbitratedPedalPos	Signal	Name: Arbitrated Pedal Position Path: AccelPdl/Arbitrated Pedal Value Determination/Switch Port Index: 1 Field/Element:
ActualPedalPos	Signal	Name: Actual Pedal Position Path: AccelPdl/Primary Logic Port Index: 2 Field/Element:

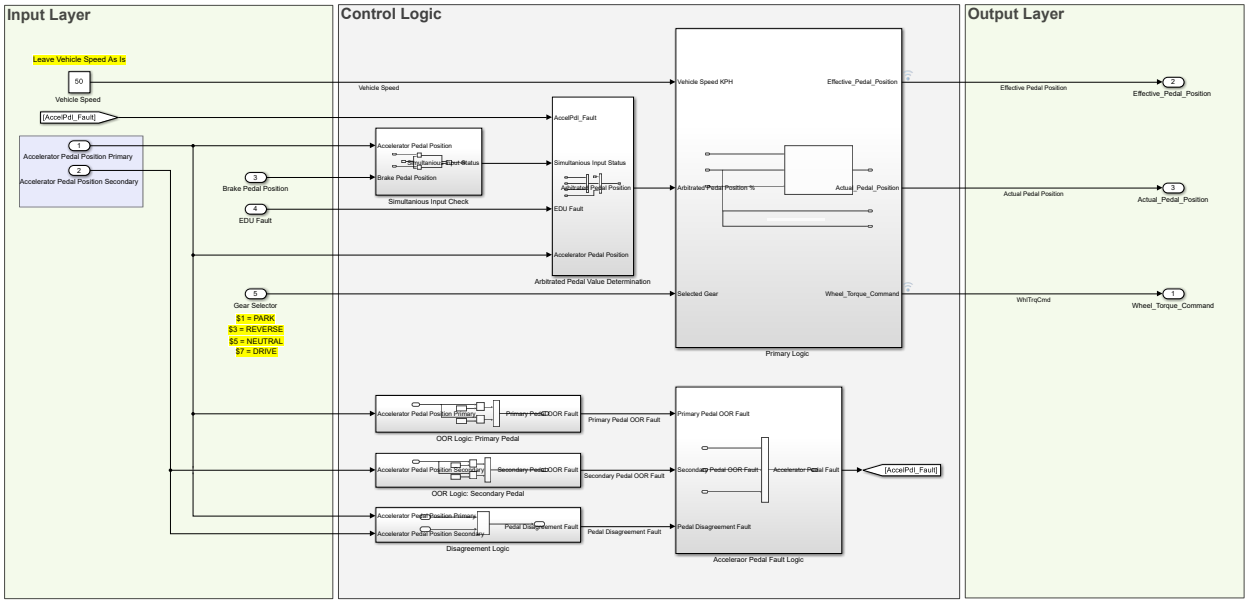
1.1.4. AP4-4_0TorqueNeutral

Test Details

Requirements	• Description: AP 4 0 torque if accelerator pedal is pressed and the vehicle is in neutral Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assessment1	At any point of time, whenever **ArbitratedPdlPos ~= 0 & GearSelector == 5** is true then, with no delay, **WheelTorque == 0** must be true	

Symbols

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td>GearSelector</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Gear Selector:1</td></tr>
<tr><td>Path</td><td>AccelPdl/Gear Selector</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
<tr><td>WheelTorque</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>WhlTrqCmd</td></tr>
<tr><td>Path</td><td>AccelPdl/Primary Logic</td></tr>
<tr><td>Port Index</td><td>3</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
<tr><td>ArbitratedPdl-Pos</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Arbitrated Pedal Position</td></tr>
<tr><td>Path</td><td>AccelPdl/Arbitrated Pedal Value Determination/Switch</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
</table>

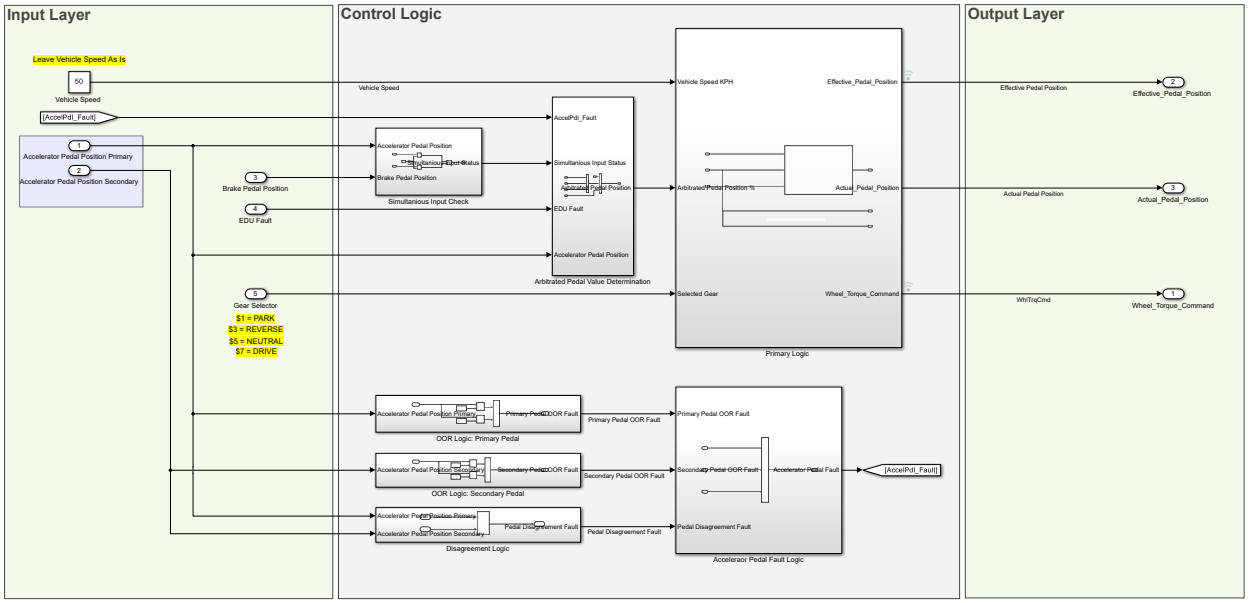
1.1.5. AP5-5_0TorquePark

Test Details

Requirements	• Description: AP 5 0 torque if accelerator pedal is pressed and vehicle is in park Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assessment1	At any point of time, whenever **ArbitratedPdlPos ~= 0 & GearSelector == 1** is true then, with no delay, **WheelTorque == 0** must be true	

Symbols

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td>GearSelector</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Gear Selector:1</td></tr>
<tr><td>Path</td><td>AccelPdl/Gear Selector</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
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</td></tr>
<tr><td>WheelTorque</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>WhlTrqCmd</td></tr>
<tr><td>Path</td><td>AccelPdl/Primary Logic</td></tr>
<tr><td>Port Index</td><td>3</td></tr>
<tr><td>Field/Element</td><td></td></tr>
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</td></tr>
<tr><td>ArbitratedPdl-Pos</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Arbitrated Pedal Position</td></tr>
<tr><td>Path</td><td>AccelPdl/Arbitrated Pedal Value Determination/Switch</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
</table>

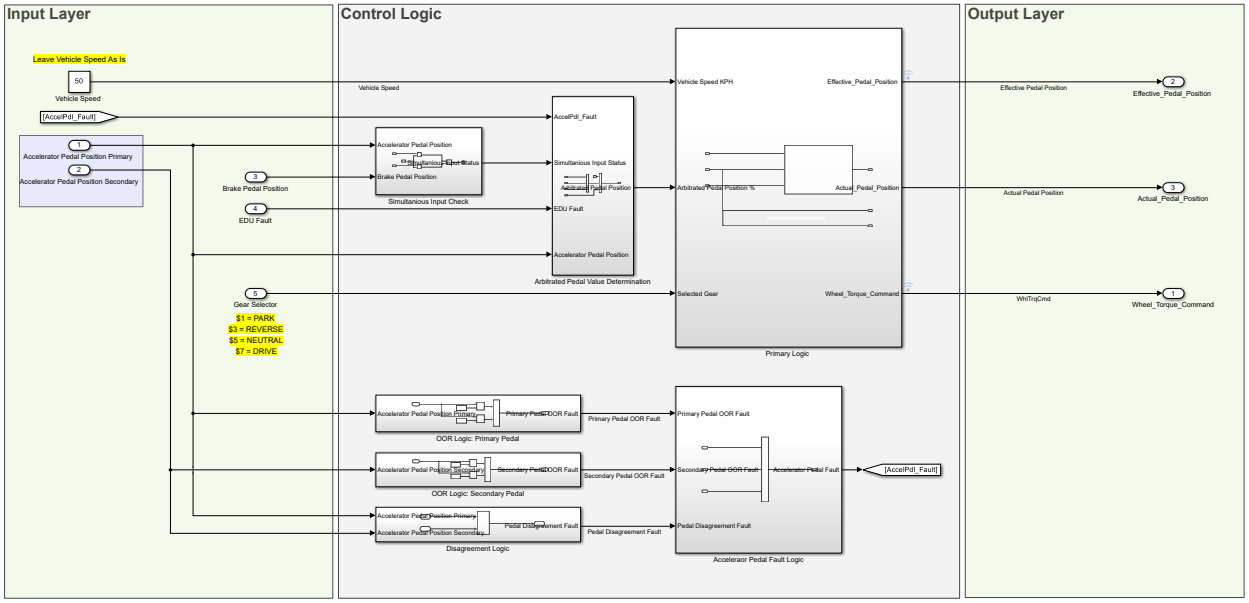
1.1.6. AP6-6_PositiveTorque

Test Details

Requirements	• Description: AP 6 Torque is positive in drive Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assessment1	At any point of time, whenever **GearSelector == 7** is true then, with no delay, **WheelTorque > 0** must be true	

Symbols

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td>GearSelector</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Gear Selector:1</td></tr>
<tr><td>Path</td><td>AccelPdl/Gear Selector</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
<tr><td>WheelTorque</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>WhlTrqCmd</td></tr>
<tr><td>Path</td><td>AccelPdl/Primary Logic</td></tr>
<tr><td>Port Index</td><td>3</td></tr>
<tr><td>Field/Element</td><td></td></tr>
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</td></tr>
</table>

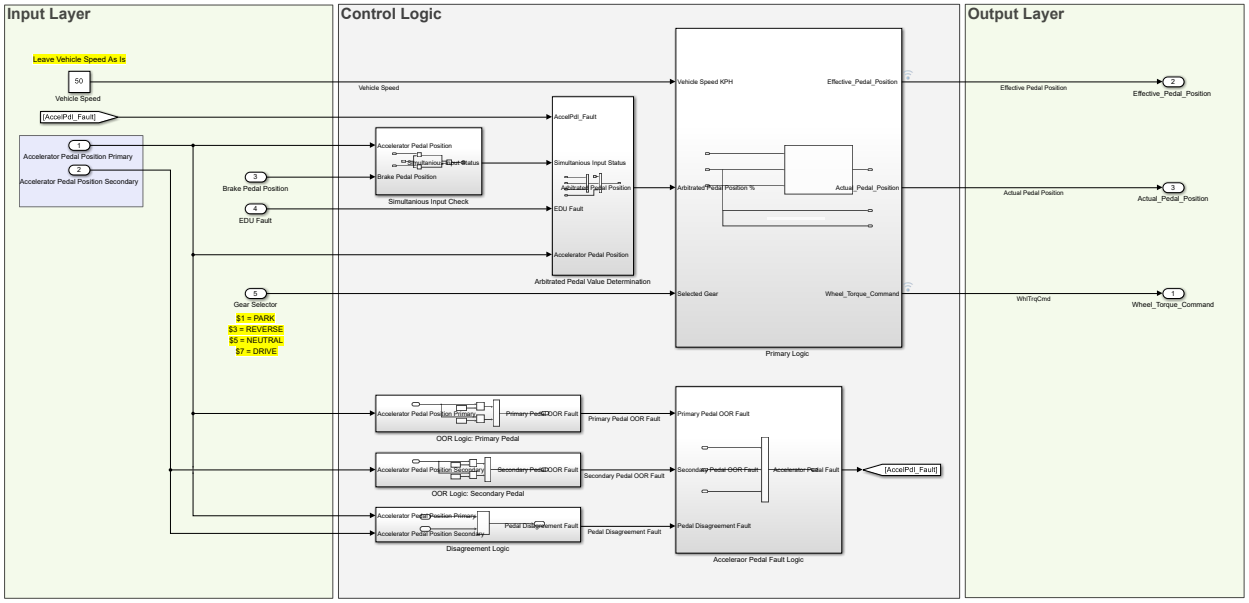
1.1.7. AP7-7_NegativeTorque

Test Details

Requirements	• Description: AP 7 Torque is negative in reverse Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assess-ment1	At any point of time, whenever **GearSelector == 3** is true then, with no delay, **WheelTorque < 0** must be true	

Symbols

Symbol	Scope	Metadata
GearSelector	Signal	Name: Gear Selector:1 Path: AccelPdl/Gear Selector Port Index: 1

Symbol	Scope	Metadata
		Field/Element:
WheelTorque	Signal	Name: WhlTrqCmd Path: AccelPdl/Primary Logic Port Index: 3 Field/Element:

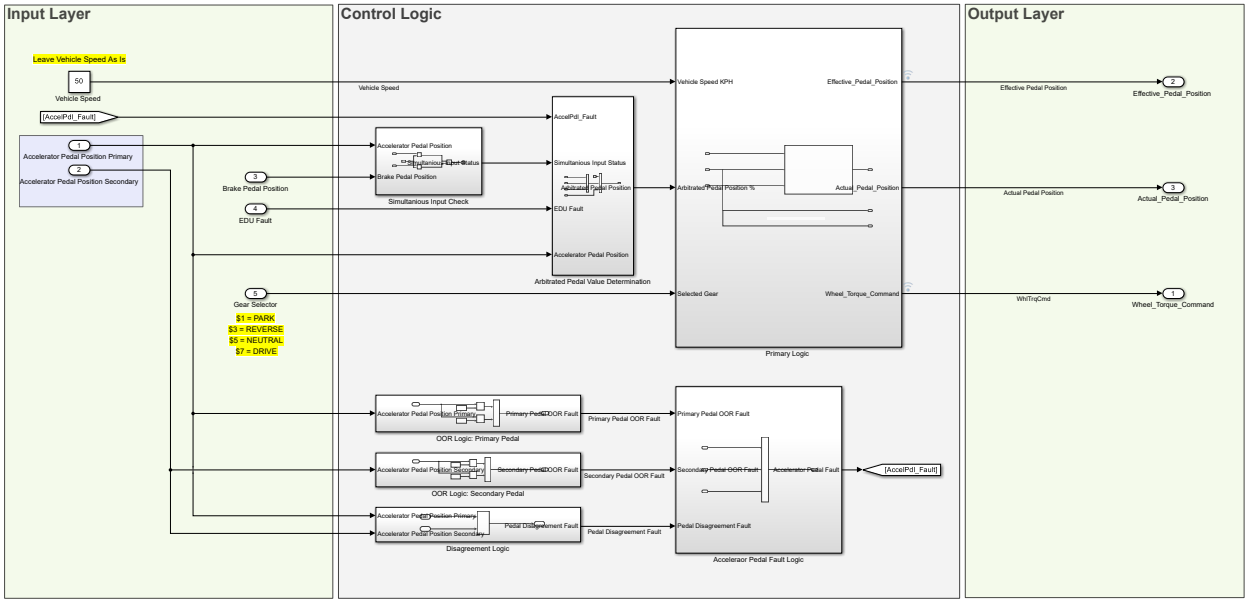
1.1.8. AP8-8_DisagreementFault1

Test Details

Requirements	• Description: AP 8 Disagreement fault is 1 if Accelerator Pedal position primary and secondary are different Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assessment1	At any point of time, whenever **AccelPedposPri ~= AccelPedposSec** is true then, with no delay, **DisagreementFault == logical(1)** must be true	

Symbols

Symbol	Scope	Metadata
AccelPedposPri	Signal	Name: Accelerator Pedal Position Primary:1 Path: AccelPdl/Disagreement Logic/Accelerator Pedal Position Primary

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td></td><td></td><td><table>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/
Element</td><td></td></tr>
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<tr><td>AccelPedpos-
Sec</td><td>Signal</td><td><table>
<tr><td>Name</td><td>Accelerator Pedal Position Secon-
dary:1</td></tr>
<tr><td>Path</td><td>AccelPdl/Disagreement Logic/Ac-
celerator Pedal Position Secon-
dary</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/
Element</td><td></td></tr>
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<tr><td>Disagree-
mentFault</td><td>Signal</td><td><table>
<tr><td>Name</td><td>NotEqual:1</td></tr>
<tr><td>Path</td><td>AccelPdl/Disagreement Log-
ic/NotEqual</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
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</table>

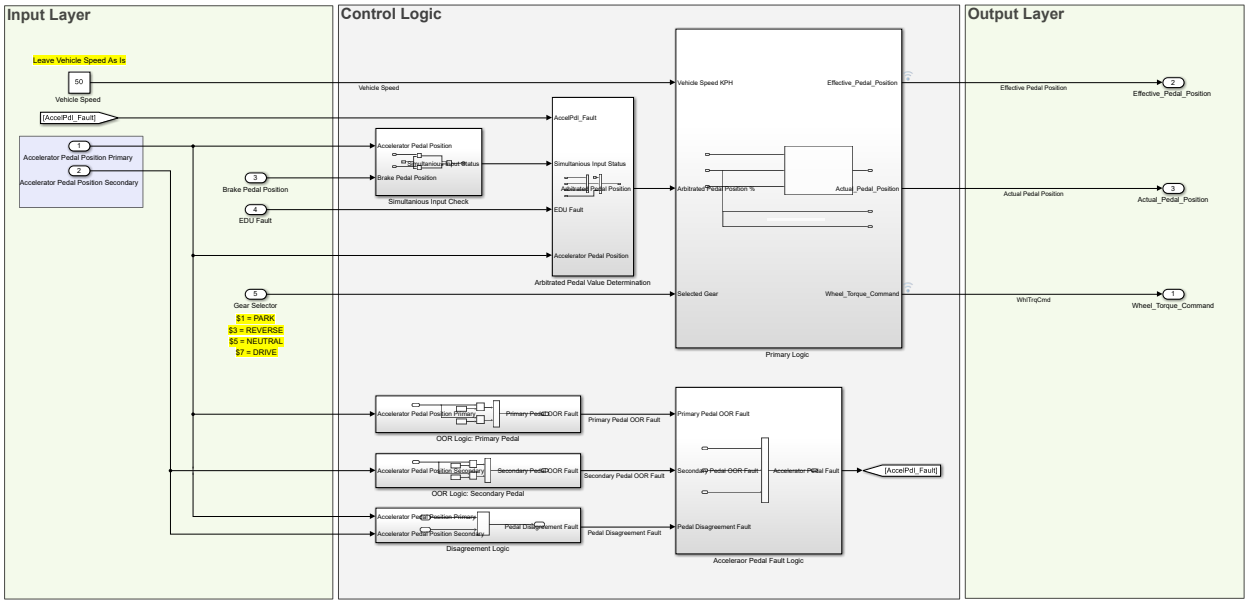
1.1.9. AP9-9_PrimaryOutOfRangeFault1

Test Details

Requirements	• Description: AP 9 Primary Out of Range Fault is 1 if Primary Pedal Position is less than 0 or greater than 100 Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assessment1	At any point of time, whenever **AccelPdlPosPri < 0 | AccelPdlPosPri > 100** is true then, with no delay, **PrimaryOOR == logical(1)** must be true	

Symbols

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td>AccelPdlPos-Pri</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Accelerator Pedal Position Primary:1</td></tr>
<tr><td>Path</td><td>AccelPdl/OOR Logic: Primary Pedal/Accelerator Pedal Position Primary</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/ Element</td><td></td></tr>
</table>
</td></tr>
<tr><td>PrimaryOOR</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>OR:1</td></tr>
<tr><td>Path</td><td>AccelPdl/OOR Logic: Primary Pedal/OR</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
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1.1.10. AP10-10_SecondaryOutOfRangeFault1

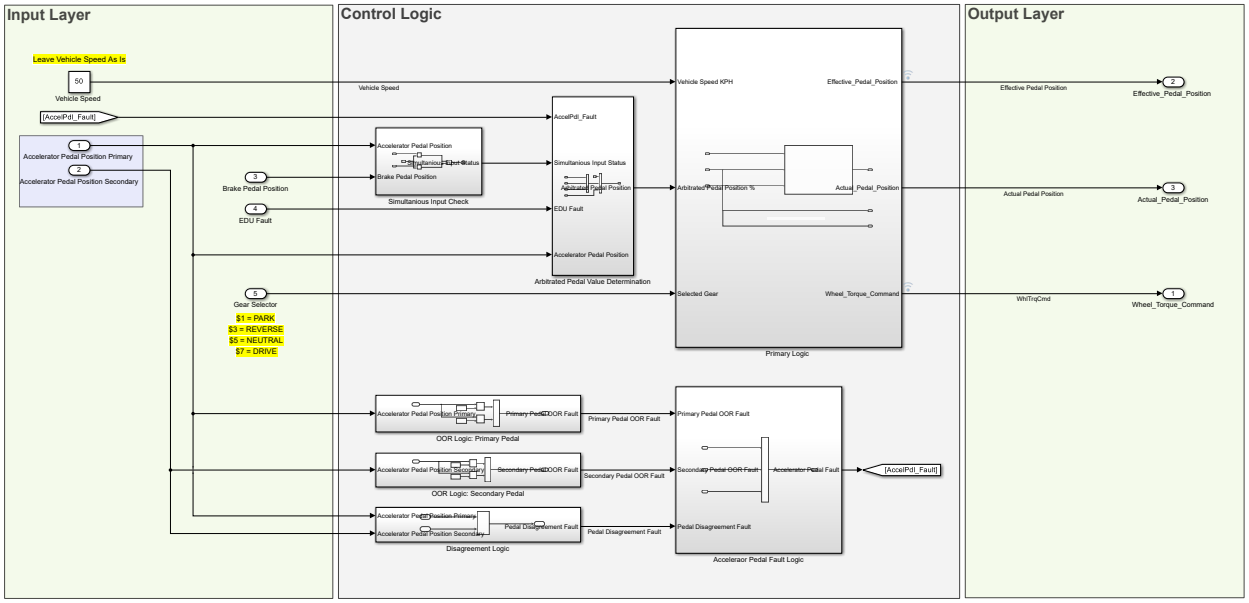
Test Details

Requirements	• Description: AP 10 Secondary Out of Range Fault is 1 if Secondary Pedal Position is less than 0 or

	greater than 100 Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assessment1	At any point of time, whenever **AccelPdlPosSec < 0 | AccelPdlPosSec > 100** is true then, with no delay, **SecondaryOOR == logical(1)** must be true	

Symbols

<table>
<tr><th>Symbol</th><th>Scope</th><th>Metadata</th></tr>
<tr><td>AccelPdlPos-Sec</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>Accelerator Pedal Position Secon-dary:1</td></tr>
<tr><td>Path</td><td>AccelPdl/OOR Logic: Secondary Pedal/Accelerator Pedal Position Secondary</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/ Element</td><td></td></tr>
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</td></tr>
<tr><td>Secondar-yOOR</td><td>Signal</td><td>
<table>
<tr><td>Name</td><td>OR:1</td></tr>
<tr><td>Path</td><td>AccelPdl/OOR Logic: Secondary Pedal/OR</td></tr>
<tr><td>Port Index</td><td>1</td></tr>
<tr><td>Field/Element</td><td></td></tr>
</table>
</td></tr>
</table>

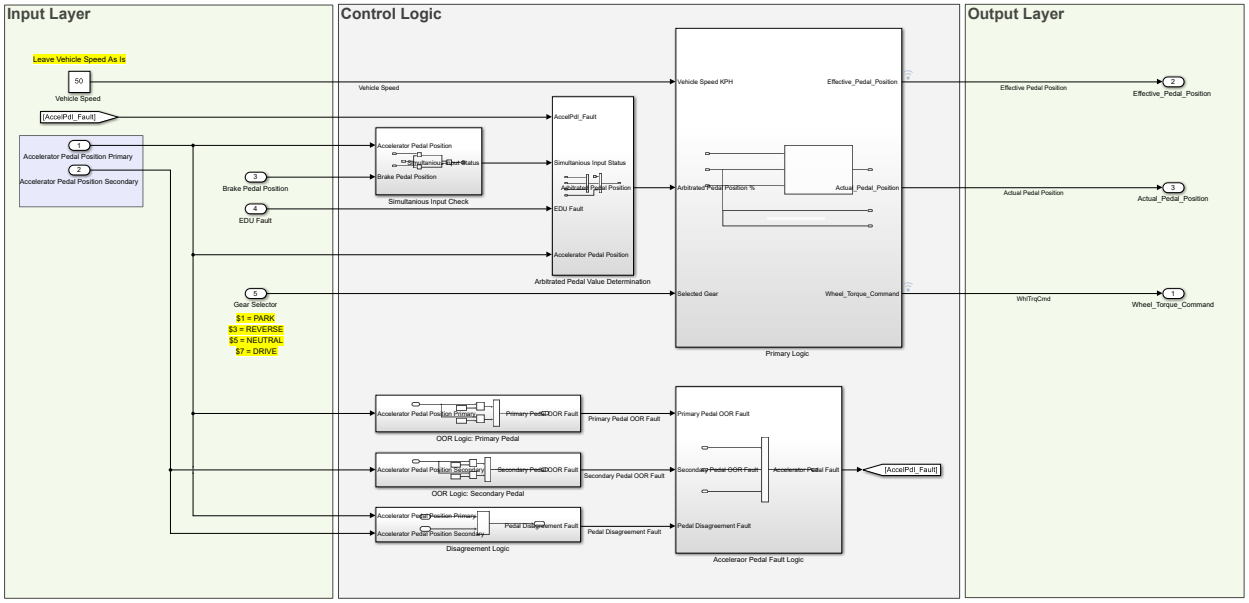
1.1.11. AP11-11_AcceleratorPedalFault1

Test Details

Requirements	• Description: AP 11 Accelerator Pedal Fault is 1 if any of the faults occur Document: Accel_Pdl.slreqx

System Under Test

Model Name: AccelPdl



Simulation Settings Overrides

Simulation Mode	[Model Settings]
Releases	Current
Start Time	0
Stop Time	33

External Inputs

Name	File Path	Status
ModelInputs.mat (Active)	C:\Users\yakub\Desktop\PETER\Projects\pcm-dev-challenge-y3\ModelInputs.mat	Successfully mapped inputs.

Output Triggers

Start Logging	On simulation start
Stop Logging	When simulation stops
Shift time to zero	True

Configuration Settings Overrides

Configuration settings	Do not override model settings

Logical and Temporal Assessments

Assessments

Enabled	Name	Definition	Requirements
True	Assessment1	At any point of time, whenever **PrimaryOOR == logical(1) | SecondaryOOR == logical(1) | PedalDisagreement == logical(1)** is true then, with no delay, **AccelPdlFault == logical(1)** must be true	

Symbols

Symbol	Scope	Metadata
PrimaryOOR	Signal	Name: Primary Pedal OOR Fault:1 Path: AccelPdl/Acceleraor Pedal Fault Logic/Primary Pedal OOR Fault

Symbol	Scope	Metadata
		Port Index: 1 Field/Element:
Secondar-yOOR	Signal	Name: Secondary Pedal OOR Fault:1 Path: AccelPdl/Acceleraor Pedal Fault Logic/Secondary Pedal OOR Fault Port Index: 1 Field/Element:
PedalDisa-greement	Signal	Name: Pedal Disagreement Fault:1 Path: AccelPdl/Acceleraor Pedal Fault Logic/Pedal Disagreement Fault Port Index: 1 Field/Element:
AccelPdl-Fault	Signal	Name: Accelerator Pedal Fault

Symbol	Scope	Metadata
		<table><tr><td>Path</td><td>AccelPdl/Acceleraor Pedal Fault Logic/OR</td></tr><tr><td>Port Index</td><td>1</td></tr><tr><td>Field/Element</td><td></td></tr></table>