

## 1. Description

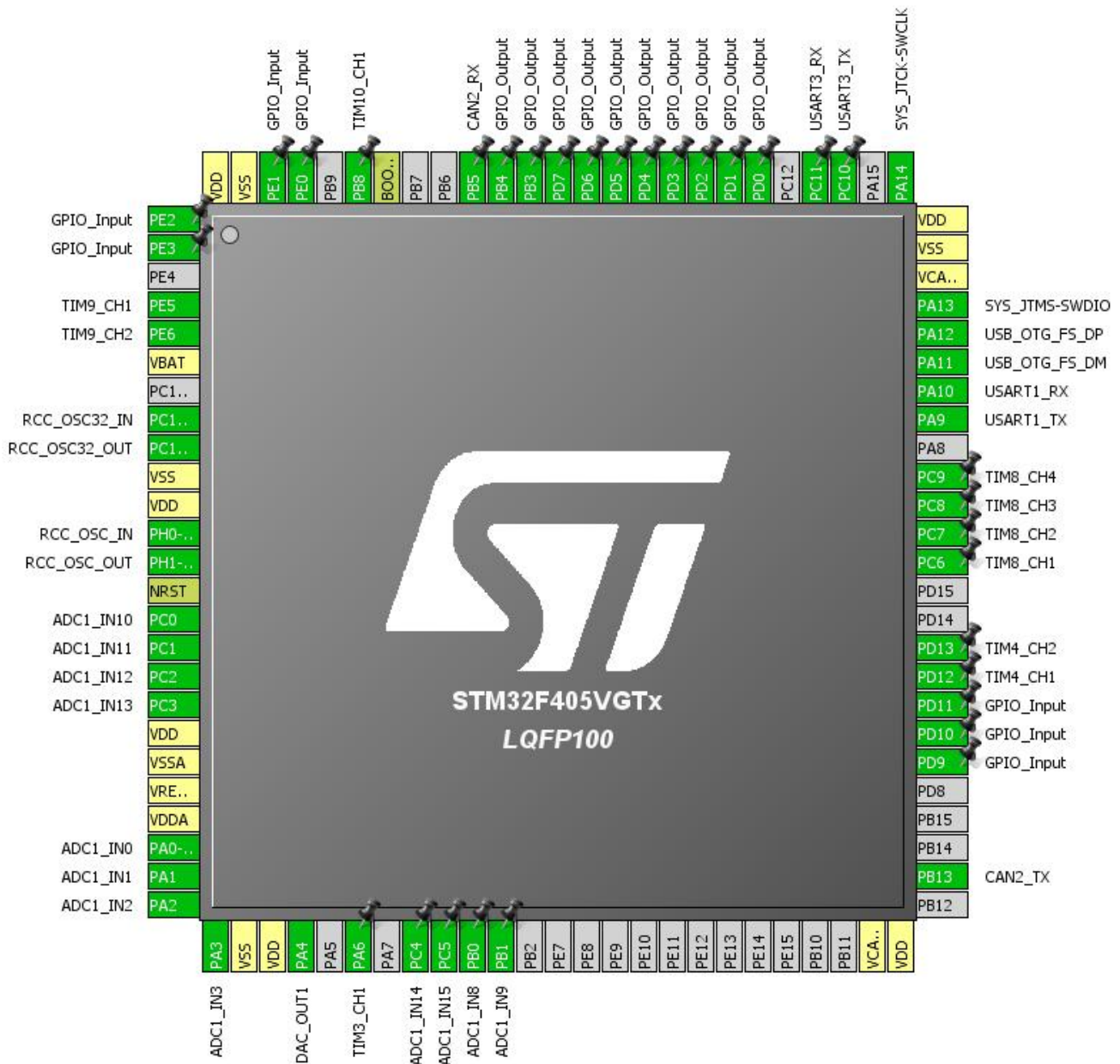
### 1.1. Project

Project Name	SkyPulse
Board Name	SkyPulse
Generated with:	STM32CubeMX 4.24.0
Date	02/07/2018

### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405VGTx
MCU Package	LQFP100
MCU Pin number	100

## 2. Pinout Configuration



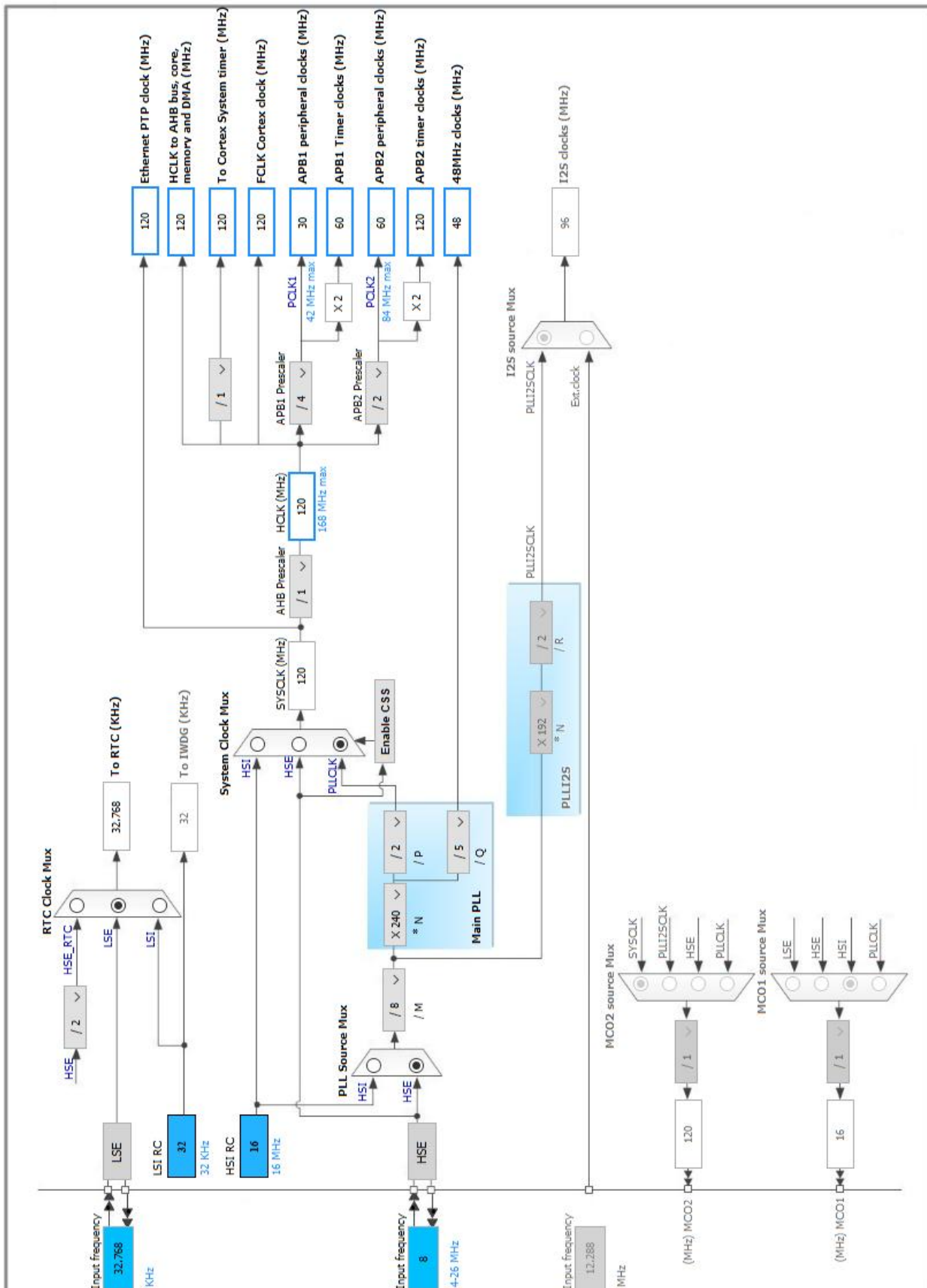
### 3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	FSW2
2	PE3 *	I/O	GPIO_Input	FSW3
4	PE5	I/O	TIM9_CH1	FAN_TACHO1
5	PE6	I/O	TIM9_CH2	FAN_TACHO2
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_IN10	Psense0
16	PC1	I/O	ADC1_IN11	Psense1
17	PC2	I/O	ADC1_IN12	Psense2
18	PC3	I/O	ADC1_IN13	Psense3
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	PUMP_CSENSE
24	PA1	I/O	ADC1_IN1	T1_H2O
25	PA2	I/O	ADC1_IN2	T1_H2O
26	PA3	I/O	ADC1_IN3	_5V
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	DAC_OUT1	
31	PA6	I/O	TIM3_CH1	PUMP_TACHO
33	PC4	I/O	ADC1_IN14	Dsense1
34	PC5	I/O	ADC1_IN15	Dsense2
35	PB0	I/O	ADC1_IN8	_12V
36	PB1	I/O	ADC1_IN9	_24V
49	VCAP_1	Power		
50	VDD	Power		
52	PB13	I/O	CAN2_TX	
56	PD9 *	I/O	GPIO_Input	cwbBUTTON

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
57	PD10 *	I/O	GPIO_Input	cwbDOOR
58	PD11 *	I/O	GPIO_Input	cwbENGM
59	PD12	I/O	TIM4_CH1	_LED1
60	PD13	I/O	TIM4_CH2	_LED2
63	PC6	I/O	TIM8_CH1	_BOTTLE_OUT
64	PC7	I/O	TIM8_CH2	_BOTTLE_IN
65	PC8	I/O	TIM8_CH3	_AIR
66	PC9	I/O	TIM8_CH4	_WATER
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	USART3_TX	
79	PC11	I/O	USART3_RX	
81	PD0 *	I/O	GPIO_Output	_RED1
82	PD1 *	I/O	GPIO_Output	_GREEN1
83	PD2 *	I/O	GPIO_Output	_YELLOW1
84	PD3 *	I/O	GPIO_Output	_BLUE1
85	PD4 *	I/O	GPIO_Output	_RED2
86	PD5 *	I/O	GPIO_Output	_GREEN2
87	PD6 *	I/O	GPIO_Output	_YELLOW2
88	PD7 *	I/O	GPIO_Output	_BLUE2
89	PB3 *	I/O	GPIO_Output	_12Voff
90	PB4 *	I/O	GPIO_Output	_SYS_SHG
91	PB5	I/O	CAN2_RX	
94	BOOT0	Boot		
95	PB8	I/O	TIM10_CH1	FAN_PWM
97	PE0 *	I/O	GPIO_Input	FSW0
98	PE1 *	I/O	GPIO_Input	FSW1
99	VSS	Power		
100	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. IPs and Middleware Configuration

### 5.1. ADC1

mode: IN0

mode: IN1

mode: IN2

mode: IN3

mode: IN8

mode: IN9

mode: IN10

mode: IN11

mode: IN12

mode: IN13

mode: IN14

mode: IN15

#### 5.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler **PCLK2 divided by 4 \***

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment **Left alignment \***

Scan Conversion Mode **Enabled \***

Continuous Conversion Mode **Enabled \***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled \***

End Of Conversion Selection EOC flag at the end of single channel conversion

##### ADC\_Regular\_ConversionMode:

Number Of Conversion **12 \***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 0

Sampling Time 3 Cycles

<u>Rank</u>	<b>2 *</b>
Channel	<b>Channel 1 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>3 *</b>
Channel	<b>Channel 2 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>4 *</b>
Channel	<b>Channel 3 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>5 *</b>
Channel	<b>Channel 8 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>6 *</b>
Channel	<b>Channel 9 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>7 *</b>
Channel	<b>Channel 10 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>8 *</b>
Channel	<b>Channel 11 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>9 *</b>
Channel	<b>Channel 12 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>10 *</b>
Channel	<b>Channel 13 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>11 *</b>
Channel	<b>Channel 14 *</b>
Sampling Time	3 Cycles
<u>Rank</u>	<b>12 *</b>
Channel	<b>Channel 15 *</b>
Sampling Time	3 Cycles
<b>ADC_Injected_ConversionMode:</b>	
Number Of Conversions	0
<b>WatchDog:</b>	
Enable Analog WatchDog Mode	false

## 5.2. CAN2

mode: Mode

### 5.2.1. Parameter Settings:

#### Bit Timings Parameters:

Prescaler (for Time Quantum)	4 *
Time Quantum	133.33333333333334 *
Time Quanta in Bit Segment 1	10 Times *
Time Quanta in Bit Segment 2	4 Times *
Time for one Bit	2000 *
ReSynchronization Jump Width	4 Times *

#### Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Enable *
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Enable *

#### Advanced Parameters:

Operating Mode	Normal
----------------	--------

## 5.3. DAC

mode: OUT1 Configuration

### 5.3.1. Parameter Settings:

#### DAC Out1 Settings:

Output Buffer	Enable
Trigger	Timer 8 Trigger Out event *
Wave generation mode	Disabled



## 5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

### 5.4.1. Parameter Settings:

#### System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

#### RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

#### Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
-------------------------------	---------------------------------

## 5.5. RTC

mode: Activate Clock Source

mode: Activate Calendar

### 5.5.1. Parameter Settings:

#### General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

#### Calendar Time:

Data Format	Binary data format *
Hours	15 *
Minutes	30 *
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Set *

#### Calendar Date:

Week Day	<b>Tuesday *</b>
Month	<b>November *</b>
Date	<b>7 *</b>
Year	<b>17 *</b>

## 5.6. SYS

**Debug: Serial Wire**

**Timebase Source: TIM2**

## 5.7. TIM3

**Channel1: Input Capture direct mode**

### 5.7.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>60 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	0
Internal Clock Division (CKD)	No Division

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	<b>Update Event *</b>

#### Input Capture Channel 1:

Polarity Selection	<b>Both Edges *</b>
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	<b>15 *</b>

## 5.8. TIM4

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

### 5.8.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>75 *</b>
Internal Clock Division (CKD)	No Division

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

#### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

## 5.9. TIM8

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 5.9.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>29 *</b>
Counter Mode	<b>Center Aligned mode1 *</b>
Counter Period (AutoReload Register - 16 bits value )	<b>__PWMRATE *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode	<b>Enable (sync between this TIM (Master) and its Slaves (through TRGO)) *</b>
-------------------	--

Trigger Event Selection

**Update Event \***

**Break And Dead Time management - BRK Configuration:**

BRK State	Disable
BRK Polarity	High

**Break And Dead Time management - Output Configuration:**

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

**PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

**PWM Generation Channel 2:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

**PWM Generation Channel 3:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

**PWM Generation Channel 4:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

## 5.10. TIM9

**mode: Clock Source**

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

### 5.10.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>60 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	0
Internal Clock Division (CKD)	No Division

#### Input Capture Channel 1:

Polarity Selection	<b>Both Edges *</b>
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	<b>15 *</b>

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

## 5.11. TIM10

mode: Activated

Channel1: PWM Generation CH1

### 5.11.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>29 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>__PWMRATE *</b>
Internal Clock Division (CKD)	No Division

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	<b>10 *</b>
Fast Mode	Disable
CH Polarity	High

## 5.12. USART1

Mode: Asynchronous

### 5.12.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 5.13. USART3

Mode: Asynchronous

### 5.13.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	<b>57600 *</b>
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 5.14. USB\_OTG\_FS

Mode: Device\_Only

### 5.14.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled

Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

## 5.15. FATFS

**mode: User-defined**

### 5.15.1. Set Defines:

#### Version:

FATFS version	R0.12c
---------------	--------

#### Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

#### Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	<b>Enabled with dynamic working buffer on the STACK *</b>
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	<b>Enabled with f_getcwd *</b>

#### Physical Drive Parameters:

VOLUMES (Logical drives)	<b>2 *</b>
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

#### System Parameters:

FS_TINY (Tiny mode)	Disabled
---------------------	----------

FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

## 5.16. FREERTOS

**mode: Enabled**

### 5.16.1. Config parameters:

#### Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

#### Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

#### Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	<b>0x10000 *</b>
Memory Management scheme	



## heap\_2 \*

### Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Enabled *
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Option2 *

### Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

### Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

### Software timer definitions:

USE_TIMERS	Disabled
------------	----------

### Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

## 5.16.2. Include parameters:

### Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled

xTaskGetHandle

Disabled

## 5.17. USB\_DEVICE

### Class For FS IP: Communication Device Class (Virtual Port Com)

#### 5.17.1. Parameter Settings:

##### Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

##### Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

#### 5.17.2. Device Descriptor:

##### Device Descriptor:

VID (Vendor Identifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

##### Device Descriptor FS:

PID (Product Identifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

\* User modified value

## 6. System Configuration

### 6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	Psense0
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	Psense1
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	Psense2
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	Psense3
	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	PUMP_CSENSE
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	T1_H2O
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	T1_H2O
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	_5V
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	Dsense1
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	Dsense2
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	_12V
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	_24V
CAN2	PB13	CAN2_TX	Alternate Function Push Pull	<b>Pull-up *</b>	<b>Very High *</b>	
	PB5	CAN2_RX	Alternate Function Push Pull	<b>Pull-up *</b>	<b>Very High *</b>	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	<b>Pull-up *</b>	Low	PUMP_TACHO
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High *</b>	_LED1
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b>	_LED2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	High *	_BOTTLE_OUT
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	High *	_BOTTLE_IN
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	High *	_AIR
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	High *	_WATER
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	Pull-up *	Low	FAN_TACHO1
	PE6	TIM9_CH2	Alternate Function Push Pull	Pull-up *	Low	FAN_TACHO2
TIM10	PB8	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	High *	FAN_PWM
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	Very High *	
USART3	PC10	USART3_TX	Alternate Function Push Pull	Pull-up	Very High *	
	PC11	USART3_RX	Alternate Function Push Pull	Pull-up	Very High *	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	Pull-down *	Very High *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	Pull-down *	Very High *	
GPIO	PE2	GPIO_Input	Input mode	Pull-up *	n/a	FSW2
	PE3	GPIO_Input	Input mode	Pull-up *	n/a	FSW3
	PD9	GPIO_Input	Input mode	Pull-down *	n/a	cwbBUTTON
	PD10	GPIO_Input	Input mode	Pull-down *	n/a	cwbDOOR
	PD11	GPIO_Input	Input mode	Pull-down *	n/a	cwbENGM
	PD0	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_RED1
	PD1	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_GREEN1
	PD2	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_YELLOW1
	PD3	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_BLUE1
	PD4	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_RED2
	PD5	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_GREEN2
	PD6	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_YELLOW2
	PD7	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_BLUE2
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	_12Voff
	PB4	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	_SYS_SHG

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE0	GPIO_Input	Input mode	<b>Pull-up *</b>	n/a	FSW0
	PE1	GPIO_Input	Input mode	<b>Pull-up *</b>	n/a	FSW1

## 6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
TIM4_UP	DMA1_Stream6	Memory To Peripheral	Low
TIM8_UP	DMA2_Stream1	Memory To Peripheral	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream3	Memory To Peripheral	Low
DAC1	DMA1_Stream5	Memory To Peripheral	Low
USART1_RX	DMA2_Stream5	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low

### ADC1: DMA2\_Stream0 DMA request Settings:

Mode: **Circular \***  
 Use fifo: Disable  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: Half Word

### TIM4\_UP: DMA1\_Stream6 DMA request Settings:

Mode: Normal  
 Use fifo: **Enable \***  
 FIFO Threshold: Full  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: Half Word  
 Memory Data Width: **Byte \***  
 Peripheral Burst Size: Single  
 Memory Burst Size: Single

### TIM8\_UP: DMA2\_Stream1 DMA request Settings:

Mode: **Circular \***  
 Use fifo: **Enable \***  
 FIFO Threshold: Full  
 Peripheral Increment: Disable

Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: **Word \***  
Peripheral Burst Size: Single  
Memory Burst Size: Single

USART3\_RX: DMA1\_Stream1 DMA request Settings:

Mode: **Circular \***  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

USART3\_TX: DMA1\_Stream3 DMA request Settings:

Mode: Normal  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

DAC1: DMA1\_Stream5 DMA request Settings:

Mode: **Circular \***  
Use fifo: **Enable \***  
FIFO Threshold: Full  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word  
Peripheral Burst Size: Single  
Memory Burst Size: Single

USART1\_RX: DMA2\_Stream5 DMA request Settings:

Mode: **Circular \***

Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

USART1\_TX: DMA2\_Stream7 DMA request Settings:

Mode: Normal  
Use fifo: Disable  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte



### 6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
TIM1 break interrupt and TIM9 global interrupt	true	5	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	5	0
USART1 global interrupt	true	5	0
USART3 global interrupt	true	5	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream1 global interrupt	true	5	0
CAN2 TX interrupts	true	5	0
CAN2 RX0 interrupts	true	5	0
CAN2 SCE interrupt	true	5	0
USB On The Go FS global interrupt	true	5	0
DMA2 stream5 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM4 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts		unused	
CAN2 RX1 interrupt		unused	
FPU global interrupt		unused	

\* User modified value

## 7. Power Consumption Calculator report

### 7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405VGTx
Datasheet	022152_Rev8

### 7.2. Parameter Selection

Temperature	25
Vdd	3.3

## 8. Software Project

### 8.1. Project Settings

Name	Value
Project Name	SkyPulse
Project Folder	C:\Users\Mocnik\Desktop\skyCube\CubeMx
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.18.0

### 8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

## ***9. Software Pack Report***