MINI MIPS

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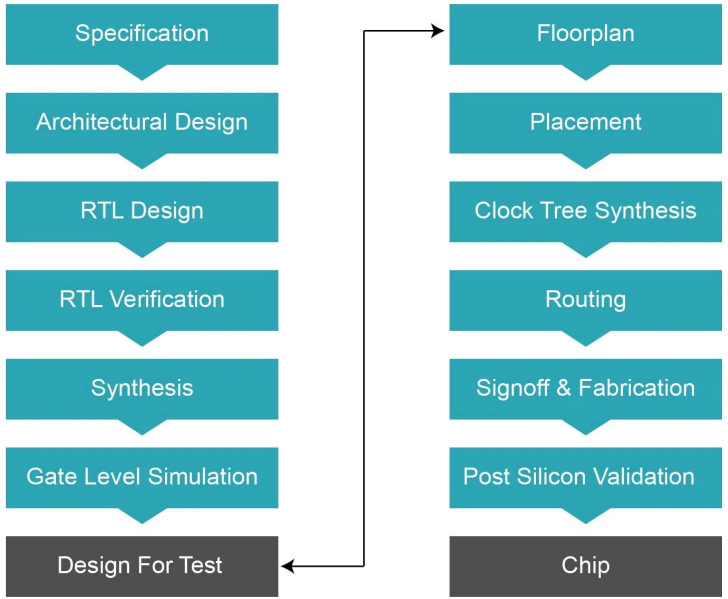
Background

What is the project?

- MIPS-based processor implemented in Verilog
- Used Cadence SimVision, Innovus, and Virtuoso for design/layout, Synopsys Design Compiler and TetraMAX for synthesis/ATPG
- Functional verification via custom testbenches
- Included DFT features for post-silicon validation
- Full layout with AMI 0.5µm standard cell library
- Github: https://github.com/yalongwastaken/mips_cpu/tree/main



Background: MIPS

What is the theoretical background?

- **RISC Philosophy**: MIPS follows the Reduced Instruction Set Computing model—simple, fixed-length instructions enable high clock rates.
- **Load/Store Architecture**: Only LW/SW access memory; all ALU ops work on registers, simplifying datapath design.
- **Five-Stage Pipeline**: Fetch → Decode → Execute → Memory → Write-Back supports one-instruction-per-cycle throughput under ideal conditions.

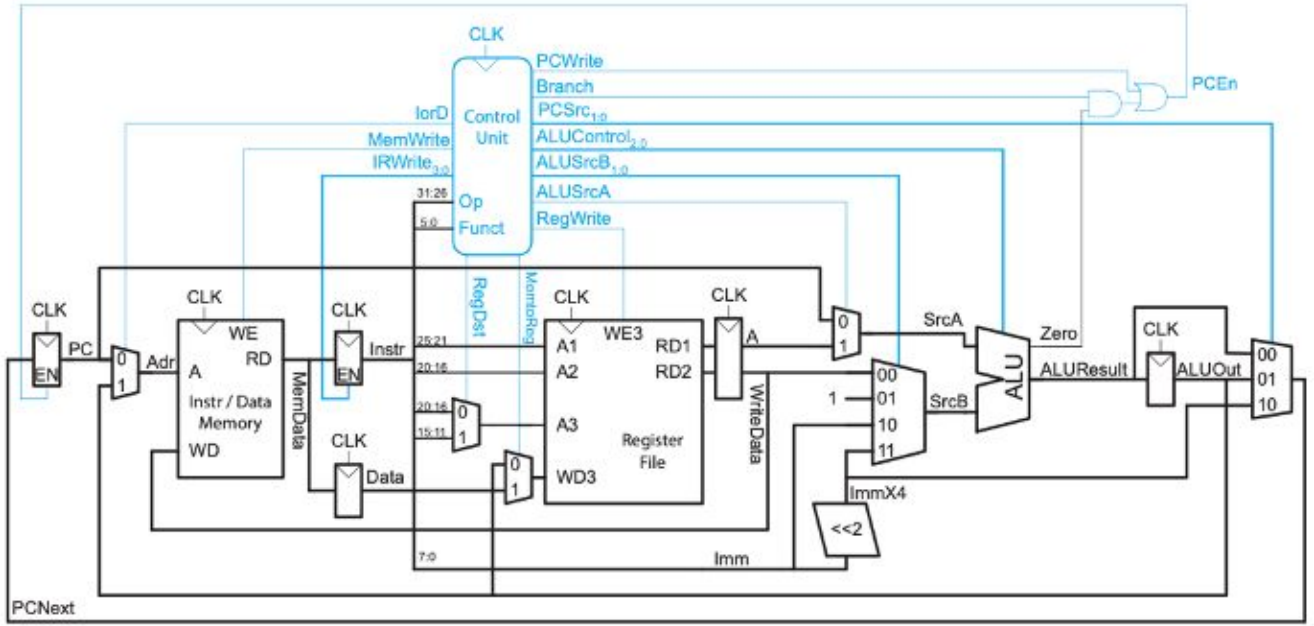
MIPS Instructions	Name	Format
addu	addu	R
subtract	subu	R
add immediate	addiu	I
load word	lw	I
store word	sw	I
load byte	lb	I
store byte	sb	I
load upper immediate	lui	I
branch on equal	beq	I
branch on not equal	bne	I
set less than	slt	R
set less than immediate	slti	I
jump	j	J
jump register	jr	R
jump and link	jal	J

Architecture: High Level

What is the design?

2 Main Modules:

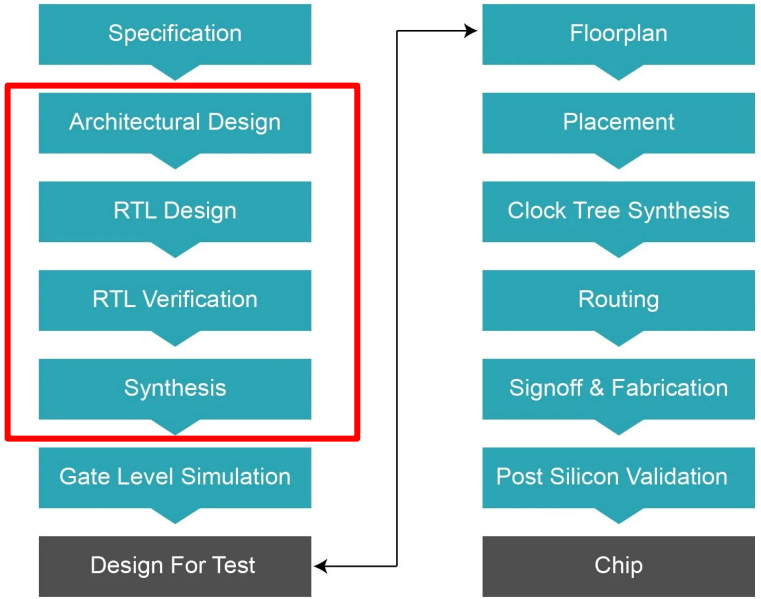
- Control unit
  - Blue
- Datapath
  - Black



Architecture: Low Level

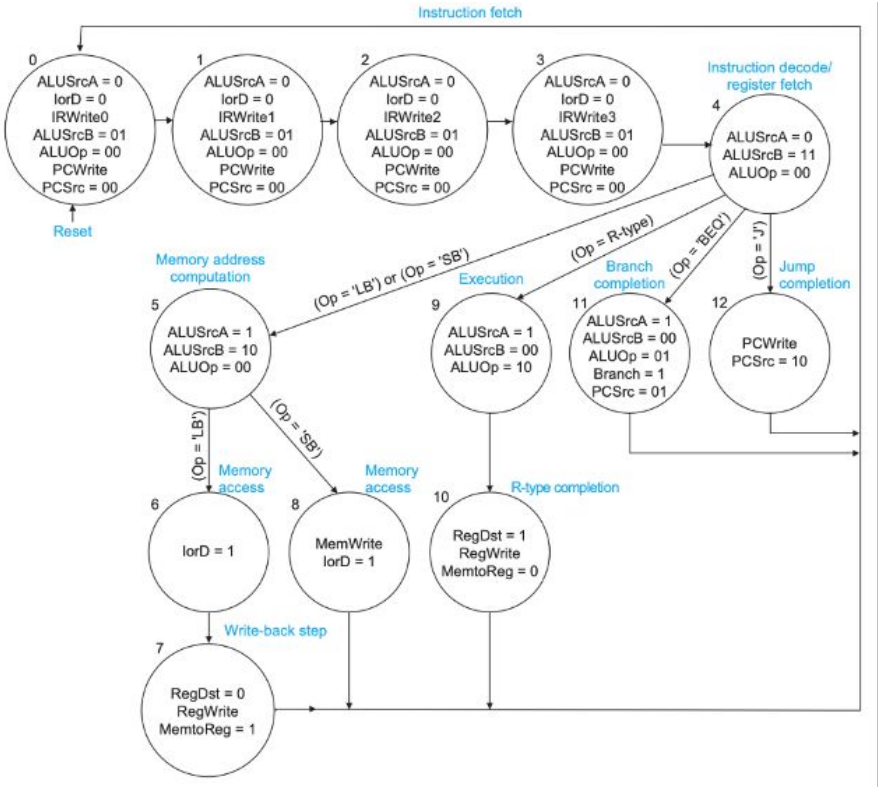
What are the submodules?

- Control Unit:
  - ALU Controller
- Datapath:
  - DFF
  - 2-1 Mux
  - 3-1 Mux
  - 4-1 Mux
  - Instruction/Data Memory
  - Register File
  - ALU
- HDL Implementation:
  - Behavioral modeling

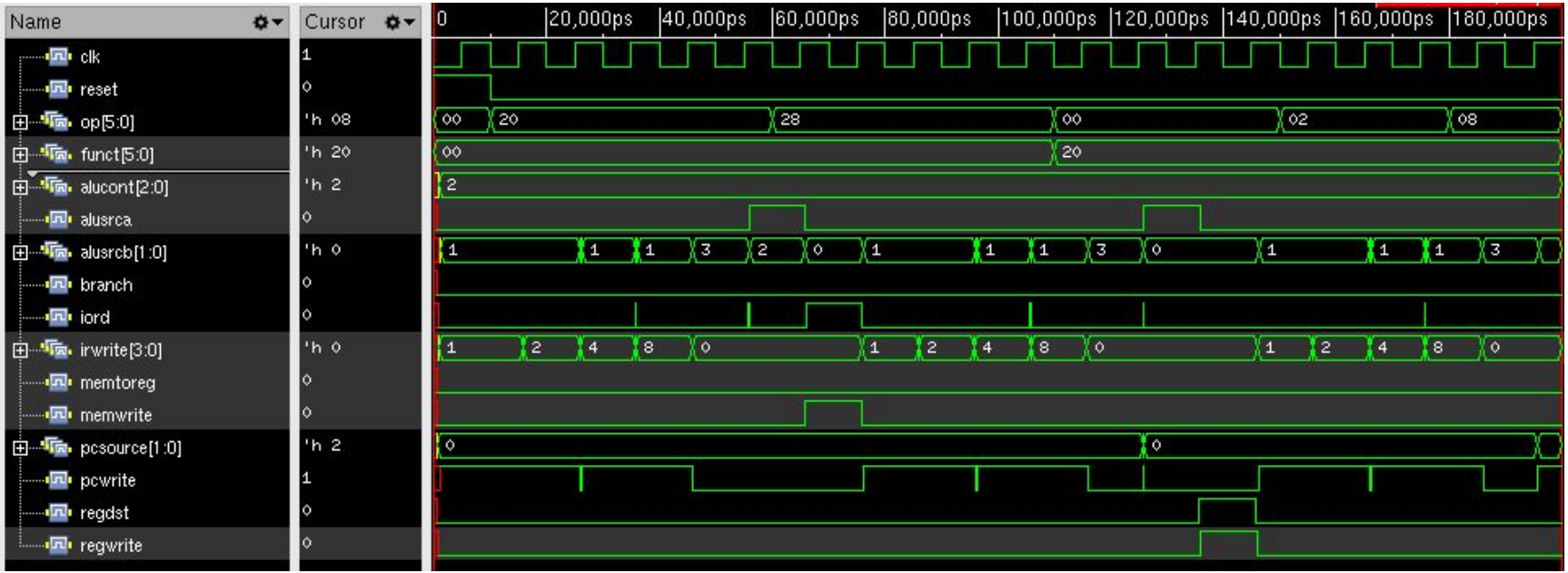


Architecture: Controller FSM

What is the design?

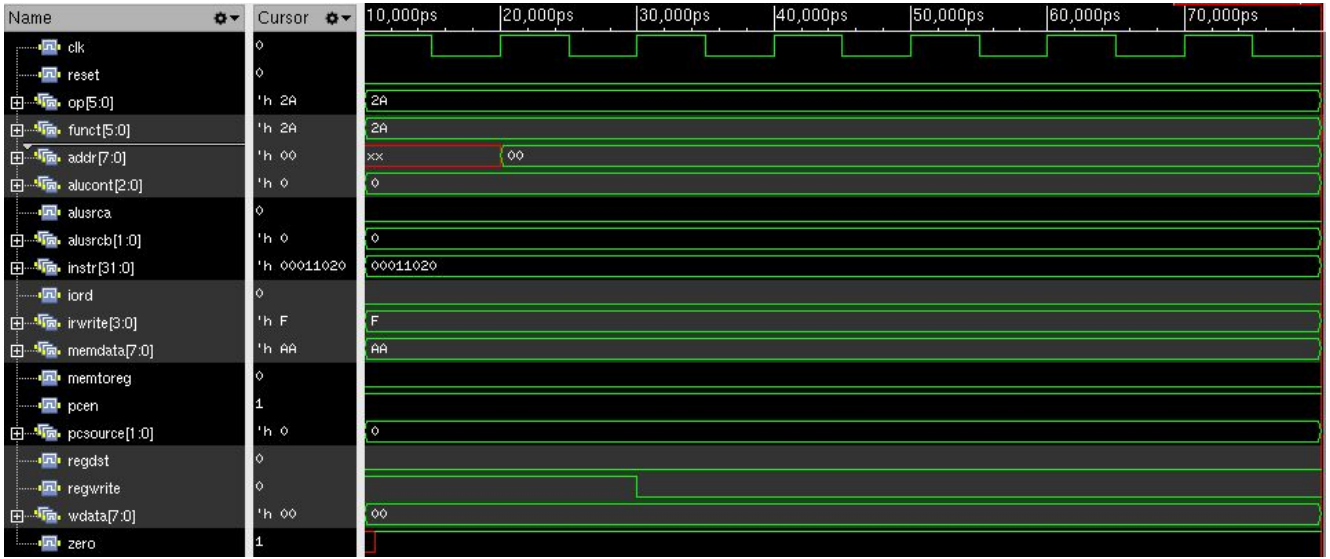


HDL - Controller



HDL - Datapath

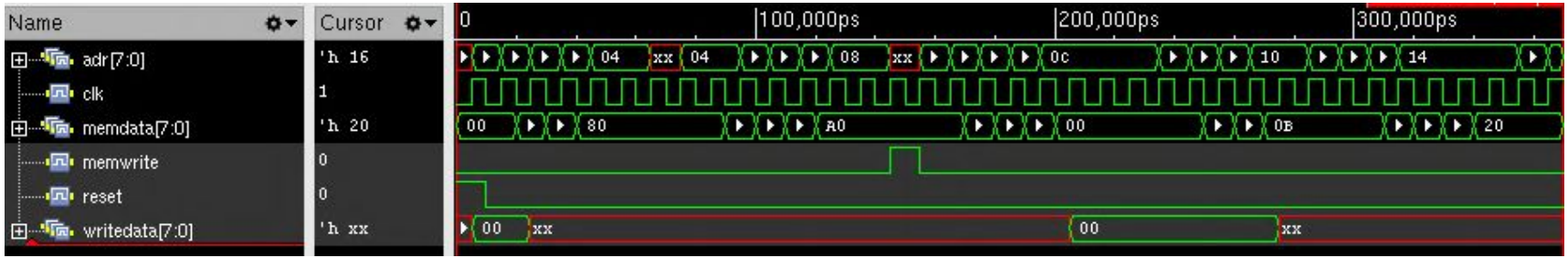
What is the Verilog?




```
xcelium> run
time=                    0 | addr=xx | wdata=xx | zero=x | op=xx | funct=xx
time=                10000 | addr=xx | wdata=00 | zero=1 | op=2a | funct=2a
time=                20000 | addr=00 | wdata=xx | zero=1 | op=2a | funct=2a
Simulation complete via $finish(1) at time 80 NS + 0
../tb/datapath_tb.v:84        $finish;
xcelium>
```

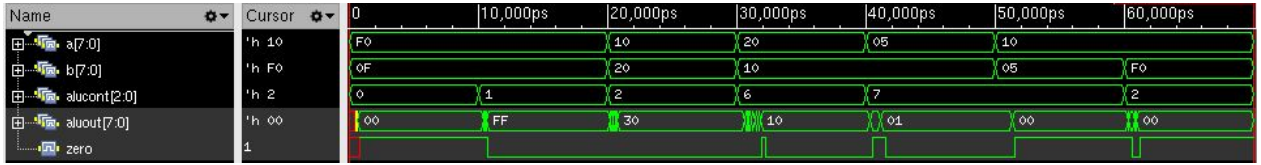
HDL - MIPS


```
xcelium> run
Time:                 0 | memwrite: 0 | adr: xx | writedata: xx | memdata: 00000000
Time:               500 | memwrite: 0 | adr: 00 | writedata: 00 | memdata: 00000000
Time:              1500 | memwrite: 0 | adr: 01 | writedata: 00 | memdata: 00000000
Time:              2000 | memwrite: 0 | adr: 01 | writedata: 00 | memdata: 10111111
Time:              2500 | memwrite: 0 | adr: 02 | writedata: xx | memdata: 10111111
Time:              3000 | memwrite: 0 | adr: 02 | writedata: xx | memdata: 11001100
Time:              3500 | memwrite: 0 | adr: 03 | writedata: xx | memdata: 11001100
Time:              4000 | memwrite: 0 | adr: 03 | writedata: xx | memdata: 10000000
Time:              4500 | memwrite: 0 | adr: 04 | writedata: xx | memdata: 10000000
Time:              6500 | memwrite: 0 | adr: xx | writedata: xx | memdata: 10000000
Time:              7500 | memwrite: 0 | adr: 04 | writedata: xx | memdata: 10000000
Time:              9000 | memwrite: 0 | adr: 04 | writedata: xx | memdata: 00000000
Time:              9500 | memwrite: 0 | adr: 05 | writedata: xx | memdata: 00000000
Time:             10000 | memwrite: 0 | adr: 05 | writedata: xx | memdata: 01100110
Time:             10500 | memwrite: 0 | adr: 06 | writedata: xx | memdata: 01100110
Time:             11000 | memwrite: 0 | adr: 06 | writedata: xx | memdata: 01110111
Time:             11500 | memwrite: 0 | adr: 07 | writedata: xx | memdata: 01110111
Time:             12000 | memwrite: 0 | adr: 07 | writedata: xx | memdata: 10100000
Time:             12500 | memwrite: 0 | adr: 08 | writedata: xx | memdata: 10100000
Time:             14500 | memwrite: 1 | adr: xx | writedata: xx | memdata: 10100000
Time:             15500 | memwrite: 0 | adr: 08 | writedata: xx | memdata: 10100000
Time:             16500 | memwrite: 0 | adr: 09 | writedata: xx | memdata: 10100000
Time:             17000 | memwrite: 0 | adr: 09 | writedata: xx | memdata: 00100000
Time:             17500 | memwrite: 0 | adr: 0a | writedata: xx | memdata: 00100000
Time:             18000 | memwrite: 0 | adr: 0a | writedata: xx | memdata: 00000001
Time:             18500 | memwrite: 0 | adr: 0b | writedata: xx | memdata: 00000001
Time:             19000 | memwrite: 0 | adr: 0b | writedata: xx | memdata: 00000010
Time:             19500 | memwrite: 0 | adr: 0c | writedata: xx | memdata: 00000010
Time:             20000 | memwrite: 0 | adr: 0c | writedata: xx | memdata: 00000000
Time:             20500 | memwrite: 0 | adr: 0c | writedata: 00 | memdata: 00000000
Time:             23500 | memwrite: 0 | adr: 0d | writedata: 00 | memdata: 00000000
Time:             24500 | memwrite: 0 | adr: 0e | writedata: 00 | memdata: 00000000
Time:             25000 | memwrite: 0 | adr: 0e | writedata: 00 | memdata: 01010101
Time:             25500 | memwrite: 0 | adr: 0f | writedata: 00 | memdata: 01010101
Time:             26000 | memwrite: 0 | adr: 0f | writedata: 00 | memdata: 11110000
Time:             26500 | memwrite: 0 | adr: 10 | writedata: 00 | memdata: 11110000
Time:             27000 | memwrite: 0 | adr: 10 | writedata: 00 | memdata: 00001011
Time:             27500 | memwrite: 0 | adr: 10 | writedata: xx | memdata: 00001011
Time:             28500 | memwrite: 0 | adr: 11 | writedata: xx | memdata: 00001011
Time:             29500 | memwrite: 0 | adr: 12 | writedata: xx | memdata: 00001011
Time:             30500 | memwrite: 0 | adr: 13 | writedata: xx | memdata: 00001011
Time:             31000 | memwrite: 0 | adr: 13 | writedata: xx | memdata: 00000000
Time:             31500 | memwrite: 0 | adr: 14 | writedata: xx | memdata: 00000000
Time:             32000 | memwrite: 0 | adr: 14 | writedata: xx | memdata: 10101101
Time:             33000 | memwrite: 0 | adr: 14 | writedata: xx | memdata: 10111110
Time:             34000 | memwrite: 0 | adr: 14 | writedata: xx | memdata: 00100000
Time:             35500 | memwrite: 0 | adr: 15 | writedata: xx | memdata: 00100000
Time:             36500 | memwrite: 0 | adr: 16 | writedata: xx | memdata: 00100000
Simulation complete via $finish(1) at time 370 NS + 0
../tb/mini_mips_test_design_tb.v:106         $finish;
xcelium>
```

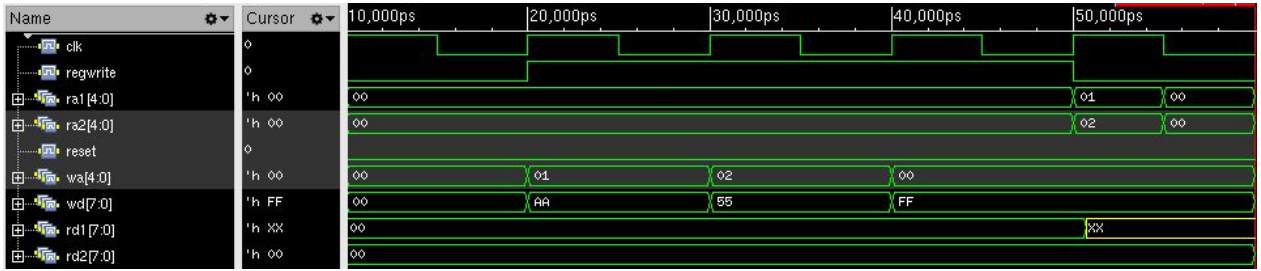


HDL - Other

ALU:



Register File:




```
xcelium> run
rd1 = 00000000 (expected 10101010)
rd2 = 00000000 (expected 01010101)
rd1 = 00000000 (expected 00000000)
rd2 = 00000000 (expected 00000000)
Simulation complete via $finish(1) at time 60 NS + 0
../tb/register_file_tb.v:72         $finish;
xcelium>
```

Synthesis: Timing Report

Worst Case Slack: 1.77ns

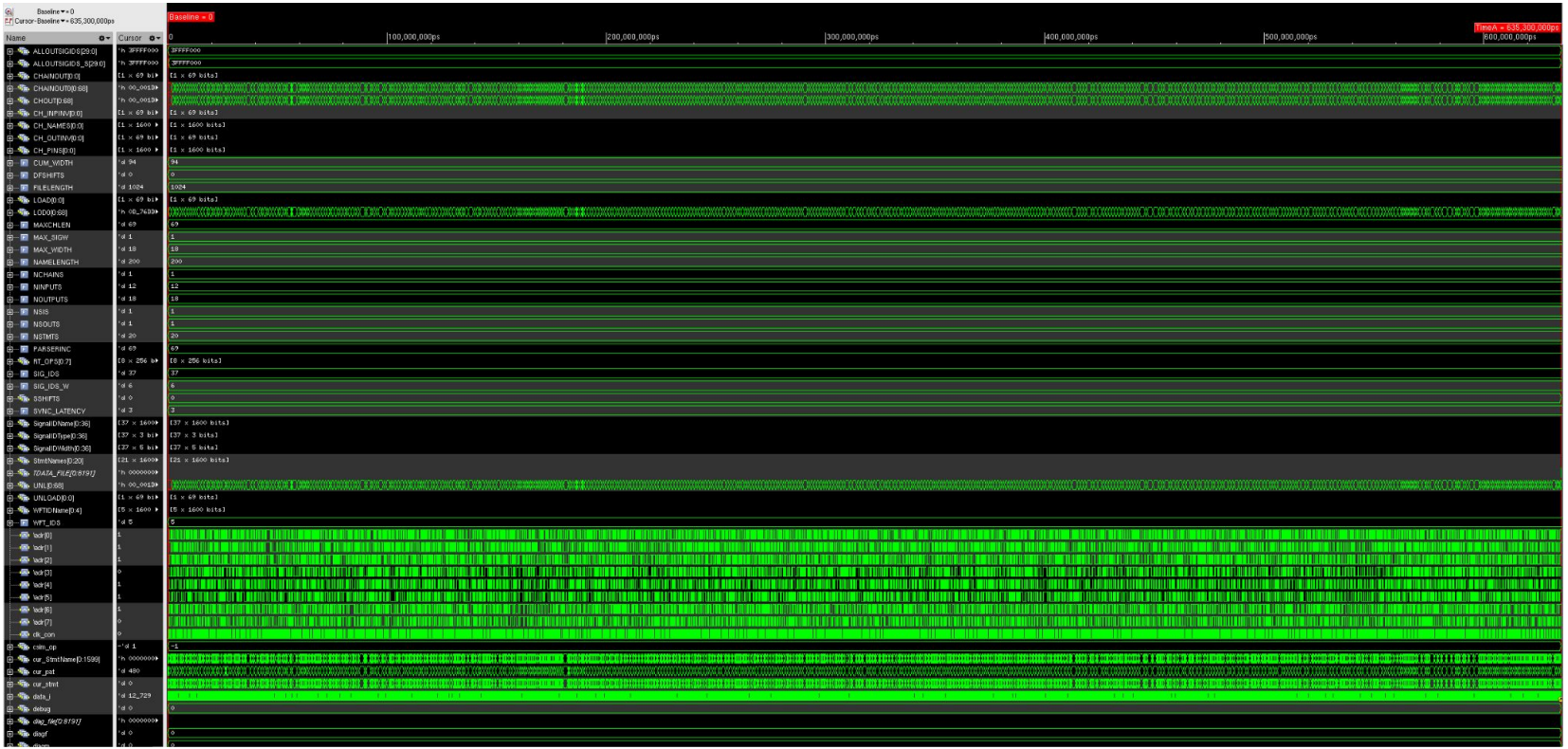
```
Startpoint: cont/state_reg[3]
            (rising edge-triggered flip-flop)
Endpoint: adr[7] (output port clocked by clk)
Path Group: (none)
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------
cont/state_reg[3]/CLK (DFFSR)                           0.000      0.000 r
cont/state_reg[3]/Q (DFFSR)                             0.971      0.971 f
cont/U20/Y (INVX2)                                      0.299      1.270 r
cont/U74/Y (NAND3X1)                                    0.110      1.380 f
cont/U72/Y (NOR2X1)                                     0.224      1.605 r
cont/U70/Y (NOR2X1)                                     0.232      1.836 f
cont/U69/Y (NAND3X1)                                    0.163      1.999 r
cont/U15/Y (INVX2)                                      0.097      2.096 f
cont/U66/Y (NAND2X1)                                    0.219      2.315 r
cont/alusrcb[0] (controller)                            0.000      2.315 r
dp/alusrcb[0] (datapath_test_design)                    0.000      2.315 r
dp/mux4_b/sel[0] (mux4)                                 0.000      2.315 r
dp/mux4_b/U28/Y (NOR2X1)                                0.727      3.042 f
dp/mux4_b/U27/Y (AOI22X1)                               0.219      3.262 r
dp/mux4_b/U25/Y (NAND2X1)                               0.167      3.429 f
dp/mux4_b/y[0] (mux4)                                   0.000      3.429 f
dp/alu/b[0] (alu)                                       0.000      3.429 f
dp/alu/U24/Y (XOR2X1)                                   0.305      3.734 f
dp/alu/add_1_root_add_16_2/B[0] (alu_DW01_add_0)        0.000      3.734 f
dp/alu/add_1_root_add_16_2/U1_0/YC (FAX1)               0.463      4.197 f
dp/alu/add_1_root_add_16_2/U1_1/YC (FAX1)               0.455      4.651 f
dp/alu/add_1_root_add_16_2/U1_2/YC (FAX1)               0.454      5.105 f
dp/alu/add_1_root_add_16_2/U1_3/YC (FAX1)               0.454      5.559 f
dp/alu/add_1_root_add_16_2/U1_4/YC (FAX1)               0.454      6.014 f
dp/alu/add_1_root_add_16_2/U1_5/YC (FAX1)               0.454      6.468 f
dp/alu/add_1_root_add_16_2/U1_6/YC (FAX1)               0.454      6.922 f
dp/alu/add_1_root_add_16_2/U1_7/YS (FAX1)               0.505      7.427 r
dp/alu/add_1_root_add_16_2/SUM[7] (alu_DW01_add_0)      0.000      7.427 r
dp/alu/U47/Y (AOI22X1)                                  0.093      7.519 f
dp/alu/U46/Y (OAI21X1)                                  0.372      7.891 r
dp/alu/aluout[7] (alu)                                  0.000      7.891 r
dp/mux2_pc/b[7] (mux2_2)                                0.000      7.891 r
dp/mux2_pc/U10/Y (AOI22X1)                              0.154      8.046 f
dp/mux2_pc/U1/Y (INVX2)                                 0.184      8.230 r
dp/mux2_pc/y[7] (mux2_2)                                0.000      8.230 r
dp/addr[7] (datapath_test_design)                       0.000      8.230 r
adr[7] (out)                                            0.000      8.230 r
data arrival time                                                  8.230
```

Synthesis: Area Report

Total Area:
363,996 μm^2

Hierarchical cell	Global cell area: Absolute Total	Global cell area: Percent Total	Local cell area: Combi-national	Local cell area: Noncombi-national	Local cell area: Black-boxes	Design
mini_mips_test_design	363996.0000	100.0	3312.0000	0.0000	0.0000	mini_mips_test_design
cont	24381.0000	6.7	16587.0000	6336.0000	0.0000	controller
cont/alucontt	1458.0000	0.4	1458.0000	0.0000	0.0000	alucontrol
dp	336303.0000	92.4	14787.0000	25056.0000	0.0000	datapath_test_design
dp/alu	23625.0000	6.5	14985.0000	0.0000	0.0000	alu
dp/alu/add_1_root_add_16_2	8640.0000	2.4	8640.0000	0.0000	0.0000	alu_DW01_add_0
dp/aluout_ff	9648.0000	2.7	2736.0000	6912.0000	0.0000	flop_0
dp/memdata_flop	9648.0000	2.7	2736.0000	6912.0000	0.0000	flop_3
dp/mux2_a	4176.0000	1.1	4176.0000	0.0000	0.0000	mux2_0
dp/mux2_a3	2664.0000	0.7	2664.0000	0.0000	0.0000	mux2_DATA_WIDTH5
dp/mux2_pc	4176.0000	1.1	4176.0000	0.0000	0.0000	mux2_2
dp/mux2_w3	4176.0000	1.1	4176.0000	0.0000	0.0000	mux2_1
dp/mux3_pc	6840.0000	1.9	6840.0000	0.0000	0.0000	mux3
dp/mux4_b	8640.0000	2.4	8640.0000	0.0000	0.0000	mux4
dp/pc_flop	11736.0000	3.2	4824.0000	6912.0000	0.0000	flop_en
dp/rdata1_flop	9648.0000	2.7	2736.0000	6912.0000	0.0000	flop_2
dp/rdata2_flop	9648.0000	2.7	2736.0000	6912.0000	0.0000	flop_1
dp/regfile	191835.0000	52.7	77787.0000	114048.0000	0.0000	register_file
Total			183996.0000	180000.0000	0.0000	

DFT



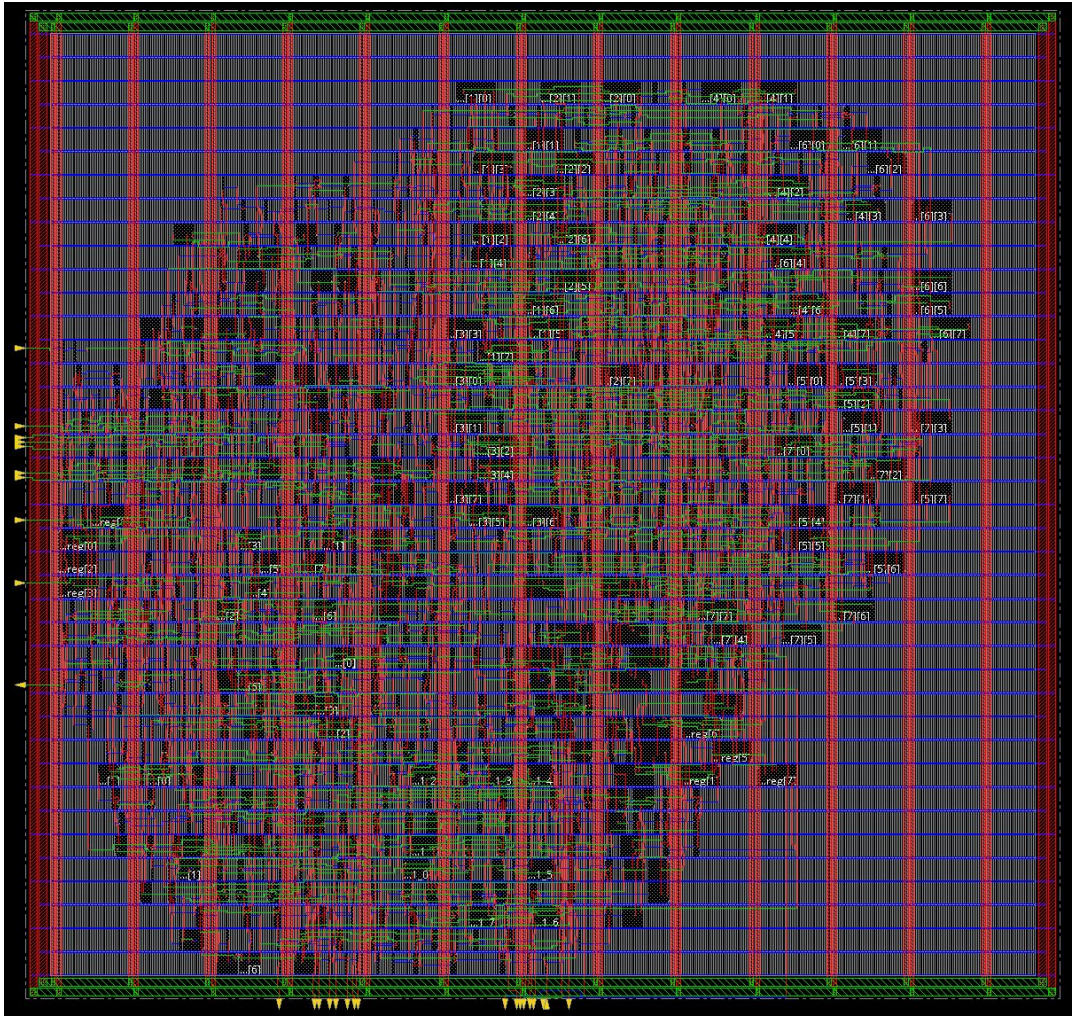
DFT

```
XTB: Starting parallel simulation of 481 patterns
XTB: Using 0 serial shifts
XTB: Begin parallel scan load for pattern 0 (T=200.00 ns, V=3)
XTB: Begin parallel scan load for pattern 5 (T=6100.00 ns, V=62)
XTB: Begin parallel scan load for pattern 10 (T=12100.00 ns, V=122)
XTB: Begin parallel scan load for pattern 15 (T=18900.00 ns, V=190)
XTB: Begin parallel scan load for pattern 20 (T=24600.00 ns, V=247)
XTB: Begin parallel scan load for pattern 25 (T=30700.00 ns, V=308)
XTB: Begin parallel scan load for pattern 30 (T=37800.00 ns, V=379)
XTB: Begin parallel scan load for pattern 35 (T=45000.00 ns, V=451)
XTB: Begin parallel scan load for pattern 40 (T=51200.00 ns, V=513)
XTB: Begin parallel scan load for pattern 45 (T=56600.00 ns, V=567)
XTB: Begin parallel scan load for pattern 50 (T=62800.00 ns, V=629)
XTB: Begin parallel scan load for pattern 55 (T=68500.00 ns, V=686)
XTB: Begin parallel scan load for pattern 60 (T=74400.00 ns, V=745)
XTB: Begin parallel scan load for pattern 65 (T=81100.00 ns, V=812)
XTB: Begin parallel scan load for pattern 70 (T=87300.00 ns, V=874)
XTB: Begin parallel scan load for pattern 75 (T=94700.00 ns, V=948)
XTB: Begin parallel scan load for pattern 80 (T=101700.00 ns, V=1018)
XTB: Begin parallel scan load for pattern 85 (T=108800.00 ns, V=1089)
XTB: Begin parallel scan load for pattern 90 (T=115200.00 ns, V=1153)
XTB: Begin parallel scan load for pattern 95 (T=121400.00 ns, V=1215)
XTB: Begin parallel scan load for pattern 100 (T=128300.00 ns, V=1284)
XTB: Begin parallel scan load for pattern 105 (T=134400.00 ns, V=1345)
XTB: Begin parallel scan load for pattern 110 (T=141800.00 ns, V=1419)
XTB: Begin parallel scan load for pattern 115 (T=148200.00 ns, V=1483)
XTB: Begin parallel scan load for pattern 120 (T=155700.00 ns, V=1558)
XTB: Begin parallel scan load for pattern 125 (T=161400.00 ns, V=1615)
XTB: Begin parallel scan load for pattern 130 (T=165900.00 ns, V=1660)
XTB: Begin parallel scan load for pattern 135 (T=170200.00 ns, V=1703)
XTB: Begin parallel scan load for pattern 140 (T=173900.00 ns, V=1740)
XTB: Begin parallel scan load for pattern 145 (T=177200.00 ns, V=1773)
XTB: Begin parallel scan load for pattern 150 (T=180200.00 ns, V=1803)
XTB: Begin parallel scan load for pattern 155 (T=186100.00 ns, V=1862)
XTB: Begin parallel scan load for pattern 160 (T=189700.00 ns, V=1898)
XTB: Begin parallel scan load for pattern 165 (T=196500.00 ns, V=1966)
XTB: Begin parallel scan load for pattern 170 (T=203000.00 ns, V=2031)
XTB: Begin parallel scan load for pattern 175 (T=209600.00 ns, V=2097)
XTB: Begin parallel scan load for pattern 180 (T=216400.00 ns, V=2165)
XTB: Begin parallel scan load for pattern 185 (T=223400.00 ns, V=2235)
XTB: Begin parallel scan load for pattern 190 (T=230600.00 ns, V=2307)
XTB: Begin parallel scan load for pattern 195 (T=237800.00 ns, V=2379)
XTB: Begin parallel scan load for pattern 200 (T=244400.00 ns, V=2445)
XTB: Begin parallel scan load for pattern 205 (T=251100.00 ns, V=2512)
XTB: Begin parallel scan load for pattern 210 (T=258900.00 ns, V=2590)
XTB: Begin parallel scan load for pattern 215 (T=265100.00 ns, V=2652)
XTB: Begin parallel scan load for pattern 220 (T=272300.00 ns, V=2724)
XTB: Begin parallel scan load for pattern 225 (T=278900.00 ns, V=2790)
XTB: Begin parallel scan load for pattern 230 (T=285500.00 ns, V=2856)
XTB: Begin parallel scan load for pattern 235 (T=292800.00 ns, V=2929)
XTB: Begin parallel scan load for pattern 240 (T=299500.00 ns, V=2996)
XTB: Begin parallel scan load for pattern 245 (T=306100.00 ns, V=3062)
XTB: Begin parallel scan load for pattern 250 (T=314000.00 ns, V=3141)
XTB: Begin parallel scan load for pattern 255 (T=321400.00 ns, V=3215)
XTB: Begin parallel scan load for pattern 260 (T=329000.00 ns, V=3291)
XTB: Begin parallel scan load for pattern 265 (T=336400.00 ns, V=3365)
XTB: Begin parallel scan load for pattern 270 (T=343000.00 ns, V=3431)
XTB: Begin parallel scan load for pattern 275 (T=349600.00 ns, V=3497)
XTB: Begin parallel scan load for pattern 280 (T=355800.00 ns, V=3559)
XTB: Begin parallel scan load for pattern 285 (T=362400.00 ns, V=3625)
XTB: Begin parallel scan load for pattern 290 (T=368900.00 ns, V=3690)
XTB: Begin parallel scan load for pattern 295 (T=375200.00 ns, V=3753)
XTB: Begin parallel scan load for pattern 300 (T=381400.00 ns, V=3815)
XTB: Begin parallel scan load for pattern 305 (T=387900.00 ns, V=3880)
XTB: Begin parallel scan load for pattern 310 (T=394700.00 ns, V=3948)
XTB: Begin parallel scan load for pattern 315 (T=401700.00 ns, V=4018)
XTB: Begin parallel scan load for pattern 320 (T=408900.00 ns, V=4090)
XTB: Begin parallel scan load for pattern 325 (T=417400.00 ns, V=4175)
XTB: Begin parallel scan load for pattern 330 (T=425900.00 ns, V=4260)
XTB: Begin parallel scan load for pattern 335 (T=432900.00 ns, V=4330)
XTB: Begin parallel scan load for pattern 340 (T=440100.00 ns, V=4402)
XTB: Begin parallel scan load for pattern 345 (T=449000.00 ns, V=4491)
XTB: Begin parallel scan load for pattern 350 (T=457700.00 ns, V=4578)
XTB: Begin parallel scan load for pattern 355 (T=466000.00 ns, V=4661)
XTB: Begin parallel scan load for pattern 360 (T=474400.00 ns, V=4745)
XTB: Begin parallel scan load for pattern 365 (T=481400.00 ns, V=4815)
XTB: Begin parallel scan load for pattern 370 (T=489600.00 ns, V=4897)
XTB: Begin parallel scan load for pattern 375 (T=497500.00 ns, V=4976)
XTB: Begin parallel scan load for pattern 380 (T=504700.00 ns, V=5048)
XTB: Begin parallel scan load for pattern 385 (T=512200.00 ns, V=5123)
XTB: Begin parallel scan load for pattern 390 (T=520000.00 ns, V=5201)
XTB: Begin parallel scan load for pattern 395 (T=527900.00 ns, V=5280)
XTB: Begin parallel scan load for pattern 400 (T=536500.00 ns, V=5366)
XTB: Begin parallel scan load for pattern 405 (T=543800.00 ns, V=5439)
XTB: Begin parallel scan load for pattern 410 (T=551800.00 ns, V=5519)
XTB: Begin parallel scan load for pattern 415 (T=559100.00 ns, V=5592)
XTB: Begin parallel scan load for pattern 420 (T=564900.00 ns, V=5650)
XTB: Begin parallel scan load for pattern 425 (T=569100.00 ns, V=5692)
XTB: Begin parallel scan load for pattern 430 (T=575300.00 ns, V=5754)
XTB: Begin parallel scan load for pattern 435 (T=585500.00 ns, V=5856)
XTB: Begin parallel scan load for pattern 440 (T=591700.00 ns, V=5918)
XTB: Begin parallel scan load for pattern 445 (T=599900.00 ns, V=6000)
XTB: Begin parallel scan load for pattern 450 (T=604600.00 ns, V=6047)
XTB: Begin parallel scan load for pattern 455 (T=609400.00 ns, V=6095)
XTB: Begin parallel scan load for pattern 460 (T=614200.00 ns, V=6143)
XTB: Begin parallel scan load for pattern 465 (T=619000.00 ns, V=6191)
XTB: Begin parallel scan load for pattern 470 (T=623800.00 ns, V=6239)
XTB: Begin parallel scan load for pattern 475 (T=628700.00 ns, V=6288)
XTB: Begin parallel scan load for pattern 480 (T=634600.00 ns, V=6347)
XTB: Begin parallel scan load for pattern 480, unload 2 (T=635100.00 ns, V=6352)
XTB: Simulation of 481 patterns completed with 0 mismatches (time: 635300.00 ns, cycles: 6353)
```

481 Patterns & 0 Mismatches

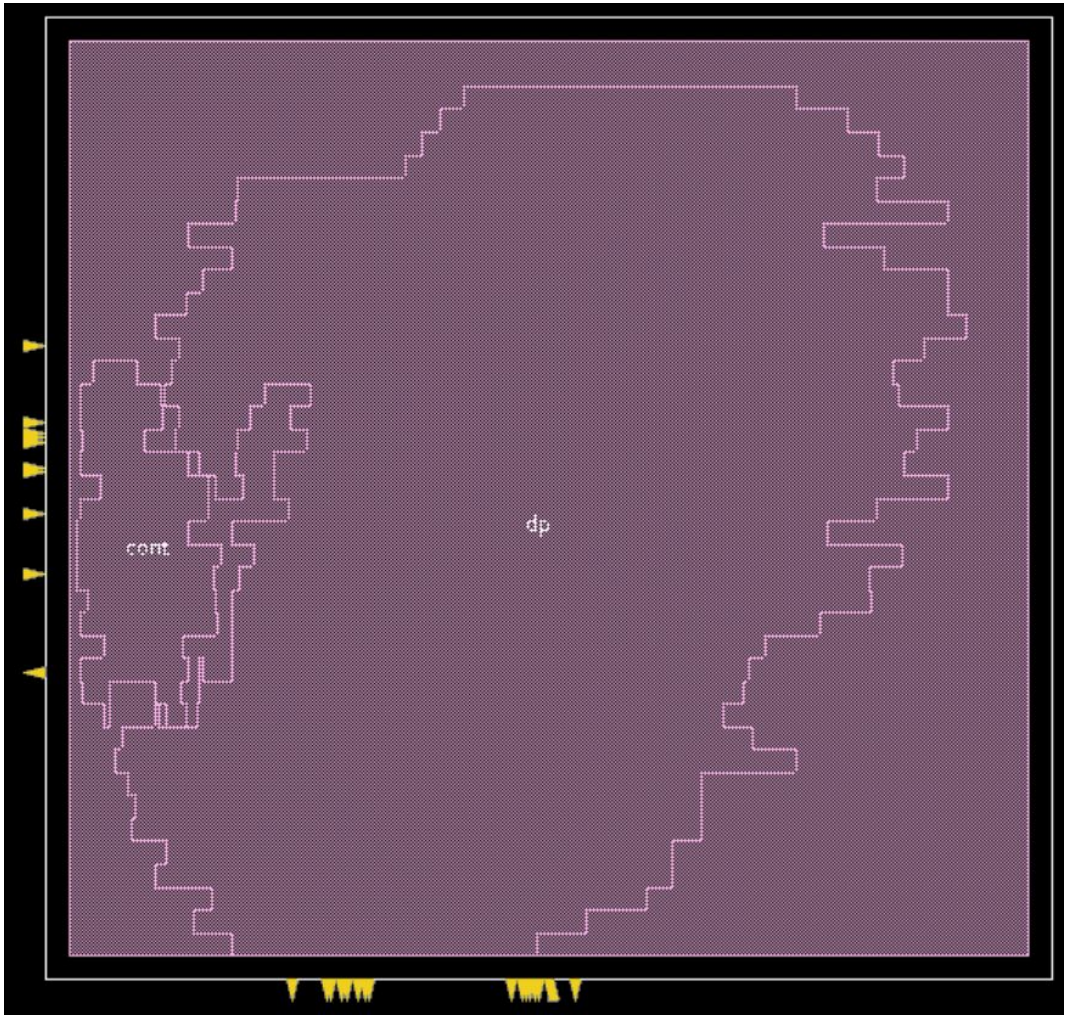
Layout

Mini MIPS



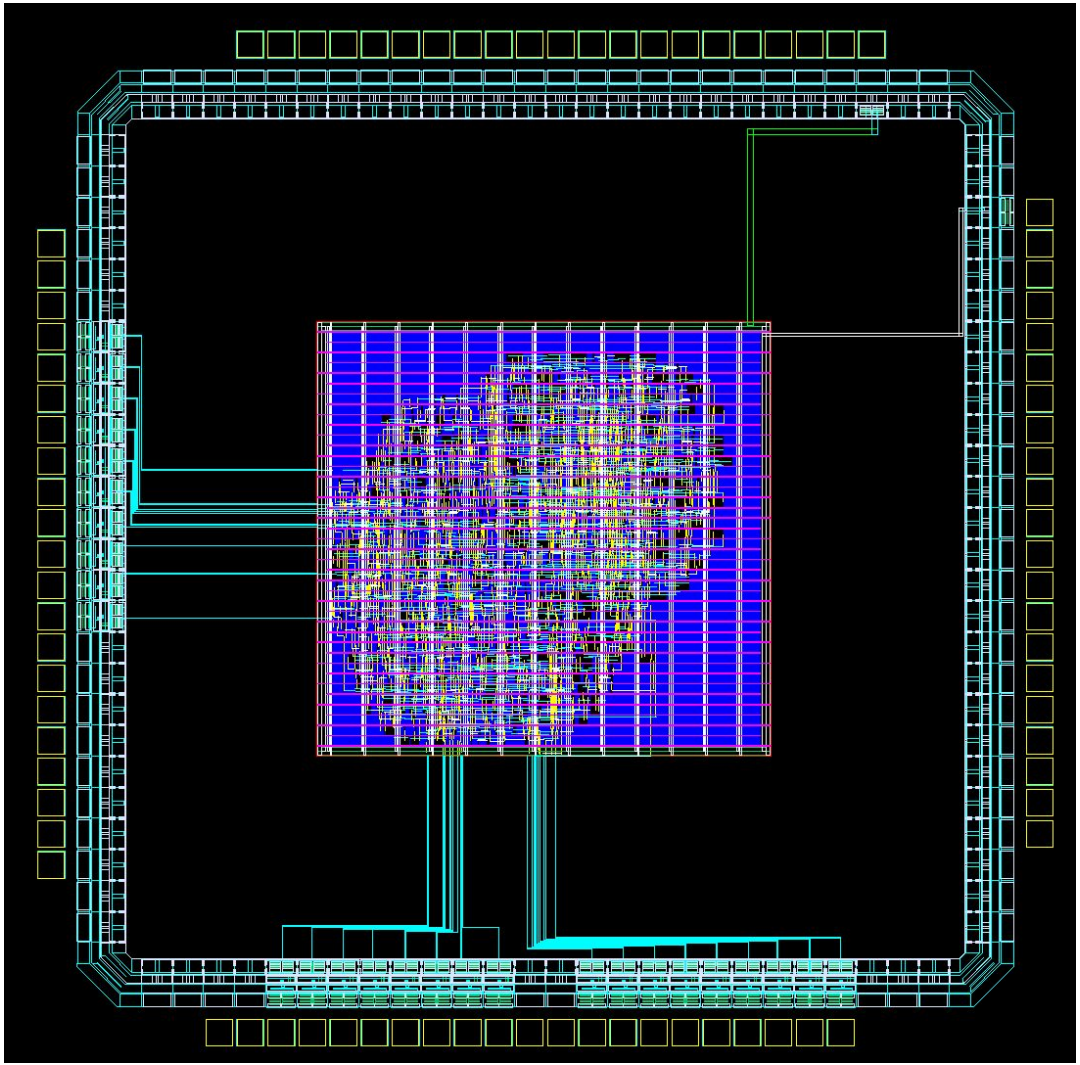
Layout

Mini MIPS



Layout

Mini MIPS & Pad



THANK YOU

https://github.com/yalongwastaken/mips_cpu/tree/main