Yamaha Digital Guitar Amplifiers

DG60FX-112 Circuit explanation

1. Introduction

This document details the circuit operation of the DG60FX-112 Digital Guitar Amplifier. Unlike some "digital" guitar amplifiers in which analog signal circuitry is simply *controlled* by digital circuitry (usually a microprocessor), this model uses Digital Signal Processor (DSP) chips to process the guitar signal. Apart from the final power amplifier and some analog gain and buffer stages around the Analog to Digital and Digital to Analog converters (AD/DA), all signal processing of the guitar signal is performed in the digital domain. Microprocessor control of all functions also allows "patches" to be memorised and recalled using MIDI, footswitch or front-panel selection.

The circuitry of this model is similar to that used in other models within the DG range. It is suggested that you use this text in conjunction with the Service Manual for this model.

2. Block Diagram

The circuitry can be divided down into several sections, each performing a specific task –

- Analog input/output circuitry and AD/DA converters
- Main operating system, consisting of a CPU, ROM and SRAM
- Front panel circuitry, consisting of switches, LEDs and potentiometers
- Digital Signal Processing circuitry
- Power supply and power amplifier

3. Analog and AD/DA circuitry

a) Input Preamp

The Input Preamp circuitry is located on a small front-panel mounted PCB (Main 3/8). The guitar signal enters the amplifier via one of two ¼" jacks. One has a high sensitivity and the other a low sensitivity. Both jacks can be used simultaneously allowing two instruments to share the amplifier. The initial preamp stage consists of a dual FET input op-amp IC401, which is an NJM072 device that has low noise and high input impedance characteristics. Each half of IC401 buffers its respective input with a 1-Megohm impedance as set by resistors R402 and R407, and a gain of +16.5dB for the High input and +6dB for the Low input. Back-to-back diodes across the opamp inputs protect against excessively high input levels.

The frequency response of this first preamp stage extends down to below 10 Hz – well below the fundamental frequency of a guitar's low E string. In other guitar amplifiers, a significant bass rolloff is usually applied around this stage to prevent overloading of subsequent stages, and as

part of the amplifier's intended tonal characteristics. In the DG60FX-112 however, all equalisation is done in the digital domain by the DSP chips.

The outputs of the High and Low preamps are applied to one half of IC402, another NJM072 opamp. This stage has a gain of very close to unity and mixes the two input signals. Its output is fed to the A/D buffer stages and to the other half of IC402, which drives the front panel "PEAK" LED. The LED turns on when the signal level from either half of IC401 is about 17 volts p-p or 3dB below their clipping level.

b) Pre-A/D conditioning

The remainder of the signal path circuitry, both analog and digital, up to and including the D/A, is situated on the DM PCB. In the DG60FX-112, a single device IC104 (AK4520A) combines the functions of stereo (2-ch) A/D and D/A conversion. However, in this application, IC104's two-channel input capability is used to increase the conversion resolution of the mono guitar signal.

Prior to being applied to IC104, the preamp signal undergoes gain adjustment, phase splitting and level shifting by NJM5532 opamps IC102/IC103. IC102 generates a balanced or differential version of the guitar signal, which is fed to the R-ch differential inputs of IC104; the L-ch inputs of IC104 are similarly fed from IC103. Zener diodes ZD101/ ZD102 and diodes D103/D104 limit the output voltage swing of IC102 to prevent overloading of IC104. A +2.5V DC reference derived from resistors R124-R126 sets the quiescent output levels of IC102/IC103 to the midpoint of the A/D input voltage range.

Although IC102 and IC103 are fed with the same signal, their gains are different, so that the signal levels into the left and right channel inputs of IC104 differ by 18dB (or three bits in the digital domain). Through the use of digital signal level detection and crossfading algorithms in the DSP chips, the ADC's original 20-bit resolution is increased to 23-bits. At low signal levels, the A/D's R-ch is selected for processing in preference to the L-ch because the former has the higher signal amplitude. As the input signal's level increases, the R-ch will eventually overload. Before this occurs, the DSP crossfades to the ADC's L-ch.

c) Analog outputs

After processing by the DSP ICs, the (now) two-channel digital audio signal is fed into the SDTI input (pin 13) of IC104. Its L-ch (pin 26) and R-ch (pin 27) analog outputs are fed to the OUTPUT volume control VR314, and from there to the remainder of the output circuitry situated on the Main 2/8 PCB, which is mounted on the rear panel.

One half of dual opamp IC501 (NJM4556AD) amplifies the L-ch signal from VR314's wiper by about 21dB and drives the HEADPHONE and LINE OUT L/MONO jacks; the other half of IC501 does the same for the right channel. The L-ch signal from the volume control is also fed to IC502 (NJM5532P). One half of this IC amplifies the signal by +4.2dB and feeds the second half via a switching contact on the POWER AMP IN jack. When an external signal is applied to this jack, the DG60FX-112's power amplifier stage is disconnected from its normal preamp signal.

d) AD/DA clock generator

In order for any digital audio system to work, the processing stages within it must be supplied with the necessary clocks. In the DG60FX-112, these are generated by CMOS ICs, IC107-IC110. A 24.576 MHz crystal connected around one section of inverter IC107 generates the master clock. This is buffered and fed to a TC74HC4040F binary counter IC108, which derives frequencies of 12.288MHz, 6.144MHz, 3.072MHz and 48Khz from its QA, QB, QC and QI outputs respectively. If we call the 48KHz clock “Fs” (the system’s sampling frequency), then the other frequencies can be regarded as “256Fs”, “128Fs” and “64Fs”.
The 74HC164 shift-register IC109 derives delayed versions of the Fs clock fed into it to suit the specific timing requirements of IC104 and the DSP ICs. The 74HC175 quad D-type flip-flop IC110 simply ensures that the edges of all of the generated clocks are coincident in time, before being fed to the system. Table 1 summarises the AD/DA system clocks.

CLOCK	FREQUENCY	DESTINATION
256Fs	12.288MHz	IC104 AD/DA - MCLK Pin 15
128Fs	6.144MHz	IC17 DIT2 - MCLK Pin 2
"	"	IC8 DSP6 - MCKS Pin 13
"	"	IC9 DSP6 - MCKS Pin 13
64Fs	3.072MHz	IC104 AD/DA - SCLK Pin 12
Fs	48KHz	IC104 AD/DA - LRCK Pin 11
SYNC	48KHz	IC8 DSP6 - SSYNC Pin 14
"	"	IC8 DSP6 - SYNCI Pin 6
"	"	IC9 DSP6 - SSYNC Pin 14
"	"	IC9 DSP6 - SYNCI Pin 6
"	"	IC17 DIT2 - WCIN Pin 6

Table1. Digital Audio System clocks

Note that the clock generation system just described has nothing to do with either the main CPU operating clock or the master clock for the DSP ICs. These will be discussed later.

4. Main operating system

A single Hitachi H8/3002 series microprocessor IC12 (CPU) controls the entire unit. This is a 100-pin QFP device that includes internal RAM, Serial Interface, A/D converter, Timers and other circuits. Additional peripheral chips that make up the rest of the operating system are the 8-Mbit Program ROM IC1, two 256-Kbit SRAMs IC2 and IC3, Reset/Backup Controller IC4 and some logic gates that provide chip enabling.

Many of the CPU’s pins allow it to interface with external chips that for example, read switches or controls, or drive LED, etc. These pins act as so called “ports” that don’t directly affect the CPU’s ability to execute a program stored in the ROM. The signals or logic levels present at several specific pins of the CPU however, are crucial to the correct running of the operating system. These include –

XTAL (pin 69) and **EXTAL** (pin 68) – A 12.00MHz crystal is connected across these pins, and together form the CPU's master clock oscillator.

/RES (pin 65) – Initial Clear input to CPU. The Reset Controller IC4 generates this "hardware reset" signal. On power-up, this line will stay low for about 100 milliseconds, after which it will switch high, allowing the CPU to operate.

MD0 (pin 75), **MD1** (pin 76) and **MD2** (pin 77) – Configures the CPU to have access to a 16-Mbyte address space and to use its internal 512 bytes of RAM (MD0="0", MD1="0", MD2="1"). These pins are tied to either 0V or +5V supply lines.

/CS0 (pin 93) – Chip select for Program ROM IC1. This pin always has negative-going pulses on it because IC1 is the sole source of instructions that the CPU fetches and executes. There is no internal CPU ROM.

/CS1 (pin 92) – Chip select for SRAMs IC2 and IC3. This pin always has negative-going pulses on it because of the CPU's constant need to access the SRAMs, either to write data to or read data from them.

/CS2 (pin 91) and **/CS3** (pin 90) – Chip-Select lines for DSP IC8 and DSP IC9 respectively. These pins are normally high but will pulse low whenever the DSP ICs are called upon to change memories or adjust parameter values. The pins pulse either individually or appear to pulse together, depending on which parameter is being adjusted. Strictly speaking, they cannot pulse simultaneously because they are decoded from different areas of the CPU's address space

/RD (pin 72) – Read signal for accessing data from peripheral ICs. Like the **/CS0** signal, this pin constantly pulses because of the CPU's need to fetch instructions from the ROM or read data from the SRAMs and when required, from the DSPs.

/HWR (pin 73) and **/LWR** (pin 74) – Write-enable signal for SRAMs and DSP ICs. These pins constantly pulse because of the CPU's need to write data to the SRAMs and when required, to the DSPs. The CPU has a 16-bit external data buss and *reads* the SRAMs simultaneously, but it can *write* to each device individually. To write data to the DSPs, both /LWR and /HWR *and* the relevant chip select line (/CS2 or /CS3) for that DSP must all be low simultaneously.

To allow selection by the CPU, an operating system device requires at least two of the aforementioned signals to be active simultaneously. For example, to read the ROM, both **/CS0** *and /***RD** must be low simultaneously. Only under these conditions, will the output pin 3 of OR gate IC5 go low to enable the ROM. The other gates of IC5, IC6 and IC7 function similarly for the SRAMs and DSPs.

The CPU's data lines (D0-D15) and address lines (A0-A19) should all show activity when the system is running correctly.

5. Front Panel Circuitry

a) Switches and LEDs

The switch/LED circuitry is driven by the system CPU and is shown in block form in Figure 1. A total of twenty-one switches (seventeen on the front panel and four on the optional footswitch) are arranged in a 4 x 6 matrix. The CPU generates cyclic negative-going pulses on its Port lines PB0-PB7. These are buffered by a 74HC244 octal buffer IC14, and latched into seven 74HC374 octal D-type Flip-Flops IC301 – IC307. One of these, IC301 drives the switch matrix columns. When a switch is pressed, the negative column pulses appear on the relevant row line, are buffered by IC15, a 74HC244 octal buffer and are then fed to CPU Input Port lines P75 – P77 and P80.

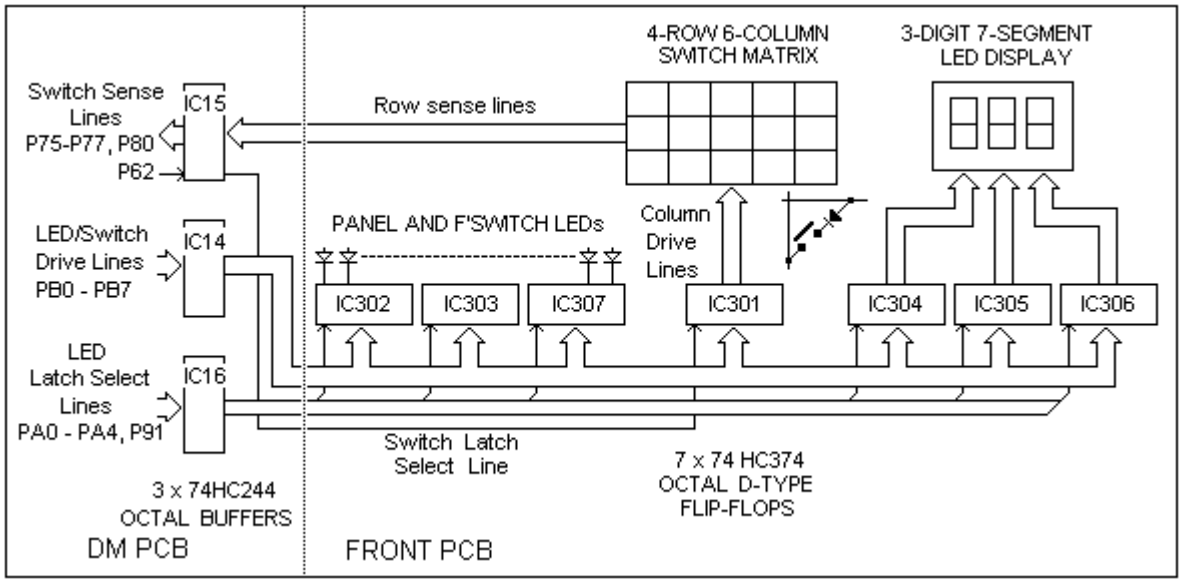

Figure 1. Switch/LED section block diagram

There is a total of forty-seven LEDs that are under the control of the CPU – seventeen on the front panel, six in the optional footswitch and twenty-four contained within the 3-digit, 7-segment display. In this system, each LED is latched either ON or OFF, rather than multiplexed, where an LED is rapidly and continually switched on and off in turn. Each LED has its anode connected to +5 volts and its cathode connected via a current-limiting resistor to one of the outputs of IC302 – IC307. The PB0 – PB7 lines are latched to the outputs of these ICs to drive the LEDs.

The LED Latch Select Lines PA0 – PA4 and P91, generated by the CPU and buffered by IC16, provide the means by which the current state of the PB0 – PB7 lines (ie, the required LED pattern) is latched into the correct octal latch IC. A spare buffer in IC15 is used for the Switch Latch Select Line (CPU P62). In comparison to those of the PB0 – PB7 lines, the pulse width of the LED/Switch Select Lines is extremely short and use of a logic probe (in pulse-catcher mode) is preferable to an oscilloscope when checking signals.

b) Potentiometers

Fourteen rotary potentiometers are mounted on the Front panel PCB to allow the guitarist control over familiar parameters such as BASS, MIDDLE, TREBLE, etc. Of these, only the OUTPUT potentiometer directly controls the level of audio signal through it; the others simply provide variable DC voltages, which the CPU uses to control the relevant parameter. In addition to the potentiometers, an 8-position AMP SELECT rotary switch is provided, which functions as a "stepped" potentiometer, selecting eight discreet DC voltages between 0V and +5V as the switch is rotated. Figure 2 shows the potentiometer circuitry in block form.

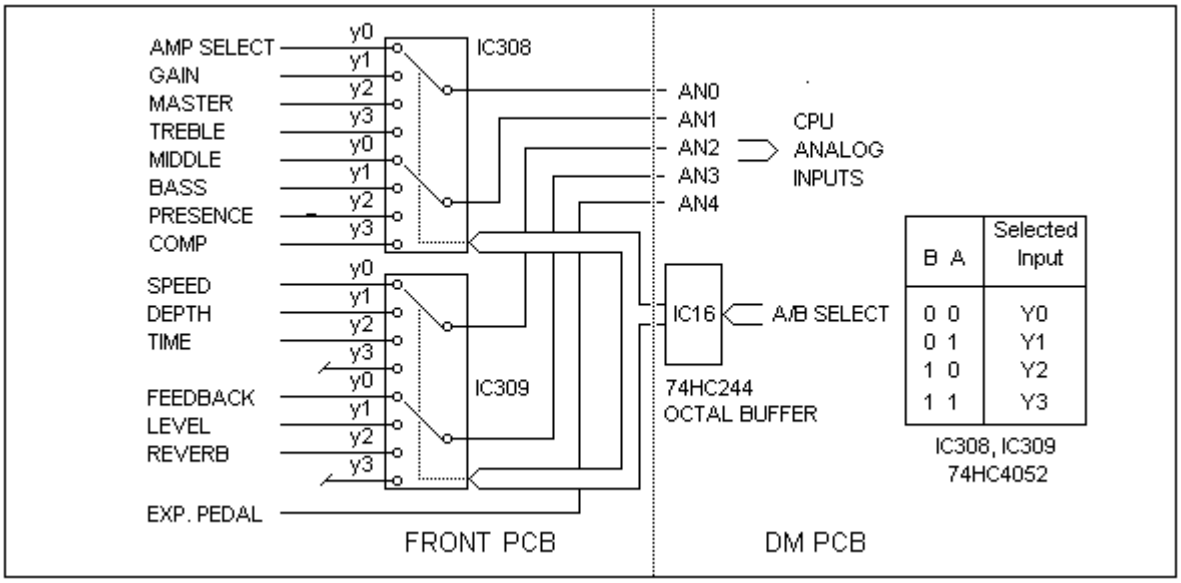

Figure 2. Potentiometer section block diagram

The outer terminals of each potentiometer are connected across the +5V supply, and each wiper terminal is connected to one of the inputs of a 74HC4052 Dual 4-input Analog Multiplexer (IC308 and IC309). The CPU provides a repeating (00,01,10,11,00,01…) binary combination to the multiplexers' A and B select lines, which allows it to read the wiper voltages of four potentiometers at the same time and feed these to four of its analog inputs. The optional external foot controller is directly connected to another of the CPU's analog inputs.

6. Digital Signal Processing

a) DSP6 ICs

All digital signal processing in the DG60FX-112 is performed by two YSS910 (DSP6) integrated circuits IC8 and IC9. A block diagram of the DSP6 chip's internal circuitry and pin functions is shown in Figure 3 and Table 2 respectively. A block diagram of the DSP section signal path is shown Figure 4.

The DSP6 can accept and output multi-channel, digital audio signals in serial or parallel form and perform 32-bit processing of these signals. In the DG60FX-112, serial format signals are

passed between the AD/DA converter IC104 and the two DSP6 chips; the parallel interface pins are not used. However, the microprogram, coefficient and control data required by the DSP6 to process digital audio signals are input as parallel data via its CPU interface. This allows a much faster realtime re-configuration or setup of the device when changing parameters or patches compared to most of Yamaha's earlier DSP chips, which used a serial control interface.

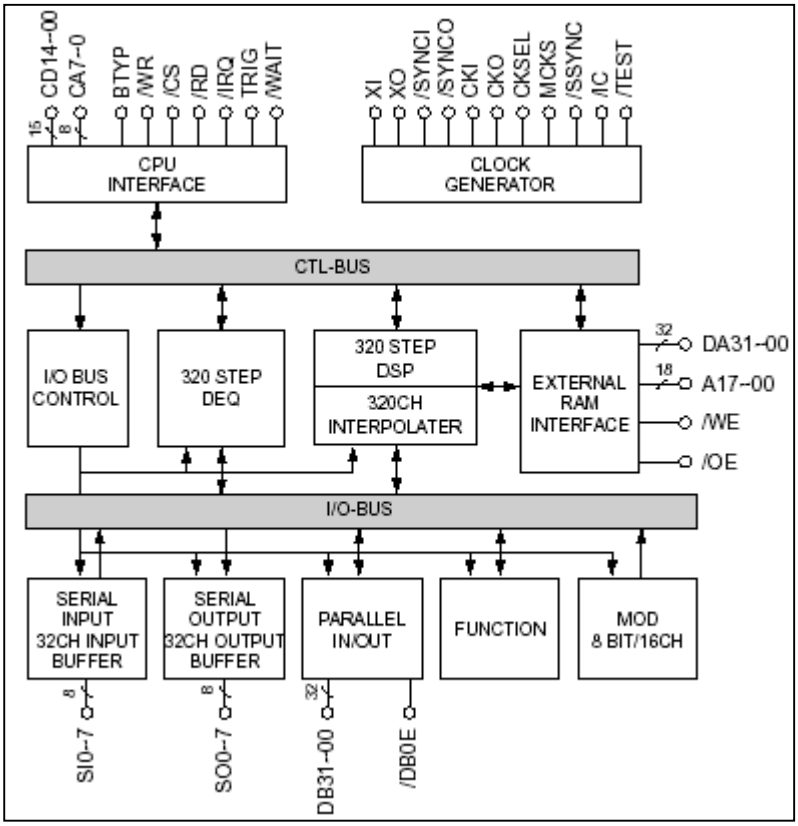

Figure 3. YSS910 (DSP6) IC internal circuitry block diagram

Name	I/O	Function	Typical condition
XI	I	System master clock input	30MHz clock
XO	O	System master clock output	Not used, open pin
/SYNCI	I	System synchronous clock input	48KHz SYNC clock
CKI	I	System clock input	Not used, connected to ground
/SYNCO	O	System synchronous clock output	Not used, open pin
CKO	O	System clock output	Not used, open pin
CKSEL	I	System master clock select (60/30MHz)	+5V (30MHz mode selected)
MCKS	I	Serial I/O master clock input	6.144MHz (128Fs) clock
/SSYNC	I	Serial I/O synchronous clock input	48KHz SYNC clock
/IC	Is	Initial Clear	Low (0V) level briefly on power-up, then switches to and remains high (+5V)
/TEST	I+	Test mode	+5V (Normal mode)
CD00-15	I/O	Host CPU data buss	Normal CPU data buss activity
CA0-7	I	Host CPU address buss	Normal CPU address buss activity
BTYP	I	Host CPU data buss width select	+5V (16-bit mode selected)
/CS	Is+	Chip Select	Normally +5V but pulses low when that specific device (IC8 or IC9)is selected during

			patch or parameter changes
/RD	Is+	Read signal	Constantly pulsing
/WR	Is+	Write signal	Normally +5V but pulses low when changing patches or parameters
/IRQ	O	Interrupt Request	Not used, open pin
TRIG	I/O	Transfer trigger signal input/output	
/WAIT	O	WAIT output	Not used, open pin
SI0-7	I+	Serial digital audio data inputs	SI0/SI1 only, pulses when signal present. Remaining input pins unused, left open
SO0-7	O	Serial digital audio data outputs	SO0/SO1/SO2 only, pulses when signal present. Remaining output pins unused, left open
DB00-31	I+/O	Parallel digital audio data in/out	Not used, open pins
TIMO/DBOE	I/O	Timing output/Parallel buss control input	Not used, connected to +5V via 10K resistor
DA00-31	I+/O	External memory data buss	Not used on IC9. On IC8/DRAMs, pulses when signal present
A17/CE	O	Address/Chip Enable	Not used, open pin
A16/CAS	O	Address/Column Address Strobe	Not used on IC9. Pulses on IC8
A15/RAS	O	Address/Row Address Strobe	Not used on IC9. Pulses on IC8
A10-14	O	External memory address buss	Not used, open pins
A00-09	O	External memory address buss	Not used on IC9, Pulses on IC8
/WE	O	External memory Write Enable	Not used on IC9. Pulses on IC8
/OE	O	External memory Output Enable	Not used on IC9. Pulses on IC8
N.C.	-	No connection	
VDD5	-	+5V supply	
VDD	-	+3.3V supply	
VSS	-	Ground	

Table 2. YSS910 (DSP6) IC pin functions

The function of and signal flow through each IC in the DSP section is as follows –

A/D (IC104) -> Compressor (IC8) -> 4fs Oversampling (IC8) -> Amplifier sound character processing eg distortion, overdrive, etc (IC9) -> Downsampling (IC8) -> EQ (IC8) -> Speaker Simulation (IC8) -> Effects (IC8) -> D/A (IC104) and DIT2 (IC17)

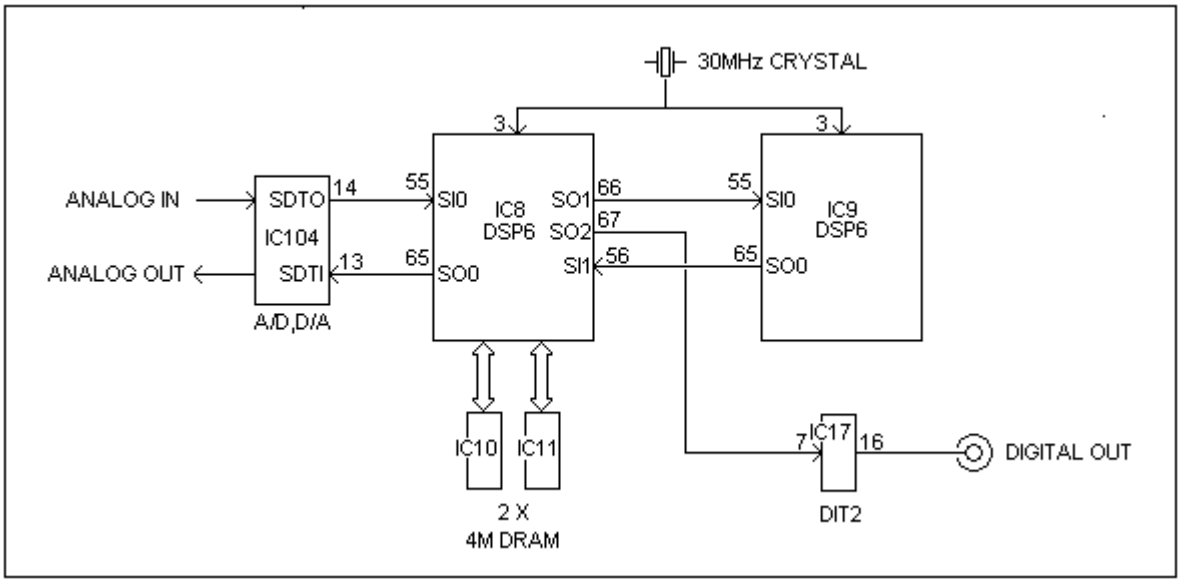

Figure 3. DSP section block diagram

Memory space necessary for effects (reverb, delay, phasing, etc) is provided by the two 4Mbit DRAMs IC10 and IC11. Each DRAM handles sixteen bits, so two are needed for IC8's 32-bit data buss. IC11 handles the low-order bits DA00 - DA15 and IC10 handles the high-order bits DA16 – DA31.

A single, 30MHz crystal oscillator provides the master clock for the internal operation of both DSP6 chips. The actual clocking of digital audio signals into and out of each device is dependent on sync and bit clocks, which have already been described. A failure of the master 30MHz clock will stop all signal activity through the DSP section even if sync and bit clocks are still present. Since all signal flow is in serial form (with the exception of parallel data between IC8 and the DRAMs), the presence of signals at the device pins can easily be monitored with an oscilloscope synchronised to either the "SYNC" or "Fs" 48-KHz system word-clocks.

Noise or other extraneous sound will most likely be caused by a faulty DRAM. Since the IC10 DRAM handles the high-order bits, its failure will have a much greater effect on the sound than will IC11.

b) Digital Interface Transmitter

In addition to the final analog output that is fed to the power amplifier, the DG60FX-112 also provides a co-axial digital output from a rear-panel mounted RCA jack. The digital audio output from SO2 pin 67 of DSP6 IC8 is fed to the DIN input pin 7 of a YM3437F Digital Interface Transmitter (DIT2) IC17. This chip converts the Yamaha digital audio format at its input to the Sony Philips Digital Interface Format (SPDIF) at its DOUT pin 16. The signal is then buffered by a parallel connection of three sections of a 74HCU04 hex inverter IC107. This provides adequate current drive to the output transformer, which in turn feeds the co-axial output jack.

To do its job, IC17 needs to be provided with a bit-clock and word-clock. These are present at pins 2 and 6 respectively. Additionally, its CLD, CIN and CCK lines (pins 13, 12 and 11 respectively) allow the CPU to include channel status information such as sampling frequency, emphasis, etc. in the SPDIF bitstream. CLD is normally high and both CIN and CCK are normally low. Pulse activity on these lines can be briefly observed during the initial CPU bootup period immediately after the amplifier is switched on.

7. Power Supply and Power Amplifier

Except where noted, all of the power supply and power amplifier components apart from the mains 240V input cable and power transformer are mounted on the Main 1/8 PCB.

The power supply is a conventional mains transformer, rectifier and capacitor type. Mains voltage is switched through to the transformer's primary winding by the amplifier's POWER switch and fused by FZ601.There are two secondary windings. The main center-tapped winding, fuses FZ602/FZ603, bridge rectifier DB601 and filter capacitors C606/C607 produce about +/-45V DC for the power amplifier. Dropping resistors R611 to R614 and zener diodes ZD603/ZD604 produce +/-15V DC for the pre-amplifier circuitry. Regulator IC11 (DM PCB) produces a +5V supply for the AD/DA converter IC104.

The remaining secondary winding, fuse FZ604, bridge rectifier DB602 and filter capacitors C613/C614 produce about +12V DC into the NJM7805 regulator IC601. The +5V output from this IC powers all of the digital circuitry in the amplifier. Regulator IC18 (DM PCB) produces a +3.3V supply for the DSP6 ICs.

The power amplifier is a conventional, complementary-symmetry, Class AB type using nine transistors. A single pair of bipolar output devices (TR609 and TR611) are used and these, together with the thermal compensation transistor TR610 are mounted on a L-shaped aluminium heatsink screwed to the amplifier's bottom panel.

To prevent audible "thumps", a muting circuit consisting of transistors TR601 – TR603 and their surrounding passive components, briefly shorts the power amplifier's input signal to ground when the DG60FX-112 is switched on or off. The 8-ohm internal loudspeaker is directly coupled to the amplifier's output without an intervening relay.

The amplifier configuration used here would normally provide a very low (almost zero) output driving impedance to the loudspeaker. However, to provide a positive output impedance more characteristic of a valve output stage, the negative lead from the loudspeaker is returned to ground via a 0.33-ohm resistor R637. The signal current through the loudspeaker develops a voltage across this resistor, which is used as additional negative feedback. As the loudspeaker's impedance rises due its own resonance characteristics, less signal voltage is developed across R637. Consequently, less negative feedback is applied around the amplifier and so its gain increases, resulting in a larger loudspeaker signal. This accentuates the audible effects of the speaker's resonance characteristics.

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4 October 2002