Yamaha Electronic Musical Instruments

Clavinova CLP970 /CLP990 circuit explanation

1. Introduction

This document explains the circuitry of the CLP970 and CLP990 Clavinova models. The bulk of the text applies to the CLP970. However, the CLP990 differs from the CLP970 only in its use of a new wooden keyboard assembly and additional tone generation capability. These differences are detailed later. It is suggested that you use this text in conjunction with the Service Manual for the respective model.

These models incorporate circuitry that is representative of that used in many current Yamaha Electronic Musical Instrument products. The use of Surface Mount Devices (SMDs) is reducing the physical size of the Printed Circuit Boards (PCBs) used in these products to the point where, in some cases, it is cheaper to replace an entire PCB than it is to diagnose down to an offending component. However, many products are constructed as a collection of assemblies and it is still necessary to understand the workings of each assembly to avoid unnecessary PCB replacement.

2. Block diagram

The circuitry can be divided down into several sections, each performing a specific task –

- Main operating system, consisting of a CPU, EPROM, DRAM and Flash ROM.
- 88-note keyboard, Key Scanner (KSN) and Keyboard Interface IC (MI2)
- Panel circuitry, consisting of panel switches, LEDs, and LCD
- D-JACK PCB circuitry (MIDI, TO HOST, Pedals)
- Tone generator section, consisting of multiple, modular tone generator subsystems, Digital to Analog Converters (DACs) and analog circuitry

3. Main operating system

A Hitachi SH7043 series microprocessor (IC1) controls the entire unit. This is a 32-bit QFP device that includes internal program ROM, RAM, Serial Interfaces, Timers and other circuits. Additional peripheral chips that make up the rest of the operating system are the two EPROMs (IC7 and IC8), two DRAMs (IC5 and IC6), Flash ROM (IC22), address decoder (IC21), Serial Gate Array (IC4) and Floppy Disk Controller (IC2).

The signals or logic levels present at several pins of the CPU are crucial to the correct running of the operating system. These include –

/RES (pin 108) – Initial Clear input to CPU. This “hardware reset” signal is generated by the circuitry around IC18, an SN74HC132 quad Schmidt Trigger NAND gate. The CPU is the only device in the system that is reset by hardware. All other devices that need to be reset are done so by software-generated initial clear lines that are output from the CPU.

MD0 (pin 103) & **MD1** (pin 102) – Configures the CPU to use its on-chip 128KByte ROM (MD0="0", MD1="1").

MD2 (pin 97) & **MD3** (pin 95) – Sets the CPU's clock mode to internally multiply the 7MHz crystal oscillation frequency at pins 94 & 96 by a factor of four. This is achieved through the use of an internal Phase Locked Loop (PLL) circuit.

PLLCAP (pin 105) – Timing components for the internal master clock multiplying PLL.

/CS0 (pin 50) – Chip select for IC7 & IC8 EPROMs

/CS1 (pin 49) – Chip select for IC21, an SN74HC138, which then decodes address lines A20 & A21 to generate the enable signal for either the LCD, SIO4 chip IC4, or Flash ROM IC22.

/CS3 (pin 53) – Chip select for IC3, the MI2 Keyboard Interface chip.

/CS2 (pin 54) – Chip select for IC2, the Floppy Disk Drive (FDD) controller.

/CASL (pin32) & **/CASH** (pin 34) – Column address strobe signal for DRAM IC6.

/CASHL (pin 29) & **/CASHH** (pin 4) – Column address strobe signal for DRAM IC5.

/RAS (pin 31) – Row address strobe signal for both DRAM ICs

/WRL (pin 46) – Write enable signal for various eight-bit peripheral ICs. Although the CPU is a 32-bit device, a low logic level on this line signifies that the lowest eight bits of the 32-bit data buss have valid information that can be written to the peripheral chips.

/RD (pin 43) – Read signal for accessing data from peripheral ICs.

RD /WR (pin 35) – Read / write signal for DRAMs IC5 & IC6.

The EPROMs IC7 / IC8 and DRAMs IC5 /IC6 are 16-bit devices and each is paired with its partner to provide for the 32-bit CPU's requirements. Both ICs of a pair are simultaneously addressed and chip-selected but each outputs its data onto different halves of the 32-bit data buss.

The Flash ROM is used to store user settings. In previous models, a super capacitor and SRAM chip were used to back up this data, but if the super capacitor was left uncharged for a prolonged period (about one week), the data was lost. Compared to SRAM, writing to the Flash ROM takes longer, but no capacitor or battery is required for backup and the memory capacity is greatly increased.

The SIO4 gate array chip IC4 allows the CPU to read information from the SWX tone generator modules (to be described later). Real-time key and voice information is sent directly from the CPU's internal Serial Control Interface to the SWX modules as "one way" serial data and IC4 is *not* involved with this. However, during system boot-up and also during various steps in the test program, the CPU needs to determine which of the SWX modules is fitted or is faulty and it

achieves this by reading parallel data from IC4 that has been converted from serial ID data from the modules.

4. Keyboard and Interface circuitry

IC1 on the KSN2 PCB is a complete one-chip microprocessor whose sole purpose is to scan the keyboard and detect when keys have been pressed or released. A 4MHz ceramic resonator connected between pins 19 and 20 provides the master clock for this chip, and scanning begins immediately after the chip comes out of reset (as determined by the logic state of its /IC line, pin 26). The keyboard contacts are arranged in a matrix. One side of each key contact is connected to a common BK line with six other adjacent keys. The other side of each key contact is connected via an isolating diode, to an MK line that is common to all like-named notes; all “A” notes are connected together, all ”A#” notes are connected together, and so on. The KSN2 IC drives each BK line in turn to logic “0”, and while that line is low, checks the state of its MK inputs. When no key is pressed, all of the MK lines remain at logic “1”, being pulled high by resistors connected to +5 volts. A pressed key whose contact is currently being driven low by a BK line will pass this low via the isolation diode to the relevant MK line, and that key is then identified as having been pressed.

Double contacts are used under each key to provide velocity sensitivity. The physical shape of the key actuator ensures that when a key is pressed, one of the pair of contacts for that key closes before its partner. The time interval between the closures depends on the speed at which the key is struck and this interval is used to calculate velocity information. The actual calculation is done in the KSN2 IC.

Key events (key note on, key note off and velocity) are transmitted out from the KSN2 IC as serial data from SO pin 23, and a serial clock at a rate at which the transmission is sent, is output from XCK pin 25. The clock is present only while serial data is being transmitted, otherwise XCK is logic “1”. Pin 24, the ACK line, is normally at logic “1” and is pulsed low by the MI2 IC (IC3 on the DM PCB) whenever that IC is ready to accept serial data from the KSN2 IC.

The MI2 IC is capable of handling data from several keyboards at the same time; as would be the case with Yamaha Electone model organs that have three manuals – upper, lower and pedal. Additionally, it can serve as an interface between the Main and any Sub CPU systems in these organs. In the CLP970 however, the MI2 IC is used only as a single keyboard interface. The MI2 IC converts the serial key data from the KSN2 IC into parallel data and sends this to the main CPU via its data buss.

The MI2 IC issues a logic “0” on its /MIRQ output pin 10 to signal its need to send keyboard data to the main CPU. The main CPU then reads this data by setting the /MCS input pin 7 and /RD input pin 8 of the MI2 IC to logic “0”.

5. Panel Switch, LED and LCD Circuitry

a) Panel switches

The forty-six switches mounted on the front panel of the CLP970 are arranged in a matrix and scanned by the main CPU using a similar method to that used for the keyboard.

The constantly changing logic states of pins 111, 113 and 114 of the main CPU are decoded by a 74HC138 3 to 8 line decoder IC20, to provide negative going pulses at each of its eight

outputs, pins 7 and 9 – 15. These pulses are buffered and inverted by the transistor array, TA1 to provide the matrix drive lines, DV0 to DV7. Only one of these lines can be high (logic "1") at any given time. One side of each panel switch is connected to a DV line. The other side of each switch is connected to one of five switch sense lines, PS0 to PS5, which are in turn connected to pins 138, 139, 140, 123, 125 and 126 respectively of the main CPU and are each tied to logic "0" by 10K pulldown resistors. When a panel switch is pressed, the logic "1" level that may be present on that switch's DV line, forces the corresponding PS line to logic "1" as well.

The DV and PS lines can be thought of as the "rows" and "columns" of the matrix and this method of switch detection is almost universally used in all but the simplest systems. When the CPU drives any row, it checks the state of all the columns to determine if any switch is pressed. Since there are eight DV rows and six PS columns, it is possible to detect a total of forty-eight switches although only forty-six are used in this system.

b) Panel LED drive

If the matrix only involved switch scanning, the transistor array TA1 mentioned before would not be needed (apart from its inverting function). It is there to provide for the high current requirements of the twenty-one Light Emitting Diodes (LEDs) fitted to the same matrix. Each LED anode is connected to one of the seven drive lines DV0 to DV6, and its cathode is connected via a current limiting resistor to one of three "L" lines L1 to L3. These in turn are connected to the collectors of digital transistors, TR3, TR4 and TR5 (mounted on the DM PCB). CPU pins 115, 116 and 137 drive these transistors in turn to provide the ground return for the LEDs. An LED illuminates when the DV and L lines connected to it are simultaneously at logic "1" and "0" respectively. When illuminated, LEDs appear to be continuously on but are in fact are being turned on and off at a fast rate – a technique known as multiplexing. As is the case with switch matrix scanning, multiplexing is a very commonly used technique.

c) Liquid Crystal Display (LCD)

The CPU drives a 24-character by 2-line backlit LCD. When any instruction or display character data are to be sent to the LCD, they are placed on the CPU's data buss. The time duration during which this data exists on the buss is shorter than that required by typical LCDs, so IC17, a 74HC374 Octal Flip-Flop, is used to latch this data for use by the LCD. The combination of /WR and /LCDCS at pins 1 and 2 of IC19, a 74AC32 OR gate, results in a negative going pulse at its pin 3, the trailing edge of which latches the data to appear on IC17's outputs, LCD0 to LCD7. With the data now available to the LCD, several other control lines from the main CPU are set that allow the LCD to accept the data. LCDRS indicates whether the data is an instruction to be executed or a character to be displayed by the LCD. LCDENBL is a positive going pulse that allows the LCD to accept the data presented to it. LCDBLT allows the CPU to control the LCD's backlight. When at logic "1", LCDBLT turns on TR202 (mounted on the "PNR" PCB), which turns on constant-current source TR201 and illuminates the LEDs in the backlight. The viewing contrast of the LCD is varied by a potential divider arrangement consisting of two resistors and a "CONTRAST" potentiometer, VR201. The voltage at the wiper of the pot is buffered by TR203 and sent to the LCD.

6. D-JACK PCB circuitry (Pedals, MIDI, TO HOST)

a) Pedals

Damper (sustain), Sostenuto and Soft pedals and an Auxiliary pedal jack are provided and these interface directly with analog input pins on the CPU.

The Damper pedal uses a potentiometer connected between +5 volts and ground to provide a varying voltage to pin 119 on the main CPU. The Sostenuto and Soft pedals both use simple on/off switches, and connect to CPU pins 121 and 122 respectively. When pressed, each switch forces its CPU pin to ground (logic “0”), which is otherwise set to logic “1” (+5volts) by a 10K pull-up resistor.

An optional pedal can be connected to the Auxiliary Pedal Jack to provide Expression and other additional functions. The optional pedal can take the form of a continuously variable pedal, such as the Yamaha FC7 Foot Controller, or a simple pedal switch, such as the FC4 or FC5 footswitch.

When the FC7 is connected, the ring terminal of its Tip-Ring-Sleeve (TRS) ¼ “ plug provides a varying voltage between approximately zero and +5 volts, depending on the position of the pedal, and this is fed to analog input pin 120 of the main CPU. The FC4 and FC5 footswitches are normally-closed types and are each fitted with a Tip-Sleeve (mono) ¼ “ plug. Pressing or releasing the pedal feeds zero or +5 volts to the same CPU pin. Normally-open type footswitches are accommodated by user definable settings.

b) MIDI

MIDI communication with other instruments is directly to and from the CPU via the CLP970’s MIDI IN, OUT and THRU terminals. With the HOST SELECT switch (to be discussed later) set to the MIDI position, the current-loop signals received at the MIDI IN terminal are converted by IC3, a 6N137 photo-coupler, into voltage logic signals and fed to the RXD1 input pin 133 of the main CPU. They are also sent to transistors TR3 and TR4, which drive the MIDI THRU terminal. To transmit a MIDI message, the CPU outputs the signal from its TXD1 pin 134 to transistors TR1 and TR2, which drive the MIDI OUT terminal.

d) TO HOST Interface

The TO HOST connector allows the CLP970 to send and receive “MIDI” messages to and from the serial (or COM) port of a PC or MAC computer. Normally, the joystick port of a PC computer’s soundcard is used for MIDI communication but if a suitable interface is not used, problems can occur due to the incompatibility between MIDI’s use of a current loop and the TTL voltage level requirements of a joystick port.

IC2, an SN75C116B Driver-Receiver chip, converts between the RS-232 levels used by the computer’s COM port and the CLP970 circuitry’s CMOS logic levels. TO HOST signals to and from the CPU pass via the HOST SELECT switch to appear at pins 3 and 15 of IC2 respectively. IC1 buffers an internally generated 1-MHz clock that a connected MAC computer needs for correct serial communication.

The HOST SELECT switch can be set to one of four positions. Three of these allow communication via the TO HOST connector and the remaining position allows MIDI communication via the MIDI jacks. The switch has four poles. The first two route the transmit / receive lines from the CPU to either the MIDI or TO HOST jacks. When a MAC computer is used, the third pole switches the buffered 1-MHz clock to pin 1 of the TO HOST terminal.

Otherwise, it controls a PC computer's RTS/CTS lines. Depending on the switch position, the fourth pole sends one of four discrete analog voltages from a voltage divider consisting of resistors R2, R3, R4 and R5, to analog input pin 118 of the CPU. This tells the CPU what position the HOST SELECT switch is set to.

7. Tone generation

a) SWX modules

The CLP870's tone generation system consists of five "SWX" PCB modules, which each plug in to the main DM PCB. Each module is itself a complete sub-CPU system, containing a CPU/Tone generator IC, ROM, SRAM, WaveROM and in some modules, DRAM. The five modules are known as SWX-XG, SWX-A, SWX-C, SWX-E and SWX-F. Although the modules use a common PCB layout, they are not interchangeable as there are component differences between them and so each module must be fitted to its respective socket on the DM PCB.

As its name suggests, the SWX-XG module generates the XG voices of the CLP970 and the remaining four modules generate all the other voices. Each module has an allocated range of notes and voices and when it is called upon by the main CPU to generate its allocated sounds, it does so and passes the digital audio data on to the next module. The data is sent in the order of SWX-A -> SWX-C -> SWX-E -> SWX-F and mixed along the way. The Reverb effect is applied to the mixed signal in the SWX-F module. The data is then returned back to the SWX-A module, where the Chorus effect is applied before being sent to the SWX-XG module, where it is mixed with the XG sounds and finally sent to the DACs.

Being complete systems in themselves, the SWX modules operate independently of each other, but due to the series configuration of the digital audio path through them, all the modules need to be fitted for signal to appear at the instrument's output.

A twenty-pin connector connects each SWX module to the DM PCB. It has two rows (A and B) of ten pins each. A description of the signal or voltage at each pin follows –

A1, A2 – **+5V.** Digital power supply

A3 – **MIXIN.** Serial format digital audio input into the SWX module used to accept the signal from the preceding module

A4 – **RXD.** Asynchronous serial format ID signal input into the SWX module used to accept the signal from the preceding module

A5 – **SWXCLK.** Synchronous clock input into the SWX module used to clock SWXDATA into the SWX IC

A6 – **SWXDATA.** Synchronous serial format data input into the SWX module used to accept keynote and voice information from the main system CPU

A7 – **/SWXIC.** Software generated active-low Initial Clear or reset signal

A8 – **SYI.** 44.1KHz word clock input into the SWX module used to accept the clock from the preceding module

A9 – **MCLK.** 33.8688MHz master clock input into the SWX module

A10 – **0V** Digital power supply

B1, B2 – **+3.3V** Digital power supply for SWX IC

B3 – **MIXOUT.** Serial format digital audio output from the SWX module

B4 – **TXD.** Asynchronous serial format ID signal output from the SWX module

B5 – **MELOUT.** Alternative serial format digital audio output from the SWX module

B6 – **SYSCLK.** 16.9344MHz clock output from SWX module. Not used in this system

B7 – **QCLK.** 2.8224MHz bit clock output from SWX module (only used in "SWX-XG" module to provide the bit clock required by the DACs

B8 – **SYO.** 44.1KHz word clock output from the SWX module

B9, B10 – **0V.** Digital power supply

All of the SWX modules share common SWXCLK, SWXDATA, MCLK and /SWXIC lines and power supplies. RXD, TXD, MIXIN, MIXOUT, MELOUT, SYI and SYO allow digital audio and data flow through the series configuration of modules.

The digital audio format at the MIXIN, MIXOUT and MELOUT terminals differs between each SWX module. The relationship between the SWX modules and the formats used on each is listed below –

	SWX-XG	**SXW-A**	**SWX-C**	**SWX-E**	**SWX-F**
MIXIN	2ch/line	2ch/line	8ch/line	8ch/line	8ch/line
	MSB last	MSB last	MSB last	MSB last	MSB last
MIXOUT	1ch/line	8ch/line	8ch/line	8ch/line	not used
	LSB last	MSB last	MSB last	MSB last	
MELOUT	1ch/line	2ch/line	not used	not used	2ch/line
	LSB last	MSB last			

In the 2ch/line MSB last format (known as the MEL2 format), two 24-bit words representing two independent audio channel samples are transmitted on one line within the period of one word-clock (SYI or SYO) cycle. The MSB of each word is transmitted last. One word is transmitted

during the high level of the word clock, the other during the low level. Although this format has a 24-bit capability, only 16-bit words are used in the CLP970.

The digital audio path from the MIXOUT terminal of SWX-A through to the MIXIN terminal of SWX-F uses an 8ch/line format that allows some independence between each module's contribution to the overall signal. Like the MEL2 format, the MSB of each audio word is transmitted last but here, up to eight independent channels are transmitted in the period of one word-clock cycle.

b) Digital to Analog Converters (DACs)

The MIXOUT and MELOUT terminals of the SWX-XG module (representing the final left and right output channels of the tone generation system) each output a single channel 16-bit signal with the LSB transmitted last. The two Burr-Brown PCM1702 DACs - IC10 for the Left channel and IC11 for the Right - require this format. These are 20-bit devices that operate from +/- 5 volt power supplies derived from 78L05/79L05 series voltage regulators, IC12 and IC13. Single channel serial digital audio data words at a sampling rate of 44.1 KHz are input into pin 1 of each DAC. The data are clocked into the DAC by a 2.82 MHz bit clock applied to pin 2, and Latch Enable (/LE) pulses at the sampling rate are applied to pin 7. The negative transition of an /LE pulse latches the last 20 bits of serial data that preceded it, and converts the data to an analog signal current at Pin 14. This current is fed to the virtual earth inverting input of op-amp IC16, which converts it to a signal voltage for processing by the subsequent analog circuitry.

Differences between the CLP970 and CLP990

a) Tone generation

When the notes of an acoustic piano are sampled to provide the tone generation of an electronic keyboard, the number of samples taken is limited by the size of the memory available in which to store the samples. Because of this, it is quite common for samples to be taken several notes apart. To play back notes that are "in between" valid samples, the tone generation systems uses interpolation, filtering and crossfading techniques to provide a reasonable timbre. The piano's notes also need to be sampled at several velocity values, because striking a piano key softly doesn't result in a sound that is simply lower in volume than when struck hard – the timbre also changes.

The CLP970 uses valid samples for every third key (total of 30 keys sampled) with each of those keys having been sampled at five velocity points. The CLP990 uses a valid sample for each key (88 notes), each also having been sampled at five velocity points. To provide this additional capability, the CLP990 uses seven SWX modules as opposed to the CLP970's five. This increases the available WaveROM capacity and note polyphony from 72 MBytes and 160 notes (CLP970) to 152 Mbytes and 224 notes (CLP990).

Circuit operation of the CLP990's tone generation and most of its remaining circuitry is identical to that of the CLP970.

b) Wooden Keyboard

Since the introduction of the Clavinova product range in 1983, a number of different keyboard mechanisms have been used in an attempt to provide a realistic piano “feel”. Originally, this was achieved with lead weights moulded into the front of the individual keys. This mechanism was superseded by the “Action Effect” (AE) keyboard, which used swinging hammers and levers. Following this, the “Graded Action” (GH) Keyboard was introduced, which used different length wire hammers to grade the keyboard’s span into four zones to achieve a progressively lighter initial feel as higher keys were struck.

The electrical contacts used with these mechanisms ranged from metal leaf changeover types to dual contact rubber types, to provide the necessary velocity sensitivity. Regardless of the mechanical methods used, the electronics of the tone generation systems used with these mechanisms were only “aware” of two possible key states – key “on” or key “off”. The CLP990 uses a new wooden keyboard mechanism and multiple sets of key contacts not only to improve the mechanical feel but also to provide a characteristic known as “Key Off” sound.

Normally with a piano, if the player gradually releases a key, a damper-felt comes into contact with the string. The damper felt gradually restrains the vibration of the string until the sound finally stops. The sound from when the damper starts to touch the string until the sound stops is not just a change of the string’s volume level; the timbre also changes. This is called the Key Off sound.

Figure 1 is a simplified diagram of the CLP990’s wooden keyboard. It uses four normally-open switches for each key. Two of the switches detect whether the key is pressed or not, the other two detect the position of a weighted hammer that the key actuates when pressed. Physically, the switches are conventional rubber contact types similar to those used in other current Clavinova models.

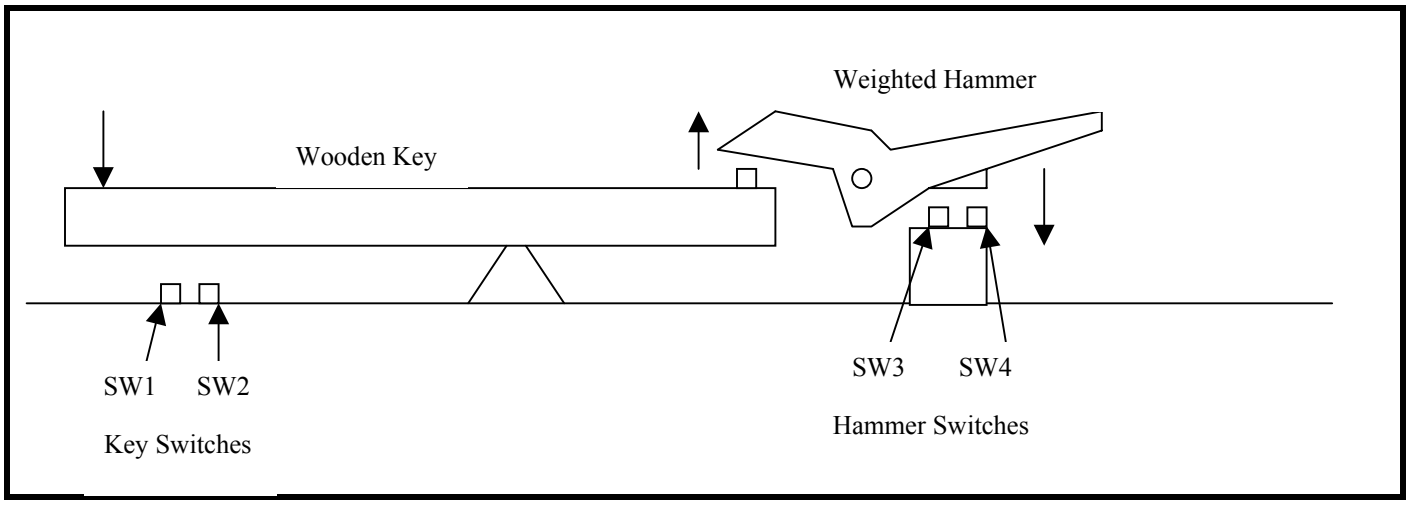

Figure 1 - Simplified Diagram of the CLP990 wooden keyboard

With the key in the rest position, all four switches are open. When the key is pressed, switch 1 is the first to close, then switch 2, then switch 3 and finally switch 4. At this point, the key is regarded as having been pressed and a “Key On” event occurs, triggering the tone generator to produce a sound. When the key is released, the switches open in the reverse order. However,

suppose that, after having been pressed fully, the key is then partially released to the position where only switch 1 remains closed. This corresponds to the condition on an acoustic piano where the damper felt is applying only light pressure on the string. The CLP990 generates the “Key Off Note” sound as opposed to the “Key Off” sound generated when switch 1 finally opens on full key release

In a keyboard using only a single set of contacts (as in the CLP970), the partial and fully released key positions cannot be distinguished from each other. In the CLP990, the dual switch-set configuration also allows a more realistic sound when playing fast, repetitive keystrokes. The keyswitch timing during normal and repetitive playing is shown in Figure 2.

Three KSN2 Keyboard Scanner ICs are used in the CLP990 as opposed to the single device used in the CLP970. The multiple-keyboard capability of the MI2 Keyboard Interface IC is used to accept the data from the two KSN2 ICs. Its operation with each KSN2 IC is identical to that described for the CLP970.

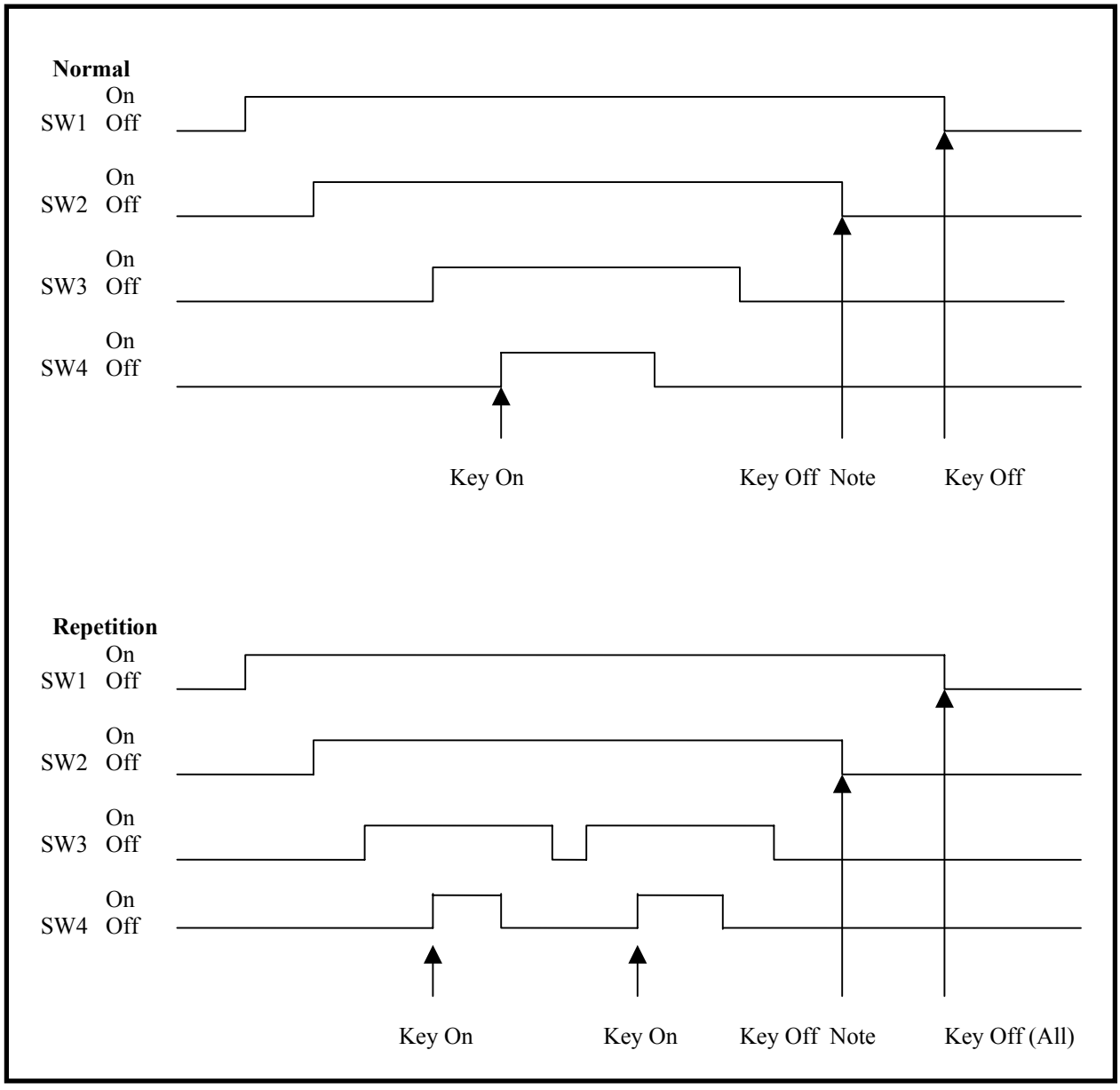

Figure 2 - Keyswitch timing during normal and repetition keypress

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