Yamaha Digital Bass Guitar Amplifier

BBT500H Circuit explanation

1. Introduction

This document details the circuit operation of the BBT500H Digital Bass Amplifier Head. Although Yamaha has released several digital guitar amplifiers in recent years, the BBT500H is the first model to use a Class D, PWM Digital Power Amplifier to drive loudspeakers. This, together with an in-built Switch-Mode Power Supply (SMPS) allows the BBT500H to deliver 500W/2 ohms from a package that weighs only 5Kg! Apart from the use of several op-amps in the Input, FX Send/Return and Line Out stages, all signal processing including power amplification is performed in the digital domain. Microprocessor control of all functions also allows up to five "patches" to be memorised and recalled using MIDI or front-panel selection.

It is suggested that you use this text in conjunction with the Service Manual for this model.

2. Block Diagram

The circuitry can be divided down into several sections, each performing a specific task (see Figure 1):

- Analog input/output circuitry and AD/DA converters
- Main control system, consisting of a CPU, FlashROM and SRAM
- Front panel circuitry, consisting of switches, LEDs and potentiometers
- Digital Signal Processor
- High-Efficiency Switch-Mode Power Supply
- High-Efficiency Class D PWM Power Amplifier

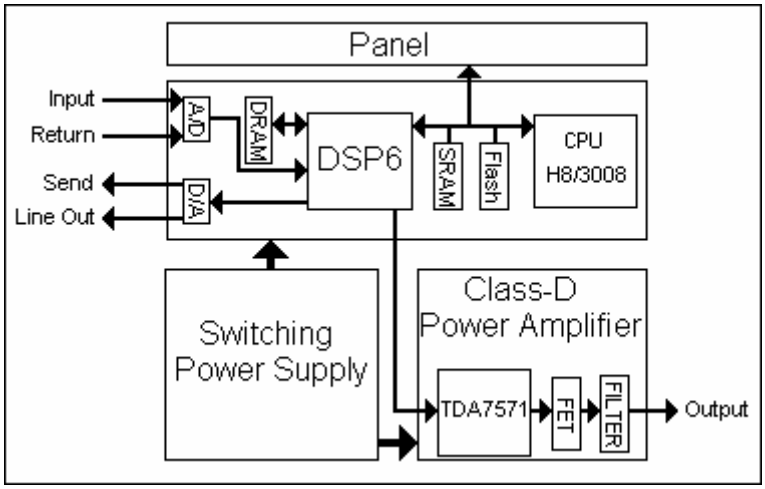


Figure 1. BBT500H Block Diagram

3. Analog and AD/DA circuitry

a) Input Preamp

BBT500H Overall Circuit Diagram 1/2 (DM2/2) Grid Reference B8

The Input Preamp circuitry is located on a small front-panel mounted PCB (DM2/2). The bass guitar signal enters the amplifier via a single ¼" jack. The initial preamp stage consists of a dual, low-noise, FET input NJM072M op-amp IC301. One half of IC301 buffers the input with a 1-Megohm impedance as set by resistor R302, and a gain of +35dB and -8.5dB respectively at

the maximum and minimum settings of the INPUT LEVEL potentiometer VR301. Back-to-back diodes across the opamp inputs protect against excessively high input levels.

The optimum setting of the INPUT level control for a given input is indicated by LEDs LD301 (red) and LD302 (green), which are driven by transistors TR301 - TR303 and the remaining half of IC301. If the preamp output level is too low, none of the transistors is forward-biased and the LEDs remain unlit. As the signal level increases, TR303 will be the first to turn on to illuminate the green LED. When the signal level is higher than optimum, diodes D303 and ZD301 conduct to allow positive-going signal peaks to turn on Tr301/TR302, which illuminates the red LED.

The preamp output signal leaves the DM2/2 PCB on CN302 pin 1 and ends up at the DM1/2 PCB at CN106 pin 1. Here, it is fed to both the A/D converter circuitry, and to the TUNER OUT ¼" jack on the rear panel. Apart from this jack's obvious use, it can also be used to feed another BBT500H to create a bi-amplified system, where one amplifier is used to drive high frequencies and a second amplifier drives the lows. Each amplifier's onboard crossover filter (LPF or HPF) will determine the range of frequencies that it will deliver.

b) A/D converter

BBT500H Overall Circuit Diagram 1/2 (DM1/2) Grid Reference E7

IC122 is an AK5383-VF Stereo 24-bit Analog-to-Digital Converter (ADC) chip. In the BBT500H, the preamp signal is applied to the ADC's left-channel inputs (pins 4 & 5), while the FX LOOP RETURN signal is applied to its right-channel inputs (pins 24 & 25). Since these inputs are differential types, NJM5532 opamps IC112 and IC114 generate a balanced or differential version of either the input preamp's output signal (IC112) or the RETURN signal (IC114). A +2.5V DC reference derived from resistors R121 and R122 sets the quiescent output levels of IC112/IC114 to the midpoint of the ADC's input voltage range. The ADC's MSB-first, 2's complement, 2-ch/line digital audio output appears at SDATA pin 15 (see Figure 2).

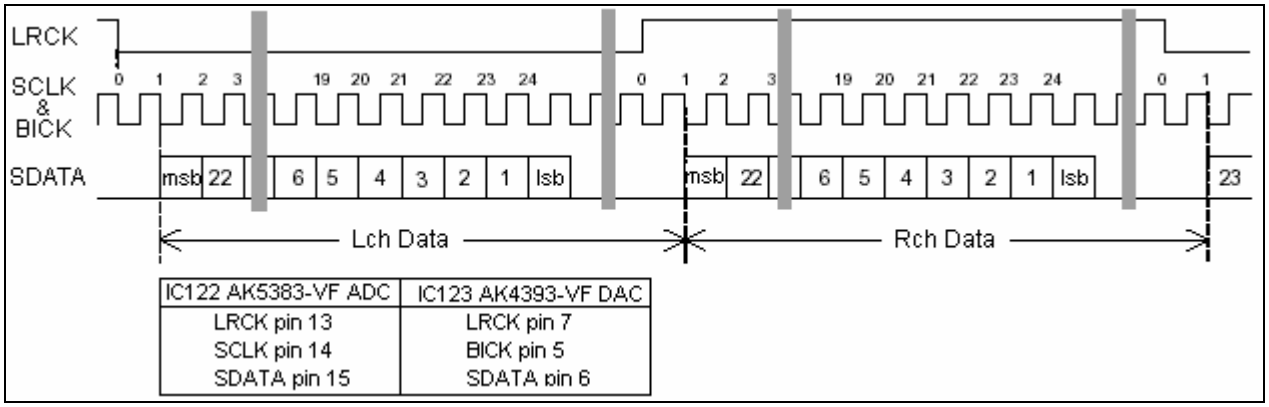


Figure 2. ADC/DAC Serial Data Timing

c) D/A Converter & Analog outputs

BBT500H Overall Circuit Diagram 1/2 (DM1/2) Grid Reference F8

IC123 is an AK4393-VF Stereo 24-bit Digital-to-Analog Converter (DAC) IC. After processing by the DSP IC, the MSB-first, 2's complement, 2-ch/line EFFECTS SEND and LINE OUT digital audio signals are applied to the DAC's SDATA input pin 6 (see Figure 2). The DAC's analog outputs appear in differential form at pins 23 & 22 (SEND signal) and pins 21 & 20 (LINE OUT signal), and are converted into their respective single-ended signals in the NJM5532M dual opamp IC113. The SEND signal at IC113 pin 1 is fed into one half of another NJM5532 opamp IC115, which in turn feeds the rear-panel SEND output jack. The signal level at this jack (and incidentally, the sensitivity of the RETURN jack) can be set to either +4dB or -20dB by the rear-panel FX LOOP LEVEL switch SW105. This switch alters the signal feedback around IC115, and hence its gain (and also that of IC114 in the ADC section).

The rear-panel LEVEL potentiometer VR101 varies the level of the LINE OUT signal at IC113 pin 7 before sending it to several final opamp stages: IC117 (NJM4556) for PHONES; IC115 (NJM5532M) for UNBALANCED LINE OUT; and IC118 (NJM4556) for XLR BALANCED LINE OUT.

Inserting a headphone plug into the PHONES jack causes its switching contacts to put +5 volts onto the HP_MUTE line to the digital power amplifier's muting circuitry, shutting off the SPEAKER output signal.

d) AD/DA clock generator

BBT500H Overall Circuit Diagram 1/2 (DM1/2) Grid Reference D8

A 22.579 MHz crystal connected around one section of an SN74LVU04A hex-inverter IC116 generates the master clock. This is buffered by a second inverter within IC116 and fed to an SN74LV4040A binary counter IC119, which provides frequencies of 11.289MHz, 5.644MHz, 2.822MHz and 44.1Khz at its QA, QB, QC and QI outputs respectively.

Table 1 shows how the available clocks are distributed around the digital audio circuitry.

CLOCK	FREQUENCY	DESTINATION
256Fs	11.289MHz	IC107 (PW PCB) Digital Power Amp MCK Pin 46
		IC122 ADC MCLK Pin 17
		IC123 DAC MCLK Pin 3
128Fs	5.644MHz	IC104 DSP MCKS Pin 13
64Fs	2.822MHz	IC107 (PW PCB) Digital Power Amp SCK Pin 50
		IC122 ADC SCLK Pin 14
		IC123 DAC BICK Pin 5
Fs	44.1KHz	IC104 DSP SYNCI Pin 6
		IC104 DSP SSYNC Pin 14
		IC107 (PW PCB) Digital Power Amp WS Pin 50
		IC122 ADC LRCK Pin 13
		IC123 DAC LRCK Pin 7

Table 1. Digital Audio System clocks

4. Main control system

BBT500H Overall Circuit Diagram 1/2 (DM1/2) Grid Reference E2

A single Hitachi H8/3008 series microprocessor IC106 (CPU) controls the entire unit. This is a 100-pin QFP device that includes internal RAM, Serial Interface, A/D converter, Timers and other circuits. Additional peripheral chips that make up the rest of the control system are the 4-Mbit Program Flash ROM IC101, the 256-Kbit SRAM IC102, and Reset Controller IC103.

Many of the CPU's pins allow it to interface with external chips that for example, read switches or controls, or drive LED, etc. These pins act as so called "ports" that don't directly affect the CPU's ability to execute a program stored in the ROM. The signals or logic levels present at several specific pins of the CPU however, are crucial to the correct running of the control system. These include –

XTAL (pin 67) and **EXTAL** (pin 66) – A 16.00MHz crystal is connected across these pins, and together form the CPU's master clock oscillator.

/RES (pin 63) – Initial Clear input to CPU. The Reset Controller IC103 generates this "hardware reset" signal. On power-up, this line will stay low for about 100 milliseconds, after which it will switch high, allowing the CPU to operate.

MD0 (pin 73), **MD1** (pin 74) and **MD2** (pin 75) – Configures the CPU to have access to a 16-Mbyte address space and to use its internal 4K bytes of RAM (MD0="0", MD1="0", MD2="1"). These pins are tied to either 0V or +3.3V supply lines.

/CS0 (pin 91) – Chip Enable for Program Flash ROM IC101. This pin always has negative-going pulses on it because IC101 is the sole source of instructions that the CPU fetches and executes. There is no internal CPU ROM.

/CS1 (pin 90) – Chip Enable for SRAM IC102. This pin always has negative-going pulses on it because of the CPU's constant need to access the SRAM, when writing data to or reading data from it.

/CS2 (pin 89) – Chip Select line for DSP IC104. This pin is normally high but will pulse low whenever the DSP IC is called upon to change memories or adjust parameter values.

/RD (pin 70) – Read signal for accessing data from peripheral ICs. Like the **/CS0** signal, this pin constantly pulses because of the CPU's need to fetch instructions from the Flash ROM or read data from the SRAM and when required, from the DSP.

/HWR (pin 71) – Write-enable signal for the Flash ROM, SRAM and DSP ICs. This pin constantly pulses because of the CPU's need to write data to the SRAM and when required, to the DSP.

The CPU's data lines (D0-D15) and address lines (A0-A19) should all show activity when the system is running correctly.

5. Front Panel Circuitry

a) Switches and LEDs

BBT500H Overall Circuit Diagrams 1/2 (DM1/2) Grid Reference G5, and 1/2 (PN) Grid Reference K8

The switch circuitry is driven by the system CPU and is shown in block form in Figure 3. Seven momentary, push-button switches on the front panel and three slide switches on the rear panel are arranged in a 3-column x 4-row matrix. The CPU generates cyclic negative-going pulses on its Port lines P60 to P62. These are buffered by a 74LV245 octal transceiver IC107 and applied to the switch matrix as column-drive lines SW_0 to SW_2. When a switch is pressed, the negative column pulses appear on one of the row lines SW_A to SW_D, and are buffered by IC110, another 74LV245 octal transceiver, which then feeds them to CPU Input Port lines P91 and P93 to P95.

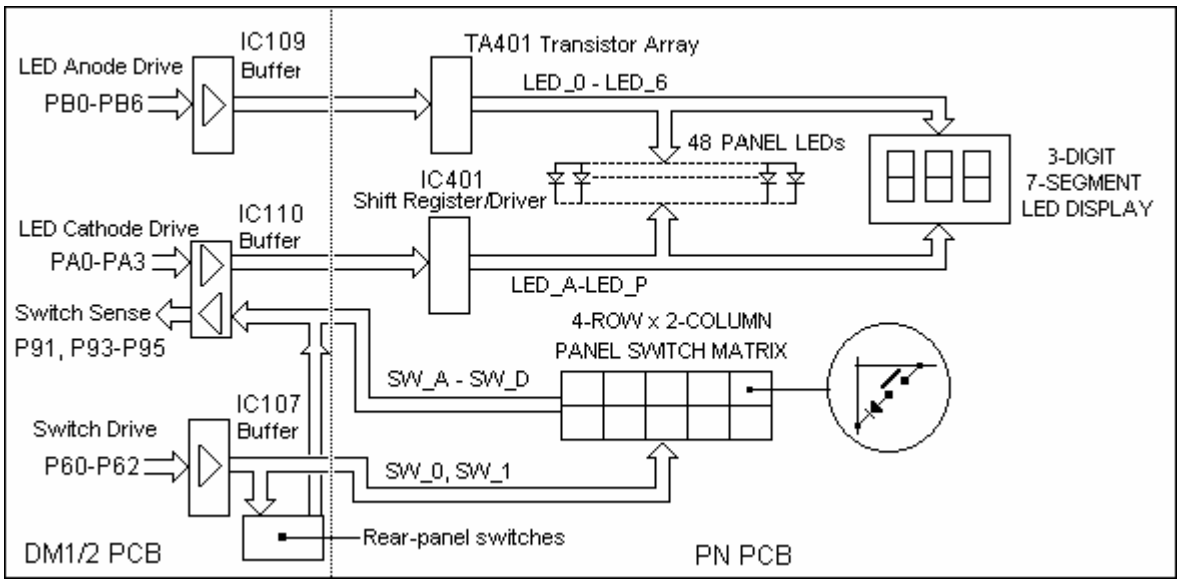


Figure 3. Switch/LED section block diagram

BBT500H Overall Circuit Diagrams 1/2 (DM2/2) Grid Reference C4, and 1/2 (PN) Grid Reference N8

Like the switches, the seventy-two front-panel LEDs are directly scanned by the CPU, although most of these are normally unlit and hidden behind the darkened, transparent front panel. The LEDs are driven in a conventional multiplexed fashion: Transistor Array TA401 supplies the LED anodes with positive-going drive pulses on lines LED_0 to LED_6, while the LED cathodes are driven low by Shift Register/Driver IC401 on lines LED_A to LED_P, as shown in Figure 3.

The LED anode drive lines LED_0 to LED_6 are simply buffered, inverted versions of CPU Port lines PB0 to PB6. Each Port line individually pulses low for 800 microseconds every 8 milliseconds. When it does, the group of LEDs driven by that line has a positive supply available to it. To turn on a LED or LEDs in that group only requires the relevant LED cathodes to be driven low by IC401. To do this, the following sequence of events occurs on Port lines PA0 to PA3:

- Port line PA0 provides IC401 with the 16-bit serial data representing the desired LED cathode pattern.

- As each serial data bit appears, it is clocked into IC401's internal shift register by a clock pulse on Port line PA1 (a total of sixteen clock pulses).

- When all the data has been clocked in, Port line PA2 pulses high to latch the data.

- Finally, PA3 goes low to allow the internal state of IC401's 16-bit data register to appear at its output pins.

Since IC401 provides a constant-current drive on its outputs, the LED cathodes are driven directly without the need for current-limiting resistors. The 100-ohm resistor R401 determines the constant-current value.

b) Potentiometers

BBT500H Overall Circuit Diagram 1/2 (DM2/2) Grid Reference F5, and 1/2 (PN) Grid Reference M11

Ten rotary potentiometers are mounted on the Front panel PN PCB to allow the bass-guitarist control over familiar parameters such as BASS, MIDDLE, TREBLE, etc. Unlike a conventional amplifier, no audio signals pass through the potentiometers; they simply provide continuously variable DC voltages between 0V and +3.3V, which the CPU uses to control the relevant parameter. One of these potentiometers – the SOUND TYPE control – is mechanically detented to simulate the action of an 11-position rotary switch. It functions as a "stepped" potentiometer, selecting eleven discreet DC voltages as it is rotated. Figure 4 shows the potentiometer circuitry in block form.

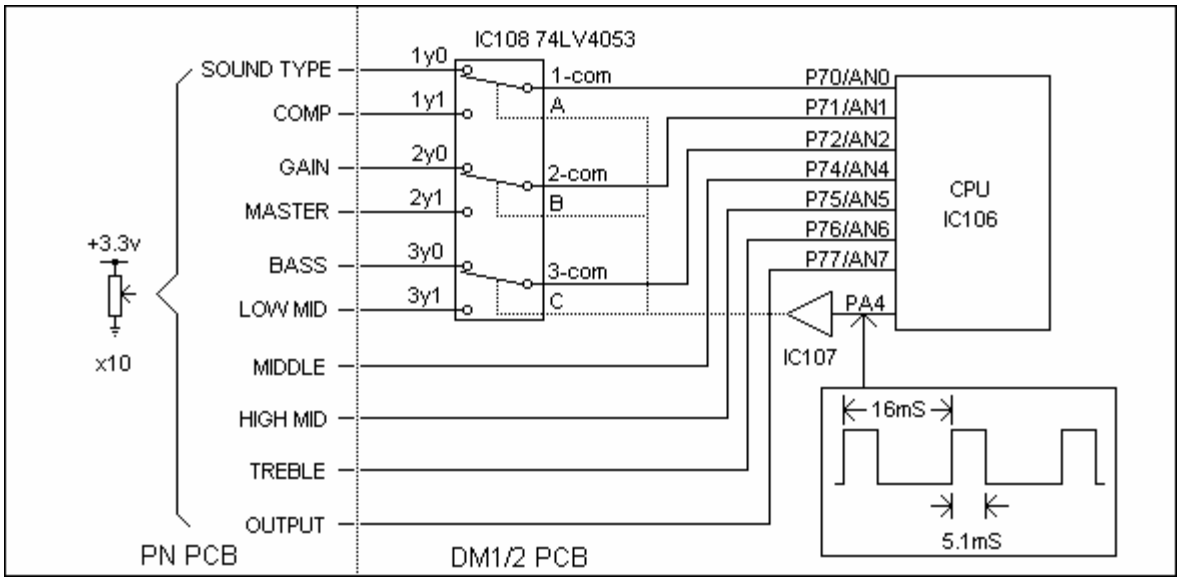


Figure 4. Potentiometer section block diagram

The outer terminals of each potentiometer are connected across the +3.3V supply, and each wiper terminal is connected either directly to one of the CPU's analog input ports, or indirectly via a 74LV4053 Triple 2-input Analog Multiplexer IC108, which is used because there are more potentiometers than there are CPU analog inputs. The logic state of CPU Port line PA4 determines which of the two groups of three potentiometers is connected to the CPU.

6. Digital Signal Processing

BBT500H Overall Circuit Diagram 1/2 (DM2/2) Grid Reference C4

All of the digital signal-processing in the BBT500H is performed by a single YSS910 (DSP6) integrated circuit IC104. A block diagram of the DSP6's internal circuitry, and its pin functions, are shown in Figure 5 and Table 2 respectively.

The DSP6 can accept and output multi-channel, digital audio signals in serial or parallel form and perform 32-bit processing of these signals.

In the BBT500H, only serial format input and output signals are present; the parallel interface pins are not used. However, the microprogram, coefficient and control data required by the DSP6 to process digital audio signals are input as parallel data via its CPU interface. This allows a much faster realtime re-configuration or setup of the device when changing parameters or patches compared to most of Yamaha's earlier DSP chips, which used a serial control interface.

Memory space necessary for effects (reverb, delay, phasing, etc) is provided by the 4Mbit DRAM IC105.

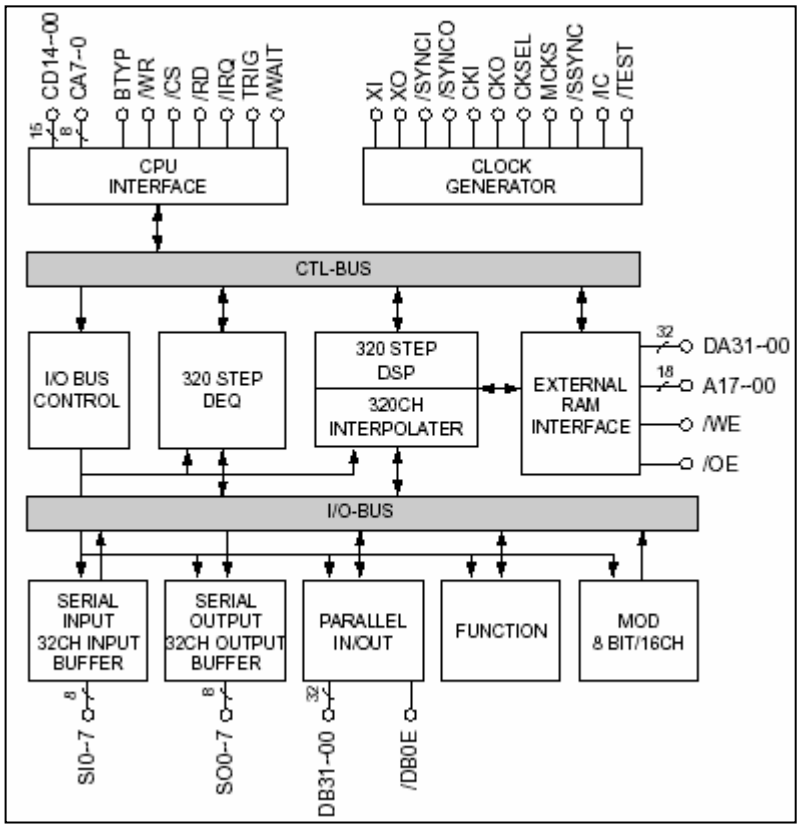


Figure 5. YSS910 (DSP6) IC internal circuitry block diagram

A single, 30MHz crystal oscillator provides the master clock for the internal operation of the DSP6 IC. The actual clocking of digital audio signals into and out of each device is dependent on sync and bit clocks, which have already been described. A failure of the master 30MHz clock will stop all signal activity through the DSP/DRAM section even if sync and bit clocks are still present. Since all signal flow is in serial form (with the exception of parallel data between the DSP and its DRAM), the presence of signals at the device pins can easily be monitored with an oscilloscope synchronised to the "Fs" 44.1KHz system word-clock.

Pin name	I/O	Function	Typical condition
XI	I	System master clock input	30MHz clock
XO	O	System master clock output	Not used, open pin
/SYNCI	I	System synchronous clock input	48KHz SYNC clock
CKI	I	System clock input	Not used, connected to ground
/SYNCO	O	System synchronous clock output	Not used, open pin
CKO	O	System clock output	Not used, open pin
CKSEL	I	System master clock select (60/30MHz)	+3.3V (30MHz mode selected)
MCKS	I	Serial I/O master clock input	5.644MHz (128Fs) clock
/SSYNC	I	Serial I/O synchronous clock input	44.1KHz SYNC clock
/IC	Is	Initial Clear	Low (0V) level briefly on power-up, then switches to and remains high (+3.3V)
/TEST	I+	Test mode	+3.3V (Normal mode)
CD00-15	I/O	Host CPU data buss	Normal CPU data buss activity
CA0-7	I	Host CPU address buss	Normal CPU address buss activity
BTYP	I	Host CPU data buss width select	+5V (16-bit mode selected)
/CS	Is+	Chip Select	Normally +3.3V but pulses low when access to the device is needed during patch or parameter changes
/RD	Is+	Read signal	Constantly pulsing
/WR	Is+	Write signal	Normally +5V but pulses low when changing patches or parameters
/IRQ	O	Interrupt Request	Not used, open pin
TRIG	I/O	Transfer trigger signal input/output	Not used, open pin
/WAIT	O	WAIT output	Not used, open pin
SI0-7	I+	Serial digital audio data inputs	SI0 only, pulses when signal present. Remaining input pins unused and grounded
SO0-7	O	Serial digital audio data outputs	SO0/SO1 only, pulses when signal present. Remaining output pins unused, left open
DB00-31	I+/O	Parallel digital audio data in/out	Not used, open pins
TIMO/DBOE	I/O	Timing output/Parallel buss control input	Not used, connected to +3.3V via 10K resistor
DA00-31	I+/O	External memory data buss	DA16-31 only, pulses when signal present
A17/CE	O	Address/Chip Enable	Not used, open pin
A16/CAS	O	Address/Column Address Strobe	Pulses on IC105
A15/RAS	O	Address/Row Address Strobe	Pulses on IC105
A09-14	O	External memory address buss	Not used, open pins
A00-08	O	External memory address buss	Pulses on IC105
/WE	O	External memory Write Enable	Pulses on IC105
/OE	O	External memory Output Enable	Pulses on IC105
VDD	-	+3.3V supply	
VSS	-	Ground	

Table 2. YSS910 (DSP6) IC pin functions

7. High-Efficiency Switch-Mode Power Supply (SMPS)

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference A4

The SMPS in the BBT500H is essentially the same as that fitted to the EMX5000 mixer, the main differences being the use of a dual-section mains filter, and much lower supply voltage rails for the Digital Power Amplifier. The block diagram of the SMPS is shown in Figure 6.

All of the SMPS's circuitry is mounted on the PW PCB together with that of the Digital Power Amplifier. The functions of the line filter, power switch and fuse are self-explanatory.

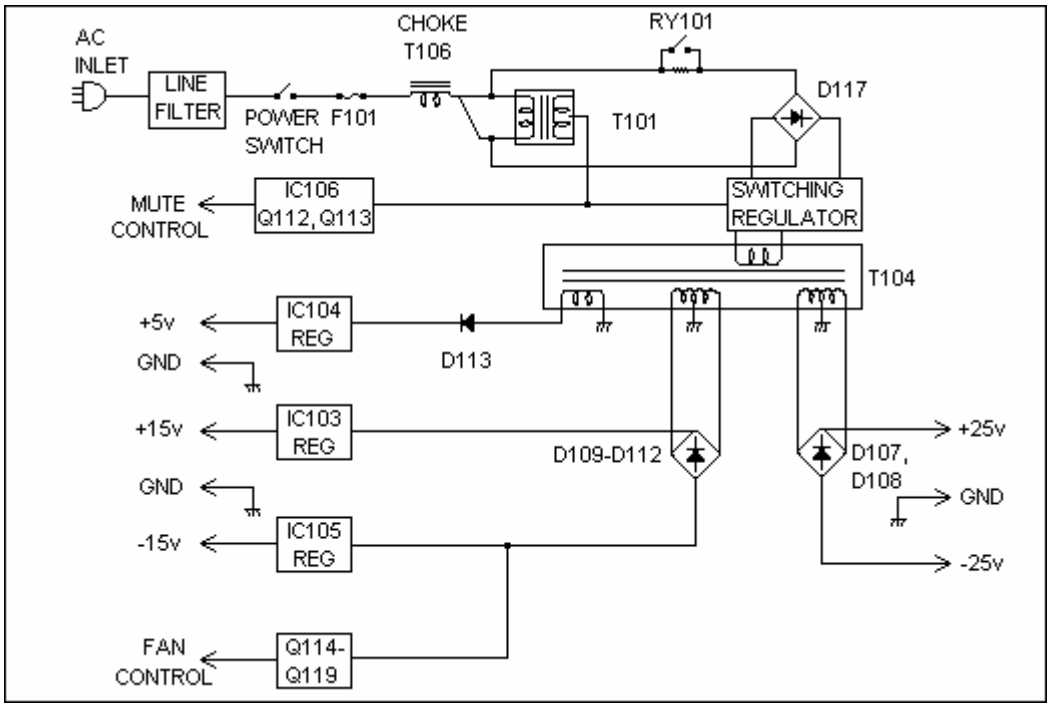


Figure 6. High-Efficiency Switch-Mode Power Supply block diagram

Relay RY101 is initially unenergised and its contacts are open when power is first applied, so the incoming 240V AC reaches the bridge rectifier D117 via two, series-connected 6.8-ohm 5W resistors R123 and R124. These limit the peak current into the (initially) discharged electrolytic capacitors C118 and C119. After the SMPS starts up, RY101's coil is energised and its contacts short out R123 and R124 to provide full power capability.

Using the negative terminal of C119 as a reference, the voltage at the positive terminal of C118 is about 340V DC (A-spec model). The 22Kohm resistors R121 and R127 maintain a "half supply" of 170V DC. A regulated +15V DC supply for the switch-mode controller IC102 is derived from low-voltage transformer T101 and 7815-type regulator IC101.

a) Switching regulator

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference D3

Resistor R102 and capacitor C111 are the timing components for the 70KHz oscillator inside IC102. Out-of-phase rectangular pulses of 15V p-p amplitude appear at pins 7 and 5, and drive complementary transistor pairs Q106/Q107 and Q108/Q109. Each pair drives its respective power-switching Insulated-Gate Bipolar Transistor (IGBT) Q110 or Q111.

Unlike a conventional transistor, an IGBT is voltage-driven, not current-driven, but it still requires a current to charge and discharge its gate capacitance (just like a MOSFET). This ensures efficient switching at high frequencies. This is the reason why Q110/Q111 are driven by buffer stages rather than directly from IC102. Gate resistors R118/R119 slow down the turn-on time of their respective IGBT, while diodes D104/D105 ensure rapid turn-off. This increases the short period of time (the necessary "dead time") within each switching cycle when neither IGBT is on.

One end of the primary winding of the high-frequency, switching transformer T104 is connected via capacitor C117 to the 170V “half supply” mentioned earlier. The other end of T104’s primary winding is alternately switched to either 0V or 340V DC by Q111/Q110. The voltages induced in T104’s secondary windings are rectified and filtered in conventional fashion to provide all of the required supply rails. Note that there is no actual regulation of secondary voltages by optical or transformer feedback to IC102.

b) Overcurrent protection

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference E4

An excessive current drawn from T104’s secondary windings will activate the SMPS’s overcurrent protection circuit consisting of transistors Q101, Q104 and Q105 to effectively switch off the entire power supply.

Under normal conditions, Q101 is off and IC102 operates to produce switching pulses. When an overload occurs, the current reflected into T104’s primary winding from the high secondary winding current develops a voltage across resistors R116/R117 that switches on Q105. This in turn switches on Q104 and Q101. This disables IC102’s oscillator and all switching of T104 ceases. In addition to turning on Q101, Q104 also feeds back to the base of Q105, which “latches” on to maintain this shutdown state. The only way to restore switching operation (assuming a temporary overload condition initiated the shutdown) is to turn off the POWER switch, then turn it back on.

A sustained, high secondary current draw whose value is not sufficient to trip the overcurrent protection circuit will tend to increase the dissipation of Q110/Q111, making them run hotter than normal. To protect against excessively high device temperatures, a Positive Temperature Coefficient (PTC) thermistor PR101 is mounted on the same heatsink as Q110/Q111 and monitors its temperature. When cold, PR101’s resistance is low and transistor Q103 is off. If Q110/Q111 get too hot, the subsequent increase in PR101’s resistance will allow Q103 to turn on and initiate the same shutdown sequence described earlier.

Transistor Q102 inhibits IC102’s oscillator (and consequently, SMPS operation) for a short time after initial power-up. Initially, C113 is discharged and turns on Q102, which turns on Q101, inhibiting oscillation. As C113 charges up, Q102 and Q101 progressively turn off to allow normal SMPS operation.

c) Muting Control

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference D5

This circuit is used to mute the Digital Power Amplifier both on power-up, and as soon as either the POWER switch is turned off or if there is any interruption to the 240V AC supply.

On power-up, capacitor C132 is initially discharged, which turns on transistor Q113 to put +15 volts onto the MUTE line, disabling the power amplifier. Eventually, when C132 has charged through resistor R131, Q113 turns off and the MUTE line falls to -15 volts. As long as mains power is present and the BBT500H is switched on, Q113 remains off because Q112 is kept off

by the action of the photo-coupler IC106. The low-voltage AC from transformer T101 is half-wave rectified and lightly filtered, and illuminates the LED portion of IC106. Consequently, IC106's transistor saturates and reverse-biases Q112. As soon as the BBT500H is switched off, IC106's LED is extinguished, and Q112 discharges C132 to enable the MUTE condition.

d) Fan control

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference G6

The BBT500H incorporates a rear-panel mounted, two-speed cooling fan that is controlled by transistors Q114 to Q119. The fan and its control circuitry are connected between GND, and the -25V supply rail to the -15V regulator (a positive-ground system).

The temperature-sensing elements are two, Positive-Temperature-Coefficient (PTC) thermistors PR102 and PR103. PR102 is mounted on, and monitors the temperature of, the main power amplifier heatsink, while PR103 monitors that of one of the main rectifying dual-diodes (D107) for the high-current secondary supply rails.

The thermistors, and resistors R141 (5.6K) and R144 (470-ohm), form a voltage divider between the emitter of Q114 and the -25V rail. Zener diode ZD1 maintains Q114's emitter at about 11.5-volts above the –25V rail (in other words, there is 11.5V across the voltage divider). The voltage across each resistor determines whether the transistor connected across it (Q114 and Q116 respectively), is turned on or off.

When the BBT500H is cold, the thermistors have a low resistance, and both transistors are on. This shorts the base of Darlington-connected Q117/Q118 to the –25V rail, disabling the fan. As the thermistors' resistances rise with increasing temperature, Q116 is the first to turn off, releasing its stranglehold of Q117's base. Q115 is still turned on however, as is Q119, whose collector is shorting the cathode of zener diode ZD2 to -25V. Q117's base is now allowed to rise to result in around 10 -11 volts appearing across the fan, allowing it to run at its low speed.

If the heatsinks' temperatures continue to rise, the thermistors' resistances will increase proportionally, eventually turning off Q115 and Q119. This allows Q117/Q118 to supply around 25-volts to drive the fan at its high speed.

8. High-Efficiency Class-D PWM Power Amplifier

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference C9

The choice of an SMPS over a conventional, transformer/capacitor power supply, particularly in a high-output power amplifier such as the BBT500H, is made mainly on the basis of weight reduction. Power supply *efficiency* is a secondary consideration when regulated supply rails are not needed, such as in most power amplifiers.

However, low efficiency and consequently, heat generation are inherent in the operation of a conventional Class AB power amplifier's output-stage. Many novel designs to improve output-stage efficiency have appeared over the years, with varying degrees of success. As an example

of one of these designs, Yamaha's EEEngine power amplifier circuit has for some years now been used in many of its products.

Consequently, to cater for the demand for even higher-efficiency and more compact power amplification, particularly now that digital signal sources predominant, fully digital, switchmode audio power amplifier driver ICs have become available. The BBT500H uses the TDA7571 device (IC107 located on the PW PCB) from ST Microelectronics. Originally developed for automotive sound systems, it takes in an I2S-format digital signal into its two internal audio channels, and in conjunction with twelve MOSFET output devices, it delivers 500Watts into a 2-ohm bridge-connected loudspeaker load.

While a better idea of the TDA7571's overall operation is best gained from the block diagram rather than the BBT500H circuit diagram, in the following description, all component numbers are of those shown in the latter. The internal block diagram and simplified application diagram of the TDA7571 is shown in Figure 7.

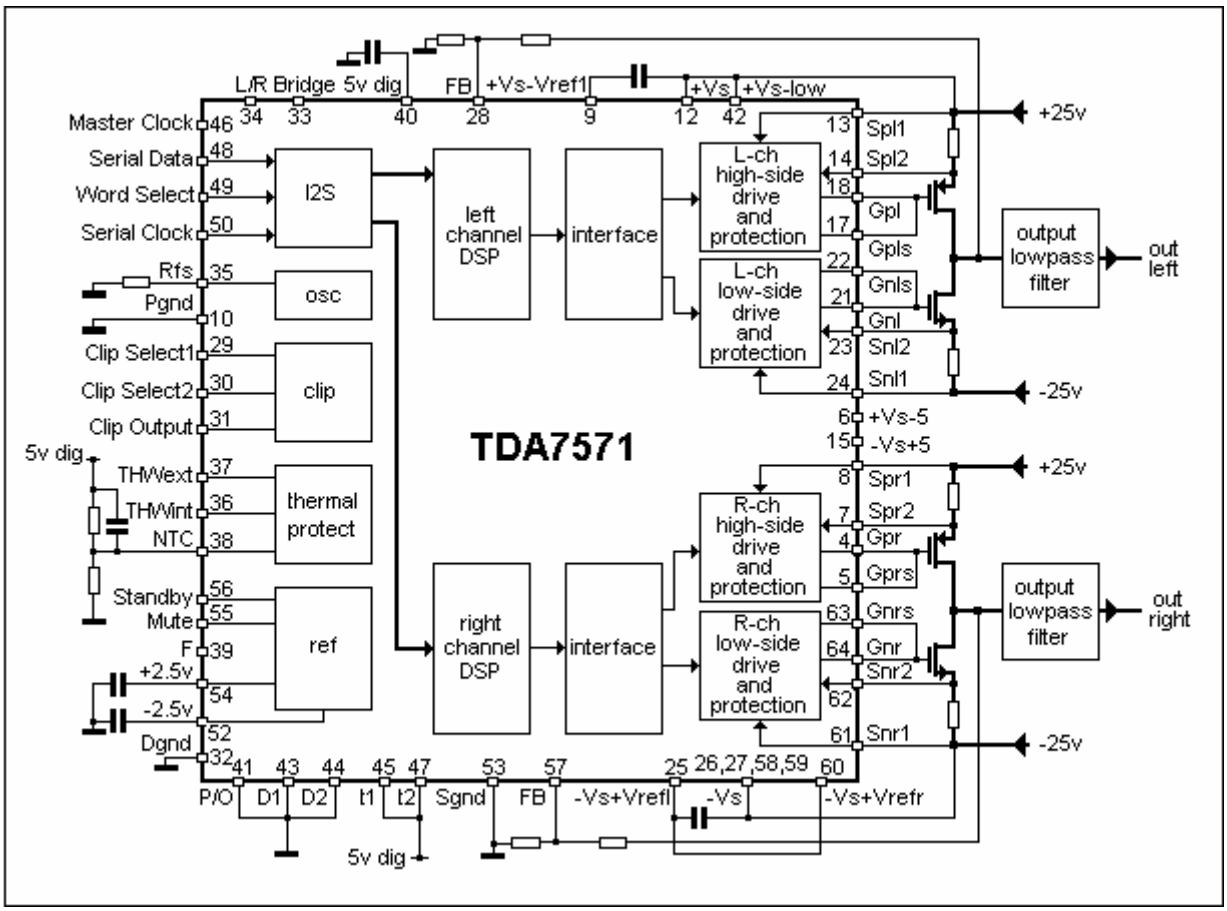


Figure 7. TDA7571 Internal block and simplified application diagram

a) Mute, Standby

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference C11

On power up, the System Reset IC108 pulls IC107's ST-BY pin 56 low for 100mS to reset its internal circuity, after which it goes high to +5V. During this reset time, there is no PWM (8Fs squarewave) waveform at IC107's outputs.

The generation of the power-on/off MUTE signal from the power supply circuitry has already been described. When high (+15V), the MUTE line turns on transistor Q132 via diode D119. This pulls pin 55 (MUTE) low, which mutes IC107's signal outputs. Note however, that although muted, unmodulated PWM action can still be observed at IC107's outputs.

b) Digital audio input section

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference B10

The 256Fs Master Clock, I2S-format digital audio signal, Fs Word Clock and the 64Fs Bit (Serial) Clock, are fed into pins 46, 48, 49 and 50 respectively of IC107. Although the I2S format is 2-channel/1-line (L-ch and R-ch)), only the L-ch signal is present. Pin 33 (BRIDGE) is tied to the +5-volts available at pin 40. This configures IC107 to use its internal channels in bridge mode. Additionally, pin 34 (L/R) is tied to GND so that only the L-ch I2S signal is used.

c) Thermal Protection

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference C9

The TDA7571 contains on-chip circuitry that will shut down the chip if its internal temperature exceeds 160degC. In addition it provides for a heatsink temperature-sensing thermistor and internal/external over-temperature warning outputs at several pins, but these functions are not used in the BBT500H.

d) Clip detection

BBT500H Overall Circuit Diagram 2/2 (PW) Grid Reference C8

Pins 29 and 30 can each be tied to +5V or 0V to indicate up to four levels of signal distortion that are due to clipping. Although this function is not used in the BBT500H, both pins are tied to +5V, and the normally-high logic level at pin 32 (CLIP output) will go low when the distortion level exceeds eight percent.

e) Output stages

BBT500H Overall Circuit Diagram 2/2 (PW) Grid References F8, F11

Before describing the MOSFET output stages and associated components, it may be helpful to see how the PWM waveforms provide the final audio signal. Figure 8 shows the waveforms present at the drain terminals of the bridge-connected MOSFET buffer stages, which are

indicated in the figure as “L-ch” and “R-ch” (not to be confused with the I2S digital audio signal’s left and right channels). Note that *anytime* the amplifier is powered, whether an audio signal is present or not, the 352.8 KHz PWM signal (the “carrier” signal) is always present. This is a logic signal that can only be either high or low, in this case +25volts or -25volts. These voltage levels are of course dependant on the supply voltage available to the MOSFET stages.

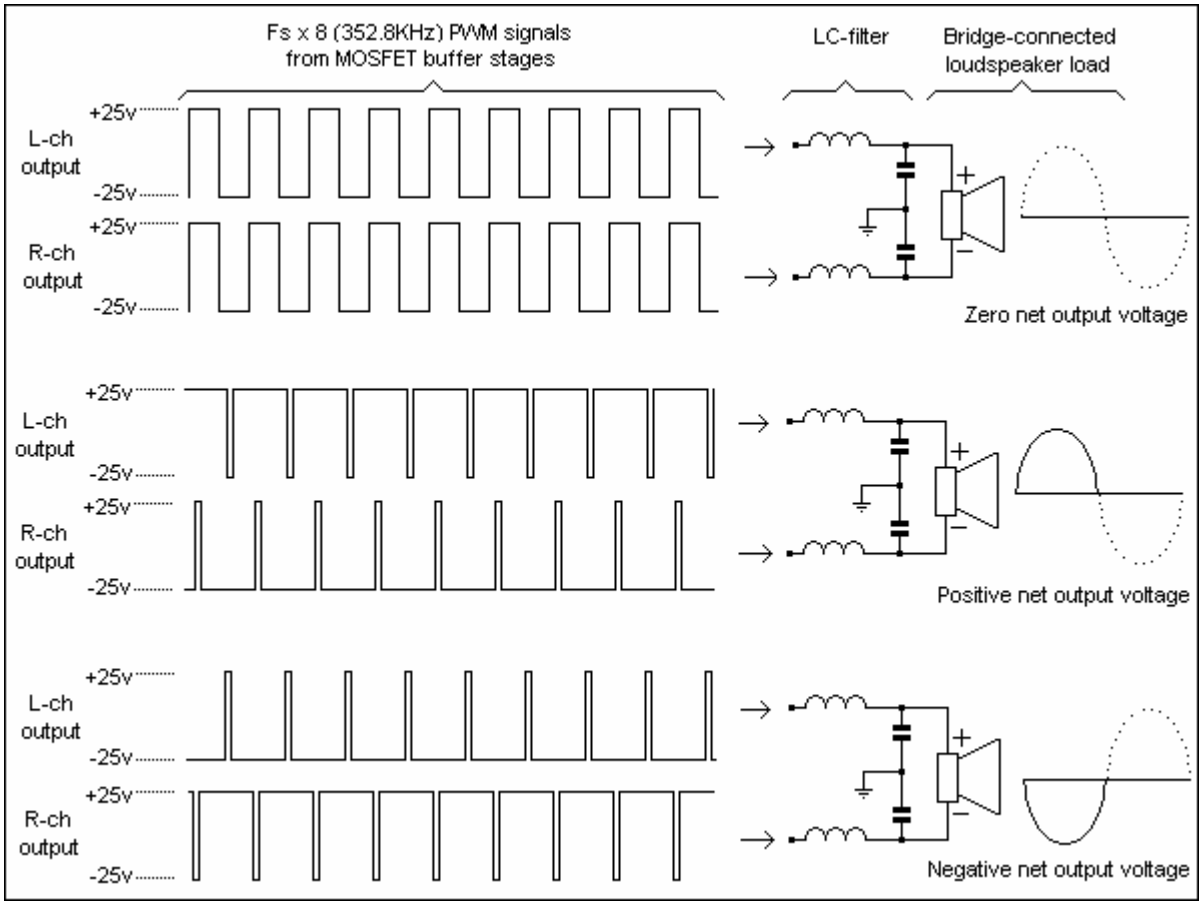


Figure 8. PWM waveforms into bridged loudspeaker load

When the instantaneous value of the audio signal is zero, the L-ch and R-ch waveforms are identical and have a 1:1 mark/space ratio. Even though both outputs are swinging above and below ground, being identical, their *differential* is zero, and so there is no voltage developed across the loudspeaker terminals. Remember, *neither* loudspeaker terminal is connected to ground.

For any positive audio signal value, the time during each PWM cycle that is spent at +25volts increases for the L-ch and decreases for the R-ch. How much of an increase and decrease depends on how positive the audio signal is. The differential is now a positive value, and with the loudspeaker connected with the polarity shown, the net result is an outward displacement of the loudspeaker cone.

Conversely, for any negative audio signal value, the mark/space ratio changes in favour of a differential that is now a negative value, which results is an inward displacement of the

loudspeaker cone. When observed on an oscilloscope, the PWM waveform's pulse width constantly changes in response to the input signal.

The purpose of the LC filter components (L101, L102, C156, and C159) is to remove the 352.8 KHz PWM switching frequency. They average out the mark/space variations so that the loudspeaker "sees" only the demodulated, original audio signal.

In a PWM system, the output voltage is determined by the switching frequency's mark/space ratio together with the voltages that are being switched, in this case the +25V and -25V power supplies. If the power supplies were to change due to line voltage or load current variations, the desired output voltage could also change. For example, if a +25V/-25V power supply was switched with a 1:1 mark/space ratio (a no-signal condition), the net output voltage would be zero. If the supplies were reduced to say, +20V and -20V, the net output would still be zero – so far, so good. But if the supplies were to change asymmetrically to say, +24V and -22V, the net output would be an unwanted value of +1.0V.

To correct this situation, feedback is applied from the MOSFET drains back to IC107 so that it "sees" these errors and takes the necessary corrective action, just like the feedback loop in an analog amplifier does. Specifically, the output PWM signals are fed back via resistors R181/R182 and R165/R164 to the FEEDBACK pins 28 and 57 of IC107. These resistors also set the overall gain to achieve the desired analog output signal amplitude for a given digital input data value.

IC107's output pins drive four groups of three, parallel-connected complementary power MOSFETs, Q120 to Q124 and Q131 in the R-ch, and Q125 to Q130 in the L-ch. The resistors and capacitors around the MOSFET terminals are critical components intended to improve output stage stability and overall distortion characteristics. They reduce the negative effects of stray inductances and capacitances of the PCB/component layout around the high impedance, high-speed MOSFET devices.

The four 0.01ohm resistors R156 to R159 connected between the supply rails and MOSFET source terminals provide load-current sensing and short-circuit protection. Figure 9 shows one of the four current-sense circuits around IC107.

Under fault conditions, the voltage drop across the threshold pins will exceed 100mV, and output drive will be reduced.

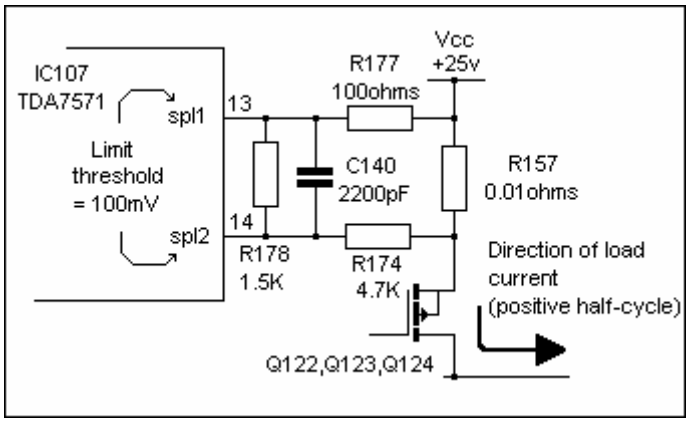


Figure 9. Short-circuit current-sensing circuit

9. Suggested repair procedure

a) Switchmode Power Supply

If there are no SMPS secondary output voltages present at all:

1. Cut or unsolder jumpers J2, J3, J4 and J5. This disconnects the high-current +/-25V supplies from the Digital Power Amplifier.

2. Check resistance values of R123, R124 (6.8-ohm 5W). Replace if open.

3. Check resistance values across Q110, Q111 collector-emitter terminals. Replace if shorted or if resistance has fallen to several ohms.

4. Check resistance values across Q106, Q107, Q108 and Q109 collector-emitter terminals. Replace if shorted or if resistance has fallen to several ohms.

5. Check resistance values of R116, R117. Replace if open or higher than correct value.

6. If fitted, check resistance values of D104, D105. Replace if shorted.

7. If desired, the opportunity can be taken to confirm the existence of switching pulses from IC102 without the risk of damage to high-power components. **With the BBT500H disconnected from the 240VAC mains**, connect an external 15-30VDC voltage supply across capacitor C107 (observe correct polarity). After confirming the output of IC101 (3-terminal regulator) is +15VDC, an oscilloscope can then be used to monitor the waveform produced between IC102 pin 5 (LO) and pin 4 (COM). A 70 KHz rectangular waveform should be observed.

9. If oscillation cannot be observed, check for any shorts in Q101, Q102, Q103, Q104 and Q105. If all these measure OK, replace IC102.

10. If the raw secondary supply voltages are incorrect, replace the switching-transformer T104.

Early production units had 1-ohm fusible resistors fitted to T104's secondary outputs to limit power-on surge current. The Service Manual's Circuit Diagram does not show these resistors, but they were fitted to the PW PCB and were labelled R128, R136, R137, R138 and R139. These were deleted in later production units. If fitted, replace these resistors with jumpers.

b) Digital Power Amplifier

1. Because of the output-stage bridge-mode configuration, any measuring device (oscilloscope, power meter, etc) connected to the SPEAKER jacks must be floating, i.e. it must not be connected to mains earth.

2. Check resistance values across the MOSFET terminals. Because these devices are paralleled, it is necessary to check each one separately. Normally, in circuit, there will be a

minimum resistance of several Kilohms across any two terminals. Replace if shorted or if resistance has fallen to a low value.

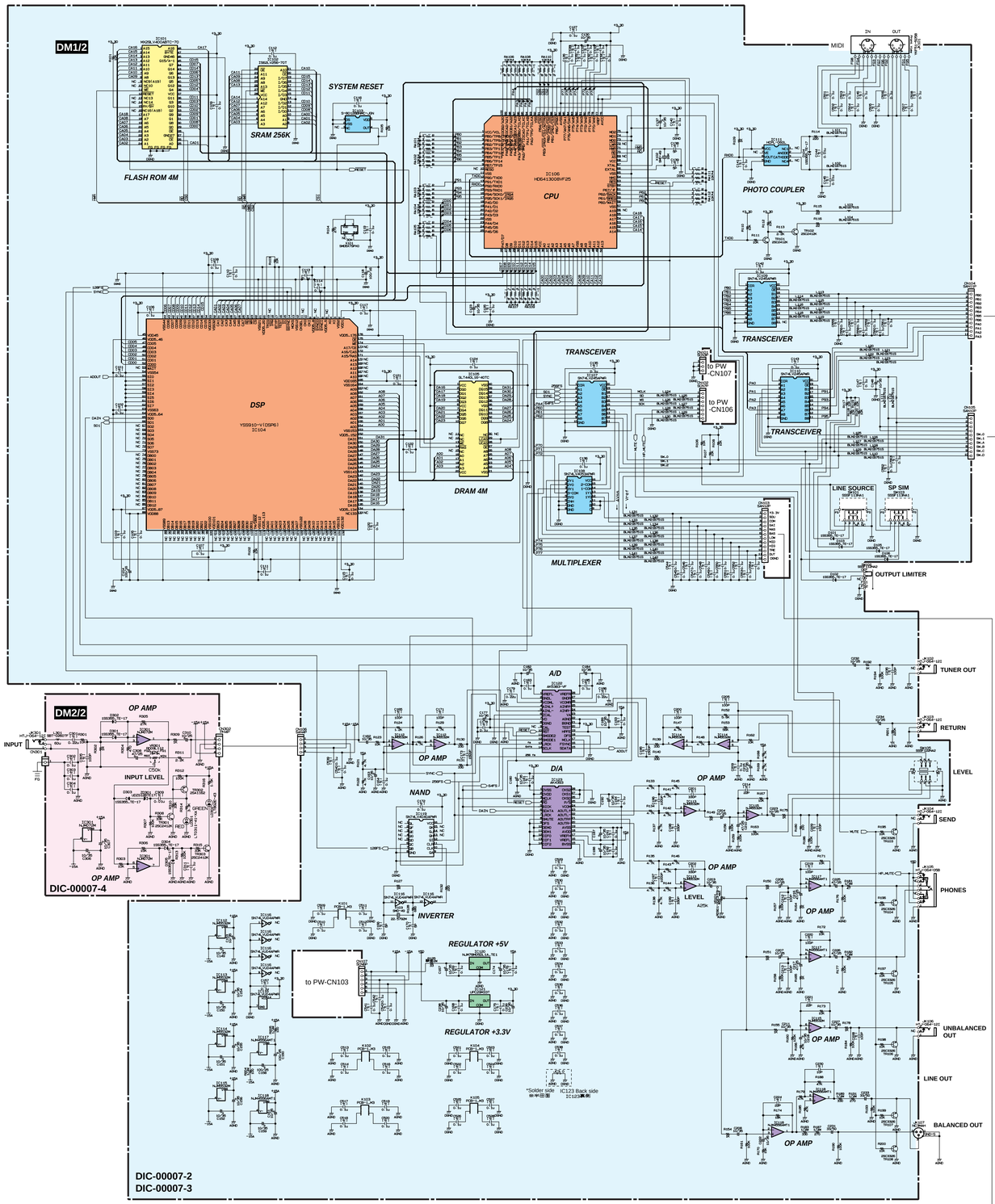
3. Check resistance values of D121, D122, D123 and D124. Replace if shorted.

4. Check resistance values of R156, R157, R158 and R159. It is possible for their resistances to have increased due to a fault condition even though they may still measure only a fraction of an ohm. Since their values determine the current-limiting point of the output stage, suspect them if an otherwise working amplifier is only capable of low volume before limiting and distortion occur.

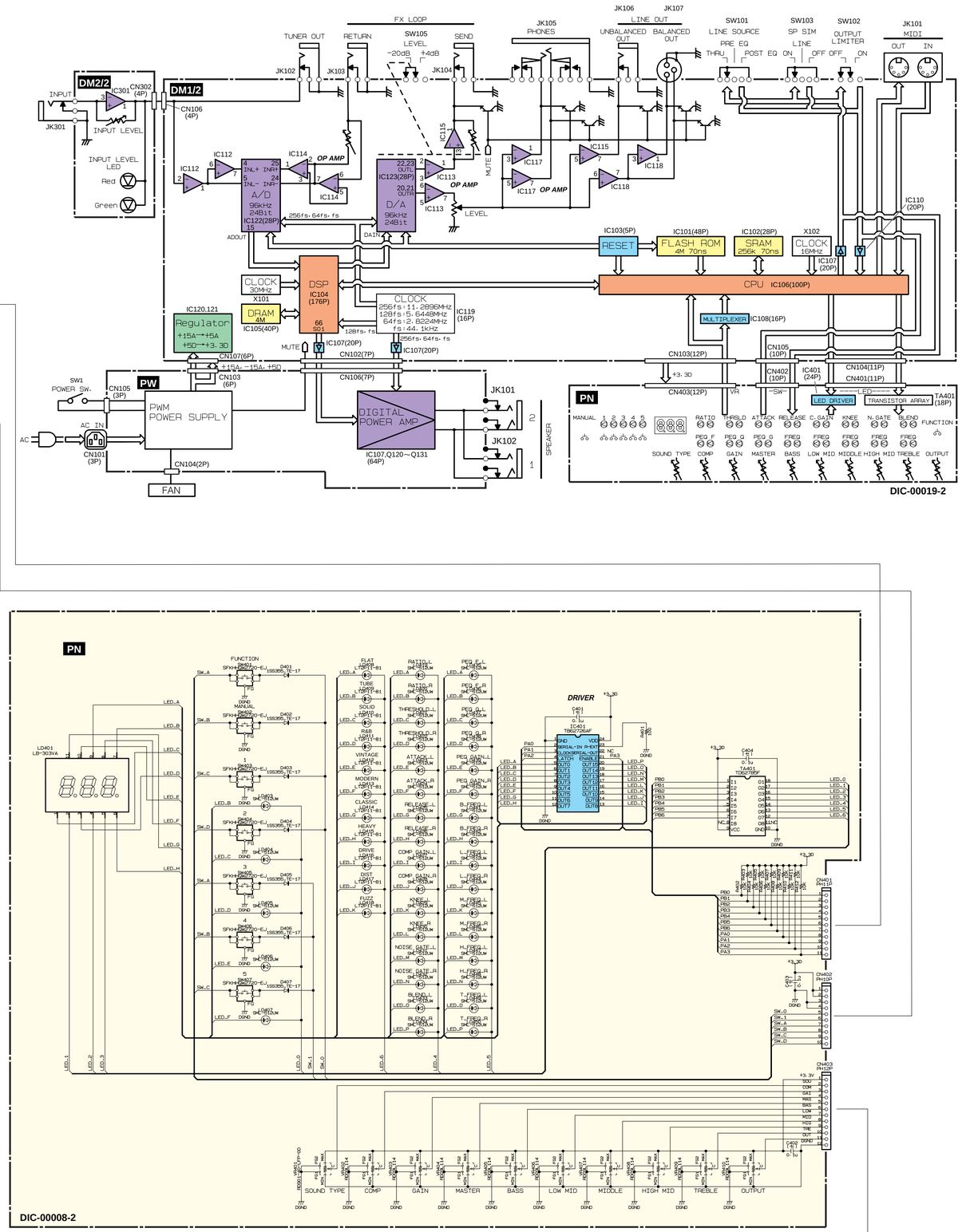
Joseph Pantalleresco
Technical Support Coordinator
Professional and Music Products
Yamaha Music Australia

18th May 2005

■ BBT500H OVERALL CIRCUIT DIAGRAM 1/2 (DM1/2, DM2/2, PN)



■ BBT500H BLOCK DIAGRAM



- •NJM78M05DL1A(TE1) (XS534A00) REGULATOR +5V IC120 — 1: INPUT 2: GND 3: OUTPUT
- •UPC29M33T-E1(XU965A00) REGULATOR +3.3V IC121 — 1: INPUT 2: COMMON 3: OUTPUT

(セ) : Ceramic Capacitor (セラミックコンデンサー)
膜金 : Metal Oxide Film Resistor (酸化金属被膜抵抗)

■ BBT500H OVERALL CIRCUIT DIAGRAM 2/2 (PW)

PW

POWER

CONTROLER

REGULATOR +15V

REGULATOR -15V

REGULATOR +5V

PHOTO COUPLER

SYSTEM RESET

DIGITAL POWER AMP

TDA7571
IC107

to DM-CN107

to DM-CN102

to DM-CN101

to FAN

N.C

SPEAKER
(BRIDGED OUT)

DIC-00009-2 ⚠2
DIC-00009-3 ⚠2

*1

Destination 仕向	T101	T102・T103	T104	F101	C117	J1	J10	CN102	R118・R119	D104・105	T105	C102・C105・C135	R221	R222
J	XY592A00	WE049900 BMH	X5087A00	10A250V	1.2/250V	○	×	○	10Ω (FP)	×	WD511000	1/275V	1MΩ	×
U	XY593A00	WE545400 BMH	X5088A00	10A250V	1.0/250V	○	○	×	10Ω (FP)	×	×	1/275V	1MΩ	1MΩ
H	XY594A00	WE049900 BMH	X5089A00	T6.3A H	1.0/250V	×	×	○	33Ω (FP)	○	VB291500	1/275V	1MΩ	×

○ : install × : not install

FP : Flame Proof Carbon Resistor
(不燃化カーボン抵抗)

Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equal to those originally installed.

⚠印の部品は、安全を維持するために重要な部品です。交換する場合は、安全のため必ず指定の部品をご使用ください。

•NJM7805FA (XJ607A00) REGULATOR +5V IC104	1: OUTPUT 2: COMMON 3: INPUT
•NJM7815FA(XD853A00) REGULATOR +15V IC101,IC103	1: OUTPUT 2: COMMON 3: INPUT
•NJM7915FA(XD854A00) REGULATOR -15V IC105	1: OUTPUT 2: COMMON 3: INPUT
•KCH30A15(WC308400) DIODE STACK 30A 150V D107	
•KRH30A15(WC308500) DIODE STACK 30A 150V D108	
•D25XB60 (VR149900) DIODE STACK 25.0A 600V D117	

*Speaker outputs serves as operation by BTL (BRIDGE) connection. Separate the ground of measuring instruments (oscilloscope, volt meter etc) from the ground of a power supply cord.

*（スピーカ出力はBTL(BRIDGE)動作による出力となっています。測定系（オシロスコープ、電圧計）のGNDは電源コードのGNDと切り離してください。切り離さない状態にて測定すると基板Ass'y上の部品を破壊する場合があります。）

(セ) : Ceramic Capacitor (セラミックコンデンサー)
(マ) : Mylar Capacitor (マイラーコンデンサー)
酸金 : Metal Oxide Film Resistor (酸化金属被膜抵抗)
セメント : Wire Wound Resistor (セメント抵抗)
規格認定コン : Capacitor (規格認定コン)