Yamaha Professional Audio Products

PC9500N Power Amplifier

Circuit explanation

Contents - Page

1. Introduction

The PC9500N is the newest model in Yamaha's long-running series of "PC" Professional Power Amplifiers. It is a 2U high, 2-channel unit rated at 1500-watts continuous per channel into 4-ohms, and 3000-watts continuous into a bridged, 8-ohm load. In order to provide this power capability efficiently, its output stages use Yamaha's established "EEEngine" circuitry, and a lightweight Switch-Mode Power Supply (SMPS) replaces the conventional, heavy power-transformer.

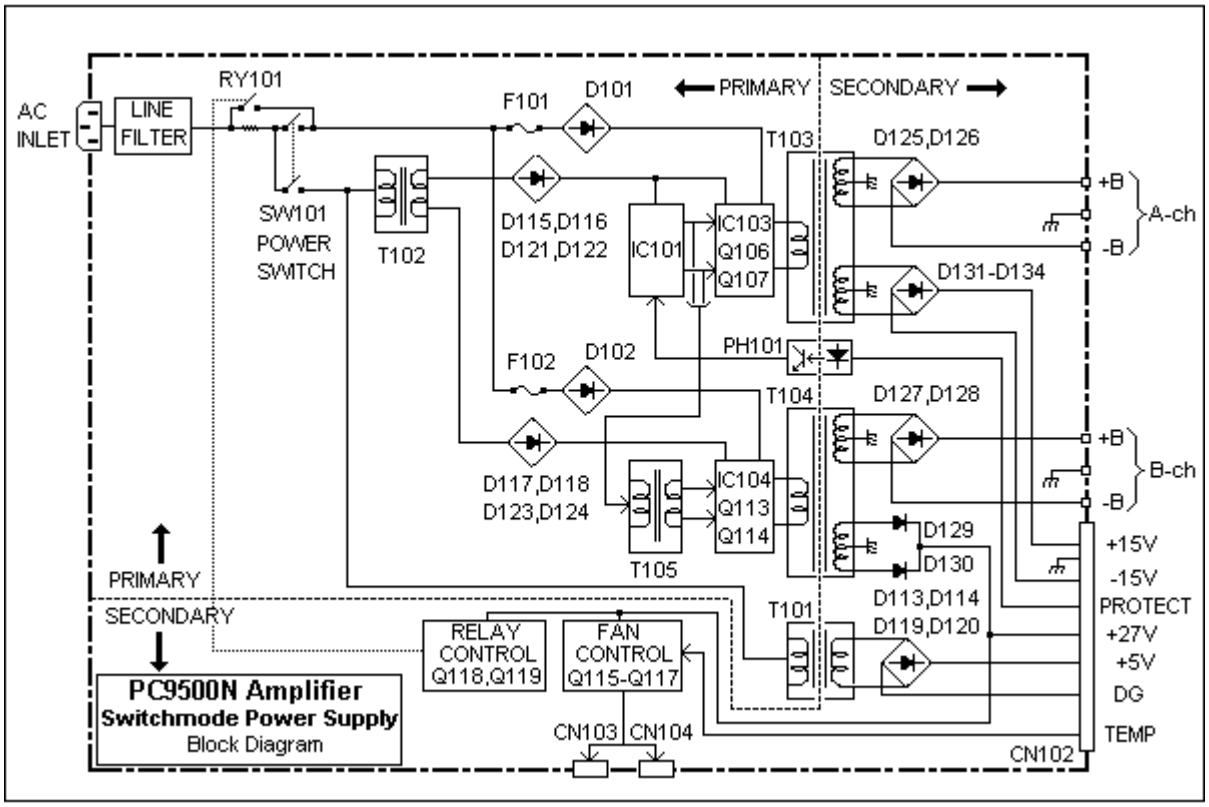
The PC9500N allows remote control and monitoring of its functions when connected as part of a network system using Yamaha's ACU16-C Amp Control Unit and NHB32-C Network Hub/Bridge under PC-computer control.

This Circuit Explanation should be used in conjunction with the PC9500N Service Manual *(Reference 1).*

2. SwitchMode Power Supply (SMPS)

PC9500N Overall Circuit Diagram 7/8 (PS10)

2.1 Block Diagram



The AC mains is fed through a line filter, an "inrush current" relay and a power switch and is directly rectified to provide separate, high-voltage DC rails. These are switched at high frequency through the primary windings of transformers T103 and T104. A 70-Khz oscillator IC101, via driver circuitry, provides switching pulses to both transformers. The low-voltage DC supply for the oscillator and drivers is derived from conventional transformer T102. The

secondary voltages from T103/T104 are rectified and filtered to provide independent, high-voltage +B and -B supplies for the amplifier modules.

Additional supply rails are derived from T103/T104 to power the preamplifier, fan-control, relay-control and protection circuitry. A +5V DC supply for the amplifier's digital control circuitry is derived from conventional transformer T101.

A large proportion of SMPS circuitry is at AC mains potential (shown as "PRIMARY" in the block diagram), which is electrically isolated from the "SECONDARY", chassis-referenced circuitry. Due care must therefore be taken when measuring voltages or waveforms in the primary section.

The entire SMPS consists of a single, large printed circuit board (PCB) mounted centrally on the bottom panel of the chassis.

2.2 Circuit explanation

a) Primary power supplies

Immediately after the POWER switch SW101 is turned "ON", relay RY101 is de-energised, which allows series resistors R129, R172 and thermistor TH101 to limit the initial "inrush" current drawn from the AC mains. After the SMPS starts up, RY101's coil is energised and its contacts short out these components (and one pole of SW101) to provide full power capability.

The arrangement of RY101's contacts (when closed) as a bypass around one pole of SW101 allows them to carry the heavy current that would otherwise flow through SW101 when the amplifier is delivering high power levels. SW101's remaining (unbypassed) pole feeds the AC mains into conventional transformers T101 and T102, which power the low-current sections of the SMPS and amplifier circuitry.

Two independent, high-voltage, DC supply rails (about 340V DC each) are produced directly from the AC mains by diode bridges D101 and D102 and their associated groups of electrolytic capacitors. These supplies are switched at high frequency into transformers T103 and T104 by their respective driver circuitry. Two additional (and again, independent) +15V supplies are produced from T102's dual secondary windings. One of these powers the SMPS's oscillator and A-channel driver and protection circuitry. The other powers the SMPS's B-channel driver and protection circuitry.

Each high-voltage DC supply is paired with and shares a common zero-volt line with its respective +15V supply, but apart from the AC legs of D101 and D102, each pair is electrically isolated from the other.

b) Oscillator

The oscillator contained within the SG3525A PWM Control Circuit IC101 is the source of all switching activity in the SMPS. The SG3525A is normally used in switching-regulator applications where feedback to the device (usually by an opto-coupler or transformer) modulates its waveform pulse-width to regulate the output voltage. In this application however, no feedback is used, and both the frequency and pulse-width of the output waveform are fixed.

A sawtooth waveform is generated across C107 by repetitively charging it with a constant-current, the value of which is set by resistor R103, and rapidly discharging it through resistor R107. A rectangular waveform appears at pin 11 (A output) and pin 14 (B output) of IC101. The operating frequency is approximately 70KHz. Note that the A and B output pins just described should not be confused with the terms “A-channel” and “B-channel”, which refer to the SMPS’s independent output sections. During normal operation, other than during the “dead time”, either A or B is high (+15V) but not together. The “dead time” is determined by the value of R107 and is that short period of time during normal switching operation when neither A nor B is high. The dead time is necessary to avoid the momentary short circuits across the high-voltage supplies that would otherwise occur in the SMPS’s half-bridge output stages during the switchover between A and B.

A high logic level at IC101’s SHUTDOWN pin 10 disables oscillation (and consequently, the generation of all SMPS secondary supply rails). This pin is held low during normal operation.

c) Transformer drivers

The pulses from IC101’s A and B outputs are fed directly to the inputs of IC103 and indirectly to IC104 via coupling transformer T105. Both ICs are IR2110 High/Low Drivers and provide voltage level-shifting and current drive to the half-bridge switching transistors Q106/Q107 (A-channel) and Q113/Q114 (B-channel). The IR2110 device has provision for disabling its outputs, but this is used only on IC104. This will be explained later.

T105 serves two purposes. Firstly, it allows IC101 to drive IC104 while maintaining the isolation between the SMPS’s A-channel and B-channel sections and secondly, it inverts the phases of the switching pulses between the two sections. This cancels out the directions of charging currents into the large electrolytic capacitors and ensures a “quieter” ground.

The switching transistors are Insulated Gate Bipolar Transistors (IGBTs). An IGBT can be regarded as a combination of a MOSFET and a bipolar transistor and is used here because its ON-resistance is much lower than that of the more commonly used MOSFET device.

d) SMPS Protection/Shutdown

- Overcurrent and thermal protection

Various fault conditions within the PC9500N’s circuitry will activate the SMPS’s shutdown function, preventing further damage. The A-channel and B-channel sections of the SMPS each has its own overcurrent and thermal protection circuitry. Fault detection and operation of each circuit is identical except in the method of ultimate shutdown. The A-channel is described here; the B-channel is identical. Note that the thermal protection described here applies only to the SMPS - that for the amplifiers is handled by additional protection circuitry, whose operation will be described later.

Fusible resistors R166 and R167 protect against short-circuits or faults that draw excessive currents from the +/-15V supplies derived from T103’s low-voltage secondary winding. Similarly, R173 protects the +27V supply.

A power amplifier failure that draws excessive current from the +B or -B high-voltage supplies will activate the SMPS’s overcurrent protection circuit consisting of transistors Q101, Q103, Q105, Q109 and Q111. Under normal conditions, Q101 is on and IC101 operates to produce

switching pulses. When an overload occurs, the current reflected into T103's primary winding from the high secondary winding current develops a voltage across resistors R148, R150, R152 and R156 that switches on Q111. This in turn switches on Q109 and Q105, which switches off Q101. This allows R105/R106 to pull the SHUTDOWN pin 10 of IC101 high, stopping its oscillator. In addition to turning on Q105, Q109 also feeds back to the base of Q111, which "latches on" to maintain this shutdown state. All secondary supply rails fall to zero and the amplifier goes into PROTECTION mode. The only way to restore switching operation (assuming a temporary overload condition initiated the shutdown) is to turn off the unit's POWER switch, then turn it back on.

Under some conditions, the value of a sustained, high secondary current draw may not be sufficient to trip the overcurrent protection circuit, but will make Q106/Q107 run hotter than normal. To protect against excessively high device temperatures, a Positive Temperature Coefficient (PTC) thermistor PR101 is mounted on the same heatsink as Q106 and monitors its temperature. When cold, PR101's resistance is low and transistor Q103 is off. If Q106 gets too hot, the subsequent increase in PR101's resistance allows Q103 to turn on and initiate the same shutdown sequence described earlier.

- STANDBY mode

When the S/B (STANDBY) terminal (pin 4) of CN102 goes high (+5V), it illuminates the LED portion of photo-coupler PH101. Consequently, the transistor portion turns on, which switches off Q101, disabling IC101's oscillator and shutting down the SMPS.

Note that the SMPS's response to a STANDBY condition is not latched as it is to an overcurrent-detect condition. This allows the CPU to control the SMPS in response to a remote network command. The CPU shares control of the S/B line with the DC-detection circuit elsewhere in the PC9500N, and *that* circuit contains its own local latch. When the S/B line is low, the SMPS operates; when it is high, the SMPS is shut down.

- Differences in shutdown method between SMPS's A-ch and B-ch sections

Although the end result of fault detection is complete SMPS shutdown, the method used by each SMPS channel to achieve this is different. An over-current, thermal or STANDBY condition in the A-channel directly disables IC101 and stops the switching of both T103's and T104's primaries, which causes all secondary supply rails to fall to zero.

In the B-channel, an over-current or thermal fault condition causes the SD pin 11 of IC104 to be pulled high by R108/R109, which prevents switching of T104's primary. Consequently, its secondary voltages fall to zero, protecting the B-ch power amplifier. The CPU detects the low level on the BD line (CN102 pin 9), goes into STANDBY mode and illuminates the LED portion of PH101, resulting in total SMPS shutdown.

e) Fan Control

PC9500N Overall Circuit Diagram 7/8 (PS10) Grid Reference B10

Two variable-speed fans cool the PC9500N. They are connected in parallel and are driven with a variable voltage that is dependent on the temperatures of the power amplifiers' heatsinks. The current drawn from the FAN terminal (pin 8) of CN102 by the temperature sensing and monitoring circuitry (to be described later), develops a voltage drop across resistor R160. When

the amplifier is cold, there is no voltage drop and the base of transistor Q115 is pulled up to the +27V supply rail. The voltage drops across the base-emitter junctions of Q115 and Darlington-connected Q116 and Q117, and that across the zener diode D141, result in minimal fan drive voltage. As the heatsinks' temperatures increase, Q115's base is brought lower to ground, increasing the fans' drive-voltage and their speed.

f) Inrush-current Relay Control

PC9500N Overall Circuit Diagram 7/8 (PS10) Grid Reference F10

Immediately after the POWER switch SW101 is turned "ON", transistors Q118 and Q119 are off and relay RY101 is de-energised. After about two seconds, capacitor C112 has charged up sufficiently through resistor R157 to forward-bias Q119 through diode D145. This turns on current-source Q118, which energises RY101.

3. Remaining PC9500N circuitry

3.1 Signal Limiter

PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 3/5) Grid Reference C7, C11, O2, L2

A Signal Limiter circuit on each channel reduces the input level to its power amplifier when the output signal to the loudspeakers is either clipped (called "V-limiting"), or is being fed into a load impedance that is too low (called "I-limiting"). The V-limiting action is independent between channels but I-limiting occurs simultaneously on both channels when either channel delivers excessive output current.

The operation of the A-ch Limiter is described; the B-ch Limiter's operation is identical.

The Limiter element consists of the light-dependant-resistor (LDR) portion of photocell PH401, which together with series resistor R469 form a potential divider across the power amplifier input. The signal level through the Limiter varies depending on the resistance of the LDR. Under normal conditions the LDR's resistance is high and the signal passes unattenuated through the limiter and into the power amplifier.

Limiter control is by circuitry around transistors Q401 – Q405. Under normal conditions, these are all off, the LED portion of photocell PH401 is unilluminated and minimal signal path attenuation occurs - the Limiter is off. When the power amplifier clips, Q404 turns on and +15V appears at its collector. Current-sink Q403 charges capacitor C405, which turns on Q402 and illuminates the photocell LED to turn the Limiter on (V-limiting).

Q404's collector also illuminates the front-panel CLIP segment of the meter LED array via Q601 and Q602 (PC9500N Overall Circuit Diagram 2/8 (IN 1/5) Grid Reference O7). Q405 provides an indication to the CPU that clipping has occurred.

When excessive load current is detected in either of the power amplifiers, the "ICOMP" line pulls the bases of Q401 and B-ch's Q406 to 0V, which illuminates both photocell LEDs simultaneously (I-limiting).

3.2 Fault Protection

a) DC voltage

PC9500N Overall Circuit Diagram 2/8 (IN 1/5) Grid Reference D10, J10

Due to their very high power capability, the PC9500N's power amplifier output stages are connected directly to the loudspeaker terminals, not through relay contacts, as is common practice. As this offers no protection to the loudspeakers in the event of a DC voltage appearing at the amplifier outputs, the SMPS itself is called upon to switch off the high-voltage supply rails. When this occurs, it will remain in this condition until the POWER switch is turned OFF, then turned ON again.

The signals at the PC9500N's loudspeaker terminals are lowpass filtered and fed to the bases of transistors Q630/Q631 (A-ch) and Q626/Q629 (B-ch). Q631 and Q629 detect positive DC voltages; Q630 and Q636 together with Q625 detect negative voltages.

Q620 and Q624 form a latch which, once triggered by the detection of DC, will remain in the latched state even if the trigger is removed. Normally, Q620's collector is at 0V because neither it nor Q624 is on. When DC is detected, Q620's base is pulled low and both transistors latch on due to the positive feedback between them. With Q620's collector now at +5V, the SMPS's STANDBY opto-coupler is turned on, which switches off all supply rails.

Q620 also turns on Q612, which provides A-ch and B-ch signal MUTING. Q612 also turns on Q608, which illuminates the front-panel PROTECT LED and sets the CPU's PROTECT STATUS line.

b) Temperature

PC9500N Overall Circuit Diagram 6/8 (PA) Grid Reference O8
PC9500N Overall Circuit Diagram 2/8 (IN 1/5) Grid Reference H6

An LM35DT Temperature Sensor IC (IC201) measures the heatsink temperature of each PA circuit board and provides a voltage output of 10 millivolts per degree Celsius. Opamps IC505/1 (A-ch) and IC505/2 (B-ch) each compares the voltage at its non-inverting input (the sensor's output voltage) with the reference voltage at its inverting input. This reference is derived from resistors R629 and R630 and represents a temperature of approximately 45 degrees C.

When both heatsinks are below 45 degrees C, no collector currents flow in Q614 and Q615 because IC505's outputs are at –15V. Diodes D605 and D606 prevent damage to the transistors' base-emitter junctions in this state. As described earlier, the current drawn from the FAN terminal of CN102 on the SMPS PCB determines fan speed. When the temperature of either heatsink exceeds 45 degrees C, the relevant opamp's output changes to equalise the voltages at its inputs and biases on its transistor, varying its collector current and hence, fan speed.

At a heatsink temperature of approximately 85 degrees C (as set by resistors R637 and R638), transistor Q618 turns on to illuminate the front-panel TEMP LED.

The differential pair Q621/Q622 compares the buffered sensor output voltage with the voltage at the junction of R660 and R661. Below 90 degrees C, the lack of Q621 collector-current keeps transistor Q619 off. Above 90 degrees C, Q621, Q619 and transistor Q611 turn on to activate

MUTING, the PROTECT LED and the CPU PROTECT STATUS line. Q619 also turns on transistor Q623 to provide hysteresis around the threshold temperature.

c) Power-on/off detection

PC9500N Overall Circuit Diagram 2/8 (IN 1/5) Grid Reference O10

When the POWER switch is turned ON, the digital +5V supply is present almost immediately. Capacitor C601 is initially discharged and remains so until the +15V supply has been generated by the SMPS. Until then, transistors Q603 and Q610 are on. This activates MUTING, illuminates the PROTECT LED via Q608 and sets the CPU PROTECT STATUS line. Additionally, the lack of voltage on the BD line from the SMPS turns on Q637 and Q607. Q637 (and Q603) turn on Q634, which turns off Q635 and Q636.

With Q636 off, the PC9500N's amplifier output stages are biased so that no idling current flows (Class B operation). This is achieved by the use of normally-closed relay contacts (RY201) connected across the current-limiting transistors (Q217 and Q218) in each amplifier output stage.

With Q607 on, Q605 pulls the CPU AMP STATUS line to 0V and Q609 (BD PROT) activates MUTING, etc just like Q610.

As the SMPS's supply rails develop, C601 is allowed to charge through resistor R603 (the C601/R603 time constant sets the POWER-ON PROTECTION delay time) until Q603 turns off. Similarly, the presence of voltage on the BD line turns Q637, Q607 and Q634 off, and Q635 and Q636 on. The end result is that MUTING, CPU PROTECT STATUS and the PROTECT LED are turned off, the CPU AMP STATUS line goes to +5V and the amplifier output stages revert to normal Class AB operation.

3.3 Remote Control and Monitoring

a) Overall

PC9500N Overall Circuit Diagram 5/8 (IN 4/5) Grid Reference H5
PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 3/5) Grid Reference D2

Microcontroller IC801 (CPU) communicates serially with external devices connected to the rear-panel DATA port connectors, to allow remote control and monitoring of the PC9500N's functions. When the PC9500N is being remotely controlled, pin 5 of the CPU goes low, turning on transistor Q417, which illuminates the front-panel REMOTE LED.

- Items that can be monitored

Unit ID	0 – 31
Amp Type	2ch, 4ch, 6ch, 8ch
Model ID	PC9500N or PC4800N
Mode	Stereo / Bridge / Parallel
Input Level	Amplifier input signal level
Output Level	Power output in watts / volts
Output Clip	When limiter is activated

Impedance	Impedance / Warning
Protection	Protection circuit status
Temperature	Heatsink temperature warning

- Items that can be controlled

Power	Universal control of all power amplifier's ON / Standby control
Attenuator	63 step attenuation of input signal level
Remote ON / OFF	Attenuator remote ON / OFF
Phase	Normal / Reverse
Mute	On / Off

b) Unit ID

PC9500N Overall Circuit Diagram 5/8 (IN 4/5) Grid Reference F7

Dipswitch SW801 sets the amplifier's ID in a network, and where necessary, terminates the RS-485 Data Port connectors JK801 and JK802. The dipswitch's state appears at CPU pins 56-60.

c) Amp Type / Model ID

PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 5/5) Grid Reference D11

An array of resistors/jumpers R470-R483 sets the logic levels at CPU pins 85-89,102 and 104. The model "PC9500N" is identified when all of these pins are set to logic 0 (0V).

d) Mode

PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 5/5) Grid Reference P2, P8, E2

Resistors R401-R404 form a tapped voltage divider across the +15V supply. One of the sections of the 3-position rear-panel mounted MODE switch feeds the selected tap voltage to transistors Q414 and Q415, which in turn determine the logic states of CPU pins 53 and 52 respectively.

e) Input Level, Output Level, Impedance

PC9500N Overall Circuit Diagram 4/8 (IN 1/5)
PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN3/5, IN5/5) Grid Reference H9
PC9500N Overall Circuit Diagram 2/8 (IN 1/5) Grid Reference M3, F2, F4

Op-amps IC901 to IC906 are configured as conventional, precision full-wave rectifiers and averaging filters, which convert AC signals into corresponding DC voltages for use by the CPU. The function of each IC is as follows –

Opamp IC #	Function	Source	Destination CPU pin #
IC901	A-ch preamp signal level	Preamp differential input stages IC401/1 & IC401/2 via buffers IC407/1 & IC407/2	91
IC902	B-ch preamp signal level		92

IC903	A-ch speaker voltage level	Resistive dividers across speaker terminals via buffers IC601/1 & IC601/1	95
IC904	B-ch speaker voltage level		96
IC905	A-ch speaker current level	Coils L601 – L604 in speaker lines via conditioning amplifiers IC602 & IC603	93
IC906	B-ch speaker current level		98

The measurement of input and output voltage levels by the CPU is straightforward. The measurement of output current allows it to calculate load impedance and output power. Coils L601 and L602 are conventional Zobel network components normally involved with ensuring amplifier stability. Mounted concentrically within these are L603 and L604 respectively. The speaker load currents flowing through L601/L602 induce proportional voltages in L603/L604, which are amplified and filtered by IC602/ IC603 and fed to the CPU.

f) Output Clip, Protection, Temperature

PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 5/5) Grid Reference N3, K3
PC9500N Overall Circuit Diagram 2/8 (IN 1/5) Grid Reference L10, D8

The operation of these circuits was described in detail earlier. Transistors Q405/Q410 provide A-ch/B-ch CLIP and limiter indication to CPU pins 70 and 69. Q608 provides PROTECT STATUS to CPU pin 66. IC606/1 and IC606/2 amplify the DC voltage outputs from the heatsink temperature sensor ICs by a factor of four and feed CPU analog input pins 94 and 99.

g) Power/Standby Control

PC9500N Overall Circuit Diagram 2/8 (IN 1/5) Grid Reference G10

When the PC9500N receives a STANDBY message over the network, pin 4 of the CPU pulls the bases of transistors Q616 and Q617 to 0V, turning them on. Q617 acts directly on the SMPS, shutting it down (except the +5V digital supply). Q616 turns on Q613 (PROT MASK), which prevents other sections of the protection circuitry from responding to what appears to be a fault condition. Q616 also illuminates the red portion of the front-panel bi-colour POWER/STANDBY LED, changing its colour from green to orange.

h) Attenuator, remote ON/OFF

PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 5/5) Grid Reference F10

The signal levels through the PC9500N are controlled by its front-panel LEVEL potentiometers and by remote control. The buffered L-ch and R-ch signals from the wipers of the LEVEL potentiometers are sent directly to the normally-closed contacts of relay RY403, and indirectly via IC408 - a TC9413AP Stereo Digitally Controlled Attenuator (DCA) - to RY403's normally-open contacts. When in REMOTE mode, Q417 and Q416 are on, which energises relay RY403 to select the DCA signal path. Clock, serial data and strobe signals sent to the DCA from CPU pins 16, 17 and 18 respectively, set each channel's DCA attenuation factor independently. Note that when in REMOTE mode, the LEVEL potentiometer and the DCA together determine the total channel attenuation.

i) Phase

PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 5/5) Grid Reference I6, I11

Normal or Reverse signal phase can be set independently between channels and is determined by the logic levels at CPU pin 6 (A-ch) and pin 7 (B-ch). To select Reverse phase, a low logic level on the relevant pin switches on transistors Q422/Q419 (A-ch) or Q423/421 (B-ch). Relays RY401 (A-ch) or RY402 (B-ch) are energised and the inverted outputs from opamps IC402 (A-ch)/IC403 (B-ch) are selected.

j) Mute

PC9500N Overall Circuit Diagram 1/8 (IN 1/5, IN 3/5, IN 3/5) Grid Reference B7, B11, I2

The CPU can mute each channel individually by applying a low logic level from its pin 10 (A-ch) or pin 11 (B-ch) to the base of Q412 or Q413 respectively. These in turn drive Q420 or Q418, which are connected as muting transistors across the inputs of the power amplifiers.

Both channels are muted simultaneously when Q411's base (the /MUTE line) is taken to a low logic level by any of several transistors that each respond to a unique fault condition. This was explained earlier in the section on "Protection".

3.4 Signal Metering

PC9500N Overall Circuit Diagram 3/8 (IN 2/5)

A 10-segment LED array provides output level metering for each channel. The operation of the A-channel meter circuit is described here; B-channel operation is identical.

One of the LEDs in array LD701 is a CLIP indicator and its operation was described earlier as part of the Limiter circuitry. The remaining nine LEDs are connected in a series chain between the collector of transistor Q711 and ground. Q711 supplies a constant current of about 7mA. The collectors of transistors Q701-Q708 and Q710 are connected to the LED junctions and their bases are driven by the outputs of LED driver IC701. Inside this IC are nine comparators, each of which has its inverting input connected to an internal resistive voltage divider. The comparators' non-inverting inputs are fed with an attenuated and buffered version of the speaker output signal.

Under no-signal conditions, the comparators' outputs are all off, which allows resistors R701-R708 and R710 to turn on Q701-Q708 and Q710, shorting out all the LEDs. As the signal's amplitude increases, Q710 turns off, followed by Q708, then Q707 and so on. As each transistor turns off, it releases the short-circuit across its corresponding LED, allowing current to flow through the LED.

Transistor Q709 regulates the +27V supply down to +13V for use by IC701/IC702.

3.5 Power Amplifiers

PC9500N Overall Circuit Diagram 6/8 (PA)

Apart from the EEEngine circuitry, the PC9500N's power amplifier stages are of conventional design, each using a differential input stage (Q202,Q205), current-mirror (Q201,Q206), constant-current sources (Q203,Q208), voltage amplifier (Q207), cascode followers (Q209,Q211) and triple-complementary Class AB output stage (Q219,Q220,Q233,Q234,Q235N-Q241N,Q235P-Q236P). *Reference 2* explains the operation of a typical discrete-component power amplifier.

The EEEngine circuitry uses a combination of switching and linear techniques to adjust the output stage supply voltage to the minimum required to accommodate the amplifier output signal, significantly reducing heat dissipation in the process. Its method of operation is similar to that used in other Yamaha amplifiers, and is described in *Reference 3*.

The PC9500N uses MOSFETs in its switching section rather than bipolar transistors, which are used in other Yamaha EEEngine amplifiers. Note that only N-channel MOSFETS are used, rather than the expected combination of complementary N-channel and P-channel devices. This necessitates an additional inverting stage Q225 in the negative supply switching section.

Reference 1. Yamaha Professional Power Amplifiers PC9500N/PC4800N Service Manual. Document number PA011652 Electronic Products Service Department Yamaha Corporation Japan Sept 2002

Reference 2. Amplifier Servicing Guide. J. Pantalleresco, Service Department - Yamaha Music Australia 28/07/2000

Reference 3. Yamaha EEEngine and HED. J. Pantalleresco, Service Department - Yamaha Music Australia 19/05/2000

Joseph Pantalleresco
Technical Support Co-ordinator
Professional and Music Products
Yamaha Music Australia

20 November 2002