"Impact of SRAM Cell Topology on Design Metrics: A Unified Evaluation of 6T, 7T, 8T, and 9T Cells at 90nm Technology Node"

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Abstract- This paper presents a comparative study of 6T, 7T, 8T, and 9T SRAM cell topologies based on power consumption, static noise margin, and access delay, using Cadence Virtuoso simulations at 90nm technology. The results show that the 8T cell had the highest read SNM, improving stability by 95.71% compared to the 6T cell and had highest write SNM as well. The 7T cell achieved the lowest read power consumption, while 6t had the lowest write power. Regarding speed, the 6T cell had the shortest read delay, while the 7T cell offered the shortest write delay, reducing the write delay by 32.90% compared to the 6T cell. These evaluations highlight the distinct strengths and trade-offs associated with each topology, from the power efficiency of conventional 6T ,7T cells to the enhanced stability and read robustness offered by 8T and 9T topologies.

Keywords: Static noise margin, Power consumption, Delay, SRAM cell.

I. Introduction

As CMOS technology is rapidly advancing and continuously scaling predicted by Moore's Law, the design of high-performance, low-power SRAM cells is crucial for modern system-on-chip (SoC) and processor applications. SRAMs serve as essential cache memory components, providing fast and reliable data access to keep up with processor speeds. Conventional 6-transistor (6T) SRAM cells have long been used due to their simplicity and area efficiency. However, challenges such as power dissipation, read/write stability, and access delays have driven the exploration of alternative cell topologies like 7T, 8T, and 9T designs.

As device dimensions shrink, factors such as process variation and transistor aging impact SRAM performance and reliability even more. Unlike dynamic RAM (DRAM), which is volatile and requires periodic refreshing and consumes more power, SRAM offers static data retention with faster access times but often at the expense of increased power and area. Enhanced topologies aim to balance these trade-offs by improving static noise margins, reducing power consumption, and minimizing read/write delays.

This work provides a comparative analysis of 6T, 7T, 8T, and 9T SRAM cells focused on key metrics: power consumption during read and write operations, static noise margins (SNM), and access delays. The study is performed using Cadence Virtuoso simulations. Understanding these trade-offs is essential for selecting the appropriate SRAM topology required for specific applications in low-power and high-speed designs.

II. SRAM Topologies

A. 6T SRAM

Figure [1.1] shows a 6T SRAM cell consisting of six transistors—four in a pair of cross-coupled inverters to store a bit, and two NMOS access transistors that connect this storage to the bit lines (BL and BL_bar) when the word line (WL) is active which is connected to the gate terminals of these access NMOSs. It has smallest area among all of them which makes it ideal for high density arrays and it also consumed less power during read and write operations.

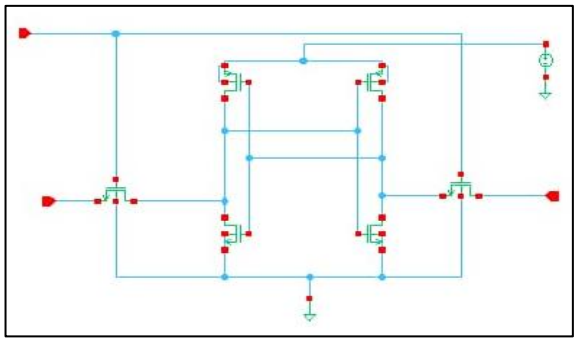

Fig 1.1

B. 7T SRAM

Figure [1.2] shows a 7T SRAM cell; one more transistor compared to 6t SRAM cell which is connected between two inverters for controlling the feedback. It lowers read disturbances which means stored data is less likely to get disturbed during read operation.

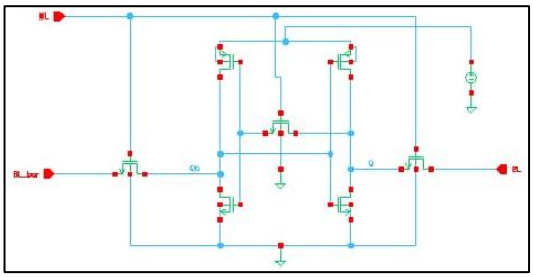

Fig 1.2

C. 8T SRAM

Figure [1.3] shows a 8T SRAM cell. It adds a complete separate read circuitry to decouple read and write operations which results in significant rise in read stability which is evident from tables given below. That additional circuitry is controlled by RWL, RBL lines.[1]

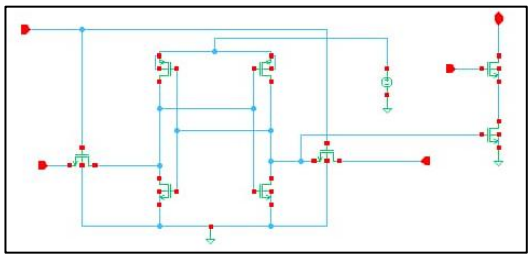

Fig 1.3

D. 9T SRAM

Figure [1.4] shows a 9T SRAM cell. It further decouples the read and write paths.[15][16] It has large area compared to 6T,7T SRAM cells but it provides significantly high write, read static noise margins.

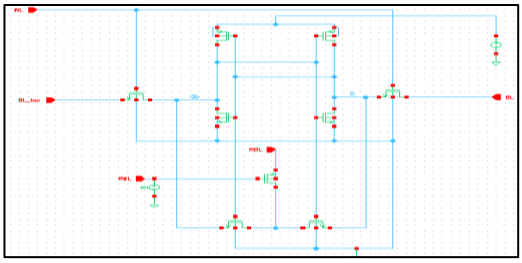

Fig 1.4

III. GRAPHS & RESULTS

A. WAVEFORM

The method of how read and write operations take place is given below.

Read operation: Pre-charge method has been used to verify read operation. The pre-charge circuit consists of two PMOSs whole one ends are connected to bit bines BL, BL_bar respectively and other ends are connected to Vdd supply.

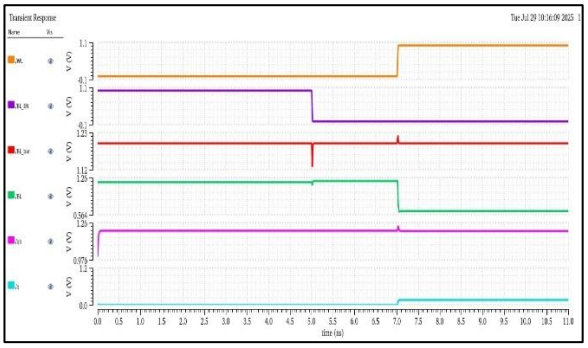

Fig 1.5

They are controlled by BL_EN pin. When BL_EN is '0', then both bit lines are charged to Vdd, then BL_EN is set to '1'. Now access transistors are enabled using the word line (WL), the corresponding stored value either 'q' or 'qb' which was '0' causes its bit line to drop some, means if 'q' was '0' then BL will drop and vice versa.

In the waveform shown in figure [], clearly BL is dropped because 'q' was '0' which was taken explicitly just to verify. Usually the stored values are unknown and can be detected using this method.

Write operation

Word line (WL) is made '1' which connects stored data to bit lines using access transistors. Now Bl, BL_bar are given complementary values using external drivers. To write '1', BL is set to '1' and BL_bar is set to '0'.

Driver circuit: It is made of two transmission gates. One input pin is used to control these transmission gates and other input pin is used to give values to these gates. These gates drive the BL, BL_bar with complemented values which are then written in the storage nodes, replacing the previously stored values.

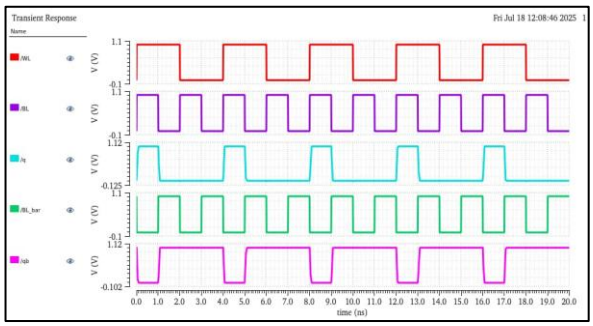

Fig 1.6

B. SNM

Read SNM:

During read, one connection between cross coupled inverters is broken. Input is given to 'q' of one inverter and corresponding 'qb' is measured for other inverter. Similarly, it is done for other inverter then both graphs are superimposed on each other. The side of maximum square that can be inserted between these two curves gives the read SNM as shown in figure [1.7].

Write SNM

Both bit lines are pre charged to Vdd. Then driver circuit constantly pull down one of the bit lines while word line is kept low. The point where stored value flips gives the write SNM value. [12][13][14].

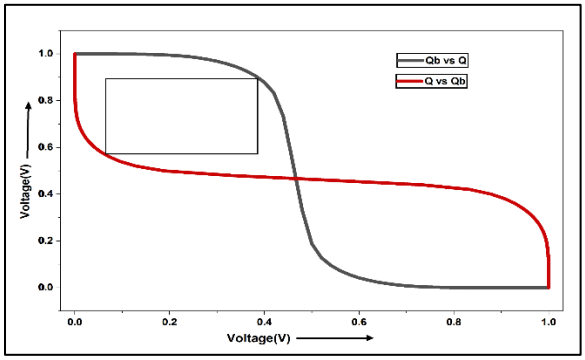

Fig 1.7

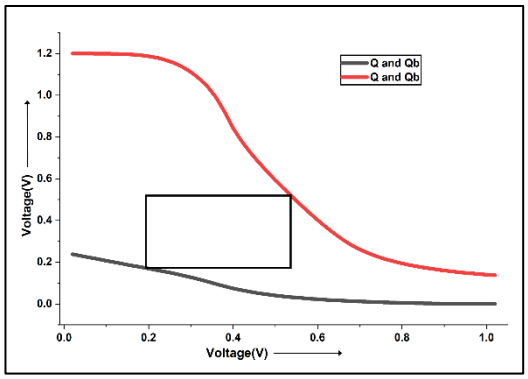

Fig 1.8

C. *TABLES*

The 8T cell leads in read stability with a read SNM of 319 mV, 95.71% higher than 6T, 108.5% higher than 7T, and 25.1% higher than 9T. Also for write SNM, 8T is the best at 340 mV, 1.5% higher than 6T, 18.4% higher than 7T, and 20.1% higher than 9T, showing stronger write robustness. It is because of the separate circuitry that it has for read operation which decouples read and write operation that gives it high read, write stability.

TABLE 1.1 SNM

SRAM topologies	WSNM in mV	RSNM in mV
6T SRAM	335	163
7T SRAM	228	153
8T SRAM	340	319
9T SRAM	283	255

6T has the lowest read power at 11.08 µW, which is 1.6% less than 7T, 30.8% less than 8T, and 54.9% less than 9T, making it the most efficient during reads. The 6T cell also consumes write power 43.31 µW—26.61% less than 7T, 42.49% less than 8T, and 47.49% less than 9T—indicating superior write power efficiency. It is because of the simple circuitry of 6T SRAM cell that it consumes less power as compared to other topologies.

TABLE 1.2 POWER

SRAM topologies	Write Power in µW	Read Power in µW
6T SRAM	45.31	11.08
7T SRAM	61.74	11.26
8T SRAM	78.79	16.01
9T SRAM	86.3	24.59

Delay is the time difference between input value reaching 50% of its maximum value to the output reaching 50% of its maximum value.6T SRAM has the fastest read delay at 12.53 ps—23.6% faster than 7T, 99.7% faster than 8T, and 126.2% faster than 9T. When it comes to write speed, 7T cell has a write delay of 20.6 ps, which is 32.90% faster than 6T, 44.6% faster than 8T, and 41.97% faster than 9T.

TABLE 1.3 DELAY

SRAM topologies	Write Delay in ps	Read Delay in ps
6T SRAM	30.7	12.53
7T SRAM	20.6	16.4
8T SRAM	37.2	24.9
9T SRAM	35.5	28.3

IV. CONCLUSION

This study presents a detailed evaluation of 6T, 7T, 8T, and 9T SRAM cell architectures, considering parameters such as read/write power, static noise margins (SNM), and access delays. The 6T cell demonstrates clear superiority in both read and write power efficiency—achieving the lowest consumption among the four topologies—attributable to its minimal and simple circuit design. Additionally, 6T offers the fastest read access, underscoring its suitability for energy- and performance-critical cache applications. In contrast, the 8T cell achieves the highest read and write SNM due to its separated read/write pathways, providing exceptional robustness against noise and process variations, which is vital for reliable memory designs. The 7T cell distinguishes itself with the fastest write speed, making it attractive for rapid data update scenarios. Meanwhile, the 9T and 8T topologies provide enhanced stability at the expense of increased area and power. These findings clearly indicate that the selection of SRAM cell topology must be tailored to specific application priorities: 6T for ultra-low power and speed, 8T for stability. Ultimately, the results establish a clear benchmark for selecting memory cell designs based on targeted power, speed, and reliability trade-offs.

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