Digital Design and Computer Organization Laboratory

UE21CS251A

3rd Semester, Academic Year 2022-23

Date:

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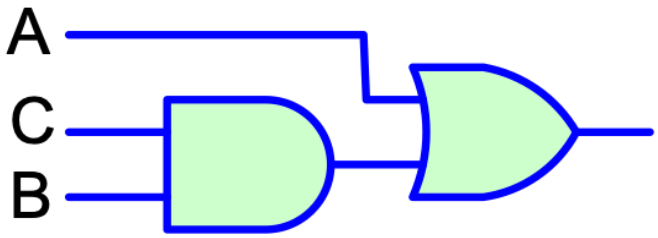
Week#____2_____ Program Number: ____1___

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A GIVEN LOGIC CIRCUIT. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

```
module simple_circuit(A,B,C,Y);
input A,B,C;
output Y;
wire X;
and G1(X,B,C);
or G2(Y,A,X);
endmodule
```



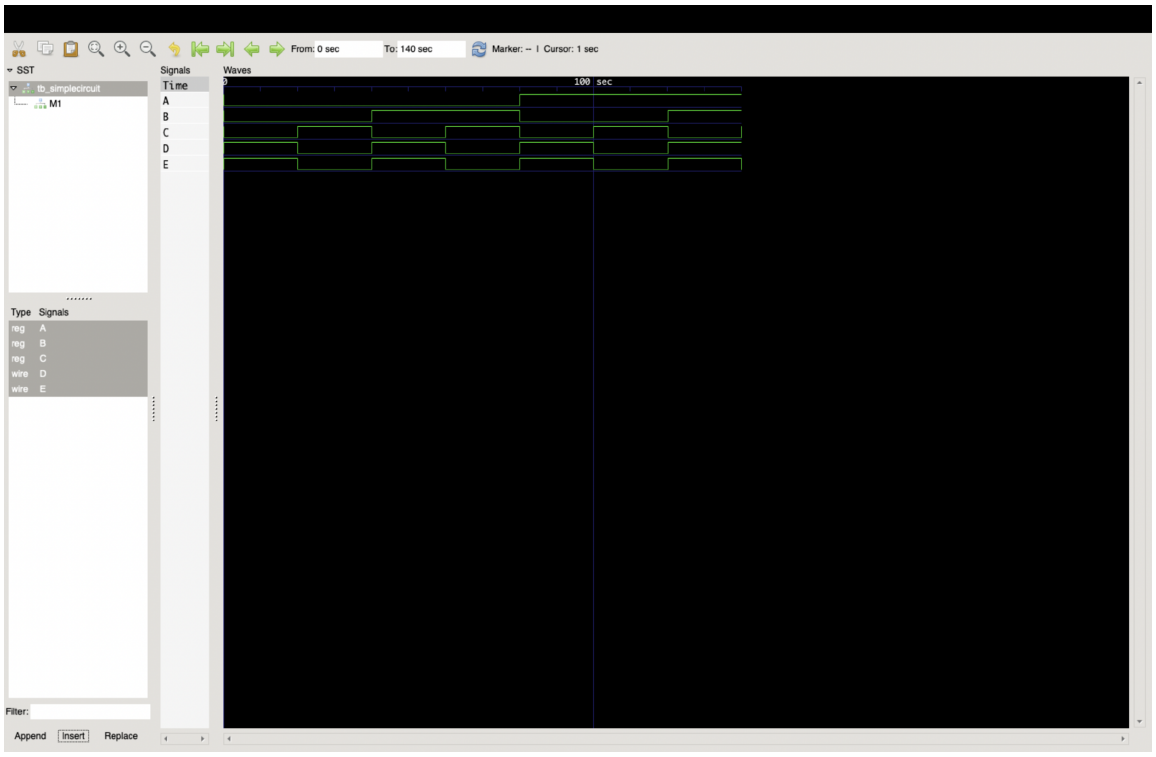
I. Verilog Code Screenshot

II. Verilog VVP Output Screen Shot

```
Last login: Mon Aug 22 16:50:11 on console
abhi@Abhisheks-MacBook-Pro ~ % cd desktop
abhi@Abhisheks-MacBook-Pro desktop % cd ddcolab
abhi@Abhisheks-MacBook-Pro ddcolab % iverilog -o tb_circuit1.v circuit1.v


abhi@Abhisheks-MacBook-Pro ddcolab % vvp test


VCD info: dumpfile simple.vcd opened for output.
                0A=0 B=0 C=0 D=1 F=1
```



III. GTKWAVE Screenshot

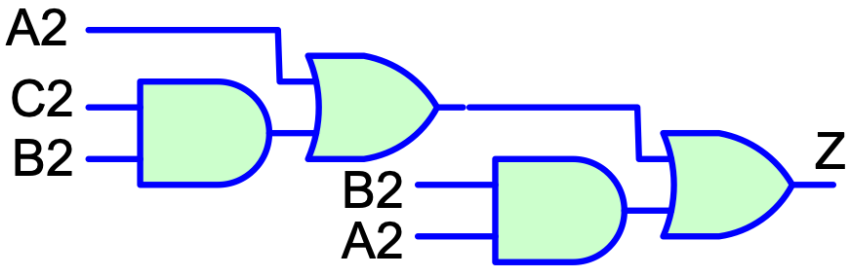
IV. Output Table to be completed and included

A	B	C	D	E
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

Week#____1_____ Program Number: ____2___

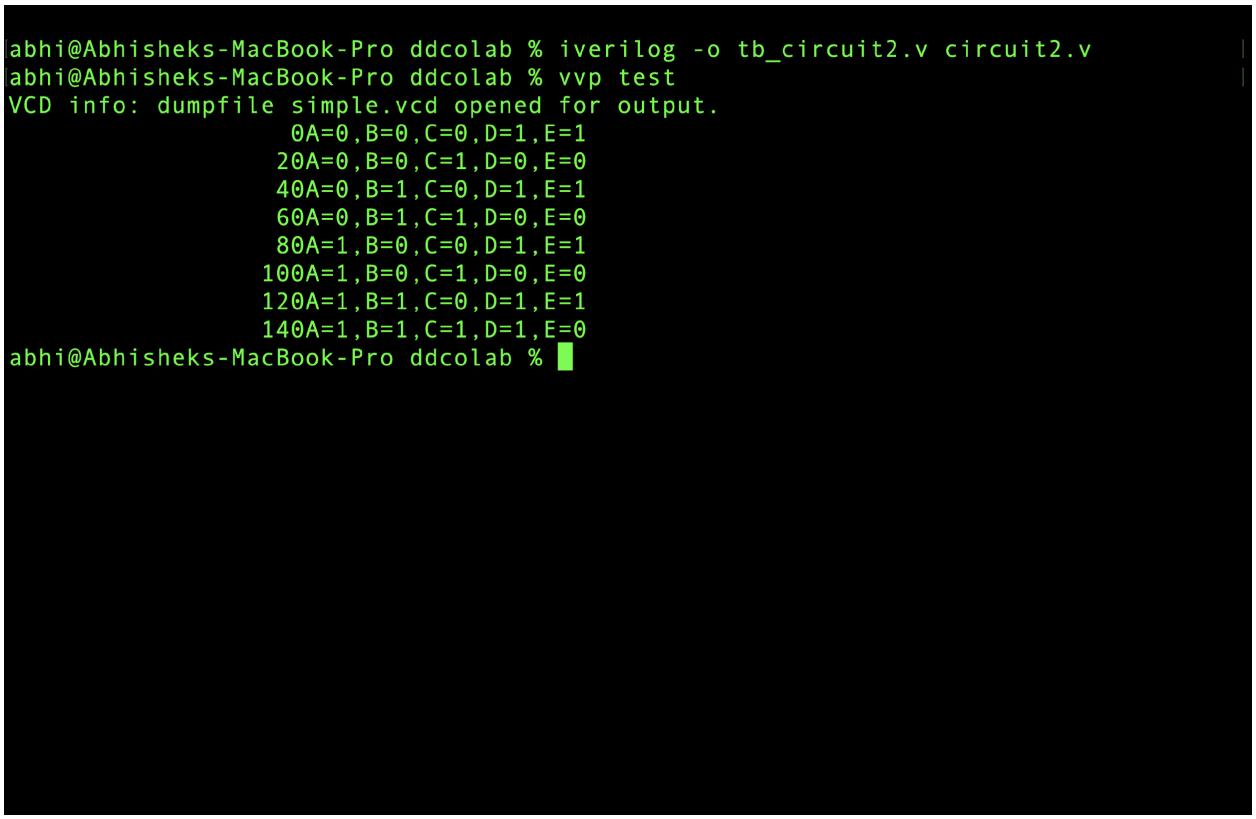
TITLE :

WRITE A VERILOG PROGRAM TO MODEL A GIVEN LOGIC CIRCUIT. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

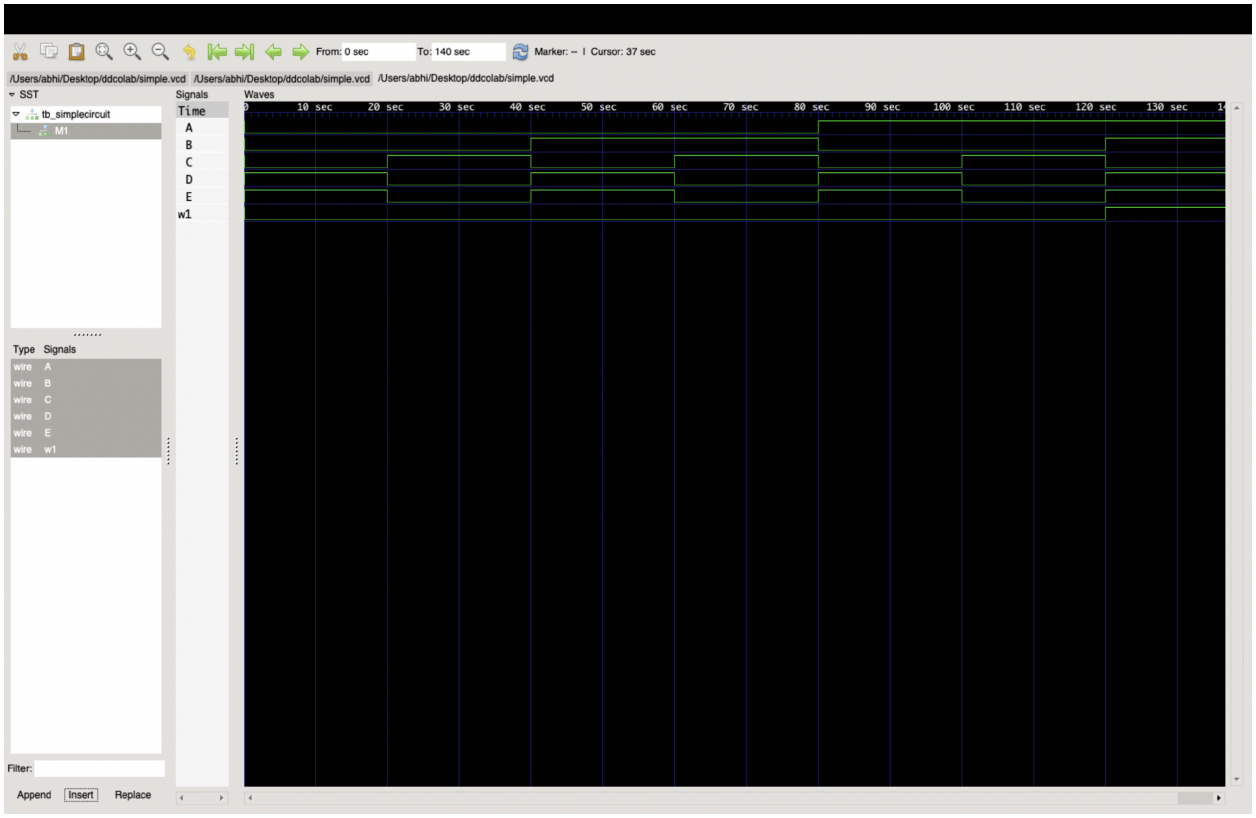


I. Verilog Code Screenshot

```
module simple_circuit(A2,B2,C2,Z);
input A2,B2,C2;
output Z;
```



II. Verilog VVP Output Screen Shot



III. GTKWAVE Screenshot

IV. Output Table to be completed and included

A	B	C	D	E
0	0	0	1	1
0	0	1	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0

1	1	0	1	0
1	1	1	1	0

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.

- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: YAMAN GUPTA

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Date:23/08/2022