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PES2UG21CS619

WEEK 3:

1) HALF ADDER:

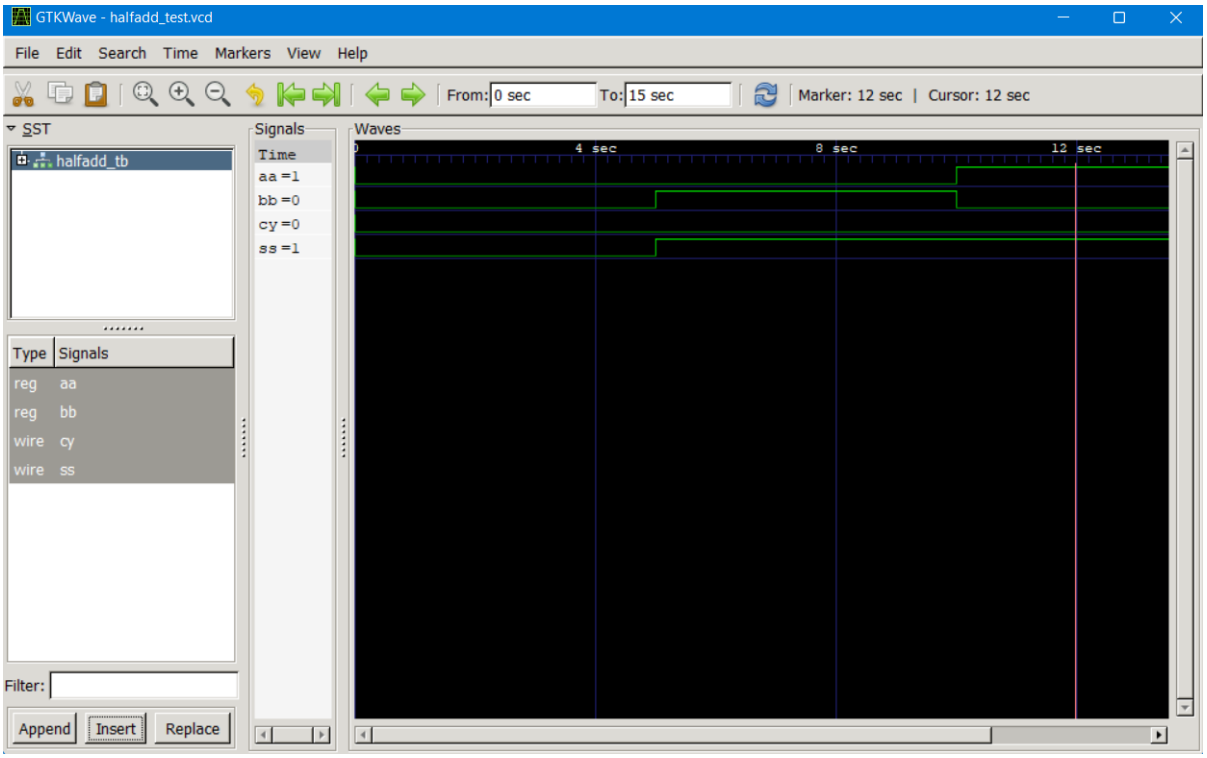
VERILOG CODE:

```
module half(input wire a,b, output wire sum,cout);
xor x0(sum,a,b);
and a0(cout,a,b);
endmodule
```

VVP VERILOG OUTPUT:

```
C:\iverilog\bin>vvp try6
VCD info: dumpfile halfadd_test.vcd opened for output.
                    0a=0,b=0,sum=0,carry=0
                    5a=0,b=1,sum=1,carry=0
                   10a=1,b=0,sum=1,carry=0
                   15a=1,b=1,sum=0,carry=1
```

GKTWAVE OUTPUT:



TRUTH TABLE:

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0

1	1	0	1

2)<u>FULL ADDER:</u>

VERILOG CODE:

```
module fulladd(output wire sum, cout, input wire a,
b, cin);
assign cout = (a & b) | (b & cin) | (a & cin) ;
assign sum = (a ^ b) ^ cin ;
endmodule
```

VVP VERILOG OUTPUT:

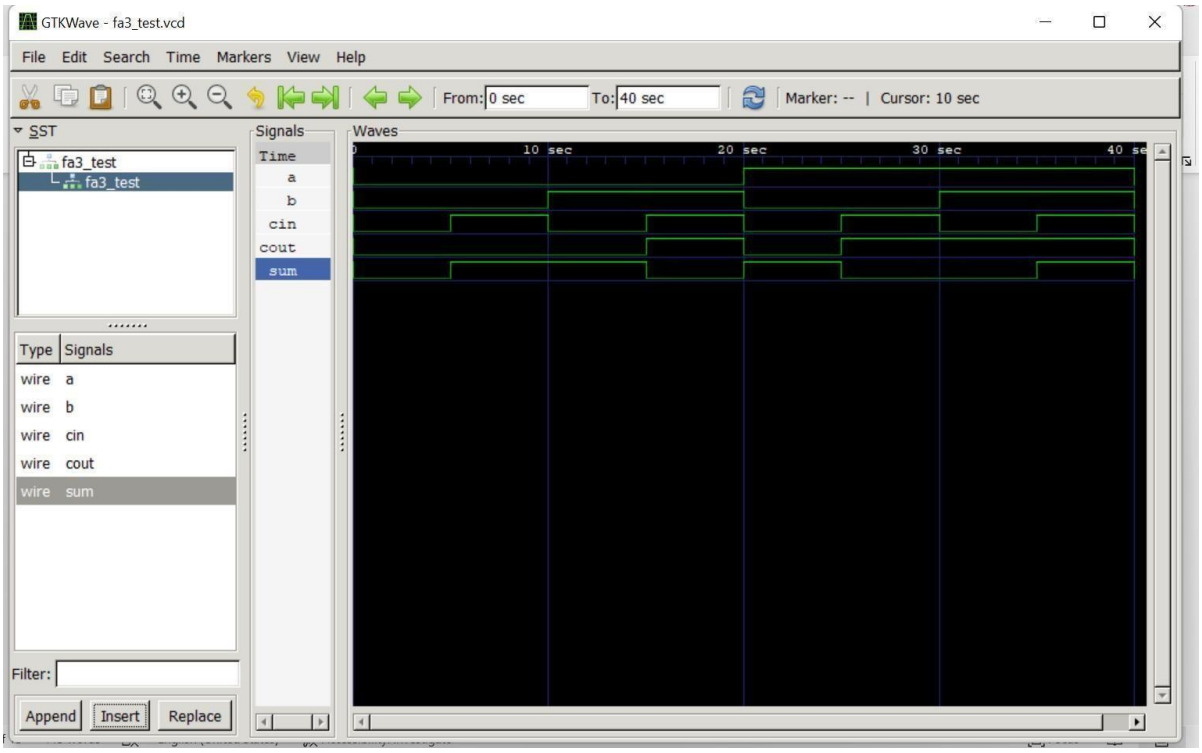
```
C:\iverilog\bin>iverilog -o dsn fulladder.v fulladder_tb.v

C:\iverilog\bin>vvp dsn
VCD info: dumpfile fa3_test.vcd opened for output.
                   0 a=0, b=0, c=0, sum=0, carry=0
                   5 a=0, b=0, c=1, sum=0, carry=1
                  10 a=0, b=1, c=0, sum=0, carry=1
                  15 a=0, b=1, c=1, sum=1, carry=0
                  20 a=1, b=0, c=0, sum=0, carry=1
                  25 a=1, b=0, c=1, sum=1, carry=0
                  30 a=1, b=1, c=0, sum=1, carry=0
                  35 a=1, b=1, c=1, sum=1, carry=1
                  40 a=0, b=0, c=0, sum=0, carry=0

C:\iverilog\bin>gtkwave fa3_test.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI
```

GTKWAVE OUTPUT:



TRUTH TABLE:

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1