Digital Design and Computer Organisation Laboratory

UE20CS256

3rd Semester, Academic Year 2022-23

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Week#____4_____ Program Number: ____1__

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A 16 BIT ALU THAT CAN PERFORM FOUR OPERATIONS-ADDITION, SUBTRACTION, AND along with OR OPERATION. ALL THESE OPERATIONS GENERATE A SIXTEEN BIT RESULT.SHOW THE VVP OUTPUT.DISPLAY THE SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

I. Verilog Code Screenshot

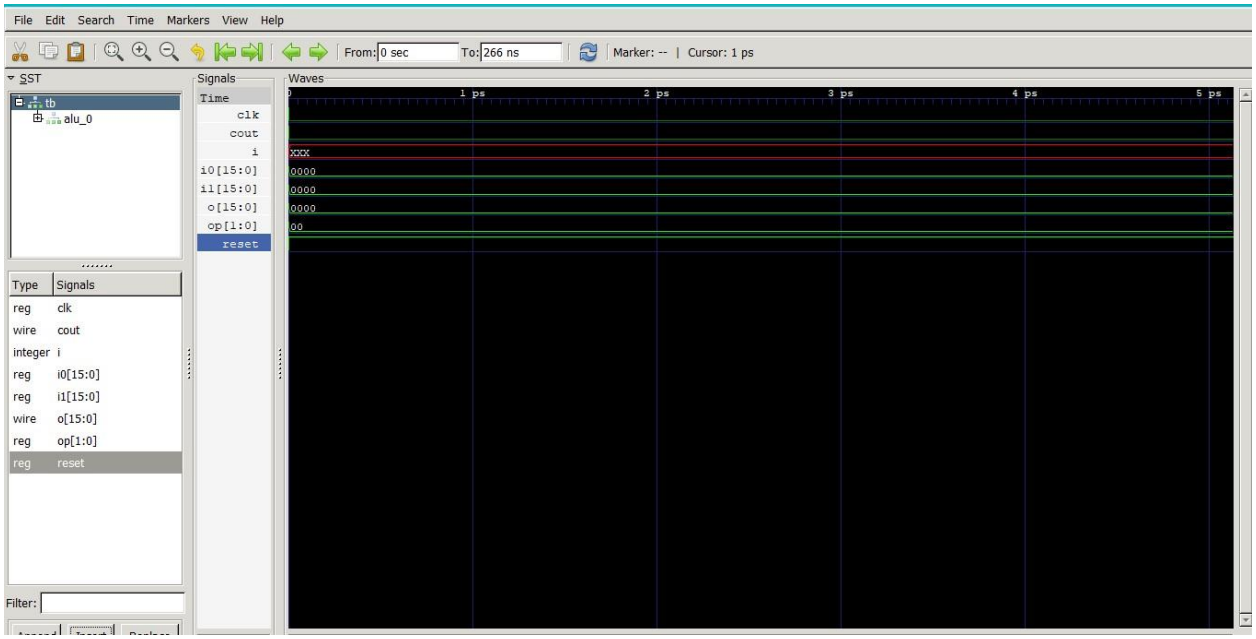
```
module fa (input wire i0, i1, cin, output wire sum, cout);
   wire t0, t1, t2;
   xor3 _i0 (i0,i1,cin,sum);
   and2 _i1 (i0,i1,t0);
   and2 _i2 (i1,cin,t1);
   and2 _i3 (i0,cin,t2);
   or3 _i4 (t0,t1,t2,cout);
endmodule


module addsub(input wire addsub, i0, i1, cin, output wire sumdiff, cout);
  wire t;
  xor2 _i1(i1,addsub,t);
  fa _i0 (i0,t,cin,sumdiff,cout);
endmodule


module alu_slice (input wire [1:0] op, input wire i0, i1, cin, output wire o, cout);
   wire t_sumdiff, t_and, t_or, t_andor;

   addsub _i0 (op[0],i0,i1,cin,t_sumdiff,cout);
   and2 _i1 (i0,i1,t_and);
   or2 _i2  (i0,i1,t_or);
   mux2 _i3 (t_and,t_or,op[0],t_andor);
   mux2 _i4 (t_sumdiff,t_andor,op[1],o);
endmodule


module alu (input wire [1:0] op, input wire [15:0] i0,i1,output wire [15:0] o, output wire cout);

   wire [14:0] c;
   alu_slice _i0 (op, i0[0], i1[0], op[0] , o[0], c[0]);
   alu_slice _i1 (op, i0[1], i1[1], c[0] , o[1], c[1]);
   alu_slice _i2 (op, i0[2], i1[2], c[1] , o[2], c[2]);
   alu_slice _i3 (op, i0[3], i1[3], c[2] , o[3], c[3]);
   alu_slice _i4 (op, i0[4], i1[4], c[3] , o[4], c[4]);
   alu_slice _i5 (op, i0[5], i1[5], c[4] , o[5], c[5]);
```

```
  xor2 _i1(i1,addsub,t);
  fa _i0 (i0,t,cin,sumdiff,cout);
endmodule


module alu_slice (input wire [1:0] op, input wire i0, i1, cin, output wire o, cout);
   wire t_sumdiff, t_and, t_or, t_andor;

   addsub _i0 (op[0],i0,i1,cin,t_sumdiff,cout);
   and2 _i1 (i0,i1,t_and);
   or2 _i2  (i0,i1,t_or);
   mux2 _i3 (t_and,t_or,op[0],t_andor);
   mux2 _i4 (t_sumdiff,t_andor,op[1],o);
endmodule


module alu (input wire [1:0] op, input wire [15:0] i0,i1,output wire [15:0] o, output wire cout);

   wire [14:0] c;
   alu_slice _i0 (op, i0[0], i1[0], op[0] , o[0], c[0]);
   alu_slice _i1 (op, i0[1], i1[1], c[0] , o[1], c[1]);
   alu_slice _i2 (op, i0[2], i1[2], c[1] , o[2], c[2]);
   alu_slice _i3 (op, i0[3], i1[3], c[2] , o[3], c[3]);
   alu_slice _i4 (op, i0[4], i1[4], c[3] , o[4], c[4]);
   alu_slice _i5 (op, i0[5], i1[5], c[4] , o[5], c[5]);
   alu_slice _i6 (op, i0[6], i1[6], c[5] , o[6], c[6]);
   alu_slice _i7 (op, i0[7], i1[7], c[6] , o[7], c[7]);
   alu_slice _i8 (op, i0[8], i1[8], c[7] , o[8], c[8]);
   alu_slice _i9 (op, i0[9], i1[9], c[8] , o[9], c[9]);
   alu_slice _i10 (op, i0[10], i1[10], c[9] , o[10], c[10]);
   alu_slice _i11 (op, i0[11], i1[11], c[10] , o[11], c[11]);
   alu_slice _i12 (op, i0[12], i1[12], c[11] , o[12], c[12]);
   alu_slice _i13 (op, i0[13], i1[13], c[12] , o[13], c[13]);
   alu_slice _i14 (op, i0[14], i1[14], c[13] , o[14], c[14]);
   alu_slice _i15 (op, i0[15], i1[15], c[14] , o[15], cout);
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp dsn
VCD info: dumpfile tb_alu.vcd opened for output.
At time =                    0, Operator= 00,i0=0000, i1=0000,Sum = 0000,Carry 0
At time =                  260, Operator= 00,i0=aa55, i1=55aa,Sum = ffff,Carry 0
At time =                  360, Operator= 00,i0=ffff, i1=0001,Sum = 0000,Carry 1
At time =                  460, Operator= 00,i0=0001, i1=7fff,Sum = 8000,Carry 0
At time =                  560, Operator= 01,i0=0000, i1=0000,Sum = 0000,Carry 1
At time =                  660, Operator= 01,i0=aa55, i1=55aa,Sum = 54ab,Carry 1
At time =                  760, Operator= 01,i0=ffff, i1=0001,Sum = fffe,Carry 1
At time =                  860, Operator= 01,i0=0001, i1=7fff,Sum = 8002,Carry 0
At time =                  960, Operator= 10,i0=0000, i1=0000,Sum = 0000,Carry 0
At time =                 1060, Operator= 10,i0=aa55, i1=55aa,Sum = 0000,Carry 0
At time =                 1160, Operator= 10,i0=ffff, i1=0001,Sum = 0001,Carry 1
At time =                 1260, Operator= 10,i0=0001, i1=7fff,Sum = 0001,Carry 0
At time =                 1360, Operator= 11,i0=0000, i1=0000,Sum = 0000,Carry 1
At time =                 1460, Operator= 11,i0=aa55, i1=55aa,Sum = ffff,Carry 1
At time =                 1560, Operator= 11,i0=ffff, i1=0001,Sum = ffff,Carry 1
At time =                 1660, Operator= 11,i0=0001, i1=7fff,Sum = 7fff,Carry 0
tb_alu.v:45: $finish called at 2660 (100ps)
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

	op[1:0]	i0[15:0]	i1[15:0]	Output
TESTVECTOR0	2’b00	16’h0000	16’h0000	0000
TESTVECTOR1	2’b00	16’haa55	16’h55aa	ffff
TESTVECTOR2	2’b00	16'hffff	16'h0001	0000
TESTVECTOR3	2’b00	16'h0001	16'h7fff	8000
TESTVECTOR4	2'b01	16'h0000	16'h0000	0000
TESTVECTOR5	2'b01	16’haa55	16’h55aa	54ab

TESTVECTOR6	2'b01	16'hffff	16'h0001	fffe
TESTVECTOR7	2'b01	16'h0001	16'h7fff	8002
TESTVECTOR8	2’b10	16’h0000	16’h0000	0000
TESTVECTOR9	2’b10	16’haa55	16’h55aa	0000
TESTVECTOR10	2’b10	16'hffff	16'h0001	0001
TESTVECTOR11	2’b10	16'h0001	16'h7fff	0001
TESTVECTOR12	2’b11	16’h0000	16’h0000	0000
TESTVECTOR13	2’b11	16’haa55	16’h55aa	ffff
TESTVECTOR14	2’b11	16'hffff	16'h0001	ffff
TESTVECTOR15	2’b11	16'h0001	16'h7fff	7fff

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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