Digital Design and Computer Organisation Laboratory

UE20CS256

3rd Semester, Academic Year 2021-22

Date: 24 August 2022

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Week#____1_____Program Number:_____1___

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT AND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

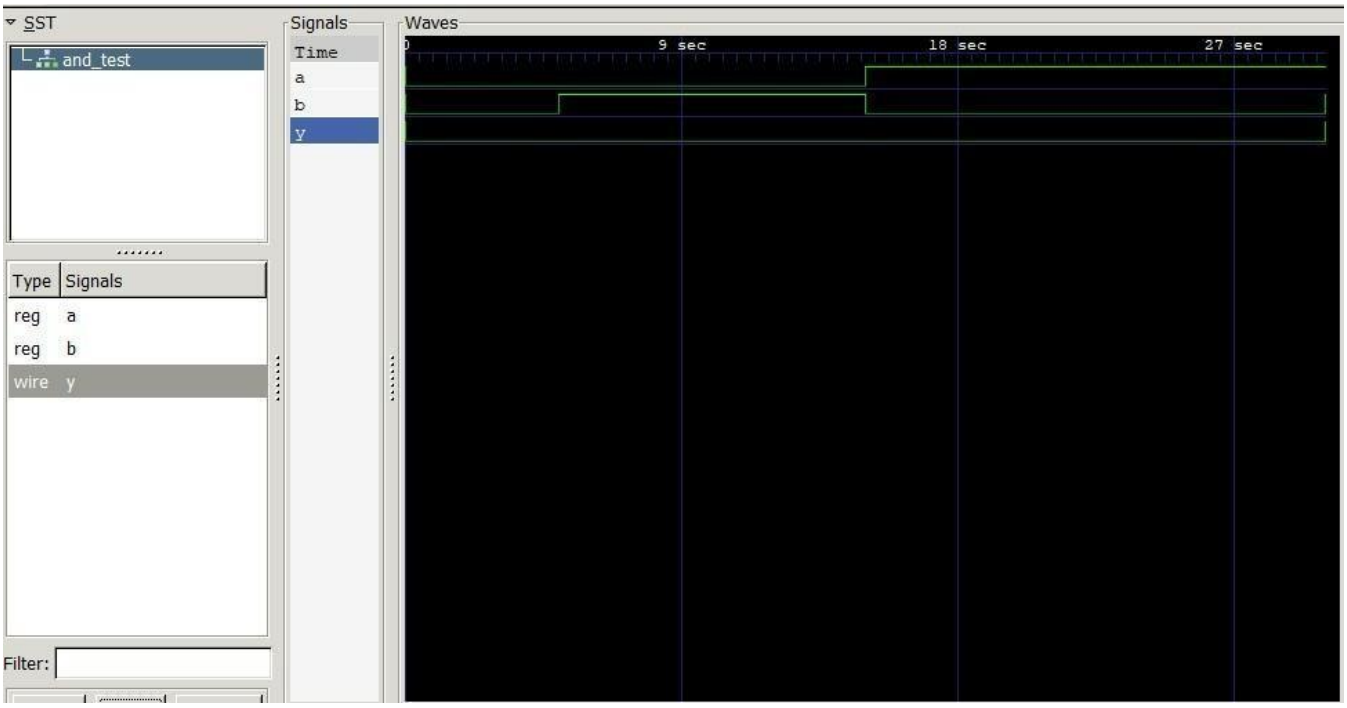
I. Verilog Code Screenshot

```
module andgate(a,b,y);
input a,b;
output y;
assign y = a&b;
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp dsnandgate.v
VCD info: dumpfile andout.vcd opened for output.
                    0a=0, b=0, y=0
                    5a=0, b=1, y=0
                   15a=1, b=0, y=0
                   30a=1, b=1, y=1
```

III. GTKWAVE Screenshot



IV. Output Table to be completed and included

2 - input AND gate

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Week#____1_____ Program Number:_____2 ___

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT OR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE OR GATE TRUTH TABLE

I. Verilog Code Screenshot

```
module orgate(a,b,y);
input a,b;
output y;
assign y = a|b;
endmodule
```

ANSWER-

II. Verilog VVP Output Screen Shot

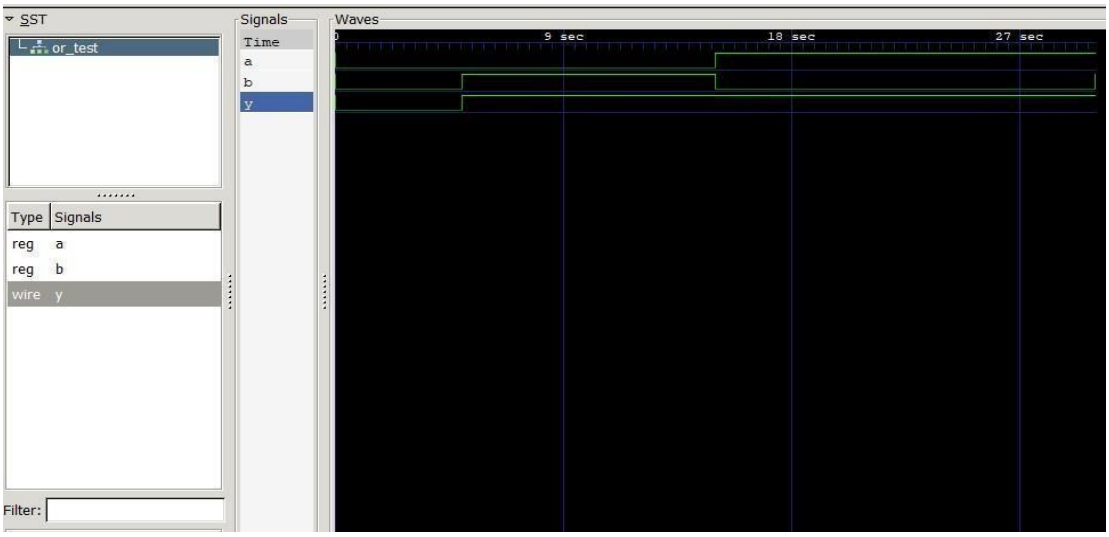
ANSWER-

```
C:\iverilog\bin>vvp dsnorgate.v
VCD info: dumpfile orout.vcd opened for output.
                   0a=0, b=0, y=0
                   5a=0, b=1, y=1
                  15a=1, b=0, y=1
                  30a=1, b=1, y=1
```

III. GTKWAVE

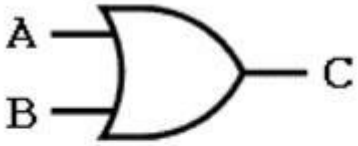
Screenshot

ANSWER-



IV. Output Table to be completed and included

OR



Inputs		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Week#____1_____ Program Number:

_____

3

_____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A NOT GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOT GATE TRUTH TABLE

I. Verilog Code Screenshot

```
module notgate(a,y);
input a;
output y;
assign y = !a;
endmodule
```

ANSWER-

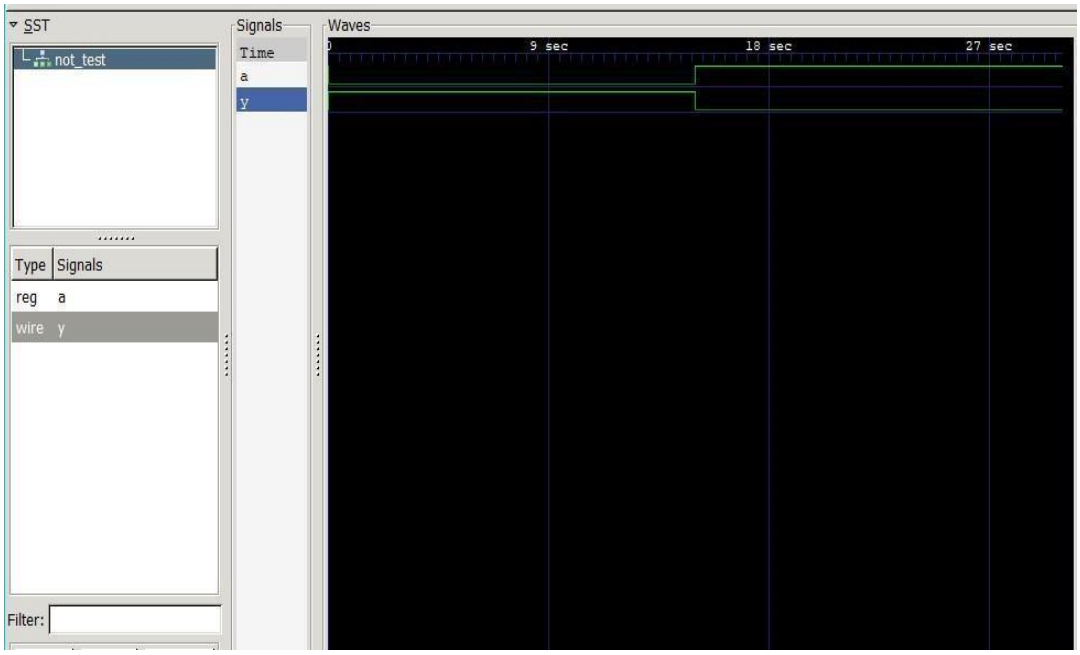
II. Verilog VVP Output Screen Shot

ANSWER-

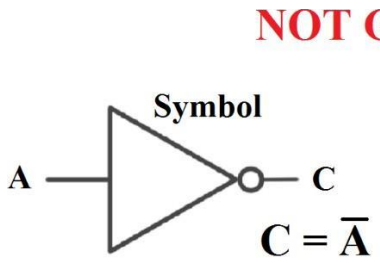
```
C:\iverilog\bin>vvp dsnnotgate.v
VCD info: dumpfile notout.vcd opened for output.
                    0a=0, y=1
                   15a=1, y=0
```

III. GTKWAVE Screenshot

Answer-



IV. Output Table to be completed and included



Truth Table

INPUT	OUTPUT
A	NOT A
0	1
1	0

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Week#____1_____ TITLE : Program Number:____4___

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NAND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NAND GATE TRUTH TABLE

I. Verilog Code Screenshot

```
module nandgate(a,b,y);
input a,b;
output y;
assign y = a~&b;
endmodule
```

Answer-

II. Verilog VVP Output Screen Shot

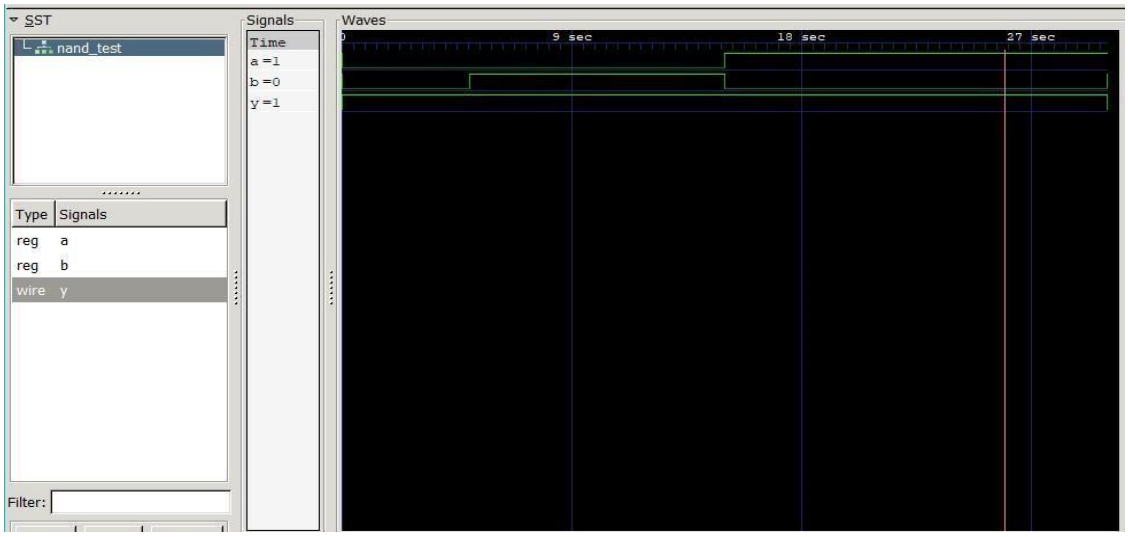
ANSWER-

```
C:\iverilog\bin>vvp dsnnandgate.v
VCD info: dumpfile nandout.vcd opened for output.
                   0a=0, b=0, y=1
                   5a=0, b=1, y=1
                  15a=1, b=0, y=1
                  30a=1, b=1, y=0
```

III. GTKWAVE

Screenshot

ANSWER-



IV. Output Table to be completed and included

Q = A NAND B

Truth Table

Input A	Input B		Output Q
0	0		1
0	1		1
1	0		1
1	1		0

Week#____1_____

Program Number:

_____

5

_____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOR GATE TRUTH TABLE

I. Verilog Code Screenshot

ANSWER-

```
module norgate(a,b,y);
input a,b;
output y;
assign y = a~|b;
endmodule
```

II. Verilog VVP Output Screen Shot

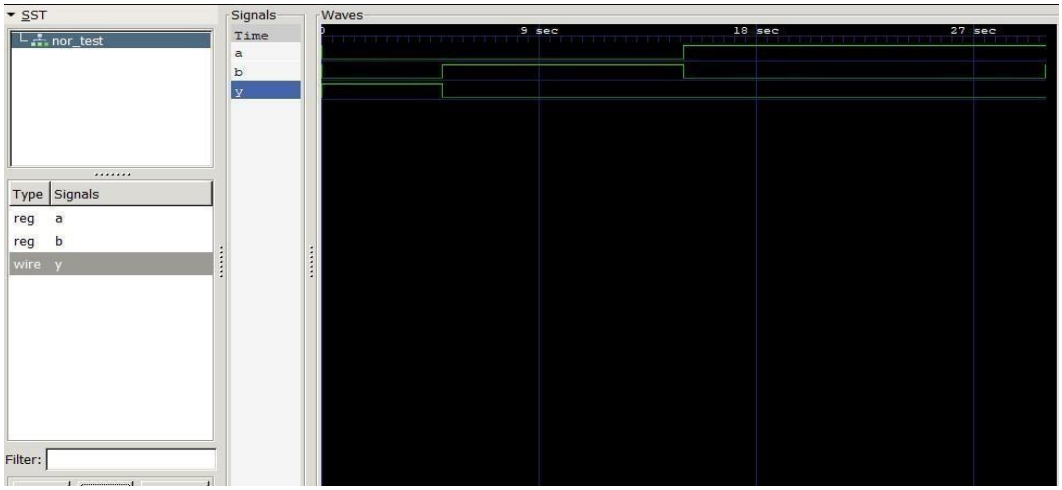
ANSWER-

```
C:\iverilog\bin>vvp dsnnorgate.v
VCD info: dumpfile norout.vcd opened for output.
                  0a=0, b=0, y=1
                  5a=0, b=1, y=0
                 15a=1, b=0, y=0
                 30a=1, b=1, y=0
```

III. GTKWAVE

Screenshot

ANSWER-



IV. Output Table to be completed and included

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Week#____1_____ Program Number:_____6__TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot

ANSWER-

```
module xorgate(a,b,y);
input a,b;
output y;
assign y = a^b;
endmodule
```

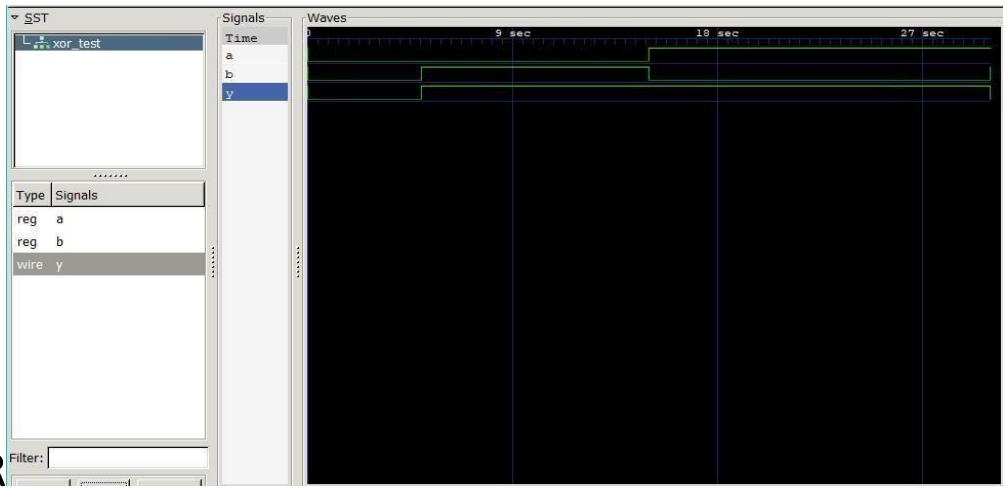
II. Verilog VVP Output Screen Shot

ANSWER-

```
C:\iverilog\bin>vvp dsnxorgate.v
VCD info: dumpfile xorout.vcd opened for output.
                   0a=0, b=0, y=0
                   5a=0, b=1, y=1
                  15a=1, b=0, y=1
                  30a=1, b=1, y=0
```

III. GTKWAVE Screenshot

ANSWER



IV Output Table to be completed and included

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Week#____1_____

Program Number:

_____

7

_____

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XNOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot

ANSWER-

```
module xnorgate(a,b,y);
input a,b;
output y;
assign y = a~^b;
endmodule
```

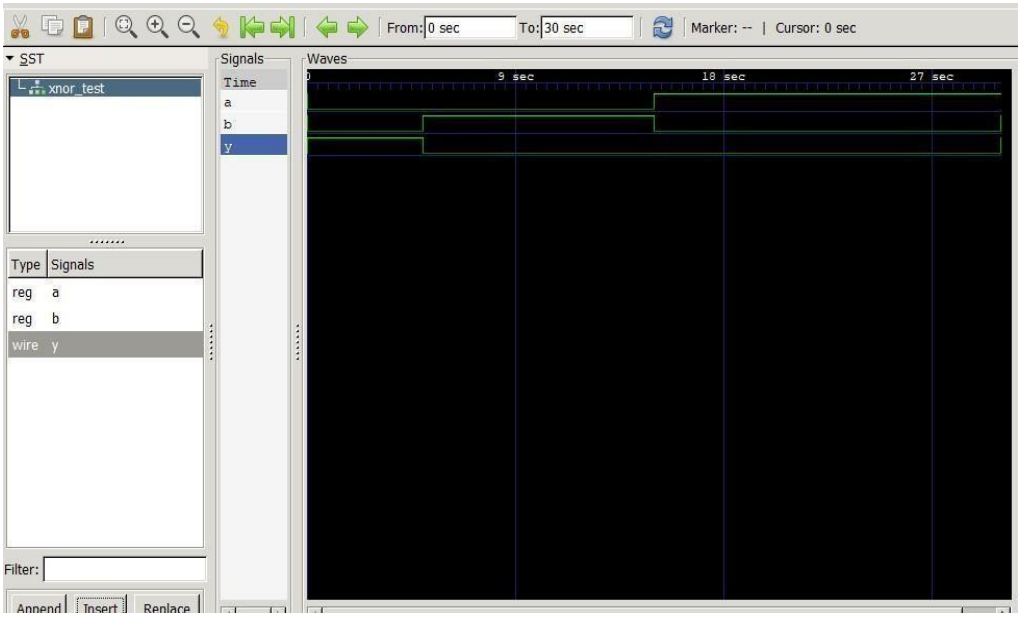
II. Verilog VVP Output Screen Shot

ANSWER-

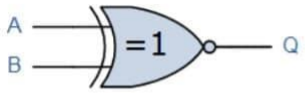
```
C:\iverilog\bin>vvp dsnxnorgate.v
VCD info: dumpfile xnorout.vcd opened for output.
 0a=0, b=0, y=1
 5a=0, b=1, y=0
15a=1, b=0, y=0
30a=1, b=1, y=1
```

III. GTKWAVE Screenshot

ANSWER-



IV. Output Table to be completed and included

Symbol	Truth Table		
 2-input Ex-NOR Gate	A	B	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A XNOR B			

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

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Section: J

Date: 24 August 2022