

Microprocessor and Computer Architecture

UE21CS251B

4th Semester, Academic Year 2022-23

Date:

Name: Yaman Gupta	SRN: PES2UG21CS61 9	Section j
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Week#____1____

Program Number:

____1____

Title of the Program

Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0

I. ARM Assembly Code

```
mov r0,#0
mov r1,#81

and r2,r1,#1
cmp r2,#1

addeq r0,r0,#255
```

II. Output Screen Shot (Two)

The output should be verified for both even and odd numbers.

Floating Point | even_odd.s

Register	Value
R0	:000000ff
R1	:00000051
R2	:00000001
R3	:00000000
R4	:00000000
R5	:00000000
R6	:00000000
R7	:00000000
R8	:00000000

```
00001000:E3A00000  mov r0, #0
00001004:E3A01051  mov r1, #81
00001008:E2012001  and r2, r1, #1
0000100C:E3520001  cmp r2, #1
00001010:028000FF  addeq r0, r0, #255
```

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Name: Yaman Gupta	SRN: PES2UG21CS619	Section J
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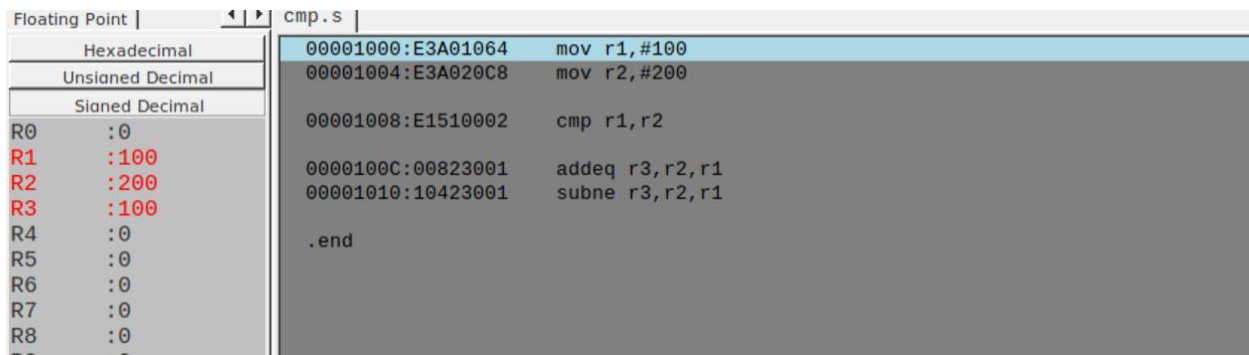
Week#____1_____
____2____

Program
Number:

Title of the Program

**Write an ALP to compare the value of R0 and R1,
add if R0 = R1, else subtract**

I.ARM Assembly Code



The screenshot shows an ARM assembly editor. On the left, a register window displays the following values: R0: 0, R1: 100, R2: 200, R3: 100, R4: 0, R5: 0, R6: 0, R7: 0, R8: 0. The main editor area shows the following assembly code:

```
00001000:E3A01064  mov r1,#100
00001004:E3A020C8  mov r2,#200
00001008:E1510002  cmp r1,r2
0000100C:00823001  addeq r3,r2,r1
00001010:10423001  subne r3,r2,r1
.end
```

II. Output Screen Shot (Two)

The output should be verified for both equal
and nor equal values

```
mov r1,#100
mov r2,#200

cmp r1,r2

addeq r3,r2,r1
subne r3,r2,r1

.end
```

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Week#____1_____
____3____

Program
Number:

Title of the Program

Based on the value of the number in R0, Write an ALP to store 1 in R1 if R0 is zero, Store 2 in R1 if R0 is positive, Store 3 in R1 if R0 is negative.
(Program shown in class)

I.ARM Assembly Code

Floating Point	pos_neg.s
Hexadecimal	00001000:E3A0001D mov r0,#29
Unsigned Decimal	00001004:E3A01000 mov r1,#0
Signed Decimal	00001008:E3A02000 mov r2,#0
R0 :0000001d	0000100C:E3500000 cmp r0,#0
R1 :00000002	00001010:02811001 addeq r1,r1,#1
R2 :00000000	00001014:C2811002 addgt r1,r1,#2
R3 :00000000	00001018:B2811003 addlt r1,r1,#3
R4 :00000000	
R5 :00000000	
R6 :00000000	
R7 :00000000	
R8 :00000012	

II. Output Screen Shot (Three)

The output should be verified for zero, positive and negative cases.

```
mov r0,#29
mov r1,#0
mov r2,#0

cmp r0,#0

addeq r1,r1,#1
addgt r1,r1,#2
addlt r1,r1,#3

.end
```

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.

- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: Yaman Gupta

Name: Yaman Gupta

SRN: PES2UG21CS619

Section: J

Date: 18/01/2023