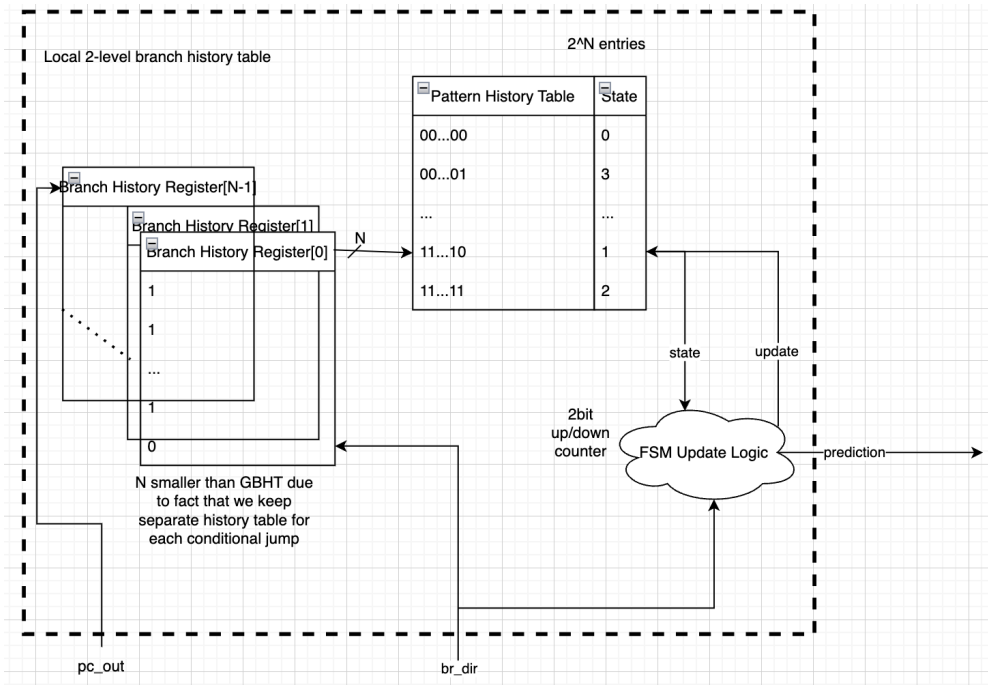
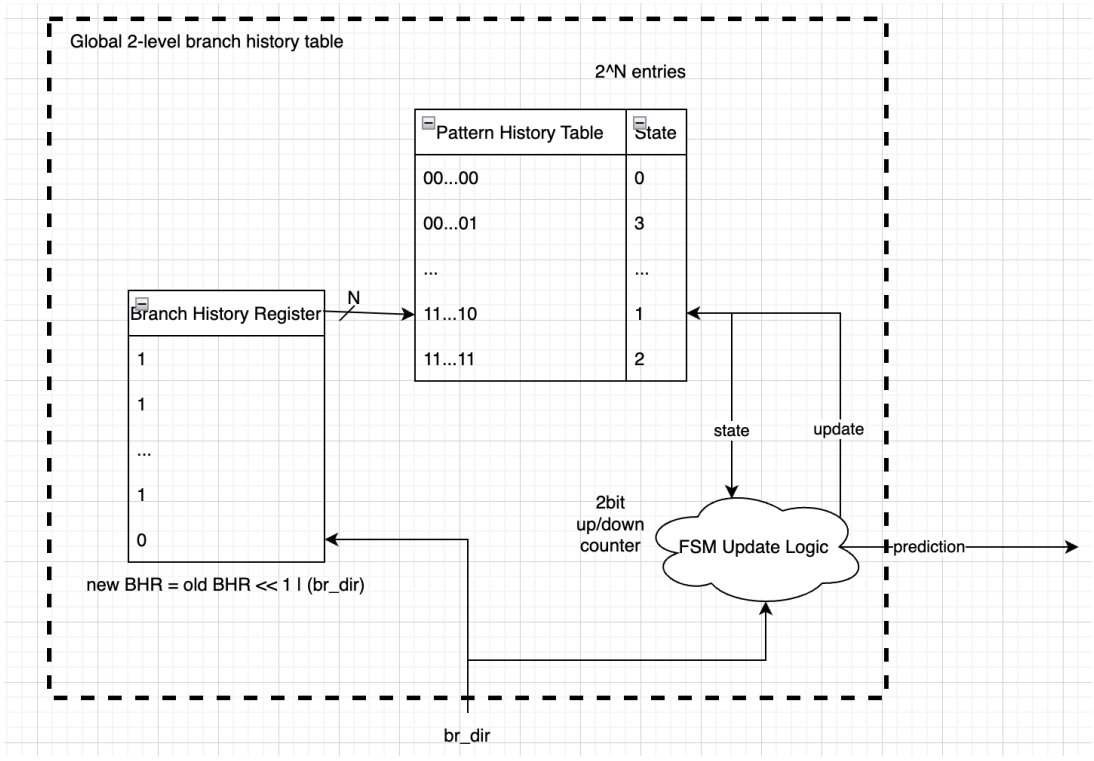
CP2 Advanced Feature Designs/Notes

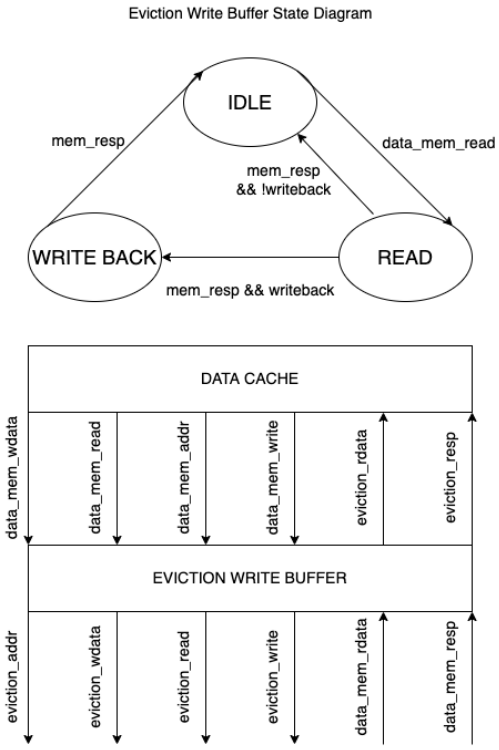
Local Branch History Table



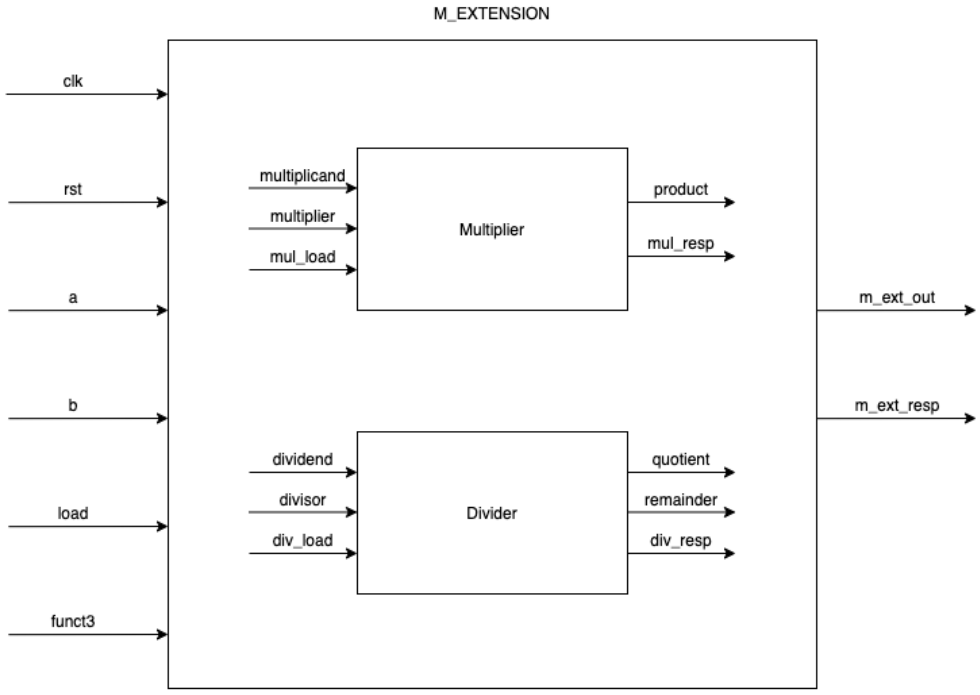
Global 2-level Branch History Table



Eviction Write Buffer

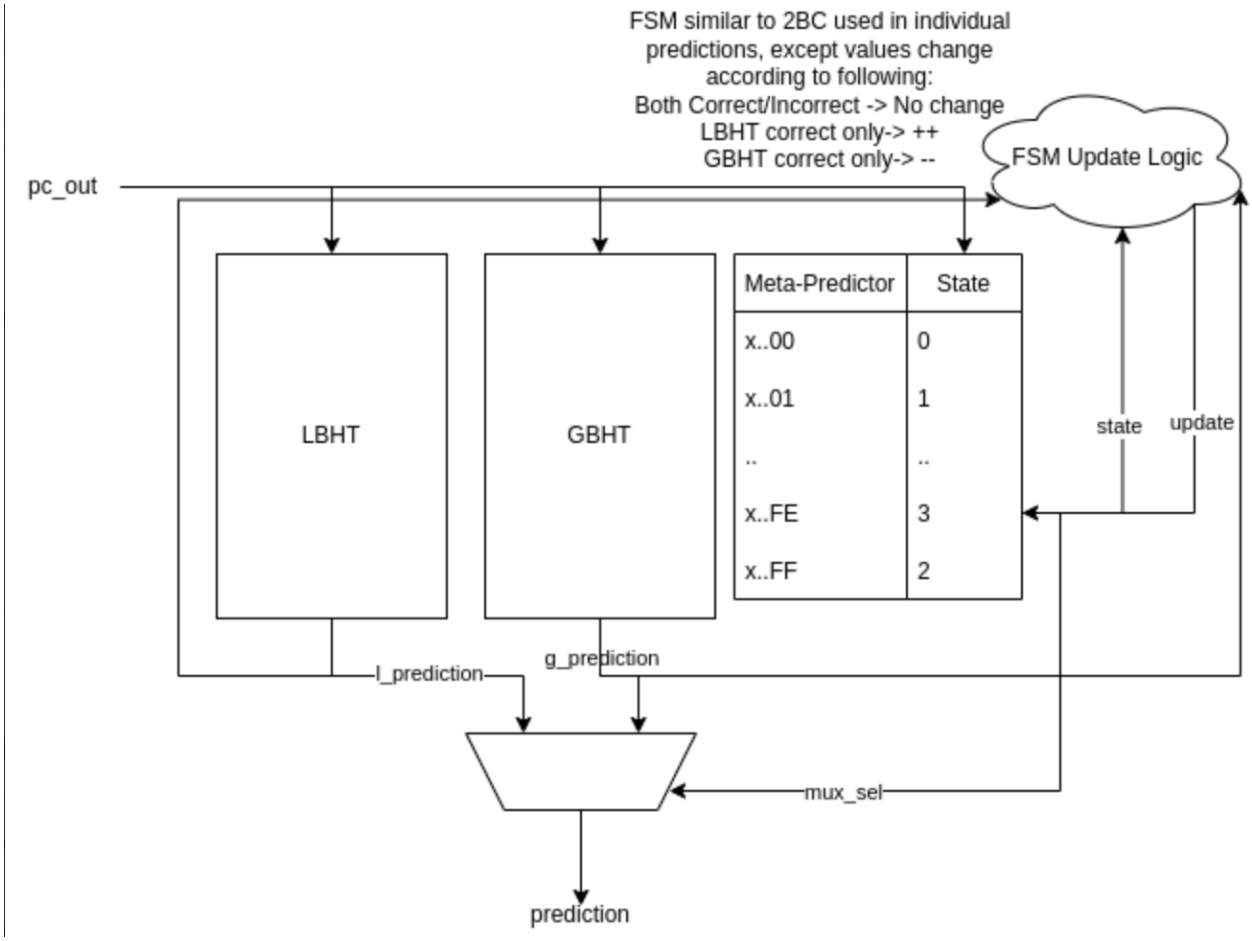


RISC-V M Extension



load when opcode = op_reg and funct7=1
The multiplier will apply Shift-and-Add Multiplication
The Divider will apply Shift-and_Subtract Division

Tournament Branch Predictor



L2 - Cache + 4-way Set Associative Cache

We will create a separate larger L2 cache that interfaces with the L1 cache and arbiter where in the event of L1 cache miss we look into the L2 cache.

To create the 4-way set associative cache we simply bolster the current implementation by making the LRU array bigger to support 4-ways. Use pseudo-LRU.