CP3 Progress Report/Roadmap

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Ching-Chia worked on implementation of RISC-V M extension, Eviction write buffer, Basic Hardware Prefetching, L2 Cache System, Parameterized cache, and 4-way Associative Cache, debugging and testing, Nicholas worked on the Global Branch History Table, Local Branch History Table, and Tournament Branch Predictor, as well as debugging and testing. Himanshu tried working on L2+ Cache System, Parameterized cache, and 4-way Associative Cache but was not able to make his code work.

Functionalities Implemented

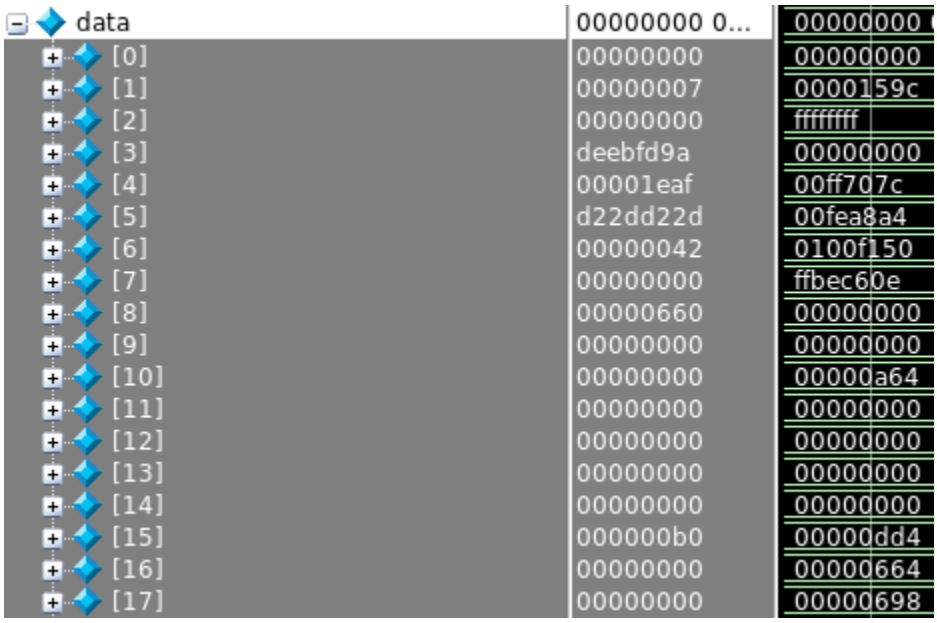
The advanced features we implemented were L2 Cache System, 4-way Associative Cache, Local Branch History Table, Global Branch History Table, Tournament Branch Predictor, RISC-V M Extension, and Eviction Write Buffer and Basic Hardware Prefetching. First of all, the RISC-V M extension implementation consists of multiplier.sv, divider.sv, and m_ext.sv. Multiplier applied Shift-and-Add Multiplication, divider applied Shift-and-Subtract Division, the m_ext wrapper will parse the funct3 signal and decide the corresponding strategy for signed/unsigned data type. Next, we worked on the write eviction buffer for the data cache, it holds dirty data which will be written to memory. Then, we worked on Basic Hardware Prefetcher for instruction cache, since the spatial locality of testing code for data cache is much lower than the instruction cache. Finally, we implemented the 4-way set associative parameterized cache and added L2 cache for both instruction and data cache.

The local branch history table utilizes the PC offset as well as the branch history register to get a more precise estimation of branch direction. States are stored in the pattern history register, which holds a 2-bit state corresponding to the 2-bit state FSM talked about in class. 00 is the Strongly Not Take state, 01 is the Not Take, 10 is the Take, and 11 is the Strongly Take state. The global branch history table works in a similar way, except that it is less dependent on PC values to determine the state for each pattern history table entry. At each clk edge, opcodes from the IF stage and EX stage are read. If the IF stage is a branch opcode, then a prediction is made. Once this instruction flows down to the EX stage, we must compare and verify our previous prediction. If it is not correct, we send a miss signal from the branch predictor. The tournament predictor sits above these 2 and finds which of the 2 predictors performs better based on the PC value. The better of the 2 is filtered down to be the actual prediction and miss values.

This is done similarly to each branch predictor itself, with state and 2-bit FSM. 00 is Strongly take GBHT, 01 is take GBHT, 10 is take LBHT, and 11 is Strongly take LBHT.

Testing Strategies

To verify our advanced feature, we used the all three provided test programs, mp4-cp1/2/3.s, comparing the correct test result from the previous checkpoint(without advanced feature). We used comp2_m.s for RISC-V M extension verification. In addition, we added performance counters for every advanced feature in order to make sure the advanced features were being used. We also compared the overall runtime between design with/without advanced features for validating if the advanced features improve the performance. Furthermore, we also passed the comp1.s, comp2_m.s, and comp3.s test codes with our design. The following is the end result of our registers for mp4-cp3.s.



Timing and Energy Analysis

We ran into some issues with the module being too big for the given board size, but after some optimizations and removing the L2 cache temporarily, we were able to get the compilation and timing analysis. Below are our results. Our fast model had a negative 0.146 slack and negative 1.196 TNS.

	Fmax	Restricted Fmax

Slow 900mV 100C	51.17MHz	51.17MHz
Slow 900mV -40C	54.42MHz	54.42MHz
Fast 900mV -40C	n/a	n/a

The following is the power analyzer results.

Power Analyzer Status	Successful - Mon Apr 25 21:46:35 2022
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Standard Edition
Revision Name	mp4
Top-level Entity Name	mp4
Family	Arria II GX
Device	EP2AGX45DF25I3
Power Models	Final
Total Thermal Power Dissipation	1433.04 mW
Core Dynamic Thermal Power Dissipation	297.93 mW
Core Static Thermal Power Dissipation	350.44 mW
I/O Thermal Power Dissipation	784.67 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

```
Info: 21077 Low junction temperature is -40 degrees C
Info: 21077 High junction temperature is 100 degrees C
Info: 332104 Reading SDC File: 'mp4.out.sdc'
Info: 332152 The following assignments are ignored by the derive_clock_uncertainty command
Info: 223000 Starting Vectorless Power Activity Estimation
Info: 223001 Completed Vectorless Power Activity Estimation
Info: 218000 Using Advanced I/O Power to simulate I/O buffers with the specified board trace model
Info: 334003 Started post-fitting delay annotation
Info: 334004 Delay annotation completed successfully
Info: 215049 Average toggle rate for this design is 12.180 millions of transitions / sec
Info: 215031 Total thermal power estimate for the design is 1433.04 mW
Info:       Quartus Prime Power Analyzer was successful. 0 errors, 1 warning
```

Roadmap

For the next checkpoint, we will optimize our design by testing different combinations of our modules that produce the fastest outcome of our overall processor. We noticed in this checkpoint that some modules, like the L2 cache even though theoretically improves the performance of a processor by reducing the memory latency, actually caused our processor to be slower. This can be caused by a multitude of issues, such as poor optimization, or memory locality not being exploited enough for L2 cache to make sense. Thus, by removing features like these or changing the parameters and seeing what produces the most optimal result, we can try to do the best we can on this

next checkpoint. Furthermore, we will split up this work between our group and report amongst ourselves to find the best combination. The final report and video will be done as a group.