ECE411 Final Project
5-stages-of-grief

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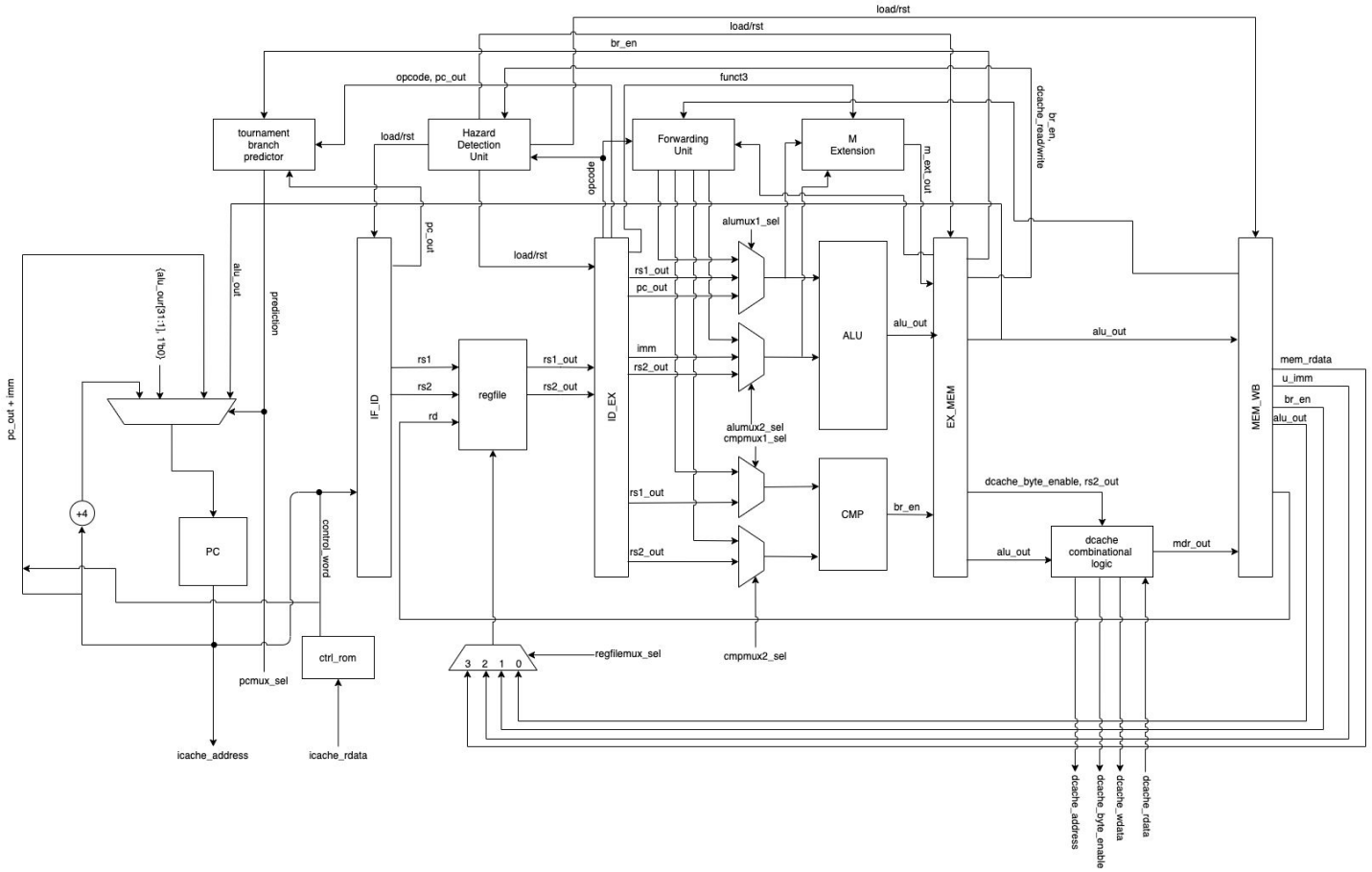
Design Overview

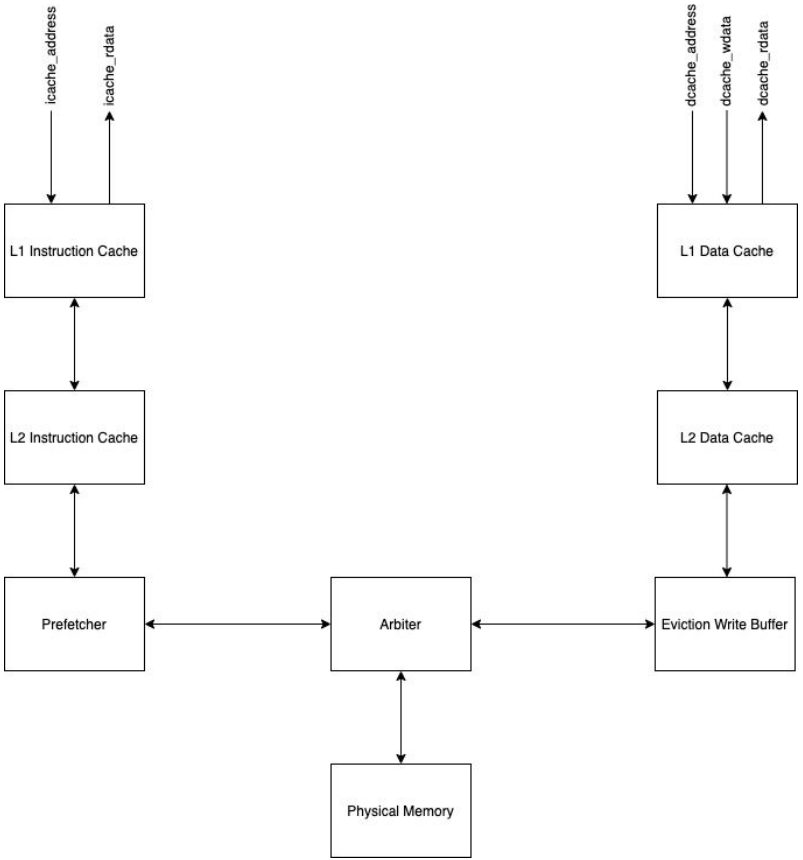
Advanced feature we implemented across all checkpoints:

- L2 Cache System
- 4-way Associative Cache
- Local Branch History Table, Global Branch History Table, Tournament Branch Predictor
- RISC-V M Extension,
- Eviction Write Buffer
- Basic Hardware Prefetching

Data Path Overview



Memory Hierarchy Overview

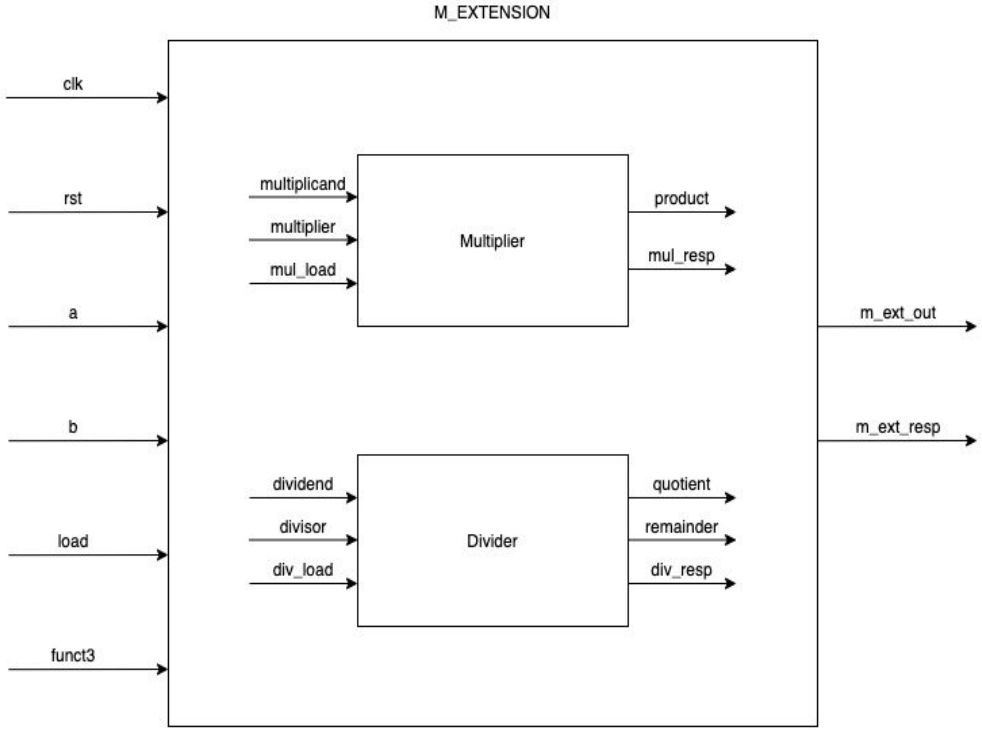


Basic Design Result

5-Stage Pipeline with hazard detection and forwarding unit

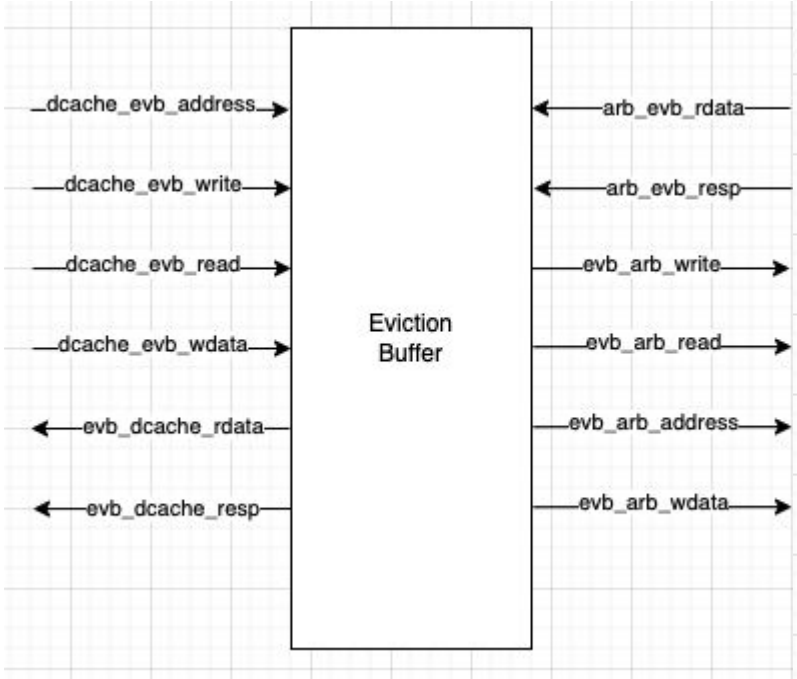
	comp1.s	comp2_i.s	com3.s
Runtime	2,189,325 ns	6,214,575 ns	4,152,265 ns

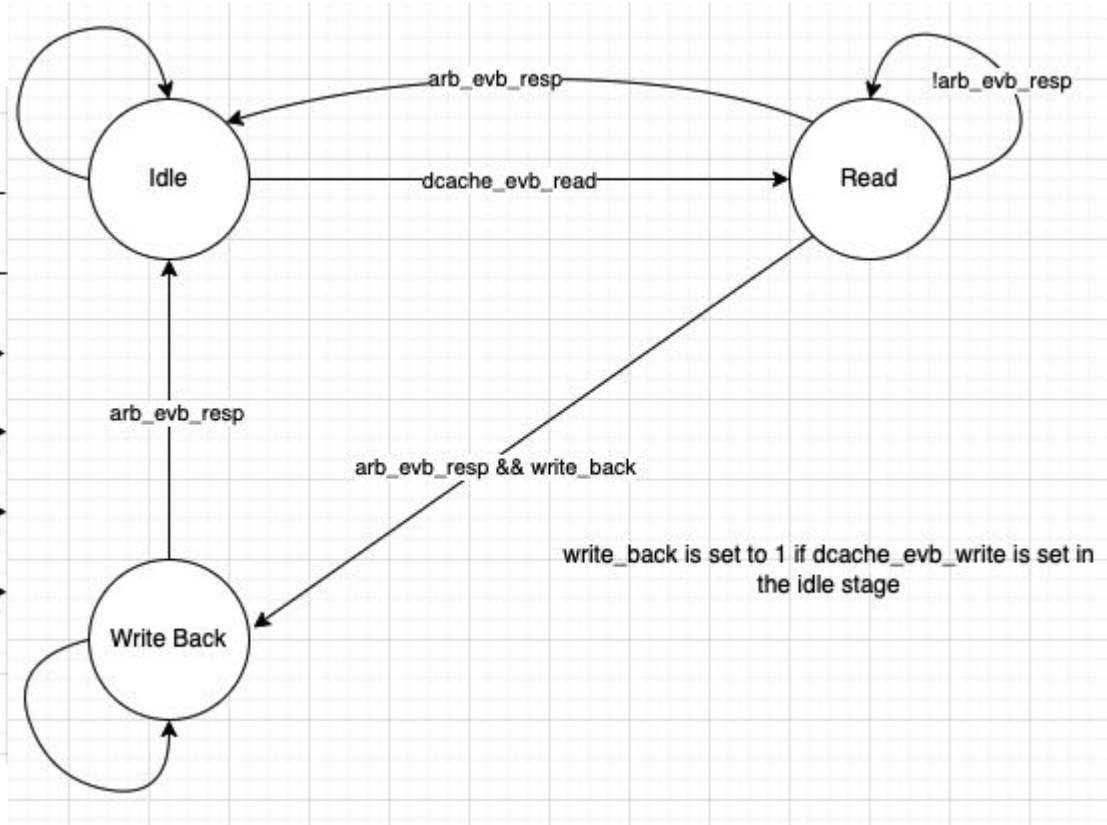
M Extension



funct3	Action
0	signed multiplication -> output product[31:0]
1	signed multiplication -> output product[63:32]
2	signed * unsigned -> output product[63:32]
3	unsigned multiplication -> output product[63:32]
4	signed quotient division
5	unsigned quotient division
6	signed remainder division
7	unsigned remainder division

Eviction Buffer





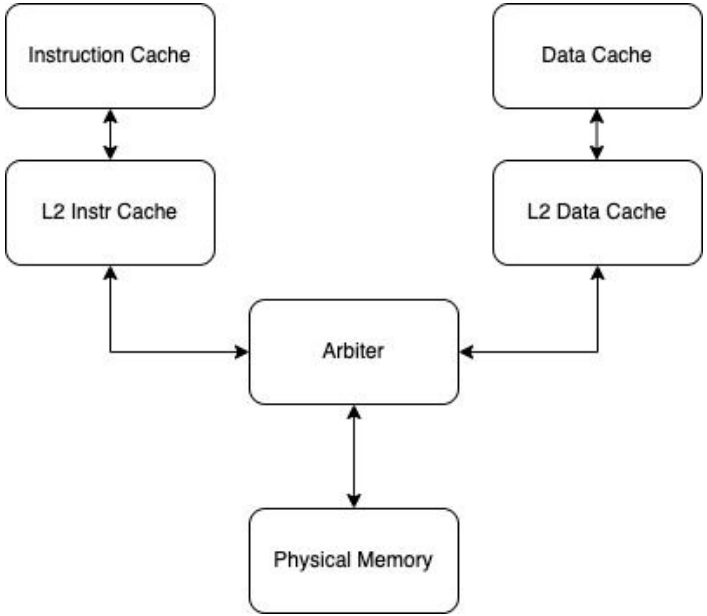
Eviction Buffer Result

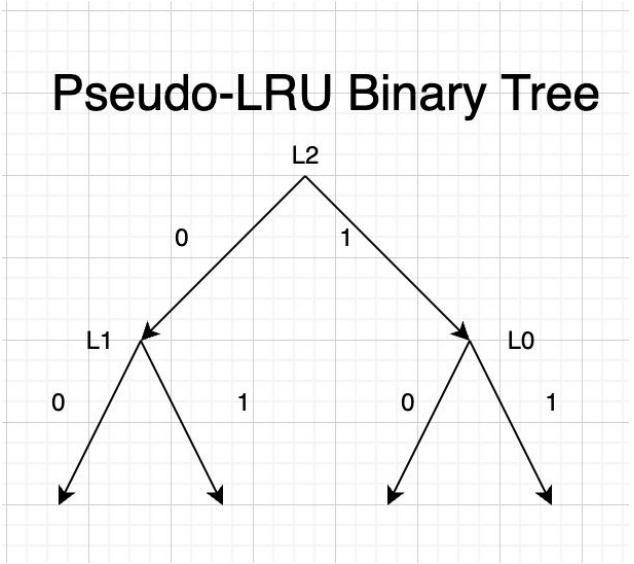
	comp1.s	comp2_i.s	com3.s
Used times	7 times	260 times	728 times
Runtime	2,189,395ns	6,205,925 ns	4,151,605 ns

M Extension Result

	comp2_i.s	comp2_m.s
Used times	0 times	1,733 times
Runtime	6,214,575 ns	792,365 ns

Advanced Cache



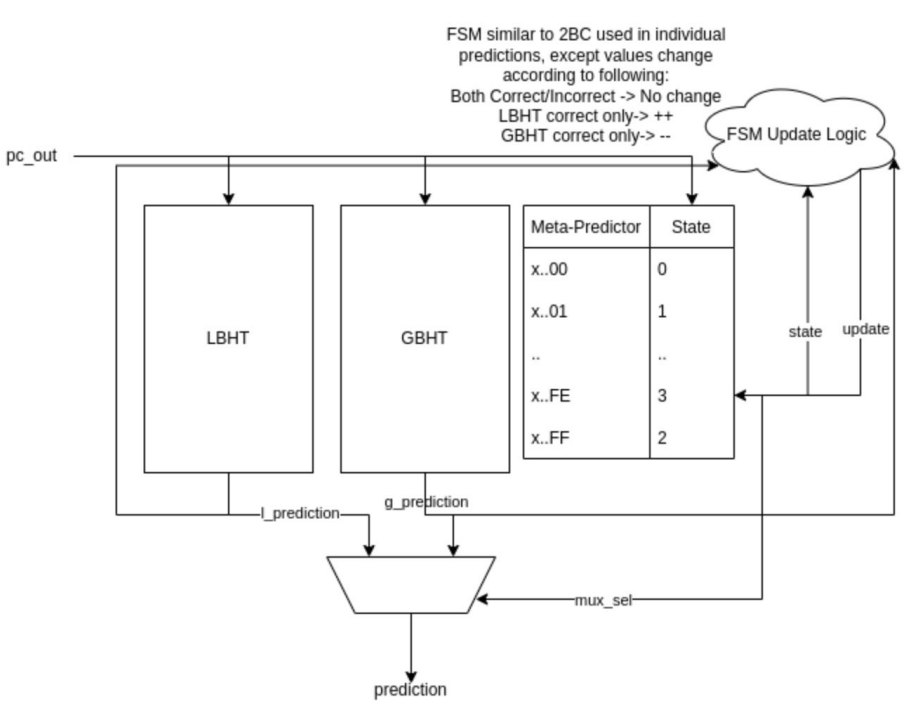


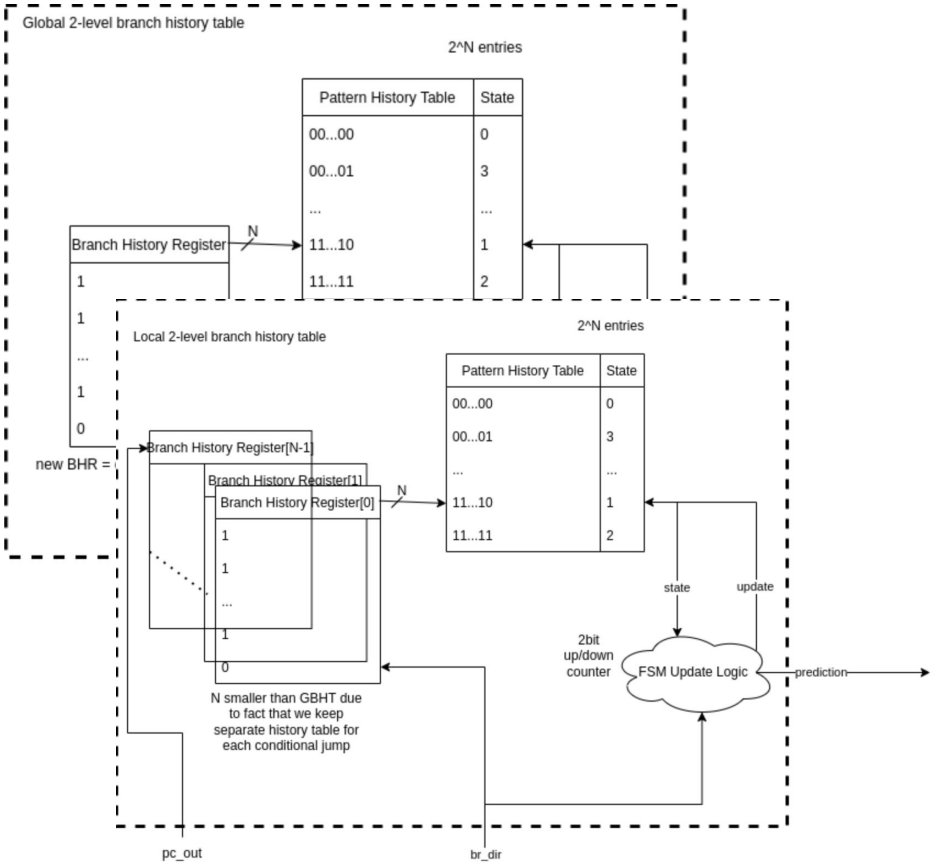
Advanced Cache Result

w/o L2	comp1.s	comp2_i.s	com3.s
hit/miss times	instr: 57,780 / 25 data: 3841 / 7	instr: 135,240 / 76 data: 7088 / 24	instr: 65,450 / 33 data: 13,410 / 283
Runtime	587,835 ns	1,388,755 ns	668,845 ns

w/ L2	comp1.s	comp2_i.s	com3.s
L1 hit/miss times L2 hit/miss times	instr: 57,794 / 25 data: 3845 / 7 instr: 57,818 / 25 data: 3852 / 7	instr: 135,282 / 76 data: 7090 / 24 instr: 135,358 / 76 data: 17,129 / 24	instr: 66,016 / 33 data: 13,410 / 283 instr: 66,049 / 33 data: 13,693 / 283
Runtime	588,465 ns	1,390,685 ns	675,155 ns

Tournament Branch Predictor Design

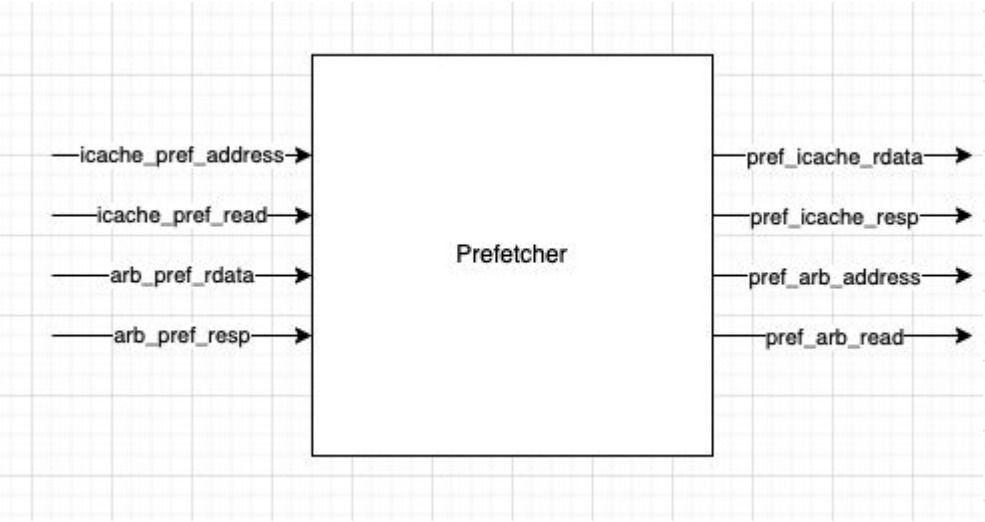


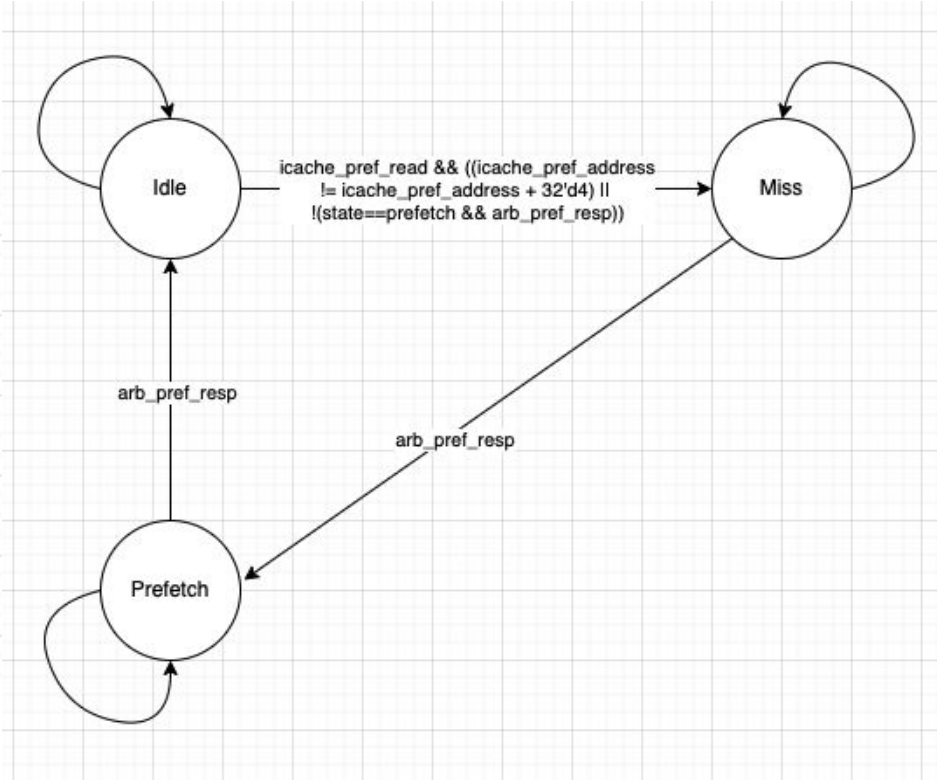


BP Result

	comp1.s	comp2_i.s	com3.s
1 - Flush rate	1-2176/7134=0.705	1-8056/27043=0.702	1-135/2615=0.945
Runtime	2,186,755 ns	6,215,415 ns	4,150,355 ns

Basic Hardware Prefetcher





Basic Hardware Prefetcher Result

	comp1.s	comp2_i.s	com3.s
Used times	4,105 times	10,817 times	8,003 times
Runtime	3,081,845 ns	8,420,365 ns	6,140,515 ns

What we can do differently

-BRAM recommended for speed in L1 cache, but very hard to implement due to inflexibility of design -> Make design more flexible and able to handle clock cycle changes.

-Stage registers we created must reserve space for all signals we need throughout all 5 stages -> Modularizing and making specific registers may conserve space on the chip.

-Our design made the combinational logic for PC very long, which impacted performance -> Although we added a fix, an alternate design may have decreased our times for the test code.

What we can do differently (c.)

-For M Extension, we can try more complicated algorithm such as Wallace Tree instead of simple Add_Shift Multiplier, Substract_Shift Divider

-We wished we could have gotten rvfi monitor working -> fixing our halt and commit signal early on could have aided in our debugging processes.

-4-way L1 cache takes up lots of space- > 2-way L1 instead of 4-way L1 to decrease the overall size of design and increase clk cycle frequency.

Final Design result

Advanced feature: M Extension, 4-way set associative cache

FMAX	81.02MHz
Power Consumption	644.33 mW

	comp1.s	comp2_m.s	com3.s
Runtime	587,835 ns	564,205 ns	668,845 ns

Q&A