Determining the junction temperature in a semiconductor package, part III the use of the junction-to-board thermal characterization parameter

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In recent issues, this column has dealt with the use of a number of thermal metrics to calculate the junction temperature of integrated circuits under various conditions. These metrics explored were θ_{JA}, θ_{JC}, and Ψ_{JT}. To summarize the uses of these metrics:

- θ_{JA} represents the junction-to-air thermal resistance for a package tested in an industry-standard test environment. It is useful in determining changes in thermal performance due to design changes and for ranking package thermal performance. θ_{JA} is of limited value in predicting the junction temperature in an application.
- θ_{JC} , the junction-to-case thermal resistance, is useful in predicting the junction temperature when a package has a heat-sink mounted on top of it.
- Ψ_{JT} , the junction-to-top of package thermal characterization parameter, is used to determine the junction temperature of a chip in an existing system from a measurement of the temperature on the top of the package.

None of these metrics is useful in predicting the junction temperature in a semiconductor package without a heat sink in an actual system. When there is no heat sink, the primary heat flow path for a surface-mounted package is typically though the PCB. Hence, this situation requires a thermal metric relating the junction and the board temperatures.

The recently specified θ_{JB} thermal resistance metric [1,2] is measured under conditions in which nearly all of the heat is flowing to the board. It is useful in the analysis of actual systems when it is used as a component in a thermal resistor network defining the other heat flow paths.

The thermal characterization parameter Ψ_{JB} [1,3] is measured under conditions more typical of actual applications -- namely with most of the heat flowing through the board, but a non-negligible portion of it flowing from the top of the package to the air. Hence, it is a stand-alone parameter that can be quite useful in predicting the junction temperature from a measurement of the board temperature. Ψ_{JB} is defined as

$$\Psi_{JB} = T_J - T_B / P$$

where the board temperature, T_B , is measured just beyond the package edge, along its centerline, preferably by soldering a type T thermocouple to the appropriate trace on the board. P represents the total power dissipated on the device.

The value of Ψ_{JB} for a particular package depends upon many factors in the package design. These factors will not be explored here. However, some insight into to behavior of Ψ_{JB} for a popular package format can be derived from examining the graph top right. This graph demonstrates the relationship between Ψ_{JB} and θ_{JA} , a much more widely known parameter, for a family of 35 mm PBGA packages of varying thermal performance.

The graph indicates that, for this particular group of packages $\square_{JA}$, varies from 12 to 25°C/W. Ψ_{JB} has a linear relationship with respect to $\square_{JA}$ and varies between 5 and 19°C/W. This behavior is consistent with the fact that the dominant heat flow path is from the junction to the board to the air. Since Ψ_{JB} characterizes the thermal efficiency of this path, a reduction in Ψ_{JB} is manifested as an equivalent reduction in $\square_{JA}$.

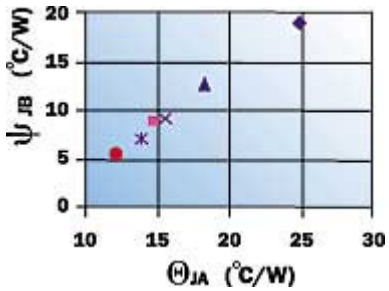

Figure 1. Ψ_{JB} versus $\square_{JA}$ for a family of 35 mm PBGA packages of varying construciton. Packages mounted to JEDEC-standard test board. Natural convection conditions.

The following Table illustrates how Ψ_{JB} can be used to predict the maximum power for a device, consistent with the maximum allowable junction temperature and the board temperature. In this hypothetical example Ψ_{JB} equals 15°C/W.

Predicted Power in Application based on Ψ_{JB} = 15°C/W						
T_{Board} (°C)	$T_{J,Max}$ (°C)					
	90	100	110	120	130	140
	Maxium Allowable Power (W)					
50	2.7	3.3	4.0	4.7	5.3	6.0
60	2.0	2.7	3.3	4.0	4.7	5.3
70	1.3	2.0	2.7	3.3	4.0	4.7
80	0.7	1.3	2.0	2.7	3.3	4.0
90	0.0	0.7	1.3	2.0	2.7	3.3
100	N/A	0.0	0.7	1.3	2.0	2.7

In this table, the maximum allowable power for a given combination of $T_{J,Max}$ and T_B is located at the intersection between the column and row associated with the values of interest. The difference between $T_{J,Max}$ and T_B can be defined as the thermal budget for the package. The allowable power depends linearly on the thermal budget available to the package. Here it ranges from a minimum of 0W to a maximum of 6.0W -- for an unusually large thermal budget.

This table makes it very clear that the maximum power possible in a package depends on three factors: $T_{J,Max}$, which is specified by the semiconductor producer; T_B, which is controlled by the system house; and Ψ_{JB}, which is determined by the chip and package design.

It is rare for the semiconductor producer or the package provider to know T_B . However, such a table can be the start of a three-way dialog in which the impact of the board temperature on the maximum allowable power is defined. This, in turn, can help facilitate informed decisions regarding cost/performance tradeoffs between packaging choices and system design.

References

1. Bennet Joiner, "Use of Junction-to-Board Thermal Resistance in Predictive Engineering," Electronics Cooling Magazine, Vol.5, No. 1, (January, 1999), pp. 14-17.
2. JEDEC Standard, "Integrated Circuits Thermal Test Method Environmental Conditions - Junction-to_Board," EIA/JESD51-8. [Available for downloading at www.jedec.org at no charge.]
3. JEDEC Standard, "Integrated Circuits Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)," EIA/JESD51-6.