Taking A Closer Look At Doherty Amplifiers

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Contents:

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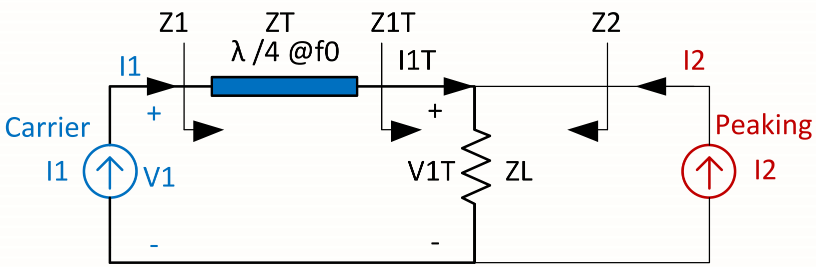
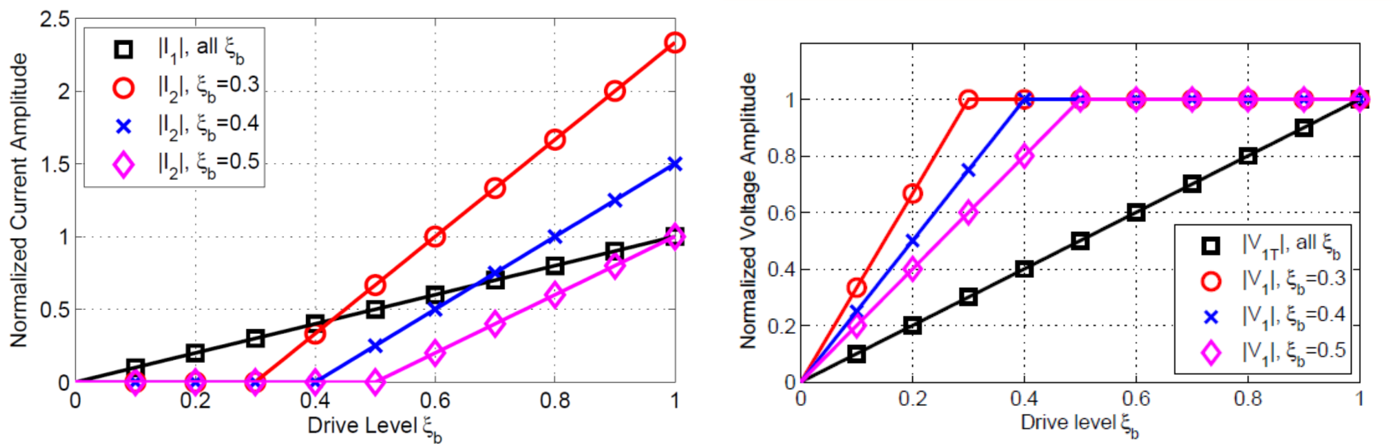
Center Frequency Analysis of Ideal Doherty PA

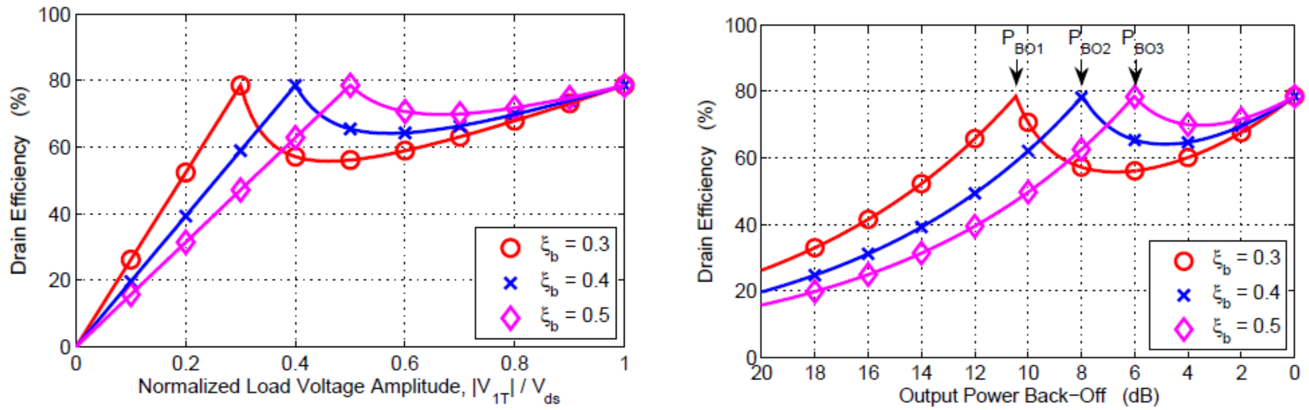
MACOM



$$I_1 = \xi \cdot \frac{I_{max1}}{2}$$

$$I_2 = \begin{cases} 0, & 0 < \xi < \xi_b \\ \frac{I_{max1}}{2} \cdot \frac{\xi - \xi_b}{\xi_b} \cdot e^{-j\theta}, & \xi_b < \xi < 1 \end{cases}$$





(a) (b)

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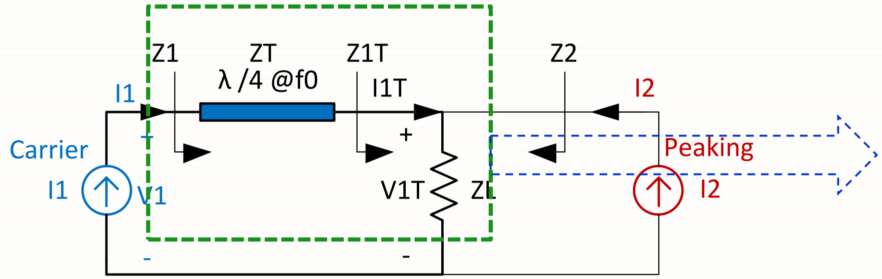
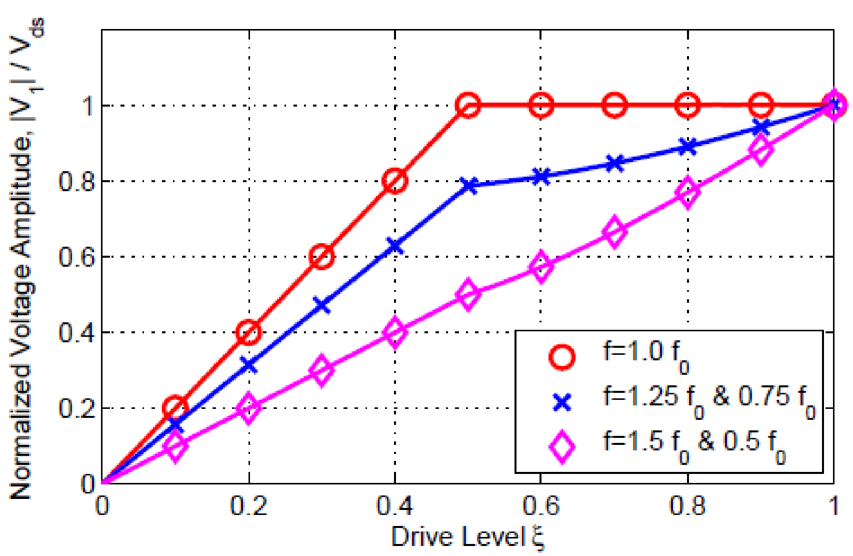
Frequency Response of Ideal Doherty PA(1)

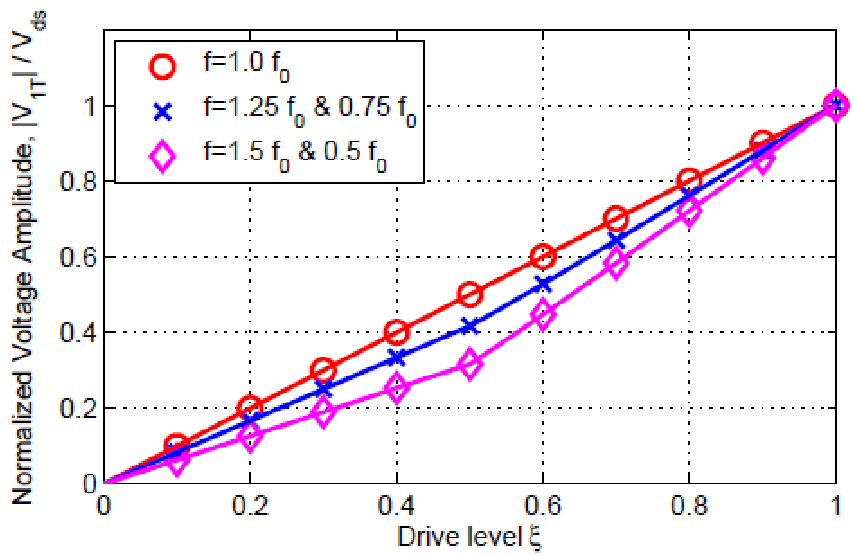


$$Z=\begin{bmatrix} Z_T\cdot\dfrac{Z_L\cdot\cos(\theta)+j\cdot Z_T\cdot\sin(\theta)}{Z_T\cdot\cos(\theta)+j\cdot Z_L\cdot\sin(\theta)} & \dfrac{Z_T\cdot Z_L}{Z_T\cdot\cos(\theta)+j\cdot Z_L\cdot\sin(\theta)} \\ \dfrac{Z_T\cdot Z_L}{Z_T\cdot\cos(\theta)+j\cdot Z_L\cdot\sin(\theta)} & \dfrac{Z_T\cdot Z_L\cdot\cos(\theta)}{Z_T\cdot\cos(\theta)+j\cdot Z_L\cdot\sin(\theta)} \end{bmatrix}$$

$$\mathrm{V1}=\begin{cases} \mathrm{V_{ds}}\cdot\left(\dfrac{\xi\cdot\xi_b\cdot\cos(\theta)+j\cdot\xi\cdot\sin(\theta)}{\cos(\theta)+j\cdot\xi_b\cdot\sin(\theta)}\right), 0<\xi<\xi_b \\ \mathrm{V_{ds}}\cdot\left(\dfrac{\xi\cdot\xi_b\cdot\cos(\theta)+j\cdot\xi\cdot\sin(\theta)}{\cos(\theta)+j\cdot\xi_b\cdot\sin(\theta)}\right), \xi_b<\xi<1 \end{cases}$$

$$\mathrm{V1T}=\begin{cases} \mathrm{V_{ds}}\cdot\left(\dfrac{\xi\cdot\xi_b}{\cos(\theta)+j\cdot\xi_b\cdot\sin(\theta)}\right), & 0<\xi<\xi_b \\ \mathrm{V_{ds}}\cdot\left(\dfrac{\xi\cdot\xi_b+(\xi-\xi_b)\cdot\cos(\theta)\cdot(\cos(\theta)-j\cdot\sin(\theta))}{\cos(\theta)+j\cdot\xi_b\cdot\sin(\theta)}\right), & \xi_b<\xi<1 \end{cases}$$





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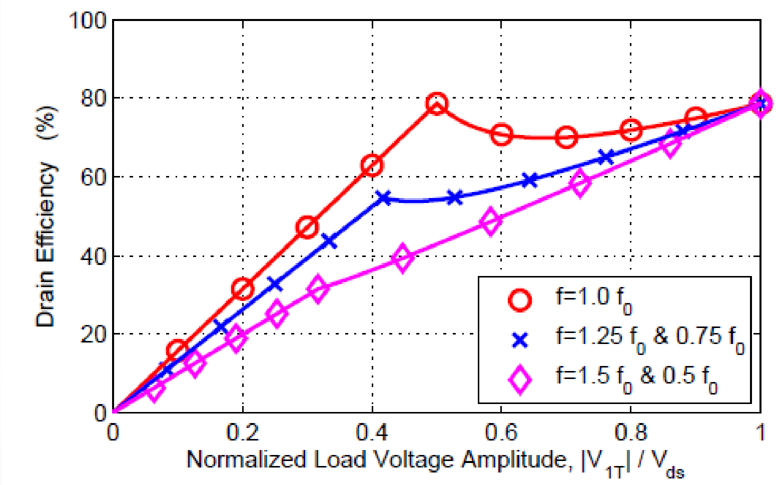
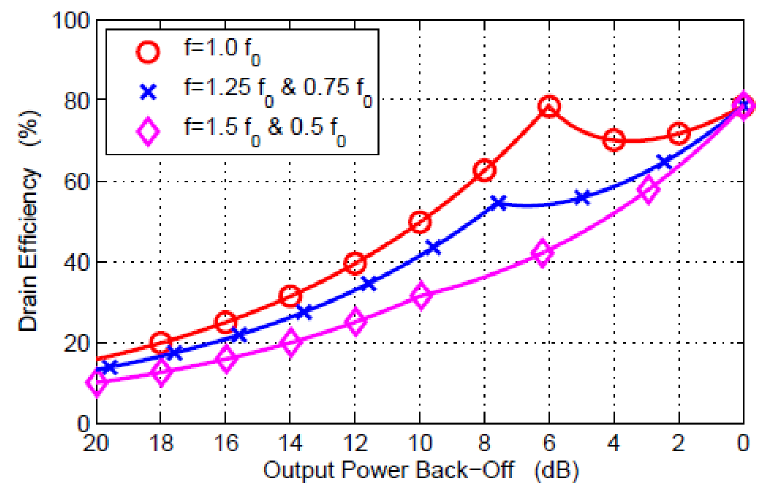
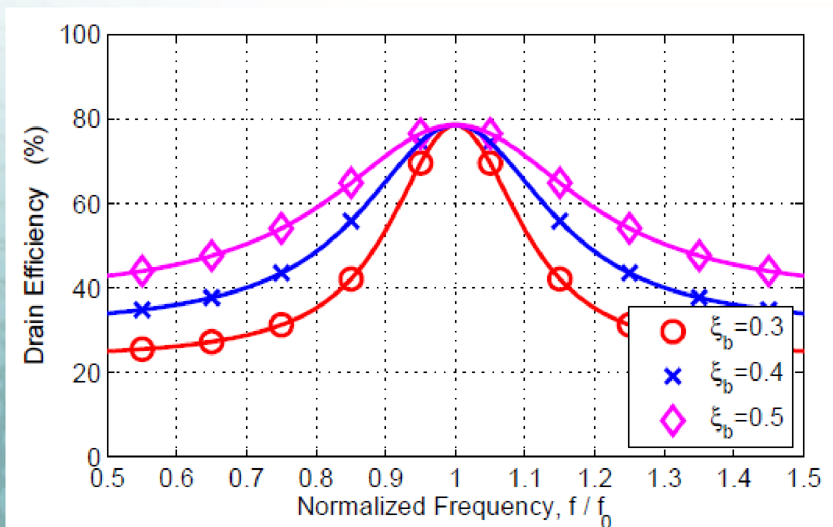
Frequency Response of Ideal Doherty PA(2)

Frequency Response of Symmetrical Ideal Doherty





The more BO is, the narrower BO efficiency bandwidth is



ξ_b	P_{bo}	$BW_{\eta-1dB}$
0.30	10.5 dB	14%
0.35	9.1dB	18%
0.40	8.0 dB	23%
0.45	6.9 dB	28%
0.50	6.0 dB	34%

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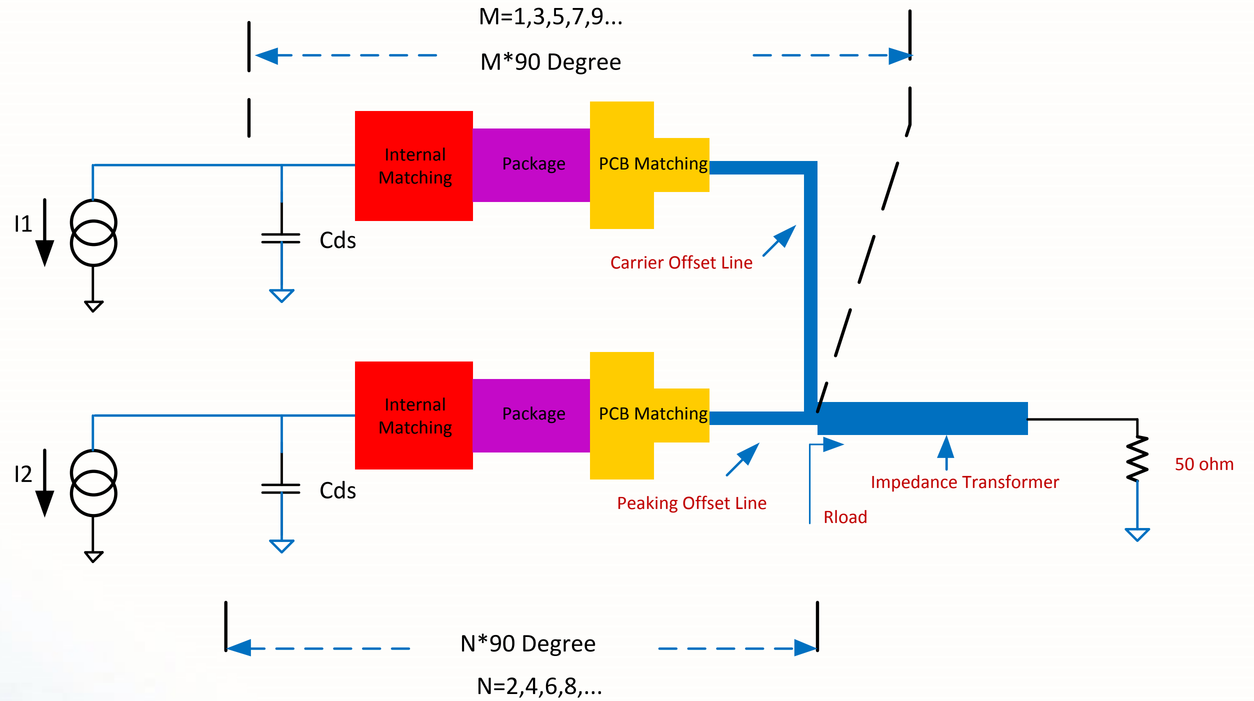
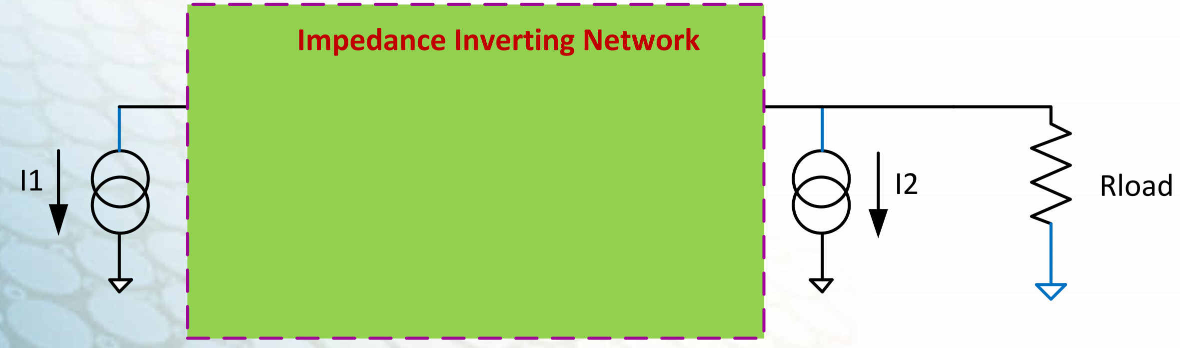
A Real Doherty Circuit Diagram

Low Frequency Doherty Using Discrete Transistor



In MMIC design, Choose M=1,N=0

High Frequency MMIC Doherty Design



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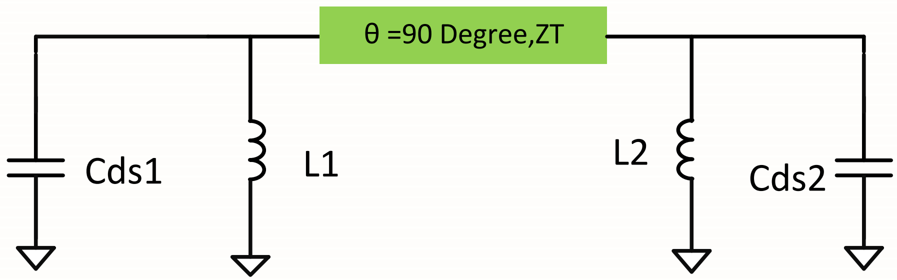
Topologies Of Impedance Inverting Network (1)

Impedance Inverting Network

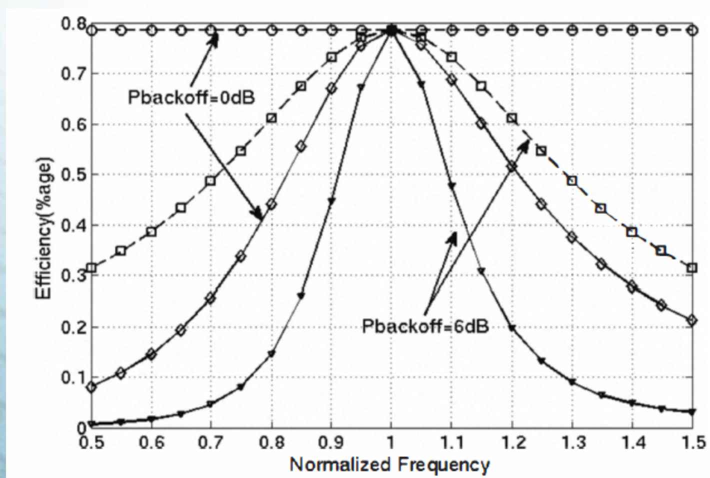


Shunt L Topology

1. For MMIC Design, For low or medium power, ZT will larger than 100 ohm, The strip line on die is difficult to be realized

2. L1 and L2 are very difficult to be realized because of DC current handling;

3. Reduce the bandwidth;



Dash Line: DPA without Cds;
Solid Line: DPA with Cds and using Shunt L

EFF VS Freq. of DPA

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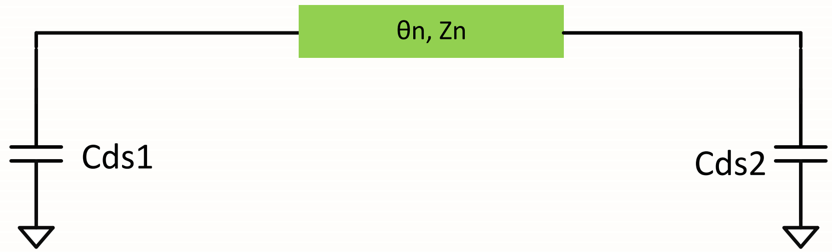
Topologies Of Impedance Inverting Network (2)

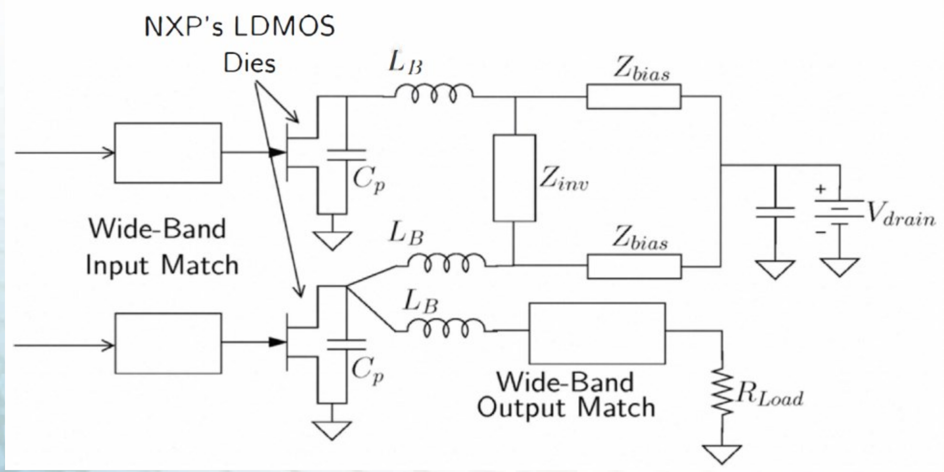
Impedance Inverting Network



Quasi-lumped network

$$\theta_n = \arccos(\omega_0 \cdot C_{out} \cdot Z_T) \qquad Z_n = \frac{Z_T}{\sin(\theta_n)}$$

1. The topology can absorb the Cds and bond wires into the impedance inverter;
2. When Z_T is high, Z_n is very small, maybe difficult to realize
3. Additional Bias network is needed



Reference: J. Qureshi, N. Li, W. Neo, F. van Rijs, I. Blednov, and L.de Vreede, “A Wide-Band 20W LMOS Doherty Power Amplifier,” in 2010 IEEE MTT-S Int. Microwave Symp. Dig., may 2010, pp. 1504-1507.

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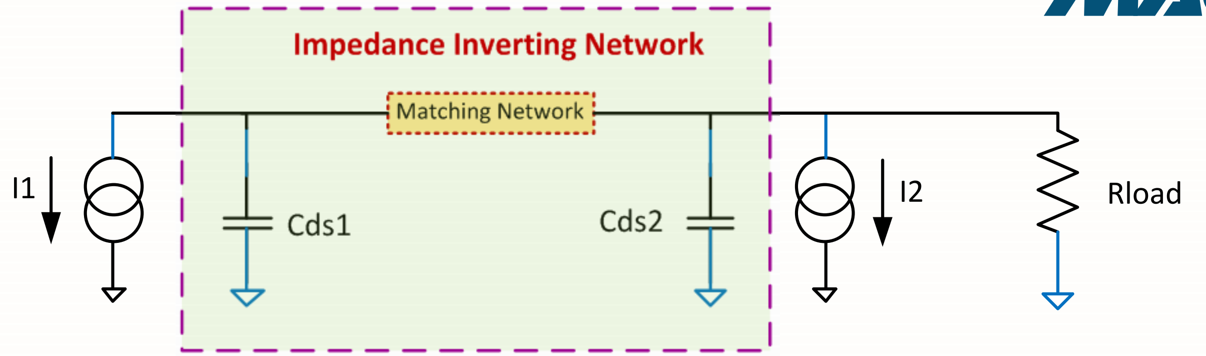
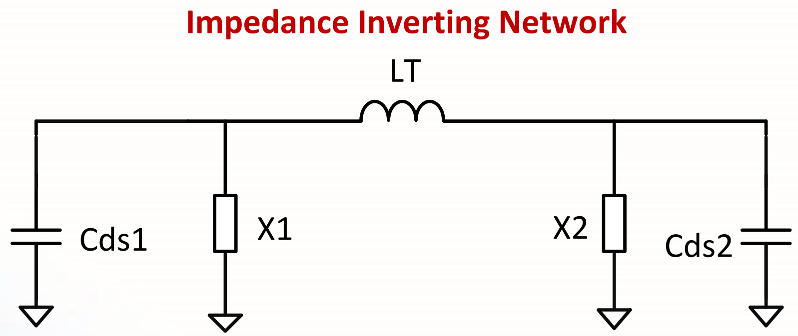
Topologies Of Impedance Inverting Network (3)





π network

$$X_i = \frac{1}{\omega_0 \cdot (C_{out,i} - C_T)}$$

$$C_T = \frac{1}{\omega_0 \cdot Z_T} \qquad L_T = \frac{Z_T}{\omega_0}$$

1. L_T maybe too large to be realized in MMIC process

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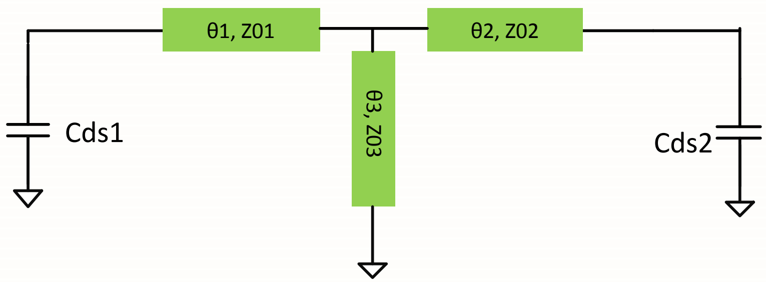
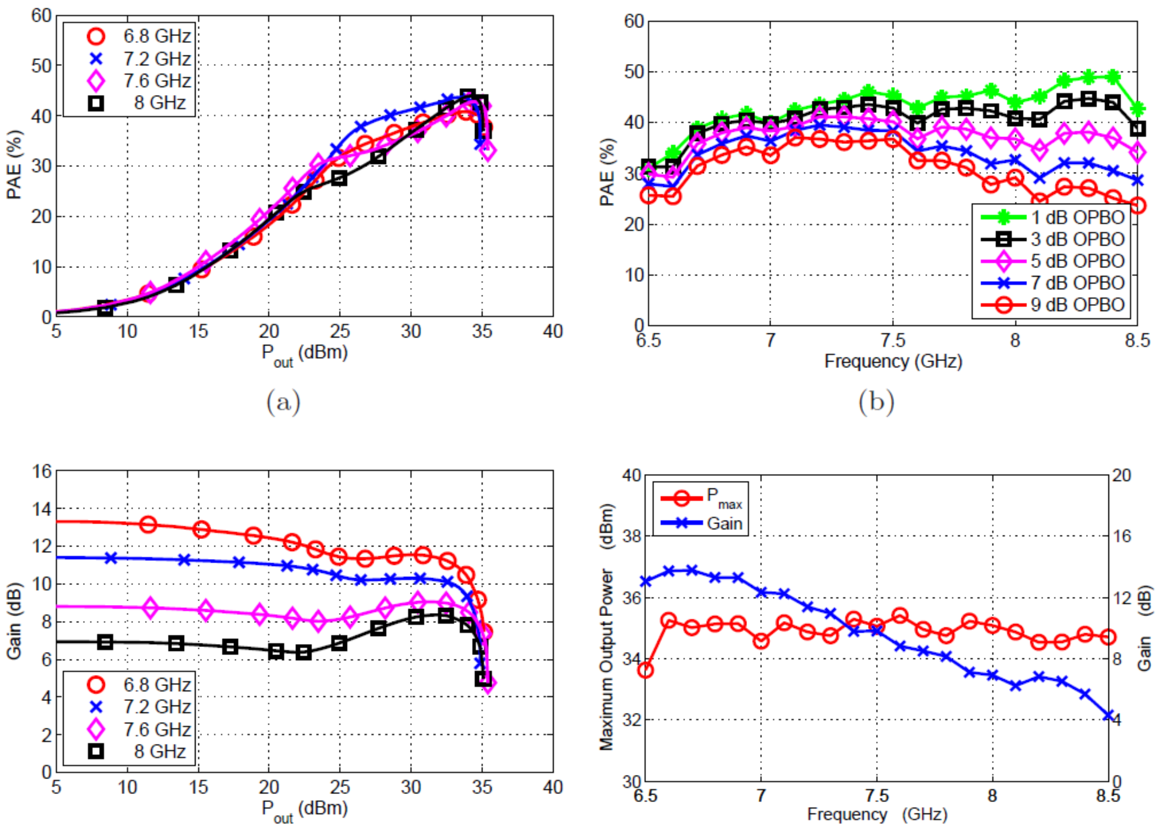
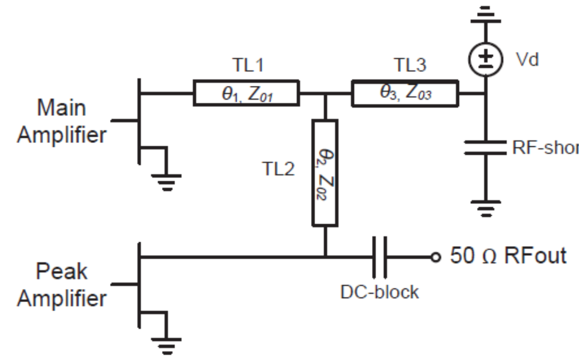
Topologies Of Impedance Inverting Network (4)

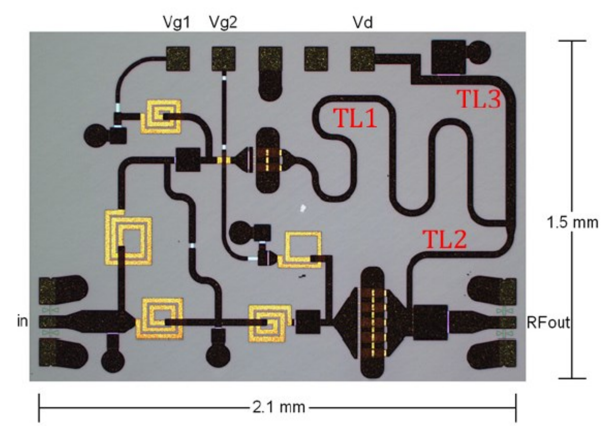
Impedance Inverting Network



T network







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Off State performance of Peaking Amplifier (1)

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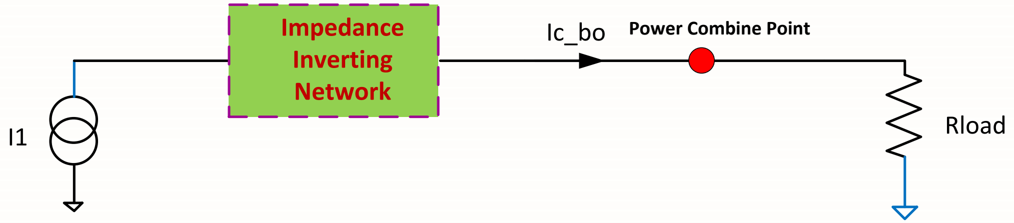
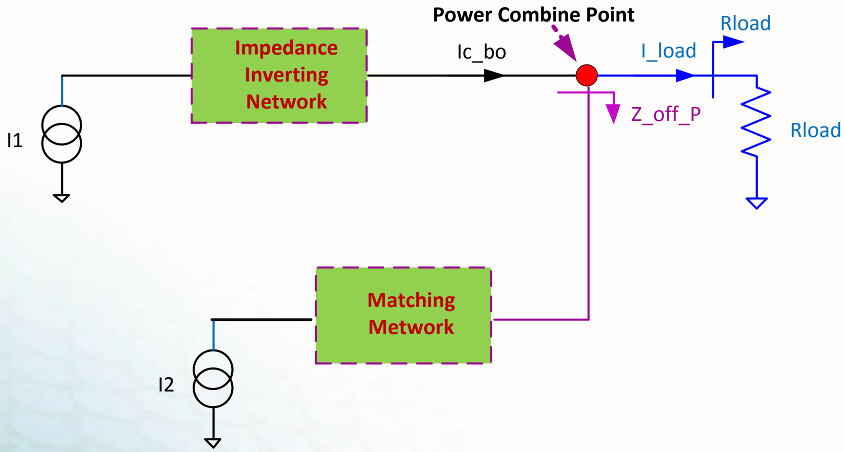
1. When No Off State Peaking Amplifier Connected To The High Load Carrier Amplifier



$$P_L = Ic\_bo^2 \cdot R_{load}$$

2. Then Adding The Off State Peaking Amplifier To The High Load Carrier Amplifier (Assuming Adding Off State Peaking Do Not Affect The Impedance Too Much)



$$I\_load = Ic\_bo \cdot \frac{Z\_off\_P}{Z\_off\_P + R}$$

$$P_L' = Ic\_bo^2 \cdot \left(\frac{Z\_off\_P}{Z\_off\_P + R}\right)^2 \cdot R_{load}$$

3. Then the Transducer Loss can be calculated:

$$TL = 10 \cdot \log\left(\frac{P_L'}{P_L}\right) = 10 \cdot \log\left(\frac{P_L'}{P_L}\right) = 10 \cdot \log\left(\frac{Z_{off_P}}{Z_{off_P} + R}\right)^2 = -20 \cdot \log\left(\frac{Z\_off\_P + R}{Z\_off\_P}\right) = -20 \cdot \log\left(1 + \frac{R}{Z\_off\_P}\right)$$

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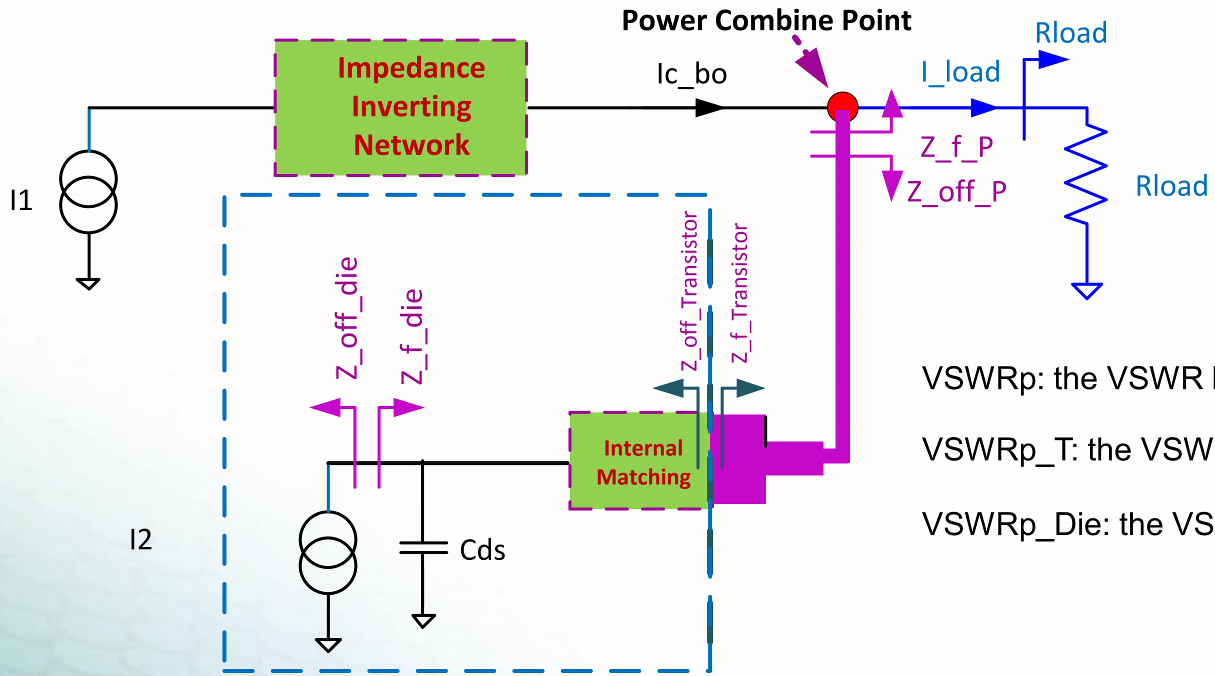
Off State performance of Peaking Amplifier (2)

MACOM

4. The Relationship Between TL, VSWRp and VSWRp_T



VSWRp: the VSWR between Z_f_p and Z_off_P

VSWRp_T: the VSWR between Z_f_Transistor and Z_off_Transistor

VSWRp_Die: the VSWR between Z_f_Die and Z_off_Die

$$\left.\begin{aligned} \mathbf{TL} &= -20\cdot\log\left(1+\frac{\mathbf{R}}{\mathbf{Z\_off\_P}}\right) \\ Z\_f\_p &= \frac{R}{1-\xi_b} \end{aligned}\right\} \Rightarrow \mathbf{TL} = -20\cdot\log\left(1+\frac{(1-\xi_b)\cdot Z\_f\_p}{\mathbf{Z\_off\_P}}\right) = -20\cdot\log\left(1+\frac{1-\xi_b}{\mathbf{VSWRp}}\right)$$

If assuming PCB matching is lossless, then

$$\mathbf{TL} = -20\cdot\log\left(1+\frac{1-\xi_b}{\mathbf{VSWRp\_T}}\right)$$

The VSWRp_T can be called ***the figure of merit*** for off state peak performance

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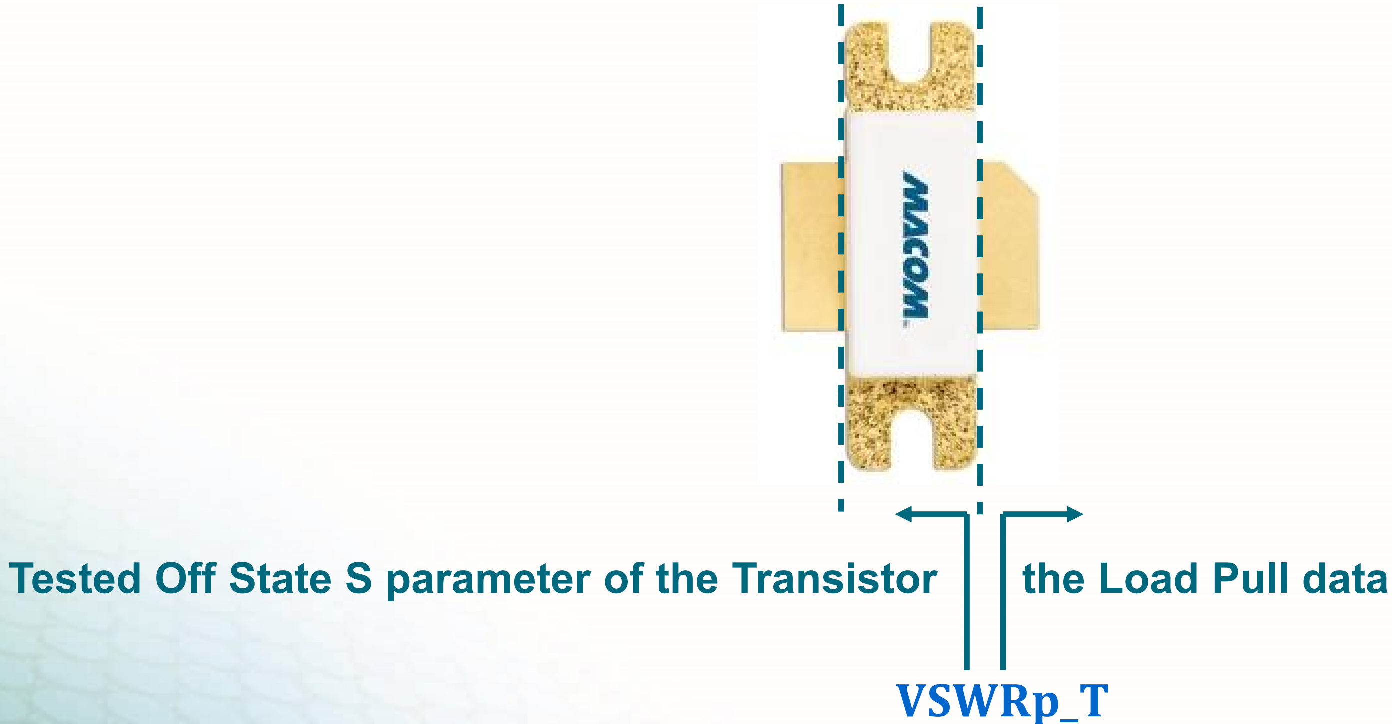
Off State performance of Peaking Amplifier (3)



1. Choosing PCB matching impedance close to the MXP point will get better off state performance
2. Loss between the Die and Power combine point will degrade the off state performance,
So zero phase delay is highly recommended rather than 180 degree phase delay in peaking amplifier design

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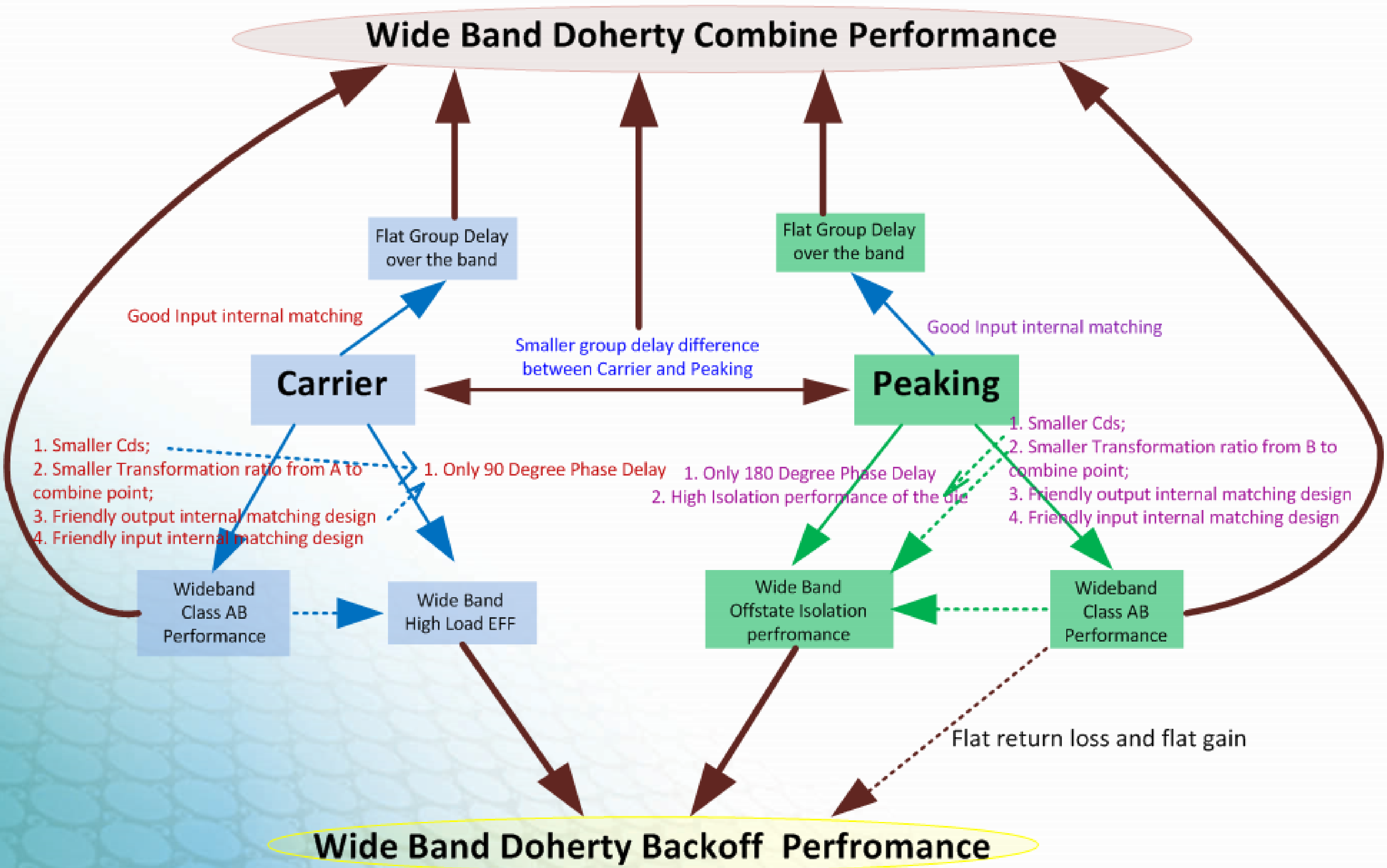
All Factors Matters For Doherty Bandwidth



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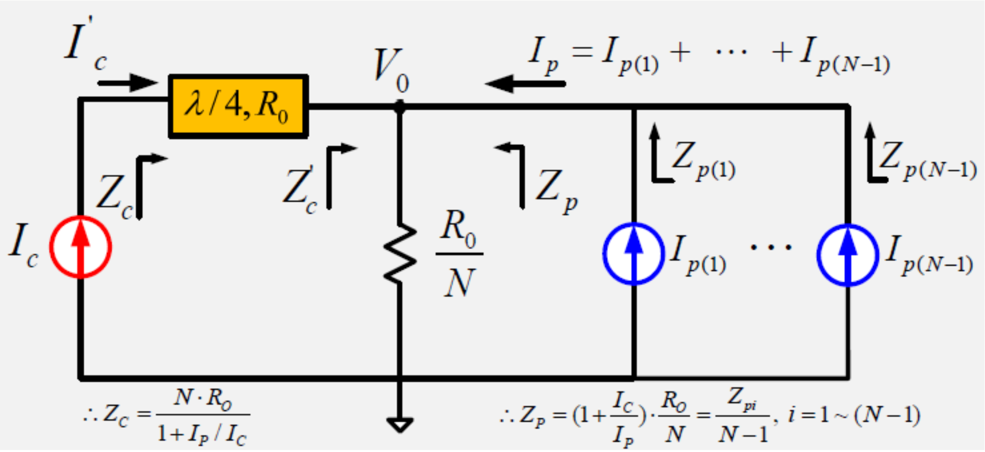
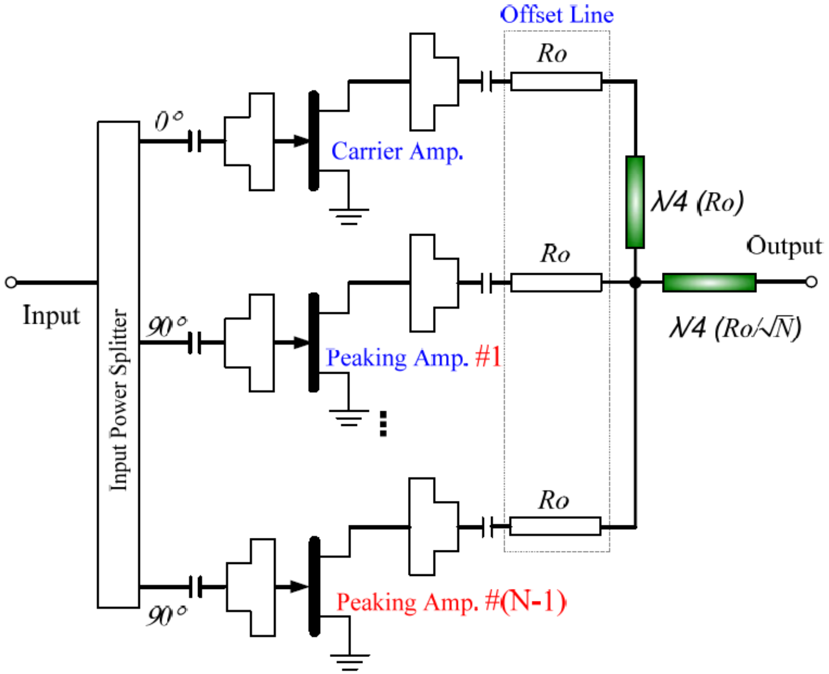
‘N Way’ Doherty





Be called ‘N way’ Doherty

Also be called Asymmetrical Doherty

1. N+1:1 load modulation for Carrier Amplifier
2. All N peaking amplifier be turned on at the same time
3. Bandwidth is limited by the high load modulation
4. EFF will drop a lot between the two MAX EFF points

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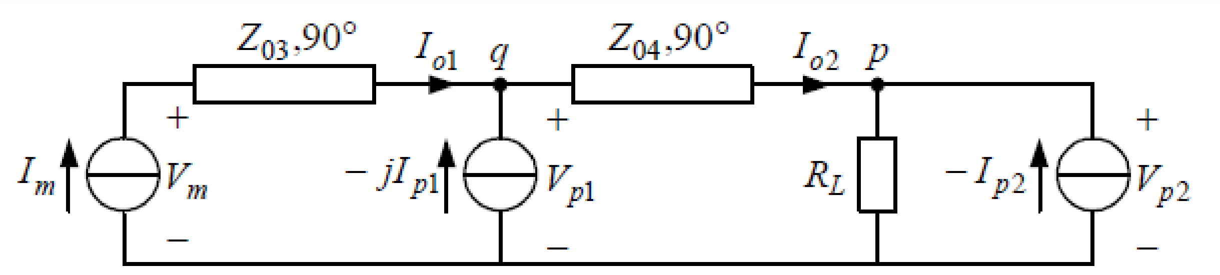
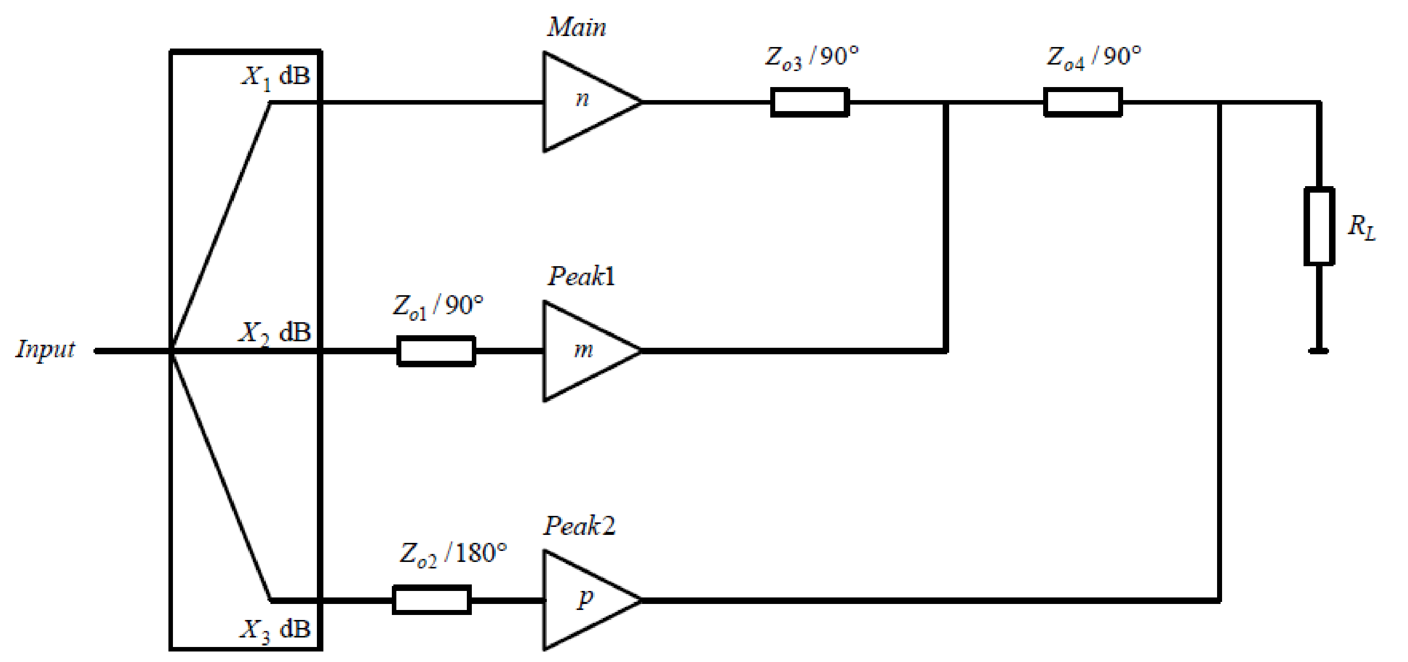
Conventional 3-stage Doherty Amplifier





Can be seen as One Doherty Amplifier + an additional peaking amplifier

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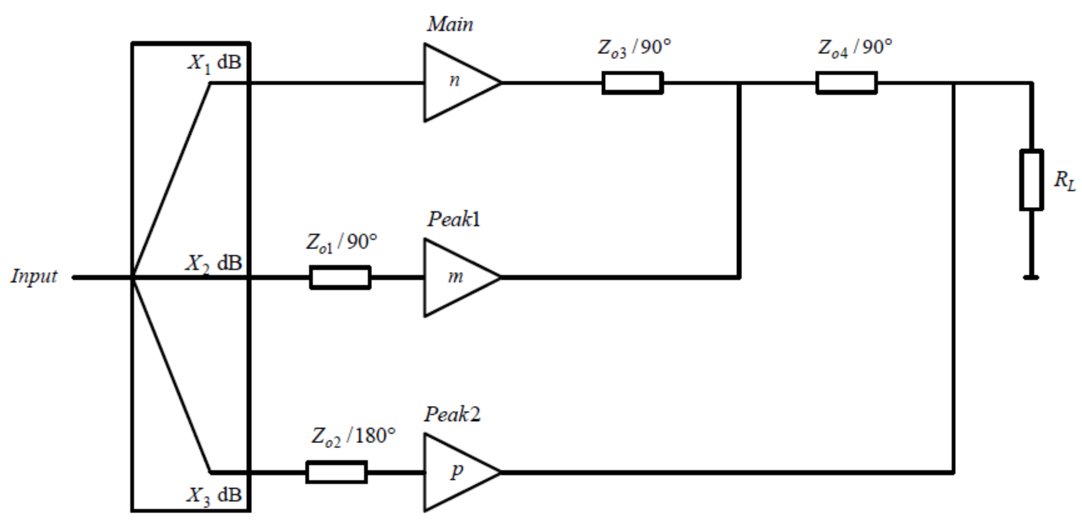
Conventional 3-stage Doherty Amplifier

If the MAX power of the carrier, 1ST peaking and 2ND peaking amplifier are given,
The BO point (k1, k2) can be determined by the following equation:

$$k_2 = \frac{P_{\max\_C}}{P_{\max\_C} + P_{\max\_P1}} \qquad k_1 = \frac{P_{\max\_C} + P_{\max\_P1}}{P_{\max\_C} + P_{\max\_P1} + P_{\max\_P2}} \qquad P_{\max\_C}:P_{\max\_C}:P_{\max\_C} = k_1 k_2 : k_1(1\text{-}k_2) : (1\text{-}k_1)$$



$$Z_{03} = \sqrt{\frac{Z_{mF} \cdot Z_{p1F} \cdot (1 - k_2)}{k_2}}$$

$$Z_{04} = \sqrt{\frac{Z_{p1F} \cdot Z_{p2F} \cdot (1 - k_1) \cdot (1 - k_2)}{k_2}}$$

$$R_L = Z_{p2F} \cdot (1 - k_1)$$

Load line modulation factor of carrier PA is:

$$VSWR = \frac{k_1}{k_2}$$

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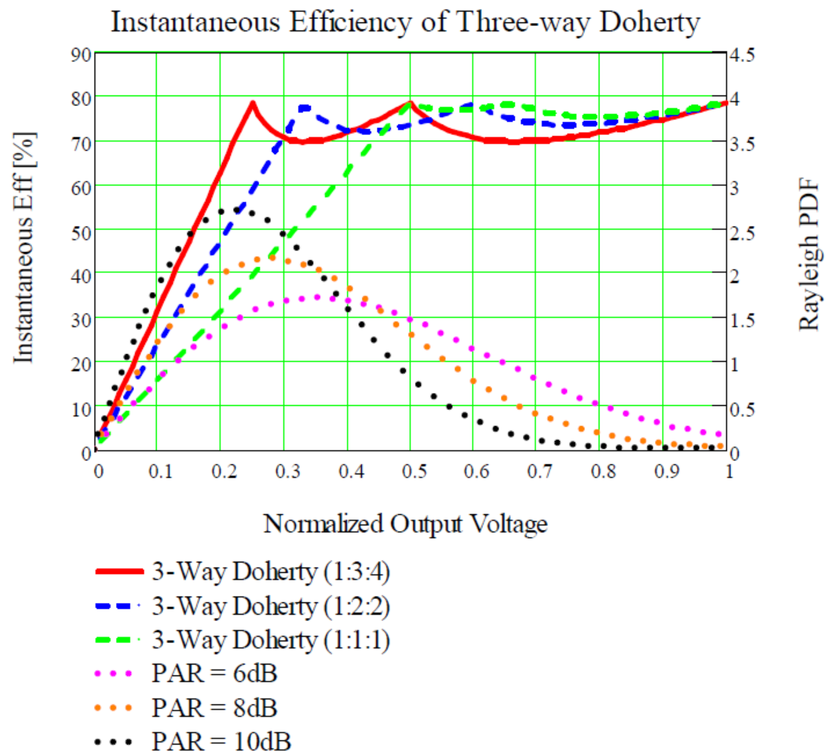
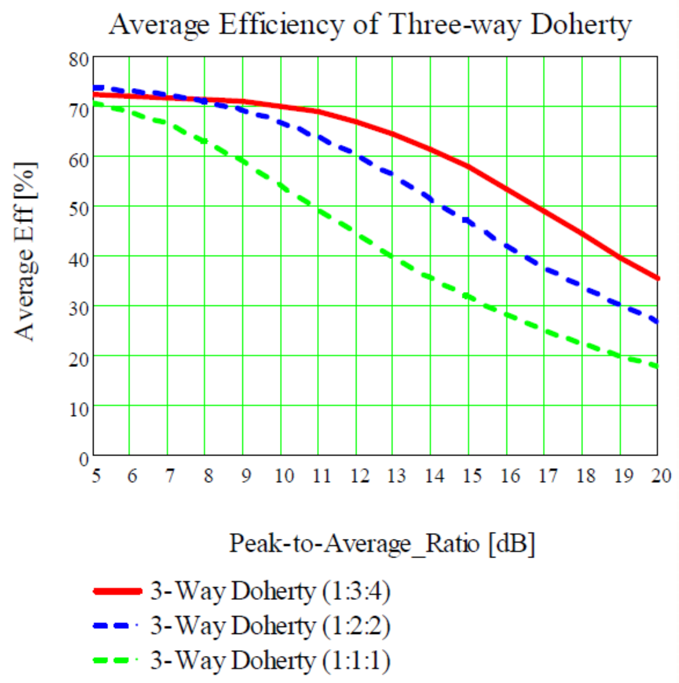
Conventional 3-stage Doherty Amplifier

$R_{mL} = R_{p1L} = R_{p2L} = 50\Omega$

	P_{main}	P_{peak1}	P_{Peak2}	$10\log(k_2^2)$	$10\log(k_1^2)$	Z_{03} Ohm	Z_{04} Ohm	R_L Note 1	VSWR_main
k_1=1/2,k_2=1/4	1	3	4	-12dB	-6dB	86.6	43.3	25	2
k_1=4/7,k_2=1/4	1	3	3	-12dB	-4.9dB	86.6	37.5	21.4	2.3
k_1=3/5,k_2=1/3	1	2	2	-9.5dB	-4.4dB	70.7	33.3	20	1.8
k_1=2/3,k_2=1/2	1	1	1	-6dB	-3.5dB	50	25	16.7	1.33





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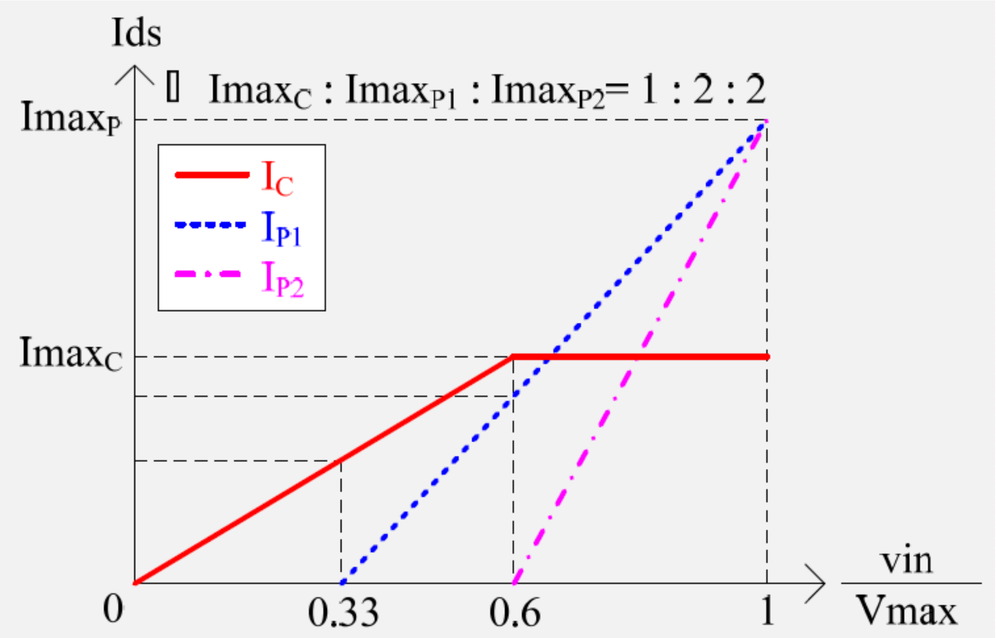
Issues of Conventional 3-stage Doherty Amplifier



1. The load line of Carrier amplifier stops at a certain power level causing heavy saturation of the carrier device, And will also cause gate current flow for GaN HEMT;

2. If better modulated signal back off efficiency achieved than using 2 way Doherty, different size of transistor will Be used in carrier, peaking1 and peaking2 amplifier

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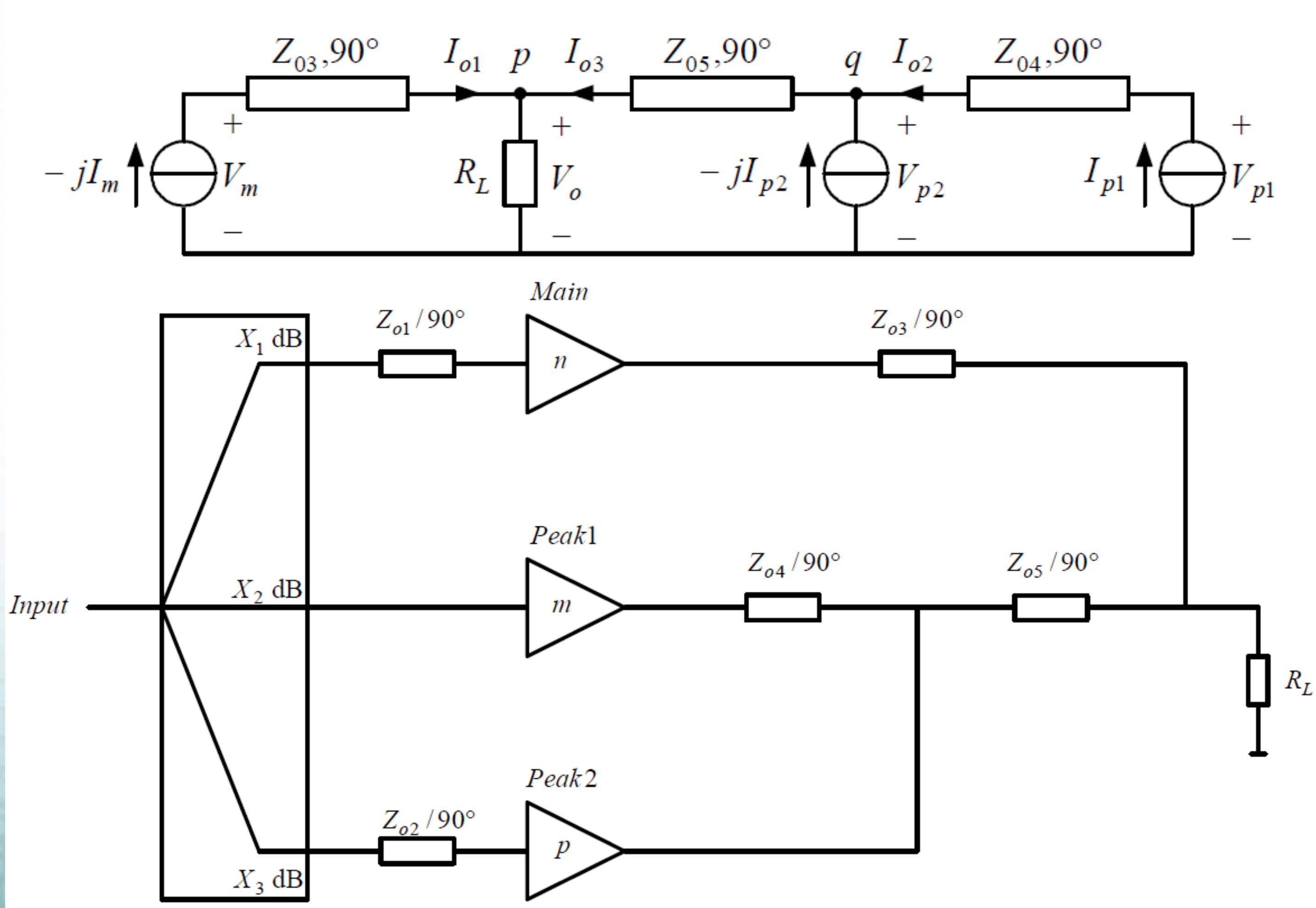
Novel 3-stage Doherty Amplifier



Can be seen as One Carrier Amplifier + an additional Doherty Amplifier working as a peaking amplifier

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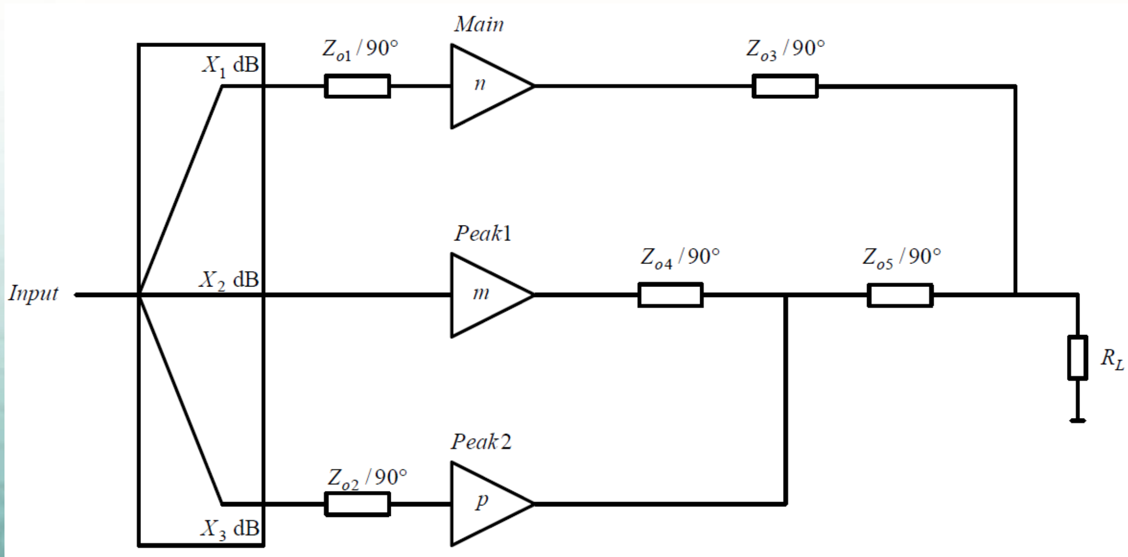
Novel 3-stage Doherty Amplifier

If the MAX power of the carrier, 1ST peaking and 2ND peaking amplifier are given, The BO point (k1, k2) can be determined by the following equation:

$$k_1 = \frac{P_{\max\_p1}}{P_{\max\_p1} + P_{\max\_P2}} \qquad k_2 = \frac{P_{\max\_C}}{P_{\max\_C} + P_{\max\_P1} + P_{\max\_P2}}$$

$$P_{\max\_C}:P_{\max\_p1}:P_{\max\_p2} = k_2 : k_1(1\text{-}k_2) : (1\text{-}k_1)\,(1\text{-}k_2)$$



$$Z_{03} = \sqrt{\frac{R_{L\_f} R_L}{k_2}}$$

$$Z_{05} = Z_{03} \cdot \left(\frac{k_2}{1 - k_2}\right)$$

$$Z_{04} = \frac{R_{L\_f}}{k_1}\left(\frac{k_2}{1 - k_2}\right)$$

Load line modulation factor of carrier PA is:

$$VSWR = \frac{1}{k_2}$$

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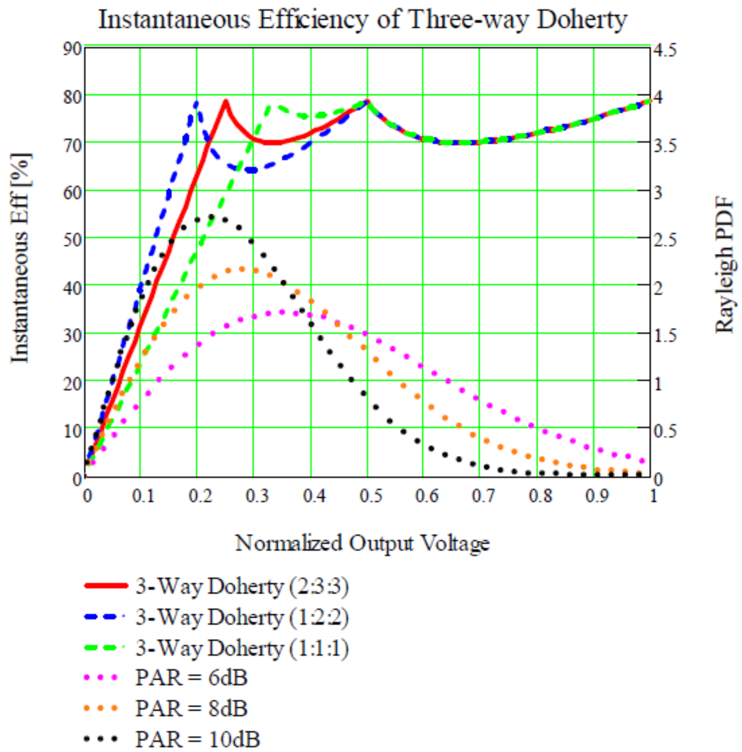
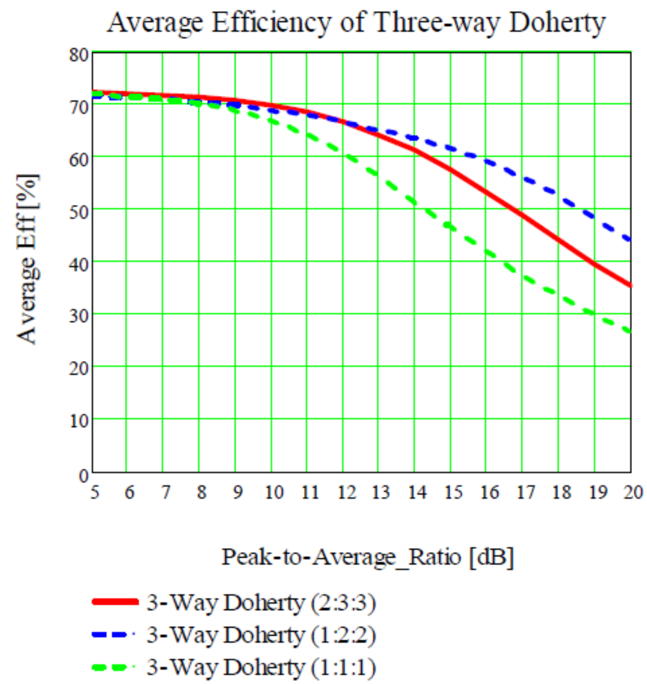
Novel 3-stage Doherty Amplifier

$R_{m\_L} = R_L = 50\Omega$

	P_{M_1dB} (W)	P_{P1_1dB} (W)	P_{P2_1dB} (W)	$10\log(k_2^2)$	$10\log(k_1^2)$	Z_{03} Ohm	Z_{04} Ohm	Z_{05} Ohm	VSWR_main
k_1=1/2,k_2=1/5	(1)	(2)	(2)	-14dB	-6dB	111.8	28	25	5
k_1=1/2,k_2=1/4	(2)	(3)	(3)	-12dB	-6dB	100	33.3	33.3	4
k_1=1/2,k_2=1/3	(1)	(1)	(1)	-9.5B	-6dB	86.6	50.0	43.3	3





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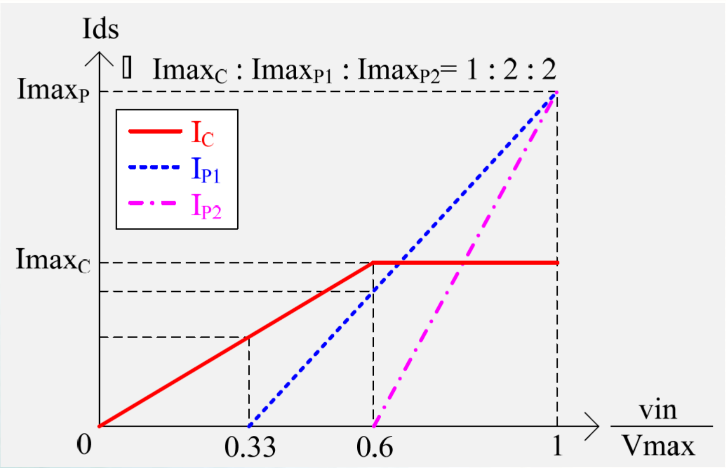
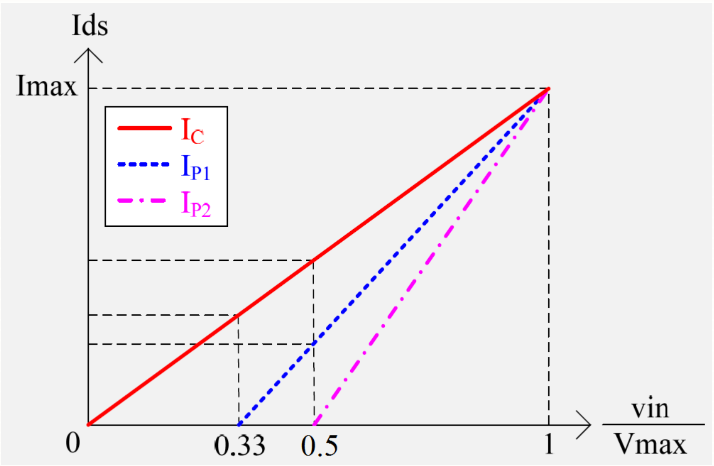
Comparison Between Conventional and Novel 3-stage Doherty Amplifier

1. Principle of working:
   Conventional : Can be seen as One Doherty Amplifier + an additional peaking amplifier
   Novel: Can be seen as One Carrier Amplifier + an additional Doherty Amplifier working as a peaking amplifier

2. Current Variation when input power increase:





Load line modulation factor of carrier PA is:

$$VSWR = \frac{k_1}{k_2}$$

Load line modulation factor of carrier PA is:

$$VSWR = \frac{1}{k_2}$$

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Overview of Doherty Design Template

Very useful tool for designers who design package asymmetrical Doherty transistors

Sub Modules in the Template

A

Doherty Structure

1. Die Selection Tool;
2. Doherty Design Tool;
3. Doherty HB Simulation module

B

Transistor Design

1. Internal input and output matching design
2. Active transistor model build
3. Simulated and tested Load pull data analysis

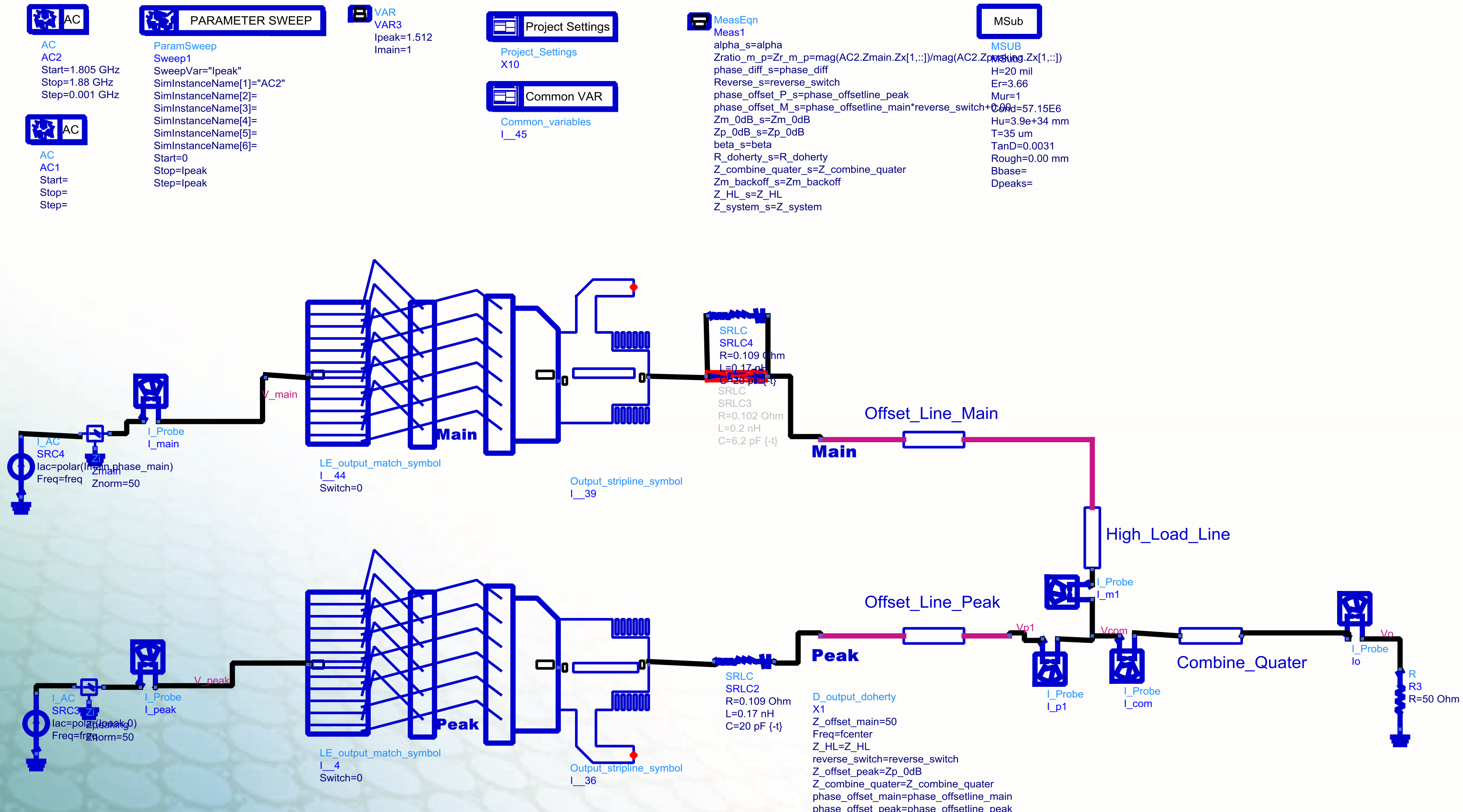
C

PCB Matching Design

1. Input and output PCB matching design;

3. Introduction of Analysis Tools

1) Bandwidth Analysis Tool(a)



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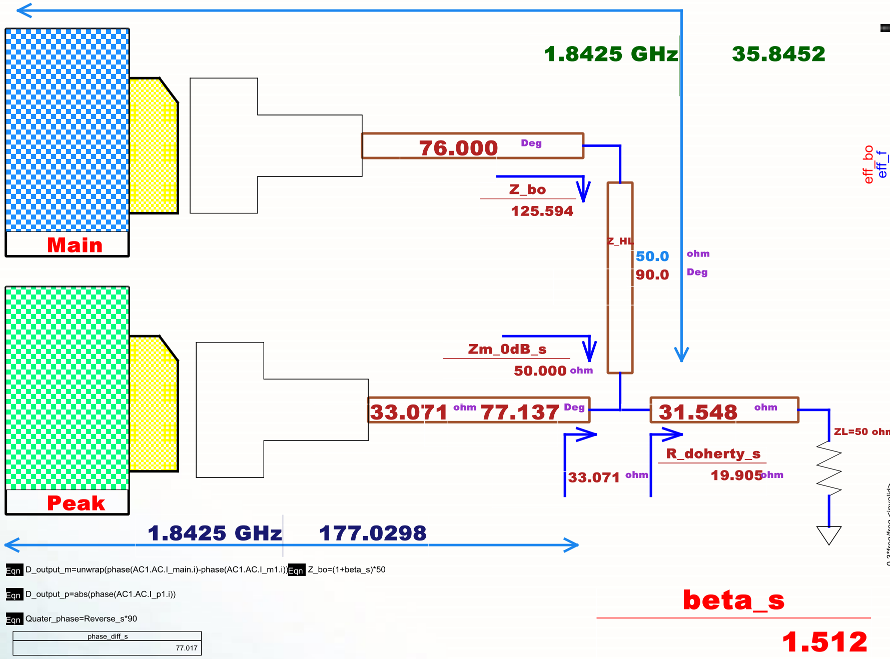
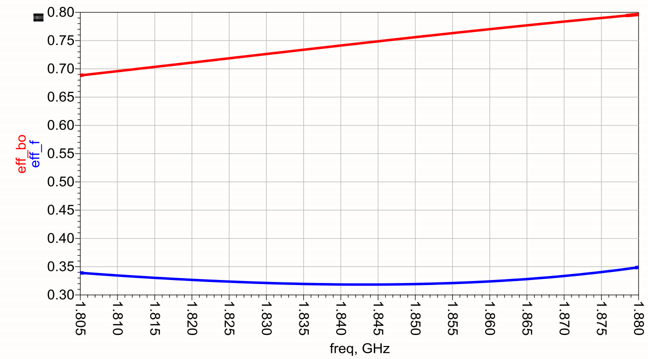
3. Introduction of Analysis Tools

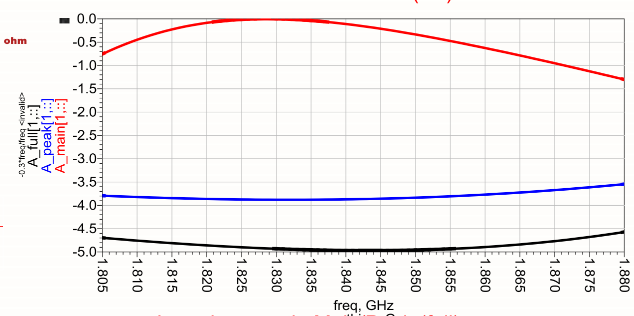
1) Bandwidth Analysis Tool(b)



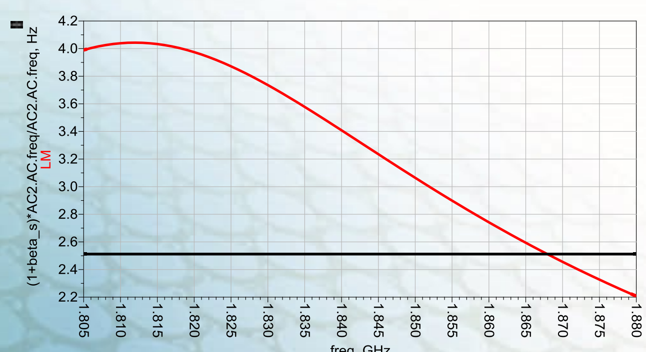
Relative Deff (bo - full)



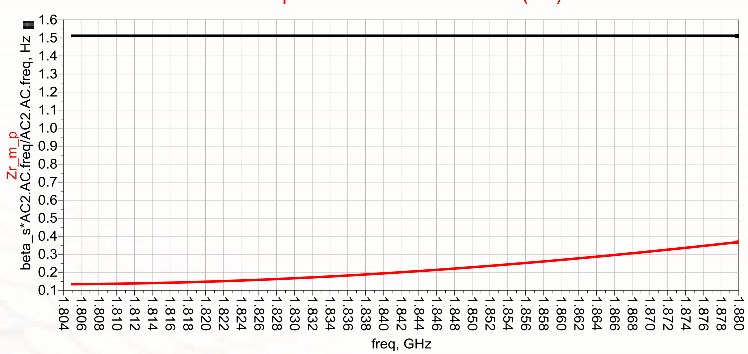
Relative Po loss (full)



Load modulation Main (bo - full)



Impedance ratio Main/Peak (full)



Can calculate the relative bandwidth , the load modulation behavior over the band

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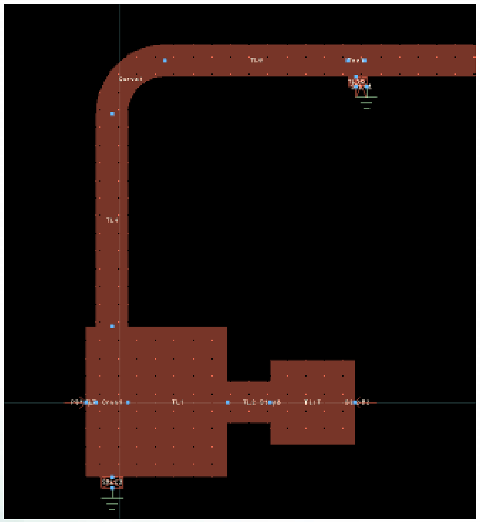
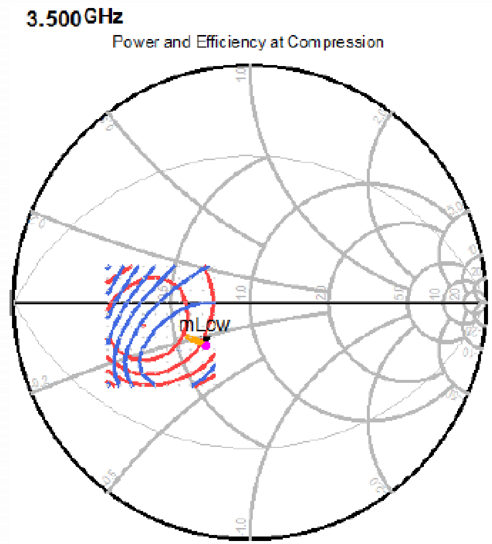
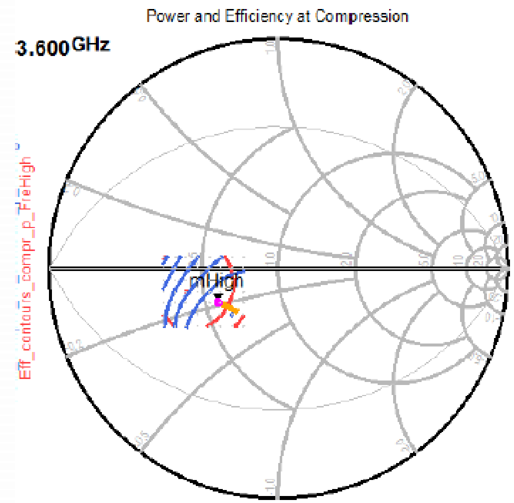
3. Introduction of Analysis Tools

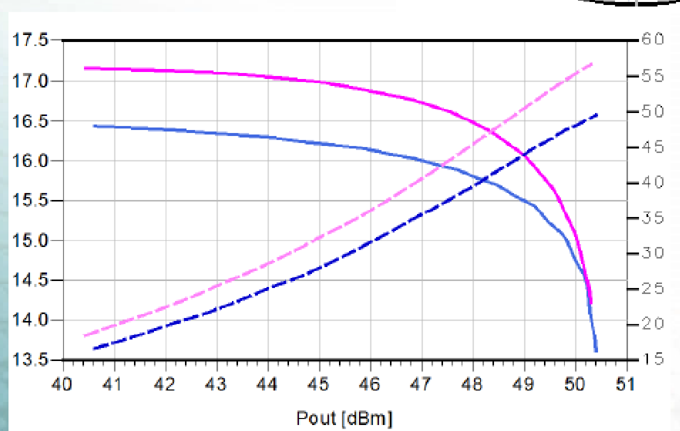
2) LP data analysis tool(a),

Can map impedance matching results onto the LP data









	3.500GHz	3.600GHz
Pout	50.40dBm	50.30dBm
Pout	109.56W	107.04W
Eff	49.58%	56.75%

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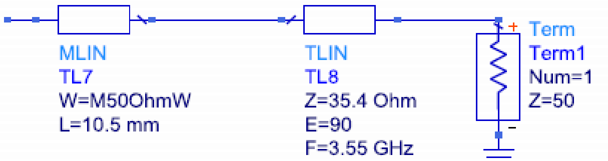
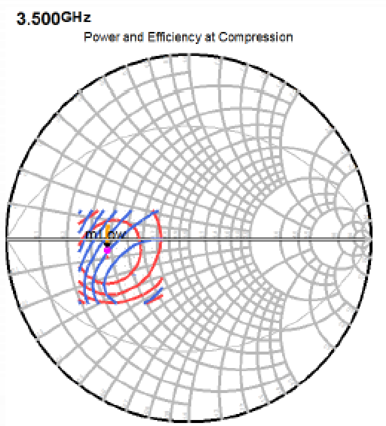
3. Introduction of Analysis Tools

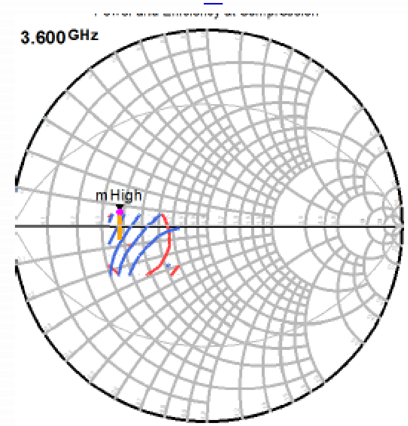
2) LP data analysis tool(b),

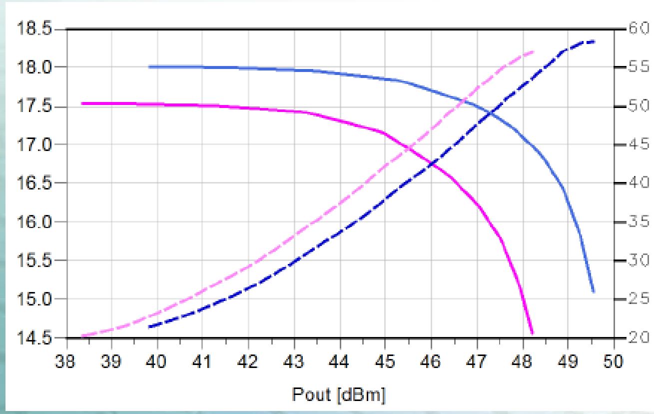
Can analysis the high load performance over the band



2:1 High Load







	3.500GHz	3.600GHz
Pout	49.54dBm	48.20dBm
Pout	89.92W	66.11W
Eff	58.37%	56.96%

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Any Questions?

Thanks

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