CHAPTER 6

THERMAL DESIGN CONSIDERATIONS

Thermal design considerations Chapter 6

INTRODUCTION

The ability to describe the thermal performance characteristics of a semiconductor IC package is becoming increasingly crucial. With increased power densities, improved reliability and shrinking system sizes, the cooling of IC packages has become a challenging task for design engineers. The situation is further exacerbated by the demand for ever decreasing sizes of electronic devices because, in general, decreasing the size of an electronic package decreases the thermal performance. The designer must carefully balance the benefits of miniaturization and performance against the potential reduction in reliability of electronic components resulting from high operating temperatures.

THERMAL RESISTANCE

The ability of a particular semiconductor package to dissipate heat to its environment is expressed in terms of thermal resistance ($R_{th(j-a)}$). This single entity describes the heat path impedance from the active surface of the semiconductor device (junction) to the ambient operating environment. $R_{th(j-a)}$ can be expressed by its constituents as follows:

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-a)}$$

$R_{th(j-c)}$ is the impedance from junction to case (outside surface of package) and $R_{th(c-a)}$ is the impedance from case to ambient. It is sometimes useful to use only the $R_{th(c-a)}$ to describe high performance packages where case temperatures are important and externally attached heat radiators may need to be attached. In these cases the overall $R_{th(j-a)}$ will also include the contribution of the heat radiator.

JUNCTION TEMPERATURE

With the $R_{th(j-a)}$ of a package known, the rise in junction temperature (T_j) with respect to the ambient temperature (T_{amb}) can be determined at a given power dissipation (P_d) of the semiconductor device:

$$T_j = (R_{th(j-a)} \times P_d) + T_{amb}$$

Where:

T_j = junction temperature (°C)
$R_{th(j-a)}$ = thermal resistance junction to ambient (K/W)
P_d = power dissipated (W)
T_{amb} = ambient temperature (°C)

It's important to note that a lower $R_{th(j-a)}$ indicates a higher thermal performance.

FACTORS AFFECTING $R_{th(j-a)}$

There are several factors which affect the characteristic thermal resistance of IC packages. Some of the more significant of these include the test board configuration, the lead frame material, the design of the lead frame and the moulding compound.

Test board Configuration

An IC package's thermal resistance highly depends on the Printed Circuit Board (PCB) on which the package is mounted. The copper traces and thermal vias on the PCB provide the major heat dissipation path of the package, therefore the configuration and the size of the copper traces play a significant role in affecting $R_{th(j-a)}$. For test purpose, JEDEC standards (EIA/JEDEC51-3 and others) specify two categories of test boards: low effective thermal conductivity test board (low K board) and high effective thermal conductivity test board (high K board). The low K board is a single sided board with only fine signal traces, the high K board is a board with two signal layers and two power (or ground) layers. The real application board is almost always different from the standard test boards, however, the thermal resistance measured from the standard test board provides basic comparable information of the IC package thermal resistance.

Lead Frame Material

The lead frame material is one of the more important factors in IC package thermal resistance. In early dual in-line packages (DIPs), a Ni/Fe alloy (A42) was the material of choice for lead frames as it provided a good combination of strength and formability as well as assembly process compatibility. However, with the continued miniaturization of IC packages and the need for increased electrical conductivity for advanced ICs, a switch to sophisticated copper alloys was required. Copper alloy lead frames offer several advantages over A42:

- they have a high thermal conductivity which reduces thermal resistance, essential for packages such as the Shrink Small Outline Package (SSOP) and Thin Shrink Small Outline Package (TSSOP)
- their improved electrical conductivity enhances the electrical performance of a package

Most plastic encapsulated packages produced by Philips Semiconductors incorporate copper alloy lead frames into their design.

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Lead Frame Design

The design of a lead frame is another significant contributing factor to thermal resistance. The most important design aspect is the IC attach-pad size and tie bar design. However, the lead frame designer is often faced with fixed parameters such as die size and wire bonding limitations, which reduce lead frame design flexibility.

Moulding Compound

Moulding compounds also determine IC package thermal resistance. The mould compounds used by Philips Semiconductors are optimized for high purity and quality to provide good thermal performance and reliability.

Heat Spreaders

The option of a heat spreader, or heat slug, within some packages can improve thermal behaviour by spreading the heat over a larger area of the package, and so improve $R_{th(j-a)}$ or $R_{th(j-c)}$.

Adhesive and Plating Type

Other package related factors include die attach adhesive and lead frame plating type, but the actual influence on thermal resistance is small owing to the fine geometry of these factors.

THERMAL RESISTANCE TEST METHODS

Philip Semiconductors uses what is commonly called the Temperature Sensitive Parameter (TSP) method which meets EIA/JEDEC Standards EIA/JESD51-1, EIA/JESD51-2 and EIA/JESD51-3. A typical test fixture in still air is shown in Fig.1. The enclosure is a box with an inside dimension of 1 ft^3 (0.0283 m^3). The enclosure and fixtures are constructed from an insulating material with a low thermal conductance, and all seams thoroughly sealed to ensure there is no airflow through the enclosure. The IC package is then positioned in the geometric center of the enclosure.

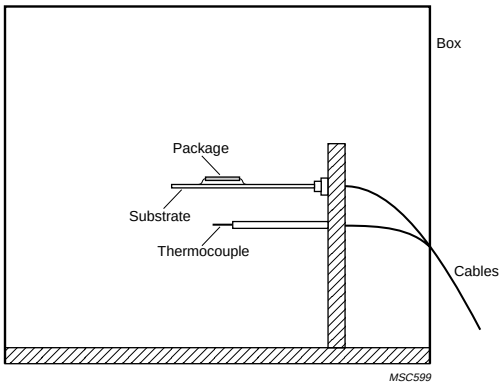

Fig.1 The test fixture in still air.

The forward voltage drop of a calibrated diode incorporated into a special IC is used to correlate a junction temperature change in the IC package to be tested. As the power dissipation is known, the thermal resistance can be calculated using the following equation:

$$R_{th(j-a)} = \frac{\Delta T_j}{P_d} = \frac{(T_j - T_{amb})}{P_d}$$

Where:

$R_{th(j-a)}$ = thermal resistance junction to ambient (°C/W)
T_j = junction temperature (°C)
P_d = power dissipated (W)
T_{amb} = ambient temperature (°C)

TEST PROCEDURE

The TSP diode on the semiconductor device is calibrated using a constant temperature oil bath and a constant current power supply (see Fig.2). Calibration temperatures are typically 25 °C and 100 °C with a measured accuracy of ±0.1 °C. The calibration current must be kept low and constant to avoid significant junction heating. The temperature coefficient (K-factor) shown in Fig.3 is calculated using the following equation:

$$K = \frac{(T_2 - T_1)}{(V_{F2} - V_{F1})}$$

Where:

K = temperature coefficient (°C/mV)
T_2 = high test temperature (°C)
T_1 = low test temperature (°C)
V_{F2} = forward voltage at T_2 (mV)
V_{F1} = forward voltage at T_1 (mV)

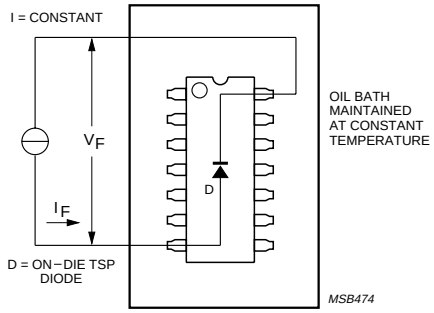

Fig.2 Test procedure.

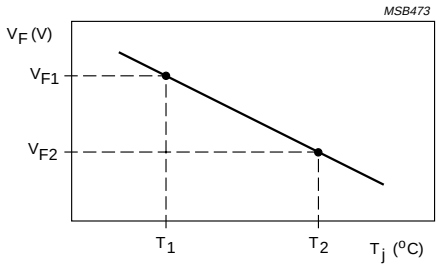

Fig.3 V_F as a function of T_j.

With the K-factor determined, $R_{th(j-a)}$ can be calculated by powering up the device at ambient conditions and measuring the forward voltage drop across the TSP diode after temperature equilibrium. Manipulating the original thermal resistance equation with the K-factor, the $R_{th(j-a)}$ of the package can be determined:

$$R_{th(j-a)} = \frac{\Delta T_j}{P_d} = \frac{(T_j - T_{amb})}{P_d} = \frac{K(V_{F(amb)} - V_{F(s)})}{V_H \times I_H}$$

Where:

$V_{F(amb)}$ = forward voltage of TSP at ambient temperature (mV)
$V_{F(s)}$ = forward voltage of TSP at steady-state temperature (mV)
V_H = heating voltage (V)
I_H = heating current (A)

FORCED AIR FACTORS FOR THERMAL RESISTANCE

Many applications with ICs have the benefit of forced air cooling by fans or other means. The junction to moving-air thermal resistance can be measured by placing the test setup inside a low velocity wind tunnel (see Fig.4). The test board and device under test are supported with minimal obstruction to the air flow.

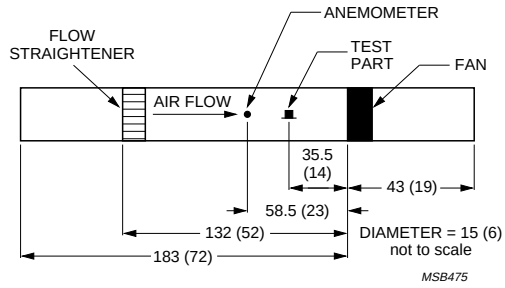

Fig.4 Wind tunnel - dimensions in cm (inches).

The average effect of airflow on thermal resistance for package types at a particular air flow rate can be determined using a “derating” curve (see Fig.5). When using derating curves, it’s important to note that the variety of sizes in a package type group has been averaged. See the following section on “Thermal resistance data - assumptions and precautions” concerning airflow.

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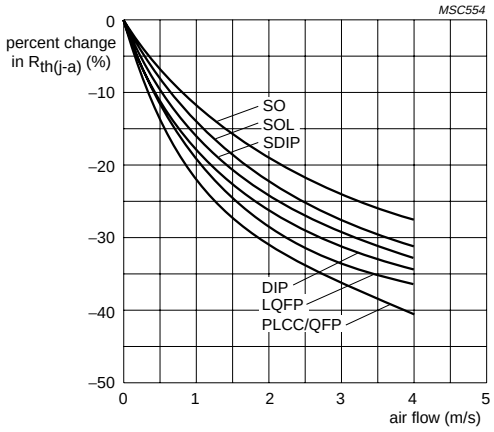

Fig.5 Average effect of airflow on $R_{th(j-a)}$.

THERMAL RESISTANCE DATA - ASSUMPTIONS AND PRECAUTIONS

The graphical data presented in this section are based on **measurements**, **modelling** and **estimations**. As with all data, some assumptions and contributing factors should be noted:

1. The “measured” thermal resistance of an IC package is highly dependent on the configuration and size of the test board. Data may not be comparable between different semiconductor manufacturers because the test boards may not be the same. Also, the thermal performance of packages for a specific application may be different than presented here because the configuration of the application boards may be different than the test boards. Philip Semiconductors uses low effective thermal conductivity test boards for most of its packages.
2. Device standoff is a factor in determining thermal resistance especially for surface mounted packages such as SO and QFP packages. The same package from two different manufacturers will often have different standoff from the test boards. In general, high standoff corresponds to a higher thermal resistance.
3. The operating environment temperature must be used as the ambient temperature when calculating junction temperatures in an application. The temperatures inside an electronic enclosure are generally higher than the room temperature.
4. When using airflow derating curves (see Fig.5), please note that in actual applications where airflow is available, the flow dynamics may be more complex and turbulent than in a wind tunnel. Also, the many different sizes of packages in a package family such as QFP have been averaged to give one curve for ease-of-use. Lastly, the test boards used in the wind tunnel contribute significantly to forced convection heat transfer and may not be similar to an actual application PC board, especially its size.
5. Thermal resistance will vary slightly as a function of input power. Generally, as the power input increases, thermal resistance decreases. Thermal resistance changes approximately 5% for a 100% power change.
6. Thermal resistance data for some packages were not available at the time of publication. Please contact Philips Semiconductors for information on packages not listed in this handbook.
7. All data presented are accurate to approximately ±15%. For more specific information regarding an application, please contact Philips Semiconductors.
8. Philips Semiconductors is evaluating a new technique, which was described in the ESPRIT project DELPHI, to thermally characterize IC packages. This results in a description of the package by means of a resistor network, the so-called compact model. This resistor network gives an accurate model of the package and is valid for all practical environments. It is expected that these models can be imported into system- and PCB-level analyses tools in the near future. If you require more information about compact models, please contact the ATO-Innovation office in Nijmegen, the Netherlands tel. +31-24-3533085 or fax +31-24-3533350.

THERMAL RESISTANCE ($R_{th(j-a)}$) DATA

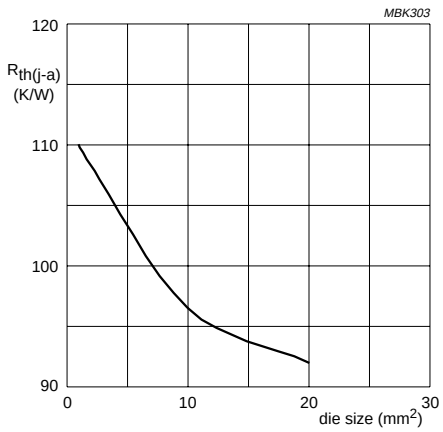

Fig.6 DIP8 (300 mil).

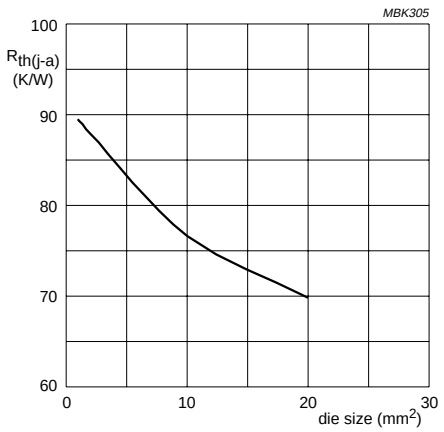

Fig.7 DIP14/16 (300 mil).

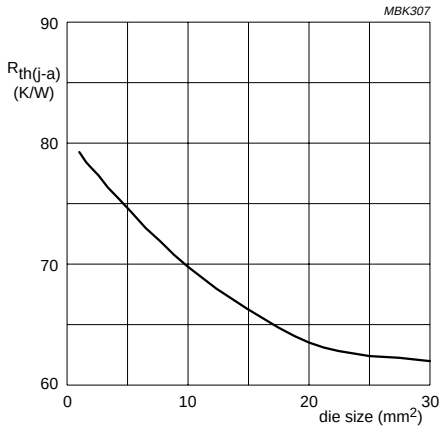

Fig.8 DIP18 (300 mil).

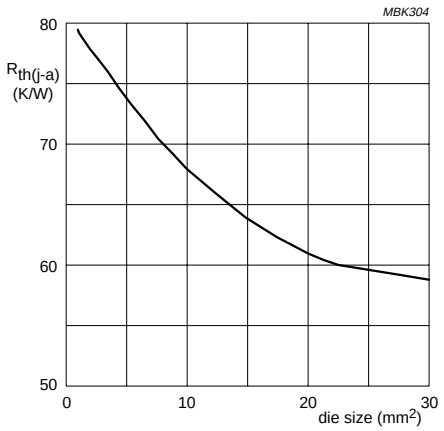

Fig.9 DIP20 (300 mil).

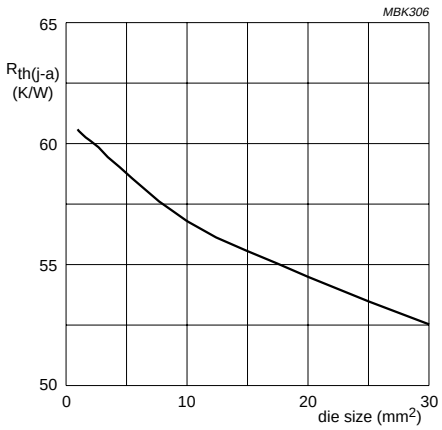

Fig.10 DIP22 (400 mil).

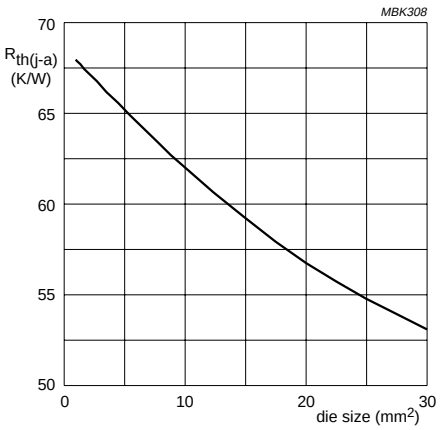

Fig.11 DIP24 (300 mil).

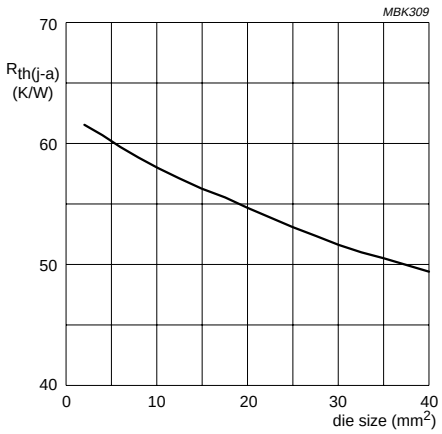

Fig.12 DIP24 (400 mil).

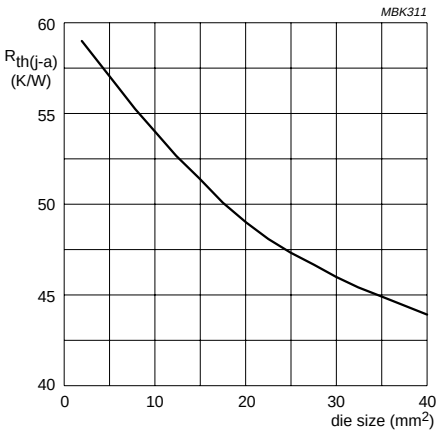

Fig.13 DIP24 (600 mil).

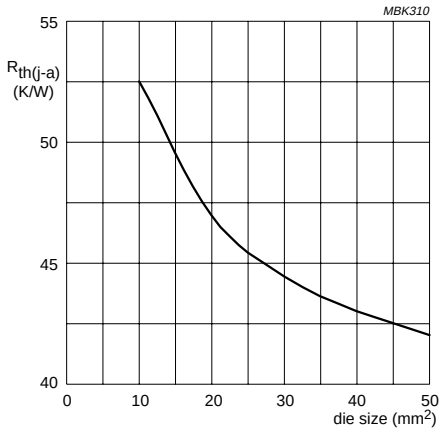

Fig.14 DIP28 (600 mil).

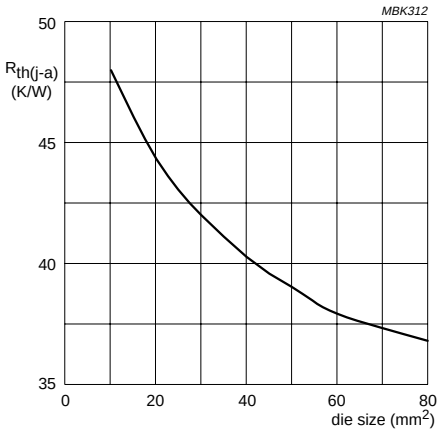

Fig.15 DIP40 (600 mil).

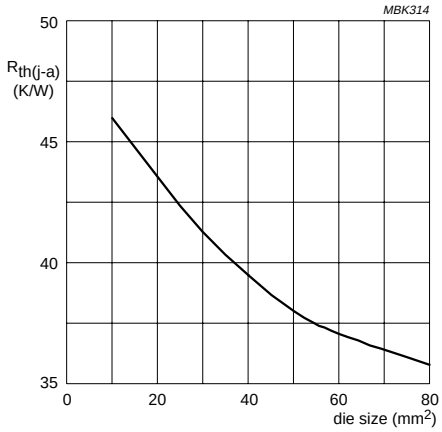

Fig.16 DIP48 (600 mil).

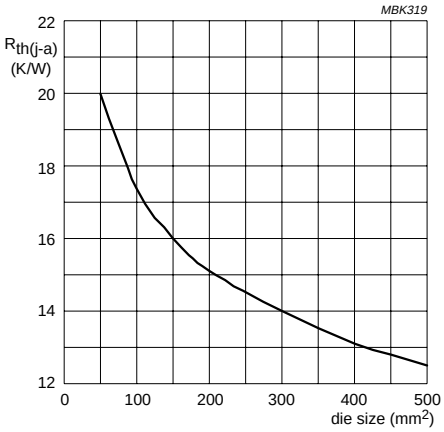

Fig.17 HSQFP240 ($32 \times 32 \times 3.4$ mm).

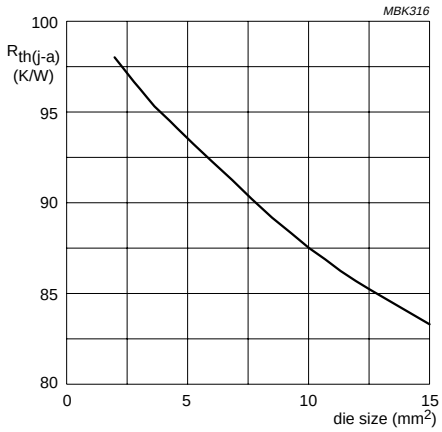

Fig.18 LQFP32 ($5 \times 5 \times 1.4$ mm)

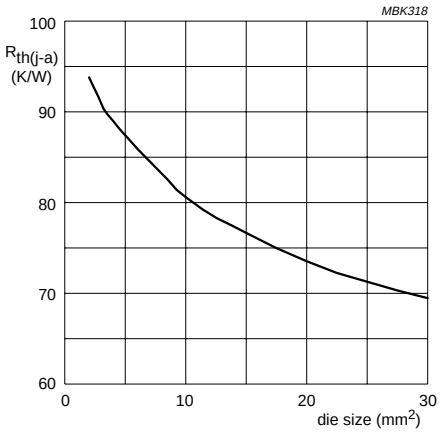

Fig.19 LQFP32 ($7 \times 7 \times 1.4$ mm).

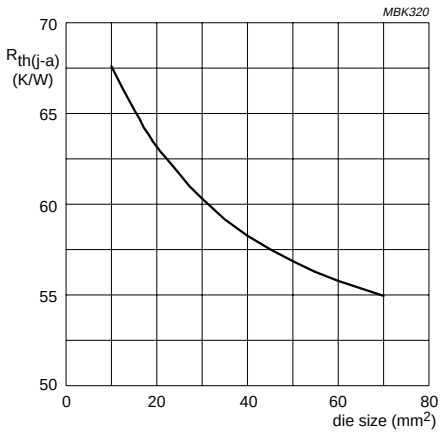

Fig.20 LQFP44 ($10 \times 10 \times 1.4$ mm)

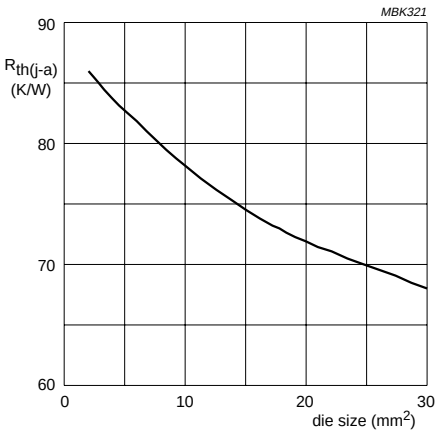

Fig.21 LQFP48 ($7 \times 7 \times 1.4$ mm).

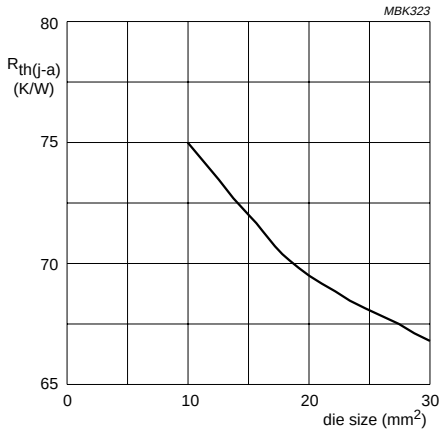

Fig.22 LQFP64 ($7 \times 7 \times 1.4$ mm).

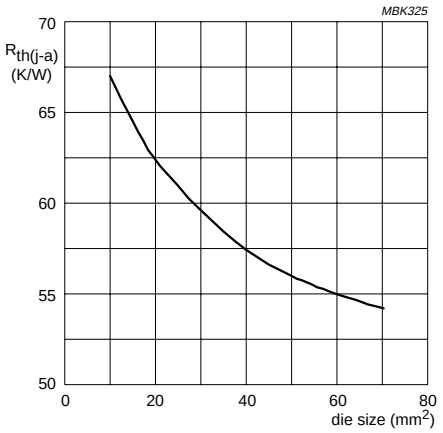

Fig.23 LQFP64 ($10 \times 10 \times 1.4$ mm).

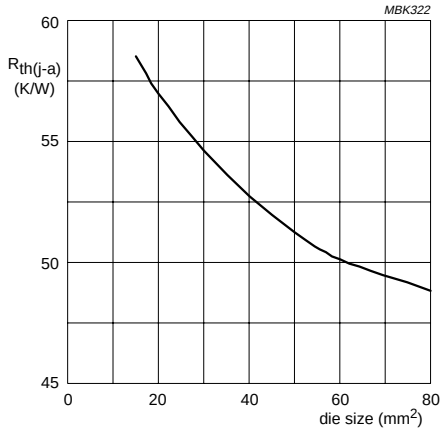

Fig.24 LQFP80 ($12 \times 12 \times 1.4$ mm).

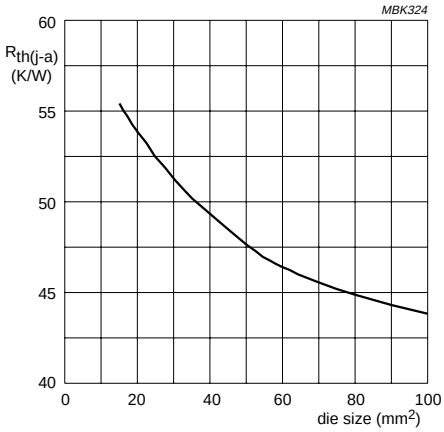

Fig.25 LQFP100 ($14 \times 14 \times 1.4$ mm).

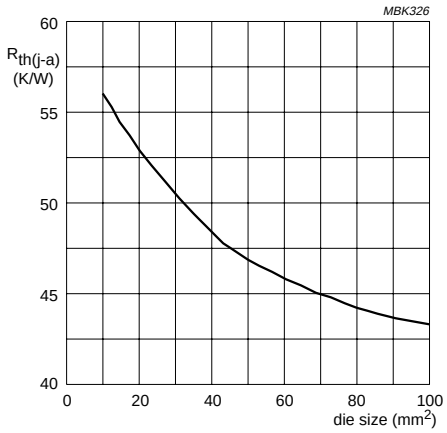

Fig.26 LQFP128 ($14 \times 14 \times 1.4$ mm).

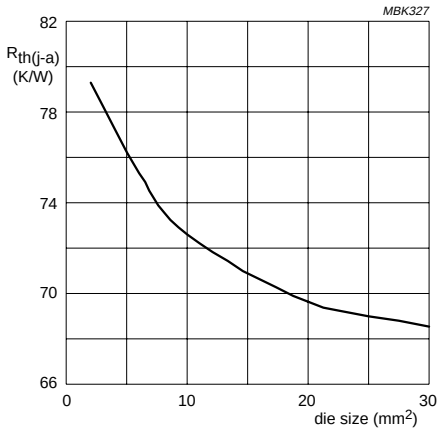

Fig.27 PLCC20 (310 mil).

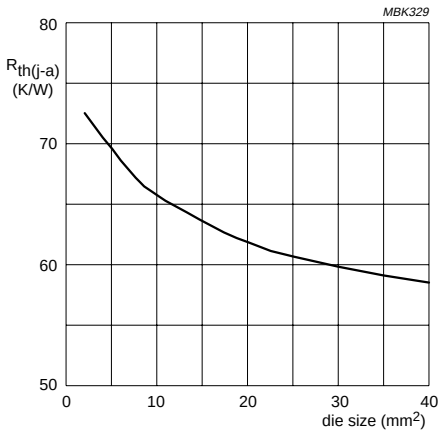

Fig.28 PLCC28 (410 mil).

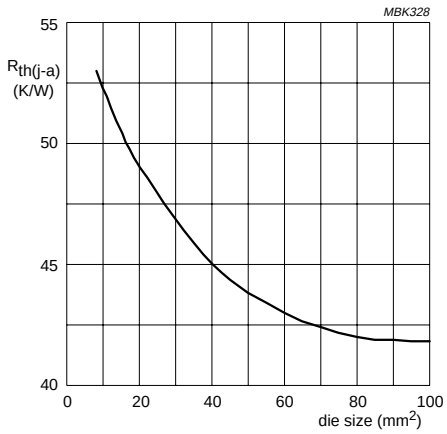

Fig.29 PLCC44 (610 mil).

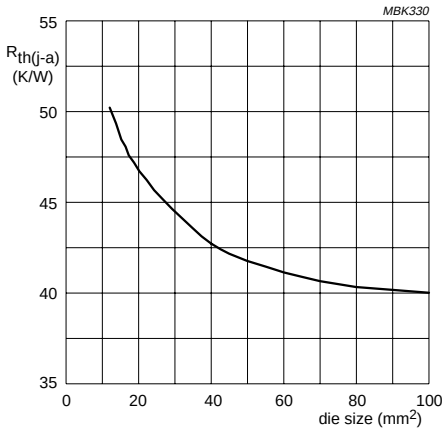

Fig.30 PLCC52 (710 mil).

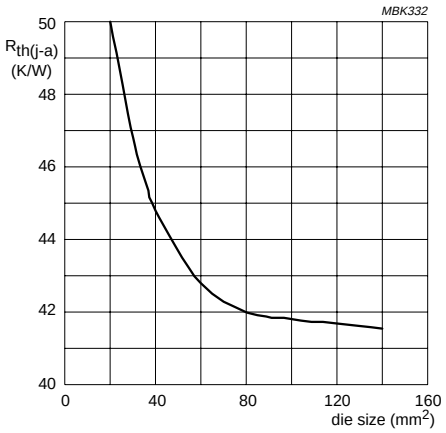

Fig.31 PLCC68 (910 mil).

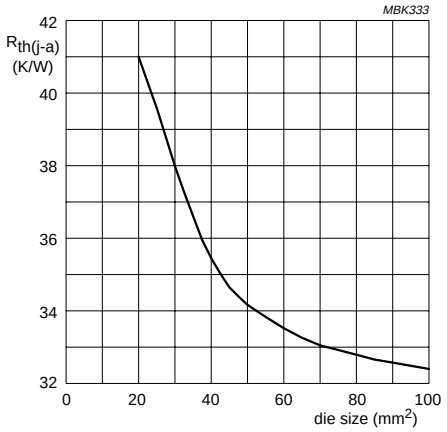

Fig.32 PLCC84 (1110 mil).

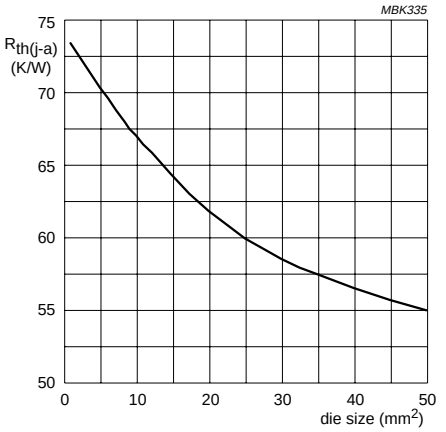

Fig.33 QFP44 ($10 \times 10 \times 1.75$ mm).

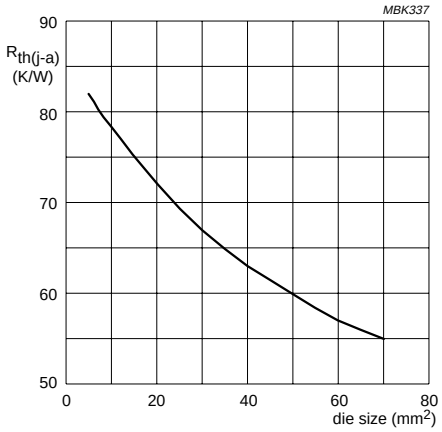

Fig.34 QFP44 FeNi ($14 \times 14 \times 2.2$ mm).

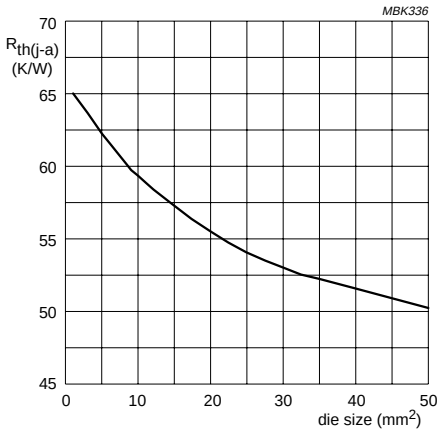

Fig.35 QFP52 ($10 \times 10 \times 2$ mm).

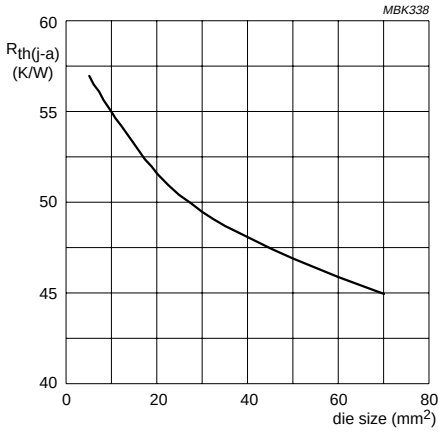

Fig.36 QFP64 ($14 \times 14 \times 2.7$ mm).

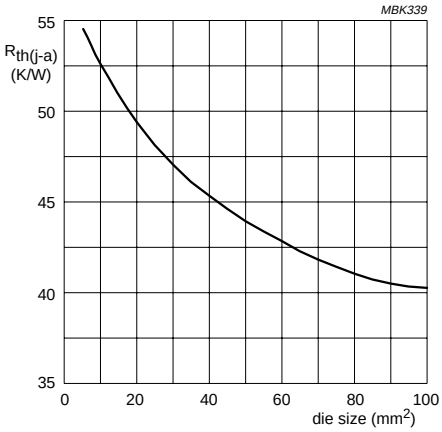

Fig.37 QFP64 ($14 \times 20 \times 2.8$ mm).

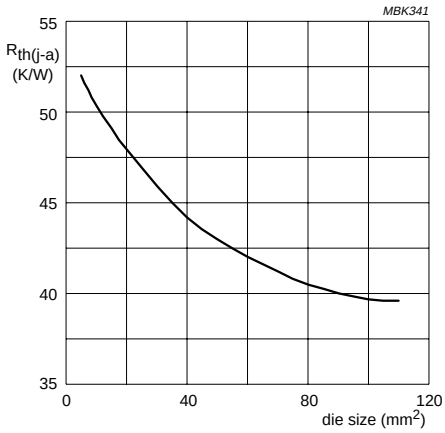

Fig.38 QFP80 ($14 \times 20 \times 2.8$ mm).

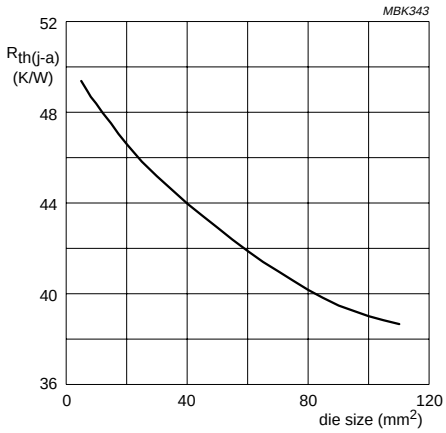

Fig.39 QFP100 ($14 \times 20 \times 2.8$ mm).

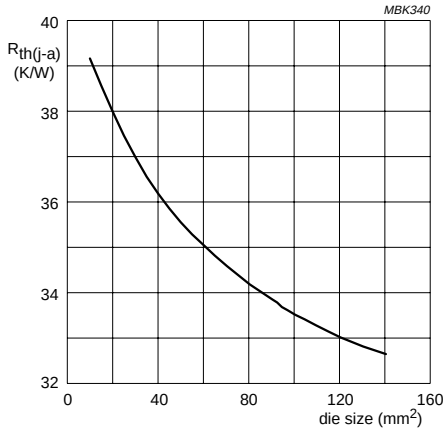

Fig.40 QFP120 ($28 \times 28 \times 3.4$ mm).

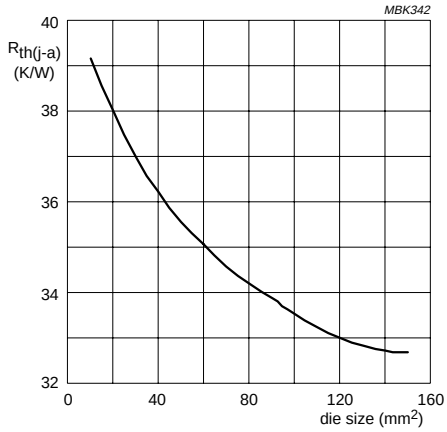

Fig.41 QFP128 ($28 \times 28 \times 3.4$ mm).

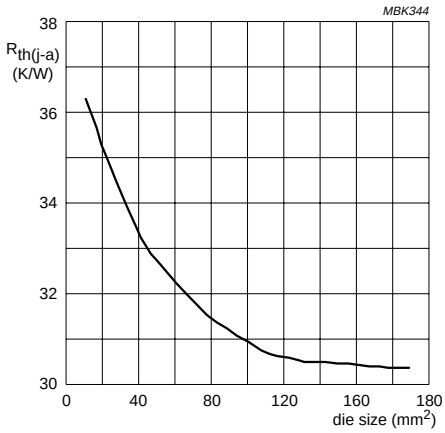

Fig.42 QFP160 ($28 \times 28 \times 3.4$ mm).

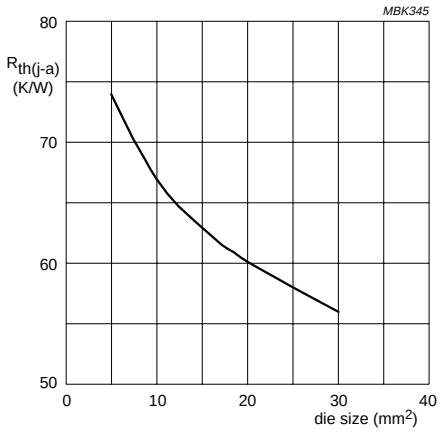

Fig.43 SDIP24 (400 mil).

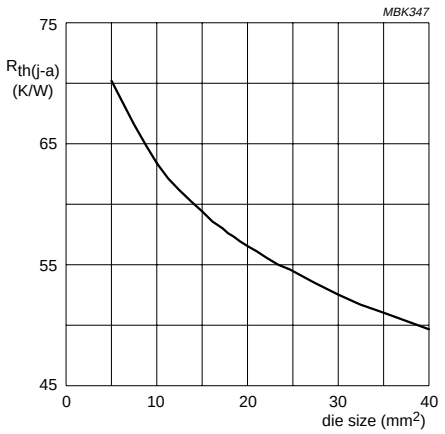

Fig.44 SDIP32 (400 mil).

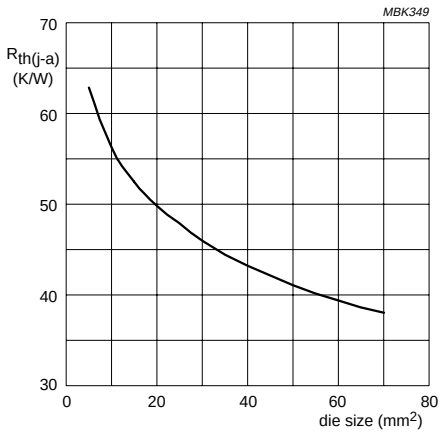

Fig.45 SDIP42 (600 mil).

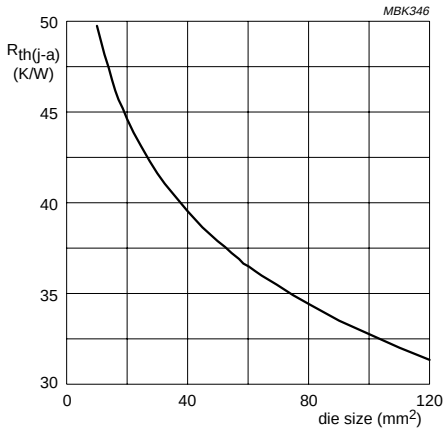

Fig.46 SDIP52 (600 mil).

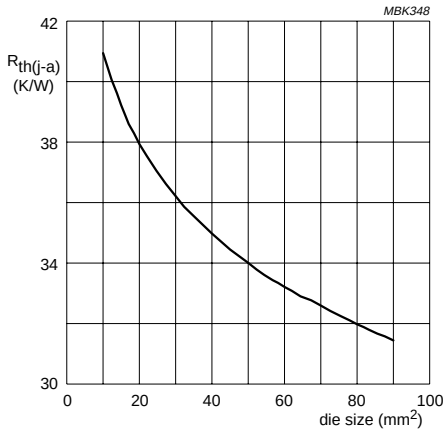

Fig.47 SDIP64 (750 mil).

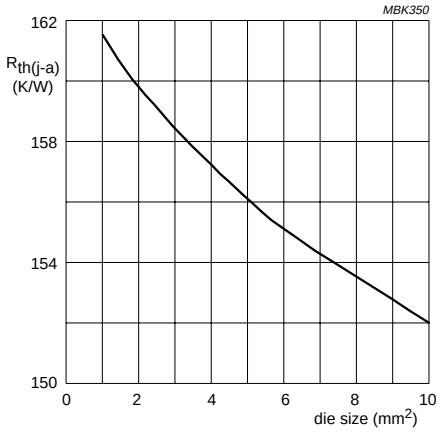

Fig.48 SO8 (150 mil).

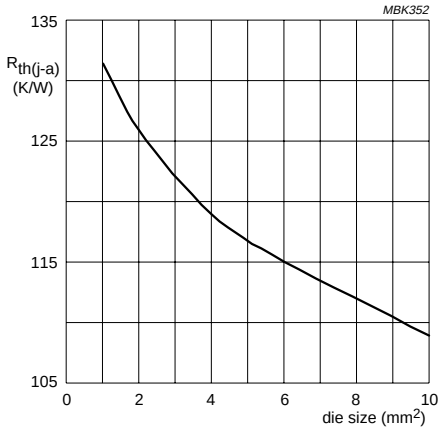

Fig.49 SO14 (150 mil).

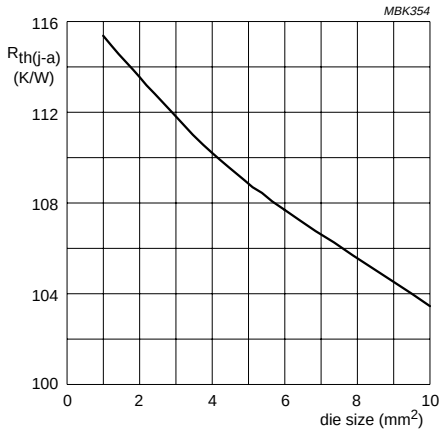

Fig.50 SO16 (150 mil).

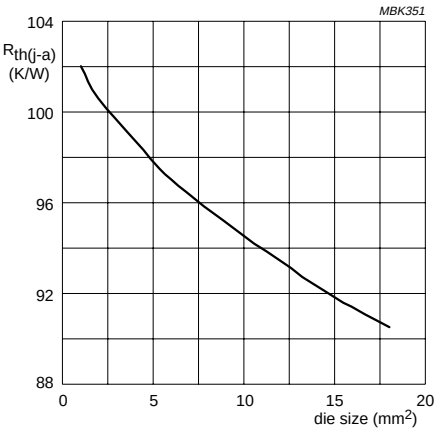

Fig.51 SO16 (300 mil).

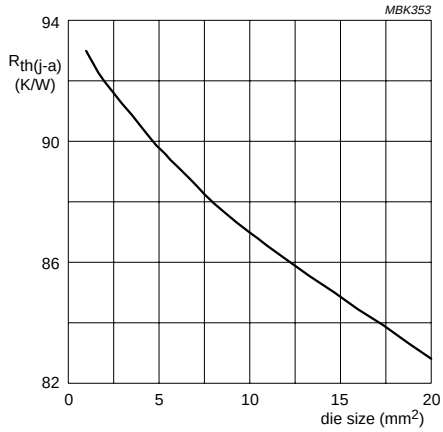

Fig.52 SO20 (300 mil).

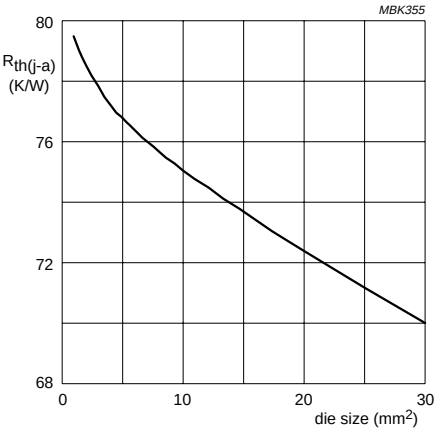

Fig.53 SO24 (300 mil).

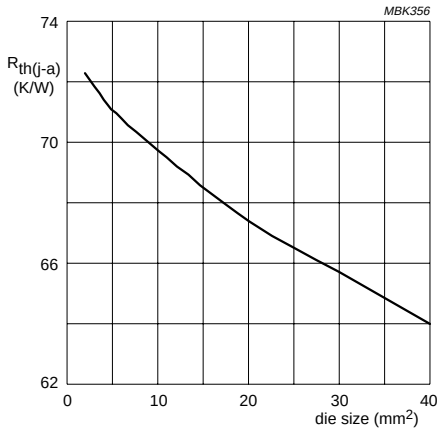

Fig.54 SO28 (300 mil).

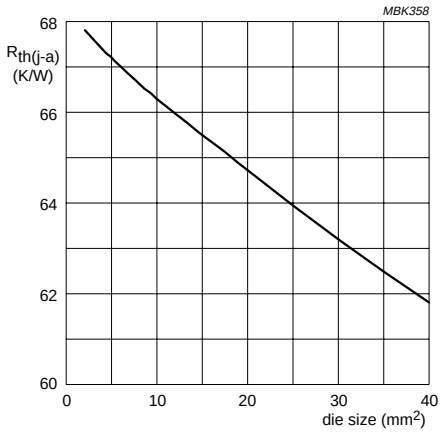

Fig.55 SO32 (300 mil).

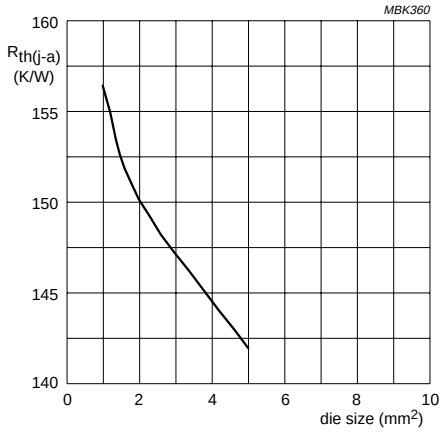

Fig.56 SSOP14 (5.3 mm).

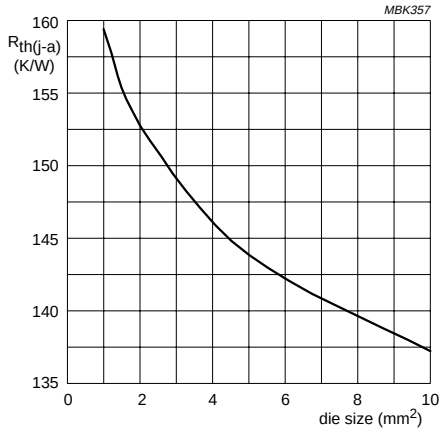

Fig.57 SSOP16 (4.4 mm).

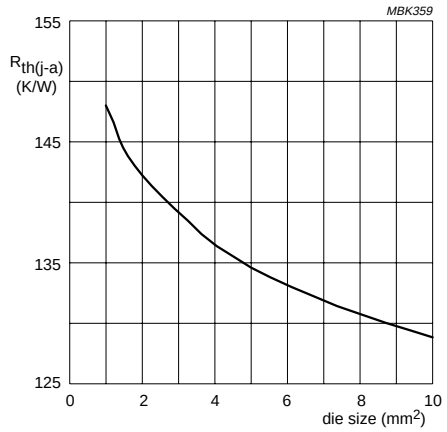

Fig.58 SSOP16 (5.3 mm).

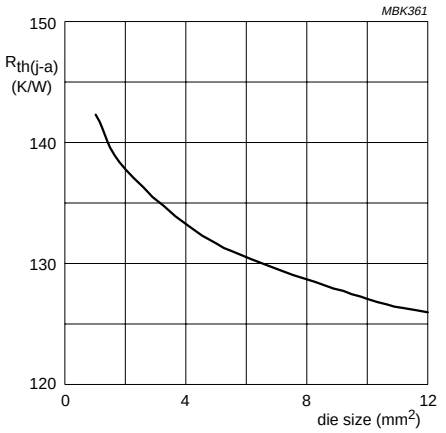

Fig.59 SSOP20 (4.4 mm).

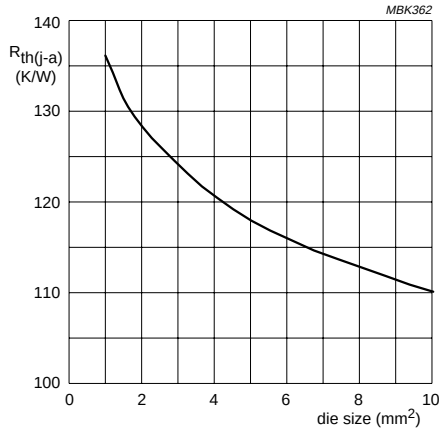

Fig.60 SSOP20 (5.3 mm).

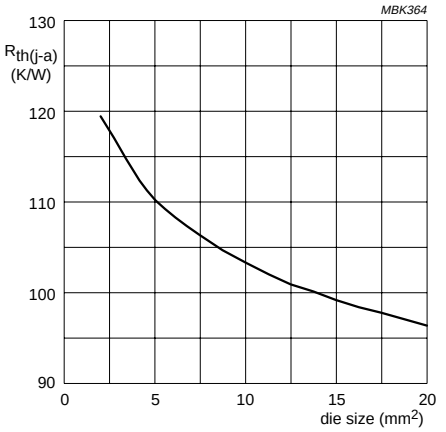

Fig.61 SSOP24 (5.3 mm).

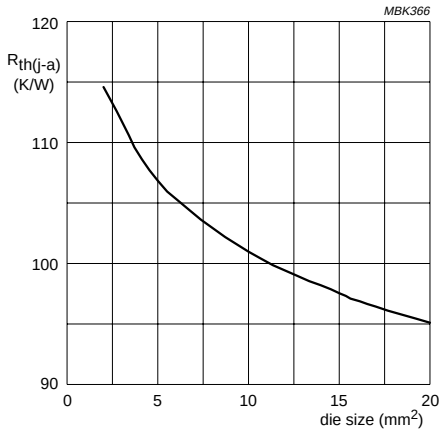

Fig.62 SSOP28 (5.3 mm).

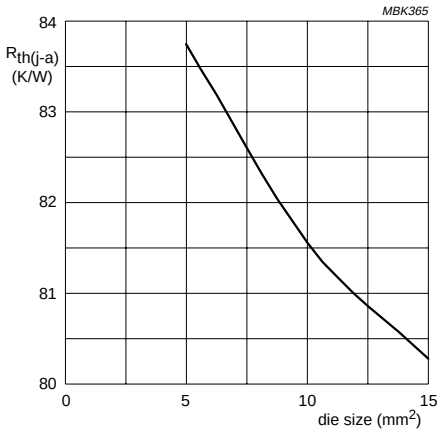

Fig.63 SSOP56 (7.5 mm).

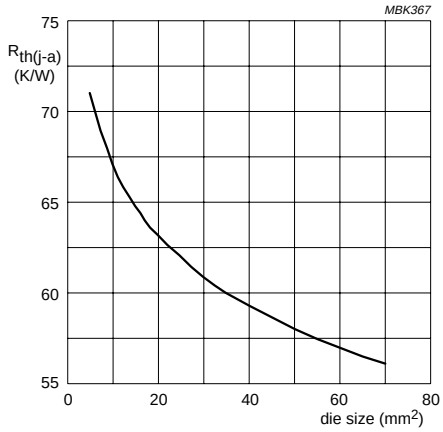

Fig.64 TQFP44 ($10 \times 10 \times 1$ mm).

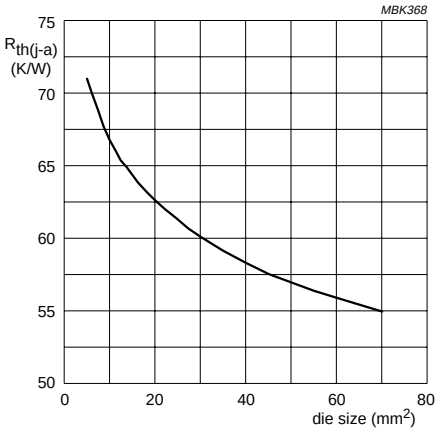

Fig.65 TQFP64 ($10 \times 10 \times 1$ mm).

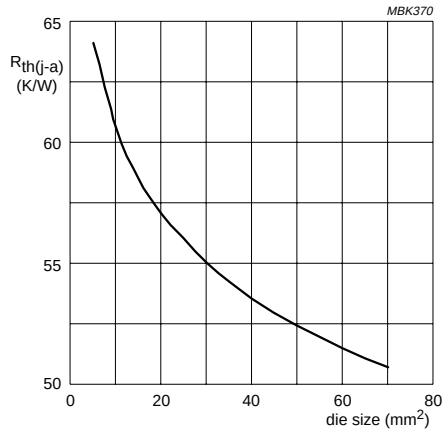

Fig.66 TQFP80 ($12 \times 12 \times 1$ mm).

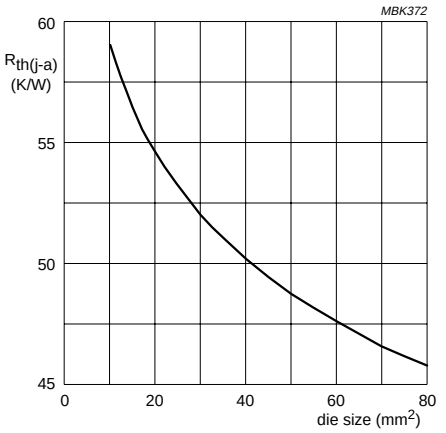

Fig.67 TQFP100 ($14 \times 14 \times 1$ mm).

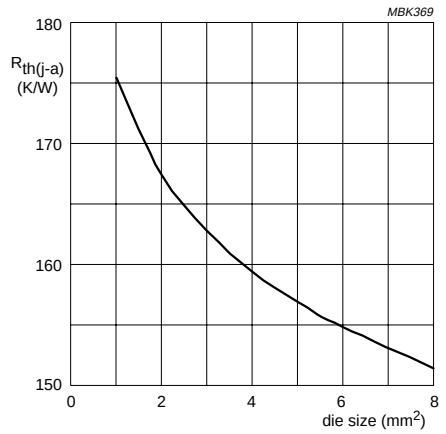

Fig.68 TSSOP14 (4.4 mm).

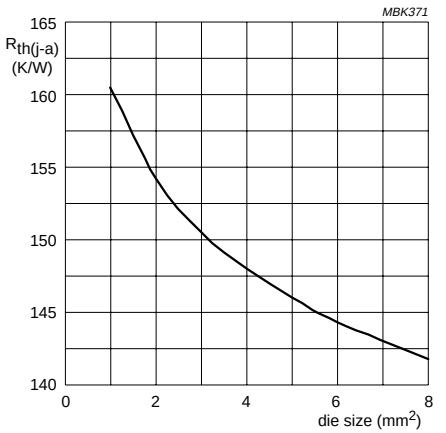

Fig.69 TSSOP16 (4.4 mm).

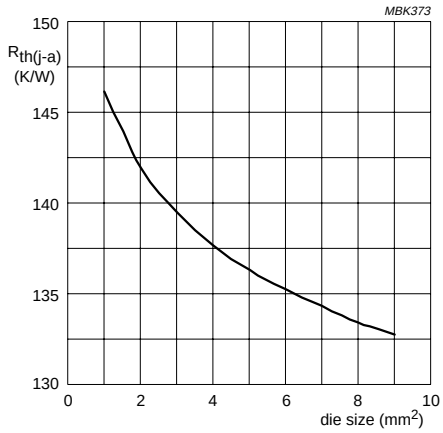

Fig.70 TSSOP20 (4.4 mm).

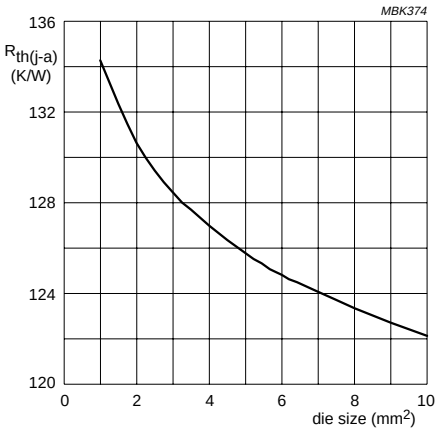

Fig.71 TSSOP24 (4.4 mm).

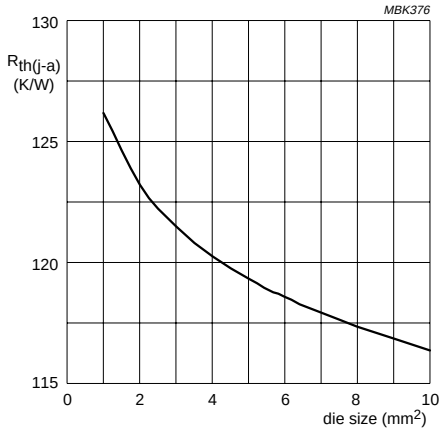

Fig.72 TSSOP28 (4.4 mm).

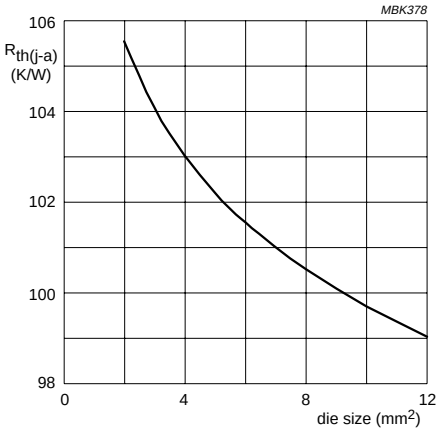

Fig.73 TSSOP48 (6.1 mm).

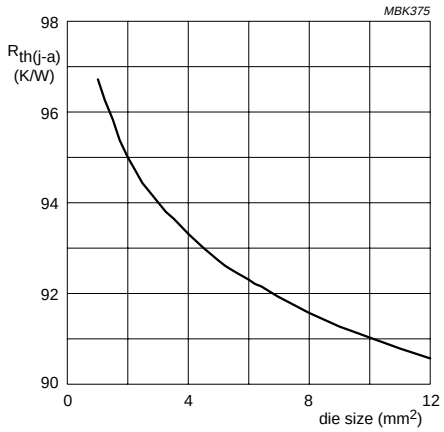

Fig.74 TSSOP56 (6.1 mm).

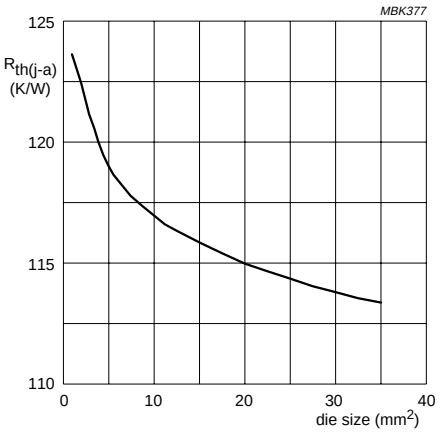

Fig.75 VSO40 FeNi (7.5 mm).

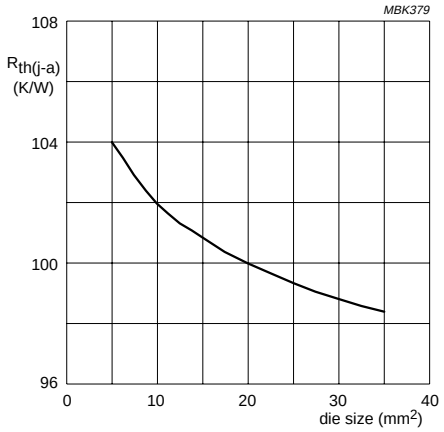

Fig.76 VSO56 FeNi (11 mm).

THERMAL RESISTANCE ($R_{th(j-c)}$) DATA TABLES - POWER PACKAGES(1)

PACKAGE NAME	PHILIPS OUTLINE CODE	$R_{th(j-c)}$ (K/W) GLUED DIE	$R_{th(j-c)}$ (K/W) SOLDERED DIE
DBS9MPF	SOT111-1	6.0 to 12.0	n.a.
DBS9P	SOT157-2	1.0 to 4.0	0.8 to 3.0
DBS13P	SOT141-6	1.0 to 4.0	0.8 to 3.0
DBS17P	SOT243-1	1.0 to 4.0	0.8 to 3.0
DBS23P	SOT411-1	n.a.	0.8 to 3.0
HSOP20	SOT418-2	1.0 to 4.0	0.8 to 3.0
RBS9MPF	SOT352-1	6.0 to 12.0	n.a.
RDBS13P	SOT462-1	1.0 to 4.0	0.8 to 3.0
SIL9MPF	SOT110-1	6.0 to 12.0	n.a.
SIL9P	SOT131-2	1.0 to 4.0	0.8 to 3.0
SIL13P	SOT193-2	1.0 to 4.0	0.8 to 3.0

Note

1.

a) Almost all of the values in the table were determined with measurements.

b) Low values should be used with a large die, high values should be used with a small die.