

# Millimeter-Wave GaN Power AMPLIFIER DESIGN

EDMAR CAMARGO

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Edmar Camargo



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# Preface

After my retirement in 2017, I felt the need to write a book on the subject of millimeter-wave power amplifier design. The objective was to produce a book suitable for engineers starting to work at millimeter-waves, providing them with the important design methodologies reinforced by a number of practical applications. The topics are treated at the appropriate depth to guide the engineers in the design of modern and sophisticated power amplifiers. The focus is on GaN technology, which has been shown in recent years to dominate power millimeter-wave applications due to its capabilities for high power, gain, and efficiency. Actually, a wide range of new millimeter-wave applications has been created to support the new 5G systems. Even though the main focus is on GaN material, the content is equally applicable to any field effect-based technologies, such as GaAs or InP. The opportunity to engage in such a project became a reality after two events. One was the encouragement and support that I received from Professor Denise Consoni after a lecture that I gave at Escola Politecnica, University of São Paulo, Brazil, in 2019. The other was the prospect of being secluded for a year due to the Covid-19 pandemic and using that time to some advantage. The resulting book represents my 20 years of accumulated experience in the area of millimeter-wave design.

In order to properly follow the book, it is assumed the reader has a sufficient background in various technologies. He or she needs to have a sound background in microwave circuit fundamentals and in the operation of field effect transistors from the point of view of an electrical component. At the present time, amplifiers for operation at microwave and millimeter-wave are designed based on the monolithic microwave integrated circuit (MMIC). Therefore, a good knowledge of the basics of this technology is essential to fully understand and absorb the design techniques reported in this book.

The organization of the six chapters is quite standard, starting in Chapter 1 with the advantages of GaN technology in power applications, the need of high-power millimeter-wave amplifiers for the backhaul of base stations, and the demand of high-efficiency components generated by the 5G cell phone market. In Chapter 2, we discuss the GaN HEMT device structure and properties that drive electrical performance. The passive and active linear models are also addressed, including their use to obtain key design parameters. Even though nonlinear models are not extensively used in the designs, simple EEHEMT models are discussed and used in some specific applications. The basic properties of power FET amplifiers are addressed in Chapter 3, including the basic DC parameters, load line, class of operation, and how these are affected at millimeter-wave frequencies. We cover class A, AB using

linear models and class F using nonlinear models. The impedance matching topic is tackled in Chapter 4, which includes lumped and distributed element prototypes with techniques to enhance the matching bandwidth. The important conversion between one type of prototype to another complements this topic. Also covered is another important aspect of impedance matching, as far as power amplifiers are concerned, which is the use of power dividers and combiners that simultaneously perform impedance matching. Chapter 5 is quite dense in content, due to the inclusion of a detailed description of the design steps for power amplifiers. The discussion starts with device sizing and establishing the amplifier design criteria. Several case studies are included to cover the different options available to the design, such as efficiency, power, and linearity sufficient to meet the 5G New Radio requirements. The conversion of electrical-based models to electromagnetic-based models for the amplifier is properly addressed and shows the importance of that analysis on the final amplifier performance. Chapter 5 ends with stability tests for the amplifier. It includes the three most popular tests, namely the  $K$ -factor or the  $\mu$ -factor, the loop stability, also known as internal stability, and the odd-mode stability. Chapter 6 provides a survey of the state-of-the-art power MMICs reported in recent years, which are designed fully or partially with the methodologies presented in Chapter 5, corroborating the validity of the design process.

Over the years, I have been fortunate to receive valuable insights from experienced engineers who helped me to improve my understanding of millimeter-wave amplifier design. It all started when Wayne Kennan and Taka Kawai introduced me to the MMIC world in 1994 and to Yuichi Hasegawa who later introduced me to millimeter-wave power amplifiers when working for Fujitsu Compound Semiconductor Inc. I must add the contribution of Dr. Amarpal Khanna during my stay at Hewlett Packard. He introduced me to the design of digital millimeter-wave radios, opening my understanding of how the components fit into real TX/RX systems. I also recognize the contribution of Andrea Betti Beruto in the design of millimeter-wave distributed amplifiers for lightwave modulators, starting when we worked for Fujitsu and later for GigOptix Technology Inc. In more recent years, I acknowledge the contribution of James Schellenberg who gave me the first steps on the GaN technology and the support I received from John Kuno, during the time we worked together at Quinstar Technology, Inc.

A special acknowledgement is due to Professor Denise Consoni, retired from the University of São Paulo Brazil. She was an important contributor in the preparation of this book. Besides being a constructive critic of my work, she helped me with the review and correction of the manuscript. I would like to thank and acknowledge the support of Cadence AWR for providing me with the software tools to carry on the design simulations. Also, I must add the support of Trong Phan, an MMIC design engineer, for the innumerable discussions that we had during the realization of this book.

## CHAPTER 1

# Introduction

The research and development of gallium nitride high electron mobility transistor (GaN HEMTs) technology, or the wideband gap technology, as it was initially called, started gaining momentum in the late 1990s, encouraged by their exceptional properties compared to laterally diffused metal oxide semiconductor (LDMOS) at 2 GHz [1]. Those included high-power density and the possibility to operate at 35V, becoming a tough competitor to LDMOS. By the early 2000s, GaN gained relevance when grown on top of silicon carbide (SiC) substrates [2]. As seen in Table 1.1, this combination results in exceptional thermal properties. By the mid-2000s the GaN HEMT power devices became a serious competitor to LDMOS in some microwave power amplifier applications. Reports of power density similar to LDMOS appeared by this time for applications in 3G and 4G. Investigations at millimeter-wave frequencies followed the trend. By the end of the decade, it was mature enough to provide power in the W-band range [3]. The key properties of GaN compared to other semiconductor materials are summarized in Table 1.1.

## 1.1 Millimeter-Wave GaN

Initially, the GaN found application in the wireless market for base stations. One of the advantages of GaN-based HEMTs is its high-power density at high bias voltages. Bias voltages at 50V and above are now common in GaN for base stations, found in commercial catalogs for high microwave power. For power amplifiers, high voltages imply higher impedance, compared to GaAs technology, resulting in

**Table 1.1** Semiconductor Material Parameters

Material	Mobility, $\mu$ ( $cm^2/Vs$ )	Saturated Electron Velocity ( $\times 10^7$ cm/s)	Thermal Conductivity (W/cm-K)	Bandgap (e.g., eV)	Breakdown Voltage (MV/cm)	$P_{dens}$ (W/mm)	$T_{max}$ (°C)
Si	1,300	1	1.5	1.1	0.3	1.5	300
GaAs	8,500	1.3	0.5	1.42	0.4	0.45	300
4H-SiC	700	2	4.5	3.25	3	17	600
GaN	1,000 to 2,000	2.5	1.7	3.49	3.3	25	700

smaller size and lower losses. Slowly, after 2010, GaN started showing its potential at millimeter-wave frequencies, when feasibility of gate lengths close to  $0.1\text{ }\mu\text{m}$  became real. Besides the high power potential, it also showed high efficiency. The discrete devices migrated to a monolithic microwave integrated circuit (MMIC) approach, so that a complete millimeter-wave amplifier is contained in a single die. The trend is to have more functions integrated within the same die, building up subsystems with microwave and millimeter-wave components. A more correct name to designate millimeter-wave chips would be monolithic millimeter-wave integrated circuits (MMMIC). However, the original name continues to be used to denote high-frequency integrated circuits.

Currently, GaN is predominantly grown on top of SiC to take advantage of the high thermal conductivity of that material, about three times higher than Si, measured at room temperature. However, in normal operation the channel temperature can be  $150^\circ\text{C}$ , where this difference drops to less than 2 [4]. There are issues in the interface of the GaN layer deposited on top of SiC, and they were solved by process engineers, who developed special buffer layers to neutralize the crystal mismatch between both materials. This problem is more aggravated on silicon substrates, but the much lower cost of the process drove the development of this technology. Recent investigations have actually shown that similar performance is expected for power levels up to 10W in the Ka-band [5]. Currently, at least one foundry offers this type of technology [5].

## 1.2 State of the Art

The current state of the art for GaN-based MMICs at millimeter-wave frequencies is shown in Figure 1.1. The data in this plot, taken from a recent publication [6], reports the best output power and associated power-added efficiency (PAE) versus

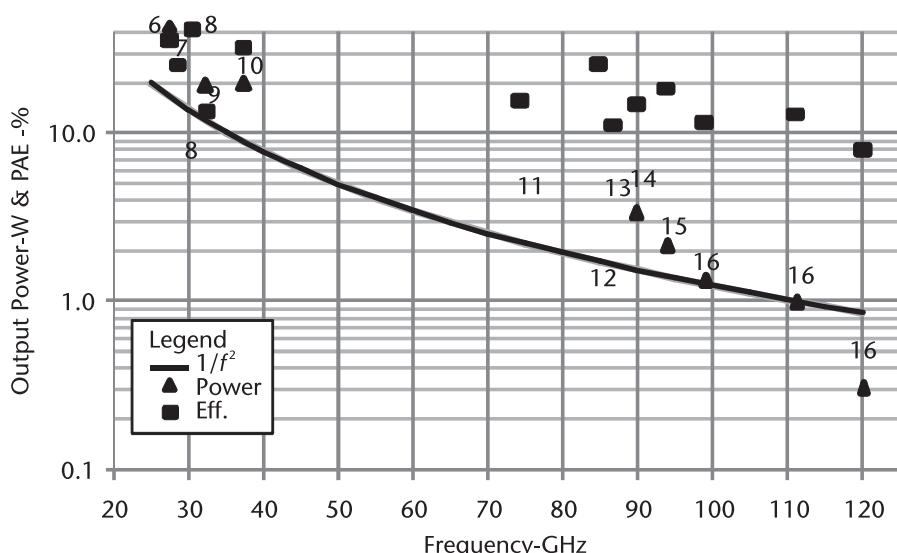


Figure 1.1 State of the art of GaN MMICs. (After: [6]. © 2020 IEEE.)

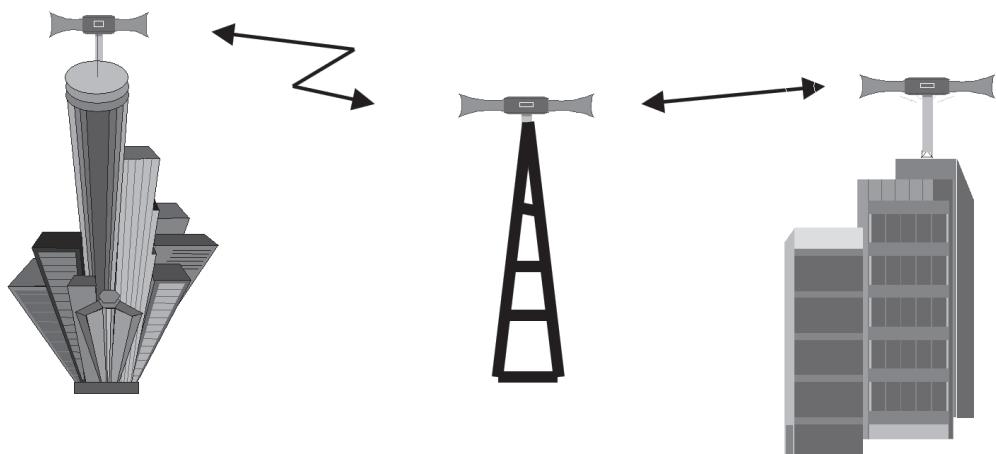
frequency from 26 to 110 GHz. These results are from MMIC chips under continuous wave (CW) operation, usually assumed to be a single-tone sinusoidal wave. The author noted that the power versus frequency follows a  $1/f^2$  curve, shown in the figure. Note that this curve predicts the reported power results through 110 GHz fairly accurately. The general trends indicate that the efficiency, contrary to the power behavior, does not seem to fall at the same rate. This difference is probably due to a higher efficiency of the technology employed above 70 GHz.

GaN devices for lower-frequency applications, in particular 3G and 4G, are manufactured with gate length,  $L_g$ , ranging from 0.3 to 0.5  $\mu\text{m}$ . For microwave applications, the devices are built with a gate length of 0.25  $\mu\text{m}$ . Applications for the frequency of 28 GHz, one of the frequencies selected for 5G applications, need to use a technology with a gate length of 0.15  $\mu\text{m}$ . For E-band and F-band applications, the gate length has to be equal to or lower than 0.1  $\mu\text{m}$ .

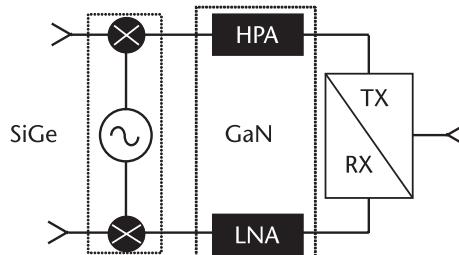
### 1.3 Applications

Among the applications for GaN millimeter-wave power amplifiers, the point-to-point systems, shown in Figure 1.2, are the most traditional and are mostly used to make the connection between base stations for cell phone systems. In most cases, the link between the antennas is of the type of line of sight (LOS), with no obstruction of the high-frequency signal path.

A typical T/R module employed by these systems is shown in Figure 1.3. The LO and mixers are integrated on a silicon germanium (SiGe) chip, along with the logic control for the overall module. The high power amplifier (HPA) for the TX path is the main application for the GaN. The LNA can also be built on SiGe; however, they are also being considered to be built on the same technology as the PA for two reasons: due to its robustness against high peak voltages and integration of PA and low noise amplifier (LNA) in the same chip. The high peak signals, originating from the power amplifier (PA) or from some external sources, may flow into the LNA path, requiring limiters to protect the circuit. Some authors [7, 8]



**Figure 1.2** Point-to-point links between base stations.



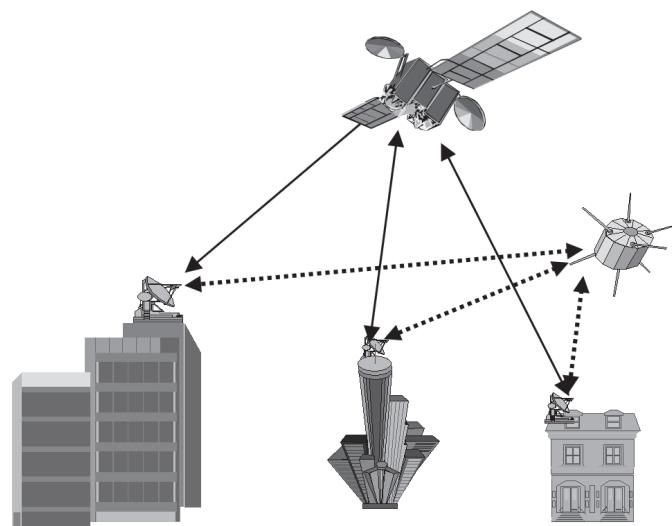
**Figure 1.3** Block diagram of a typical TXRX.

have reported that GaN LNAs can take power in the order of several watts at the gate without degradation. That means that the limiters can be eliminated and low noise performance can be improved.

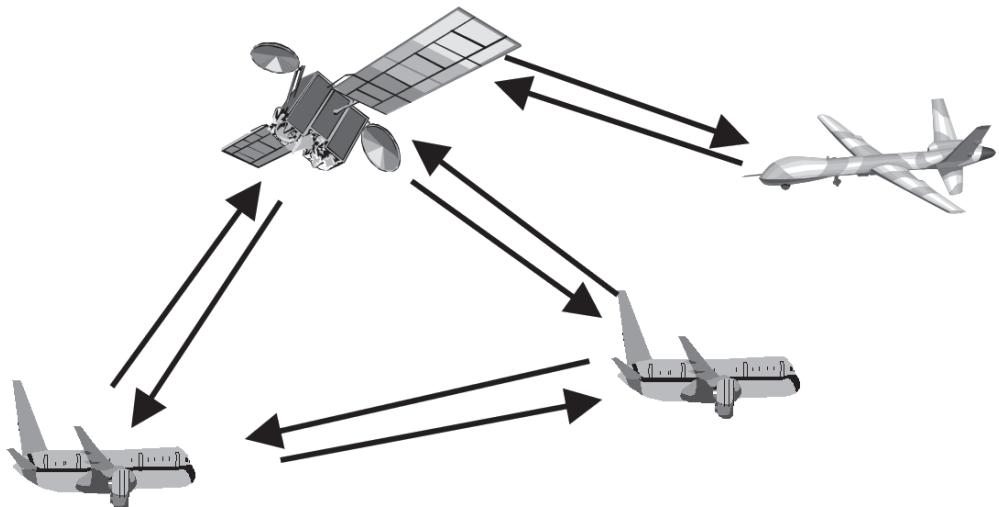
The diplexer connects the PA to the antenna and isolates the LNA from PA. Filters, micro electro-mechanical systems (MEMs) switches, circulators, or even GaN switches are candidates for the diplexer. The HPA, LNA, and diplexers may be considered a front-end subsystem. For base station applications, the linearity requirements are met with the use of digital predistorters, which is part of the HPA block diagram. The power efficiency is more dependent on how the amplifier is designed. Use of the envelope elimination and restoration technique can improve both linearity and efficiency [9].

The satellite to ground links at the Ka-band is represented in Figure 1.4 for the geosynchronous equatorial orbit (GEO) satellites and for the low Earth orbit (LEO) satellites. High-power SSPA-solid state amplifiers have been developed for this application for quite some time. For instance, in 2005, a 16-W Ka-band power amplifier was reported, using discrete pseudomorphic HEMT (pHEMT) gallium arsenide (GaAs) chips [10].

The air-to-air communications have appeared in recent years and are targeted to establish connections between airplane to airplane, airplane to satellite, and satellite to drones, illustrated in Figure 1.5. This last application is benefited by the



**Figure 1.4** Satellite links, GEO and/or LEO, operating at lower millimeter-wave frequencies.



**Figure 1.5** Air-to-air communications, operating at E-band.

lower propagation losses at altitudes higher than 3 km. They are about 0.08 dB/km compared to the value of 0.45 dB/km at the ground level. All these examples will use higher communication frequencies, like E-band, to be able to accommodate large bandwidths and, consequently, higher digital speeds [11].

## 1.4 Cell Phone Connectivity

Point-to-point links are key in the interconnectivity of cell phone base stations, along with optical fibers. In order to have an insight of this particular application, it is interesting to review the development of cell phones. It started back in 1980, employing an analog frequency division multiple access (FDMA) system called the advanced mobile phone system (AMPS). The cell phone was connected to a base station using carriers between 800 and 900 MHz, with 30-kHz subbands. The connectivity or backhaul<sup>1</sup> links between base stations were made at a much higher speed, 2 Mbps. Today this system is considered as first generation (1G) for coherence with modern classification. The next evolution in the cell phone systems was the development of digital cell phones using the Groupe Special Mobile (GSM) developed in Europe and code division multiple access (CDMA) developed in the United States, both in 1980. These systems provided similar quality of service. The data rate for the GSM was 64 kbps and the CDMA2000 provided 110 kbps. They are classified as second generation (2G) systems. The backhaul connection was made at a speed of 10 Mbps. The third generation (3G) system is based on wideband code division multiple access (WCDMA) technology with cell phone connectivity that started with 300 kbps and later reached 10 Mbps. Consequently, the speed of the connections between base stations increased to 300 Mbps. At the present time, the fourth generation (4G) system is deployed based on the Long Term Evolution

1. Backbone link = backhaul links = point-to-point.

(LTE) with a planned data rate of 100 Mbps in the downlink and 50 Mbps in the uplink. The actual speeds are about half these values. To accommodate this volume of information, the backhaul uses a connectivity of 2.5 Gbps.

For the coming fifth generation (5G) applications, the planned capability is 1 Gbps on the handset level and 10 Gbps at the backbone. The conventional radio system employed in 4G is not capable of handling such speeds. Broader bands for the information are needed to move to millimeter-wave and to a new radio paradigm.

In the new radio, instead of having a single PA illuminating a cell area, the radio was modified to a phased array PA system that sweeps the cell area [12, 13]. This is like a point-to-point link valid only at the instant of connectivity. The transmitting power in a phased array results from a number of small power amplifiers where the energy is spatially combined. The phased array system eases the burden of efficiency on the PAs, for higher efficiency is expected from smaller power devices. This means that millimeter-wave power will not only be employed in the backhaul, but, for the first time, it will be used in the handsets. That is just one of the many modifications in the 5G mobile system to achieve a large increase in the volume of data traffic over the years. Microwave and millimeter-wave have been used for the wireless backbone connectivity for quite some time. Now, in view of the high speed and volume of data, the connectivity will depend on millimeter-wave systems operating at V-band and E-band.

An interesting proposal for 5G is the use of microwave and millimeter-wave frequencies simultaneously [14]. This heterogeneous network (HETNET) was successfully applied in 4G systems with the objective of increasing the cell capacity with the help of smaller cell sizes [15]. All the control protocols and low data rate information are transmitted in a macro cell to the handset at sub-6-GHz bands, while the high data rates are transmitted to the handsets contained within the millimeter-wave micro cells. An illustration of this type of connectivity is represented in Figure 1.6, where millimeter-wave micro cells are layered within microwave cells. The millimeter-wave signals, represented by narrow beams, from the base station



**Figure 1.6** Proposed planned connectivity between 5G cells. (Courtesy of Mitsubishi [14].)

are transmitted via LOS to a fixed micro cell station limited by a radius of 200m. The cells are designed such that, in face of any obstacle, another cell is created to maintain the LOS.

High power amplifiers are needed in the backhaul of the main base stations and in the connectivity between the micro and macro cells. Power levels lower than 1W are sufficient for handsets. Currently, the sub-6-GHz bands are located between 1 and 4.2-GHz carriers with signal bandwidths of 600 MHz. The millimeter-wave bands approved by the U.S. Federal Communications Commission (FCC) are as follows: 24, 28, 37, 39, and 47 GHz. The signal bandwidth at millimeter-wave is expected to be 5 GHz. In addition to high-speed, 5G networks are expected to show a lower latency<sup>2</sup> compared to 4G. The latest 4G developments shows a latency in the order of 20 to 30 ms. It does not affect present 4G systems, but it will be a problem for 5G where it will include the Internet of Things. More specifically, this time is critical in the interaction with machines. With 5G, it is expected a reduction in the latency of at least two times.

Figure 1.7 gives an idea of how power, frequency, and technology interact with different environments [14]. In this case, the environment is actually the distance between TX and RX, represented in the vertical axis. The figure shows a dotted line that separates the level of power required by the system. The figure shows the proposed EIRP<sup>3</sup> values for macro cells at sub-6-GHz bands, micro and macro cells at millimeter-wave. For indoor communications, less than 100m, EIRP are in the order of 40 dBm either at microwave or millimeter-wave frequencies. Silicon technology will be used for indoor applications. For distances higher than 100m up to 2 km, EIRP grows to 60 and 70 dBm for microwave frequencies.

In the case of millimeter-wave distances from 30m to 500m, 50 to 65 dBm of EIRP are needed. GaN is one of the contenders for its capability of power and efficiency. The linearity of amplifiers has been conventionally overcome using digital predistorter technology. But due to latency reduction, they are not allowed in 5G. Technology studies are under way to make the GaN power amplifiers more linear.

There are many proposed topologies for the phased array 5G radio. The one in Figure 1.8 [16] shows a basic analog architecture of the phased array involving frequency converters, power combiner/dividers, phase shifters, LNAs, PAs, single pole double throw (SPDT) switches, and the antenna. Future trends consider that these components will be built in silicon, with PA, LNA, and SPDT built on GaN/Si. A large number of antenna elements and millimeter-wave modules are assembled into a panel in single or multiple planes. The elevation of the antenna beam is electronically controlled by adjusting the relative phase-shift of the feeding signals. The phased arrays are often two-dimensional (2-D), which makes it possible to steer the beam in the azimuth direction as well.

- 
2. Latency is defined as the time it takes for a digital command to do a roundtrip in the system.
  3. EIRP stands for effective isotropic radiated power and is obtained from the product of PA power output and antenna gain.

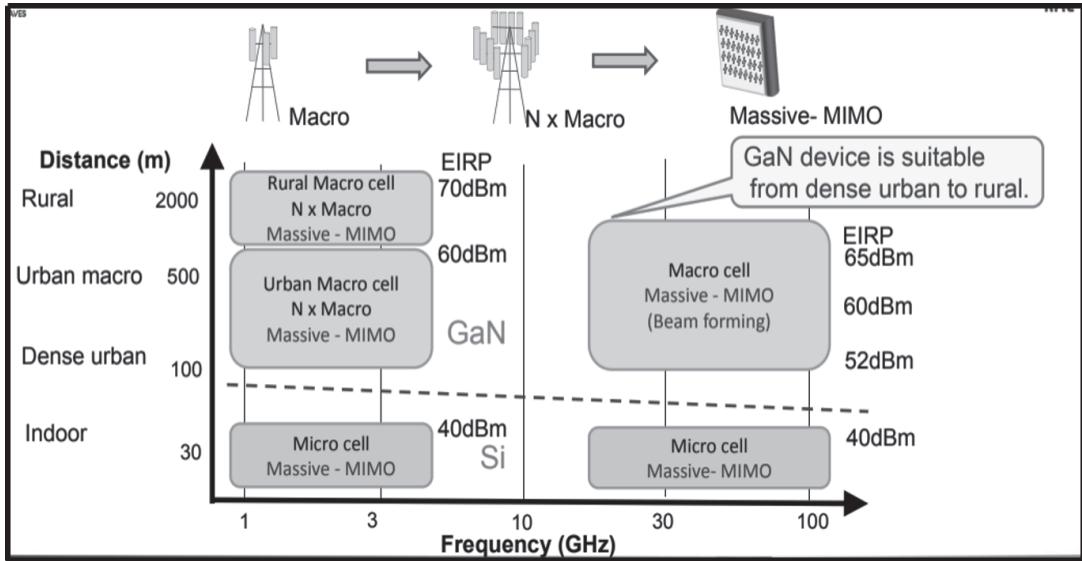


Figure 1.7 Dependency of frequency and technology on environment. (Courtesy of Mitsubishi [14].)

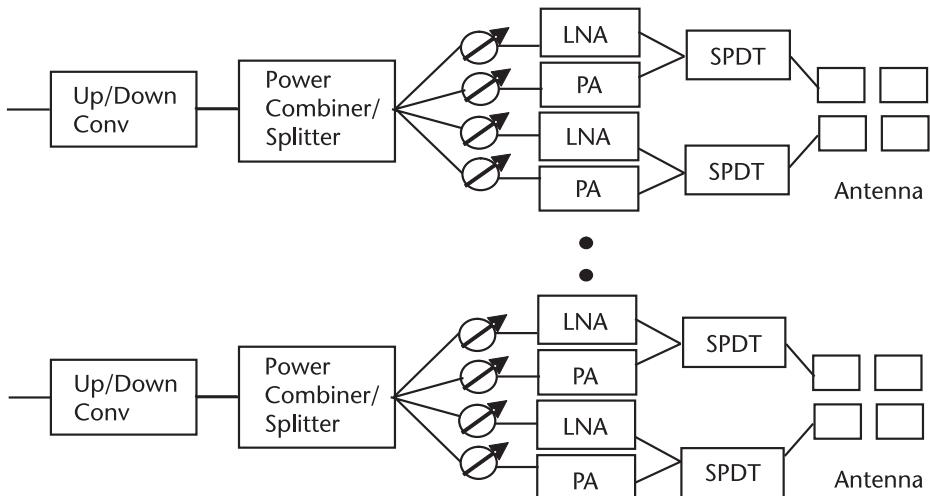


Figure 1.8 An analog option to design a millimeter-wave beam forming with 64 elements [16].

## 1.5 GaN-Based Power Amplifiers

We described the importance of the high-power amplifiers (HPAs) for millimeter-wave communication systems. We also touched upon its application in the next generation of mobile communication systems, the new 5G radio. The dotted line drawn in Figure 1.8 kind of separates the amplifier power into two levels. The low level, located below the dotted line, is for applications of cells up to 100m. Silicon-based technology will drive these applications. The driving technology above the line is mostly GaN-driven. The simple reason for this trend is that the main power consumption in any wireless system is concentrated in the HPA. GaN is the material that, since its introduction in late 1990s, has been shown to be the most efficient semiconductor material until the present time. In spite of Figure 1.8 being for 5G applications, it is also valid for a variety of other millimeter-wave applications.

The MMIC's HPA can be built with two different technologies, namely, microstrip line (MSL) and coplanar waveguide (CPW). Both technologies consist of a substrate on which the transmission lines, passive and active components, are fabricated. The most important difference between the two technologies is related to the location of the ground plane. In MSL technology, the signal plane is on the top and the ground plane is located on the backside of the substrate. In CPW technology, the signal and ground are both on the same plane. This makes coplanar technology easier and cheaper to fabricate than microstrip. Lower radiation losses, good electrical grounding, and lower parasitic effects are among the advantages of CPW. However, in power applications, MSL is the technology followed by the industry, due to the difficulty to evacuate the heat generated by the power devices in the CPW approach.

The discrete microwave devices migrated into the MMIC technology, which any circuit designer needs to master today. A good reference to learn details of the MMIC technology is [17]. However, the design of a 7-GHz amplifier is very different from the design of a 70-GHz amplifier. Due to a lack of material that can guide young engineers into millimeter-wave power design and its growing importance for the future, I decided to share the material contained in this book as a summary of my experience in power design. The design process and details discussed in this text are useful for the range 30 to 100 GHz. The main design goals of amplifiers for communications emphasizes power, efficiency, and linearity. In many cases, it is only possible to emphasize two of these objectives. The information collected here is applied to GaN, but it is also applicable to other technologies such as SiGe, GaAs, and InP.

## References

- [1] Kikkawa, T., et al., "Surface-Charge Controlled AlGaN/GaN-Power HFET Without Current Collapse and Gm Dispersion," *IEDM 2001*, Vol. 1, 2001, pp. 585–588.
- [2] Pengelly, R. S., et al., "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 60, No. 6, June 2012, pp. 1764–1783.
- [3] Micovic, M., et al., "GaN HFET for W-Band Power Applications," *Electron Devices Meeting*, San Francisco, CA, December 2006.
- [4] Boles, T., "GaN-on-Silicon Present Challenges and Future Opportunities," *Digest of the 12th European IC Conference*, 2017, Germany, pp. 21–24.
- [5] Gasmi, A. M., et al., "10W Power Amplifier and 3W Transmit/Receive Module with 3 dB NF in Ka Band Using a 100nm GaN/Si Process," *2017 IEEE Compound Semiconductor Integrated Circuit Symposium*, 2017.
- [6] Schellenberg, J. M., "Millimeter-Wave GaN SSPAs: Technology to Power 5G and the Future," *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium*, 2020.
- [7] Micovic, M., et al., "Robust Broadband (4 GHz–16 GHz) GaN MMIC LNA," *IMS2007*, 2007, pp. 1–4.
- [8] Ciccognani, W., et al., "An Ultra-Broadband Robust LNA for Defence Applications in AlGaN/GaN Technology," *IMS2010*, 2010, pp. 493–496.
- [9] Wang, F., et al., "An Improved Power-Added Efficiency 19 dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 54, No. 12, December 2006, pp. 4086–4099.
- [10] DeLisio, M. P., et al., "Power and Spectral Regrowth Performance of 10-W and 16-W Ka-Band Power Amplifiers with Single-Chip Output Stages," *IEEE MTT-S, International Microwave Symposium Digest*, 2005, pp. 839–842.
- [11] McSpadden, J., et al., "E-Band Communications at Raytheon: Potential Applications and Technologies," *Workshop on E-Band Communications: Market, Technology and IC Design*, *IMS2016*, San Francisco, CA, 2016.
- [12] Chen, Y. -K., "Emerging Ultra Broadband RF SoC Technologies," *IEEE International Microwave Symposium, Workshop on Exploratory Semiconductor Devices for the 5G mm-Wave Era and Beyond*, Boston, MA, 2019.
- [13] Andrews, J. G., et al., "What Will 5G Be?" *IEEE Journal on Selected Areas in Communications*, Vol. 32, No. 6, June 2014, pp. 1065–1082.
- [14] Inoue, A., "Millimeter Wave GaN Device for 5G," *IEEE International Microwave Symposium, Workshop on Exploratory Semiconductor Devices for the 5G mm-Wave Era and Beyond*, Boston, MA, 2019.
- [15] Wannström, J., and K. Mallison, "Heterogeneous Networks in LTE," <https://www.3gpp.org/technologies/keywords-acronyms/1576-hetnet>, 2019.
- [16] Rebeiz, G. M., and L. M. Paulsen, "Advances in Low-Cost Phased Arrays Using Silicon Technologies," *2017 IEEE International Symposium on Antennas and Propagation*, 2017, pp. 1035–1036.
- [17] Marsh, S., *Practical MMIC Design*, Norwood, MA: Artech House, 2006.

# Models for GaN Technology

The high electron mobility transistor (HEMT) is an advanced heterostructure device that evolved from basic metal semiconductor field effect transistor (MESFET) [1]. It was initially developed on gallium arsenide (GaAs) material showing low noise and high gain characteristics. The advent of HEMTs on gallium nitride (GaN) built on silicon carbide (SiC) substrates offered a radio frequency (RF) technology with higher power density and higher power-added efficiency (PAE) compared to other semiconductor materials. Besides, it is capable of operating at millimeter-wave frequencies. This is possible due to its higher carrier transport and good thermal properties. So far, SiC is the preferred power substrate, due to its higher thermal conductivity compared to GaAs and silicon. However, the performance over silicon has already been demonstrated as a viable option and will dominate the consumer market. The objective of this chapter is to introduce some of the GaN technology properties to engineers who are entering into this design field. Throughout the text, the acronym FET is used as a reference to any field effect-based device, either MESFET, HEMT, or pHEMT for common electrical properties.

## 2.1 Passive Components

The substrate for passive components is not actually a GaN but a SiC material. There is no difference in the design of these components compared to GaAs substrates. It is just a difference in the dielectric constant, 10.2 for SiC and 12.5 for GaAs. Therefore, the review of this section can be applied to either technology. Most of the work on passive components has been developed for MIC thin-film technology and modified for MMIC design. A good recommendation before starting the design is to validate the models for the passive components when the project is based on a new foundry or a new design kit. That will help the designer to gain time in the design steps.

The passive circuit elements, such as capacitors, inductors, and transmission lines, are defined by analytic equations describing their electric function. However, such equations are not capable to accurately define such elements when laid out on a semiconductor substrate. They are better described by an electromagnetic analysis of the structure to obtain their electric function. The former is called by some engineers as circuit level (CL) and others use the term closed form (CF). In this book, we refer to the electric models by the abbreviation EE and EM designates a model generated from electromagnetic analysis.

### 2.1.1 Microstrip Line

A microstrip line is the most popular passive element in MMICs. Commercial simulators and/or foundries use proprietary equations to describe microstrip parameters. Figure 2.1 shows the geometry of the microstrip structure and the parameters defining its most important property, the line characteristic impedance. A second important parameter is the substrate dielectric constant that determines the line length. In a coaxial environment, the signal propagates in TEM mode, and the effective length of line is defined by the ratio between the length of wave on air and the square root of the dielectric constant. In a microstrip, the wave propagates between the strip conductor and the ground plane, but the fields are not entirely contained within the dielectric. This type of wave propagation in microstrip is called a quasi-TEM mode. The effective dielectric constant,  $\epsilon_{\text{eff}}$ , then replaces the dielectric constant to determine the microstrip line dimensions. The deposition of a thin metal layer on top of a high dielectric substrate is denominated as thin-film technology.

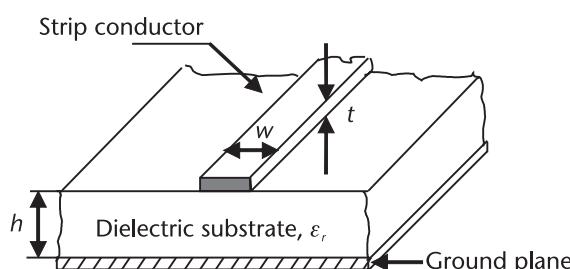
The physical length of the microstrip lines,  $l$ , are found by calculating the wavelength  $\lambda$ , in free space, divided by the effective dielectric constant, (2.1). If the speed of light,  $c$ , is in mm/s and the frequency in hertz, the line dimensions will be in millimeters.

$$l = \frac{c}{f} \frac{1}{\sqrt{\epsilon_{\text{eff}}}} \quad (2.1)$$

The closed-form expressions to synthesize microstrip lines, was developed by Hammerstead [2]. He proposed four equations, (2.2) to (2.5), to determine the impedance and effective dielectric constant as a function of the line dimensions and the substrate dielectric constant. Notice that the equations are a function of the ratio  $w/h$ .

For  $w/h \leq 1$ ,

$$Z_0 = \frac{60}{\sqrt{\epsilon_{\text{eff}}}} \ln \left( \frac{8h}{w} + \frac{1}{(4h)} \right) \quad (2.2)$$



**Figure 2.1** Microstrip line geometry.

where

$$\epsilon_{\text{eff}} = \frac{(\epsilon_r + 1)}{2} + \frac{(\epsilon_r - 1)}{2} \left( \frac{1}{\sqrt{1 + \frac{12h}{w}}} + 0.04 \left(1 - \frac{w}{h}\right)^2 \right)$$

For  $w/h > 1$ ,

$$Z_0 = \frac{120\pi}{\epsilon_{\text{eff}}} \left( \frac{w}{h} + 1.393 + 0.667 \ln \left( \frac{w}{h} + 1.444 \right) \right) \quad (2.3)$$

where

$$\begin{aligned} \epsilon_{\text{eff}} &= \frac{(\epsilon_r + 1)}{2} + \frac{(\epsilon_r - 1)}{2} \left( \frac{1}{\sqrt{1 + \frac{12h}{w}}} \right) \\ \epsilon_r &< \epsilon_{\text{eff}} < \frac{\epsilon_r + 1}{2} \end{aligned}$$

Hammerstead also proposed equations for the reverse calculation, that is,  $w/h$  as a function of impedance,  $Z_0$ , and  $\epsilon_r$ .

For  $w/h \leq 2$ ,

$$\frac{w}{h} = \frac{8 \exp(A)}{\exp(2A) - 2} \quad (2.4)$$

For  $w/h > 2$ ,

$$\frac{w}{h} = \frac{2}{\pi} B - 1 - \ln(2B - 1) + \frac{\epsilon_r + 1}{2\epsilon_r} \left[ \ln(B - 1) + 0.39 - \frac{0.61}{\epsilon_r} \right] \quad (2.5)$$

where

$$\begin{aligned} A &= \frac{Z_0}{60} \sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{2\epsilon_r} \left[ 0.23 + \frac{0.11}{\epsilon_r} \right] \\ B &= \frac{377\pi}{2Z_0\epsilon_r} \end{aligned}$$

The substrate heights in MMIC processes are typically between 100 and 200  $\mu\text{m}$  for microwave applications and 50 and 75  $\mu\text{m}$  for millimeter-wave applications. The reason for smaller thickness at higher frequencies is the minimization of radiation losses and of phase velocity dispersion. This makes the fields more concentrated under the transmission line. According to the equations above, a  $50\Omega$  line is built with a trace width between 50 and 100  $\mu\text{m}$ . The minimum line width,  $w$ , for thick

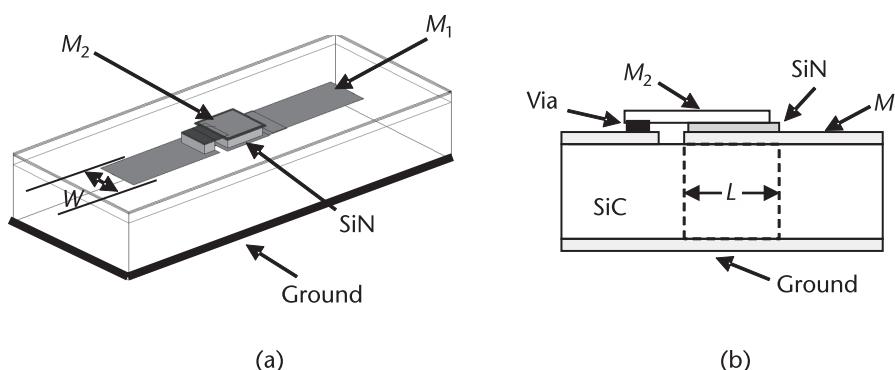
transmission lines is 5  $\mu\text{m}$  and 2  $\mu\text{m}$  for thin transmission lines. They correspond, respectively, to a characteristic impedance of 102 $\Omega$  and 122 $\Omega$ , for a 50- $\mu\text{m}$ -thick substrate. Such a line is lossy, and its application is tolerated when the line is short. The thick lines are in order of 3 to 5  $\mu\text{m}$ , while thin metal lines are between 1 and 2  $\mu\text{m}$ . On the other extreme, 15 $\Omega$  results on a large line width, say, 300  $\mu\text{m}$  wide. These numerical values for the dimensions represent only the order of magnitude, as each foundry has its own rules. These equations are useful for synthesizing microstrip circuits, constituting what we call an electrical model.

### 2.1.2 Series Capacitors

This is a parallel plate capacitor, composed of two plates of metal with a thin, high dielectric constant material between them. In the MMIC world, it is called a metal-insulator-metal (MIM). They are used for DC current isolation and impedance matching. A magnified view of a MIM is in Figure 2.2(a), constructed on top of metal  $M_1$ , right after a gap in the microstrip line. The capacitor cross-section is in Figure 2.2(b). The capacitor, with dimensions  $W \times L$ , is composed of the top plate  $M_2$  and the bottom plate  $M_1$ , together with a dielectric layer. Both plates share the same microstrip ground plane, performing as a section of transmission line. Therefore, for modeling purposes, we split the capacitor into two transmission lines, each measuring  $W \times L/2$ . Between the lines, we insert an ideal lumped capacitor whose dimensions define the capacitance, according to (2.6).

$$C = \frac{(\epsilon_r \epsilon_0 L W)}{d} \quad (2.6)$$

where  $L$  = length of capacitor in  $\mu\text{m}$ ,  $d$  = dielectric thickness = 0.22  $\mu\text{m}$ ,  $W$  = width of capacitor in  $\mu\text{m}$ ,  $\epsilon_r$  = relative dielectric constant, and  $\epsilon_0$  = dielectric constant free space =  $8.854 \times 10^{-12}$  F/m.



**Figure 2.2** MIM capacitor: (a) 3-D view, and (b) cross-section view.

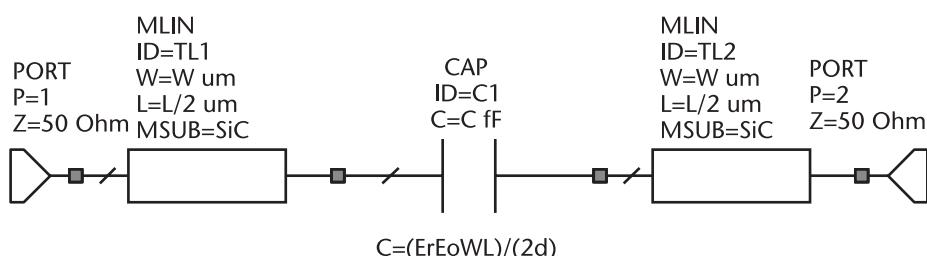
The electrical model of a series MIM capacitor is in Figure 2.3. The capacitance value is given by the lumped value and the frequency effects by the transmission lines. The contact between the top of capacitor  $M_2$  and the microstrip is implemented by means of an air bridge over the gap. The air bridge for contacting the layers can be represented by an additional transmission line. This additional line is not included in the model, because its dimensions are determined by the foundry technology. The electric fields propagating within the SiC substrate from left to right under  $M_1$  spreads through the dielectric material and the SiC. After the air bridge, the electric field continues propagating under  $M_1$  and the ground.

The dielectric materials mostly used are silicon nitride (SiN) and silicon dioxide ( $\text{SiO}_2$ ). The former has a dielectric constant,  $\epsilon_r$ , of 6.7 and the latter has a dielectric constant of 3.8. The dielectric thickness range used by most foundries is between 0.15 and 0.25  $\mu\text{m}$ . The capacitance typical dimensions for SiN used in millimeter-wave MMIC, using square geometry, range from  $L = 10$  to 100  $\mu\text{m}$ . Assuming a SiN material and dielectric thickness of 0.22  $\mu\text{m}$ , this range corresponds to capacitance values between 30 and 3 pF.

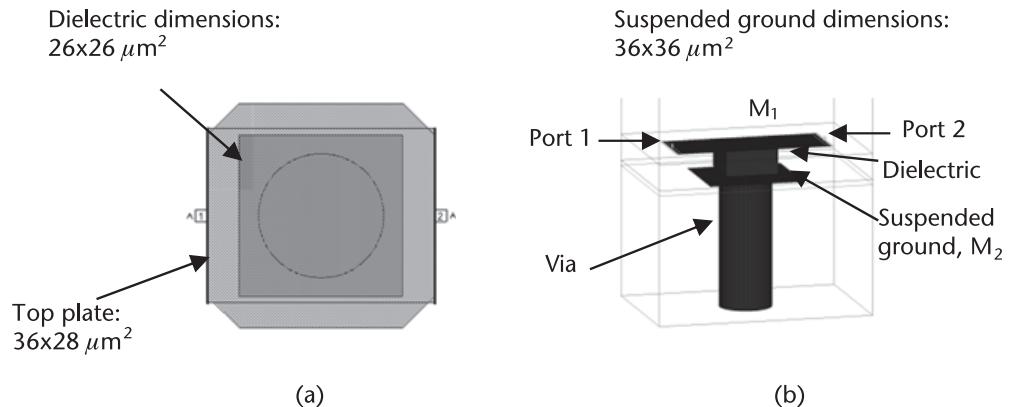
### 2.1.3 Shunt Capacitors

Shunt capacitors are useful for DC bypass and matching purposes. Nowadays they are available on top of via from most foundries. The layout view in Figure 2.4(a) shows a via represented by a circle, the top view of the dielectric material, and the top plate and suspended ground plate. The 3-D view of the capacitor is in Figure 2.4(b), showing the same elements. One can identify three main parts, namely:

1. The capacitor itself is represented by the dielectric material sandwiched between the top plate  $M_1$  and the suspended ground at metal  $M_2$  level. A lumped capacitor is used to simulate the capacitor action.
2. The air transmission lines between the dielectric and the edges of the capacitor are represented by an RLC circuit.
3. The air bridge that connects the top of capacitor  $M_2$ , to the microstrip on metal  $M_1$ , represented by a short air transmission line.



**Figure 2.3** Equivalent model for the MIM capacitor.



**Figure 2.4** Layout and 3-D view of capacitor on top of a via: (a) capacitor layout on top of a via, and (b) 3-D view of the capacitor.

The model representing these parts is shown in Figure 2.5. The model validity was confirmed by EM simulations for various capacitor values. However, the transition of the suspended ground to the common ground is not taken into account, in this simple equivalent model. Besides, if the capacitor is close to other transmission lines, there are couplings that degrade the accuracy of the model. It is a good element to start a design, and its real effect is obtained from EM analysis.

The contact from the top to the bottom of the chip, called via, is modeled by a series RL circuit, with the values found from EM analysis, calculated from (2.7) and (2.8). In the equations,  $h$  represents the substrate thickness. The via height unit is in μm, the resistance is in ohms, and the inductance is in pH.

$$R = \frac{0.125}{h} \quad (2.7)$$

$$L = \frac{14}{h} \quad (2.8)$$

The parameters defined in Figure 2.5 are valid as long as the top metal dimensions ( $36 \times 28 \mu\text{m}^2$  for this particular example) do not change. Only the dielectric dimension,  $L_c$  and  $W_c$ , varies as a function of the desired capacitance. If there is a variation in the width of the top metal, then the model has to be recalibrated with EM analysis.

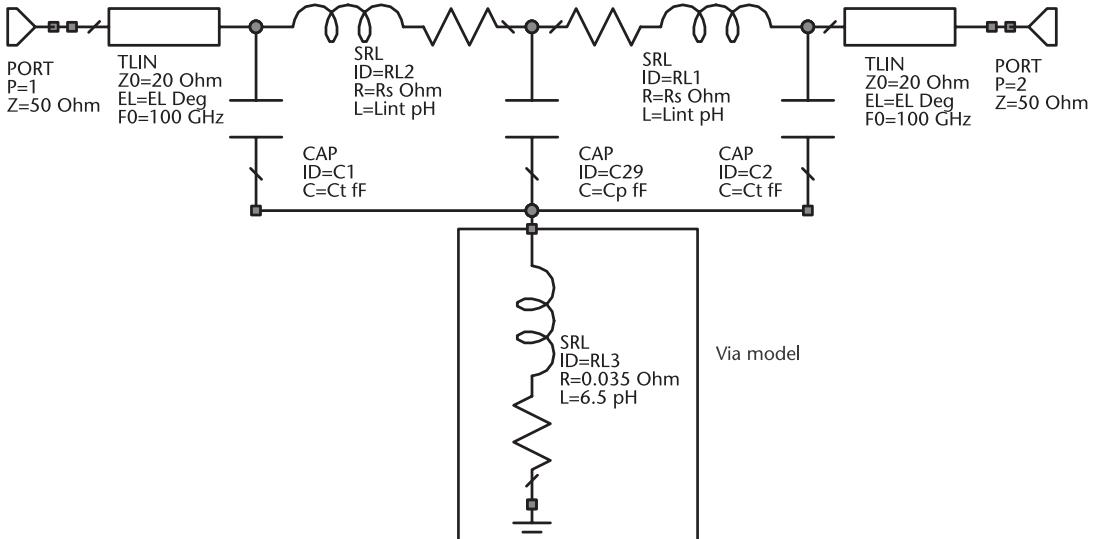
$L_c$  = capacitor length in μm;

$L_{\text{int}} \times C_t$  = model for capacitor top plate;

$W_c$  = capacitor width in μm;

$L_{\text{int}} = (40 - L_c)/2$ ;

$R_S$  = inductor losses =  $0.18\Omega$ ;



**Figure 2.5** Schematic representing a MIM capacitor on top of the via.

$$C_p = 0.001 \times 8.854 \times 6.7 \times L_c \times W_c/d \text{ fF};$$

$d$  = capacitor thickness = 0.2  $\mu\text{m}$ ;

EL = transmission line angle =  $(-10.5 + L_c/2)$ ;

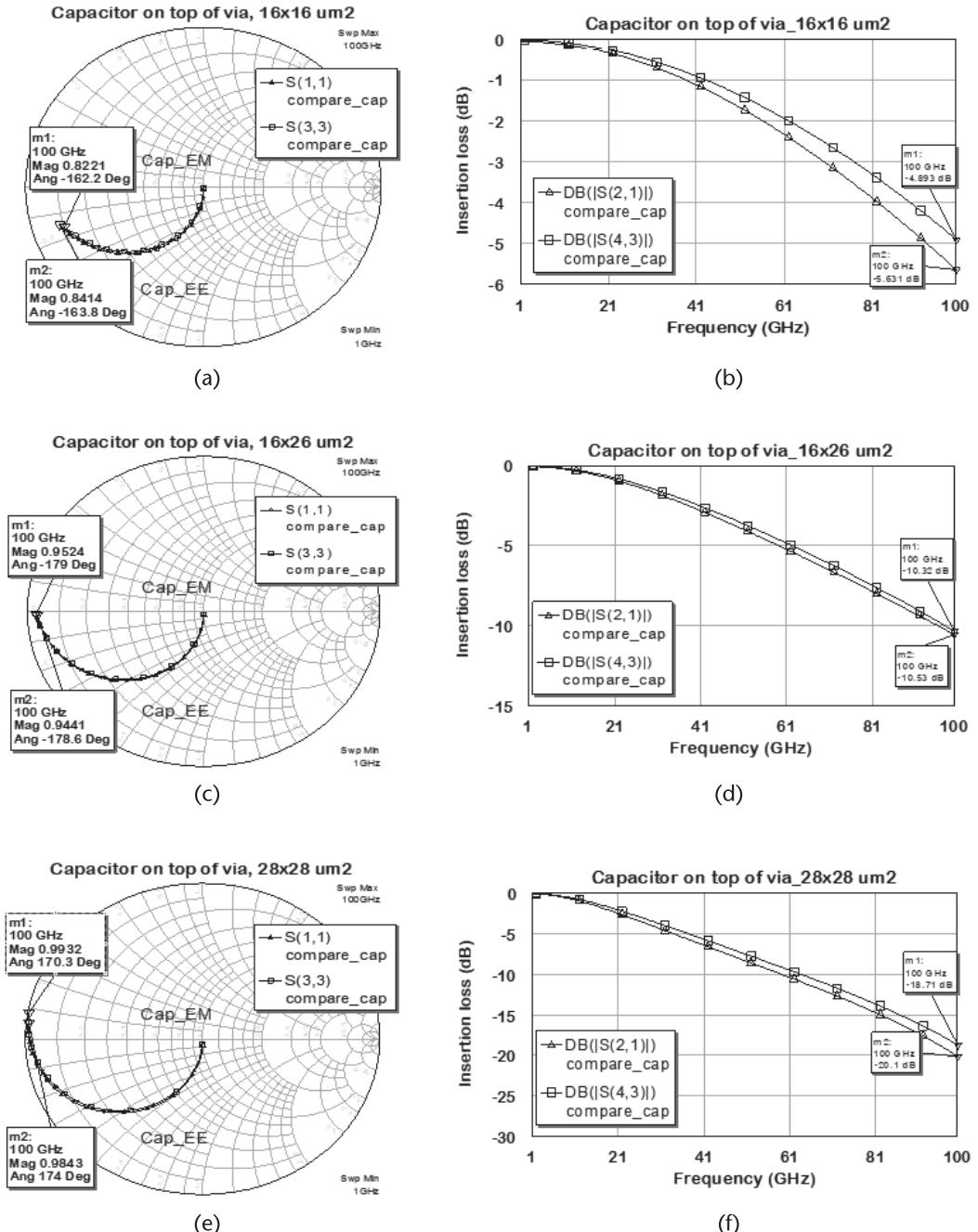
$$C_t = 0.001 \times 8.854 \times 0.5 \times (40 - L_c) \times W_c/(L_c \times d) \text{ fF}.$$

One should keep in mind that, in many instances, the capacitor in the layout is near a large width transmission line creating a strong coupling. As a result, the capacitor value is no longer correct. The EE model then needs to be modified by the EM model for the particular circuit. The definition of parameters for the capacitor on top of the via are as follows.

When performing the EM of the complete circuit, the capacitor dimensions have to be adjusted to represent the desired electrical behavior. Low capacitor values need to be carefully considered. They have to be within the foundry minimum dimensions, specifically for the capacitor on top of the via.

A lower limit from GaN millimeter-wave foundries is in the order of  $10 \times 10 \mu\text{m}^2$ . The EE model was compared to EM analysis for three different capacitor sizes, within the frequency range between 1 and 100 GHz. The results are shown in Figure 2.6. One can see that the input  $S_{11}$  for both EE and EM models have a reasonable agreement over frequency. A difference in the transfer parameter  $S_{12}$  is observed, which is larger at the high end of the band. A maximum difference of 1.4 dB is observed for the larger size capacitance.

A note should be mentioned about the suspended ground. Some foundries use a circular ground, and others use a square or a square with chamfered corners. These shapes affect the capacitance. The simulations shown in Figure 2.6 are for a suspended ground with squared chamfered corners. The self-resonance of a capacitor makes it an ideal element to DC bypass biasing lines.

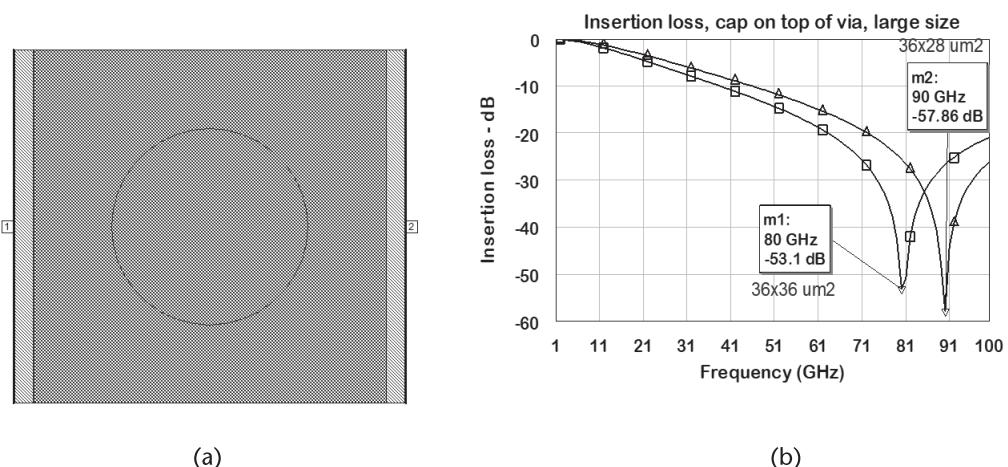


**Figure 2.6** MIM capacitors for three different dimensions:  $16 \times 16 \mu\text{m}^2$ ,  $16 \times 26 \mu\text{m}^2$ , and  $28 \times 28 \mu\text{m}^2$ : (a)  $16 \times 16\_S11$ , (b)  $16 \times 16\_S21$ , (c)  $16 \times 26\_S11$ , (d)  $16 \times 26\_S21$ , (e)  $28 \times 28\_S11$ , and (f)  $28 \times 28\_S21$ .

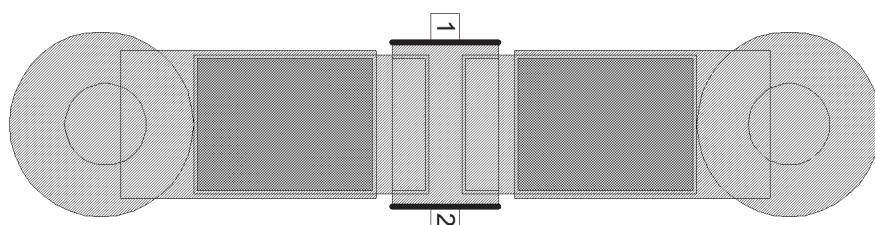
The layout shown in Figure 2.7(a) is for a top plate measuring  $36 \times 36 \mu\text{m}^2$ , with a squared ground plane. The resulting EM analysis, in Figure 2.7(b), shows that the circuit resonates at 63 GHz. Decreasing the capacitor's dimensions to  $36 \times 28 \mu\text{m}^2$ , we observe that the resonance increases to 90 GHz.

To bypass frequencies below 60 GHz, a larger capacitor is necessary. In general, there are limitations from the foundry regarding the maximum size of the suspended ground. So larger capacitors on top of the via are not always feasible. The most common alternative is to insert a capacitor at each side of a microstrip line and a ground via. The layout for this structure is in Figure 2.8, and the corresponding electrical model is in Figure 2.9.

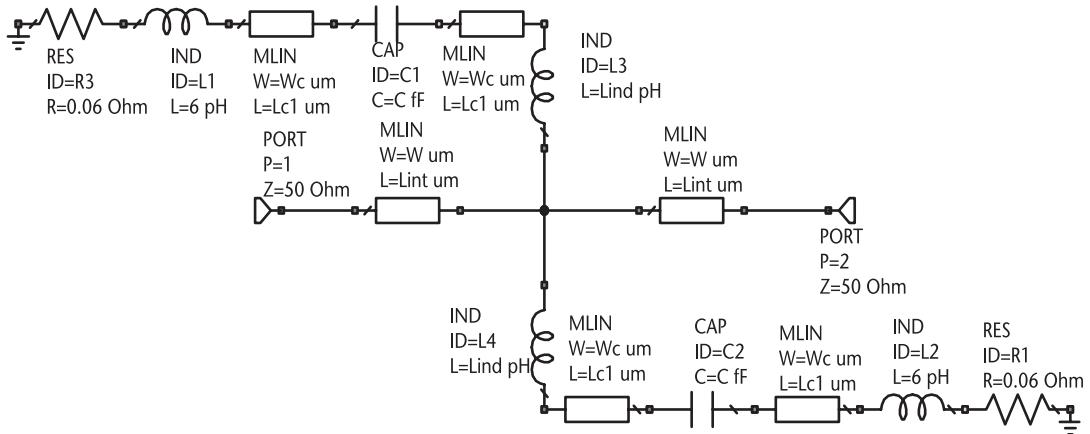
Each capacitor between the line and the via is a transmission line with the common ground reference. The EE models for the microstrip lines are from the Cadence AWR design kit. The parameter dimensions are in Table 2.1. The input S-parameters for both EM and EE models are in Figure 2.10(a). The input impedance shows that the circuit self-resonates at 31 GHz. The isolation is shown in the rectangular plot in Figure 2.10(b).



**Figure 2.7** Insertion loss and layout of MIM capacitors on top of the via with a squared ground. (a) Layout for a capacitor measuring  $36 \times 36 \mu\text{m}^2$ . (b) Insertion loss for  $36 \times 28 \mu\text{m}^2$  and  $36 \times 36 \mu\text{m}^2$ .



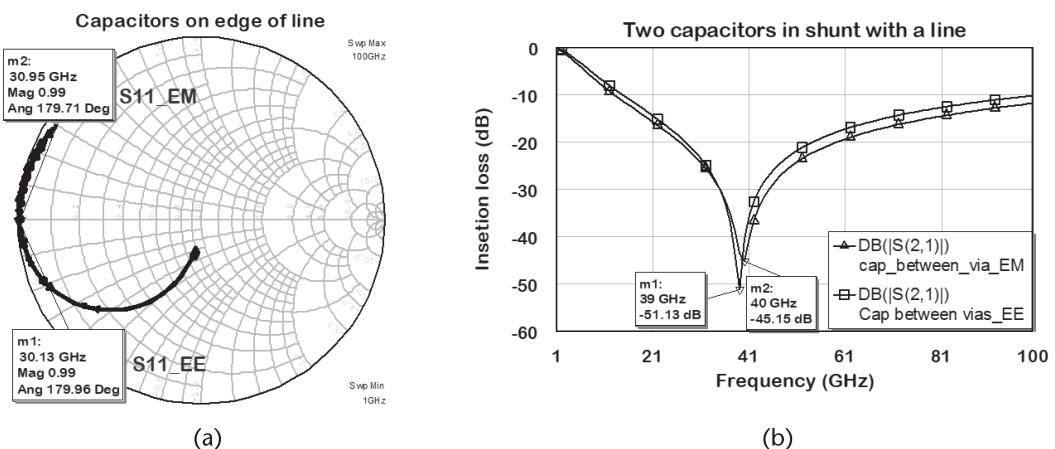
**Figure 2.8** Top view of layout for two MIM  $32 \times 43 \mu\text{m}^2$  capacitors in shunt with the transmission line.



**Figure 2.9** Schematic for two capacitors in shunt with the transmission line.

**Table 2.1** Two Shunt Capacitor Circuit Parameters

Parameters	Values	Parameter	Values
$W_c$ ( $\mu\text{m}$ )	32	$d$ ( $\mu\text{m}$ )	0.15
$L_c$ ( $\mu\text{m}$ )	43	$L_{c1}$	$L_c/2$
$L$ ( $\mu\text{m}$ )	20	$L_{\text{ind}}$ ( $\mu\text{m}$ )	4
$E_r$	6.7		
C	$0.001 \times 8.854 \times E_r \times L_c \times W_c / d$ , fF		



**Figure 2.10** Performance of the MIM shunt capacitor with impedance resonance at 30.2 GHz and isolation at 45 GHz. (a) Comparing  $S_{11}$  EM and EE models. (b) Comparing  $S_{21}$  from EM and EE models.

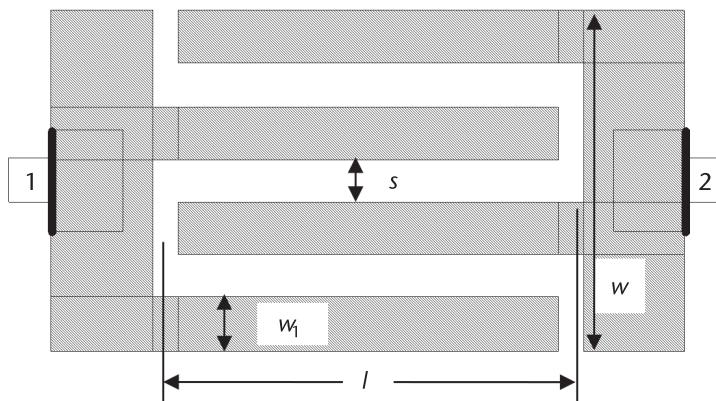
The maximum isolation is at 39 GHz and does not match the impedance resonance. However, this is not important if the circuit is used for bias. The important parameter is the isolation between ports 1 and 2. The resulting reactance at this frequency can be absorbed by the bias line reactance. The accuracy of this model to predict the isolation frequency shows less than 2.5% difference compared with the EM simulation.

#### 2.1.4 Interdigital Capacitors

The interdigital capacitor, shown in Figure 2.11, is based on the coupling of signals between metal fingers, separated by a few microns. The minimum distance between metals is determined by the foundry selected for the design. To behave as a lumped capacitor, the component length must be below  $\lambda/10$ . This type of capacitor was originally studied for MIC applications [3], with equations to determine the equivalent capacitance at microwave frequencies as a function of the topology dimensions. However, they are not sufficiently accurate for millimeter-wave MMIC circuit design. It is preferred to use an analytical EE or EM-based model from coupled lines.

The original work suggests maintaining the ratio  $W/l = 1$  and the  $S = W_1$  for the best representation of a capacitor. The topology of Figure 2.12, with the following initial parameters,  $W_1 = S = 0.01$  mm, substrate thickness = 50  $\mu\text{m}$ , and  $l = 0.080$  mm, was simulated over the band of 1 to 100 GHz. The coupled-line model in Figure 2.12, available on Cadence AWR, makes use of an EM quasi-static formulation described in [4].

The comparison between the coupled-line model and EM analysis is in Figure 2.13(a) for the amplitude of the transmission coefficient and in Figure 2.13(b) for the phase of the transmission coefficient. The coupled-line model shows a difference of 1.7 dB at 100 GHz compared to the EM model. The phase difference at 100 GHz is less than 6°. This structure corresponds to a capacitor of 20 fF with dimensions of  $65 \times 65 \mu\text{m}^2$ .



**Figure 2.11** Layout of an interdigital capacitor.

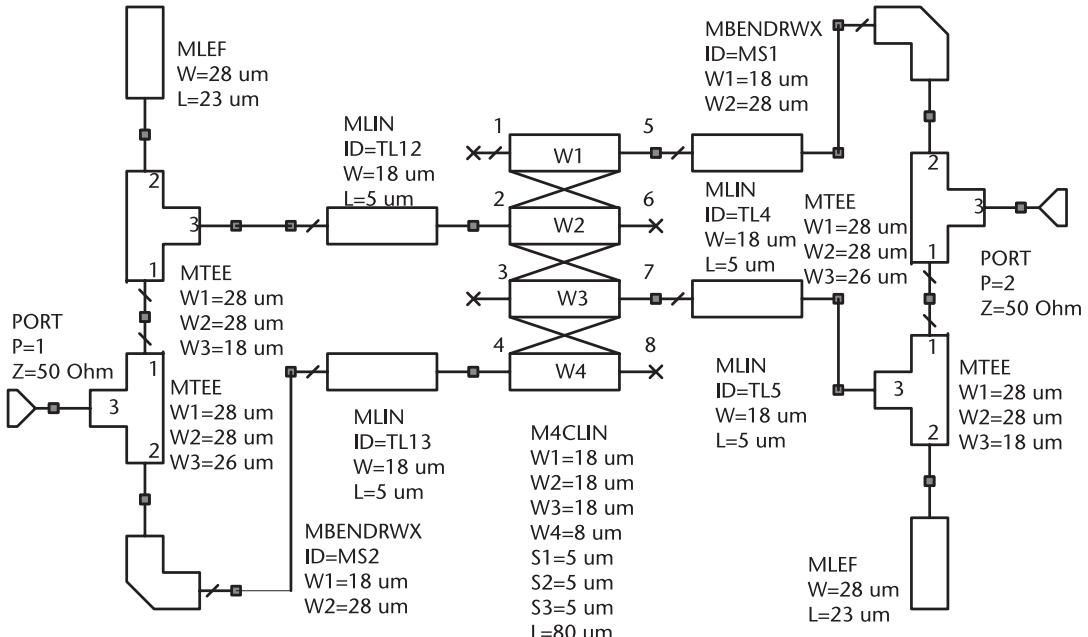


Figure 2.12 Electrical model for the interdigital capacitor.

### 2.1.5 Thin-Film Resistors

MMIC resistors are composed by a thin layer of resistive material. Nickel chrome (NiCr) and tantalum nitride (TaN) are the materials allowing stable resistance over temperature and are available with a specific resistance of 20 to 100  $\Omega/\text{square}$ . The resistor is connected to the gold trace by a special alloy that has a small parasitic resistance. This is included in the resistor model when using a foundry's design kit. The model is similar to the parallel plate capacitor, where a lumped resistor is sandwiched between two series microstrip lines, with the same width as the resistor itself. The model representation is presented in Figure 2.14 and does not consider the contact resistance.

The resistivity used in the simulations that follow is equal to  $50 \Omega/\text{square}$ . In order to have an insight on the validity of the resistor electrical model, let us do an EM simulation of a  $25\Omega$  resistor for different resistor sizes, namely,  $11 \times 22 \mu\text{m}^2$ ,  $18 \times 36 \mu\text{m}^2$ , and  $30 \times 60 \mu\text{m}^2$ .

The simulation results in Figure 2.15(a) show the EE reactance in dotted lines and the EM values in solid lines. Only the reactive results are shown since the resistances are fairly constant over the frequency. The EM simulation shows higher reactance, with a difference of 20% at 20 GHz and 50% to 100% at 100 GHz. The reactances for the  $25\Omega$ ,  $50\Omega$ , and  $100\Omega$  resistors in Figure 2.15(b) obtained from EM analysis also show higher values for the  $25\Omega$  and  $50\Omega$  resistors, compared to EE models. The  $100\Omega$  resistor in particular shows a positive reactance for the EM and a negative reactance for the EE. The observed behavior suggests using a simple

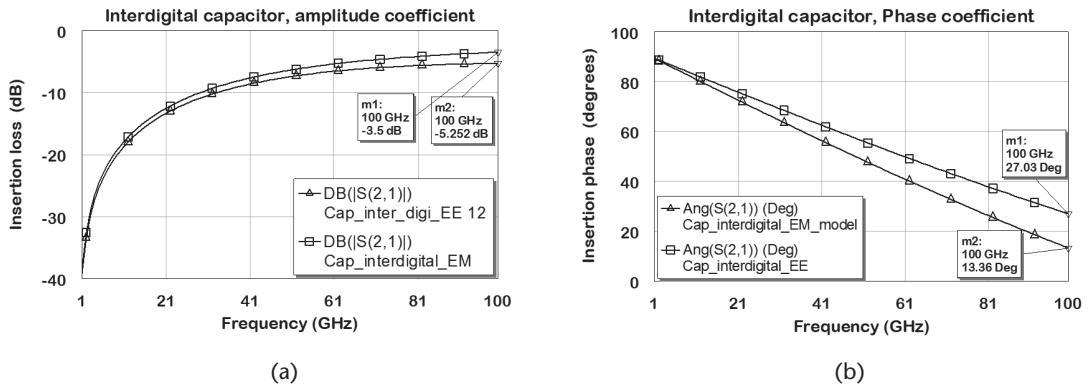


Figure 2.13 Comparing capacitances from EE with EM model: (a) amplitude transmission coefficient, and (b) phase transmission coefficient.



Figure 2.14 MMIC model for a resistor.

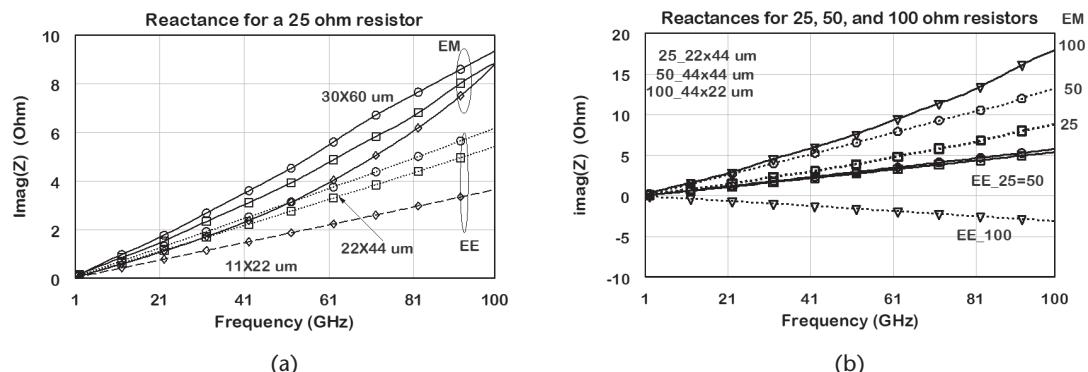


Figure 2.15 Comparing EM and EE models for typical resistors sizes for RF applications: (a) 25 $\Omega$  resistor for three different sizes, and (b) 25 $\Omega$ , 50 $\Omega$ , and 100 $\Omega$  resistors.

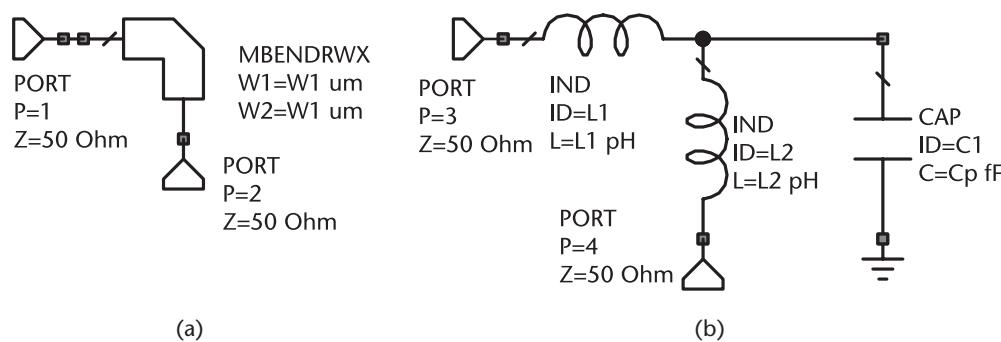
resistor model for the high-frequency simulations. The reactive effects are then taken care of during the EM analysis.

There are two other passive models that are important in MMIC design such as the bend and T-junction. A simple shunt capacitor is used to represent a bend model, shown in Figure 2.16. The bend accounts for the differences when the path of a line has to turn to the right or left under a certain degree. The most popular is the  $90^\circ$  bend. There are two situations to take into account. If the  $w/h$  ratio of the microstrip line is large, the fields tend to concentrate from the center to the inner corner. The other bend has lower fields and behaves as an open stub, shunting the signal. In order to compensate for that extra capacitance, in many instances, the corners edges are chamfered.

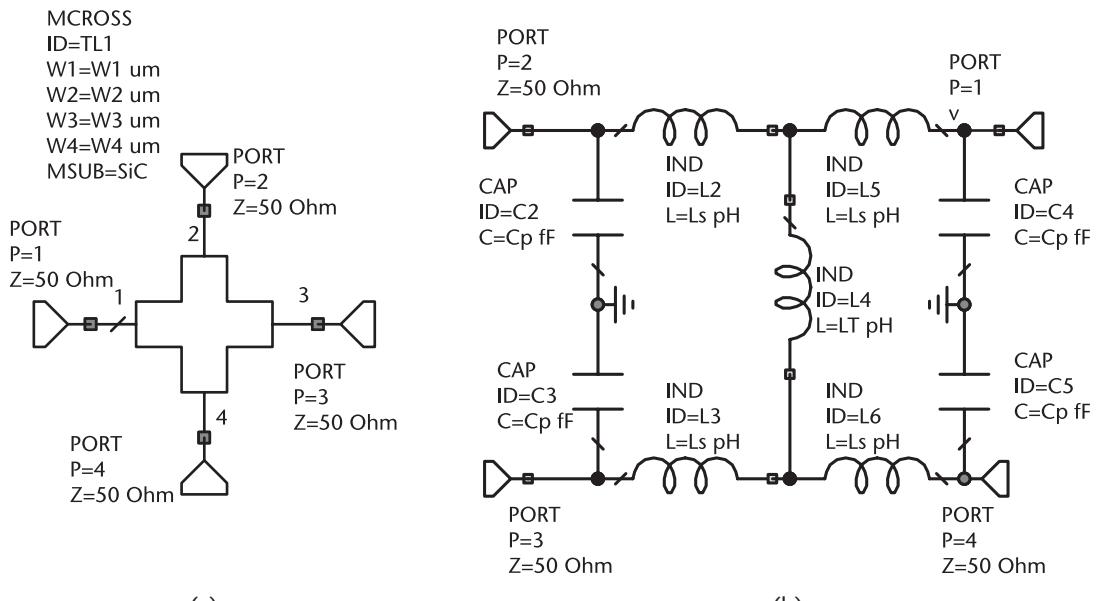
If  $w/h$  is small, then the microstrip trace is narrow. The fields tend to cut the corners. Therefore, the narrow lines reduce the effective line length compared to a straight line, while the thick lines introduce an extra phase shift. The models for considering the parasitic effects contained in commercial simulators work well in the preliminary stages of the design.

The MCROSS element is represented in Figure 2.17 by a microstrip model and an equivalent circuit. It takes into account the parasitics involved at the junction of a number of transmission lines at the same node. If their dimensions are different, then there are also fringing fields, predominantly at the larger microstrip width, contributing to the increase of the parasitic capacitances. The MTEE junction is a particular case of an MCROSS where ports 2 and 3 are merged, becoming a single port.

The values of the parasitic are also functions of the dielectric constant of the substrate and are function of the ratio  $w/h$  of the lines. In the case of millimeter-wave, this model is key to the design and layout of power combiners/dividers. Similar to the bend models, we do not need to create additional models, since the models contained in the commercial electric simulators have sufficient accuracy for the initial design phase.



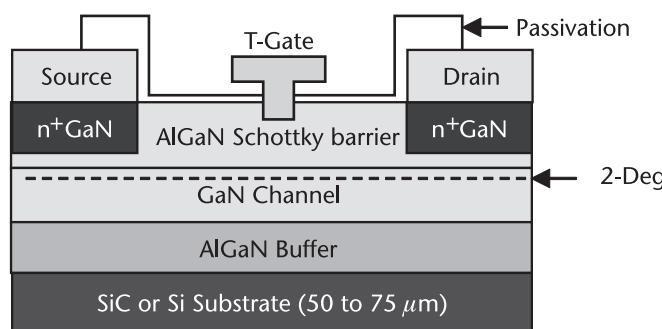
**Figure 2.16** Bends in the MMIC design: (a) microstrip bend, and (b) simplified equivalent circuit.



**Figure 2.17** Cross-sections in the MMIC design: (a) microstrip cross\_MCROSS, and (b) simplified equivalent circuit.

## 2.2 The GaN HEMT

The device cross-section for a typical double GaN HEMT (DHHEMT) device structure for millimeter-wave is shown in Figure 2.18 [5]. The name GaN heterojunction FET (DHFET) is also often used to denote the same device. The double structure device has superior performance compared with the single structure [6]. The HEMTs are built by thin crystal layers, denoted as epitaxial layers, grown on top of SiC substrates using either the metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) process. There are other substrates available such as sapphire, and aluminum nitride, but SiC gives the best trade-off between cost and performance.



**Figure 2.18** GaN DHFET device structure. (From: [5]. © 2020 IEEE.)

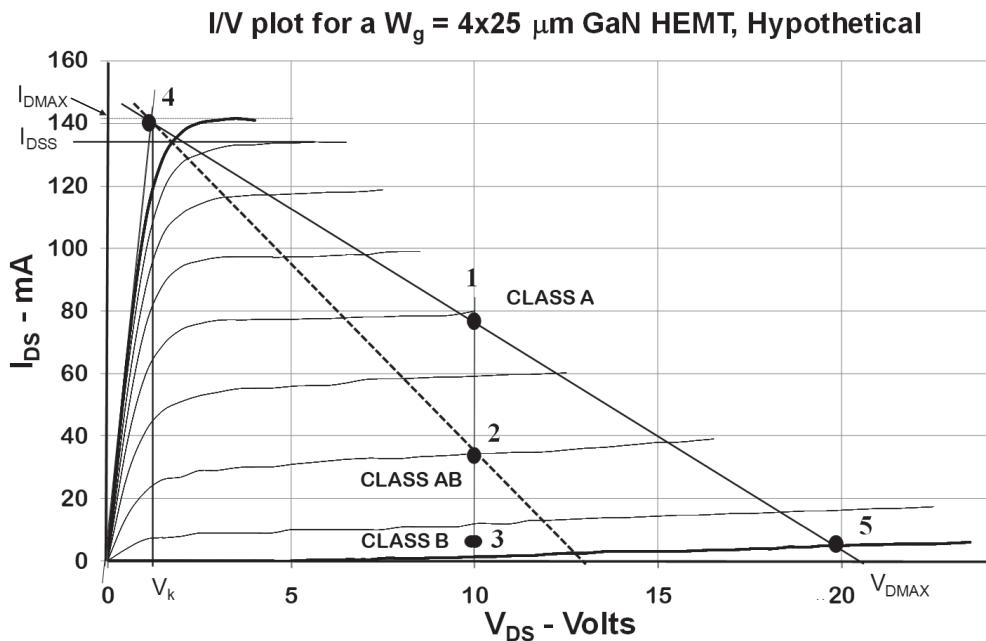
The SiC substrate acts as an excellent material to efficiently spread the heat from the active channel. Silicon is another option that is coming up as an important GaN carrier. The definition of the gate geometry is dependent on the photolithographic process employed. The optical process is capable of producing gate lengths in the order of 0.25  $\mu\text{m}$ , but millimeter-wave applications require a dimension below 0.2  $\mu\text{m}$ . For instance, gate lengths of 0.15  $\mu\text{m}$  can operate at Ka and V-bands, and 0.12  $\mu\text{m}$  and lower are adequate for operation at E and F-bands [7]. The technology used at the present time to reach these dimensions is the E-beam lithography. The gate dimension at the contact is narrow and follows a T-shape structure to minimize gate resistance. Most of the devices commercially available are built with aluminum gallium nitride (AlGaN)/GaN/AlGaN double heterojunction. The second junction is the buffer layer between the SiC and the GaN materials. That improves isolation from the substrate. Notice that the gate is built deep into the AlGaN material. This is called a recessed gate, which improves HEMT performance. The current path in the channel is indicated by the dotted line. The electrical properties of the 2DEG (2-D electron gas) are influenced by the AlGaN barrier thickness and the mole fraction of these elements. The sheet electron density can approximate concentrations of 0.8 to  $1.0 \times 10^2 \text{ cm}^{-2}$  [8], higher than those observed in other III-V materials. A GaN HEMT has been designed for the depletion and enhancement modes of operation. In the former, a negative gate voltage is applied to the gate to cut off the drain current, while in the latter, a positive gate voltage is applied to turn the drain current on.

The DC transconductance,  $G_m$ , and the  $f_T$  parameter scale roughly with the inverse of Schottky barrier thickness [9]. The Schottky barrier material also has an effect on device performance. For instance [10], devices with an InAlGaN barrier instead of an AlGaN layer exhibit higher drain current and breakdown voltage. The example in that reference showed an  $f_T$  of 113 GHz and an  $f_{\text{MAX}}$  of 230 GHz, for a gate length of 80 nm. The output power density reached 1 W/mm with a gain of 6.4 dB in load-pull measurements at 90 GHz.

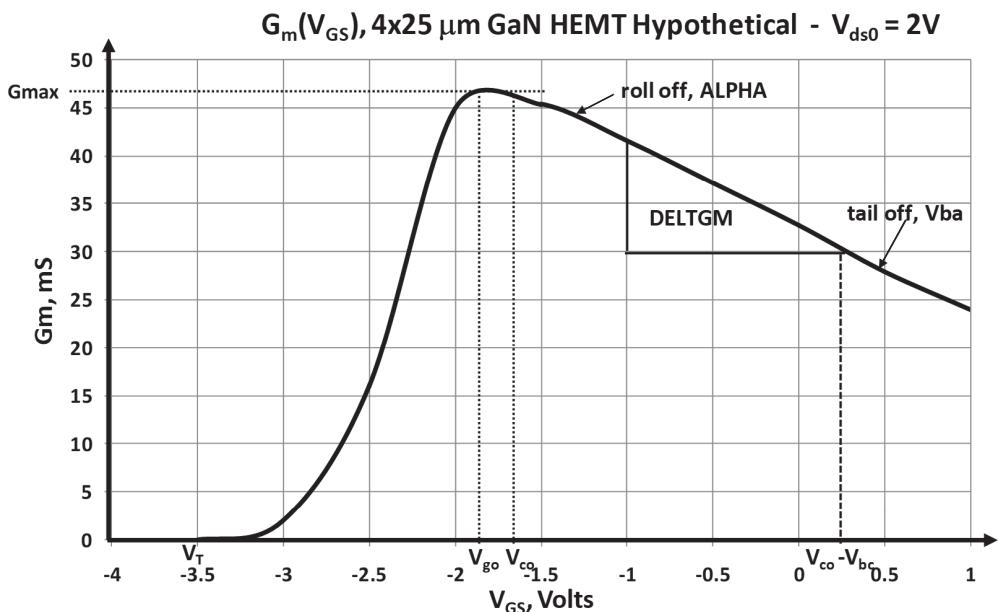
The typical pulsed I/V plot and transfer  $G_m(V_{gs})$  plot for a hypothetical GaN HEMT with a gate length of 0.125  $\mu\text{m}$  and gate periphery are represented in Figure 2.19, generated from reported results [11, 12]. Notice that the maximum drain current,  $I_{\text{DMAX}}$ , obtained from the tangent to the current in the saturation region, is in the order of 146 mA. Compared to a GaAs pHEMT device, one observes a softer transition from the linear region to the saturated region. This means that the  $I_{\text{DMAX}}$  value is not reached at low drain voltages, limiting the power capability.

The  $I_{\text{DSS}}$  current defined as the current at  $V_{GS} = 0$  is in the order of 135 mA. The  $V_{\text{DMAX}}$  is not limited by drain breakdown voltage like in GaAs technology, but by thermal limitations. It is determined from the power density that causes a maximum channel temperature of 150°C.

The knee voltage,  $V_k$ , in Figure 2.19 represents the intersection of the line tangent to the saturated current to the line tangent to the I/V curve in the linear region. The transconductance in Figure 2.20 presents an asymmetric shape. It rises steeply near turn-on and peaks around  $V_{GS} = -1.9\text{V}$  and then smoothly decreases with an increase in gate voltage. The parameters indicated in the figure are useful for the EEHEMT modeling.



**Figure 2.19** I/V from a hypothetical D mode GaN HEMT with a gate length,  $L_g = 0.125 \mu\text{m}$  for  $-3.5 < V_{gs} < 0.5$ , steps of  $0.5\text{V}$ .



**Figure 2.20**  $G_m$  from a hypothetical D mode GaN HEMT with a gate length,  $L_g = 0.125 \mu\text{m}$ .

## 2.3 DC Parameter Anomalies

The GaN power devices show some anomalies related to imperfections in the device technology. They create charge traps that capture electrons, whose effect does not show up immediately in the drain current. As a consequence, the DC and RF voltages and currents will be different, invalidating the quasi-static approach for nonlinear modeling. Currently, the improvements on the device technology have minimized these effects. The interest to the circuit designers lies on the following effects: current collapsing, gate and drain lag effects, lack of pinch-off, and the DC to RF dispersion.

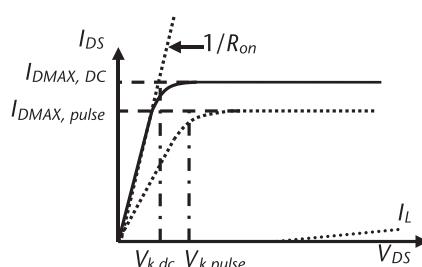
### 2.3.1 Current Collapse

The term current collapse is used to describe the reduction of drain current observed when the static DC I/V differs from the pulsed mode results, as detailed in Figure 2.21. They degrade the RF performance because they reduce the  $I_{D\text{MAX}}$  current and increase the value of the knee voltage,  $V_k$ . Similar effects have been observed [13] on GaAs HEMTs at low temperatures, in the early stages of development of the HEMT technology in the beginning of the 1980s. The proposed cause at that time is the same observed in present GaN HEMTs. The GaN surface contains charge traps, considered energy states in the semiconductor bandgap. They capture electrons reducing the sheet electron density in the channel needed to keep the overall charge neutrality. Lower electron density translates into lower  $I_{D\text{MAX}}$  and higher channel resistance,  $R_{\text{on}}$ .

The knee voltage increases, since  $V_k = I_{\text{max}} \times R_{\text{on}}$ , reducing the RF voltage swing.  $R_{\text{on}}$  accounts for the resistances between the drain and source terminals, and it is composed of four terms, according to (2.9).

$$R_{\text{on}} = 2R_C + R_{cb} + R_s + R_d \quad (2.9)$$

where  $R_C$  is the metal contact resistances,  $R_{cb}$  is the channel resistance, and  $R_s$  and  $R_d$  are the source and drain access resistances, respectively. The  $R_{\text{on}}$  resistance is determined by the inverse slope of the tangent to the I/V linear region curve on the I/V plot. The current collapse,  $I_{\text{coll}}$ , is usually expressed in terms of (2.10) in



**Figure 2.21** Ideal static and pulsed I/V plots.

percentage. At the present time, the state of the art for current collapse in GaN HEMTs technology is less than 10% [5].

$$I_{coll} = 100 \frac{I_{D\text{MAX,dc}} - I_{D\text{MAX,pulse}}}{I_{D\text{MAX,dc}}} \% \quad (2.10)$$

The injection of charges into the traps is mostly located at the drain side of the gate, due to the high electric field in the area. A technique used to minimize current collapsing is the introduction of a field plate [14] in that area, connected to the source or gate. That reduces the effect of the high electric field on the gate minimizing the current collapse. Unfortunately, this technique is not adequate for millimeter-wave, because it adds parasitic capacitance to the gate. Other solutions that successfully minimized the current collapse came from similar solutions employed by conventional HEMT technology. It consists in the passivation of the bare GaN surface between the gate and source and gate and drain. The most common passivation material is the SiN [15], but other materials have been tested as well [16]. The charge trapping can also be caused by lattice mismatches between the GaN epitaxial layer and SiC substrate. Buffer layers of AlGaN or InGaN materials have been introduced in between to minimize this problem [10].

### 2.3.2 Gate and Drain Lag

The transient response problems observed in GaN HEMTs include gate and drain lagging effects. Gate lag is a delayed response of the drain current with respect to the variation of the applied gate voltage and is usually related to the trapping mechanism located at the surface in the vicinity of the gate on the source side. However, drain lag is a delayed response of the drain current with respect to the variation of the applied drain voltage. Drain lag is also a trapping-related mechanism that usually occurs at the surface near the drain side of the gate. They are also dependent on the trapping occurring at the intersection of the GaN epitaxial layer and the substrate. Therefore, this effect and the current collapse are interrelated. Simple measurements of these effects appeared in [17] and summarized in Figure 2.22. For a better understanding of these effects, let us suppose that we apply a pulse signal to the gate and another to the drain. The lagging effects can be separated into three categories with respect to bias and type of pulse.

1. Assume that the quiescent device bias is  $V_{GQ} = 0$  and  $V_{DQ} = 0$ . Then a negative pulse is applied to the gate and a positive pulse is applied to the drain. Electric charges start filling the related traps at both the gate and the drain. Those are very fast effects compared to pulse duration. A normal I/V characteristic will result, as shown in Figure 2.22(a), for the plot corresponding to  $V_{gs0} = V_{ds0} = 0$ .
2. In the second case, the gate is biased at pinch-off and the drain is the same, that is,  $V_{GQ} = -V_P$ ,  $V_{DQ} = 0$ . A positive pulse is then applied to the gate starting at  $V_{GS} = -V_P$  towards 0. At the same time, a positive pulse is applied to the drain towards a positive voltage,  $V_{DS} = V_{DC}$ . Because the gate was

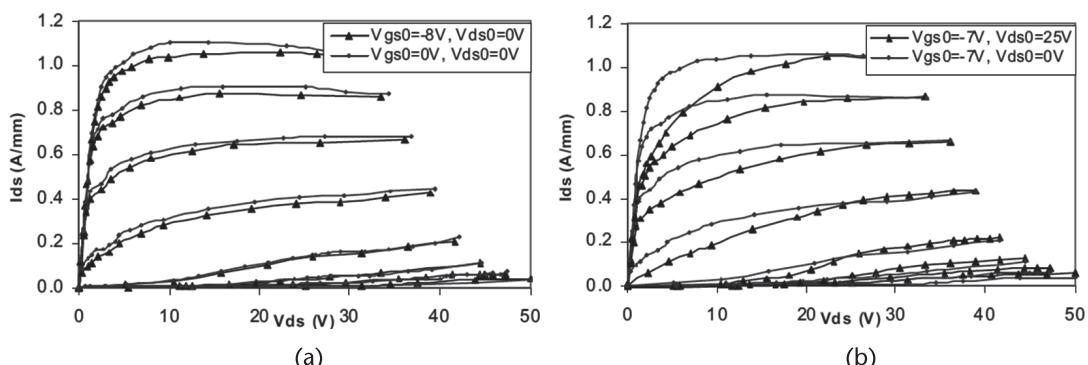
already biased, there is no immediate change on the charge trapped in the gate, but the traps at the drain are charged, changing its state. This results in a small current reduction due to drain lag. This condition is represented by  $V_{gs0} = -8V$ ,  $V_{ds0} = 0$  in the same figure.

3. The third case consists in starting with the device biased at  $V_{GSQ} = -V_p$ ,  $V_{DQ} = V_{DC}$ . All traps are filled with charge. Applying a positive voltage at the gate from the bias point towards 0, the effect is similar to the previous case. A negative pulse is applied to the drain, starting from  $V_{DC}$ , releasing the charges contained in the drain traps. If the pulse is positive starting from  $V_{DC}$ , the traps capture more free charges. The results for this condition are in the right plot of Figure 2.22(b), where  $V_{DC} = 24V$ .

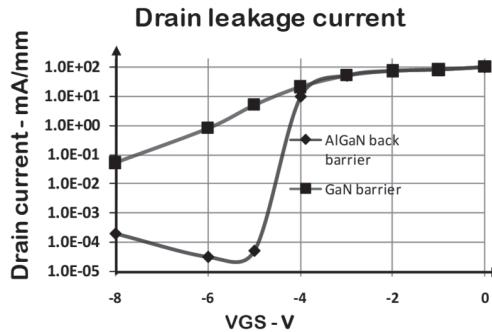
### 2.3.3 Poor Pinch-Off

This effect was originally observed in MESFETs when the gate dimensions are scaled down to  $0.1 \mu\text{m}$ . The name pinched-off described a total constriction of the channel. This term can cause confusion with the threshold voltage. The pinch-off voltage,  $V_p$ , is defined as the crossing of a line tangent to the curve  $I_{ds}(V_{gs})$  to 0. The threshold voltage,  $V_{th}$ , is the gate voltage that makes the drain current equal to 0. If we look closely at leakage currents in GaN HEMTs, we observe that the current goes down at a certain threshold voltage and starts to increase with more negative voltage. A poor pinch-off can be considered when the drain current becomes higher than  $0.1 \text{ mA/mm}$ . The drain leakage shown in Figure 2.23 is based on [16] for two types of back barriers.

This short channel effect has been minimized by device engineers, modifying the aspect ratio between the gate length and the barrier thickness, recessing the gate, and the mole fractions of the Schottky barrier material. The use of different compounds with InAlGa/GaN also has shown good improvements. A secondary cause for poor pinch-off is the leakage current coming from the buffer layer between



**Figure 2.22** Drain and gate lag measured at different quiescent bias points for a  $2 \times 50 \mu\text{m}$  AlGaN/GaN HEMT. Pulse length = 350 nS over a 30-μs period: (a) gate lag effects, and (b) drain lag effects. (From: [17]. © 2007 IEEE.)

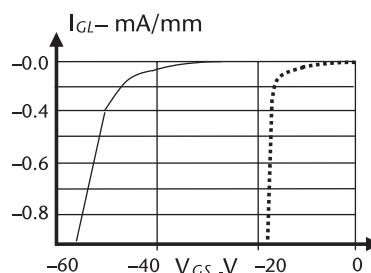


**Figure 2.23** Drain leakage currents (poor pinch-off) versus gate voltage. (From: [16]. © 2010 IEEE.)

GaN and SiC. This is more difficult to control, but using a different buffer material, a much better pinch-off characteristic has been achieved. An example of In-based buffer was reported in [10].

### 2.3.4 Gate Leakage

The gate leakage current,  $I_{GL}$ , is another important DC parameter that affects the GaN HEMT reliability. The leakage is generated by a reverse current in the Schottky junction and is more pronounced in short channels at high bias voltages. The reason for this leakage is dependent on several complex phenomena, including tunneling of electrons in the barrier. Some of the improvements in the technologies cited above contributed to minimize the leakage. Figure 2.24 shows improvements in the leakage from  $-18\text{V}$  to  $-42\text{V}$  with the use of recessed gate technology for the solid line [18]. In order to minimize most of these DC anomalies, foundries propose burning in the devices before usage. One of them [19] suggested biasing the device at  $V_{DQ} = 12\text{V}$  and adjusting the base plate temperature to maintain the  $T_{chan} = 175^\circ\text{C}$  for 200 hours. Another precaution is the effect of driving the power amplifier well above  $P_{1\text{dB}}$ . In some cases, it has been observed, during a second test, that the drain current and power performance changed, as if the threshold voltage had changed due to the stress. Readjusting the bias to the same current recovers the performance.



**Figure 2.24** Gate leakage currents versus gate voltage. (From: [18]. © 2016 IEEE.)

## 2.4 Temperature Dependence

Darwish et al. reported on the temperature parameters [20]. They measured a set of parameters of commercial AlGaN/GaN HEMTs devices from eight foundries. The gate length of the devices was between 0.1 and 0.25  $\mu\text{m}$ , and the width for all of them was 200  $\mu\text{m}$ . The temperature coefficients (TC) were measured according to (2.11).

$$\text{TC}(x) = \frac{\Delta x/x}{\Delta T} \quad (2.11)$$

The  $I_{DSS}$  temperature coefficient showed an average of  $-2.0 \text{ mA/mm}/^\circ\text{C}$ . To facilitate the reporting, the authors expressed TCs in parts per million; therefore,  $\text{TC}(I_{DSS}) = -2.0 \times 10^3 \text{ ppm}/^\circ\text{C}$ . The results for the main parameters are in Table 2.2. Notice that the temperature coefficient for  $I_{DSS}$  and  $gm\text{-dc}$ , measured at the peak, are very close to each other. The results for  $V_T$  are not in the table because they were not consistent; there were a group of devices with positive TC and a group with negative TC. However, their TCs are smaller, below  $0.5 \times 10^3 \text{ ppm}/^\circ\text{C}$ , and can be disregarded.

## 2.5 Unit Cell

The minimum elementary cell provided by most foundries is represented in Figure 2.25, consisting of two fingers: two sources, one at the top and one at the bottom of the device. The source contact is grounded with a plated via. At the center, one drain finger is located. The gate width of a FET is referred to as  $W_g$ . The width of a unit finger is referred to as unit gate width (UGW) of the transistor. The figure also shows a probe contact layout, consisting of two ground pads, connected to the ground by metalized via holes and a center contact for launching the signal in the device. There is a short transmission line from the center contact to the center of the device. This transmission line is important to give some separation from the pads to the device and to minimize the effects of transition from coaxial or coplanar probes to microstrip propagation. For millimeter-wave applications, one will find the minimum and maximum device width dimensions as 20  $\mu\text{m}$  and 800  $\mu\text{m}$ , respectively, depending on the frequency of operation. If more power is needed, then the unit cells are paralleled. Usually, sizes of 4 fingers, 8 fingers, and

**Table 2.2** Temperature Coefficients

Parameter	ppm/ $^\circ\text{C}$
TC ( $I_{ds}$ )	$-2.0 \times 10^3$
TC ( $gm\text{-dc.peak}$ )	$-2.2 \times 10^3$
TC ( $R_{on}$ )	$4.5 \times 10^3$
TC ( $V_k$ )	$1.6 \times 10^3$

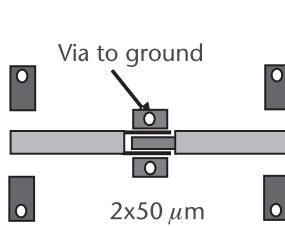


Figure 2.25 Two-finger unit cell.

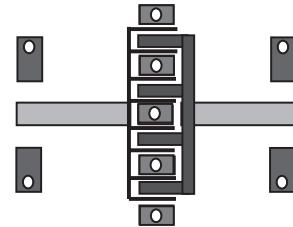


Figure 2.26 Eight-finger unit cell.

16 fingers are available for millimeter-wave applications. Notice that each source has its own ground. This approach is known as individual source via (ISV). This approach decreases the source inductance of the device and thereby increases the gain. There are 8 fingers in the layout shown in Figure 2.26. The gate fingers are connected by the gate bus and the drain terminals are connected by the drain bus.

The size limits for unit cells are dependent on frequency and power application. For high-frequency applications, the unit cells need to be small to minimize transit time effects. However, for power applications, one wants to make the unit cells as large as possible to save the chip area. That seems contradictory, but with smaller cells, more of them are needed, which implies more connecting lines between them. This approach ends up by taking more space and adds losses and parasitics to the circuit, compared to increasing the unit cell size, and connecting cells with a small bus line. Therefore, trade-offs are imposed when determining the optimum unit cell size. In any case, to consider an FET a lumped element, its size is restricted by the following:

1. In the horizontal direction by the propagation delay effect, related to the transit of carriers on the active device channel. It also is restricted by the losses in the gate transmission line.
2. In the vertical direction, the cell dimension is restricted to be much less than a half-wavelength of the operating frequency to minimize gain degradation due to phasing. This effect is related to the division and addiction of currents with a different phase. A general rule of thumb is to maintain the dimension much lower than a half-wavelength of the operating frequency.

Fortunately, the design of the unit cells is a responsibility of the foundries. They take all these precautions and care for the thermal dissipation constraints as well. They are also responsible for providing a device that can operate at high temperatures, maintaining the basic properties. The substrate thickness is another parameter of importance. At the lower millimeter-wave range, 75  $\mu\text{m}$  and 100  $\mu\text{m}$  are common values. At the higher end, they are in the range of 50 to 75  $\mu\text{m}$ . A thinner substrate, besides improving the propagation of signals, decreases the thermal resistance.

The MMIC designer does not have much control on the thermal resistance of the die, but must consider the conditions of use based on the dissipated power on the die. For instance, the die is attached to a base material using either epoxy or eutectic bonding. The base material must have a good thermal conductivity and low thermal expansion. The degree of liberty that is left for the designer on a given cell is the

control on the horizontal dimension within a certain minimum and maximum. The range of unit cells for GaN technology can be more or less considered as follows:

- 12.5 μm to 75 μm for operation up to 40 GHz;
- 12.5 μm to 37.5 μm for operation up to 90 GHz;
- 12.5 μm to 25 μm for operation up to 120 GHz.

The selected unit cell is submitted to S-parameters and power measurements. For millimeter-wave, the S-parameters should be measured in a broadband VNA, say, 45 MHz to 145 GHz. The total gate width (TGW) of a transistor is defined as number of gate fingers (NGF) multiplied by the (UGW):

$$TGW = NGF \times UGW \quad (2.12)$$

The device width can therefore be controlled by scaling the gate width and/or the number of fingers. The drain current is directly proportional to the TGW, which thus defines the obtainable output power of the device. However, the TGW impacts the gain as well, because it defines the transition from the unstable to the stable region of operation. Therefore, the unit cell has to be chosen carefully in order to meet the target output power with minimum gain degradation. The MMIC power amplifier designer is responsible for selecting the unit cells for his design, from the choices provided by the foundry.

## 2.6 Linear GaN HEMT Model

Currently, the foundries of a GaN process technology are responsible for deriving device models, which makes sense as they own the technological parameters. The models used to be open in the sense that customers would have access to the model parameters describing the operation of their devices. Nowadays, they are closed, and the design engineers are provided with a symbol to use in their electric circuit simulator. In general, the foundries provide linear and nonlinear models for specific unit cells. In my experience, those models are not always adequate for millimeter-wave due to the following: the reference plane may not be of interest to the designer; the calibration system may not be adequate; and the models are extracted when the technology is launched and do not reflect the present technology parameters. Fortunately, linear models are relatively easy to derive from S-parameters. For millimeter-wave modeling, the unit cell devices need to be evaluated to at least up to 100 GHz.

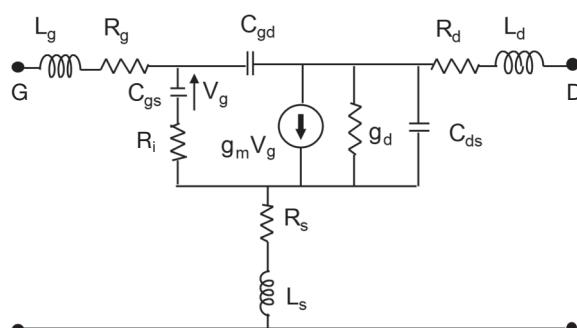
The linear model starts with preparation for S-parameter evaluations. The calibration kit is printed in the same mask in which the unit cells are built. The calibration methods most commonly used are the through-reflect-line (TRL), line-reflect-match (LRM) [21], or line-reflect-match-match (LRMM) [22]. TRL calibration is a high-frequency calibration system for S-parameter de-embedding data on wafers. However, it has a lower frequency limit, set by the use of a quarter-wavelength line, 90°, as reference. The measurement works well for a frequency

range between  $f_0/3$  up to  $3f_0$ , with  $f_0$  is at the center frequency of operation. The reflect line usually consists of a short circuit at the reference plane. LRM is quite similar to TRL, where the load match defines the system characteristic impedance. In principle, the resistor values are usually trimmed to give the exact desired value. The advantage of LRM is that of being a zero line system at the calibration point. A true zero system is not possible in real life due to the minimum distance between the probes. Also, if they are too close, there is a crosstalk between the probes that contaminates the calibration. Hence, a minimum distance between the probes of 100  $\mu\text{m}$  is observed when laying out the calibration kit. The reflect standards for input and output probes, usually a short circuit, need to be very similar. That is valid for both TRL and LRM. The LRM system is adequate for very high frequencies and works down to DC. The more sophisticated system LRMM, uses the same calibration standard as the short-open-load-through (SLOT), with algorithms that take into account associated load inductances and is more insensitive to probe placement.

The small-signal GaN model used in this book is represented in Figure 2.27. It contains 5 bias-dependent elements ( $C_{gs}$ ,  $C_{gd}$ ,  $g_m$ ,  $g_d$ , and  $R_i$ ) and 7 bias-independent elements, ( $R_g$ ,  $R_d$ ,  $R_s$ ,  $L_d$ ,  $L_s$ ,  $L_g$ , and  $C_{ds}$ ) [23]. Some authors include two extra shunt capacitors right after the  $L_g$  and  $L_s$ . They were not found to be relevant for modeling devices through the W-band.

This simplified model has been successfully employed in the design of amplifiers up to 130 GHz. The parameter extraction starts with accurate evaluation of S-parameters from a very low frequency, say, 10 MHz up to 110 GHz, or higher if it is available. The extraction starts with the measurement condition called cold FET, or a pinched-off condition. The unbiased measured S-parameters can be transformed to Z-parameters. Then the access impedances can be easily equated and manipulated to provide the access impedances,  $Z_i = R_i + j\omega L_i$ , with  $i = s, d, g$ . A detailed description of this process was reported in [24, 25].

In the next step, the device is biased at a specific bias current to determine the device intrinsic parameters. The impedance of the access series elements,  $Z_i$ , is de-embedded from the biased S-parameters to obtain the intrinsic S-parameters. This is a simple mathematical process involving matrix multiplication. The resulting parameters are converted to Y-parameters from which the intrinsic parameters  $g_m$ ,  $g_d$ ,  $C_{gs}$ ,  $C_{ds}$ , and  $C_{dg}$  are determined [26]. It is also common to determine these parameters as a function of bias for the nonlinear modeling. This is achieved by



**Figure 2.27** Small-signal GaN HEMT model [23].

biasing the device to a minimum of five bias points as indicated in Figure 2.19. For class A, #1 = quiescent bias point; #2, 3 = important for the evaluation of  $g_m$  and  $C_{in}$ ; and #3, 4, 5 for the evaluation of  $g_{ds}$  and  $C_{out}$ . For class AB, #2 = quiescent bias point; #1, 2, 3 for the evaluation of  $g_m$  and  $C_{in}$ ; and #3, 4, 5 for the evaluation of  $g_{ds}$  and  $C_{out}$ . The S-parameter measurements are made over the same frequency band as in the pinched-off case.

Once one has made the preliminary determination of the device linear model, it is not ready to be used in the designs. These raw parameters need to be inserted in the linear model and its values must be optimized in order to provide smooth S-parameters over the W-band of frequencies. The commercial software packages provide tools for modeling using their optimization routine. The task consists in entering the measured S-parameters in file A and the S-parameters from the linear model in file B, using the measured extrinsic and intrinsic parameters. Then it is up to the software to find the linear model parameters that makes the S-parameters of file A to match the S-parameters in file B. This operation is done at the bias point of interest, and if the S-parameter over bias is available, it can also derive a model function of bias.

In this book, we selected the S-parameters from a unit cell, for a GaN process, reported in [23], and slightly modified to a smaller gate length, to be used in the simulations contained in this book. The parameters for a  $4 \times 25 \mu\text{m}$  unit cell biased at 30%  $I_{D\text{MAX}}$  are in Table 2.3 referenced to a gate periphery of 1 mm. The technology is from a hypothetical 0.125- $\mu\text{m}$  gate length. Let us also assume that this technology can provide a power density of 2.4 W/mm. The power information is usually provided by the foundry or estimated from DC curves.

Two parameters of importance to define a FET technology are the  $f_T$ , transition frequency and  $f_{\text{MAX}}$ , maximum frequency of oscillation. The parameter  $f_T$  is defined by the extrapolation of current gain, when it becomes equal to 1. For an FET, it can be extracted from (2.13) [27]. It is common to neglect the terms after the first plus sign.

$$\frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m} + C_{gd}(R_s + R_d) \left[ 1 + \left( 1 + \frac{C_{gs}}{C_{gd}} \right) \frac{g_d}{g_m} \right] \quad (2.13)$$

**Table 2.3** Parameters for the Model in Figure 2.27, for a 0.125- $\mu\text{m}$  Gate Length Technology

Parameters	Value	Parameter	Value
$g_m$ (mS/mm)	460	$R_d$ (ohm/mm)	0
Tau (pS)	0.627	$R_s$ (ohm/mm)	0.21
$C_{gs}$ (fF/mm)	750	$L_s$ (pH)	3 to 5
$C_{dg}$ (fF/mm)	103	$L_g$ (pH/mm)	1.033
$C_{ds}$ (fF/mm)	190.5	$L_d$ (pH/mm)	1.217
$R_i$ (ohm/mm)	0.596	$f_T$ (GHz)	86
$R_g$ (ohm/mm)	0.17	$f_{\text{max}}$ (GHz)	220
$R_{ds}$ (ohm/mm)	37		

The parameter  $f_{\text{MAX}}$  is defined as the maximum frequency of oscillation when theoretically all generated power is fed back to the input and still sustains oscillations. It is found by extrapolating the power gain to the frequency where it is equal to the unity. It is defined by (2.14) from [28].

$$f_{\text{MAX}} = \frac{f_T}{2\sqrt{(R_i + R_s + R_g)/R_{ds} + (2\pi f_T R_g C_{dg})}} \quad (2.14)$$

## 2.7 Source and Load Modeling

To design the matching networks, one must determine an equivalent circuit for the input and output of a device. Then the device is modeled as a unilateral block, so that the input and output are disconnected from each other, as represented in Figure 2.28. The elements in the block are determined from measurements, such as DC I/V, S-parameters, or source-pull and load-pull evaluations.<sup>1</sup> Currently, one can find in the market load-pull systems operating up to 110 GHz with special setup for on-wafer load-pull. Any of these processes provides a set of source and load impedances for best power performance. The load-pull can go one step further, also providing information for best linearity. The objective is to synthesize the source and load impedance equivalent circuits. The figure also shows two matching circuit blocks.

### 2.7.1 Modeling for Gain

Before addressing gain, a quick review of stability is necessary [29]. A circuit is considered unconditionally stable if the input and output reflection coefficient of a device is less than 1 for any load or source impedance, respectively. The  $K$ -factor is defined in terms of S-parameters by inequality (2.15). If the inequality holds, then the circuit is unconditionally stable. Most engineers use the  $K$ -factor for stability, but to be rigorous, inequality (2.16) or (2.17) needs to hold simultaneously.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1 \quad (2.15)$$

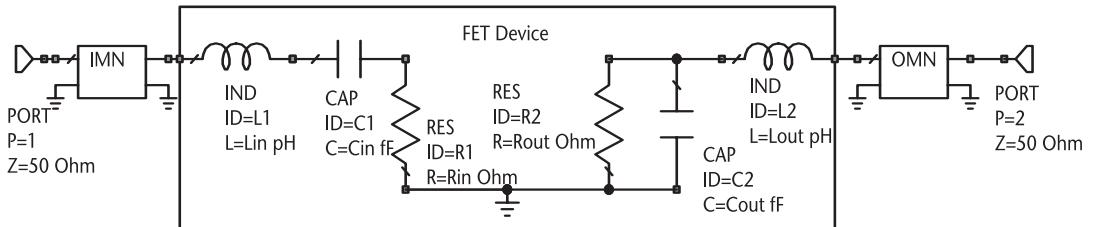
$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| < 1 \quad (2.16)$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 1 \quad (2.17)$$

The  $\mu_1$ -factor is another stability factor defined by inequality (2.18) developed for the source side, was introduced a few decades ago, and uses a single parameter to define stability. A dual equation is obtained by replacing the suffixes 1 by 2 and 2 by 1 for the drain side. Similarly, if  $\mu_2 > 1$ , the circuit is unconditionally stable.

---

1. Load-pull is detailed on page 110, Section 3.7.



**Figure 2.28** Unilateral model for the FET, adequate for the design of matching circuits.

$$\mu_1 = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \quad (2.18)$$

The *K*-factor defines what kind of gain that we can expect from an active device. If  $K > 1$ , then the maximum available gain (MAG) is defined by:

$$MAG = \frac{|S_{21}|}{|S_{12}|} (K - \sqrt{K^2 - 1}) \quad (2.19)$$

If  $K < 1$ , then the maximum stable gain (MSG) is defined by:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \quad (2.20)$$

If the device is stable, a simultaneous conjugate match is possible, and the equivalent source and load reflection coefficients are defined from (2.21) and (2.22). They can easily be converted to  $Z_L$  and  $Z_S$ . Using those values in the unilateral model, they still represent a bilateral condition.

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (2.21)$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (2.22)$$

With

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$$

$$C_1 = S_{11} - \Delta S_{22}^*$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

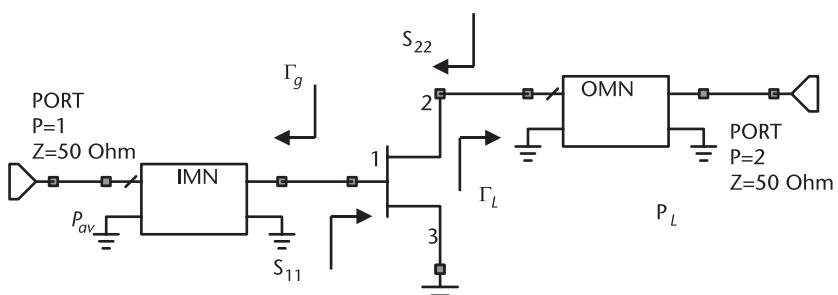
The transducer gain,  $GT$ , is defined by the ratio of power delivered to the load by the power available from the source, described by (2.23). This is the most important gain definition, where the input and output mismatches are taken into account. Their parameters description for an amplifier is shown in Figure 2.29.

This definition is based on S-parameters measured under small signal conditions. They are often referred to as small signal gain (SSG). A particular case is when the transistor is terminated with  $50\Omega$ , so that  $\Gamma_g = \Gamma_L = 0$  and the gain in  $50\Omega$  is defined as  $GT = |S_{21}|^2$ .

$$GT = \frac{|S_{21}|^2 (1 - |\Gamma_g|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_g)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_g|^2} \quad (2.23)$$

Being  $\Gamma_g = \frac{Z_g - Z_0}{Z_g + Z_0}$  and  $\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$

If  $K$  or  $\mu$  is less than 1, the conventional approach is to select a load and source for a specific gain, for instance, by using the test bench in Figure 2.30. Notice the inductors in series with the gate and drain are negative and of the same value as the model access parasitic inductors. The series and parallel capacitors are negative to tune the device capacitances over the band, instead of using inductors. After tuning, the capacitors and inductors change signs to positive. The ideal transformers provide the real part of the impedance. The source and load equivalent impedances for the device are given by the tuned elements. The matching impedances are given by the conjugated values,  $\Gamma_S^*$ ,  $\Gamma_L^*$ . This technique, proposed by Maas [30], is called negative-image modeling. The procedure is to tune the load and source, maximizing gain and matching and monitoring the stability. For high gain, we select the  $\mu$ -factor to be above 0.8, equivalent to greater than  $-1$  dB. The results for the tuning of  $4 \times 25 \mu\text{m}$  cells over 70 to 80 GHz are in Figure 2.31. A 5 pH of source inductance was inserted to guarantee stability over the band. The gain is tuned to around 9 dB at the center frequency, with  $\mu = -1.0$  dB at the lower end of the band. The worst-case return loss at the output is 12 dB at the output that is acceptable. The impedance for gain at 55, 75, and 95 GHz is in Figure 2.32, optimized each for the 10-GHz band. The results at 100 GHz are obtained with no stabilization network added, since  $\mu > 1$ . The results at 55 GHz used an inductance of 9 pH in series with the source and a  $0.5\Omega$  resistor in series with the gate.



**Figure 2.29** Schematic defining the parameters for gain calculations.

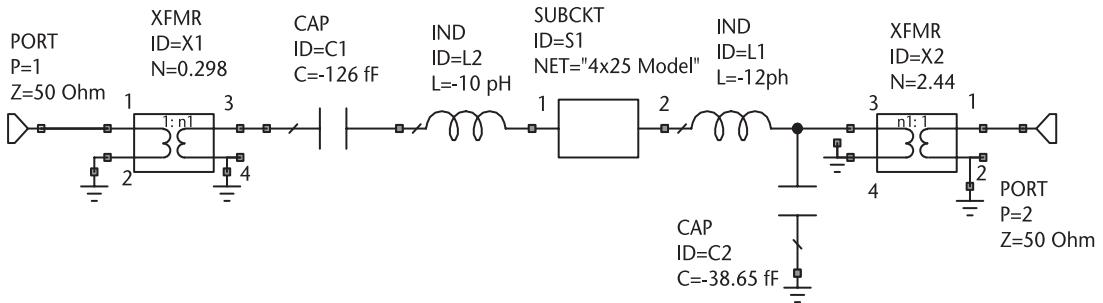


Figure 2.30 Tuning bench to find the terminations for gain, match, and stability.

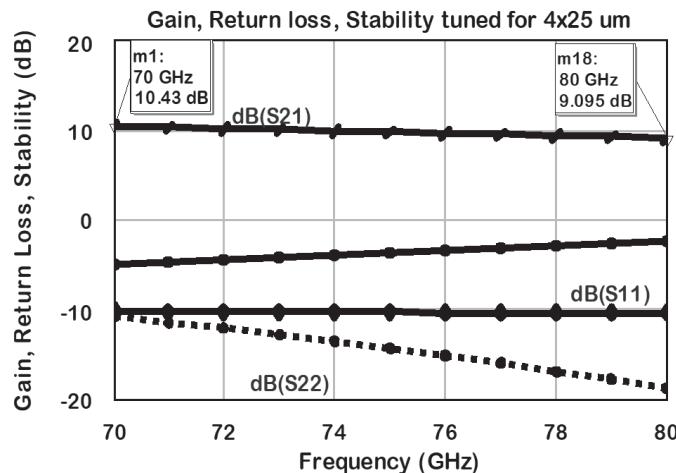


Figure 2.31 Gain tuning between 70 and 80 GHz.

### Impedance for gain, 4x25 um device

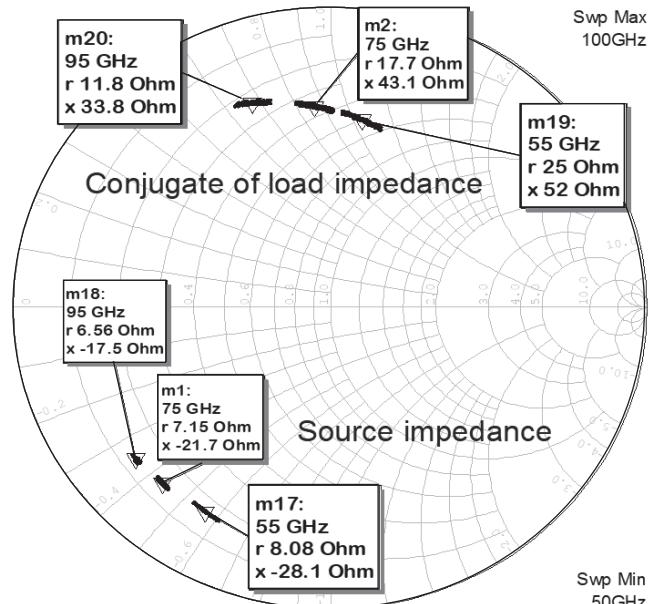


Figure 2.32 Impedance over frequency.

In the case of  $K \ll 1$ , it is difficult to match the input impedance, in particular when the associated gain is high. That is a sign of potential instability. Most commercial circuit simulators provide the maximum gain and stability factors and print the stability circles on a Smith chart, over the desired band of frequencies, directly from S-parameter files. The equations used to determine the instability areas to be drawn on a Smith chart, for the output plane, are defined by (2.24) and (2.25). The first gives the center and the second gives the radius of the instability circles. In most cases, we have  $|K| < 1$  and  $D_2 = |S_{22}|^2 - |\Delta|^2 > 0$ , resulting in unstable regions inside the circle. A similar set of equations for the source stability circle is obtained by replacing the indexes 1 by 2 and 2 by 1 in the equations [29].

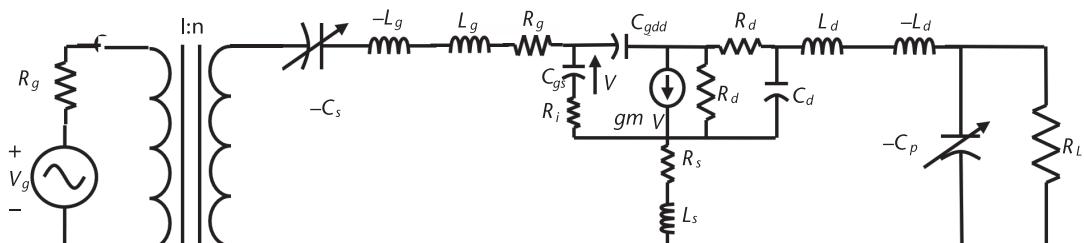
$$C_{ad} = \frac{(S_{22} - \Delta S_{11}^*)^*}{D_2} \quad (2.24)$$

$$R_{ad} = \left| \frac{S_{12} S_{21}}{D_2} \right| \quad (2.25)$$

## 2.7.2 Modeling for Power

If the amplifier is to be designed for power, we start by defining a load resistance extracted from a nonlinear model or DC measurements. To transform the resistive load,  $R_{L_{\text{opt}}}$ , into a  $Z_{L_{\text{opt}}}$ , we need to add the effect of device parasitics and of the input match. This can be obtained by building a tuning circuit, using a linear model and the DC load  $R_{\text{opt}}$ , as shown in Figure 2.33. Notice that the tuning capacitances are negative, after the Maas technique. The method consists in carrying out steps 1 to 7.

1. Add a negative inductance in series with the drain and gate with same value as the drain access inductance from the linear model. This will cancel the series inductances.
  2. Add in shunt with  $R_{L_{\text{opt}}}$ , a tunable negative capacitor to resonate with the effective drain positive capacitance.
  3. On the gate side, add a variable tunable circuit, consisting of an ideal transformer with  $1:n$ , where  $n = \text{transformation ratio}$ , and a negative series capacitance,  $C_S$ .
  4. Tune the circuit for maximum gain and input match.



**Figure 2.33** Setup to determine the optimum source and load impedance.

5. Transform the capacitances and inductances to positive.
6. The equivalent  $Z_{L_{\text{opt}}}$  is the circuit connected to the drain.
7. The equivalent  $Z_{S_{\text{opt}}}$  consists of  $L_g$ ,  $C_s$ , and the equivalent resistance from the transformer.

Let us apply this process to the determination of  $Z_{L_{\text{opt}}}$  for a unit cell measuring  $4 \times 25 \mu\text{m}$  long at 75 GHz. The DC effective load is considered to be  $150\Omega$  for this device size, obtained from its I/V DC measurements. The drain and source impedance parameters with the circuit tuned for power at different W-band frequencies are in Table 2.4.

The table includes the stabilization elements, insertion of a resistance in series with the gate, and an inductance in series with the source. The DC load line, represented in Figure 2.34 for class A operation, corresponds to the condition of the load impedance for power performance. According to the load model, it corresponds at the drain terminal, to a resistor of  $120\Omega$  in parallel with a reactance of  $-j50\Omega$ , calculated at the frequency of 75 GHz. The load impedance for gain, obtained from Figure 2.32, gives, at the drain terminal, a resistance of  $260\Omega$  in parallel with a reactance of  $-j50\Omega$ . Assuming that the load model is the same and that only the resistance changes, the resulting resistor for maximum gain is equal to  $300\Omega$ . For the sake of comparison, the load line for this resistor is represented in Figure 2.34 along with the DC load line. This factor of 2 corresponds to 3-dB lower power when the drain is matched for gain.

### 2.7.3 Source/Load as Resonant Networks

The equivalent circuit for the source and drain could be directly applied to design the matching circuits. However, we prefer to modify the terminations and make them either a series or parallel resonant circuit. This procedure is more convenient for narrowband amplifier design and evolved from previous matching techniques [31].

**Table 2.4** Source/Load Parameters Optimized for Power

Frequency	GHz	55	75	95
Source	$R_{\text{in}}$ ( $\Omega$ )	6.5	6	5.3
	$C_{\text{in}}$ (fF)	121.5	112	110
	$L_{\text{in}}$ (pH)	10.33	10.33	10.33
Load	$R_L$ ( $\Omega$ )	150	150	150
	$C_{\text{out}}$ (fF)	42.8	39	37
	$L_{\text{out}}$ (pH)	12.17	12.17	12.17
Loss	$R_g$ ( $\Omega$ )	4	0	0
Feedback	$L_s$ (pH)	10	2	0

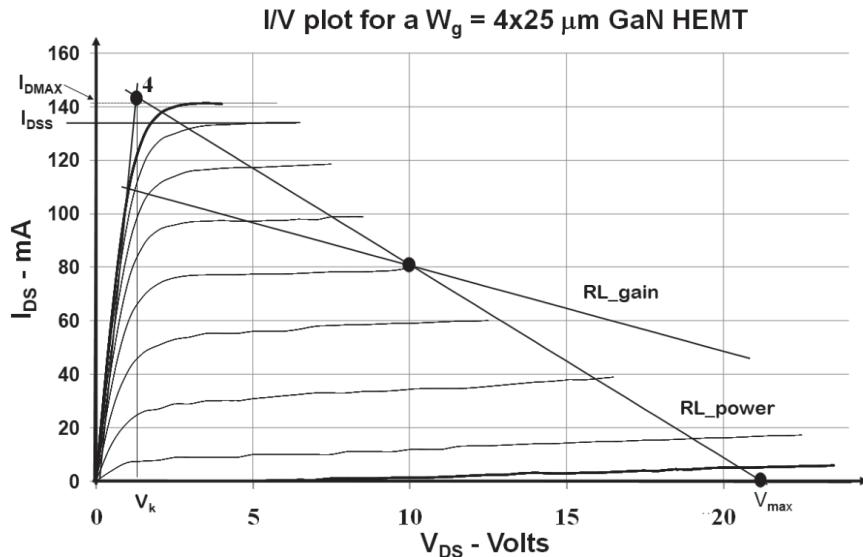


Figure 2.34 Load lines for gain and for power in class A amplifiers.

#### 2.7.4 Drain Load Impedance

Let us assume the drain impedance of the circuit in Figure 2.35. It consists of a load resistor in shunt with a capacitance and a series inductance. The impedance of this circuit in the Smith chart is represented in Figure 2.36 from 50 to 150 GHz. There are two ways of transforming this impedance into a resonant circuit. The first one is to add a series inductance,  $L$ , to move the impedance trace towards the real axis in the Smith chart.

The impedance  $Z_A$  denoted in Figure 2.37 is given by (2.26). A perfect resonance is obtained if  $L_0$  is defined by (2.27). It is not an ideal RLC series circuit for the first two terms are frequency-dependent. It can be observed that, with increasing frequency, the real and the imaginary parts of the impedance decrease by the same amount. In an ideal RLC series circuit, the resistor is frequency-independent.

This causes the trace of  $Z_A$  to shift to the left on the Smith chart above resonance and to the right below resonance, as observed in Figure 2.38. However, it does show an inductive behavior. Hence, adding a parallel capacitor with proper value will rotate the trace on the Smith chart towards a more RLC series-like

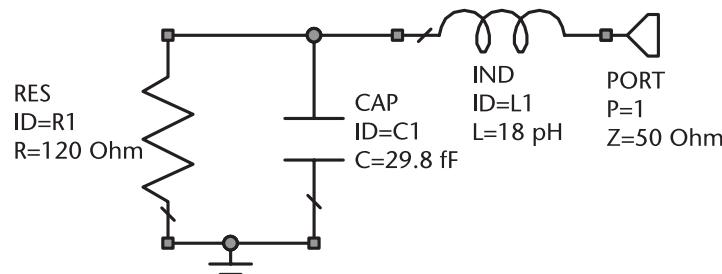
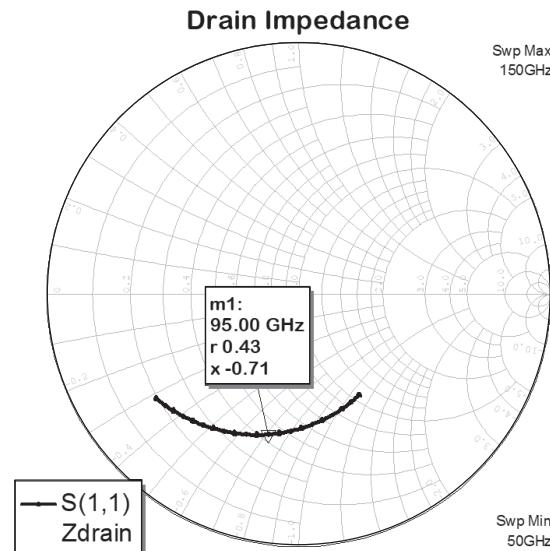
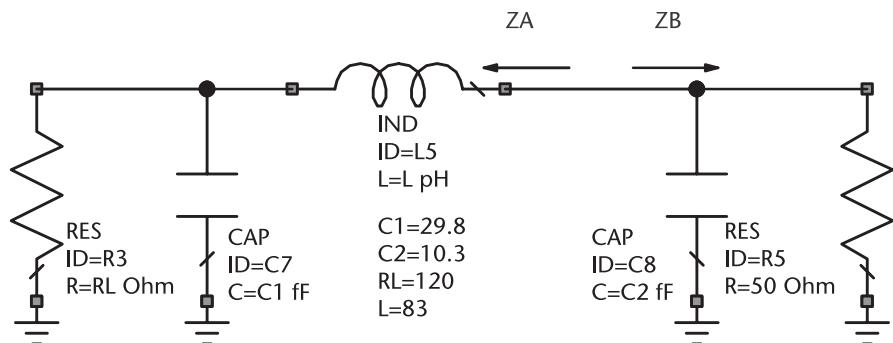


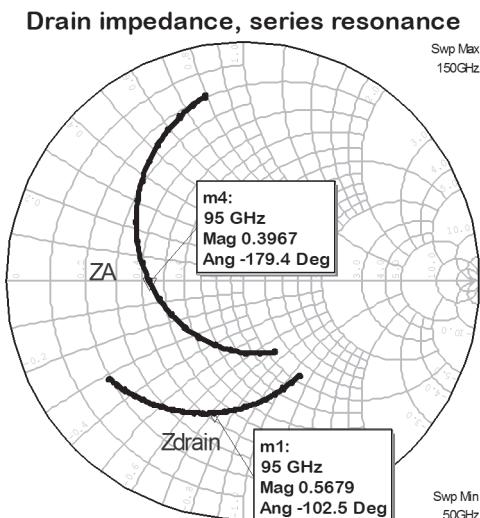
Figure 2.35 Schematic of drain impedance.



**Figure 2.36** Drain impedance in the Smith chart.



**Figure 2.37** Series resonant equivalent circuit.



**Figure 2.38** Series resonant at center frequency.

behavior (Figure 2.39). The calculation of this capacitor is complex algebra, so it is better to solve this problem directly on the Smith chart. Adding a shunt capacitor also detunes the circuit. So the series inductance value has to be slightly increased to bring the circuit back to resonance at  $\omega_0$  by the shunt capacitor. Notice that the series inductance  $L$  includes the series parasitic inductance of 18 pH.

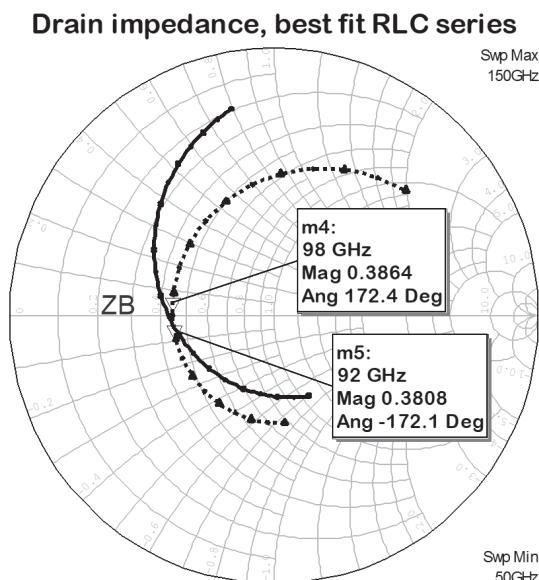
$$Z_A = \frac{R_L}{1 + (\omega R_L C_1)^2} - \frac{j\omega R_L^2 C_1}{1 + (\omega R_L C_1)^2} + jX_L \quad (2.26)$$

$$L_0 = \frac{R_L^2 C_1}{1 + (\omega_0 R_L C_1)^2} \text{ at resonance} \quad (2.27)$$

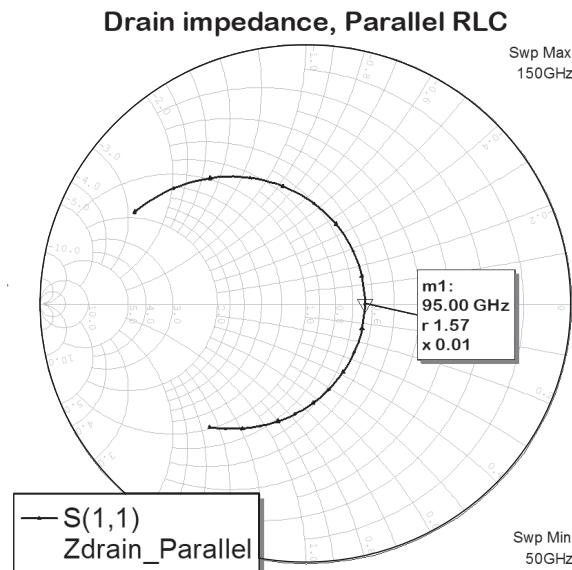
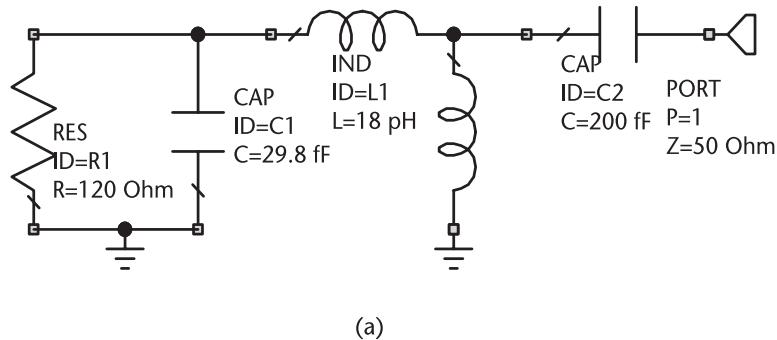
Another option is to shunt the circuit with an inductance to obtain an ideal parallel RLC circuit (Figure 2.40(a)). One can initially disregard the parasitic series inductance and apply a shunt inductance to parallel resonate the RC circuit using the Smith chart.

The series parasitic inductance is then reinserted and the shunt resonator is readjusted for a parallel RLC circuit. A series capacitance has to be added for the best fit into the ideal parallel RLC (Figure 2.40(b)).

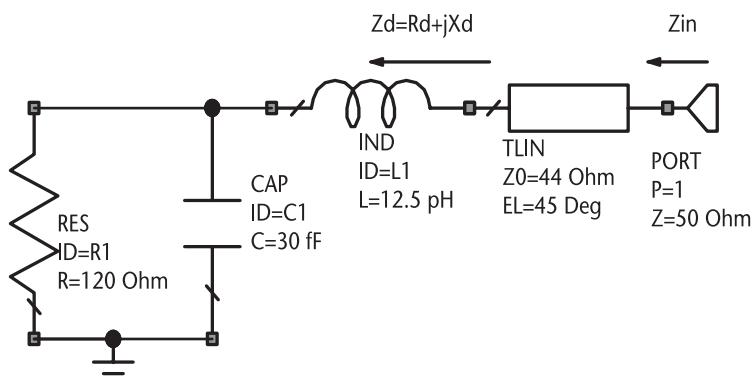
This option seems simpler to use, but it requires a ground contact close to the drain, which is not always available. Therefore, both options are needed and used in amplifier design. The parallel resonance may result in a high-value resistor, which may be difficult to match. The use of  $\lambda/8$  transmission lines to transform a complex impedance into a real value has long been used by designers and meets the requirements (Figure 2.41). The input impedance of a transmission line is given by (2.28). A  $\lambda/8$  transmission line corresponds to an electrical angle of 45°. Therefore,



**Figure 2.39** Shunt capacitor for best RLC fitting.



**Figure 2.40** Equivalent parallel RLC circuit: (a) schematic of the circuit, and (b) curve on an admittance Smith chart.



**Figure 2.41** Schematic of drain load plus  $\lambda/8$  line.

replacing the tangent by the corresponding angle value and making the imaginary part  $Z_{\text{in}}$  equal to 0, one obtains (2.29). Therefore, this line transforms a complex impedance to a real value, when the characteristic impedance of the line equals the drain impedance magnitude. The impedance in Figure 2.42 corresponds to the impedance seen by the load resistor  $R_S$ . The characteristic impedance using the values in the Smith chart is equal to  $Z_0 = 44\Omega$ .

$$Z_{\text{in}} = Z_0 \frac{R_d + j(X_d + Z_0 \tan \theta)}{Z_0 - X_d + jR_d \tan \theta} \quad (2.28)$$

$$Z_0 = \sqrt{R_d^2 + X_d^2} \quad (2.29)$$

The example in Figure 2.41 can be compared to the series drain resonance option in Figure 2.36. The trace of this impedance on the Smith chart is close to an ideal RLC series.

### 2.7.5 Gate Source Impedance

The best option is to resonate the gate capacitance, with a series inductance at the gate, as shown in Figure 2.43. This is the circuit with lower  $Q$ , showing a trace with narrow angle for  $S_{11}$ , within 50 to 100 GHz, showed in the same figure.

The alternative option is to parallel resonate the gate. This task is simplified if we first transform the RLC series into a RLC parallel circuit. The transformation can be achieved with (2.30) and (2.31). They show that the parallel equivalent  $R_p$  and  $X_p$  become a function of frequency. Therefore, the transformation series to parallel is exact only at the center frequency of operation. The impedance diverges at other

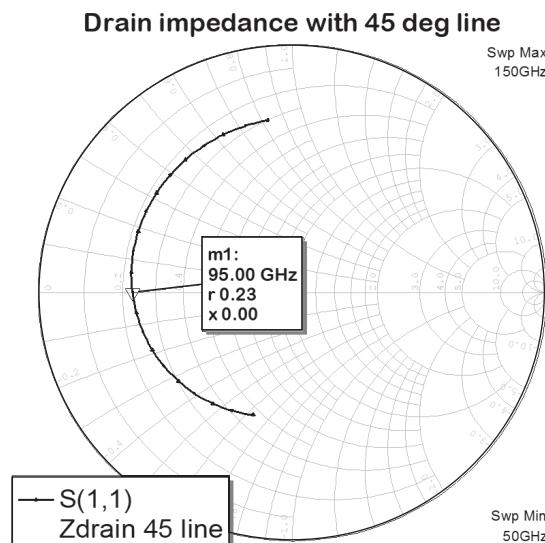


Figure 2.42 Resonance with  $\lambda/8$  line.

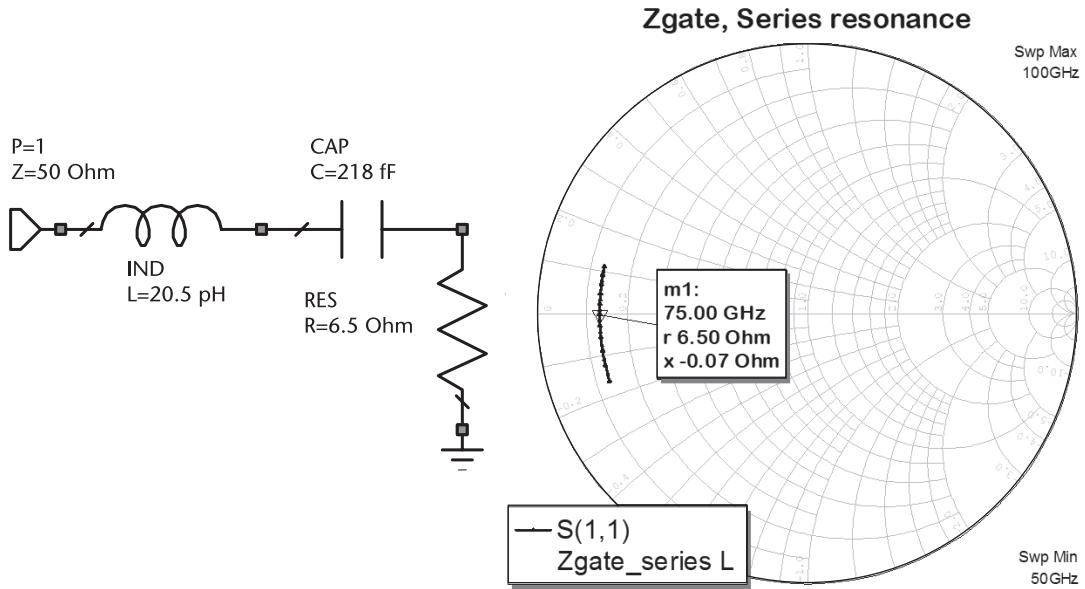
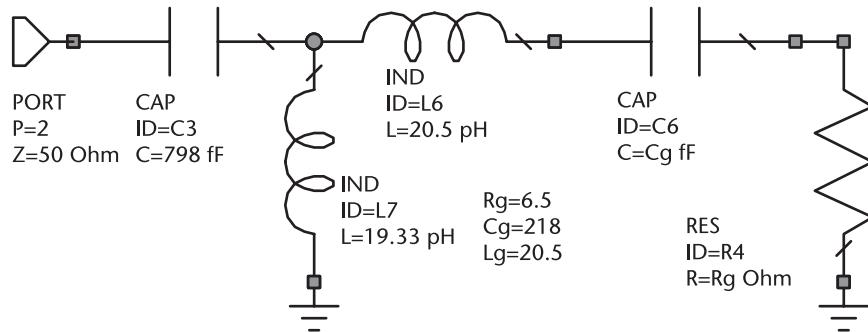
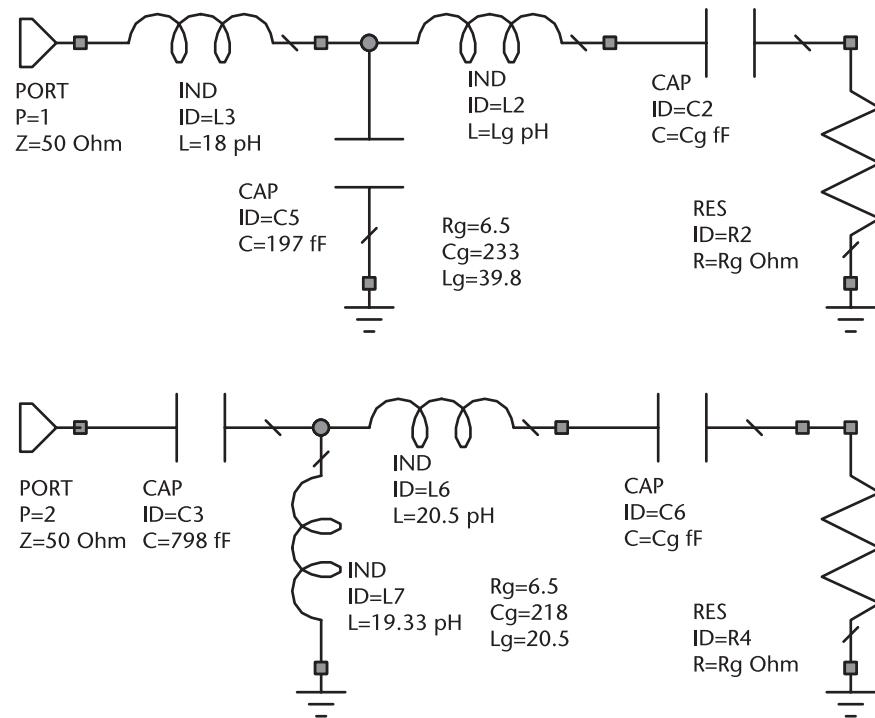


Figure 2.43 Series resonant gate impedance and representation on the Smith chart.

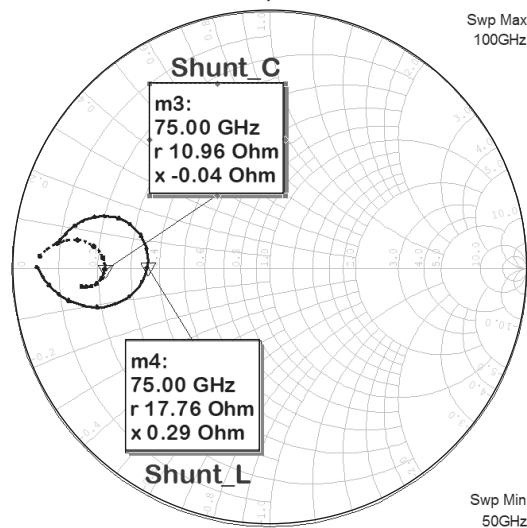
frequencies. Bandwidth is therefore affected. Alternatively, we can work directly with the RLC series in the Smith chart adding a shunt  $C$  or  $L$  to the equivalent circuit represented in Figure 2.44(a). The resonance of both circuits are observed in Figure 2.44(b), for shunt  $L$  and resonating resistance of  $9.65\Omega$ , or for shunt  $C$  and resonating resistance of  $17.3\Omega$ .

$$R_p = R_s \left[ 1 + \left( \frac{X_s}{R_s} \right)^2 \right] \quad (2.30)$$

$$X_p = \frac{R_s R_p}{X_s} \quad (2.31)$$



(a)

**Gate resonance, shunt L/shunt C**

(b)

**Figure 2.44** Parallel resonance of gate impedance.

## 2.8 Unit Cell Gain and Stability

The curves shown in Figure 2.45 represent the MSG, MAG, the  $K$ -stability factor, and the parameter  $B_1$ , for a  $4 \times 25 \mu\text{m}$  device. The linear model parameters used for gain and stability calculations are in Table 2.3. Notice the parameter  $f_k$  in Figure 2.45. It is defined as the frequency where the device MSG turns into MAG and is dependent on the total gate periphery of the device. For this particular device,  $f_k = 83 \text{ GHz}$ . The parameters  $K$ -factor and  $B_1$  are greater than 1 above  $f_k$ .

In order to compare the stability factors, let us verify the  $\mu$ -factors in the plot represented in Figure 2.46. Observe that  $\mu_1$  and  $\mu_2$  are greater than 1 above 83 GHz, the same frequency predicted by the  $K$ -factor. In the stable frequency range, one can use any stability factor. In the unstable range, one can see that  $\mu_1$ -factor is close to the  $K$ -factor, while the  $\mu_2$ -factor is closer to  $B_1$ . The approach used in this book is to stabilize the circuit based on  $\mu_1$ -factor.

### 2.8.1 Stabilization of Unit Cells

Obviously, a high gain and unconditional stable device are the best design solution if the gain is reasonable. When the design is carried out at frequencies above  $f_T$ , the designer should carefully consider shortening the device periphery, or decreasing the number of fingers, to recover gain. If that is the limit, then the designer will have to accept low gain per stage and add amplification stages as needed. Between  $f_k$  and  $f_T$ , the amplifiers can be designed for MAG, if the gain is at least 10 dB. However, for designs below  $f_k$ , the best procedure is to stabilize the device just under 0 dB and design the matching networks for the target objectives. The reasoning behind this strategy is that, at these high frequencies, the losses can be near 1 dB for the output stage and higher for the interstage. That alone would already bring the circuit into stability. In addition, stability is assured if the matching circuits are designed to impedances at the gate and drain that are far from instability areas. The

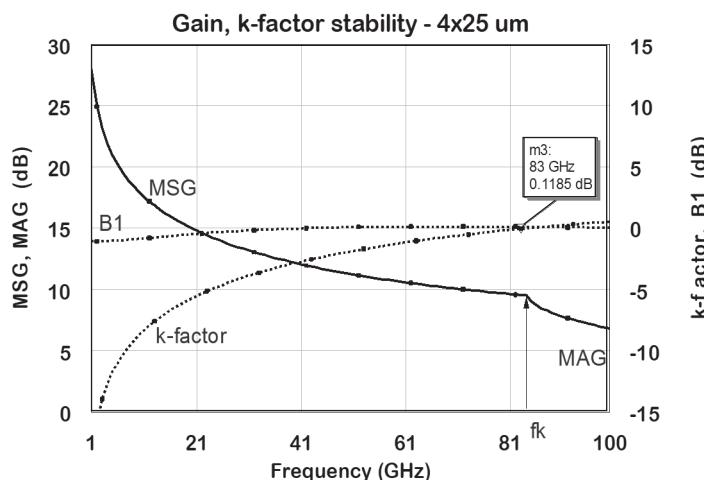


Figure 2.45 Gain and  $K$ -factor versus frequency.

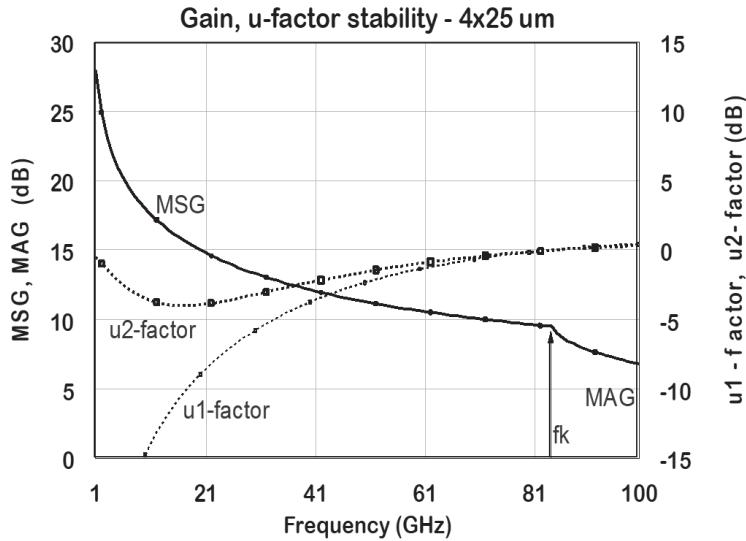


Figure 2.46 Gain and  $\mu$ -factor versus frequency.

stability can be controlled during the optimization process, making  $\mu$  or  $K$ -factors to be part of the design target. At the end of the design, we verify overall stability again, and losses may be added in the circuit if necessary. A conditional gain of 10 dB per stage is a good design compromise for GaN technology at high millimeter-wave frequencies.

By properly selecting the size of unit cells according to the desired operating frequency, it is possible in most cases to obtain a unit cell with sufficient in-band stability. For instance, Figure 2.47 compares gain for two different device sizes. If the design objective needs a unit cell with a drain periphery of  $4 \times 100 \mu\text{m}$  for operation above  $f_{k1}$ , say, between 70 and 80 GHz, a gain of 7 dB is expected. However, if we

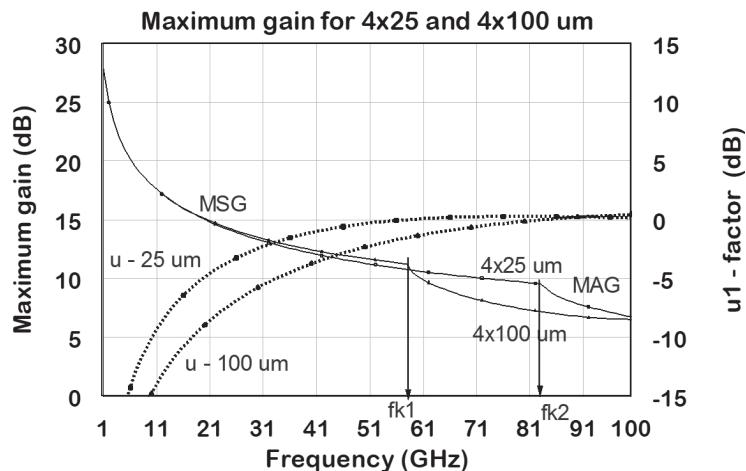


Figure 2.47 Gain and stability comparing two devices with dimensions  $4 \times 25 \mu\text{m}$  and  $4 \times 100 \mu\text{m}$ .

combine four unit cells with a drain periphery of  $4 \times 25 \mu\text{m}$ , match its impedance, and then combine the power, we will obtain nearly 10 dB of gain. When designing amplifiers below  $f_{k1}$ , say, between 40 and 60 GHz, the design with  $4 \times (4 \times 25) \mu\text{m}$  should proceed according to the procedure in Section 2.7. At lower frequencies, devices from a lower-cost technology should be used. However, in case there is a need to use a millimeter-wave device, one option is to add a resistor in series with the gate and a capacitor in shunt from gate to ground. The addition of these components improve circuit stabilization and linearize the amplifier gain. They may affect the gain but not the power capability of the device.

In conclusion, when the active device shows a  $K$  or  $\mu$ -factor in the vicinity of 0 dB and above within the frequency band of interest, then the amplifier design should proceed. If the stability factor shows a high negative value within the design band, then the device needs to be stabilized before starting the design using any of the following processes.

### 2.8.2 Source Inductor

The insertion of an inductor in series with the source is the simplest stabilization process. Since it affects gain, they need to be properly traded off. The series inductance can be replaced with a short transmission line to ground, as shown in Figure 2.48(a). This performs well for a 2-finger cell. For 4 fingers, one has to introduce the feedback on a 2-finger cell and parallel them.

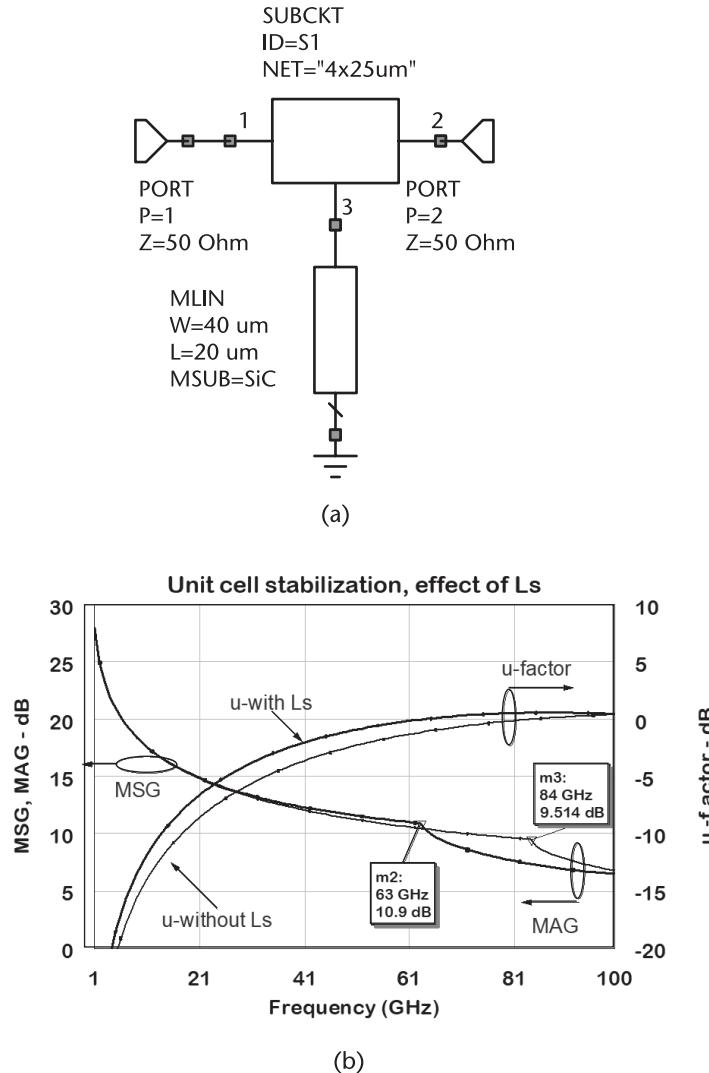
Figure 2.48(b) shows the effect of series feedback on gain and stability. It is not practical to employ this technique for larger number of fingers, due to the increase in the chip size. It is adequate for amplifiers in the range from 50 to 80 GHz.

### 2.8.3 Source Inductor and Gate Resistor

Let us say the design is for a frequency band between 35 and 40 GHz, where  $\mu$ -factor  $<-3$  dB, as depicted in Figure 2.49(a). Let us also add a  $8.5\Omega$  resistor in series with the gate and an inductance of 10 pH in series with the source, in the manner displayed in Figure 2.49(b). The results are detailed in Figure 2.49(a), showing the new  $\mu'$  factor is greater than 0 dB within the band. The minimum MAG' is in the order of 10 dB. Thus, a 10-dB gain amplifier can be designed with this stability.

Now let us take the case of a design between 70 and 80 GHz where stability factors are in the limit of stable to unstable. To improve stability by 1 dB, let us add a  $3\Omega$  resistor in series with the gate and a 5-pH inductance in series with the source. The results in Figure 2.50 show a 1-dB increase in stability with a drop of 3 dB in the gain.

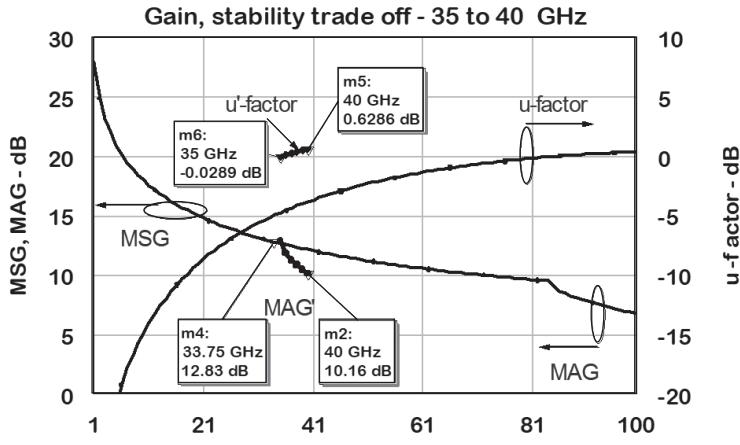
This gain reduction is unacceptable, for more amplifier stages will have to be added to recover the gain. Based on the recommendations, no stabilization is used and the amplifier is designed for a gain in the vicinity of 10 dB.



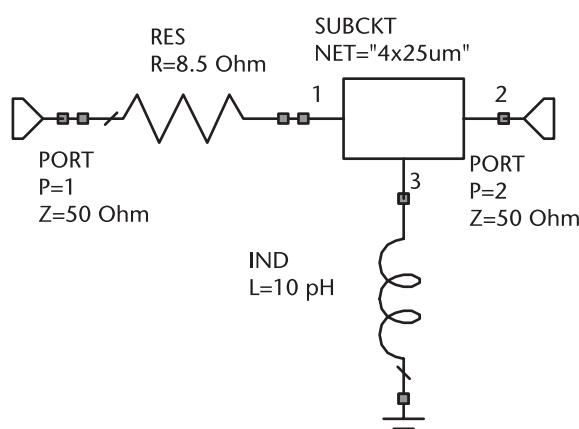
**Figure 2.48** Effect of source inductor on stability and MSG/MAG for a  $4 \times 25 \mu\text{m}$  unit cell:  
(a) schematic for series feedback, and (b) simulation results for series feedback.

#### 2.8.4 Resistor with Shunt Inductor

A resistor in series with a transmission line, connected in shunt to the gate, improves stability over a large band of frequencies. This arrangement is depicted in Figure 2.51(a) and can be part of the bias line. According to Figure 2.51(b), amplifiers can be designed up to 70 GHz employing this type of unit cell stabilization. Observe that the stability over 1 to 100 GHz is nearly stable. This option gives a good compromise for the design of a large band amplifier.

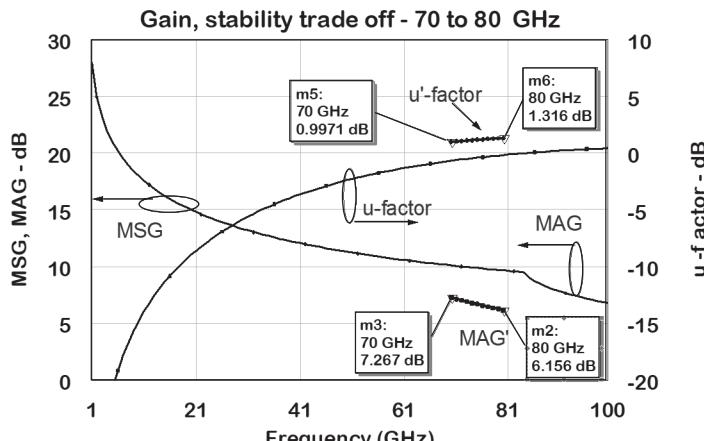


(a)

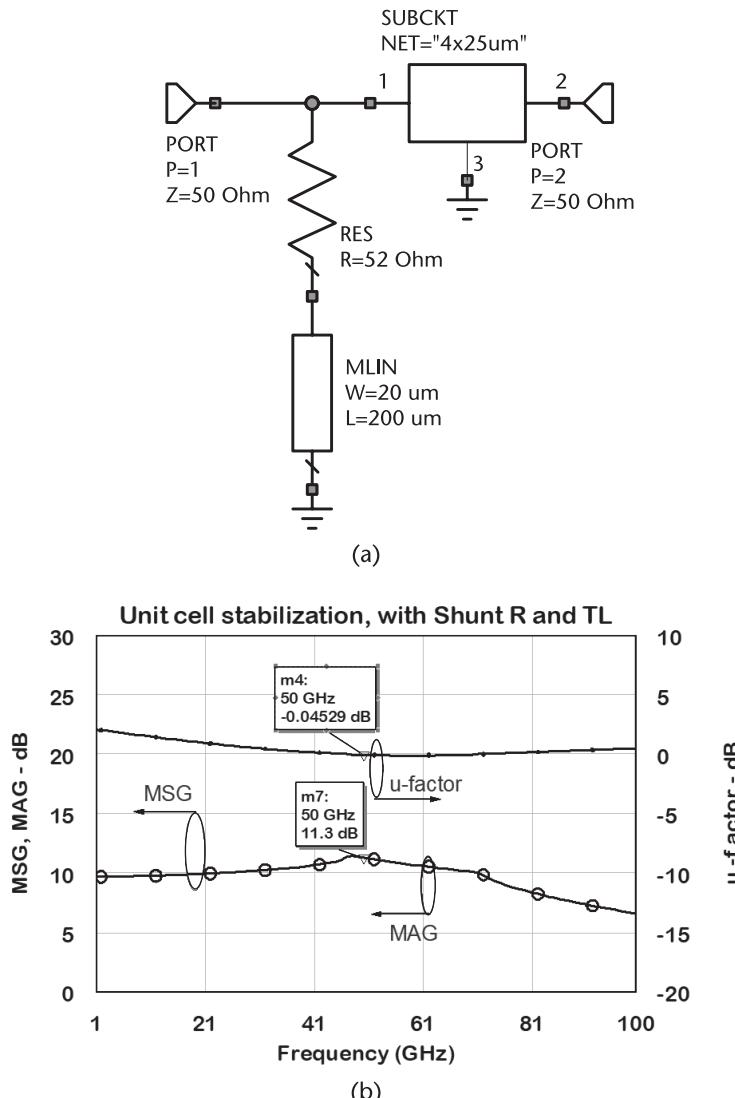


(b)

**Figure 2.49** Gain and  $\mu$ -factor within 35 to 40 GHz with a  $4 \times 25\text{-}\mu\text{m}$  device: (a) simulation results\_series feedback with gate resistor, and (b) series feedback with resistor.

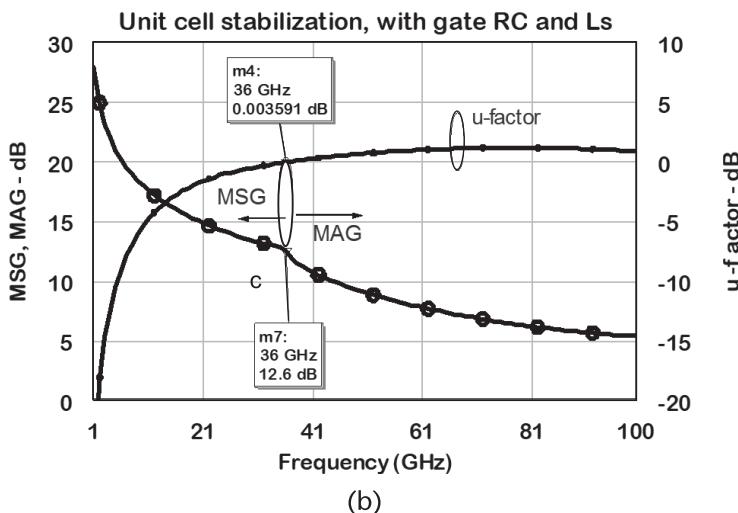
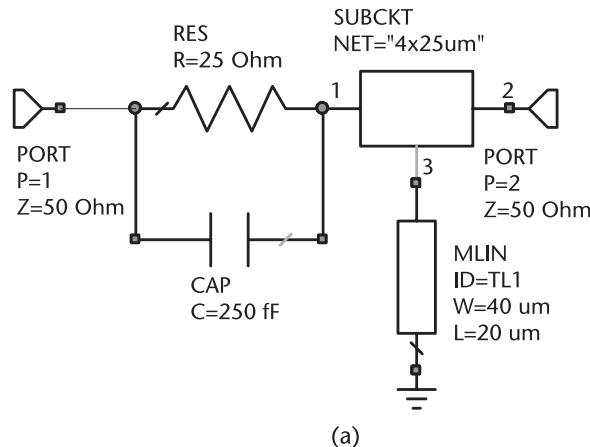


**Figure 2.50** Gain and the  $\mu$ -factor within 70 to 80 GHz.



**Figure 2.51** Use of a lossy shunt stub at the gate as stabilizing elements: (a) schematic for shunt lossy stub, and (b) simulation results for shunt lossy stub.

The addition of a parallel RC network in the gate path combined with source inductance is used by some designers (Figure 2.52(a)). The resistance will introduce losses as a function of frequency. Notice in Figure 2.52(b) that this approach is useful with the parameters from 30 to 50 GHz. One problem of this circuit is the difficulty to handle the parasitic related with the connection between the resistor and the capacitor.

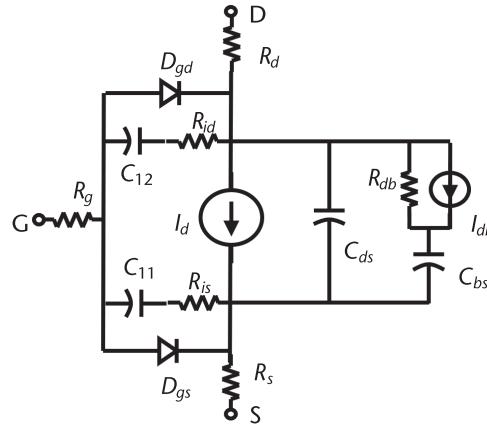


**Figure 2.52** Source inductance and parallel RC gate stabilizing network: (a) gate and source stabilization, and (b) simulation results for the gate and source stabilization.

## 2.9 Nonlinear GaN HEMT Model

The construction of nonlinear GaN models requires high investments in equipment and time involved in getting the final model topology and its parameter values. It is an expensive and lengthy process. Therefore, design houses prefer to subcontract this type of work to specialized companies, instead of developing their own nonlinear models. Besides, foundries normally provide models from their MMIC technology to the design engineers.

The most popular nonlinear models available in commercial simulators are the EEHEMT by Agilent Keysight [32] and the Chalmers or Angelov-Zirath model [33]. The standard Chalmers model uses a hyperbolic tangent to represent  $I_{DS}(V_{GS})$ , resulting in a bell-shaped transconductance with a pronounced symmetry around



**Figure 2.53** EEHEMT equivalent circuit model.

the peak value. This is not so simple to adjust for GaN HEMTs. The EEHEMT model, shown in Figure 2.53, is quite easy to adjust for a symmetric or asymmetric transconductance profile. That is probably a reason why the industry started using this model for GaN HEMTs.

Most recent publications from companies working with GaN HEMTs are still using the EEHEMT model [34]. A third model, the Dynafet by Keysight [35], was introduced in 2014 as the most advanced model for global applications. The EEHEMT model is based on the quasi-static assumption, where all model elements, linear and nonlinear, change instantaneously with changes in their control voltage. EEHEMT is capable of nonsymmetrically shaping the  $G_m(V_{GS})$  characteristic, and the DC and AC drain currents are independent of each other. That particularity facilitates the optimization steps of the DC and AC circuits.

The intrinsic equivalent circuit for the model comprises: drain current generator, gate Schottky diodes, and charge model for the gate reactance elements. The definition of these parameters is detailed in Table 2.5. The dispersion effects at the drain are also included in the figure, but are not considered for GaN HEMT modeling. The general drain current function is expressed by (2.32). The details of the equations used to define the general drain current are found in the IC-cap reference [32].

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds}^{AC}(V_{gs}, V_{ds}) + I_{ds}^{DC}(V_{gs}, V_{ds}) \quad (2.32)$$

Commercial equipment is available in the market to automatically extract the device parameters. The procedure used in this book is a short-cut process adequate for engineers in need of a model for designing power amplifiers who do not have access to that infrastructure. The starting point is the determination of the DC parameters from the DC I/V plot or table of values obtained under pulsed conditions to avoid thermal issues. One plot that should be added is the I/V from the gate side. The AC parameters are extracted from the S-parameters, partially available from the linear model. In particular, the dependence of capacitance, transconductance, and output conductance as a function of bias is a key to determine the AC parameters. One particularity of this model is that the original model uses an electrical

**Table 2.5** DC Parameters for a Unit Cell Size  $4 \times 25 \mu\text{m}$ 

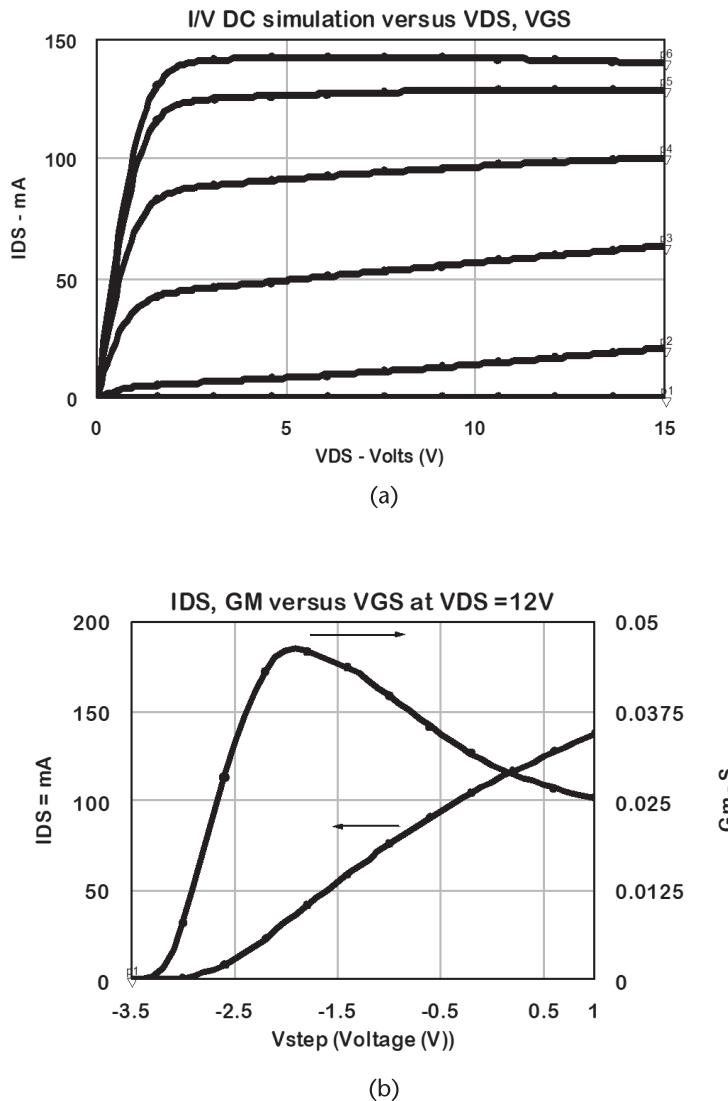
Parameter	Value	Description	Parameter	Value	Description
$V_{to}$ , V	-3.15	Threshold voltage	$R_d$ , Ohm	0.1	Contact resistance, drain
Gamma	0.004	Threshold constant to set $V_{gs}$ dependence on $V_{ds}$	$R_s$ , Ohm	3	Contact resistance, drain
$V_{go}$ , V	-1.85	Gate voltage where $g_m$ is maximum	$R_g$ , Ohm	4	Contact resistance, drain
$V_{delt}$ , V	0	Linearization of $g_m$	$R_{is}$ , Ohm	0.5	Channel resistance source end
$V_{ch}$ , V	1	Gate voltage where gamma no longer affects I/V	$R_{id}$ , Ohm	0.5	Channel resistance, drain end
$G_{mmax}$ , mS	50	Peak transconductance	$K_{bk}$	0.03	Breakdown current coefficient
$V_{dso}$ , V	2	Drain voltage where drain current is dependent on $V_{gs}$	$V_{br}$ , V	45	Gate drain breakdown voltage
$V_{sat}$ , V	2.25	Drain voltage where current saturates at the bias point	$N_{br}$	2	Breakdown current exponent
Kapa	0.022	Output conductance at $V_{gs} = V_{ch}$	$V_{co}$ , V	-1.6	Voltage for $g_m$ compression at $V_{ds} = V_{dso}$
$P_{eff}$ , mW	8000	Channel to backside DC power. Set I/V temperature	$V_{ba}$ , V	0.5	Voltage $g_m$ compression at tail off
$I_{dsoc}$ , mA	193	Open channel drain source current	$V_{bc}$ , V	1	Transition $g_m$ roll off to tail off
$I_s$ , A	$2.8 \times 10^{-12}$	Gate junction reverse saturation current	Deltgm	0.01	Slope of $g_m$ compression characteristic
N	2	Diode ideality factor	Alpha, V	0.15	Transition voltage for $g_m$ saturation to compression
$V_{dsm}$ , V	100	Voltage where $I_{db} = 0$	$G_{dbm}$ , mS	0	$I_{db}$ Conductance, not used

charge at the gate, instead of capacitors. However, the commercial circuit simulators require capacitors as the input information.

The model in this book started with the determination of the DC parameters, defined in Table 2.5. They were extracted from the I/V curves in Figure 2.19 and from the  $G_m(V_{GS})$  curve in Figure 2.20. The access resistances for the source and gate used the values from the linear model in Table 2.3. The drain access resistance, found to be 0 in the linear model, required a different value in the nonlinear model. The DC parameters were adjusted for best fitting, and the optimized values are included in the table. We did not have access to the I/V from the gate side, so the parameters from conventional Schottky diodes were used. In this particular model, they came from a template model for a GaAs pHEMT available from Microwave Office.

The DC I/V set of curves generated from the EEHEMT model is in Figure 2.54(a). In Figure 2.54(b), the drain current and DC transconductance at the drain bias of 5.0V is shown. The maximum drain current is about 146 mA and the maximum DC transconductance is equal to 48 mS.

From the charge function of voltage, the gate-source capacitance,  $C_{11}$ , is defined by the charge derivative with respect to gate voltage, (2.33). The gate-drain capacitance is determined by the charge derivative with respect to drain voltage,  $C_{12}$  in (2.34). The resistors  $R_{id}$  and  $R_{is}$  correspond to the charge delay between the depletion region and the channel. A complete procedure to determine the EEHEMT parameters are found in the literature [32, 36–38]. Improvements on the EEHEMT model,



**Figure 2.54** DC curves generated by EEHEMT model for a hypothetical 0.125- $\mu\text{m}$  GaN HEMT: (a) I/V plots for  $V_{DS}$  between 0 and 12V, and (b)  $I_{DS}$  and  $G_m$  function of  $V_{GS}$ .

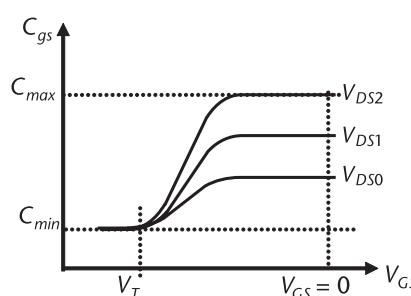
specifically for GaN modeling, were reported in [39, 40]. The gate capacitance  $C_{gs}$  is a function of gate and drain voltage and follows an approximate S shape curve shown in Figure 2.55. Drain voltage increases from  $V_{DS0}$  near zero to  $V_{DS2}$  under drain current saturation. The parameter  $C_{11th}$  corresponds to the minimum value near to  $V_{to}$  value, at  $V_{DS} = V_{DS0}$ , and  $C_{110}$  corresponds to maximum value at high gate voltage.

$$C_{11} = \frac{im(Y_{11})}{\omega} = \frac{\delta q_g}{\delta V_{gs}}, \text{ gate source capacitance} \quad (2.33)$$

$$C_{12} = \frac{im(Y_{12})}{\omega} = \frac{\delta q_g}{\delta V_{ds}}, \text{ gate drain capacitance} \quad (2.34)$$

The inflection point was assumed to be between the pinch-off voltage and near the peak of  $gm$ . The device was modeled at the bias point defined by  $V_{GS} = -1.75V$ , and  $V_{DS} = 12V$ . Thus, the capacitance is above the inflection point, and  $C_{max} = C_{gs}$  from linear model. The gate drain capacitance,  $C_{12}$ , defines two capacitances, a transcapacitance,  $C_{12sat}$ , and the conventional drain gate capacitance,  $C_{gdsat}$ . The former is determined by curve-fitting and the latter borrows the value from the linear model.

The initial AC parameters are inserted in the EEHEMT model, and it is submitted to optimization, by comparing its S-parameters to the linear model S-parameters, over a frequency range from 1 to 100 GHz. The DC parameters are maintained fixed. If the S-parameter function of bias is available, this process is to be carried out over frequency and also over bias. That would increase the accuracy of the model. A second optimization step is carried out by comparing the model power prediction with the power measured from a real test circuit. In the case of the model in this context, the power results are compared to a prematched single-stage device at the frequency of 87 GHz, reported in the literature [23]. The power adjustments are made on the DC and AC parameters like Gamma,  $G_{max}$ , and Kapa AC. A third or a second alternative optimization step would be to use the results of load-pull to fine-tune the power performance parameters.



**Figure 2.55** Capacitance from pinch to saturation in the EEHEMT model.

**Table 2.6** AC Parameters for a Unit Cell Size of  $4 \times 25 \mu\text{m}$ 

$V_{tso}$ , V	-100	Not used	$\text{Kapa}_{\text{AC}}$	74.8	AC output conductance
$V_{\text{tsoAC}}$ , V	-99	Not used	$P_{\text{effAC}}$ , mW	8,000	Channel to backsde DC power
$R_{\text{db}}$ , Ohm	10,000	Not used	$C_{11o}$ , fF	138	Max capacitance for $V_{\text{ds}} = V_{\text{dso}}$ and $V_{\text{dso}} > \text{Delt}_{\text{ds}}$
$C_{\text{bs}}$ , fF	0.2	Capacitance trapping source, not used	$C_{11\text{th}}$ , fF	58	Min capacitance for $V_{\text{ds}} = V_{\text{dso}}$
Tau, pS	0.63	Transit tme, delay	$V_{\text{infl}}$ , V	-1.9	Inflection point in $C_{11}-V_{\text{gs}}$
$C_{\text{dso}}$ , fF	20	Drain source capacitance	$\text{Delt}_{\text{gs}}$ , V	1.7	Transiton voltage from $C_{11\text{th}}-C_{11o}$
$V_{\text{toAC}}$ , V	-3.15	AC threshold voltage	$\text{Delt}_{\text{ds}}$ , V	3	Transition regon from linear to saturation
$\text{Gamma}_{\text{AC}}$	0.004	AC threshold constant	Lambda	0.01	$C_{11}-V_{\text{ds}}$ characteristic
$G_{\text{MmaxAC}}$ , mS	45	AC peak $g_m$	$C_{12\text{sat}}$ , fF	12	Transcapacitance for $V_{\text{gs}} = V_{\text{infl}}$ and $V_{\text{ds}} > \text{Delt}_{\text{ds}}$
$\text{Delt}_{\text{gmAC}}$	0.01	Slope of AC $g_m$ compression characteristic	$C_{\text{dgsat}}$ , fF	12	Gate drain capacitance for $V_{\text{ds}} > \text{Delt}_{\text{ds}}$

## 2.10 EEHEMT Model Validation

Linear and nonlinear simulations were made to validate the model compared to a previous publication [23].

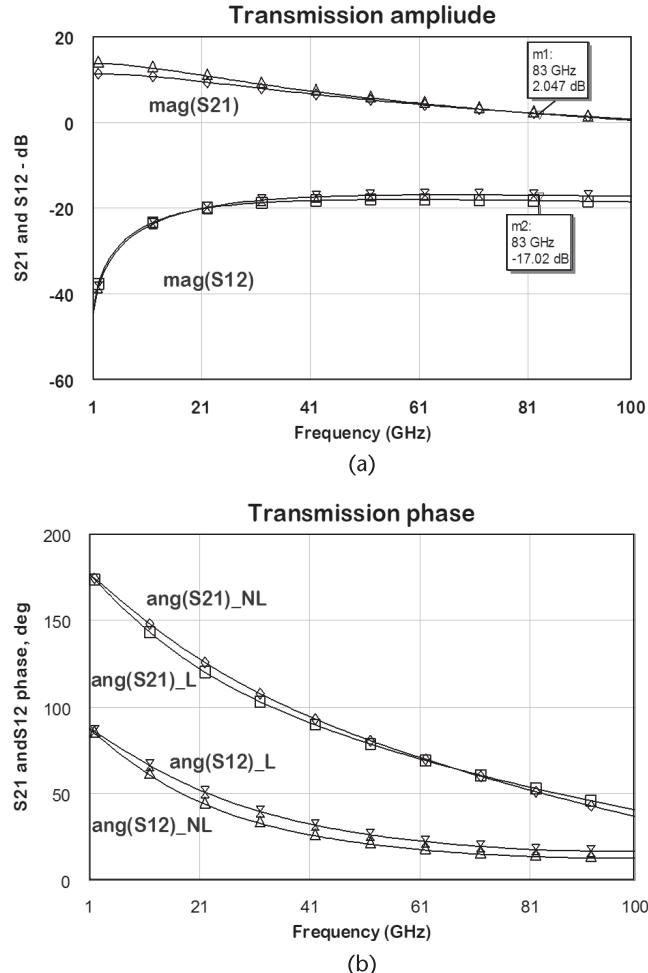
### 2.10.1 Linear Performance

The comparisons of S-parameters generated from both linear and nonlinear models are shown in the next two figures. Figure 2.56 compares the transmission coefficients for a specific bias condition,  $V_{DS} = 12\text{V}$  and  $V_{GS} = -1.75\text{V}$ ,  $I_{DS} = 38\text{ mA}$ . The device size is  $4 \times 25 \mu\text{m}$ . Both the linear and nonlinear models show a close amplitude match within less than a 1-dB difference.

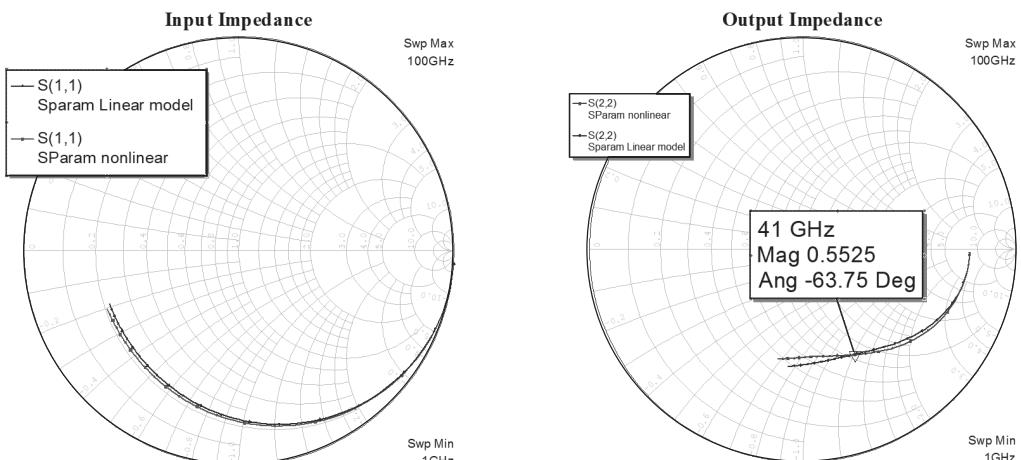
The phase match, for the same set of parameters, shows a close match at the band extremes, with a difference of less than  $5^\circ$  over the band. The input impedance parameters in Figure 2.57 are close within a few percent at the high end of the band. The output impedance shows a good match over the band.

### 2.10.2 Prematched Linear Performance

A prematched circuit to verify linear performance for the unit cell  $4 \times 25 \mu\text{m}$  was reproduced from [23], and adjusted to fit the linear parameters. The circuit elements are in Figure 2.58. The source/load circuits were converted to EM circuit blocks. The circuit S-parameters was then evaluated with the linear model from Table 2.3. The small signal curves in Figure 2.59 are close to the published results. The simulated peak gain of 8.1 dB for this circuit occurs at the frequency of 87 GHz. It is close to the value of 8.4 dB reported in the publication.



**Figure 2.56** Transmission coefficients  $S_{21}$ ,  $S_{12}$  represented in amplitude and phase, respectively, by the left and right sets of curves: (a) I/V plots for VDS between 0 and 12V, and (b) IDS and Gm function of VGS.



**Figure 2.57** Input and output reflection coefficient comparisons, represented by the set of curves on the left and right, respectively.

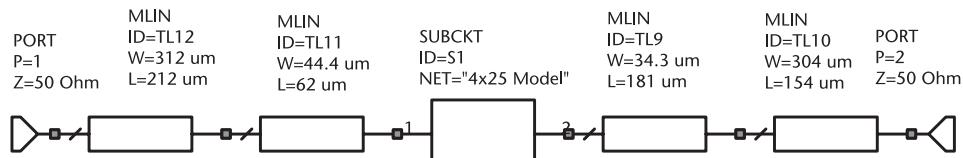


Figure 2.58 Block diagram of prematching circuit.

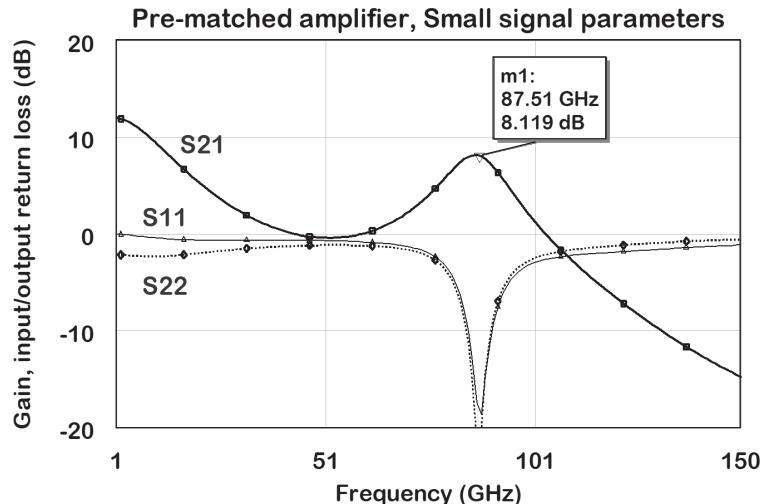


Figure 2.59 Prematching small-signal simulations.

### 2.10.3 Prematched Nonlinear Performance

A typical representation of an amplifier excited by a CW signal is in the circuit schematic contained in Figure 2.60. The nonlinear device is inserted between two bias T-networks to separate the DC circuit from the RF circuit. Typical results generated by this circuit are in Figure 2.61. The linear power and linear amplification are considered from the noise level up to the point where the gain compresses by 1 dB. The  $P_{1\text{dB}}$  power is equal to 23.7 dBm. The PAE peaks at a value of 27% at an

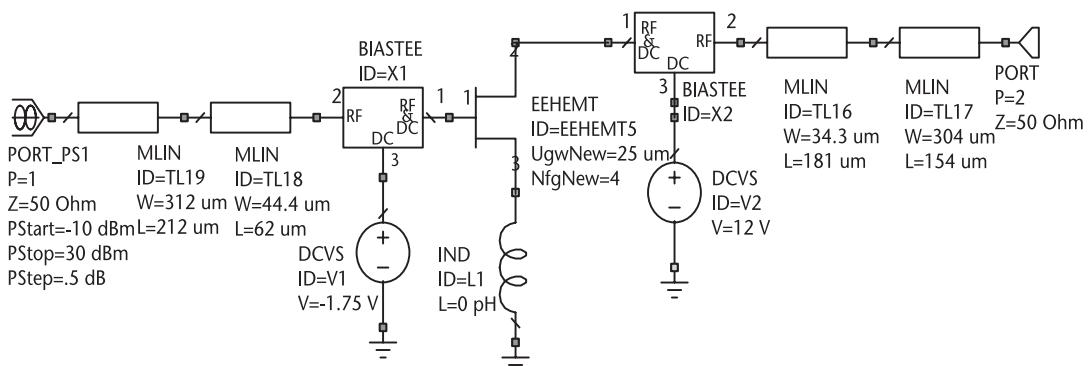


Figure 2.60 Representation of the prematch amplifier test bench.

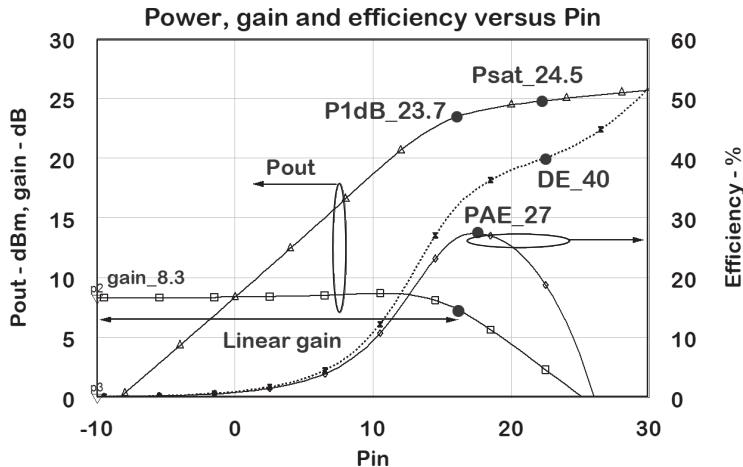


Figure 2.61 Typical amplifier power performance curves at 87 GHz.

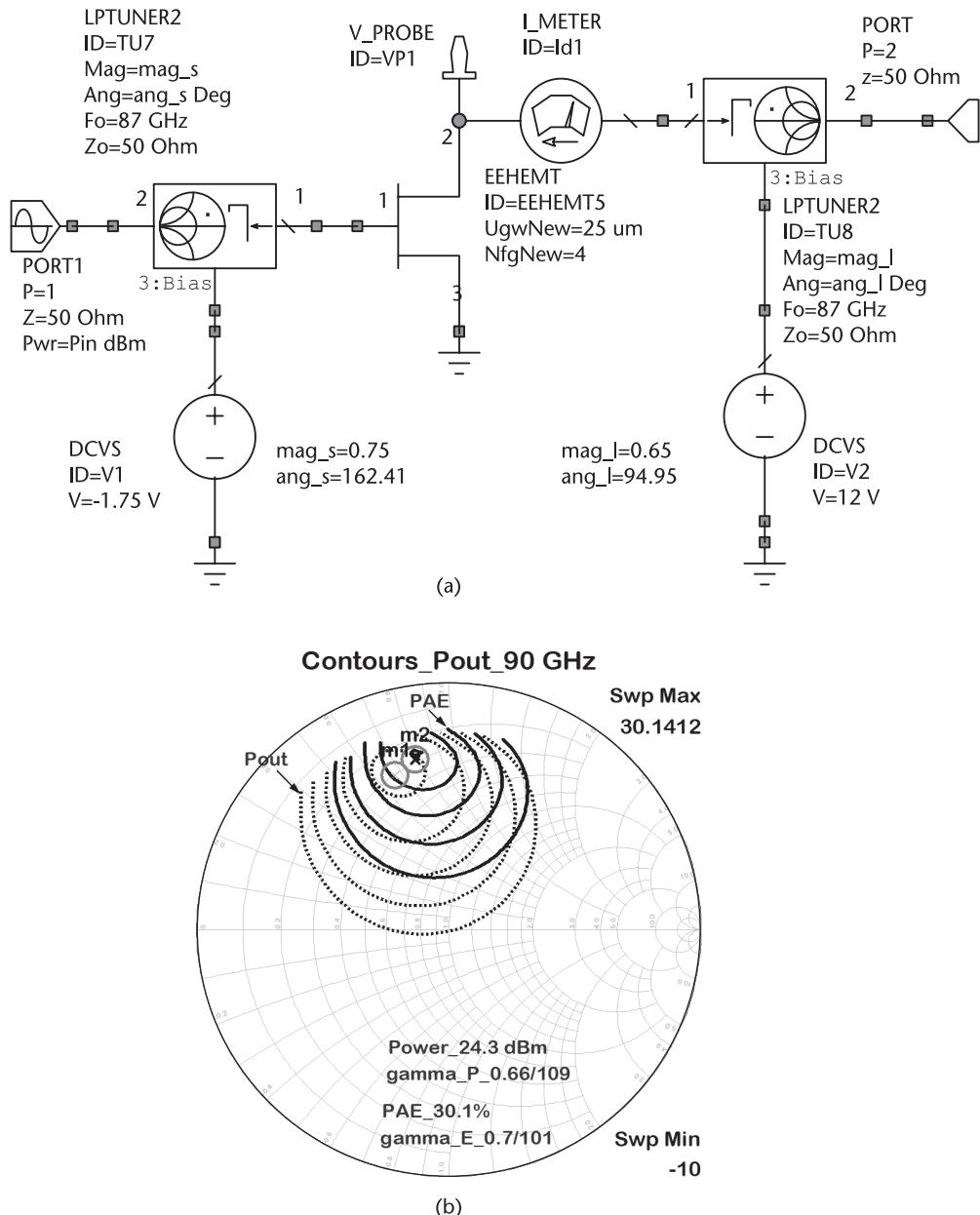
input drive of 17 dBm. Driving the amplifier above this point, the output power becomes compressed, reaching the saturated power,  $P_{SAT}^1 = 24.7$  dBm for an input drive of 21.7 dBm, and the drain efficiency is equal to 40%.

The efficiency and compressed gain are close to the published results. The simulated  $P_{SAT}$  gives a power density of 2.8 W/mm. That is higher than the published results, probably due the fact that the model in this simulation has a higher  $I_{DSS}$  compared to the model from [23].

The test bench in Figure 2.62(a) was employed in the determination of load and source impedance for best power and efficiency at 90 GHz. The simulator from Cadence AWR searches for the trade-off between the impedances for power and impedance for efficiency. The contours in Figure 2.62(b) are for 1 dB per step for power and 5% per step for efficiency.

A comparison of the device impedances obtained from different methods is shown in Table 2.7. Comparing the linear method with the numerical load-pull, we find a similar internal load resistance for both the linear method and the load-pull using the EEHEMT model. The prematch load resistance is lower than the values predicted by the linear method. That probably is due to the accuracy on predicting the S-parameters for the input and output matching blocks. On the gate side, we find a reasonable agreement for the real part of the impedance. The prematch also shows more deviation from the other values. The conjugated source/load terminations optimized for maximum gain, calculated from S-parameters, are also shown in the same table, for reference. A larger internal resistance is noticed for the small signal gain, which is an expected result. The input impedance shows a lower gate resistance.

The source and load parameters for two different unit cell sizes are in Table 2.8, defined for the gate and drain terminal. The columns named Linear correspond to values extracted from S-parameters under MAG. The columns named Power correspond to the parameters determined by the linear procedure from Section 2.7. The larger size device parameters were scaled from the smaller size. The small signal drain resistance under conjugate matching conditions is in the order of  $300\Omega$ . We



**Figure 2.62** Test bench for load-pull using a nonlinear model: (a) load pull schematic, and (b) contours of power and efficiency.

**Table 2.7** Source/Load Models from Different Sources at 90 GHz

Frequency = 87 GHz		Linear	Load Pull	Prematch	Gain
Source	$R_{in}$ ( $\Omega$ )	6.2	6	7.3	4.5
	$C_{in}$ (fF)	112	116	135	124
	$L_{in}$ (pH)	10.33	10.33	10.33	10.33
Load	$R_L$ ( $\Omega$ )	150	147	134	273
	$C_{out}$ (fF)	39.9	33	36	32
	$L_{out}$ (pH)	12.17	12.17	12.17	12.17

assumed that this condition only happens under simultaneous conjugated matched ports. Since the amplifier in general is not tuned for conjugate match, we limited this value to  $250\Omega$  in the simulations.

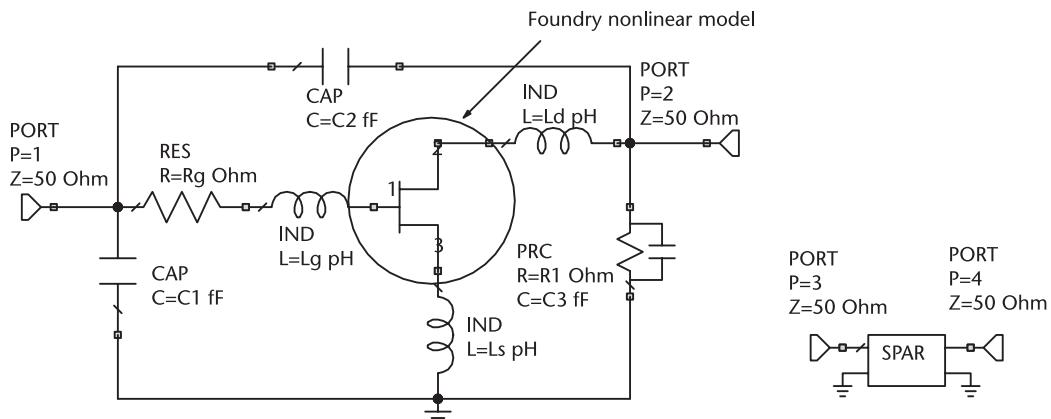
## 2.11 Model Modification

The designer of millimeter-wave power amplifiers should always characterize the S-parameters of the unit cells to be used in his project, provided from the selected foundry. The DC I/V evaluation is also important and can be performed at the same time. When designing MMICs, one should use the linear and nonlinear foundry models if available and verify if there is a match between the simulated and measured DC and S-parameters. However, if the S-parameter gain in particular is off compared to small-signal gain from nonlinear models, say, by more than 3 dB, the amount of gain compression will not be accurate. An alternative to allow the use of the foundry models is to externally modify the nonlinear model in order to match the measured S-parameters to the one determined from the nonlinear model.

In Figure 2.63, shunt and series elements are added to the nonlinear foundry model, and the small-signal S-parameters for the same device are contained in an S-parameter block SPAR. Using the same optimization tool utilized for extracting the linear model, the optimizer will modify the unknown parameters until there is

**Table 2.8** Source/Load Models for Different Cell Sizes at 90 GHz

Port	Parameter	$4 \times 25 \mu m$		$4 \times 37.5 \mu m$	
		Linear	Power	Linear	Power
Source	$R_{in}$ ( $\Omega$ )	4	6	2.6	4
	$C_{in}$ (fF)	112	112	168	168
	$L_{in}$ (pH)	10.3	10.3	6.8	6.8
Load	$R_L$ ( $\Omega$ )	300	150	167	100
	$C_{out}$ (fF)	40	3939	40	60
	$L_{out}$ (pH)	12.17	12.17	8.12	8.12



**Figure 2.63** Unit cell nonlinear foundry model S-parameters are modified to represent the small signal contained in the circuit block.

a match between both sets of S-parameters. Under this condition, the model can be used to observe the evolution of the power performance starting from small-signal to large-signal conditions.

## 2.12 Summary

This chapter introduced the basic structure and parameters of GaN HEMT devices. The concept of unit cells is widely used in the industry, being considered as the starting point of any amplifier design. The importance of evaluating S-parameters from the unit cells, as well as their power performance, was demonstrated. The resulting linear and nonlinear models allow associating unit cells to the gain and power level of interest. Stability is also a topic of importance and it was shown how to turn a unit cell to be unconditionally stable and how to explore the conditional stability in order to obtain a higher gain. In particular, we addressed the device modeling for gain and for power. The former is analytically determined from S-parameters and the latter is determined from DC evaluations and from the device linear model. Once the model is selected, the amplifier design procedure is similar to both.

## References

- [1] Ladbrooke, P. H., *MMIC Design: GaAs FETs and HEMTs*, Norwood, MA: Artech House, 1989, p. 189.
- [2] Hammerstad, E. O., “Equations for Microstrip Circuit Design,” *1975 European Microwave Conference*, 1975, pp. 268–272.
- [3] Alley, G. D., “Interdigital Capacitors and Their Applications to Lumped-Element Microwave Integrated Circuits,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 18, No. 12, December 1970, pp. 1028–1033.

- [4] Bazdar, M. B., et al., “Evaluation of Quasi-Static Matrix Parameters for Multiconductor Transmission Lines Using Galerkin’s Method,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, No. 7, July 1994, pp. 1223–1228.
- [5] Schellenberg, J. M., “Millimeter-Wave GaN SSPAs: Technology to Power 5G and the Future,” *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium*, 2020.
- [6] Micovic, M., et al., “GaN Double Heterojunction Field Effect Transistor for Microwave and Millimeterwave Power Applications,” *IEDM Technical Digest IEEE International Electron Devices Meeting*, San Francisco, CA, 2004.
- [7] Tseng, A. A., et al., “Electron Beam Lithography in Nanoscale Fabrication: Recent Development,” *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 26, No. 2, April 2003, pp. 141–149.
- [8] Pengelly, R. S., et al., “A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 60, No. 6, June 2012, pp. 1764–1783.
- [9] Lv, Y., et al., “Influence of AlGaN Barrier Layer on the RF Electric Characteristics for W-Band AlGaN/GaN HEMTs,” *2014 IEEE International Conference on Electron Devices and Solid-State Circuits*, 2014.
- [10] Joshin, K., et al., “Millimeter-Wave GaN HEMT for Power Amplifier Applications,” *IEICE Trans. Electron*, Vol. E97-C, No. 10, October 2014.
- [11] Micovic, M., et al., “GaN HFET for W-Band Power Applications,” *2006 International Electron Devices Meeting*, 2006.
- [12] Moon, J. S., et al., “Gate-Recessed AlGaN–GaN HEMTs for High-Performance Millimeter-Wave Applications,” *IEEE Electron Device Letters*, Vol. 26, No. 6, June 2005, pp. 348–350.
- [13] Fischer, R., et al., “On the Collapse of Drain I-V Characteristics in Modulation-Doped FET’s at Cryogenic Temperatures,” *IEEE Transactions on Electron Devices*, Vol. 31, No. 8, August 1984, pp. 1028–1084.
- [14] Shimawaki, H., and H. Miyamoto, “GaN-Based FETs for Microwave High-Power Applications,” *European GaAs Symposium*, Paris, 2005, pp. 377–380.
- [15] Huang, S., et al., “Effective Passivation of AlGaN/GaN HEMTs by ALD-Grown AlN Thin Film,” *IEEE Electron Device Letters*, Vol. 33, No. 4, April 2012, pp. 516–518.
- [16] Heying, B., et al., “Reliable GaN HEMTS for High Frequency Applications,” *IMS2010 International Microwave Symposium*, 2010, pp. 2118–1220.
- [17] Jardel, O., et al., “A Drain-Lag Model for AlGaN/GaN Power HEMTs,” *IMS2007*, 2007, pp. 601–604.
- [18] Xu, D., et al., “0.1- $\mu$ m InAlN/GaN High Electron-Mobility Transistors for Power Amplifiers Operating at 71–76 and 81–86 GHz: Impact of Passivation and Gate Recess,” *IEEE Transactions on Electron Devices*, Vol. 62, No. 8, August 2016, pp. 3076–3083.
- [19] Burnham, S. D., et al., “Reliability Characteristics and Mechanisms of HRL’s T3 GaN Technology,” *IEEE Transactions on Semiconductor Manufacturing*, Vol. 30, No. 4, November 2017, pp. 480–485.
- [20] Darwish, A. M., et al., “Dependence of GaN HEMT Millimeter-Wave Performance on Temperature,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-57, No. 12, November 2009, pp. 3205–3211.
- [21] Barr, J. T. IV, and M. J. Pervere, “A Generalized Vector Network Analyzer Calibration Technique,” *34th ARFTG Conference Digest*, Vol. 16, 1989.
- [22] Davidson, A., E. Strid, and K. Jones, “Achieving Greater On-Wafer S-Parameter Accuracy with the LRM Calibration Technique,” *34th ARFTG Conference Digest*, Vol. 16, 1989.
- [23] Camargo, E., et al., “F Band, GaN Power Amplifiers,” *IMS2018*, 2018.

- [24] Jarndal, A. H., “Parasitic Elements Extraction of AlGaN/GaN HEMTs on SiC Substrate Using Only Pinch-Off S-Parameter Measurements,” *IMS2014*, 2014, pp. 13–16.
- [25] Zairate-de Landa, A., et al., “A New and Better Method for the Extracting the Parasitic Elements of On-Wafer GaN Transistors” *IMS2007*, 2007, pp. 791–794.
- [26] Reynoso-Hernandez, J. A., et al., “A New Method for Extracting Ri and Rgd of the Intrinsic Transistor Model of GaN HEMT Based on Extrema Points of Intrinsic Y-Parameters,” *IMS2015*, 2015, p. 978.
- [27] Tasker, P. J., and B. Hughes, “Importance of Source and Drain Resistance to the Maximum  $f_T$  of Millimeter-Wave MODFET’s,” *IEEE Electron Device Letters*, Vol. 10, No. 7, July 1989, pp. 291–293.
- [28] Sze, S. M., *Physics of Semiconductor Devices*, New York: John Wiley & Sons, 1981, pp. 342–343.
- [29] Pozar, D. M., *Microwave and RF Design of Wireless Systems*, New York: John Wiley & Sons, 2001, pp. 201–204.
- [30] Maas, S. A., *Nonlinear Microwave and RF Circuits*, Norwood, MA: Artech House, 2003, pp. 407–409.
- [31] Camargo, E., D. Consoni, and R. Soares, “Reactance Compensation Matches FET Circuits,” *Microwave*, Vol. 24, 1985, pp. 93–95.
- [32] Agilent note 85190A, IC-CAP, Agilent Application Note, 85190A, 2008.
- [33] Angelov, I., H. Zirath, and N. Rorsman, “A New Empirical Nonlinear Model for HEMT and MESFET Devices,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, December 1992, pp. 2258–2266.
- [34] Wohlert, D., et al., “8-Watt Linear Three-Stage GaN Doherty Power Amplifier for 28 GHz 5G Applications,” *2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium*, Nashville, TN, 2019.
- [35] Xu, J., et al., “Dynamic FET Model—DynaFET—for GaN Transistors from NVNA Active Source Injection Measurements,” *IMS2014*, 2014.
- [36] Chang, Y. H., and J. J. Chang, “Analysis of an EEHEMT Model for InP pHEMTs,” *IMS 2007*, 2007, pp. 237–240.
- [37] Eskanadri, S., and F. T. Hamedani, “Extracting the Parameters of an EEHEMT Nonlinear Model for InP HEMT Operating at G-Band Frequency,” *19th International Conference on Mixed Design of Integrated Circuits and Systems*, Warsaw, Poland, May 24–26, 2012, pp. 360–363.
- [38] William, C., “Small and Large Signal Modeling of MM-Wave MHETM Devices,” Master thesis, University of Florida, 2003.
- [39] Conway, A. M., and P. M. Asbeck, “Virtual Gate Large Signal Model of GaN HFETs,” *IMS2002*, 2002, pp. 605–608.
- [40] Lautensack, C., S. Chalermwisutkul, and R. H. Jansen, “Modification of EEHEMT Model for Accurate Description of GaN HEMT Output Characteristics,” *Proceedings of the Asia-Pacific Microwave Conference*, 2007.
- [41] de Landa, A.Z., J. E. Z. Juarez, J. R. Loo-Yau, J. Apolinari, R. Hernandez, M. del Carmen Maya-Sanchez, and J. L. del Valle-Padilla, “Advances in Linear Modeling of Microwave Transistors,” *Microwave Magazine*, April 2009, pp. 100–112.

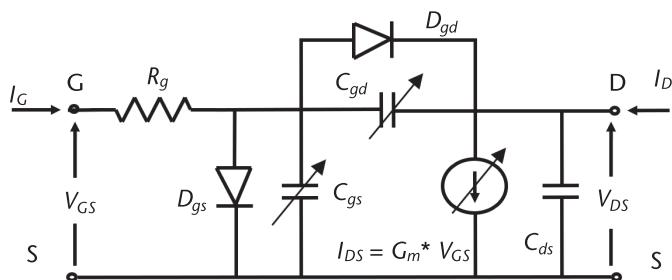


# FET-Based Amplifiers

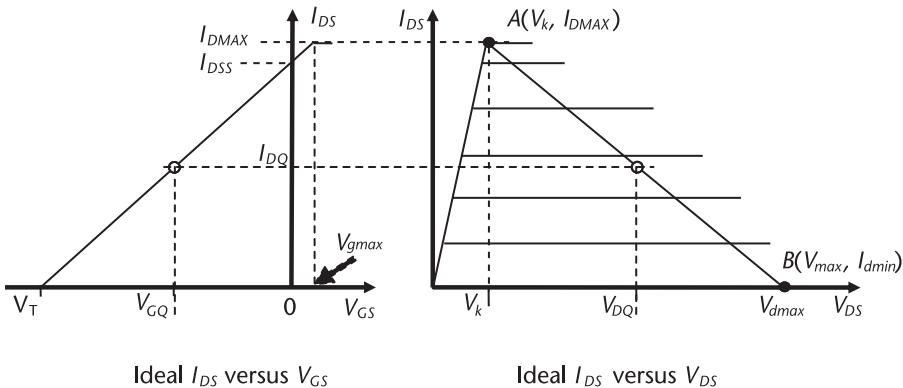
This chapter reviews basic FET amplifiers operation in classes A, AB, B, C, and F. The first four classes of operation differ by their biasing conditions, resulting in different modes of operation. It is therefore possible to describe them by their conduction angle. Class F, on the contrary, is biased similar to class B or AB, but their harmonic termination at the gate and the drain are simultaneously considered. A generic FET transistor model is initially used for the discussions and later replaced by an EEHEMT model. The metrics to compare power amplifiers used in this book are: gain, output power, linearity, and efficiency.

An idealized model for an FET is represented in Figure 3.1, where the ideal current source is controlled by the input voltage. The relation between them is a large signal transconductance,  $G_m$ . The diodes in the model account for the junctions in either GaAs FET or GaN HEMT devices. The other elements are considered parasitics of the device.

The large signal operation of the FET is defined by the DC I/V curves shown in Figure 3.2. Even though these curves have been linearized for simplicity, they show sources of nonlinearity (i.e., the knee region, cutoff, and saturation). They are quite significant to the operation of power amplifiers. At the output plane, we define a minimum drain voltage,  $V_{DS} = V_k$ , which determines the transition between linear and the saturated region. It is also often called  $V_{sat}$  for saturation voltage. A maximum voltage is defined as:  $V_{DS} = V_{D\text{MAX}}$ , which is dependent on device technology. For GaAs pHEMTs, it is dependent on the drain breakdown voltage,  $V_{D\text{MAX}} = V_B$ . For GaN HEMTs, it is defined by the dissipated power causing a maximum channel temperature,  $T_{\text{max}} = 150^\circ\text{C}$ . The current limitation is controlled by the gate voltage,  $V_{GS}$ . The maximum drain current,  $I_{DS} = I_{D\text{MAX}}$ , is defined as the drain current at the onset of gate-source diode conduction. That also defines the maximum DC gate voltage,  $V_{g\text{max}}$ . The gate voltage, which causes the drain current to stop flowing, is defined as the threshold voltage,  $V_T$ .



**Figure 3.1** Idealized model for an FET.



**Figure 3.2** Idealized DC I/V for FET devices.

### 3.1 Class A

In this section, the DC drain current is modeled as a function of gate voltage according to (3.1). That relation is assumed to be linear for gate voltages within the interval from the threshold voltage,  $V_T$ , to 0V.

$$\begin{cases} I_{ds} = I_{D\text{MAX}} \left(1 - \frac{V_{gs}}{V_T}\right), & V_T < V_{GS} < 0 \\ I_{ds} = 0, & V_{gs} < V_T \\ I_{ds} = I_{D\text{MAX}}, & V_{gs} > 0 \end{cases} \quad (3.1)$$

Class A corresponds to biasing the gate and drain voltages, such that the DC drain current is given by  $I_{DQ} = (I_{D\text{MAX}} - I_{d\text{min}})/2$ , defined as a quiescent current. The quiescent drain voltage is defined at the middle point between  $V_{D\text{MAX}}$  and  $V_k$  and is given by (3.2). For completeness, the quiescent gate voltage is similarly defined as half the difference between maximum and minimum gate voltage, (3.3).

$$V_{DQ} = V_k + \frac{(V_{D\text{MAX}} - V_k)}{2} = \frac{V_{d\text{max}} + V_k}{2} \quad (3.2)$$

$$V_{GQ} = \frac{(V_{g\text{max}} - V_T)}{2} \quad (3.3)$$

The representation of a class A amplifier with a resistive load  $R_L$  is shown in Figure 3.3. Introducing a continuous alternate voltage at the gate, the resulting drain voltage and current are represented by (3.5) and (3.6). In many instances, continuous wave (CW) is used to designate such a signal. The elements  $L$  and  $C$  are assumed

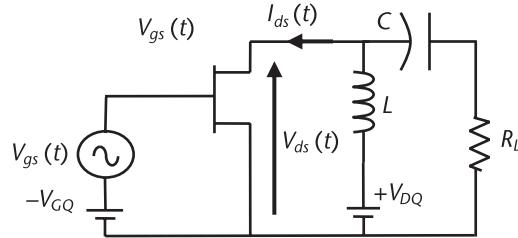


Figure 3.3 Class A amplifier with load  $R_L$ .

to be large and transparent for the AC signals at the drain port. Their waveforms are similar to the gate voltage as long as the magnitudes are below the DC limits.

$$V_{gs}(t) = V_{GQ} + V_p \cos(\omega t) \quad (3.4)$$

$$V_{ds}(t) = V_{DQ} - V_p \cos(\omega t) \quad (3.5)$$

$$I_{ds}(t) = I_{DQ} + I_p \cos(\omega t) \quad (3.6)$$

The line drawn between A ( $V_k, I_{D\text{MAX}}$ ) and B ( $V_{D\text{MAX}}, I_{d\text{min}}$ ) is called the load line. The slope of that line is given by  $I_{D\text{MAX}}/(V_{D\text{MAX}} - V_k)$  and is equal to the inverse value of the load resistance for class A. Equation (3.7) describes this geometrical definition. Considering the peak of sinusoidal voltage and current swinging around the middle point, the load resistance is also defined by (3.8). Taking (3.2) into (3.7), the load can then be expressed by (3.9). All three equations are equivalent.

$$R_L = \frac{(V_{D\text{MAX}} - V_k)}{I_{D\text{MAX}}} \quad (3.7)$$

$$R_L = \frac{V_p}{I_p} = \frac{\frac{(V_{D\text{MAX}} - V_k)}{2}}{\frac{I_{D\text{MAX}}}{2}} \quad (3.8)$$

$$R_L = \frac{2(V_{DQ} - V_k)}{I_{D\text{MAX}}} \quad (3.9)$$

The signal peak power is given by the product  $V_p I_p$ . The power of interest is the average power that is obtained by taking the root mean square values of peak voltage and current, (3.10). The power can also be defined in terms of the DC parameters for the device, by replacing  $V_p$  and  $I_p$ , as in (3.9).

$$P_{\text{out}} = \frac{V_p}{\sqrt{2}} \cdot \frac{I_p}{\sqrt{2}} = \frac{V_p I_p}{2} \quad (3.10)$$

$$P_{\text{out}} = \frac{(V_{D\text{MAX}} - V_k)I_{D\text{MAX}}}{8} = \frac{(V_{DQ} - V_k)I_{D\text{MAX}}}{4} \quad (3.11)$$

Other common definitions for power are in (3.12) and (3.13), where it is expressed in terms of the load resistance. The drain efficiency is defined by (3.15), relating the amount of RF power delivered to the load,  $P_{\text{out}}$ , and the power delivered from the power supply,  $P_{\text{DC}}$ . The PAE, which accounts for the gain of the device,  $G$  in (3.16), is also an important parameter.

$$P_{\text{out}} = \frac{(V_{D\text{MAX}} - V_k)^2}{8R_L} \quad (3.12)$$

$$P_{\text{out}} = \frac{R_L I_{D\text{MAX}}^2}{8} \quad (3.13)$$

$$P_{\text{DC}} = V_{DQ}I_{DQ} = \frac{(V_{D\text{MAX}} + V_k)I_{D\text{MAX}}}{4} \quad (3.14)$$

$$DE = \frac{P_{\text{out}}}{P_{\text{DC}}} = \frac{(V_{D\text{MAX}} - V_k)}{2(V_{D\text{MAX}} + V_k)} = \frac{V_{DQ} - V_k}{2V_{DQ}} \quad (3.15)$$

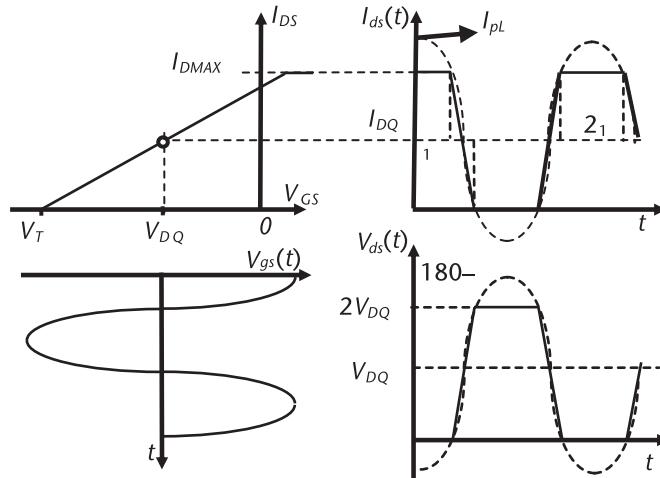
$$PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} = \frac{P_{\text{out}}}{P_{\text{DC}}} \left(1 - \frac{1}{G}\right) \quad (3.16)$$

Notice that the drain efficiency becomes 50% when  $V_k$  tends to 0. Also, if the gain is about 10 dB or more, then the PAE is approximately equal to the drain efficiency. If the amplifier gain is lower than 10 dB, it starts degrading the drain efficiency. In particular, when gain approaches the unit, there is no PAE. In class A, the optimum load for power and efficiency is the same. Notice that any change in the load lowers the output power while the DC power is maintained. Another relation important for thermal calculations is the dissipated power in the device,  $P_{\text{diss}}$ , (3.17). It is given by the difference between the DC power applied to the amplifier and the RF power that is delivered to the load.

$$P_{\text{diss}} = P_{\text{DC}} + P_{\text{in}} - P_{\text{out}} \quad (3.17)$$

### 3.1.1 Overdriven Class A

The waveforms for this condition are presented in Figure 3.4. The gate and drain voltage and current waveforms in this figure consider DC and AC values. The device is still biased in class A with a gate voltage alternating beyond the limits between  $V_{GS} = V_T$  and  $V_{GS} = 0$ . Hence, both tips of the drain voltage and current are clipped.



**Figure 3.4** Drain and gate waveforms.

The clipping occurs as shown in the figure for a resistive load. These clipped waveforms are correct if the load is broadband. That means that the load contains a resistive component and the eventual reactances in parallel are ideally zero up to the fourth harmonic component. If these conditions are not met, then the harmonics are filtered, and the drain voltage may become sinusoidal. In the figure, a linear drain current was superimposed on the drain waveform, showing the top of the sinusoid up to peak,  $I_{pL}$ . The negative tips are below 0 and are also clipped. A publication [1] approximated these waveforms by trapezoids, as illustrated in the figure.

The angles  $\alpha_1$ ,  $\alpha_2$ , indicate where the current starts to clip. Angle  $\alpha_1$  also indicates the current compression and  $\alpha_2$  determine the amplifier class (A, B, or C). Angle  $\alpha_3$  indicates the clipping of voltage and also measures the drain voltage compression. The drain current can be specified by (3.18). The drain voltage is specified by (3.19).

$$\begin{cases} I_{\max} = I_p + I_{DQ} \\ I_{ds}(t) = I_{DMAX}, 0 < \theta < \alpha_1 \\ I_{ds}(t) = I_{DQ} + I_p \cdot \cos(\theta), \alpha_1 \leq \theta < \alpha_2 \\ I_{ds}(t) = 0, \alpha_2 \leq \theta \leq 360 - \alpha_2 \end{cases} \quad (3.18)$$

$$\begin{cases} V_{ds}(t) = 0, 0 < \theta < \alpha_3 \\ V_{ds}(t) = V_{DQ} - V_{DQ} \cdot \cos(\theta), \alpha_3 \leq \theta < 180 - \alpha_3 \\ V_{ds}(t) = 2V_{DQ}, 180 - \alpha_3 \leq \theta \leq 180 + 2\alpha_3 \end{cases} \quad (3.19)$$

For class A operation, the conduction angles in Figure 3.4 are  $\alpha_1 = \alpha_3 = 0$ ,  $\alpha_2 = 180^\circ$ . For overdriven class A, it is assumed that both voltage and current will enter

into compression at the same input power level, making the conduction angles  $\alpha_1 = \alpha_3$ , and the clipping gives the degree of compression on the sinusoid. The Fourier analysis of these waveforms for the DC and fundamental components are expressed in (3.20) to (3.22) [1]. The DC component of voltage in this case is obviously the applied supply voltage,  $V_{DQ}$ . The knee voltage is assumed to be 0 in these equations. It can easily be taken into account by replacing  $V_{DQ}$  by  $V_{DQ} - V_k$ .

$$V_{d1} = \frac{V_{DQ}}{\pi} \frac{\pi - 2\alpha_3 + \sin(2\alpha_3)}{\cos(\alpha_3)} \quad (3.20)$$

$$I_{d1} = \frac{I_{DMAX}}{\pi} \frac{\cos(\alpha_1)\sin(\alpha_1) - \cos(\alpha_2)\sin(\alpha_2) + \alpha_2 - \alpha_1}{\cos(\alpha_1) - \cos(\alpha_2)} \quad (3.21)$$

$$I_{d0} = \frac{I_{DMAX}}{\pi} \frac{\alpha_1 \cos(\alpha_1) - \alpha_2 \cos(\alpha_2) + \sin(\alpha_2) - \sin(\alpha_1)}{\cos(\alpha_1) - \cos(\alpha_2)} \quad (3.22)$$

The DC and RF output power can be calculated by using (3.23) and (3.24). They assume that the drain voltage is symmetrical around the bias point  $V_{DQ}$ . Assuming symmetrical clipping, one can relate  $\alpha_1$  and  $\alpha_2$  by  $\alpha_2 = \pi - \alpha_1$ .

$$P_{DC} = \frac{V_{DQ} I_{DMAX}}{\pi} \frac{\alpha_1 \cos(\alpha_1) - \alpha_2 \cos(\alpha_2) + \sin(\alpha_2) - \sin(\alpha_1)}{\cos(\alpha_1) - \cos(\alpha_2)} \quad (3.23)$$

$$P_{out} = \frac{V_{DQ} I_{DMAX}}{2\pi^2} \frac{\pi - 2\alpha_3 + \sin(2\alpha_3)}{\cos(\alpha_3)} \frac{\sin(\alpha_1)\cos(\alpha_1) - \sin(\alpha_2)\cos(\alpha_2) + \alpha_2 - \alpha_1}{\cos(\alpha_1) - \cos(\alpha_2)} \quad (3.24)$$

Replacing the angles into the equations, we find, as expected, no change in the DC power, and on the bias current as a consequence. The output power for a class A overdriven amplifier, with a nonsinusoidal drain voltage, is in (3.25). This power is denominated as  $P_{SAT}$  for saturated power.

$$\begin{aligned} P_{DQ} &= \frac{V_{DQ} I_{DMAX}}{\pi} \frac{\alpha_1 \cos(\alpha_1) + (\pi - \alpha_1) \cos(\alpha_1)}{2 \cos(\alpha_1)} = V_{DQ} I_{DQ} \\ P_{out} &= \frac{V_{DQ} I_{DMAX}}{2\pi^2} \frac{\pi - 2\alpha_1 + \sin(2\alpha_1)}{\cos(\alpha_1)} \frac{\pi - 2\alpha_1 + 2 \sin(\alpha_1) \cos(\alpha_1)}{2 \cos(\alpha_1)} \\ P_{out} &= \frac{V_{DQ} I_{DMAX}}{4\pi^2} \left( \frac{\pi - 2\alpha_1 + \sin(2\alpha_1)}{\cos(\alpha_1)} \right)^2 \end{aligned} \quad (3.25)$$

The power compression can be determined from the ratio between the uncompressed current peak,  $I_{pL}$ , and the compressed value,  $I_{DMAX}$ . In (3.6), let us make the peak value,  $I_{ds}(t) = I_{DMAX}$ , change the angle to  $\alpha_1$  and make the cosine's magnitude

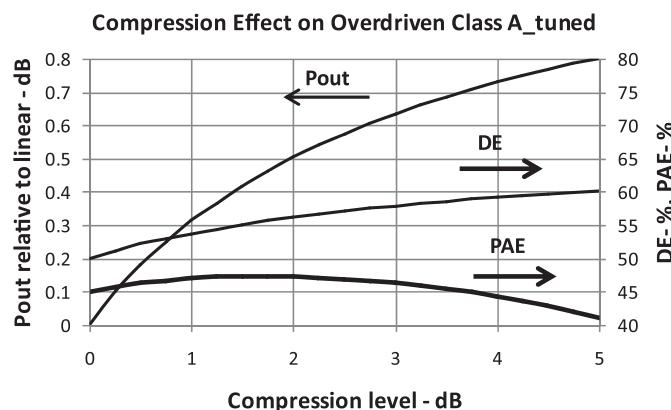
equal to the linear peak value [2]. The DC bias current is assumed to be  $I_{D\text{MAX}}/2$ . According to Figure 3.4, the angle  $\alpha_1$  represents half the conduction angle; therefore, the total angle is  $2\alpha_1$ .

$$\begin{aligned} I_{D\text{MAX}} &= I_{DQ} + I_{pL} \cos(\alpha_1) \\ \cos(\alpha_1) &= \frac{I_{D\text{MAX}}}{2I_{pL}} \end{aligned} \quad (3.26)$$

Taking the square of (3.26), we can calculate the amount of compression,  $C_L$ , as a function of the clipping angle,  $\alpha_1$ . Only half of the conduction angle defines the compression.

$$C_L = \frac{1}{\cos^2(\alpha_1)} \quad (3.27)$$

Figure 3.5 represents the power, drain efficiency, and PAE as a function of compression level for an overdriven class A amplifier. The output power starts from 0, so there is no compression and the output power is normalized to the linear value considered. The plots assume an amplifier with an SSG of 10 dB and a constant bias current and load impedance. Figure 3.5 shows the power, drain efficiency, and PAE for the tuned load case. One can see that a maximum increment in power at 5-dB compression is 0.8 dB. Since the DC power remains the same, it is expected that the drain efficiency will increase. The plot shows an increase from 50% to 60% at the same level of compression. The drain efficiency increases slightly at 3 dB and then drops to 41% at 5-dB compression. This drop is a direct consequence of a low amplifier gain. Figure 3.6 shows a case of resistive load, where higher output power and efficiency are the result of the voltage clipping.



**Figure 3.5** Overdriven class A: tuned load.

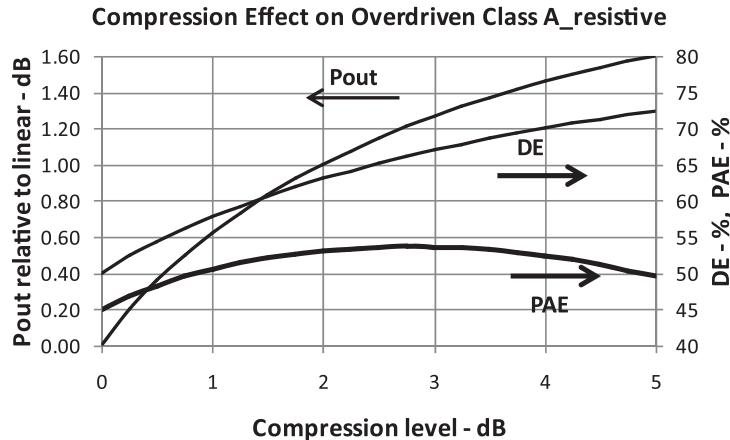


Figure 3.6 Overdriven class A: resistive load.

### 3.2 Class B

Now let us modify the gate voltage of the circuit in Figure 3.7 so that the gate is biased at pinch-off and the drain is biased at the quiescent voltage,  $V_{DQ}$ . Under this condition, there is no drain current circulating from the drain to the source. Then a sinusoidal signal with an amplitude  $V_g(t)$  is applied to the gate. The amplitude has to be larger than the threshold voltage that is  $V_g(t) - V_T > 0$ . As a consequence, a corresponding half-sinusoidal current starts circulating in the drain, as depicted in Figure 3.8, extracting current from the voltage supply through the inductor  $L$ . The drain current increases with gate voltage until the sinusoid hits the limit given by the gate-source diode junction conduction. When the gate voltage returns to  $V_T$ , the energy stored in the inductor goes back to 0. The voltage at the load follows the inductor voltage, as long as the time constant  $R_L C$  is low. The main purpose of the series capacitor  $C$  is to block the circulation of DC to the load.

The  $I_{DS}(V_{DS})$  relation is depicted by the dark line in Figure 3.8. There is no longer a meaning for a load line, as there are two lines to represent this relation: one between  $V_k$  and  $V_{DS}$  and another between  $V_{DS}$  and  $V_{DD}$ . A better term is an I/V trajectory. During the gate-voltage negative cycle, the I/V relation is a horizontal line. If the drain bias is the same as class A, the slope of the line for the positive

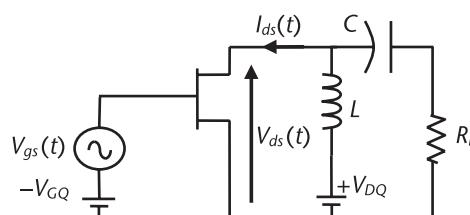
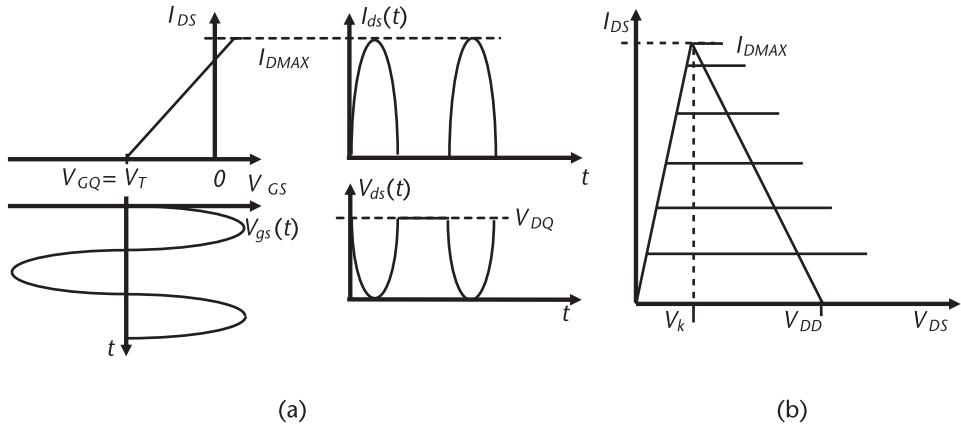


Figure 3.7 Class B amplifier with resistive load  $R_L$ .

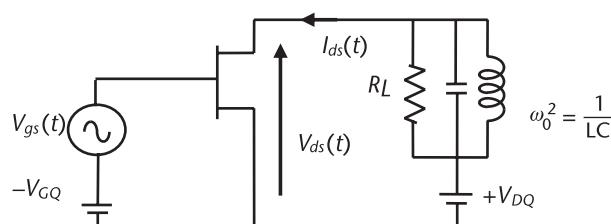


**Figure 3.8** Waveforms for a class B amplifier with a resistive load  $R_L$ : (a) drain and gate voltages and currents, and (b) corresponding I/V trajectory.

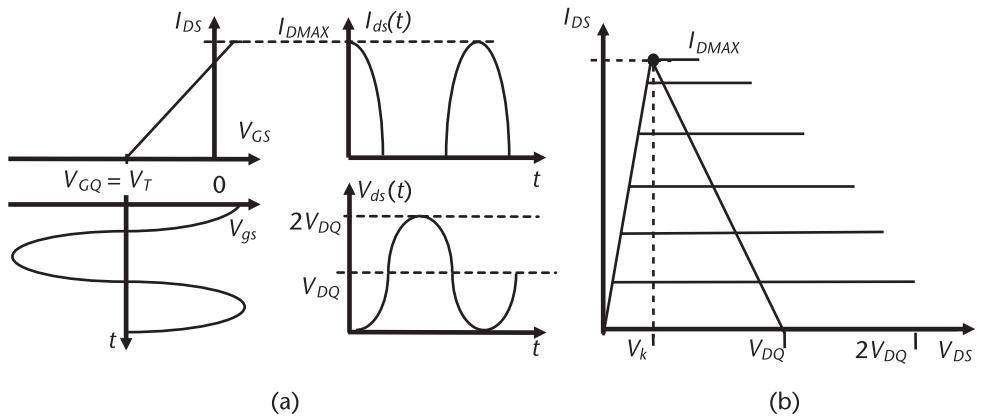
gate-voltage cycle is equal to half the slope of the class A load, assuming  $V_k = 0$ . One can see that the voltage and current waveforms are clipped and therefore this mode of operation is not useful as an RF power amplifier.

Let us now add a capacitor in shunt with the load as shown in Figure 3.9. Considering a steady-state condition where transients have faded out, when the energy stored in the inductor goes to 0, the energy stored in the capacitor is maximum. Thus, the voltage in the capacitor increases to  $V_{DQ}$  on top of the power supply voltage, doubling the voltage when  $I_d(t) = 0$ . From a frequency-domain point of view, the impedance of the LC-tuned circuit at the resonance frequency  $\omega_0$  is infinite so that the fundamental frequency sinusoidal voltage develops across the resistor  $R_L$  for a half-sinusoidal or square pulse applied to the circuit. The harmonic components contained in the distorted drain voltage are mostly shorted to ground by the tuned circuit.

The class B current and voltage waveform results are shown in Figure 3.10. The conduction angle is reduced from the full  $360^\circ$  in class A to  $180^\circ$ . The plot in Figure 3.10 also shows the  $I_{DS}(V_{GS})$  relation for a complete gate-voltage cycle. An equivalent load resistance in the frequency domain is still defined. From a basic Fourier analysis, let us consider the fundamental component of the drain half-clipped sinusoidal current,  $I_{DMAX}/2$ . The load voltage is still a sinusoid; thus, the peak voltage at the



**Figure 3.9** Schematic for the class B operation.



**Figure 3.10** Waveforms for class B amplifier with tuned load: (a) drain and gate voltages and currents, and (b) corresponding I/V trajectory.

fundamental frequency is  $V_{DQ}$ . The load impedance is defined by (3.28), which, remarkably, is similar to the load for class A, given by (3.9).

$$R_{L1} = \frac{V_{d1}}{I_{d1}} \approx \frac{2(V_{DQ} - V_k)}{I_{DMAX}} = \frac{2V_{DQ}}{I_{DMAX}} \quad (3.28)$$

The power and efficiency for maximum current is given by the (3.27) and (3.28). The classical value of 78.5% drain efficiency is obtained when  $V_k = 0$ .

$$P_{\text{out}} = P_{\text{max}} = \frac{(V_{DQ} - V_k)I_{DMAX}}{4} \quad (3.29)$$

$$DE = \frac{\pi}{4} \frac{V_{DQ} - V_k}{V_{DQ}} \quad (3.30)$$

Another important feature of class B amplifiers is the linear relation between the gate voltage and the drain current. The waveform at the load is the same as in class A, which is the reason that class B is considered a linear amplifier. However, it does have a disappointing drawback. Notice that, compared to class A, the gate amplitude needs to be doubled for the maximum drain current value. That means that the gain is reduced by 6 dB. This gain drop usually is not a suitable solution for millimeter-wave where amplifier gain is often below 10 dB. Another drawback of class B is the need of a minimum input voltage to start the flow of drain current. That is not acceptable for linear operation, where the power amplifier is expected to amplify both small signals and large signals.

Now let us assume power is reduced by 3 dB in a class B amplifier. That makes the drain and voltage coefficients to be reduced by  $\sqrt{2}$ . If we increase the load by a factor of  $R_{L1}\sqrt{2}$ , the voltage magnitude is recovered. It can easily be demonstrated that the recovered voltage will provide the original efficiency of  $\pi/4$ , with 1.5-dB lower power. If the slope on the linear region is taken into account, the  $V_k$  factor will be lower, so that the efficiency is slightly higher for a load resistor 40% larger.

That property is used by Doherty amplifiers to improve the efficiency. The class B trajectory is represented by a dark trace in Figure 3.11 and for the cases of load impedance higher and lower. For a lower load, the current is constant at  $I_{D\text{MAX}}$  and  $V_{d\text{min}} > V_k$ .

The output power is therefore calculated by (3.31) and the drain efficiency is calculated from (3.32). The power is independent of drain voltage, while the efficiency is inversely proportional. The load is considered tuned and the drain voltage is sinusoidal.

$$P_{\text{out}} = \frac{R_L I_{D\text{MAX}}^2}{8} < P_{\text{max}} \quad (3.31)$$

$$DE = \frac{\pi}{8} \frac{R_L I_{D\text{MAX}}}{V_{DQ}} < 78.5\% \quad (3.32)$$

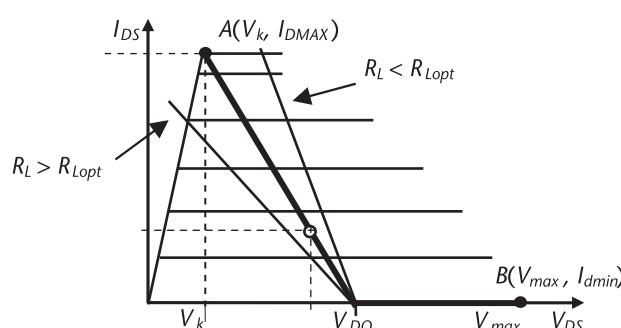
The second situation is for a load resistance higher than  $R_{L\text{opt}}$ . The maximum current is then reduced to  $I_{dm}$ , which is defined by (3.33), using the approximation  $V_{d\text{min}} = R_{\text{on}} \cdot I_{dm}$ . The minimum voltage is also different, defined by (3.34). The load impedance then is defined by (3.35).

$$I_{dm} = \frac{2V_{DQ}}{R_L + 2R_{\text{on}}} \quad (3.33)$$

$$V_{d\text{min}} = \frac{2R_{\text{on}} V_{DQ}}{R_L + 2R_{\text{on}}} \quad (3.34)$$

$$R_L = \frac{2(V_{DQ} - V_{d\text{min}})}{I_{dm}} \quad (3.35)$$

Notice that the parameter  $R_{\text{on}}$  shows up in (3.33) as a resistance in series with the load resistance. Thus, the effective load resistance increases, with power loss in  $R_{\text{on}}$ . The corrected power is obtained from (3.36), using the new maximum value for the current,  $I_{dm}$ . The drain efficiency is then straightforward, as defined by (3.37). The



**Figure 3.11** Class B I/V trajectory.

power decreases with the increase of the load resistor, and there is a small increase in the efficiency. When  $R_L \gg 2R_{\text{on}}$ , then the drain efficiency tends to 78.5%.

$$P = \frac{R_L I_{dm}^2}{8} = \frac{R_L}{2} \frac{V_{DQ}^2}{(R_L + 2R_{\text{on}})^2} < P_{\text{max}} \quad (3.36)$$

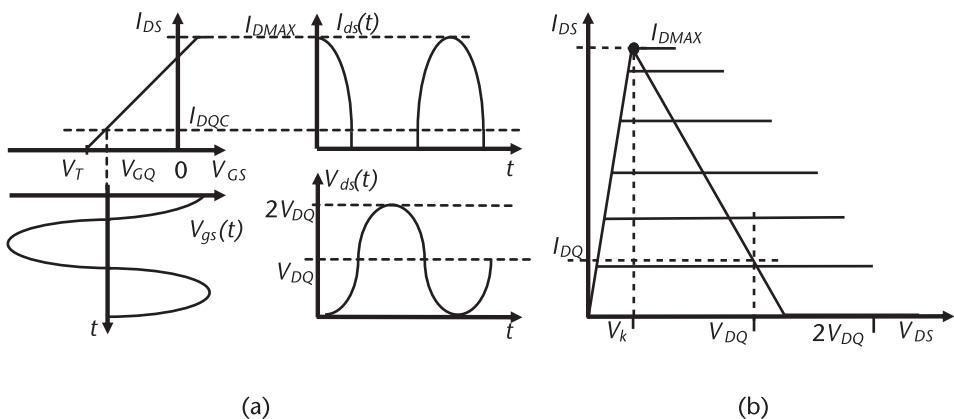
$$DE = \frac{\pi}{4} \frac{R_L}{R_L + 2R_{\text{on}}} < 78.5\% \quad (3.37)$$

The equations for a class B resistive proposed in [3] have a peak current defined by the difference between the maximum current and the DC value,  $I_p = I_{\text{DMAX}} - I_{\text{DMAX}}/\pi$ . This value is different for a tuned amplifier, where  $I_p = I_{\text{DMAX}}/2$ .

### 3.2.1 Class AB

The class AB operation is set by moving the gate bias so that  $V_{GS}$  is located between  $V_T$  and  $V_{GQ}$ , as shown in Figure 3.12. Thus, the drain current is no longer a true half-wave sinusoid waveform but the drain voltage continues to be sinusoid, due to the tuned circuit action. At low drive levels, smaller than  $V_T - V_{GQ}$ , the RF will alternate around the quiescent bias point and the output will follow the gate as in class A. As the gate-voltage amplitude increases, the drain current starts being clipped on the negative cycle. The drain current will reach  $I_{\text{DMAX}}$  for an input drive voltage higher than class A drive and lower than the one required by class B drive. While the current is off, the drain voltage is recovered from the energy stored in the tuned circuit. The  $I_{DS}(V_{DS})$  trajectory in the output plane is represented in the same figure. In the time domain, it is intuitive to conclude that the load resistance during the active cycle is a bit higher than the resistance for class B for the same drain bias point.

The DC gate voltage is fixed and the DC drain current is equal to  $1/\pi$  of the peak current value. However, the drain current waveform is dependent on the drive level, resulting in a nonlinear operation. In real amplifiers, there are other effects



**Figure 3.12** Waveforms for the class AB amplifier: (a) drain and gate voltages and currents, and (b) corresponding I/V trajectory.

that modify the waveforms, including DC rectification at the gate junction. Equations (3.21) to (3.25) can be used to represent the class AB operation by making  $\alpha_1 = \alpha_3 = 0$  and  $90^\circ \leq \alpha_2 \leq 180^\circ$ . As far as power is concerned, the maximum power delivered by a class A amplifier is the same as the power delivered by a class B. Slight higher power is expected in class AB due to the small increase in the load resistance.

### 3.2.2 Overdriven Class B and AB

The overdrive condition in a true class B setting starts when the gate voltage goes beyond the maximum gate voltage causing the drain current to be clipped. Care should be taken to limit the gate current below the limit determined by the manufacturer.

Equations (3.19) to (3.22) are valid to determine the effect of gain compression on the amplifier performance, as shown in Figure 3.13, up to a compression level of 5 dB. This figure shows an increment in power, topping 0.85 dB at 5-dB compression. It may seem to be a small difference, but it is more than 200 mW for a 1-W amplifier. Unfortunately, the drain efficiency drops from 78.5% to 74%, which is not desirable for efficiency. At higher levels of compression, the current waveform becomes approximately a square wave.

The class AB overdrive is more complex. The waveforms for the overdriven condition are illustrated in Figure 3.14. The drain voltage is assumed to be sinusoidal, which is achievable by selecting the load such that the voltage does not exceed the limit set by the rail voltage [4]. Due to the interaction of bias with an applied RF signal, the gate waveform changes the bias point. In the figure, one can notice that the sinusoid is cut off at an angle  $\beta_1$ . Maintaining the gate bias fixed and increasing the gate voltage, the cutoff changes to  $\beta_2$ .

This effect is not considered in the equations and causes the power and efficiency calculation to be inaccurate. The Fourier treatment of these effects is far more complex than a class B. The interaction effect between RF large levels and the bias, shown in Figure 3.15, were solved by Cripps, who calculated the Fourier coefficients taking them into account [5]. The results are in Figure 3.15, generalized for any conduction angle. Class A, after compression, has an increase in power to 0.8 dB maximum and about 10% in drain efficiency. This result is similar to the one shown in Figure 3.6, generated from different equations.

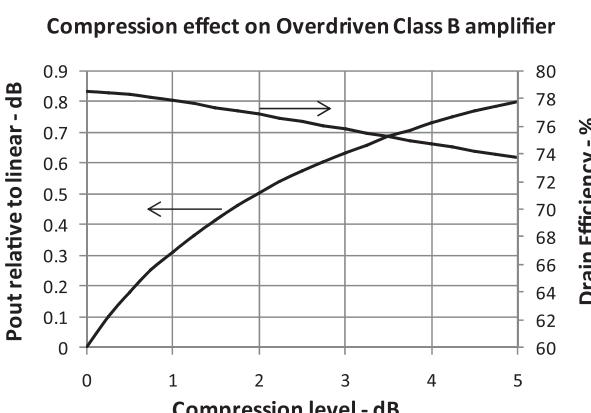
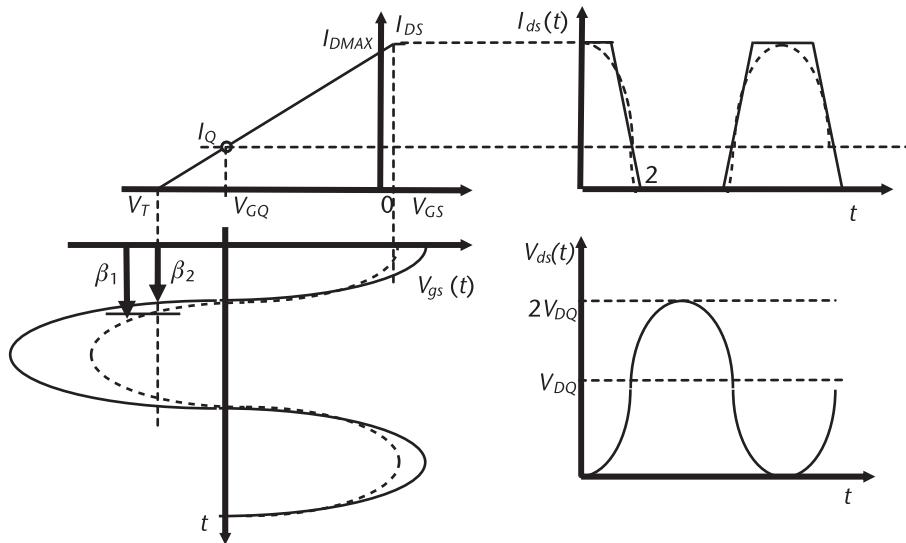
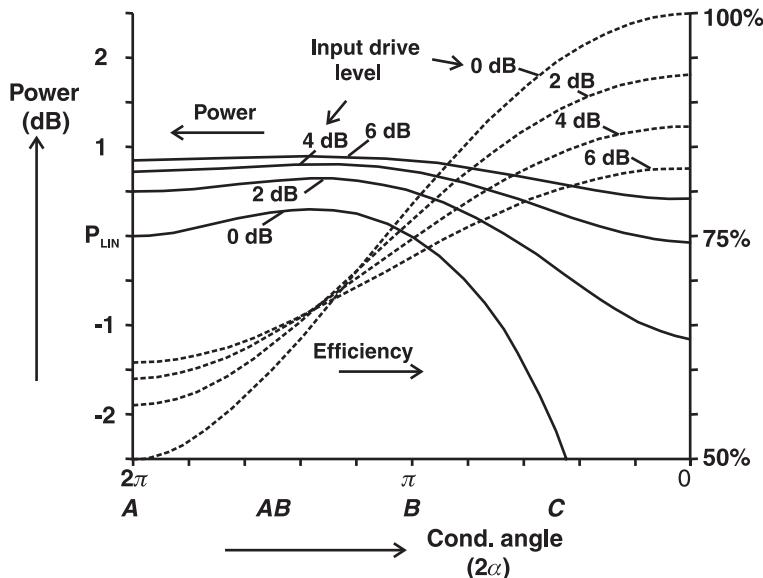


Figure 3.13 Class B overdriven effect on power and drain efficiency.



**Figure 3.14** Class AB overdriven waveforms. The dotted line shows a normal class AB. The solid line describes the overdriven drain current.

Class B amplifiers operating under saturation have a maximum of a 0.8-dB increase in power when compressed at 6 dB, but their efficiency degrades from 78.5% down to 70%. A similar result was shown in Figure 3.13. The curves also show that operation in class C results in a loss of power and efficiency, compared to class B. An overdriven class AB operation does provide a bit more power, but there is no effective improvement in efficiency. Class A provides an advantage in both power and efficiency.



**Figure 3.15** Power and efficiency as a function of conduction angle and compression level. The solid lines are for power and the dotted ones for efficiency. The 0-dB plots correspond to an unsaturated operation. The numbers 2 dB, 4 dB, and 6 dB correspond to the level of gain compression. (After: [5]. © 2006 by Artech House.)

### 3.2.3 Summary of Operation Classes

If we make the coefficient  $\alpha_3 = 0$ , the drain voltage is sinusoidal. In terms of a circuit, this is achieved by using an adequate load and/or filtering the harmonics. Also, if  $\alpha_1 = 0$ , the positive peak of drain current is sinusoidal. Taking those values to (3.21) and (3.22), the remaining coefficient  $\alpha_2$  controls the class of operation. The DC power and RF power can therefore be obtained from (3.38) and (3.39), respectively. They are used to define the power and drain efficiency performance as a function of the class of operation. The application of these equations results in the curves of Figure 3.16, showing power relative to class A power and drive level such that the drain current is always at its peak at  $I_{\max}$ .

$$P_{DC} = \frac{V_{DQ} I_{D\text{MAX}}}{\pi} \frac{\sin(\alpha_2) - \alpha_2 \cos(\alpha_2)}{1 - \cos(\alpha_2)} \quad (3.38)$$

$$P_{\text{out}} = \frac{V_{DQ} I_{D\text{MAX}}}{2\pi} \frac{\alpha_2 - \sin(\alpha_2)\cos(\alpha_2)}{1 - \cos(\alpha_2)} \quad (3.39)$$

On the horizontal axis, the first point on the left corresponds to a conduction angle of  $2\pi$ , representing class A. At this point, the drain efficiency is seen to be 50%. There is a slight increase in power when moving from class A to B where the angle is equal to  $\pi$ . The power at this point is similar to class A, but efficiency is near 78.5%. Decreasing the conduction angle further, we move into class C on the right. The drain efficiency increases but at the cost of high reduction in the output power and gain.

The drain load for any class,  $R_L$ , is obtained by dividing the fundamental component of drain voltage by the fundamental component of the drain current. This is expressed by (3.40).

$$R_L = \frac{V_{DQ}}{I_1} = \frac{\pi V_{DQ}}{I_{D\text{MAX}}} \frac{1 - \cos(\alpha_2)}{\alpha_2 - \sin(\alpha_2)\cos(\alpha_2)} \quad (3.40)$$

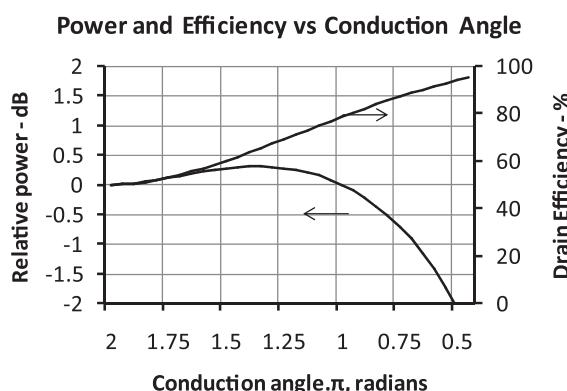


Figure 3.16 Normalized power and drain efficiency as a function of the conduction angle,  $\alpha_2$ .

The load for class B is obtained by making  $\alpha_2 = \pi/2$  in the equation. At any other angle in between  $\pi$  and  $2\pi$ , there is a small increase in the load. For practical reasons, the class AB load is considered to be equal to class A. This is an approximate conclusion, which neglects the interaction between signal levels and changes in the DC component due to internal device nonlinearities. The gain in drain efficiency between classes A and B is found by relating (3.32) and (3.17), giving a value equal to  $\pi/2$ .

$$DE_{\text{class B/A}} = \frac{\pi}{2} = 1.57 \quad (3.41)$$

### 3.3 Linearity in Amplifiers

An amplifier designed for wireless communications must possess a certain level of linearity that is dependent on the type of amplifier and the type of modulation system. In a low noise amplifier, the circuit elements are considered weakly nonlinear but generate distortions in the waveforms that may affect the system performance. However, in power amplifiers, the linearity of the circuit elements are considered mildly strong depending on the power of operation. The trend is to use amplifiers with a certain backoff output power level, such that the distortion is acceptable for the specific application.

Applying a single tone at the gate of an FET as a function of power will result in two types of distortion measured at the output. The AM-to-AM distortion causes compression or expansion in the amplifier gain, and the AM-to-PM distortion causes the phase of the amplifier gain to increase or decrease as a function of power. Both parameters are ideally constant with power and become modulated when the power level comes near the  $P_{1\text{dB}}$  point. The single-tone distortion can be described by considering the relation between the drain current and the gate voltage in FETs. In Figure 3.2, the amplifier is assumed to be linear as long as the voltage and current are within the  $V_{D\text{MAX}}, I_{D\text{MAX}}$  limits. However, in real devices, the linear condition is valid only for voltages near the bias point. As the signal amplitude increases, the representation between the drain current and the gate voltage requires a Taylor series representation, described by (3.42), truncated at the third order. When the signal increases beyond a certain level, more terms have to be added to the series. The relation is valid for operation at low frequencies where the device capacitive nonlinearities have no effect on the currents and voltages. Inserting (3.43) into (3.42), one obtains (3.44), where coefficient  $a_1$  is larger than coefficient  $a_3$ .

$$V_d = a_0 + a_1 V_g + a_2 V_g^2 + a_3 V_g^3 \dots \quad (3.42)$$

$$V_g = V_0 \cos(\omega t) \quad (3.43)$$

The output voltage is linear and proportional to coefficient  $a_1$  for small input levels. The point of 1-dB compression is reached when the linear output voltage drops by same amount in terms of voltage. This output voltage is taken to (3.44)

to determine the input voltage that causes the 1-dB compression, (3.45). With the increase of the signal drive, the second term becomes significant and introduces an AM-to-AM modulation. The same effect in terms of gain is described by (3.46). The amplifier gain decreases above a certain amplitude level considering the term  $a_3 < 0$ , resulting in gain compression. Under certain conditions,  $a_3$  can be positive, resulting in gain expansion.

$$Vd_{\omega} = a_1 V_0 + \frac{3}{4} a_3 V_0^3 \quad (3.44)$$

$$\begin{aligned} Vd_{\omega} &= a_1 V_0 10^{-0.5} \\ Vd_{\omega_{1dB}} &= \frac{4a_1(1 - 10^{-0.5})}{3a_3} \end{aligned} \quad (3.45)$$

$$G_p = \frac{Vd_{\omega}}{V_0} = a_1 + \frac{3}{4} a_3 V_0^2 \quad (3.46)$$

However, it can be demonstrated that capacitance can generate a phase modulation, even if the phase shift is constant and independent of signal amplitude [6]. In order to demonstrate this effect, let us express the output voltage as a vector sum of two phasors expressed by (3.47). One can see that, with the signal increase, the second term adds phase modulation to the output voltage. This class of amplifier is qualified as a quasi-memoryless amplifier. The definition applies when the circuit time constants are of the same order as the RF carrier.

$$Vd_{\omega} = a_1 V_0 + \frac{3}{4} a_3 V_0^3 e^{j\theta} \quad (3.47)$$

These distortion effects can be associated with the nonlinear FET current source and with the reactance nonlinearities. They can be improved to a certain extent by the amplifier design and by an amplifier topology that includes linearization enhancement. When the envelope of the modulated signals becomes modulated, the AM-to-AM and the AM-to-PM distortions become dependent on the history of past signal levels. Amplifiers that follow this behavior are defined as nonlinear amplifiers with memory [7]. The distortion is created by temperature effects, baseband terminations, and trapping effects on the semiconductor material. GaN amplifiers belong to this category.

The two-tone test consists in applying two CW signals at frequencies  $\omega_1$  and  $\omega_2$  spaced by a certain frequency within the signal bandwidth, as represented by (3.48). Inserting this voltage in (3.42), there will be many frequency components at the output. Let us retain only the fundamental tone at frequencies  $\omega_1$  and  $\omega_2$  and the components at the adjacent sidebands at the frequencies  $2\omega_1 - \omega_2$  and at  $2\omega_2 - \omega_1$ . The generated tones define what is called intermodulation distortion of the third order,  $IM_3$ . There are also fifth-order terms, but they are of lower amplitude compared with the third order.

$$V_g = V_0 (\cos(\omega_1 t) + \cos(\omega_2 t)) \quad (3.48)$$

The output power at the fundamental frequencies  $\omega_1$  and  $\omega_2$  is defined in terms of the input voltage and coefficient  $a_1$  in (3.48). Increasing the drive level, the output power increases on a decibel-per-decibel basis, resulting in a slope of 1. Equation (3.50) describes the output intermodulation power, on a 3 dB per dB of input power, so that the slope increases with a slope of 3:1. That is valid for both sidebands.

$$P_{\omega_1} = P_{\omega_2} = P_{\text{outS}} = \frac{1}{2} a_1^2 V_0^2 \quad (3.49)$$

$$P_{2\omega_2-\omega_1} = P_{2\omega_1-\omega_2} = P_d = \frac{9}{32} a_3^2 V_0^6 \quad (3.50)$$

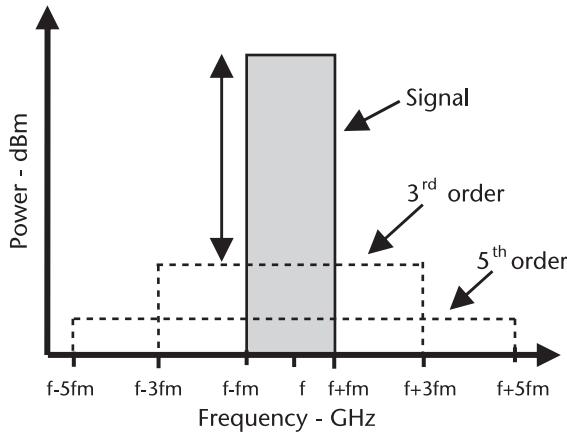
It is intuitive that increasing the signal voltage in the two functions, corresponding to lines in a rectangular plot, there is a point where both will cross due to the slope difference. Therefore, equating both (3.49) and (3.50), one can determine the drive level at which this will occur. That particular voltage,  $V_{IP}$ , is expressed by (3.51) and defines the third-order intercept point. Normalizing the output power, (3.49), by the distortion power, (3.50), and using (3.51), a simple relation is obtained for  $IMR_3$  or  $IP_3$ , based on the fundamental and distortion power levels, (3.52) and (3.53), respectively [8].  $IMR_3$  is defined as the ratio of intermodulation to the fundamental component, and  $IP_3$  is defined as the intercept point of the third order. In the equations,  $P_{\text{outT}}$  defines the power of both carriers and  $P_{\text{outS}}$  defines the power of a single carrier.

$$V_{IP} = \sqrt{\frac{4a_1}{3a_3}} \quad (3.51)$$

$$IMR_3 = \frac{P_{\text{outT}}}{P_d} = 2(IP_3 - P_{\text{outT}}) + 6 \text{ dBc} \quad (3.52)$$

$$IP_3 = P_{\text{outS}} + \frac{(P_{\text{outS}} - P_d)}{2} \quad (3.53)$$

In modern applications where the signals are digitally modulated, other specification parameters are used. Adjacent channel power ratio (ACPR) is a measure of how much energy is produced outside of a desired band, which could result in interferences in adjacent channels of a multichannel communication system. This parameter refers to the illustration in Figure 3.17. It represents the spectrum of a multitone signal contained within the band  $2f_m$ , where  $f_m$  defines the baseband maximum frequency. The ACPR parameter, expressed in dBc, specifies the ratio between the total integrated power adjacent to the signal band and the total power contained within the signal band. Details about these parameters are found in [9].

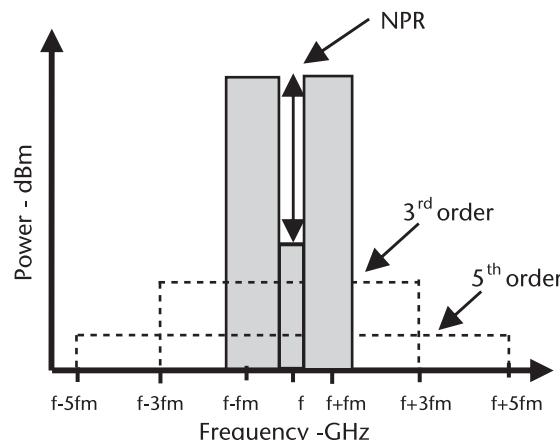


**Figure 3.17** Determination of ACPR. (After: [9].)

An additional mark that is more representative of linearity for a multicarrier system is the noise power ratio (NPR), shown in Figure 3.18. NPR represents the ratio between the in-band distortion and useful spectral densities when an in-band notch is created in the spectrum. The spectrum resembles that of a conventional DSB signal with a suppressed carrier.

Fortunately, one can still use the two-tone intermodulation parameters to estimate the ACPR [8]. For example, the ACPR can be estimated by (3.54), where one can use the  $IM_3$  level or the  $IP_3$  and  $P_{outT}$  values [8]. The parameter  $C_n$  is a correction factor related to the number  $n$  of subcarriers in the digital modulation, as defined by (3.55).

$$ACPR_{dBc} = \frac{P_{outT}}{P_d} = IM_3 + C_n = 2(IP_3 - P_{outT}) + 6 + C_n \quad (3.54)$$



**Figure 3.18** Determination of NPR. (After: [9].)

$$C_n = 10 \log \left( \frac{n^3}{16N_4 + 4M_4} \right)$$

$$\text{with } N_4 = \frac{2n^3 - 3n^2 - 2n}{24}, \quad M_4 = \frac{n^2}{4} \quad (3.55)$$

where  $n$  is the number of subcarriers in the signal and is an integer and multiple of 2.

The parameter  $C_n$  for a number of carriers equal or greater than 100 becomes equal to  $-1.2$  dB. If the number of carriers is lower, say, 50, this number increases to  $-2.9$  dB. Thus, ACPR is equal to two times the rejection of the third-order products plus  $4.8$  dB in the best case.

From the same reference, we find the relation between NPR and the  $IMR_3$ , given by (3.56).

$$NPR_{dBc} = \frac{P_{outT}}{P_d} = IM_3 - 6 + C_m = 2(IP_3 - P_{outT}) - 6 + C_m$$

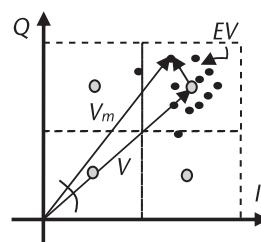
$$C_m = 10 \log \left( \frac{n^2}{4N_2 + M_2} \right) = -1.6 \text{ dB} \quad (3.56)$$

with  $M_2 = (n - 2)/2$  and  $N_2 = 3,577$ . The  $N_2$  value is fairly constant for  $n > 20$ .

The EVM is defined as the root-mean-square sum of the differences between measured and ideal symbols, as represented in (3.57), over a window of  $M$  symbols. A view of how the vectors are added in the I/Q plane is illustrated in Figure 3.19. In terms of power, EVM is defined by (3.58), which is the ratio of the average power vector error ( $P_{error}$ ) to the average ideal vector power ( $P_{ideal}$ ). The relation between the power and voltage definitions is given by (3.59).

This is a parameter about which both power and low noise amplifier designers are concerned. At lower levels, the EVM is degraded by the LNA noise figure and at high power levels it is degraded by the linearity of power amplifiers.

$$EVM (\%) = \sqrt{\frac{\sum_{n=1}^M |V_m - V_n|^2}{\sum_{n=1}^M |V_n|^2}} \quad (3.57)$$



**Figure 3.19** Representation of the EVM vectors for a 16QAM modulation system.

$$EVM \text{ (dB)} = 10 \log \left( \frac{P_{\text{error}}}{P_{\text{ideal}}} \right) \quad (3.58)$$

$$EVM \text{ (\%)} = 100 \left( 10^{\frac{EVM \text{ (dB)}}{20}} \right) \quad (3.59)$$

The EVM(dB) is also related to the  $IP_3$  by means of (3.60) found in [10].  $C_k$  refers to a constant ranging from 0 to 3 dependent on the type of modulation.

$$EVM = 2(P_{\text{out}T} - IP_3) + C_k \quad (3.60)$$

Thus, known procedures for improving  $IM_3$  can be simulated with a nonlinear model. Additional relevant parameters in the design of amplifiers for digital applications are found in [11]. These expressions are more accurate if the power level of fifth order is lower than the third order.

### 3.4 Low-Frequency Simulations

The objective of this section is to verify, through simulation, the operation of the amplifiers in classes A, B, and AB using the schematic shown in Figure 3.20. A unit cell measuring  $8 \times 75 \mu\text{m}$  was selected for this example. The nonlinear model EEHEMT was scaled from the  $4 \times 25 \mu\text{m}$  model presented in Chapter 2. In order to verify the theory presented so far, the frequency of operation was selected as 800

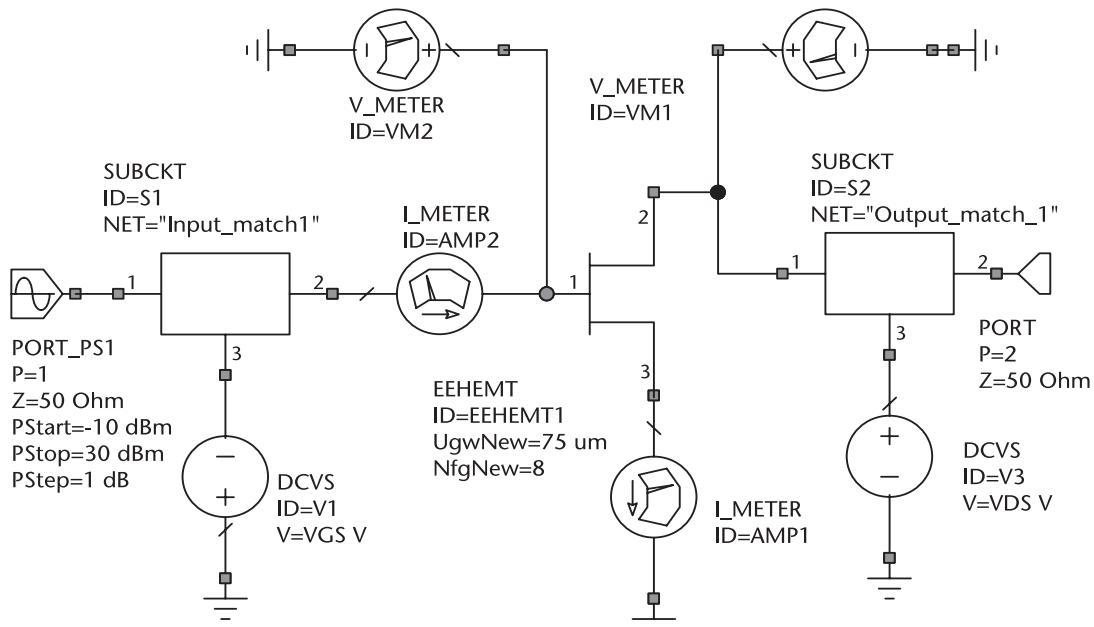


Figure 3.20 Schematic of an amplifier matched with lumped elements.

MHz. At low frequencies, the device reactance can be disregarded, so the model is nearly a DC model. In other words, the generator voltage is applied to the gate and the waveforms at the ports are similar to the waveforms at the intrinsic gate and drain nodes.

The load is obtained from (3.7) for  $V_{DQ} = 12V$ ,  $V_k = 1.7V$ ,  $V_T = -3.1V$ , and  $I_{D\text{MAX}} = 900 \text{ mA}$ . Assuming that the peak current is 10% lower than  $I_{D\text{MAX}}$ , due to GaN effects, the load results in  $R_L = 25.5\Omega$ , rounded to 30. The gate is biased at  $V_{GS} = -1V$  for class A, at  $V_{GS} = -1.75V$  for class AB, close to the device maximum transconductance, and at  $V_{GS} = -2.9V$  for class B.

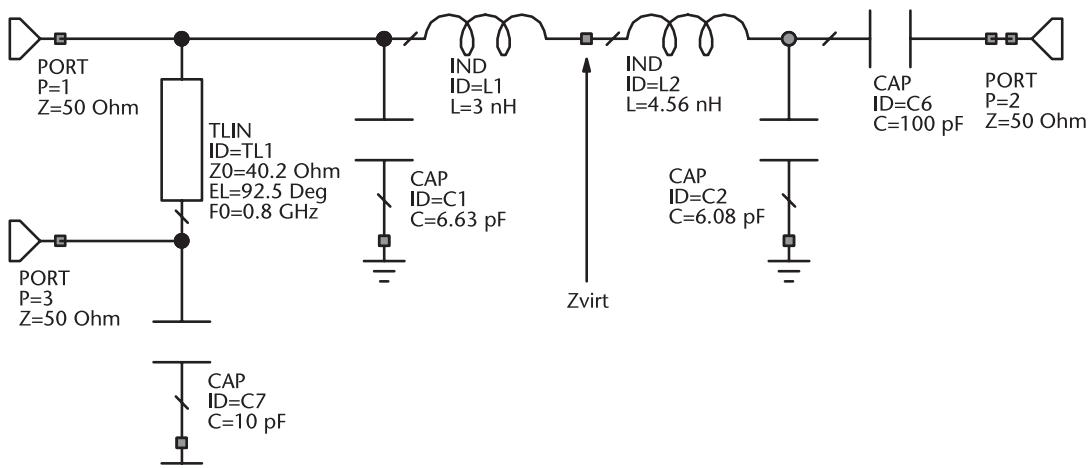
The output circuit was designed after [12], where a dual L-section back-to-back makes a PI-section, as shown in Figure 3.21. The proposal is to shunt the load impedance  $R_L$  with a reactance equal to  $-jR_L$ . The virtual impedance is then given by (3.61).

$$Z_{\text{virt}} = \frac{R_L}{1 + (\omega R_L C_1)^2} - \frac{j\omega R_L^2 C_1}{1 + (\omega R_L C_1)^2} + jX_L \quad (3.61)$$

This choice of impedance, that is,  $\omega C_1 = 1/(\omega R_L)$ , makes the virtual impedance about half the load impedance,  $Z_{\text{virt}} = R_L/2 - jR_L/2$ . The second L-section then transforms  $Z_{\text{virt}}$  to  $50\Omega$ . The high capacitance close to the load provides an additional second-harmonic rejection. The second-harmonic amplitude generated by a class B amplifier is about half the fundamental amplitude. Adding the matching network rejection, the total second-harmonic reduction adds up to more than four times.

The capacitive reactance of the first shunt reactance is then equal to  $-j30$ . The virtual impedance is  $Z_L/2$ , which means that the first section reduces the load value to  $15\Omega$  and the second section raises the impedance to  $50\Omega$ .

The gate matching started with stability considerations. As this is a millimeter-wave device, operating at low microwave frequencies, the circuit is unstable and the input impedance is nearly an open circuit. One solution to stabilize the device is to introduce feedback. Another is to add an external capacitor in shunt with the gate

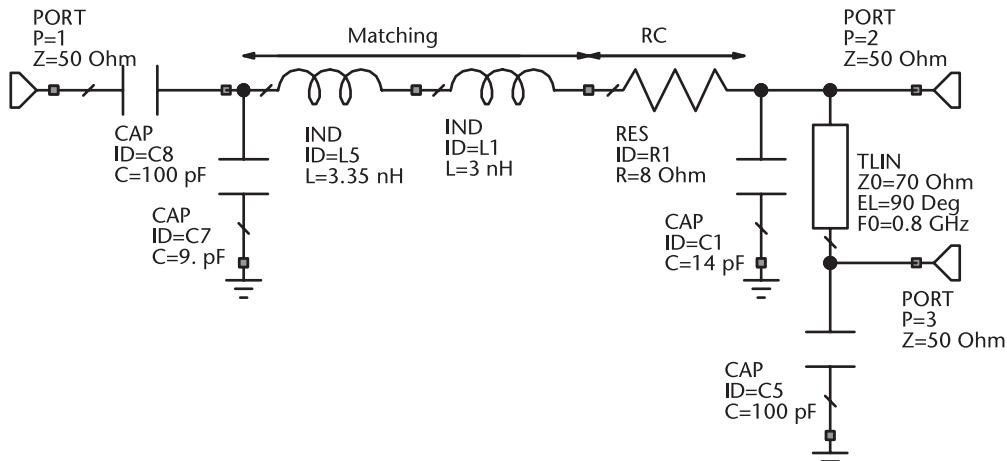


**Figure 3.21** Output match 1 with PI-section constructed from two back-to-back L-sections.

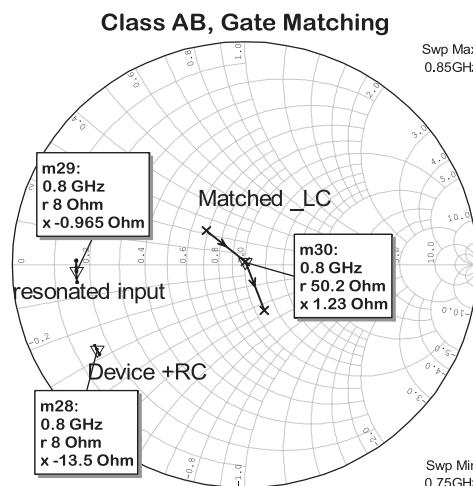
and a resistor in series to the gate circuit. This gives stability to the circuit, makes the gain more linear, and does not affect output power. Drain efficiency is also not affected, but the PAE will be reduced.

The gate-matching circuit is depicted in Figure 3.22, containing the stabilizing RC circuit, on the gate side. The resulting gate impedance and the RC network, the impedance of the resonated gate and the input impedance after matching, are represented in the Smith chart of the same figure.

A series inductance is used then to resonate the gate impedance to  $8\Omega$ . The transformation to  $50\Omega$  is achieved by using a single L-match. There was no circuit adjustment to improve the results. The shunt quarter-wave transmission line is used



(a)



(b)

**Figure 3.22** Schematic of input match 1, single L-match with a series resonator, and RC prematch: (a) circuit schematic, and (b) impedance on the Smith chart.

to bias the gate and is grounded by a 5-pF capacitor to ground. The series capacitance of 100 pF is used for blocking the DC.

The amplifier simulation for the device biased in class A is shown in Figure 3.23, showing a gain slope function of increase in power. The  $P_{1\text{dB}}$ , defined as the gain with power compressed by 1 dB, shows a value of  $P_{1\text{dB}} = 31.5 \text{ dBm}$ . The maximum power,  $P_{\text{sat}}$ , is defined for a gain compressed by more than 3 dB. The value in the figure,  $P_{\text{sat}} = 33.9 \text{ dBm}$ , is for a gain compressed by 6 dB. The drain efficiency at  $P_{\text{sat}}$  is near 70%, while the maximum PAE is equal to 62.7%. The comparison of gain for different classes of operation is shown in Figure 3.24. One can observe that the maximum power is obtained in class A, giving  $P_{1\text{dB}} = 33.3 \text{ dBm}$ , while the power at the maximum gain in class AB is  $P_{1\text{dB}} = 30.6 \text{ dBm}$ . Notice that the difference in gain between classes A and B is about 4 dB instead of the classical 6 dB. That is due to the I/V relation for this type of GaN device.

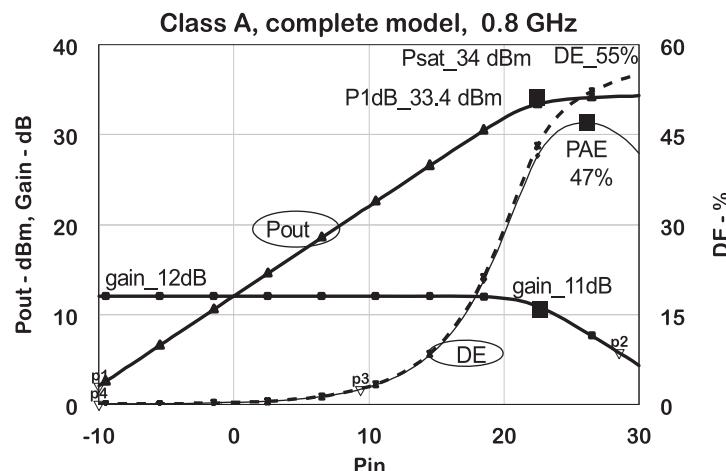


Figure 3.23 Class A power performance.

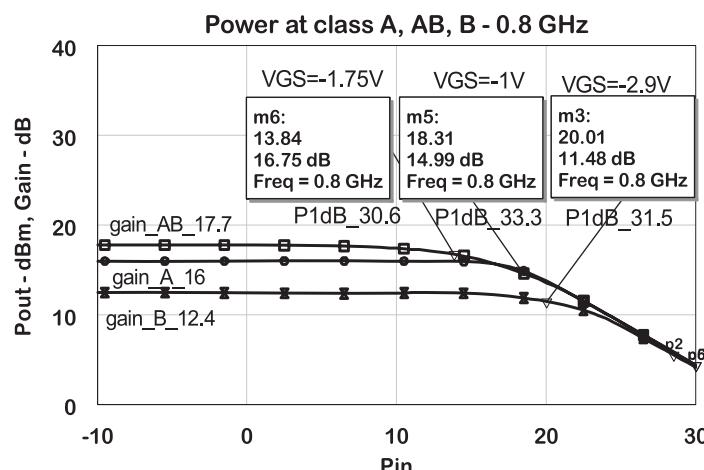


Figure 3.24 Gain for different classes of operation.

The maximum drain efficiency at a maximum drive level of 30 dBm, obtained with class B, represented in Figure 3.25, corresponds to 70%. That is a value 5% lower than the theoretical value. This simulation uses a complete EEHEMT for its evaluations. The curves in Figure 3.26 show the simulation results by making the knee voltage equal to 0 and for a 0 output conductance. The drain efficiency increases to 75.8%, which is the theoretical value. One can also observe in Figure 3.25 a nearly flat linear gain up to a 20-dBm drive level, showing good linearity performance in class B that is expected from an ideally rectified sinusoid.

Moving the gate bias from class B to class AB at  $V_{GS} = -2.25V$ , we obtain the typical power performance for this class, shown Figure 3.27. The input power is swept from  $-10$  to  $+30$  dBm. The maximum PAE of 59% occurs at an input power of 23 dBm, where an output power of 33.3 dBm is achieved. At this point, the gain is compressed by 5 dB, but still showing a value of 10 dB. The drain efficiency is

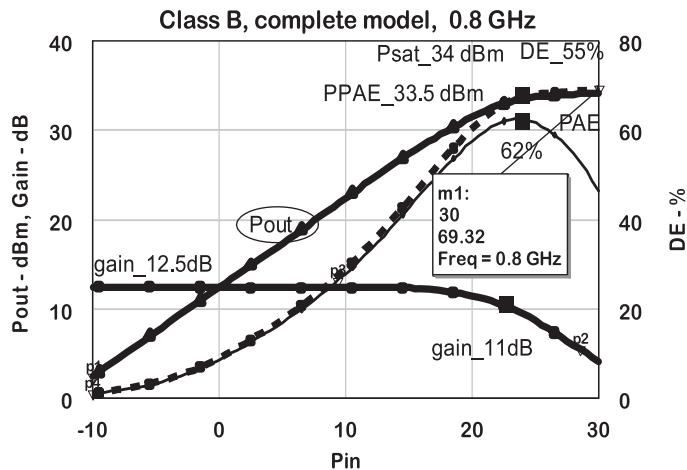


Figure 3.25 Class B power complete model.

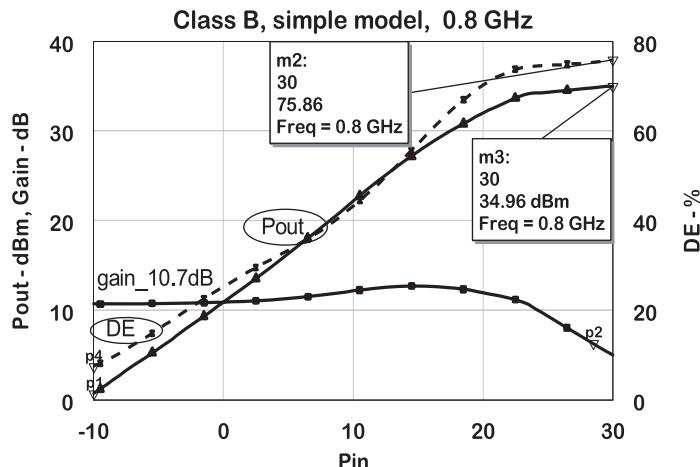


Figure 3.26 Class B simple model  $V_k = 0$ ,  $R_d = \infty$ .

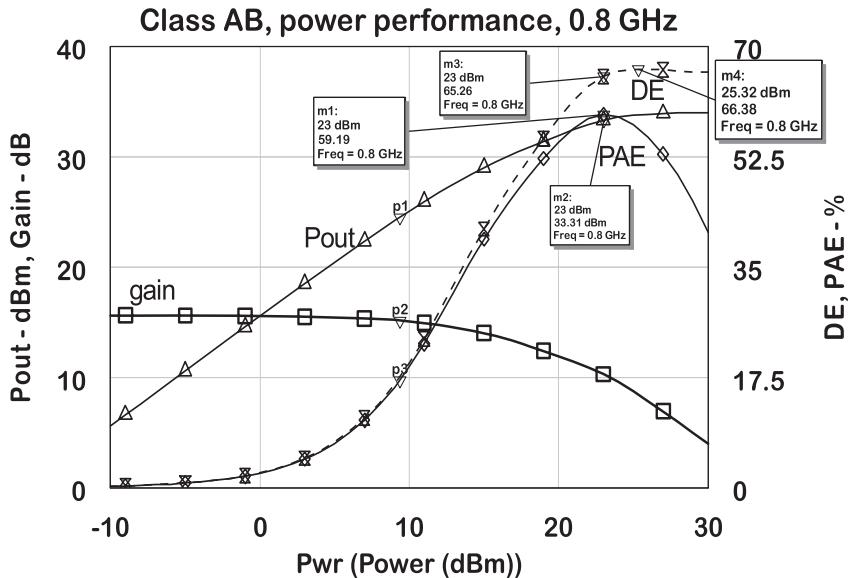


Figure 3.27 Class AB  $P_{out}$ , gain, PAE, and drain efficiency versus input power.

on top of the PAE until the gain becomes compressed. The PAE starts dropping following the gain compression, and the drain efficiency saturates around 66%.

The drain waveforms are presented in Figure 3.28. The current is a rectified sinusoid with a peak revealing third-harmonic content. The voltage is fairly sinusoidal, peaking near 24V.

To have a better insight into the device limitations, let us check the shape of I/V trajectory shown in Figure 3.29. The center path corresponds to the designed load ( $R_L = 30\Omega$ ), while the top path corresponds to a lower  $R_L$ , ( $R_L = 20\Omega$ ), and the bottom to a higher  $R_L$ , ( $R_L = 40\Omega$ ). The case of lower  $R_L$  shows higher  $V_{min}$  and higher RF current, peaking at 750 mA. The maximum value predicted of 900 mA is reached when the device is driven more into saturation. The case of higher  $R_L$  shows a decrease in the RF peak current and decrease in the  $V_{dmin}$  value.

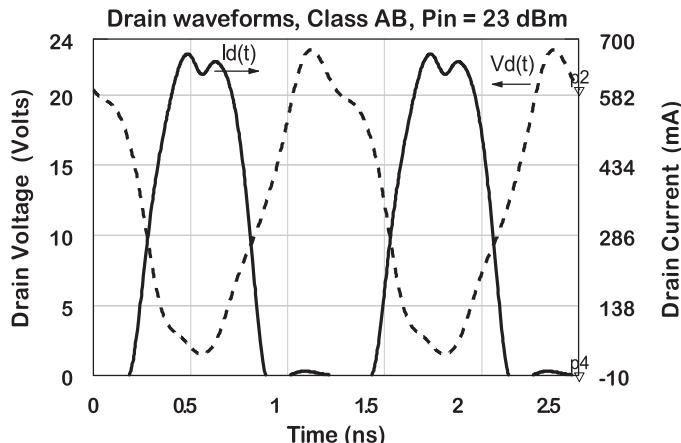


Figure 3.28 Class AB I/V drain waveforms.

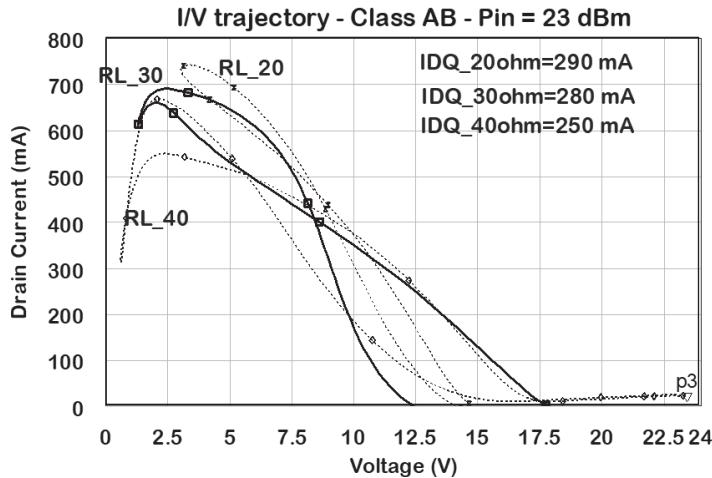


Figure 3.29 I/V trajectories for three distinct biases.

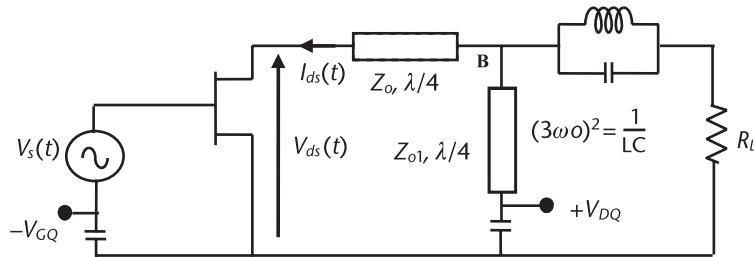
The maximum power and efficiency are achieved with  $R_L = 30\Omega$ . Lower impedance causes  $V_{min}$  increases; hence, RF voltage swing decreases, and RF current increases. The net effect is a lower power and efficiency. For higher resistance, one can see an increase in the RF voltage swing, since  $V_{min}$  is lower, while RF current decreases. The DC decreases even more. The net effect will be a lower power, but due to DC reduction, efficiency increases.

### 3.5 Class F Amplifiers

The concept of class F operation appeared in the late 1950s for vacuum tube applications [13] and later was applied to FETs [14]. The amplifier operation in class F consists in biasing the device in class B, with a specific harmonic load. The second harmonic is shorted to the ground and the third harmonic is terminated by an open circuit, to enhance a square-wave shape for the voltage. These terminations are created by the load schematic contained in Figure 3.30. At the fundamental frequency, the impedance at node B is  $50\Omega$ , because the LC circuit is assumed to be a short. The series quarter-wave line transforms the node impedance to the required load at the drain terminal. The impedance of the shunt stub at node B is an open circuit for the fundamental frequency. At the second harmonic, the shunt stub creates a short at this node, which the series line translates into a short at the drain terminal.

At the third harmonic, the shunt stub is an open circuit and the LC parallel resonant circuit is ideally an open circuit. The open circuit at node B is transformed into a short at the drain by the series transformer. The ideal drain voltage and current waveforms  $V_{ds}(t)$  and  $I_{ds}(t)$  are shown in Figure 3.31. The drain voltage shows no even harmonic components. The drain current is a half-wave sinusoidal, due to class B bias. There are no odd harmonic components in the drain current.

The fundamental components for the voltage in (3.62) and the current in (3.63) are determined from elementary Fourier analysis applied to these waveforms. The



**Figure 3.30** Electrical schematic for a class F operation.

load impedance at the fundamental frequency is obtained from the ratio between  $V_1$ ,  $I_1$ , taking into account the voltage limit  $V_k$ . The terminations at the second and third harmonics are determined from the class F definition as shown in (3.64). Using the impedance for class B, the fundamental impedance given by (3.64a–c) is equal to  $38\Omega$ .

$$V_1 = \frac{4V_{DQ}}{\pi} \quad (3.62)$$

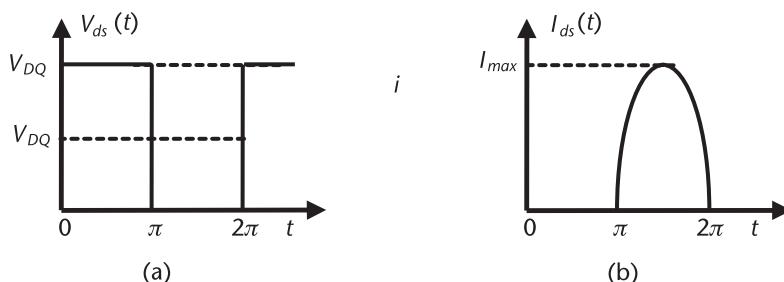
$$I_1 = \frac{I_{DMAX}}{2} \quad (3.63)$$

$$Z_{L1} = \frac{8}{\pi} \frac{V_{DQ} - V_k}{I_{DMAX}} \quad (3.64a)$$

$$Z_{Ln} = 0, n = \text{even} \quad (3.64b)$$

$$Z_{Ln} = \infty, n = \text{odd} \quad (3.64c)$$

An improvement on this class of amplifier came from Raab [15], who proposed a circuit to flatten the drain voltages, improving its square-wave shape. Later, Cripps proposed generating a square wave by inserting a third-harmonic component at the fundamental [11]. The representation of this waveform was proposed for the drain voltage employing (3.65). The resulting waveform is shown in Figure 3.32.



**Figure 3.31** Class F waveforms: (a) ideal voltage, and (b) ideal current.

$$v_{ds}(t) = 1 - \frac{2}{\sqrt{3}} \sin(\theta) + \frac{1}{3\sqrt{3}} \sin(3\theta) \dots \quad (3.65)$$

Increasing the number of odd harmonics results in a waveform closer to a square shape. However, it is not practical to design circuits taking into consideration harmonics higher than third order. The drain current is assumed to be the same as class B, a rectified sinusoid. This waveform can be achieved by increasing the fundamental load resistance, and as the DC term remains unaffected, it delivers an efficiency increased by the same factor. The fundamental voltage component for this square waveform is then given by (3.66) and the fundamental impedance by (3.67). The fundamental impedances defined by (3.64) and (3.67) are close,  $38\Omega$  and  $34\Omega$ , respectively. The former is about 8% higher than the value provided by the latter. Based on these values, one can say that the fundamental impedance is 15% to 27% higher than class A.

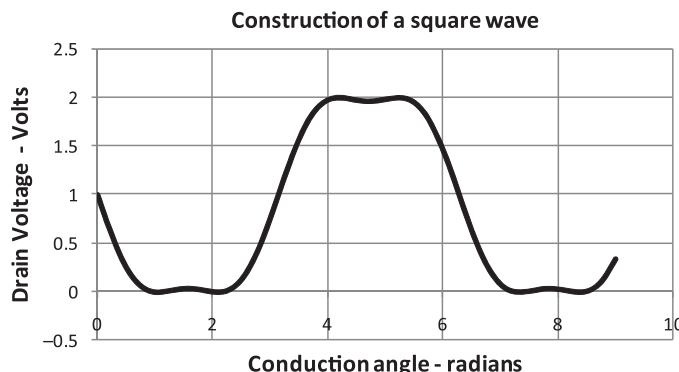
$$V_1 = \frac{2}{\sqrt{3}} (V_{DQ} - V_k) \quad (3.66)$$

$$Z_{L1} = \frac{4}{\sqrt{3}} \frac{V_{DQ} - V_k}{I_{D\text{MAX}}} \quad (3.67)$$

The output power compared to the class A power is in (3.68), showing a factor  $(2/\sqrt{3})$  greater. This amount corresponds to a 0.6-dB increase in power. The DC power remains the same as in class B; hence, the drain efficiency, according to (3.50), is 90.7%.

$$P_{RF} = \frac{2}{\sqrt{3}} \frac{V_{DQ} I_p}{2} = \frac{2}{\sqrt{3}} P_A \quad (3.68)$$

$$DE = \frac{\frac{2}{\sqrt{3}} \frac{V_{DQ} I_p}{2}}{\frac{V_{DQ} I_{DQ}}{2}} = \frac{\frac{V_{DQ} I_p}{\sqrt{3}}}{2\sqrt{3} \frac{V_{DQ} I_p}{\pi}} = \frac{\pi}{2\sqrt{3}} = 90.7\% \quad (3.69)$$



**Figure 3.32** Third-harmonic component squares for a sinusoidal waveform.

### 3.5.1 Class F Low-Frequency Simulations

The schematic shown in Figure 3.20 is also used to represent the simulations of a class F amplifier, by replacing the output match 1 and input match 1 circuit blocks by the corresponding circuits in Figures 3.33 and 3.35, respectively. A similar device size is used in the simulations. The gate is biased at  $V_{GQ} = -2.65V$ , slightly higher than  $V_T$ , to give gain under small-signal conditions. The operation is at the previously chosen frequency of 800 MHz.

The load resistance, predicted by (3.64), was used for this circuit at the fundamental frequency. The drain circuit in Figure 3.33 represents a simple topology with ideal transmission lines, which provide the desired harmonic terminations. The impedance at port 1 for this circuit is represented in Figure 3.34. The circuit is inserted in the output match block in Figure 3.20. The design started with two quarter-wave transformers, ( $TL_{64}$  and  $TL_{65}$ ), to determine the fundamental impedance. At the joining point between the two series lines, a shunt quarter-wave short stub was added, ( $TL_{80}$ ). That element imposes a second-harmonic short at the drain port. The shunt stub can be shorted through a capacitor to allow drain bias insertion at this point. The last element is a  $30^\circ$  line, ( $TL_{76}$ ), which shorts the third harmonic at the output port. That impedance is transferred to the drain terminal by the series transmission lines. The impedance at the drain port at fundamental harmonics frequency is in the Smith chart of Figure 3.34, comprising the load impedance in the frequency domain. In real circuits, the losses will affect these impedances. The series capacitor is used for DC blocking.

The circuit shown in Figure 3.35 is inserted in the input-match block. It uses the same RC stabilizing circuit as the previous design. The inductance, ( $L_1$ ), from right to left resonates with the gate impedance. The resulting resistive impedance is

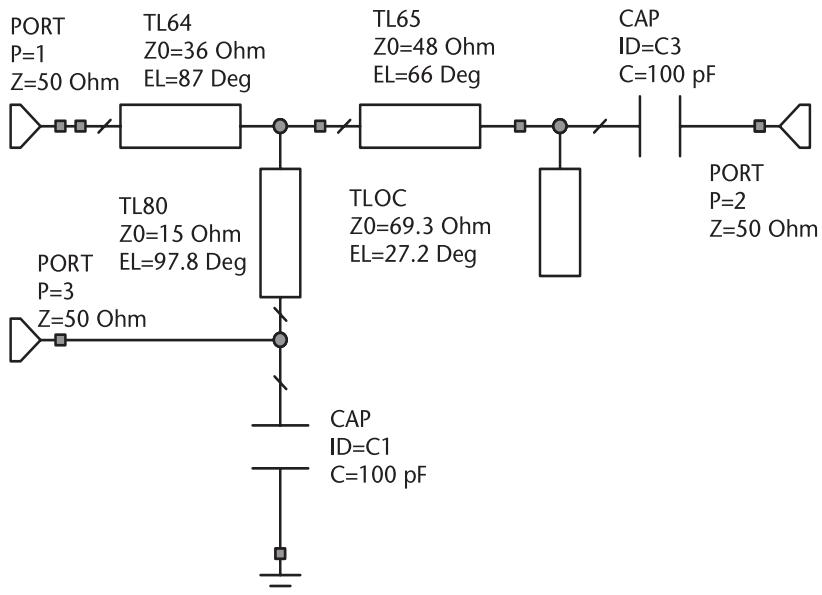


Figure 3.33 Class F harmonic load schematic.

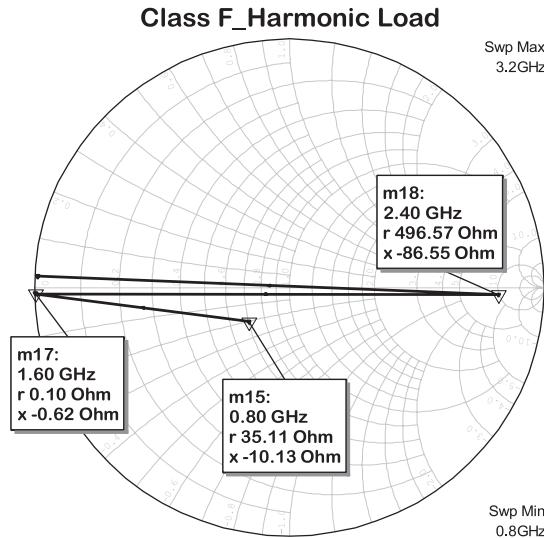


Figure 3.34 Class F harmonic impedance.

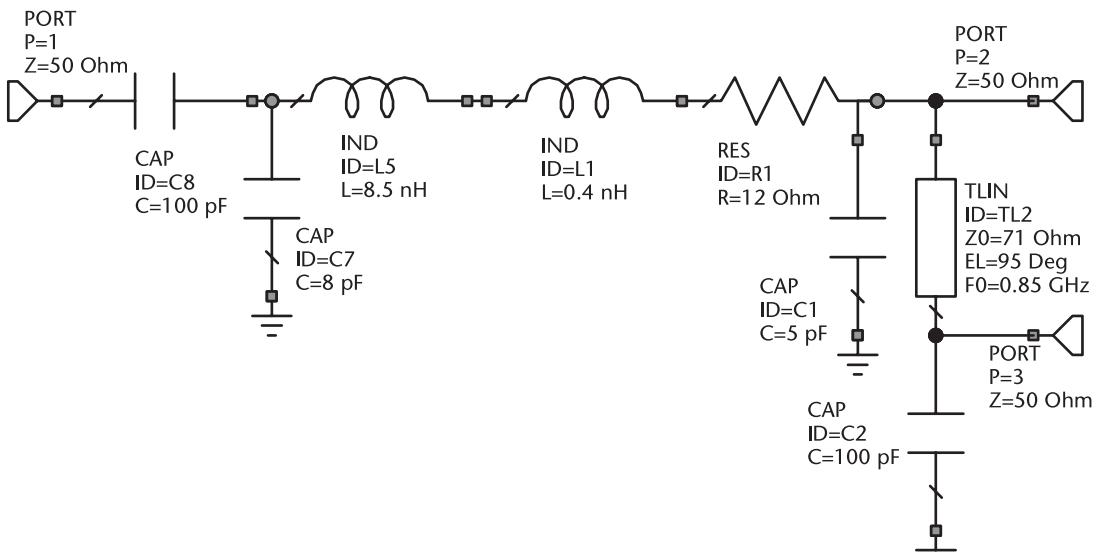


Figure 3.35 Schematic of input matching class F.

transformed to  $50\Omega$  by means of a single  $L$  lumped matching network ( $L_5-C_7$ ). The capacitor ( $C_8$ ) blocks the DC at the input port. The gate bias line ( $TL_2$ ) is a shunt stub measuring a quarter-wave at the fundamental frequency. This transmission line is transparent to the fundamental frequency and shorts the second harmonic. The  $S_{22}$  of this circuit at the fundamental and second harmonic frequency is depicted in the Smith chart of Figure 3.36.

The power performance for this amplifier is presented in Figure 3.37. The maximum PAE for the amplifier is 67% while the drain efficiency is 72%. The output

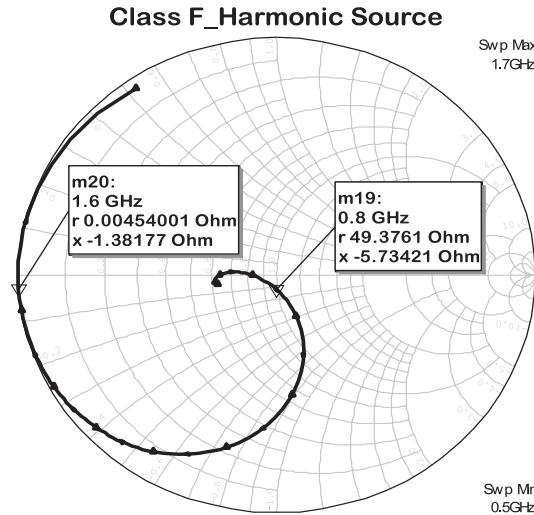


Figure 3.36 Class F input impedance.

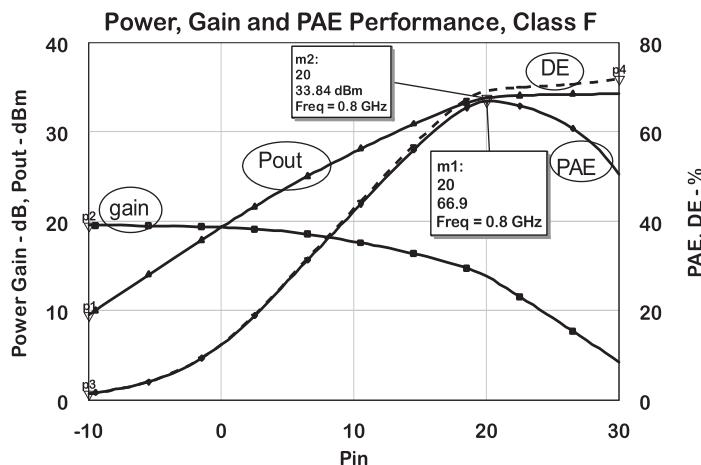


Figure 3.37 Class F  $P_{out}$ , gain, drain efficiency, and PAE versus input power.

power is 33.9 dBm, with the gain compressed by 4 dB. This amplifier shows a PAE that is 5% more efficient compared to Figure 3.25 for class B simulations. The power saturates at a level of  $P_{sat} = 34$  dBm.

Figure 3.38 shows the class F drain waveforms. The drain current is nearly a half-sinusoid and the voltage is quite squared, showing strong class F waveforms. The I/V trajectory is shown in Figure 3.39, describing the load impedance in the time domain. Between  $V_{DS} = 2V$  and  $V_{DS} = 17V$ , the shape is close to a conventional load line. The high-voltage area is a region of zero current, while at lower voltage the current peaks to 700 mA, for an input drive of 22 dBm. The minimum voltage

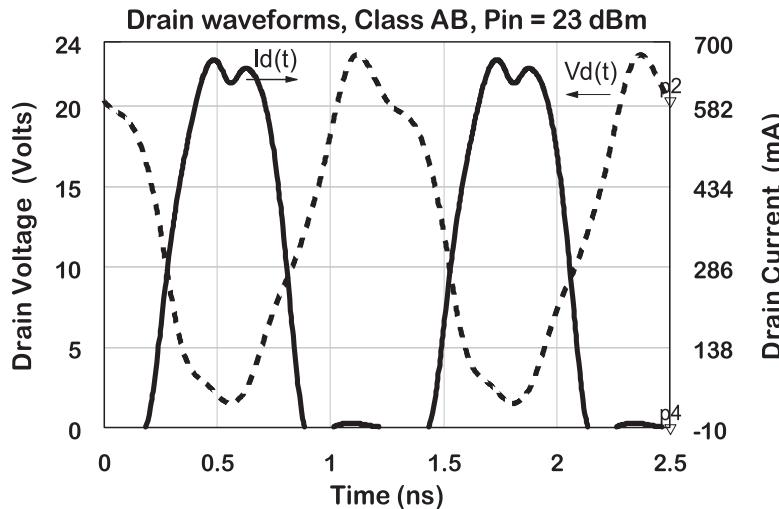


Figure 3.38 Class F drain waveforms.

of 1.1V is lower than  $V_T$ . This I/V trajectory corresponds to class F waveforms, high voltage with low current and low voltage with high current, with a transition zone in between.

The inclusion of the third harmonic brings a significant advantage: a reduction in negative swing of the drain-source voltage. This reduction allows an increase in the fundamental voltage component to occur while keeping the drain-source voltage always positive.

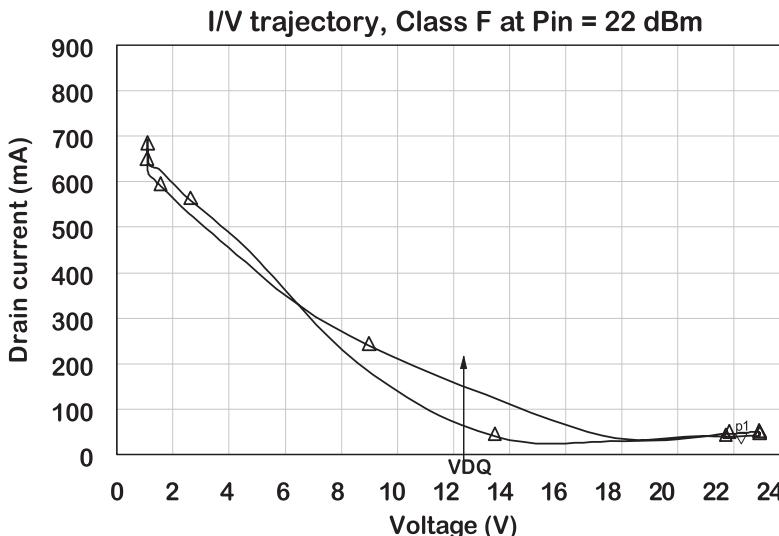


Figure 3.39 Class F I/V trajectory.

### 3.5.2 Class F Large Band

The previous circuit was designed at a spot frequency and will perform in a narrow band, around 2%. Before discussing large-band class F design, let us first verify the bandwidth limitation constraints [16]. The impedance at the fundamental frequency will overlap with the harmonic impedance, restricting the bandwidth. According to (3.70), we can verify the bandwidth as a function of harmonics. Let us consider only the fundamental and second harmonic,  $n = 1$ , and the maximum fractional bandwidth  $\Delta f/f_c$  becomes 66%. If the third harmonic is considered,  $n = 2$ , then the maximum bandwidth is reduced to 40% and to 28.6% in the case of  $n = 3$ . This limitation assumes ideal filters with sharp bandwidth rejection. In practice, the bandwidth limitation is narrower.

$$n\left(f_c + \frac{\Delta f}{2}\right) = (n+1)\left(f_c - \frac{\Delta f}{2}\right) \quad n = 1, 2, 3 \quad (3.70)$$

Classical class F amplifiers show narrowband performance, for the performance is obtained at precise impedance terminations, which is not simple to control even at low frequencies. To overcome this limitation problem, the continuous class F was proposed [17, 18], with a method to enhance the bandwidth and to synthesize the matching networks. In this book, instead of following that academic approach, we follow the simplified methodology proposed by Merrick et al. [16], consisting of simply using the optimizer to synthesize the circuit for a large band in class F.

The large-band approach using computer optimization and tuning tools were applied to the circuit of Figures 3.33 and 3.35. The target performance goals are:

1. The bandwidth for the fundamental and third harmonic considering a center frequency of 800 MHz is limited to operate between 686 and 914 MHz.
2. The minimum output power is  $P_{out} = 33$  dBm, for an input drive of 22 dBm, based on the results of Figure 3.37.
3. The efficiency goal was a PAE of 60% corresponding to 6 points below the value in Figure 3.37. It is also desirable to have a small-signal gain of 15 dB and an input return loss of 10 dB.

The topology for the output circuit is the same as that used in Figure 3.33, with the optimized values in Table 3.1. The input match uses the same RC circuit, followed by a highpass/lowpass matching prototype. The circuit schematic and values are shown in Figure 3.40.

**Table 3.1** Output-Match 1, Class F, Large Band

Output Match			
$Z_{out1}$ ( $\Omega$ )	25.38	$\Theta_{in1}$ ( $^\circ$ )	86.83
$Z_{out2}$ ( $\Omega$ )	34.39	$\Theta_{in2}$ ( $^\circ$ )	53
$Z_{out3}$ ( $\Omega$ )	15.01	$\Theta_{in3}$ ( $^\circ$ )	96.19
$Z_{out4}$ ( $\Omega$ )	32.2	$\Theta_{in4}$ ( $^\circ$ )	25.18

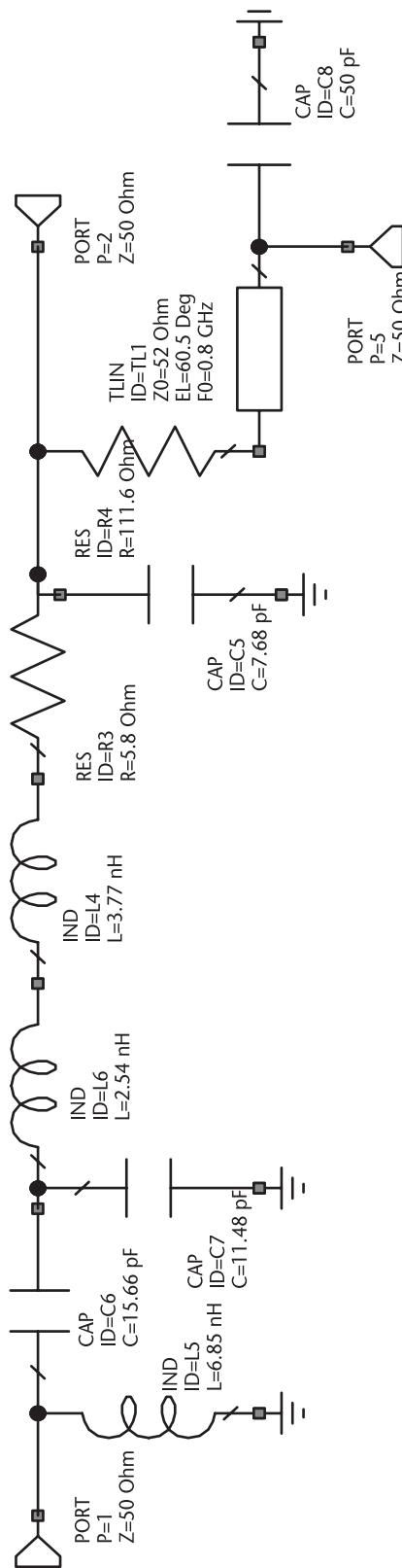


Figure 3.40 Input-match 1 circuit schematic with parameter values.

A resistor in series with a short stub was used in the gate bias line, with the objective of improving gain flatness and stability. The circuit was simultaneously optimized for the linear and nonlinear models. Therefore, two test benches were built, one for each model, with the same matching circuits. The linear simulation gives a more correct evaluation of a small-signal performance. The results are plotted in Figure 3.41, achieving a small-signal gain of 16 dB with less than 1-dB variation in the band. The input return loss is better than 10 dB. The nonlinear simulation, shown in Figure 3.42, gives a minimum output power of 33 dBm and a minimum PAE of 60%. The gain is 12.5 dB, compressed by 5.5 dB using, as reference, the linear gain.

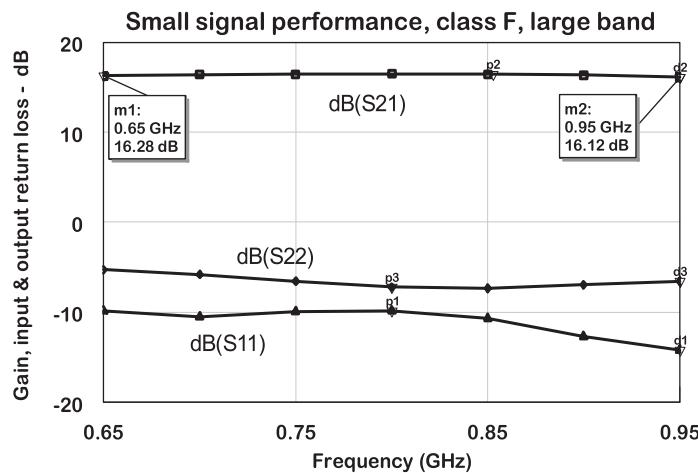


Figure 3.41 Small-signal class F performance.

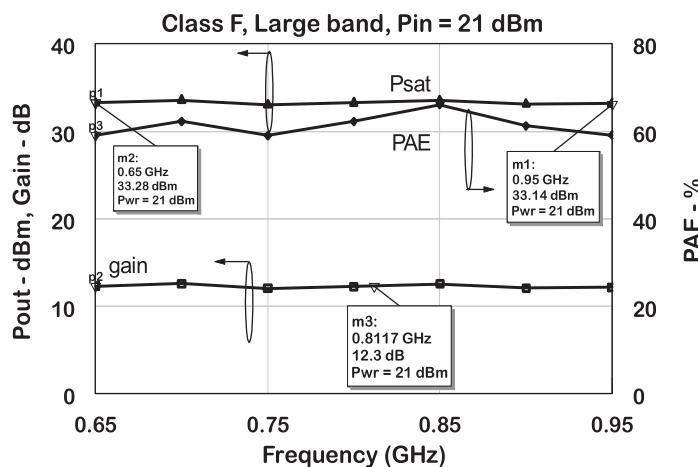


Figure 3.42 Large-signal class F performance.

### 3.6 Inverse Class F Amplifiers

By duality, an inverse class F has been proposed, where the roles of the current and voltage are interchanged, as shown in Figure 3.43. The harmonic terminations are the complement, that is, the second harmonic is ideally terminated by an open circuit and the third harmonic is shorted. For better operation in inverse class F, it has been proposed to bias the gate more into class A than class B [18]. That will minimize the amount of clipping in the current, improving the symmetry of the waveform.

The half-sinusoid shape of voltage is obtained due to voltage swing in the passive region and in the current cutoff region. The load impedance for the  $F^{-1}$  mode based on these waveforms is quite different from class F. Let us start with the definition of fundamental current and voltage, (3.71) and (3.72).

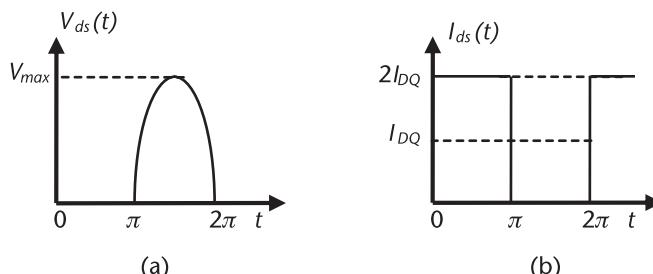
Let us also replace  $V_{DQ}$  with  $2(V_{DQ} - V_k)$ , defining the impedance as a function of parameters, (3.73). Comparing this with the impedance of class F, (3.64), it is interesting to note that the impedance in the inverse class F is 36% higher. The waveforms in Figure 3.43 are ideal in the respect that a large number of harmonics are assumed. In real circuits, only a few harmonics are considered, causing distortion in relation to the ideal waveforms.

$$V_1 = \frac{V_{MAX} - V_k}{2} \quad (3.71)$$

$$I_1 = \frac{2I_{DQ}}{\pi} \quad (3.72)$$

$$\begin{aligned} Z_{L1} &= \frac{\pi}{4} \frac{V_{MAX} - V_k}{I_{DQ}} = \frac{\pi}{2} \frac{2(V_{DQ} - V_k)}{I_{DQ}} = \frac{\pi}{2} R_{LA} \\ Z_{Ln} &= \infty, n = \text{even} \\ Z_{Ln} &= 0, n = \text{odd} \end{aligned} \quad (3.73)$$

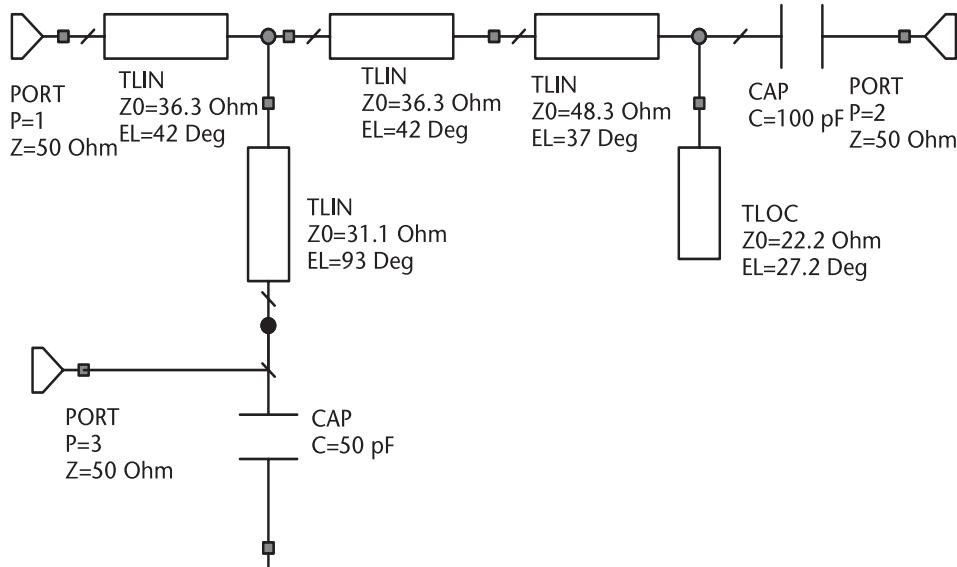
To build the harmonic load, we start from Figure 3.33 and break the first quarter-wave transformer from left to right in a cascade of two 1/8-wavelength-long transformer,  $45^\circ$ , and move the quarter-wave short shunt stub to that joining point. The fundamental impedance is still given by the cascade of two  $90^\circ$  lines. The second-harmonic impedance at the input port is open, caused by the shunt stub



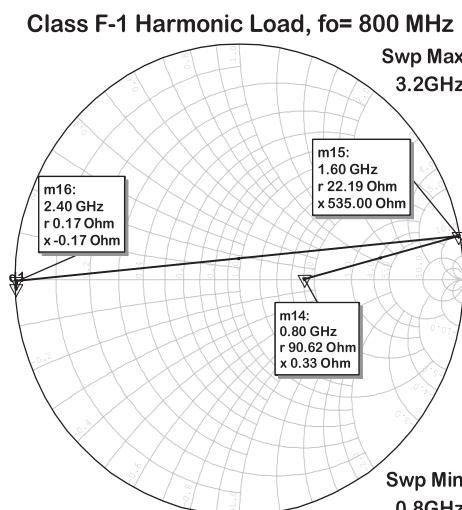
**Figure 3.43** Class  $F^{-1}$  ideal waveforms: (a) ideal voltage, and (b) ideal current.

short circuit and the  $90^\circ$  phase shift introduced by the series line. The shorted third harmonic is controlled by the open shunt stub with an electrical length of  $30^\circ$  at the fundamental frequency.

The fundamental load impedance calculated using (3.73) is near  $50\Omega$ . This value was used to calculate the initial values for the circuit indicated in Figure 3.44. The corresponding impedance of this circuit is in the Smith chart in Figure 3.45. The terminations for two harmonic frequencies are also shown. The fourth-harmonic contribution can be disregarded. The device was biased at  $V_{GQ} = -1.75V$ .



**Figure 3.44** Schematic of the load circuit class  $F^{-1}$ : (a) matching at  $f_0 = 75$  GHz, and (b) impedance presentation.



**Figure 3.45** Impedance in the Smith chart.

The gate matching network is similar to the one shown in Figure 3.35. The power simulation gives a PAE of 63.3% at an output power of 33.7 dBm. The compressed gain is 10.7 dB, down 6.6 dB from the linear gain. The performance in Figure 3.46 is, in general, comparable to the class F amplifier shown in Figure 3.37. The drain efficiency at this level is just a few points above PAE.

The waveforms in Figure 3.47 show an approximate square shape for the current as expected in spite of the dominant third-harmonic effect on the positive peak. These can be controlled by tuning the harmonics. The circuit was primarily adjusted for power and with PAE as a second priority. The voltage resembles a rectified sinusoid. The I/V trajectory can be seen in Figure 3.48, showing a shape similar to class B trajectory. It can be noticed that bias voltage goes beyond the maximum of 24V due to the class A-type bias.

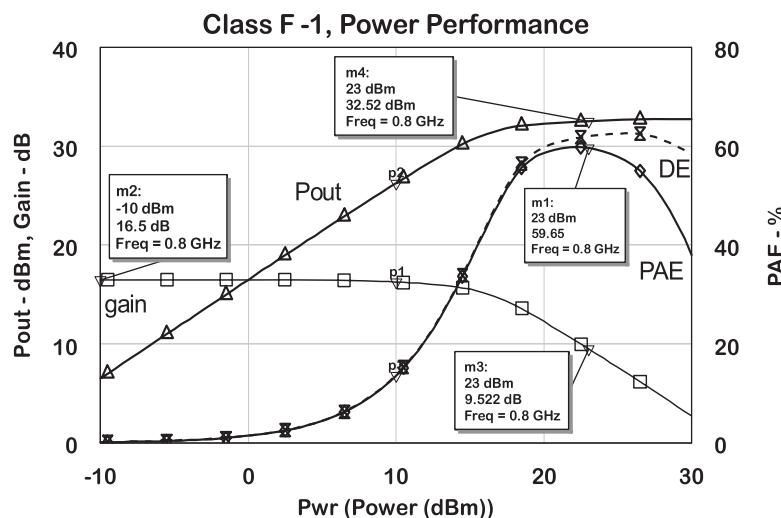


Figure 3.46 Performance of  $F^{-1}$  amplifier at 800 MHz, biased at  $V_{GQ} = -1.75V$ .

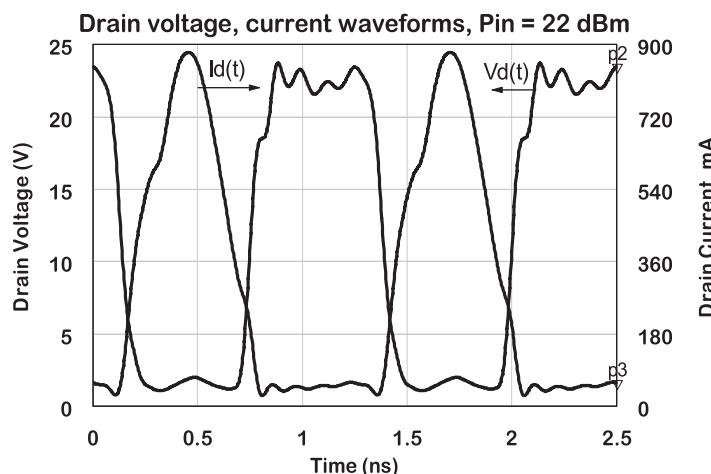
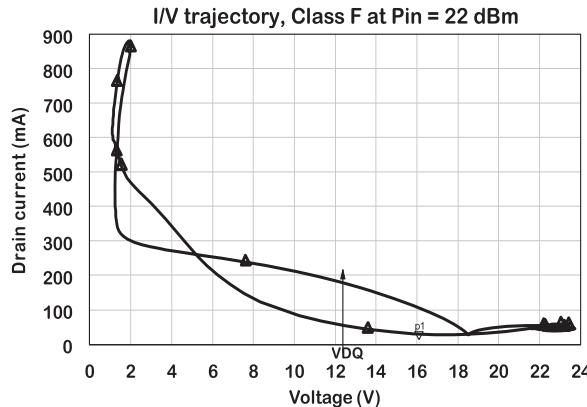


Figure 3.47 Class  $F^{-1}$  drain waveforms.



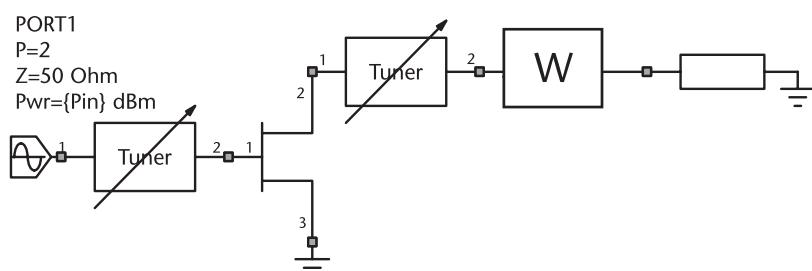
**Figure 3.48** Class F<sup>-1</sup> trajectory I/V limits.

## 3.7 Millimeter-Wave Amplifiers

The objective of this section is to verify the properties of the amplifiers discussed in the previous sections, at millimeter-wave frequencies. The waveforms at the drain port of power devices are different than the ones presented to the internal current source nodes. Thus, one cannot expect same performances from low-frequency analysis. This effect precludes the application of waveform engineering to improve efficiency at high millimeter-wave frequencies with the present GaN devices. Actually, at these frequencies, there is a difficulty to distinguish between class F, inverse class F, and class B based only on the drain waveforms.

### 3.7.1 Load-Pull Process

This process represents the evolution of the manual impedance determination method, carried out on a test bench represented in Figure 3.49. This simplified circuit contains at the device input and output a circuit block called a tuner. They provide a wide range of impedances nearly covering the Smith chart by adjusting variable impedance transformers. The generator applies power to the input tuner that feeds the gate of the test FET. The signal leaving the drain passes through the output tuner and reaches a power meter. After biasing the transistor, one can tune the output tuner for, say, the maximum output power and the input tuner for maximum gain. When the results of gain and power are satisfactory, the transistor is removed and the tuners are taken to a network analyzer for impedance measurement.



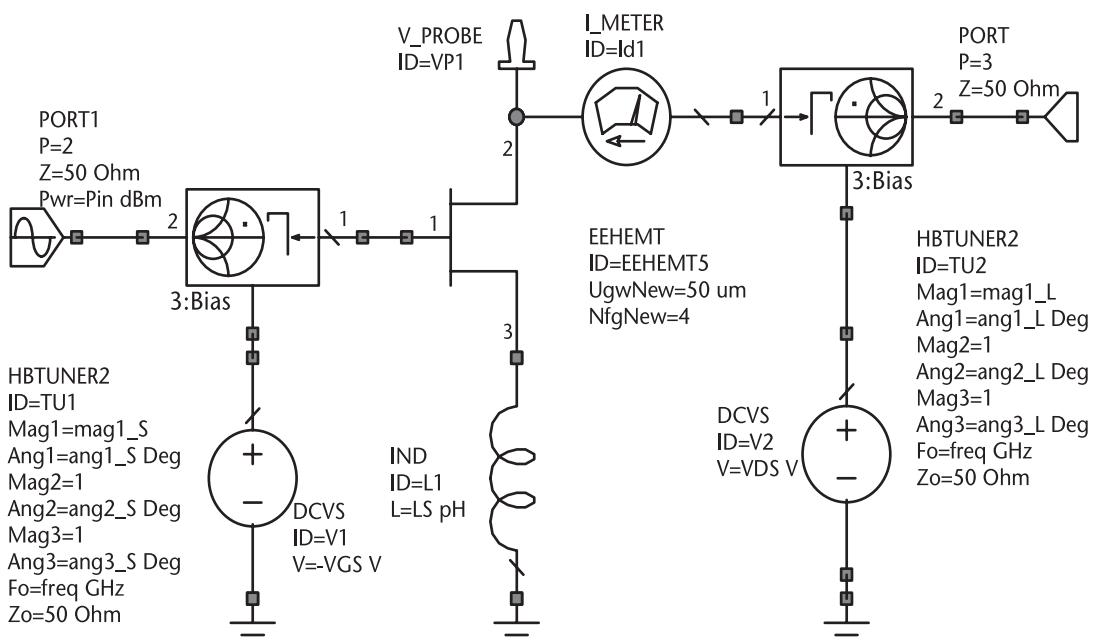
**Figure 3.49** Source and load impedances for power match.

All these operations have been automated into an automatic passive load-pull system. They are available from a number of companies. In the automated system, instead of tuning for optimizing a parameter, a certain number of impedance points are predefined on the Smith chart and the system calculates the performance at each one of these points. The software part of the system collects these data and transforms the results, by analytical means, in terms of contours of constant power, efficiency, or any parameter of interest. In general, the results are laid out on the Smith chart for both the output and input ports.

At millimeter-wave frequencies, the objective is to determine the terminations of unit cells on wafer. In a passive load-pull system, the connections and cables from the tip of the wafer probe to the tuner introduce losses that limit the maximum voltage standing wave ratio (VSWR) that can be presented to the test devices. In modern millimeter-wave systems, the tuners are small enough to be located close to the probe, greatly minimizing these losses. Unfortunately, the maximum VSWR can still be limited, say, corresponding to a reflection coefficient of 0.7. A low-cost solution to this problem is to use a prematching circuit that lowers the impedance level or increases the reflection coefficient at the device port. Harmonic load-pull is available in the market for frequencies up to Ka-band. The alternative to passive load-pull is the use of active load-pull systems [19].

### 3.7.2 Numerical Load-Pull

In lack of such a system, the designer option is to use a trustful nonlinear model for the device and perform a numerical load-pull. The concept used by the numerical load-pull and the hardware is the same. For instance, we can use the test bench in Figure 3.50 and let the load-pull controller calculate the performance to selected points on the Smith chart.



The software then calculates the desired contours and finds the center, giving the optimum output and input impedance for a giving target. The software can also find the effect of harmonics at the input and output of the device, which is convenient for class B, AB, and F.

### 3.7.3 Class AB: Load-Pull Results

A load-pull was performed on a  $4 \times 25 \mu\text{m}$  unit cell, biased at  $V_{GS} = -1.75\text{V}$  and  $V_{DS} = 12\text{V}$ , at two frequencies considered, 30 and 75 GHz. At 30 GHz, the drive power is 17 dBm, and at 75 GHz the drive is 20 dBm. The results are in Figure 3.51 at 30 GHz and in Figure 3.52 at 75 GHz. The solid lines correspond to power contours in 1-dB steps, while the dotted line corresponds to PAE in 5% steps. The optimum load corresponds to the center of the figure, so that at 30 GHz the load for power and efficiency is quite the same. At 75 GHz, the load for power is slightly lower than the load for efficiency.

The summary results expressing the load impedance in terms of an equivalent circuit are in Table 3.2 for two sizes of devices,  $4 \times 25 \mu\text{m}$  and  $4 \times 37.5 \mu\text{m}$ . The circuit assumes the second harmonic is short to ground at the drain and at the gate. One can observe in the results that the ratio of the load resistor for power and efficiency is quite close for both device sizes and frequencies.

### 3.7.4 Class F: Load-Pull Results

The same test bench in Figure 3.50 was applied to class F. The unit cell size is  $4 \times 50 \mu\text{m}$  and the evaluations were performed at 30 GHz. The magnitude of the harmonic reflection coefficients is kept at 1, while the phase is submitted to the optimization process. The device was biased at  $V_{GS} = -2.6\text{V}$  and a 20 pH was inserted in series

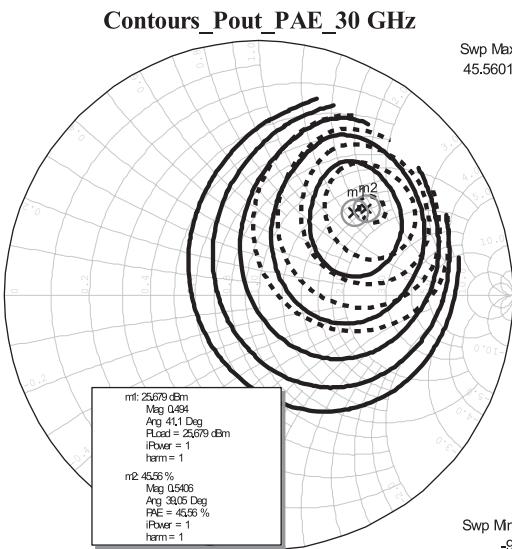


Figure 3.51  $P_{out}$ , PAE contours, 30 GHz.

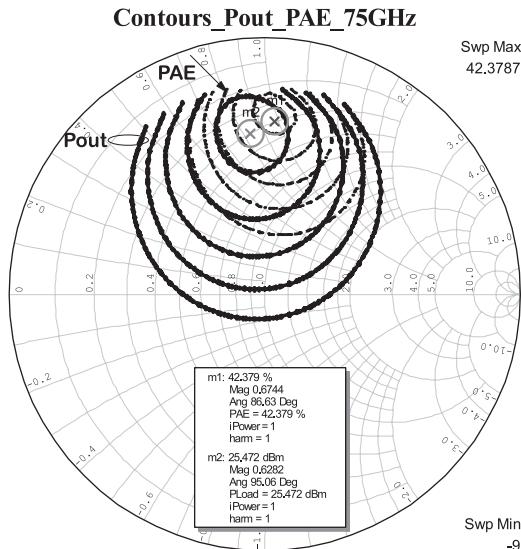


Figure 3.52  $P_{out}$ , PAE contours, 75 GHz.

**Table 3.2** Source and Load Reflection Coefficients

Frequency	Parameter	4 × 25 μm		4 × 37.5 μm	
		Power	Efficiency	Power	Efficiency
30 GHz	R <sub>Lout</sub> (Ω)	126	45%	88	102
	C <sub>out</sub> (fF)	33	33	58	53
	L <sub>out</sub> (pH)	12.17	12.17	8.12	8.12
75 GHz	R <sub>Lout</sub> (Ω)	132	160	86	100
	C <sub>out</sub> (fF)	39	37	60	60
	L <sub>out</sub> (pH)	12.17	12.17	8.12	8.12

with the source for stability. The summary of the RF parameters are in Table 3.3. The first three lines in the summary correspond to the circuit tuned for power and the last three lines correspond to the circuit tuned for efficiency.

One can observe the differences in load impedance compared to class B and the amount of efficiency obtained for the circuit tuned for efficiency at the cost of a 1-dB penalty on the output power.

In order to have a better insight into the operating conditions of the device, we investigated the difference in the impedance at the device ports and at the nodes of the internal current source for class F. To read this internal impedance, we replaced the nonlinear model by a modified linear model, shown in Figure 3.53. We suppressed the internal current source and the output conductance from the linear model.

Using a transformer connected as shown in Figure 3.54, we can look at the internal node and extract a qualitative behavior of the impedances at this terminal. The resulting impedance at the output port is shown in Figure 3.54 as dotted lines, indicating the fundamental impedance and the phases of the second and third harmonics. In the same figure, the solid lines indicate the impedance seen by the current source. It approximately follows the impedances for an inverse class F mode.

A further refinement in the optimization process can be made by sweeping one harmonic angle, keeping all the others fixed. In Figure 3.55, one can observe that the second harmonic angle can be anywhere between 80° and 100° with approximately constant power gain and efficiency. This information shows the design margin

**Table 3.3** Summary of Load-Pull for a 4 × 30-μm Device at 30 GHz

	Frequency GHz	R <sub>Lout</sub> Ω	C <sub>Lout</sub>	R <sub>gin</sub> Ω	C <sub>gin</sub>
P <sub>out</sub> 26.4 dBm	30	140	90 fF	9	250 fF
PAE 41%	60	0	j62	0	j1000
Gain 9.5 dB	90	0	j42	0	j70
P <sub>out</sub> 25.5 dBm	30	170	70 fF	9.6	300 fF
PAE 66%	60	0	j72	0	j0
Gain 9 dB	90	0	j22	0	j12

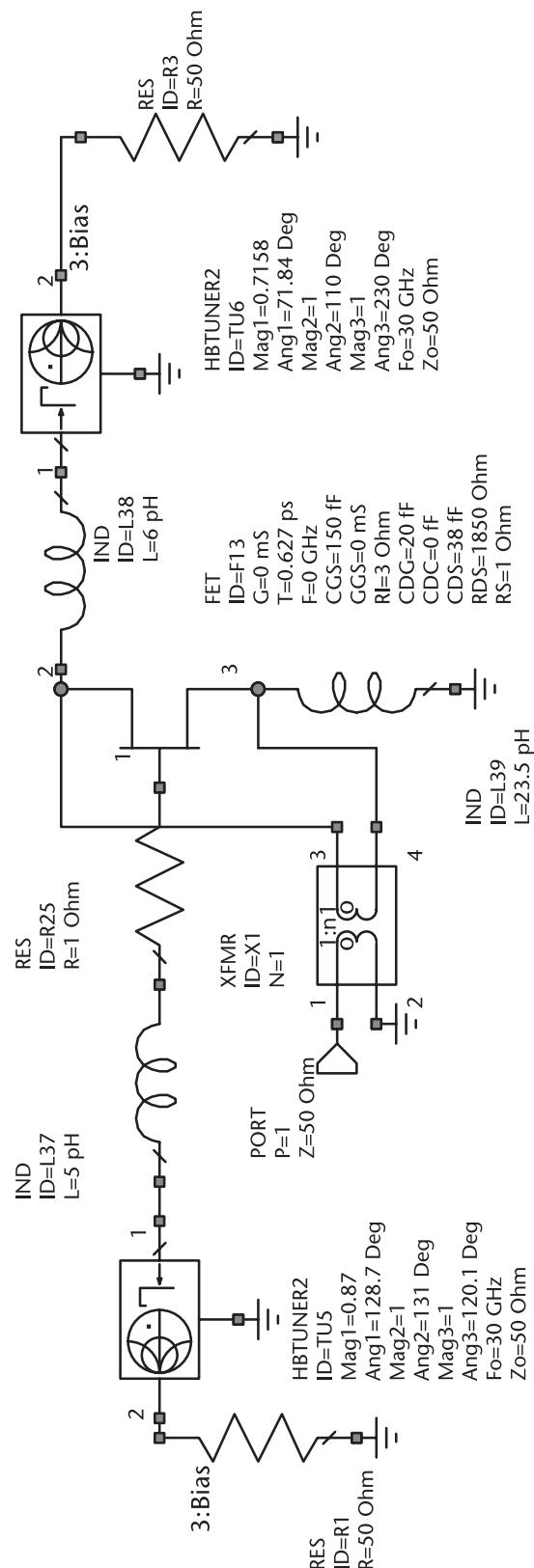
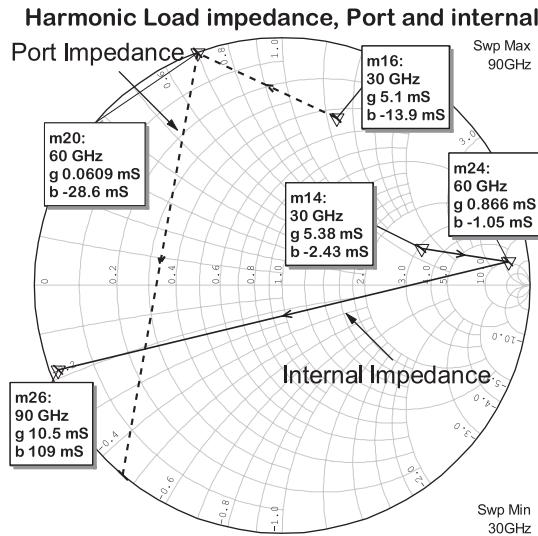


Figure 3.53 Angle rotation of impedance from the drain port to internal current source nodes.

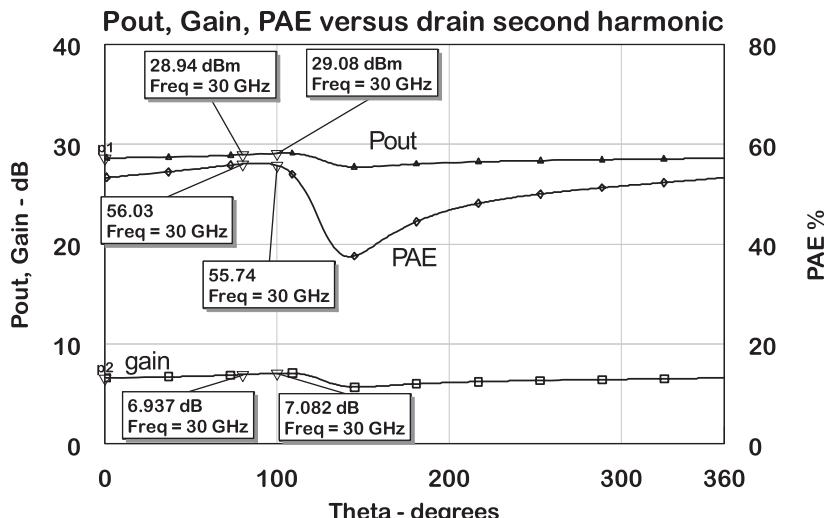


**Figure 3.54** External port and current source node impedances at the fundamental and harmonics.

for the second harmonic phase. This is very useful for the design of the harmonic matching network. A similar investigation can be made to each one of the source and load harmonics.

### 3.7.5 Class A-AB Millimeter-Wave Amplifier

The objective is to verify the performance of a class A and AB amplifier at 30 GHz. The circuit schematic is in Figure 3.56, and uses the same unit cell and device model shown in Figure 3.50. The circuit was matched using the impedance parameters from Table 3.2 with proper scaling of frequency and device size. The load was modified



**Figure 3.55** Effect of drain harmonics on power and efficiency. The third harmonic is fixed and the second is swept.

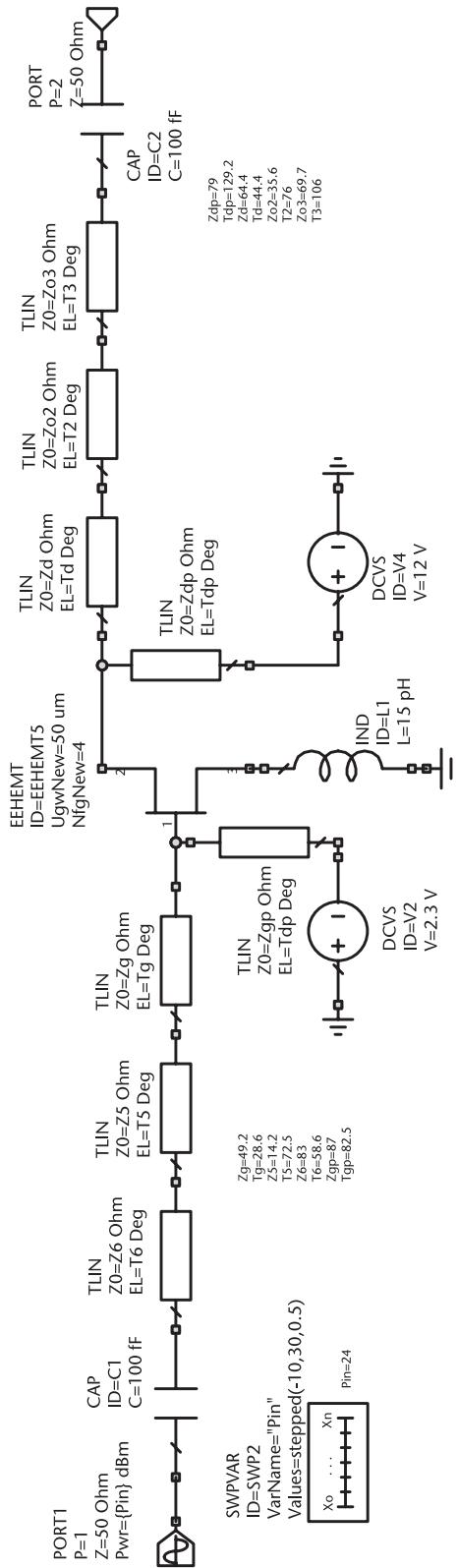
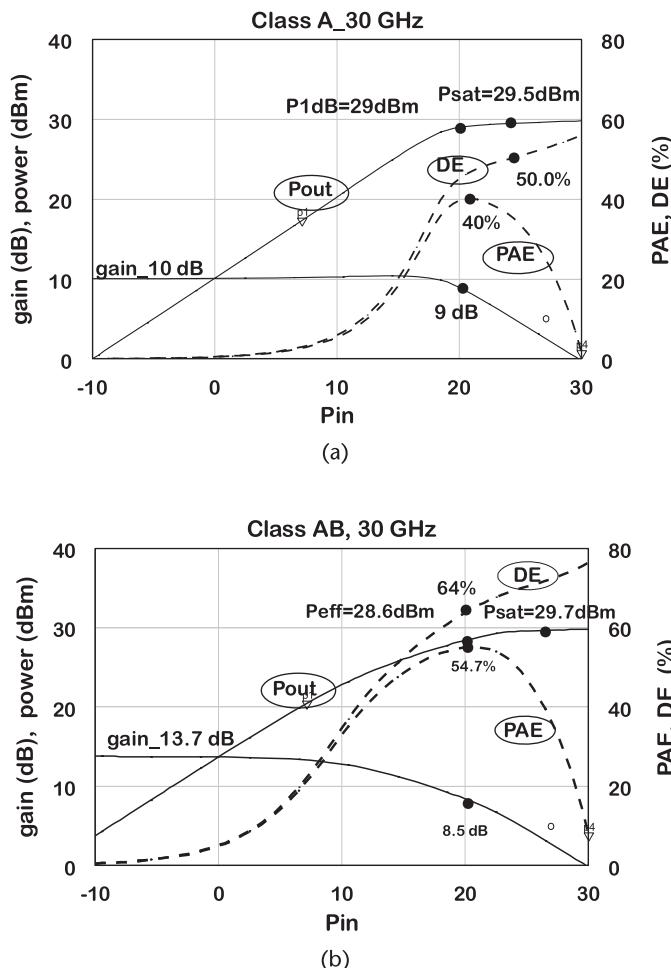


Figure 3.56 Schematic of a class AB amplifier with lumped matching elements.

for best efficiency. The second-harmonic short is provided by the shunt stub lines used for biasing the circuit. The performance for the amplifier with a single-tone CW signal applied at the input is displayed in Figure 3.57(a), for the device biased at  $V_{GS} = -1V$ . The  $P_{1dB}$  power is equal to 29 dBm with a gain of 9 dB. The drain efficiency is close to 46% and the PAE is 40%.

The class AB amplifier is represented in Figure 3.57(b) depicting a  $P_{1dB} = 28.6$  dBm, and a PAE of 54.7%, close to the value in Table 3.2. The drain efficiency goes up to 64%, with the gain compressed by 6 dB at this power level. These results are for a circuit matched with lossless transmission lines. A real circuit is expected to show a gain degraded by 1 dB and an output power by 0.5 dB.

Another linear parameter with a single-tone excitation is the amplitude and phase response. For this purpose, a low frequency at 0.8 GHz and a millimeter-wave amplifier at 30 GHz were simulated for AM-to-PM. The AM-to-AM is expressed in terms of gain compression, illustrated in previous figures. The low-frequency results are in Figure 3.58(a), showing less than 2° variation up to an input drive of +20 dBm. Figure 3.58(b) shows that classes A and B can support the same level of



**Figure 3.57** Power performance for the amplifier tuned at 30 GHz: (a) Class A performance, and (b) Class AB performance.

drive, while the class AB operation shows about  $5^\circ$  variation at an input drive of +16 dBm. Considering that the simulation at low frequency used a device 3 times larger, the 30-GHz amplifier clearly shows a larger modulation due to the effect of a nonlinear reactance in the circuit.

The plot containing the fundamental, third-order, and fifth-order intermodulation products is shown in Figure 3.59. The third-order intercept product is shown as the crossing of the lines tangent to the fundamental and third-order products, extended until they cross each other. The plots show an  $IP_3$  of +35 dBm. It is also shown that the  $IM_3$  level falls off the linear region above an input drive of 0 dBm. That sweet spot is used by the designers to improve the third-order products.

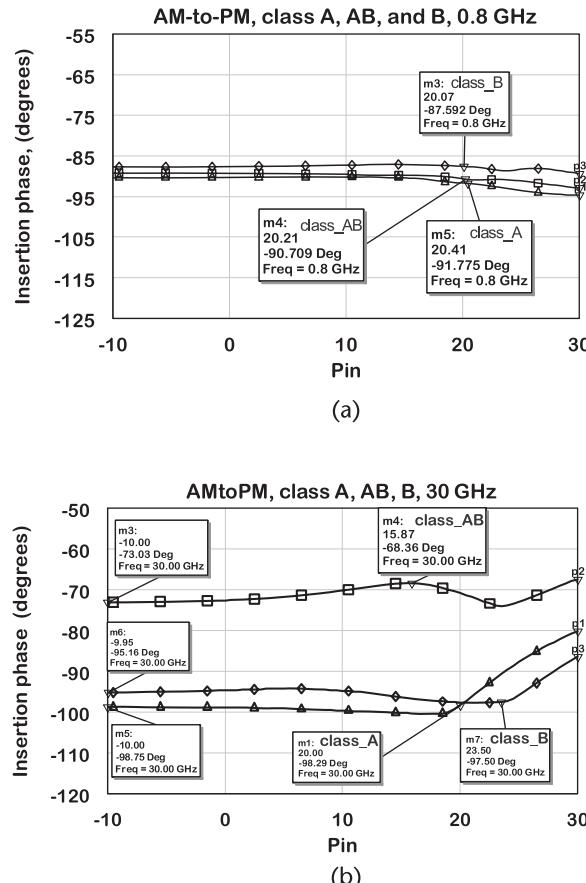
### 3.7.6 Class F Millimeter-Wave Amplifier

To confirm the results of the load-pull from Table 3.3, we simulated a test amplifier operating at a fundamental frequency of 30 GHz. We tried to obtain a bandwidth of 13%. The unit cell is of the same dimensions (i.e.,  $4 \times 50 \mu\text{m}$ ). Therefore, the saturated output power is expected to be 28 dBm. The initial circuit topology in Figure 3.60 is similar to the one employed in Figure 3.33 for the output circuit and in Figure 3.35 for the input circuit. However, the output shunt stub in the output circuit was terminated by a small capacitor to the ground. The objective was to present low effects at the fundamental frequency and better terminations at the second and third harmonics. The circuit parameters were optimized for power as the primary goal and then efficiency and bandwidth. The device is biased in deep class AB (i.e.,  $V_{GS} = -2.6\text{V}$ ).

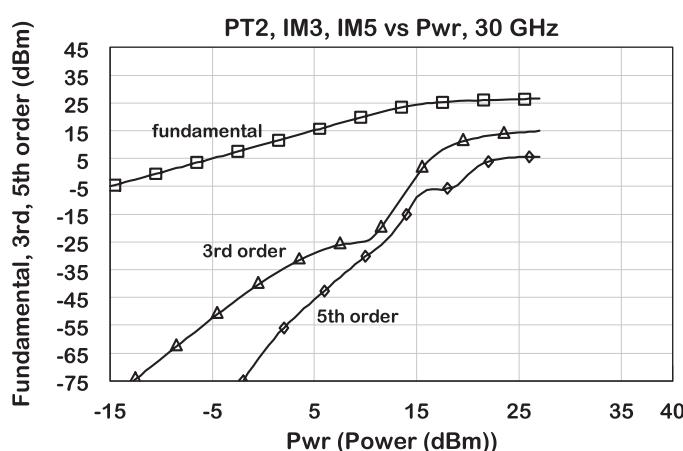
The harmonic load impedance after optimization is shown in Figure 3.61. Notice that the fundamental bandwidth of 4 GHz becomes 8 GHz at the second harmonic and 12 GHz at the third harmonic. The plot starts at 28 GHz showing the fundamental impedance. The second-harmonic termination is a shifted open circuit, while the third harmonic is in quadrature, indicating an inverse class F operation. This simple circuit shows a resonance at the beginning of the second harmonic and another near the third-harmonic band.

The power performance at 30 GHz is represented in Figure 3.62. One can notice a PAE of 60% at an output power of 28 dBm, with a compressed gain of 7 dB. At the input drive of 21 dBm, the drain efficiency is 74%. The power saturates above an input drive of 26 dBm to a value equal to 28 dBm. The small-signal frequency response is presented in Figure 3.63(a), showing a value about 2 dB lower than the small-signal gain simulated by the nonlinear model. The input and output return loss is better than 10 dB at the center frequency. The gain slope observed is due to a small inductance of 20 pH added to the source to improve stability. The slope in small-signal circuits is caused by imperfect impedance match over the band. The circuit stability is guaranteed by a source inductance. In a multistage amplifier, a resistor in series with the gate may be needed.

The power performance over the frequency band is shown in Figure 3.63(b). Notice that the slope in this case is observed under power conditions. It is caused mainly by nonuniform power compression over the band. The load impedance was slightly retuned to perform within the 13% bandwidth. Notice that the PAE at the center frequency went down from 60% to 56%. At an input power of 21 dBm, the



**Figure 3.58** Comparing AM-to-PM distortion at low (0.8 GHz) and high (30 GHz) frequencies:  
(a) AM-to-PM at 0.8 GHz, and (b) AM-to-PM at 30 GHz.



**Figure 3.59** Output power for the fundamental, third-order, and fifth-order products.

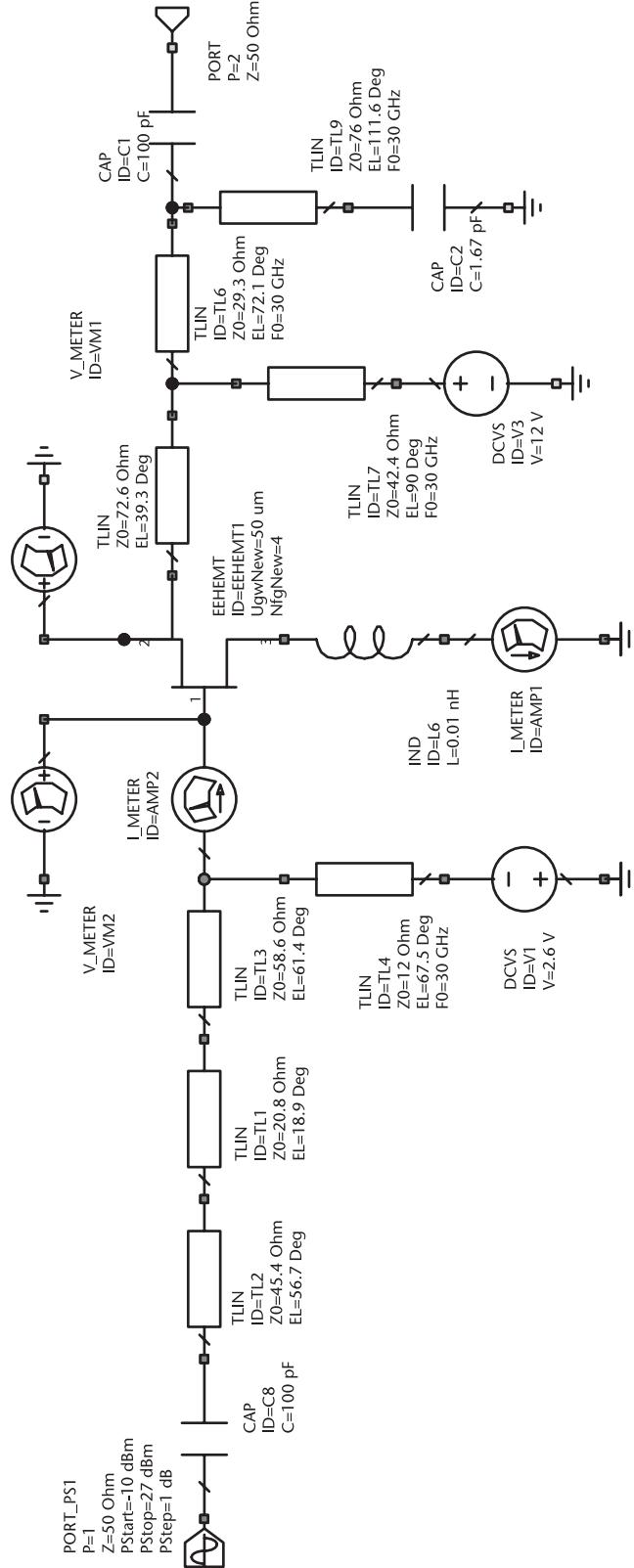
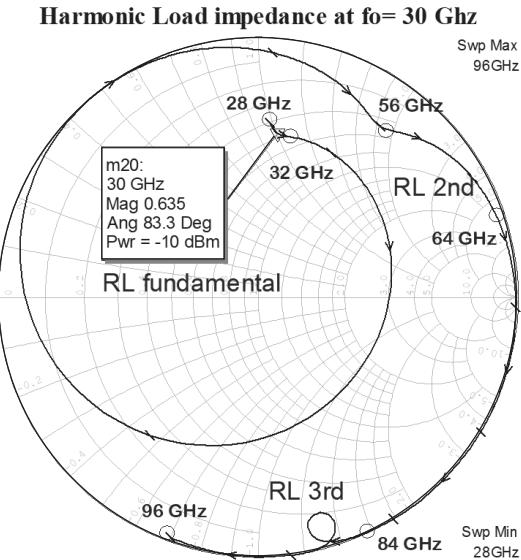
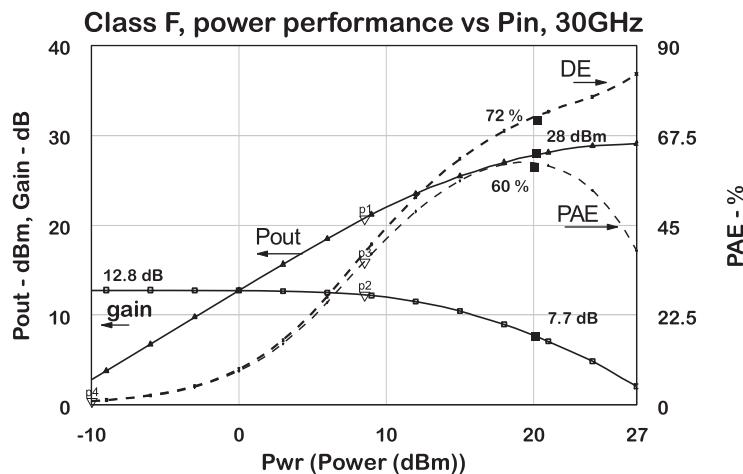


Figure 3.60 Circuit schematic for a 30-GHz power amplifier operating in class F.

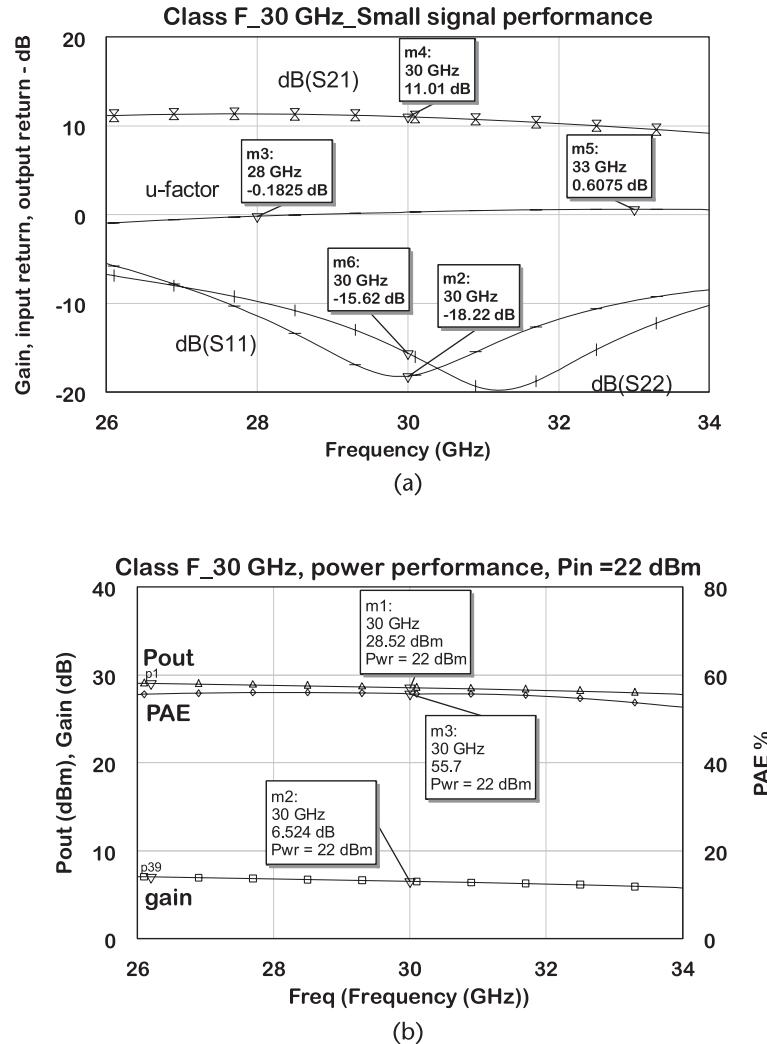


**Figure 3.61** Load impedances at  $f_0$  and the second and third harmonics measured at the device port.



**Figure 3.62** Class F  $P_{\text{out}} \times P_{\text{in}}$  over the drive level from  $-10$  to  $+27$  dBm.

output is flat at 28 dBm from 28 to 32 GHz. The PAE is also flat within the same band, showing 57% at the center frequency. The compressed gain is equal to 6 dB and is relatively flat over the band. The simulation results show that the simple harmonic load achieves a reasonable broadband in the class F operation. These results rely on the availability of an accurate nonlinear model. Without such a model, it is not possible to have access to the parameters shown in the figures.



**Figure 3.63** Class F performance matched with ideal transmission lines: (a) Class F small signal performance, and (b) Class F large signal performance.

## References

- [1] de Hek, A. P., "Design, Realization and Test of GaAs-Based Monolithic Integrated X-Band High-Power Amplifiers," Eindhoven Tech. University, 2002.
- [2] Clarke, K. K., and D. T. Hess, *Communication Circuits: Analysis and Design*, Reading, MA: Addison-Wesley, 1971, p. 145.
- [3] Kaper, V., et al., "Dependence of Power and Efficiency of AlGaN/GaN HEMT's on the Load Resistance for Class B Bias," *IEEE Lester Eastman Conference on High Performance Devices*, 2002, 118–125.
- [4] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 139.
- [5] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 142.
- [6] Maas, S. A., *Nonlinear Microwave and RF Circuits*, Norwood, MA: Artech House, 2003, p. 16.
- [7] Ku, H., M. D. McKinley, and J. S. Kenney, "Quantifying Memory Effects in RF Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 50, No. 12, December 2002, pp. 2843–2849.
- [8] de Carvalho, N. B., and J. C. Pedro, "Compact Formulas to Relate ACPR and NPR to Two Tone IMR and IP3," *Microwave Journal*, December 1999, pp. 70–84.
- [9] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 236.
- [10] Acar, E., "How Error Vector Magnitude (EVM) Improves Your System Level Performance," Technical Article by Analog Devices, 2021.
- [11] Lozhkin, A. N., T. Maniwa, and, M. Shimizu, "RF Front-End Architecture for 5G," *2018 IEEE 29th Annual International Symposium on Personal, Indoor, and Mobile Radio Communications*, 2018.
- [12] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 113
- [13] Tyler, V. J., "A New High Efficiency High Power Amplifier," *Marconi Review*, Vol. 21, No. 130, 1958, pp. 96–109.
- [14] Raab, F. H., "Introduction to Class-F Power Amplifiers," *RF Design*, Vol. 19, No. 5, May 1996, pp. 70–84.
- [15] Raab, F. H., "Class-F Power Amplifiers with Maximally Flat Waveforms," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 11, November 1997, pp. 2007–2012.
- [16] Merrick, B., J. King, and T. Brazil, "A Simplified Procedure for the Design of Continuous Class-F Power Amplifiers," *Proceeding of the European Microwave Integrated Circuits Conference*, 2013, pp. 508–511.
- [17] Carrubba, V., et al., "The Continuous Class-F Mode Power Amplifier," *Proc. of the 5th European Integrated Circuits Conference*, Paris, September 2010, pp. 432–435.
- [18] Merrick, B. M., J. B. King, and T. J. Brazil, "A Novel Continuous Class-F Mode Power Amplifier," *IMS 2014*, 2014.
- [19] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 290.



# Impedance Matching

The RF impedance of cables was standardized in the 1940s to be  $50\Omega$ . At that time, it was found that this value gives the best compromise between attenuation and power capability for the propagation of signals along coaxial lines. So the impedance of every generator, antenna, and circuit has to be matched to the standard  $50\Omega$ . Therefore, the transfer of signals between RF components is just a matter of connection. It is also common to have an RF transistor delivering power to a low-impedance load, which needs to be elevated to  $50\Omega$ . In RF amplifiers, the impedances along amplification stages need to be matched in order to guarantee a maximum transfer of power. At millimeter-wave frequencies, this problem is more critical for even small parasitic elements in the signal path and may cause signal attenuation. Because semiconductor materials are manufactured on top of semiconductor wafers of standard dimensions, say, 4, 6, or 8 inches in diameter, it is also important that the matching circuits are just large enough to fulfill its function, as space on the circuit costs money. An additional design demand for MMICs is the robustness of the circuit design. That will guarantee that the amplifier will perform within certain bounds, in spite of fabrication tolerances. The design engineer has to take all those factors into account. The objective of this chapter is to review the impedance matching techniques most appropriate for the MMIC environment.

## 4.1 Matching Requirements

A matching network can be studied as a two-port network, characterized by its S-parameter matrix. Its objective is to transfer power from a source to a load with a minimum loss possible within a desired band of frequency (Figure 4.1). In order to meet this condition, the input and output impedances are required to be conjugate-matched. Therefore, if we assume at the input port that the equivalent impedance is  $Z_{in}$  and the generator impedance is equal to  $Z_g$ , then the conjugate matching conditions are defined by (4.3) and (4.4).

$$Z_{in} = R_{in} + jX_{in} \quad (4.1)$$

$$Z_g = R_g + jX_g \quad (4.2)$$

$$\text{Conjugate matching conditions: } R_{in} = R_g \quad (4.3)$$

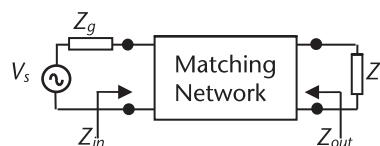
$$jX_{in} = -jZ_g \quad (4.4)$$

The GT, the transducer gain of the network, defined in Chapter 2 by (2.20), gives a more complete description of the matching network. If we build a network with 0 reflections at the input and output, with respect to the reference impedance of  $Z_0 = 50\Omega$ , then  $\Gamma_g = \Gamma_L = 0$  and the transducer gain is equal to  $|S_{21}|^2$ , which is the insertion loss of the matching network, under matched conditions. This parameter is used in the text every time we simulate the insertion loss of a passive circuit. The insertion phase is defined as the phase of  $S_{21}$ .

One can start matching a source to a load using filter theory, where the insertion loss can be expressed by a transfer function, described by the ratio of two polynomials. They are related to a lowpass prototype network consisting of a cascade of series L, parallel C cells. The most common function (Butterworth) results in a maximally flat insertion loss up to the cutoff frequency. Another function, Cheby-shev, is associated to a ripple in the filter passband up to the cutoff frequency [1]. Both approaches show an exponential insertion loss above the cutoff frequency. Given the specifications for the filter (cutoff frequency, source and load resistance, ripple), the normalized elements for the lowpass network are numerically determined or extracted from computer-generated tables resulting in the initial values for the network elements. In the case of designing broadband matching networks of an amplifier, it is necessary to compensate for the drop in the device gain with frequency. The polynomials that express the frequency response of such networks can be modified, such as to produce a prescribed amount of mismatch that compensates for the device gain slope, in the attempt to achieve a passband response as flat as possible [2]. Another possibility is to design for optimum match over the band and add an equalizer to absorb the excess gain at lower frequencies. Such an equalizer is found at the input of power amplifiers and at the output of low noise amplifiers.

There are several other methods described in the literature developed from basic filter theory to generate a network capable of matching the impedance of the active devices in a high-frequency amplifier. A good summary of matching methods is found in [3].

However, in the particular case of narrowband designs, a more simple approach can be employed. One can make use of prototype networks described by simple equations. One point that is debatable is the limit for a narrowband circuit. A bandwidth below 25% of the fractional bandwidth is commonly agreed to be considered a narrow band. Operation over an octave band or up is regarded as characterizing a broadband circuit. However, in between these limits, there is no line defining, say, a 50% band to be a maximum narrowband or large-band circuit. Fortunately, for



**Figure 4.1** Matching network as a two-port.

power amplifier matching, one is not really interested in a large-band operation, as the best performance is more easily achievable at narrower frequency bands. In other words, the larger the bandwidth, the more the performance goals have to be compromised.

The quality factor,  $Q$ , is an important parameter for impedance matching. It is defined as the ratio of stored energy to dissipated energy. For a parallel RLC circuit, the Q-factor is defined by (4.5). Equation (4.6) stands for a series RLC circuit. These relations are valid at the resonance frequency,  $\omega_0 = 1/\sqrt{LC}$ . Therefore, when we refer to a high  $Q$  inductor, it means that its series ohmic losses are very low. A high  $Q$  capacitor indicates that its parallel losses are very low.

$$Q = \frac{\omega_0 C}{G} = R \sqrt{\frac{C}{L}} \quad (4.5)$$

$$Q = \frac{\omega L}{R} = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (4.6)$$

The relationship between the 3-dB bandwidth and the Q-factor of a tuned RLC circuit is given by (4.7). Hence, the higher the  $Q$ , the narrower the band and the sharper the tuned resonance response. Thus, one aims at high  $Q$  matching components for lower losses and a matching circuit with low  $Q$  for a large-band operation. A good way to determine the Q-factor of a network is from the slope of the susceptance,  $B$ , or reactance,  $X$ , versus frequency. Equation (4.8) is applicable to an admittance defined network and (4.9) is applicable for an impedance defined network.

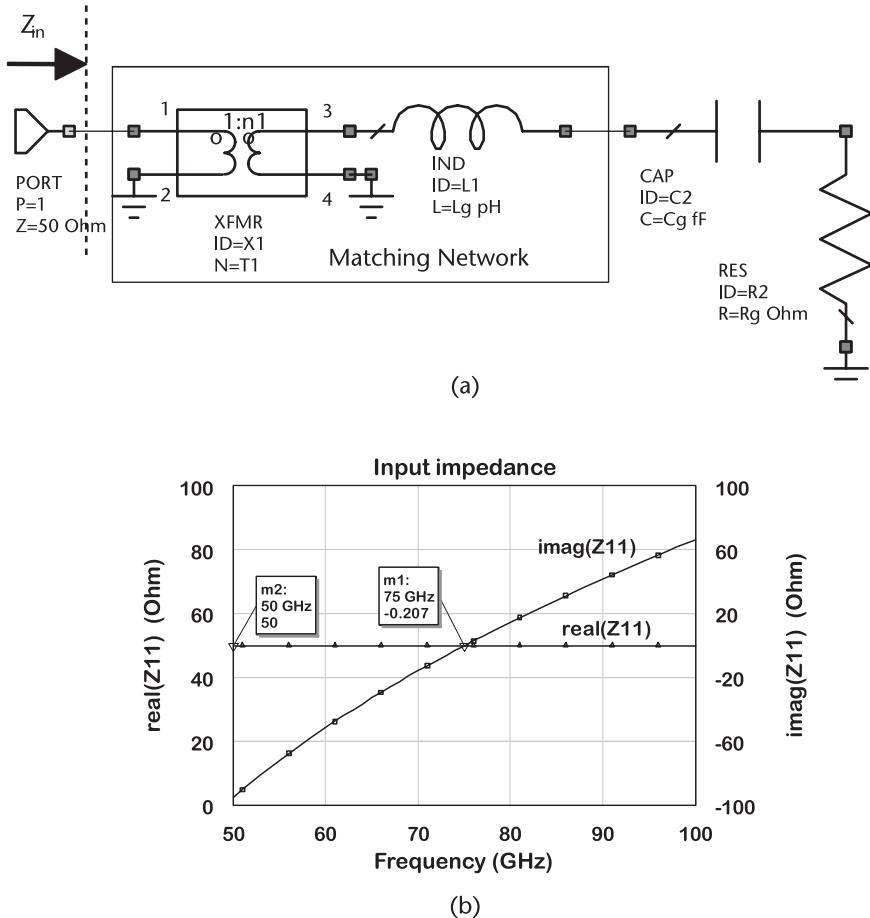
$$Q = \frac{f_0}{\Delta f} \quad (4.7)$$

$$Q = \left. \frac{\omega_0}{2G} \frac{dB}{d\omega} \right|_{\omega=\omega_0} \quad (4.8)$$

$$Q = \left. \frac{\omega_0}{2R} \frac{dX}{d\omega} \right|_{\omega=\omega_0} \quad (4.9)$$

## 4.2 Reactance Compensation

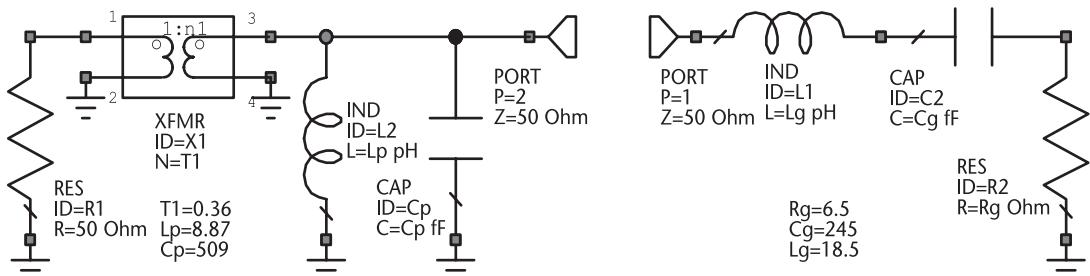
An example of a conjugate matched network can be seen in Figure 4.2. The gate capacitance is resonated with a series inductance, and the resulting impedance is transformed to  $50\Omega$  by an ideal transformer. The plot shows that the real part of the input impedance  $Z_{in}$  is matched over a large band to  $50\Omega$ . The reactive part is null only at the resonance frequency of 75 GHz. Additional conditions are needed to obtain matching over a larger frequency range. The first report describing a practical solution to this problem was made by Aitchison et al. [2, 3].



**Figure 4.2** Conjugate matching: (a) matching at  $f_0 = 75$  GHz, and (b) impedance presentation.

Let us start by considering Figure 4.3, where a parallel inductance  $L_p$  and capacitance  $C_p$  circuit have been added on the generator side. Now let's assume that we vary  $L_p$  and  $C_p$  values so that the reactance slope of the circuit from port 2 is the same as the reactance slope from port 1, with the opposite sign. The real part of impedance from source and load are kept the same during this process.

Such a condition is represented in Figure 4.4, where reactance of input impedance from ports 1 and 2 are represented. They show the center frequency slope



**Figure 4.3** Broadband matching with reactance compensation.

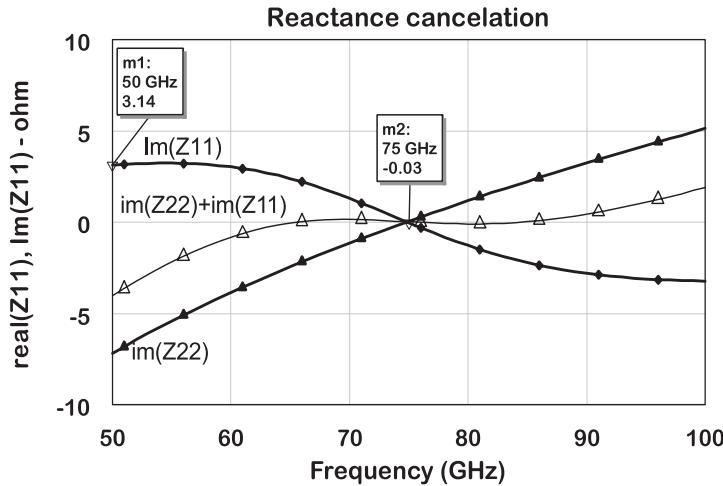


Figure 4.4 Reactance compensation curves.

of different signs. The compensated reactance corresponds to the combination of both curves. The compensation bandwidth is limited by the frequencies where the reactance falls off from the slope line crossing the center frequency.

To determine the circuit conditions for meeting such criteria, let us consider two cases. In the first case, a parallel circuit LC is added to compensate the reactance of a series LC circuit. In the second case, a series circuit is added to compensate the reactance of a parallel LC circuit. For the first condition, let us rearrange the circuit as in Figure 4.5 and calculate the input impedance  $Z_{in}$ , (4.10 and [4]). Given the series  $L_0, C_0$  circuit, what are the parallel values  $L_1$  and  $C_1$  that will produce reactance compensation?

$$Z_{in} = j\omega L_0 + \frac{1}{j\omega C_0} + \frac{R}{1 + j\omega' C_1 R} \quad (4.10)$$

With  $\omega' = \omega \left(1 - \frac{\omega_0^2}{\omega^2}\right)$  and  $\omega_0^2 = \frac{1}{L_1 C_1}$ .

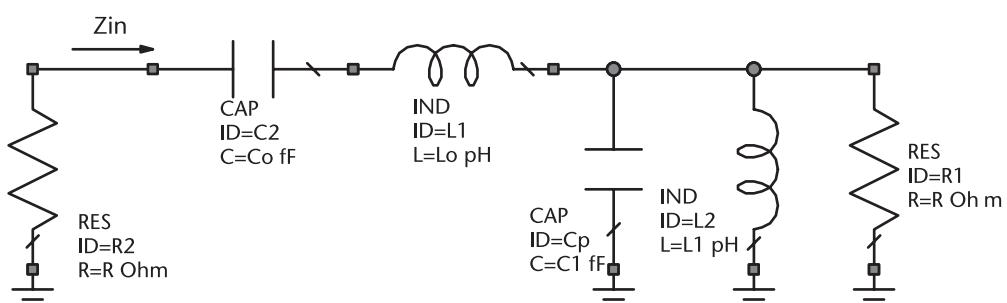


Figure 4.5 Input impedance to calculate reactance compensation for the RLC series circuit.

Next, let's calculate the derivatives of reactive components and equate them to 0.

$$\frac{dX_{in}}{d\omega} = L_0 + \frac{1}{\omega^2 C_0} - 2C_1 R^2 = 0|_{\omega=\omega_0} \quad (4.11)$$

Therefore, capacitance  $C_1$  is defined by (4.12), and  $L_1$  is defined from the resonance condition.

$$C_1 = \frac{1}{2R^2} \left( L_0 + \frac{1}{\omega_0^2 C_0} \right) = \frac{L_0}{R^2} \quad (4.12)$$

$$L_1 = \frac{1}{\omega_0^2 C_1} = R^2 C_0 \quad (4.13)$$

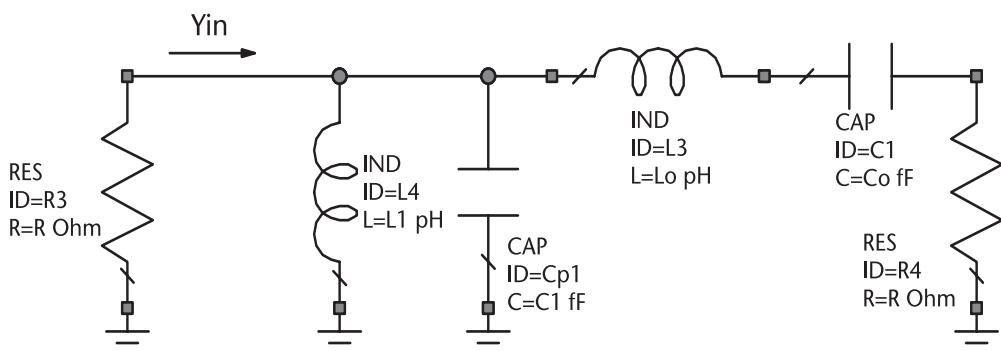
For the second case, that is, given a parallel RLC circuit ( $L_1, C_1$ ), the series LC ( $L_0, C_0$ ) is added to compensate the parallel reactance as shown in Figure 4.6. The input admittance of the circuit in the figure is defined by (4.14).

$$Y_{in} = j\omega C_1 + \frac{1}{j\omega L_1} + \frac{1}{R + j\omega' L_0} \quad (4.14)$$

Following a similar procedure, the derivative of the function gives  $L_0$  as a function of  $C_1$  and the resonance condition gives  $C_0$  as a function of  $L_0$ .

$$L_0 = \frac{R^2}{2} \left( C_1 + \frac{1}{L_1 \omega_0^2} \right) = R^2 C_1 \quad (4.15)$$

$$C_0 = \frac{1}{\omega_0^2 L_0} = \frac{L_0}{R^2} \quad (4.16)$$



**Figure 4.6** Input admittance to calculate the compensation RLC parallel circuit.

The summary for conjugate matching and reactance compensating a generator to a load impedance appears in the equations below. Similar equations are valid for source and load admittance.

$$\begin{aligned} R_L &= R_S \\ X_L &= -X_S \\ \left. \frac{dX_L}{d\omega} \right|_{\omega=\omega_0} &= - \left. \frac{dX_S}{d\omega} \right|_{\omega=\omega_0} \end{aligned}$$

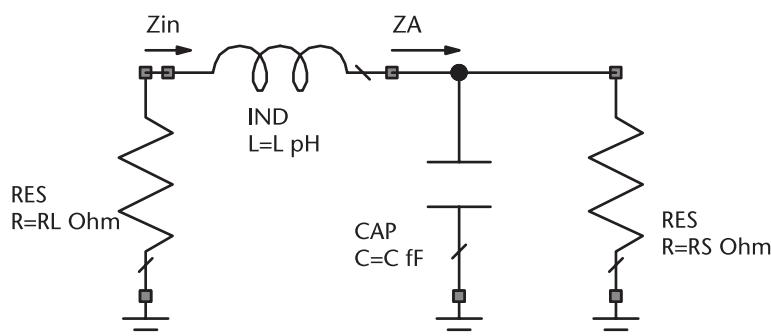
## 4.3 Matching with Lumped Prototypes

In this category, the capacitors and inductors are part of a network topology, which can meet the matching requirements. These prototypes are not directly applicable to millimeter-wave frequencies but are important in defining a basic matching topology. For most applications in high frequency, they have to be partially or fully converted to distributed elements.

### 4.3.1 L-Section

The simplest matching element is the single L network, containing a series and a parallel reactive element. The circuit in Figure 4.7 considers the case of matching a resistor  $R_L$  to  $R_S$ , with  $R_L > R_S$ . Calculating the impedance  $Z_A$ , we obtain (4.17). It is observed that  $R_L$  is divided by a factor greater than 1, which will reduce  $R_L$  to the desired value  $R_S$ , after (4.18). Therefore, the circuit steps down to the resistance  $R_L$ . There is a residual capacitive reactance that can be eliminated by a series inductance defined by (4.19). The input impedance  $Z_{in}$  at the center frequency of operation then becomes equal to  $R_S$ .

A systematic way of obtaining this solution and avoiding many calculations consists in the use of a process called transformation-Q [3]. In (4.17), it can be noted that the load  $R_L$  is divided by a factor  $1 + (\omega R_L C_1)^2$ , which is equal to  $1 + Q^2$ . Then the Q-factor can be defined as the ratio of the two resistances intended to be matched, (4.20).



**Figure 4.7** Single L matching between  $R_L$  and  $R_S$  for  $R_L > R_S$ .

$$Z_A = \frac{R_L}{1 + (\omega R_L C)^2} - \frac{j\omega R_L^2 C}{1 + (\omega R_L C)^2} \quad (4.17)$$

$$R_S = \frac{R_L}{1 + (\omega R_L C)^2} \quad (4.18)$$

$$L = \frac{R_L^2 C}{1 + (\omega R_L C)^2} \quad (4.19)$$

The parallel association of resistor  $R_L$  and capacitance  $C$  defines a series reactance  $X_S$ , (4.21), using the same Q-factor. Considering that the Q-factor of the series  $R_S$ , the  $L$  circuit is equal to the Q-factor of the parallel  $R_L$ ,  $C$  circuit, one obtains (4.22). The set of design equations for single L matching is then (4.20) to (4.22).

$$Q = \sqrt{\frac{R_L}{R_S} - 1} \quad (4.20)$$

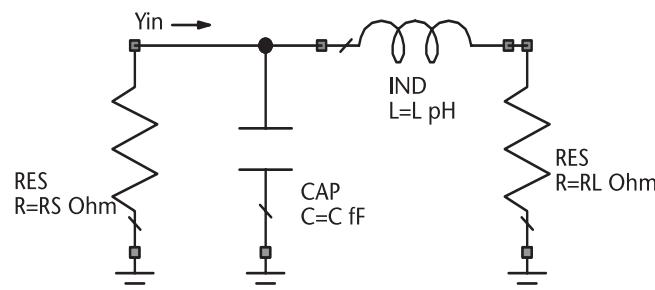
$$X_S = QR_S \quad (4.21)$$

$$X_p = \frac{R_L}{Q} \quad (4.22)$$

The single L network can also be used to raise the impedance  $R_L$  to  $R_S$ , shown in Figure 4.8. The input admittance for the circuit is given by (4.23). The real part of impedance is in (4.24), and the capacitance required to tune the residual reactance is in (4.25).

$$Y_{in} = \frac{1}{R_L + j\omega L} + j\omega C = \frac{R_L}{R_L^2 + (\omega L)^2} - \frac{j\omega L}{R_L^2 + (\omega L)^2} + j\omega C \quad (4.23)$$

$$R_S = \frac{R_L^2 + (\omega L)^2}{R_L} \quad (4.24)$$



**Figure 4.8** Single L matching between  $R_L$  and  $R_S$  for  $R_S > R_L$ .

$$C = \frac{L}{R_L^2 + (\omega L)^2} \quad (4.25)$$

The design equations are (4.26) to (4.28). One can notice that the design equations for this circuit and the previous one are derived in a similar way. The final result is analogous, with  $R_S$ ,  $R_L$  and  $X_S$ ,  $X_p$  interchanged.

$$Q = \sqrt{\frac{R_S}{R_L} - 1} \quad (4.26)$$

$$X_S = QR_L \quad (4.27)$$

$$X_p = \frac{R_S}{Q} \quad (4.28)$$

The procedure to determine the element values of these networks are in the following equations with  $R_L > R_S$ .

The design steps are the following:

Step (a): The shunt reactance is in parallel with the highest resistance.

Step (b): Calculate the transformation ratio,  $R_L/R_S$ .

Step (c): The Q-factor is determined from  $Q = \sqrt{\frac{R_L}{R_S} - 1}$ .

Step (d): Make  $X_S = QR_S$ .

Step (e): Make the resonating reactance,  $X_p = \frac{R_L}{Q}$ .

Step (f):  $X_s$  and  $X_p$  have different signs.

Notice that the procedure is valid for either up or down resistance scaling if step (a) is observed. That is, the  $R_L$  is designated to be the larger value connected in shunt with the reactive element to be scaled down. It is also important to notice the expressions are in terms of reactance,  $X_S$  for the series element and  $X_p$  for the parallel element. Therefore, the procedure is also valid if the capacitance and inductance are swapped by the inductance and capacitance, respectively. The procedure is not valid for the case of an L network composed by two inductors or two capacitors.

### 4.3.2 L-Section and Reactance Compensation

Adding a reactance compensation network to a single L cell improves bandwidth response. As an example, let us transform the drain impedance of a typical FET into  $50\Omega$ , at the frequency of 75 GHz using a single L, as represented in Figure 4.9. The parallel drain resonance was discussed in Chapter 2, obtained through the insertion of a parallel inductance  $L_p$  and accounting for the parasitic series inductance  $L_d$ . The L section matching ( $C_2/L_2$ ) is calculated after (4.26) to (4.28). To insert a reactance compensation circuit, one needs to find the equivalent RLC parallel circuit. The equivalent circuit of node A suppressing the circuit on the right

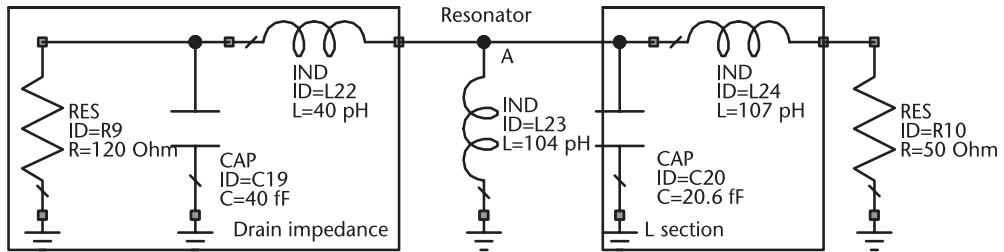


Figure 4.9 Matching a parallel resonated drain impedance to  $50\Omega$  using a single L matching.

is obtained by first transforming the parallel RC circuit in series, adding the series inductance, and then converting the resulting impedance to parallel equivalent to add the resonating inductance. A much faster solution is to enter the drain circuit in the simulator, and use the Smith chart to perform these operations. Applying (4.15) and (4.16), we obtained  $L_0 = 400$  pH and  $C_0 = 11.3$  fF. The complete circuit is in Figure 4.10. The L section was modified to take account of approximations on reading the Smith chart impedance values.

There are two important impedances in Figure 4.10. The load impedance,  $Z_L = 1/Y_{11}$ , is obtained from node A, looking towards  $50\Omega$ , with the drain suppressed.

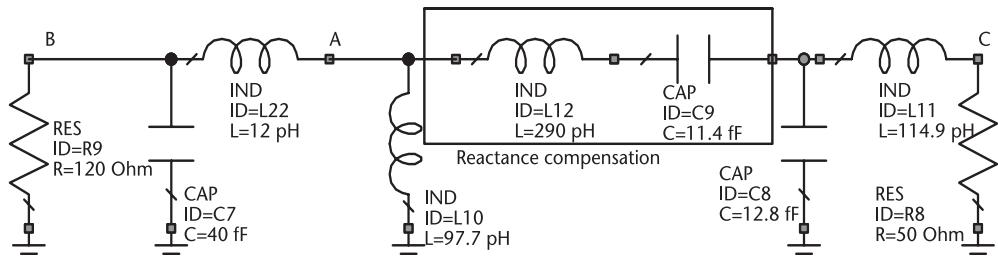


Figure 4.10 Use of the series LC reactance compensation network.

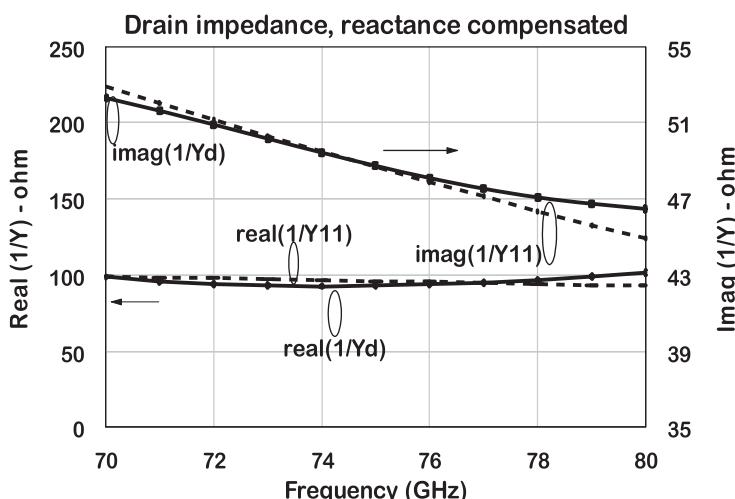


Figure 4.11 Drain and load impedance.

The drain impedance is also obtained from node A, looking towards the drain, defined by  $Z_d = 1/Y_d$ , with the load circuit suppressed. The load impedance is shown in Figure 4.11, which shows the curves for the real part of both impedances. The imaginary curves show a negative slope for  $Z_d$  and a positive slope for the load circuit. The imaginary part of the drain circuit was multiplied by  $-1$  in order to use only positive values in the graph. One can see that both the real and imaginary parts of the load track the drain impedance. However, they are not exact because the circuit is compensating only the drain-resonated circuit. The L matching to  $50\Omega$  is not compensated. The impedance looking from node C towards the drain is in the Smith chart of Figure 4.12, represented by the parameter  $S_{22}$ . The impedance looking from node B towards the  $50\Omega$  load is represented by the parameter  $S_{11}$ .

Another example of interest is the reactance compensation of a series resonated drain impedance, using a single L match, as shown in Figure 4.13. That makes the node A impedance towards the drain equal to  $20\Omega$  at 75 GHz.

The L matching ( $L_2/C_2$ ) is then used to step up  $20\Omega$  to  $50\Omega$ . In this case, a parallel reactance compensation network,  $L_1$ ,  $C_1$ , was inserted in shunt to the drain port and the L matching circuit. The circuit shows similar behavior as Figures 4.11 and 4.12. The circuit parameters are listed in Table 4.1.

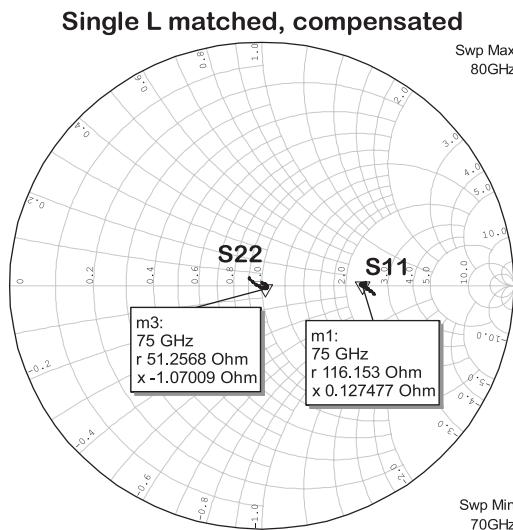


Figure 4.12 Impedance at the  $50\Omega$  port.

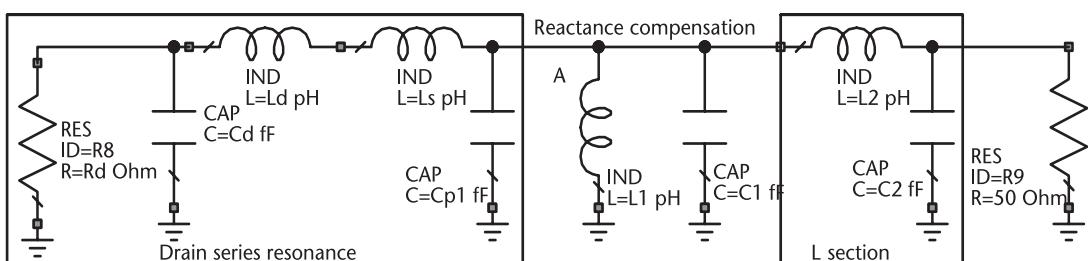


Figure 4.13 Parallel LC compensating network.

**Table 4.1** Parameters for the Matching Circuit in Figure 4.13

Parameter	Value	Parameter	Values
$R_d$ ( $\Omega$ )	120	$L_1$ (pH)	333
$C_d$ (fF)	40	$C_1$ (fF)	30
$L_d$ (pH)	10	$L_2$ (pH)	58.2
$L_s$ (pH)	93	$C_2$ (fF)	51.3
$R_1$ ( $\Omega$ )	100	$R_s$ ( $\Omega$ )	50

### 4.3.3 Cascade of L Sections

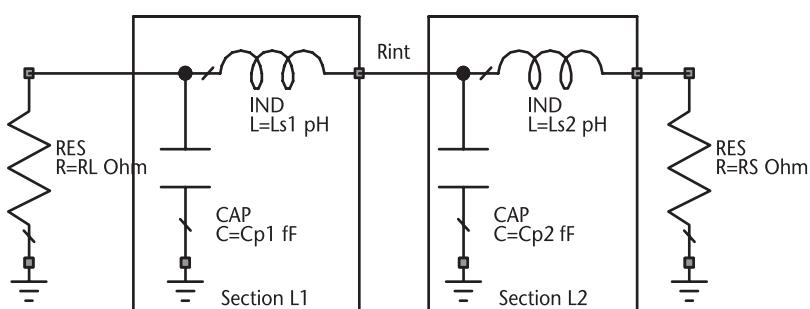
The Q-factor of a single L matching network is given by (4.20), related to the ratio of load and source resistance. Now let us assume a cascade of two L sections, in the forms shown in Figures 4.14 and 4.15. The first is called the lowpass/lowpass option and the second is a highpass/lowpass option. The first network transforms  $R_L$  to a virtual intermediate impedance,  $R_{int}$ . The second network transforms  $R_{int}$  to  $R_S$ . The design of each cell is similar to the single L case, where the resistance to be lowered is shunted by a reactive element. The design procedure is described below. There are two other options for cascading L sections, which are not shown here. They are, namely, the lowpass/highpass and highpass/highpass types.

The summary for the design procedure is as follows:

Step (a): Let us assume that the relation between the virtual resistance and the source and load is a geometric mean, as expressed by (4.29).

$$\frac{R_L}{R_{int}} = \frac{R_{int}}{R_S} \quad (4.29)$$

Step (b): Equation (4.29) comes from assuming that the Q-factors of network  $L_1$  and network  $L_2$  are the same, that is,  $Q_1 = Q_2$ . From this, we can conclude that the Q-factor of the cascade can be lower than the Q-factor for the single L network. Therefore, this option can provide larger bandwidth. The Q-factor of each cell is defined by (4.30) and (4.31).

**Figure 4.14** Lowpass/lowpass.

$$Q_1 = \sqrt{\frac{R_L}{R_{\text{int}}} - 1} \quad (4.30)$$

$$Q_2 = \sqrt{\frac{R_{\text{int}}}{R_S} - 1} \quad (4.31)$$

Step (c): The reactance of each element is given by the Q-factor of each section. Therefore, the network from Figure 4.14 can be calculated using (4.32) and (4.33). For Figure 4.15, one should use (4.34) and (4.35).

Step (c1): Lowpass-lowpass:

$$X_{s1} = \omega L_{s1} = R_{\text{int}} Q_1, \quad X_{s2} = \omega L_{s2} = R_S Q_1 \quad (4.32)$$

$$X_{p1} = \frac{1}{\omega C_p} = \frac{R_L}{Q_1}, \quad X_{p2} = \frac{1}{\omega C_p} = \frac{R_{\text{int}}}{Q_1} \quad (4.33)$$

Step (c2): Highpass-lowpass:

$$X_{s1} = \frac{1}{\omega C_s} = R_{\text{int}} Q_1, \quad X_{s2} = \omega L_s = R_S Q_2 \quad (4.34)$$

$$X_{p1} = \omega L_{p1} = \frac{R_L}{Q_1}, \quad X_{p2} = \frac{1}{\omega C_p} = \frac{R_{\text{int}}}{Q_2} \quad (4.35)$$

The schematic for an application to match a series resonated drain impedance to  $50\Omega$  is shown in Figure 4.16. The circuit uses a lowpass/highpass circuit to transform the impedance at node A of  $22.7\Omega$  to  $50\Omega$ . The impedance  $Z_A$  looking towards the drain is equal to  $22.7\Omega$ .

That makes the internal resistance  $R_{\text{int}}$  of the cascade equal to  $33.7\Omega$ . The element values are in Table 4.2. The Q-factors must be equal, that is,  $Q_1 = Q_2 = 0.7$ .

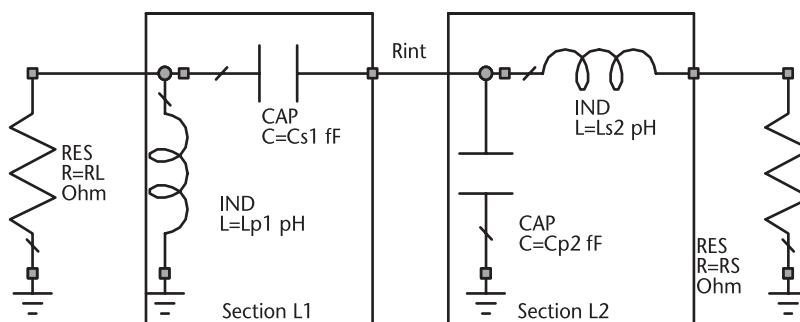
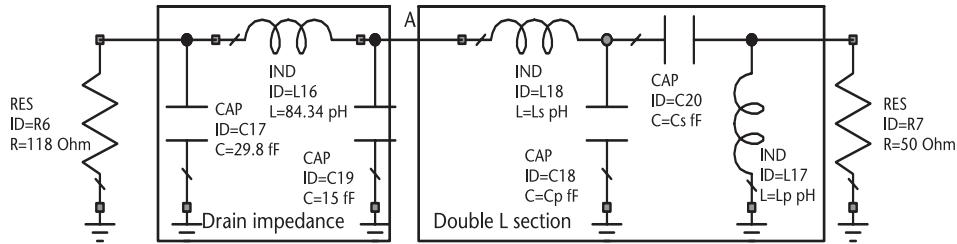


Figure 4.15 Highpass/lowpass.



**Figure 4.16** Use of lowpass, highpass matching network.

The circuit parameters were initially calculated from (4.34) and (4.35). The parameters were then optimized.

The simulation results for the double-L matching network are presented in Figure 4.17 for the initial and optimized design values. They are measured from the internal resistor node to the external resistor node. It can be noticed in the figure that the initial circuit identified by  $S_{21}$  and  $S_{22}$  in the dotted lines has a nearly constant insertion and return loss parameters within a 10% bandwidth. The optimization goal was to extend the band as much as possible, maintaining the return loss below 20 dB. Optimizing the circuit, identified by  $S_{43}$  and  $S_{44}$  in the solid lines, has a bandwidth from 87 to 102 GHz.

That gives about 15% fractional bandwidth. The plot in Figure 4.18 shows the impedance from the  $50\Omega$  node. The initial circuit reaches  $50\Omega$  at the center frequency. The optimized circuit encloses the chart center, improving the matching over a larger bandwidth.

The matching with three L sections decreases the circuit  $Q$ . However, the component losses increase, so it may offset the advantage of a larger bandwidth. This association is mostly applied at the gate side of the amplifier, where a small increase in loss can be tolerated. An example of cascading two lowpass cells and one highpass cell is shown in Figure 4.19.

Each cell is designed as an individual cell with its own source and load resistor. The relation between each one of these terminations is in (4.36).

$$\frac{R_L}{R_A} = \frac{R_A}{R_B} = \frac{R_B}{R_S} \quad (4.36)$$

**Table 4.2** Parameters for the Matching Circuit in Figure 4.16

Parameter	Initial	Optimized
$C_s$ (fF)	94.8	150
$C_p$ (fF)	39.4	50
$L_s$ (pH)	30.1	10
$L_p$ (pH)	120.4	71.83

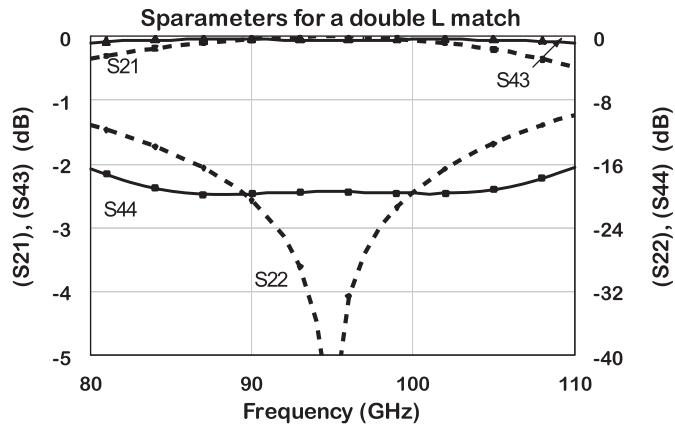


Figure 4.17 L section insertion and return loss.

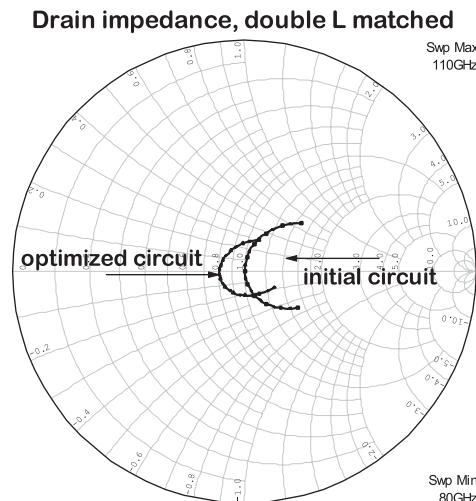


Figure 4.18 Impedance in the Smith chart.

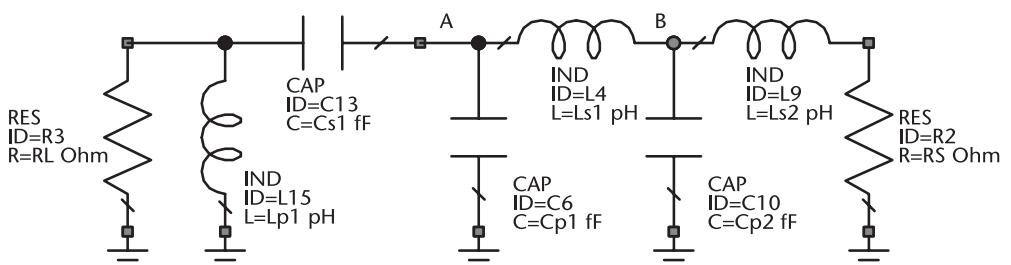


Figure 4.19 Application of a triple L section matching.

#### 4.3.4 PI Section

Adding one more parallel capacitor to the single L cell in Figure 4.8, we obtain a lowpass PI cell. Conventionally, the advantage of a PI cell over an L cell is the possibility of high harmonic rejection, a desirable feature in a class B type of amplifiers. One can think of a PI section as two single L sections in a back-to-back connection with the series elements, as shown in Figure 4.20 [4]. In this case, the virtual impedance at the joining point,  $R_B$ , has to be smaller than both  $R_L$  and  $R_S$ . There are two Q-factors in this circuit:  $Q_1$  for the circuit at the left of node B and  $Q_2$  for the circuit at the right. The equation connecting them is linked by the virtual resistance  $R_B$ . The values for the shunt capacitances can be obtained from (4.28), using the respective Q-factor value. The series element is obtained by adding the two inductances in series, each extracted from (4.27). With simple algebra, we obtain the design equations (4.37) to (4.41). The same equations are applicable for a highpass PI section composed of two shunt inductors and a series capacitance.

The design equations are valid for  $R_L > R_S$ . Notice that the first  $Q_1$  factor is designer-defined. Equation (4.37) defines a lower limit. The two Q-factors are not the same, so the larger Q dictates the bandwidth. The other parameters can be obtained from single L section design. The reactance of  $X_s$  is positive and  $X_{p1}$  and  $X_{p2}$  have the same negative signs.

$$Q_1 > \sqrt{\frac{R_L}{R_S} - 1} \quad (4.37)$$

$$Q_2 = \sqrt{\frac{R_S}{R_L} (1 + Q_1^2)} - 1 \quad (4.38)$$

$$X_{p1} = \frac{R_L}{Q_1} \quad (4.39)$$

$$X_{p2} = \frac{R_S}{Q_2} \quad (4.40)$$

$$X_s = \frac{R_L (Q_1 + Q_2)}{1 + Q_1^2} \quad (4.41)$$

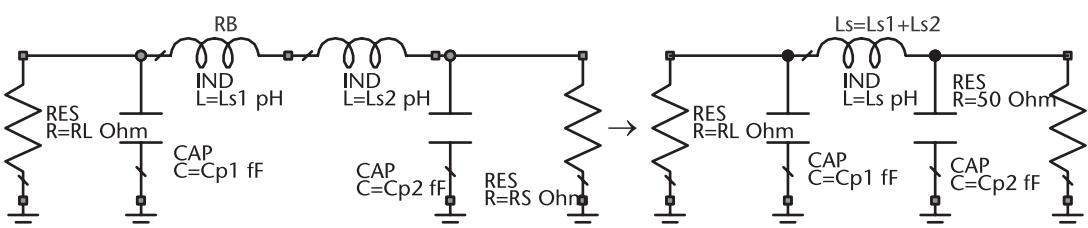


Figure 4.20 PI lowpass cell composed of two single L-type lowpass sections.

Figure 4.21 shows the simulation results for the lowpass PI circuit to transform  $100\Omega$  into  $50\Omega$ . The parameters used in this simulation are:  $C_{p1} = 23.5 \text{ fF}$ ,  $C_{p2} = 12 \text{ fF}$ , and  $L_s = 136 \text{ pH}$  for a center frequency of 75 GHz. The solid lines are for the  $50\Omega$  port, and the dotted lines are for the  $100\Omega$  port.

For the high side impedance,  $100\Omega$  is achieved at the center frequency and changes about  $\pm 10\Omega$  over the band. Notice that the reactances of both sides cross 0 at the center frequency with  $+j5$  and  $-j10$  at the edges of the band.

#### 4.3.5 T Section

Adding one more series element to the single L cell, we obtain a lowpass T section [5]. In Figure 4.22, it is shown that the T cell can also be obtained by connecting two L cells in a back-to-back configuration. The virtual resistance  $R_C$  at joining node now has to be larger than the values of  $R_L$  and  $R_S$ .

In this case, the series elements are defined by (4.27) and the shunt element is defined by (4.28), where  $X_{p1} = R_B/Q_1$  and  $X_{p2} = R_B/Q_2$ . The shunt component is defined by the parallel combination of  $X_{p1}$  and  $X_{p2}$ . The same equations are applicable for a highpass option, where the series elements are capacitors and the shunt element is an inductor. They also assume that  $R_L > R_S$ .

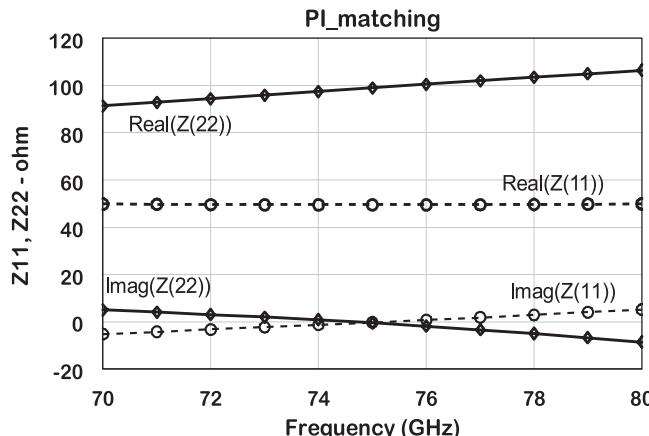


Figure 4.21 Simulation for a transformation from  $100\Omega$  to  $50\Omega$  using a PI section matching.

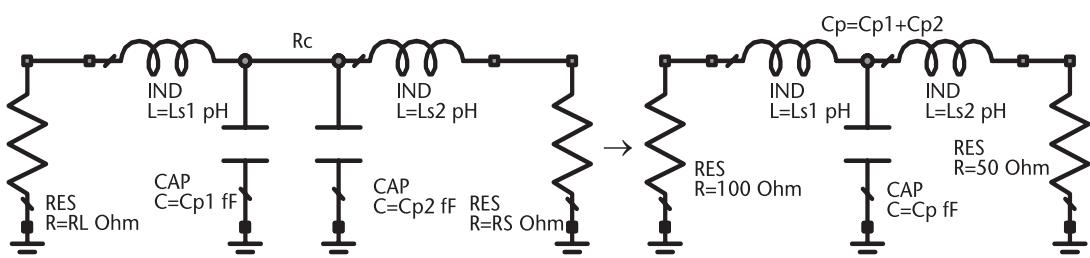


Figure 4.22 T type of cell composed of two lowpass L sections.

$$Q_2 > \sqrt{\frac{R_L}{R_S} - 1} \quad (4.42)$$

$$Q_1 = \sqrt{\frac{R_S}{R_L} (1 + Q_2^2) - 1} \quad (4.43)$$

$$X_{s1} = R_L Q_1 \quad (4.44)$$

$$X_{s2} = R_S Q_2 \quad (4.45)$$

$$X_p = \frac{R_S (1 + Q_2^2)}{Q_2 + Q_1} \quad (4.46)$$

The equations for a lowpass T section were tested in the transformation of  $100\Omega$  into  $50\Omega$ , at 75 GHz. The matching parameters are as follows:  $L_{s1} = 116.8$  pH,  $L_{s2} = 68.6$  pH, and  $C_p = 27.3$  fF. The circuit and simulation results are shown in Figure 4.23. The high-impedance port shows a flat resistance of  $100\Omega$  over the band. The low-impedance port crosses the  $50\Omega$  line at the center frequency. It shows a variation of less than  $5\Omega$  on either side. The reactance of both ports crosses 0 at the center frequency. The high-impedance side port shows a higher reactance variation, in the order of  $+/-j10\Omega$ . The low-impedance side shows less than  $+/-j5\Omega$  reactance variation.

There are other associations of double L that can be combined into a T or PI configuration. The most relevant is shown in Figure 4.24.

The design equations from the lowpass version, (4.42) to (4.45), are also valid for this case. Equation (4.46) should be replaced by (4.47).

$$X_p = \frac{R_S (1 + Q_2^2)}{Q_2 - Q_1} \quad (4.47)$$

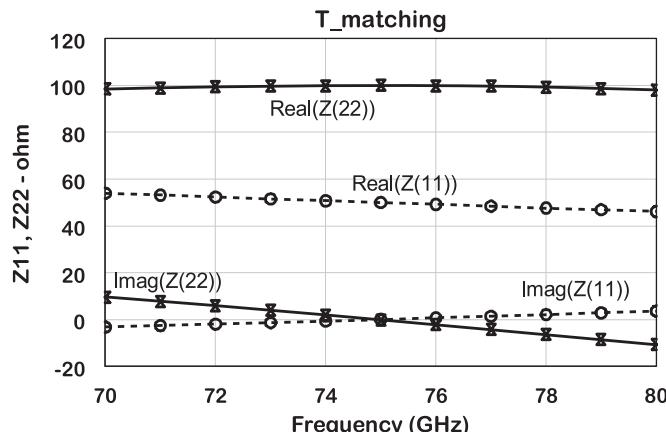
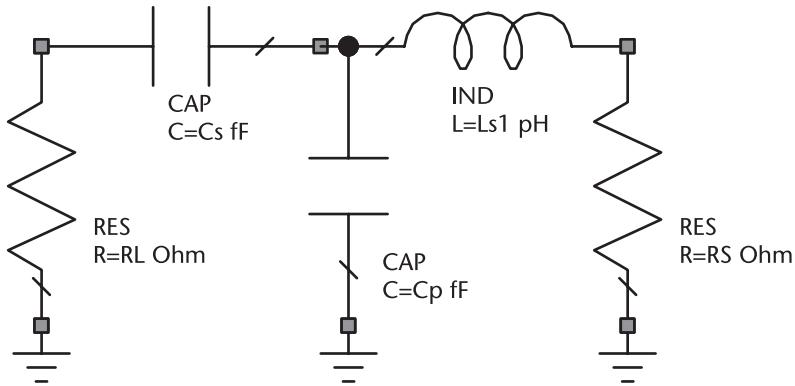


Figure 4.23 Simulation of a T section to match  $100\Omega$  to  $50\Omega$ .



**Figure 4.24** Alternative T cell type.

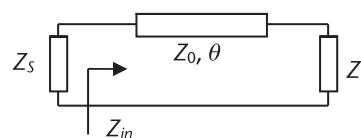
## 4.4 Matching with Distributed Prototypes

At millimeter-wave frequencies, transmission lines are the preferred matching elements, as lumped elements cannot represent the transit time and/or the phase shift of currents and voltages along the elements. If the matching circuits are designed directly with distributed elements, one can skip the step of transforming the lumped to distributed elements. A review is made of the most popular topologies of distributed matching networks employed in MMIC design.

### 4.4.1 Single Line Match

A single transmission line can match a complex load  $Z_L = R_L + jX_L$  to a resistive source,  $Z_S$ , represented in Figure 4.25. That is a very appealing approach for its lower losses. However, there are restrictions, as the application is valid only for some particular load values. The impedance at the transmission line input is given by (4.48). The magnitude of the characteristic impedance  $Z_0$  is expressed in (4.49) and its electrical length  $\theta$  can be extracted from (4.50) [6]. The matching condition is obtained by imposing for  $Z_{in} = Z_S$ .

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \theta}{Z_0 + jZ_L \tan \theta} \quad (4.48)$$



**Figure 4.25** The transmission line parameters.

$$Z_0 = \sqrt{Z_{in} R_L \left( 1 - \frac{X_L^2}{R_L (Z_{in} - R_L)} \right)} \quad (4.49)$$

$$\tan \theta = \left( \frac{Z_0 (Z_{in} - R_L)}{X_L Z_{in}} \right) \quad (4.50)$$

where  $\lambda$  refers to the wavelength propagating in air, where  $\epsilon_r = \mu_r = 1$ ,  $l$  is the length of line (in millimeters) assuming air propagation, and  $\theta$  is the electrical angle,  $\beta l = \frac{\omega l}{c} = \frac{2\pi l}{\lambda} = \frac{2\pi fl}{3 \times 10^{11}}$ .

The single line is only feasible if the number within the square root in (4.49) is greater than 0. Therefore, a single line matching is applicable if they meet either of the criteria below:

$$\left( R_L - \frac{Z_{in}}{2} \right) + X_L^2 < \frac{Z_{in}^2}{4}, \text{ for } Z_{in} > R_L \quad (4.51)$$

$$\left( R_L - \frac{Z_{in}}{2} \right) + X_L^2 > \frac{Z_{in}^2}{4}, \text{ for } Z_{in} < R_L \quad (4.52)$$

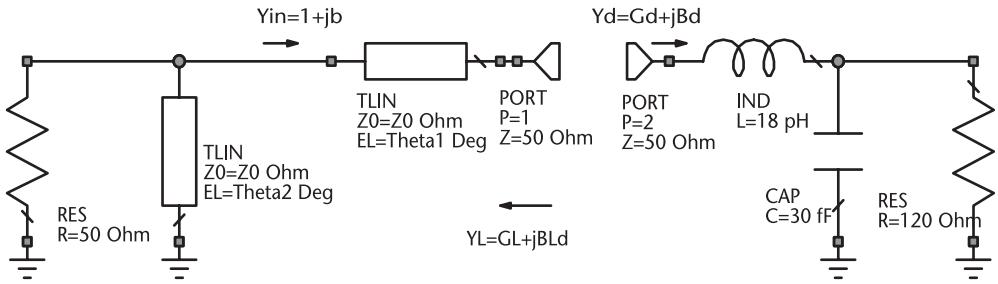
In general, this solution provides narrowband solutions. Except for the particular case of  $\theta = 90^\circ$  in (4.49), which describes the traditional quarter-wavelength transmission line transformer. The input impedance in this case is defined by (4.53). Notice that this element performs impedance transformation between  $Z_{in}$  and  $Z_L$ , being the characteristic impedance of the transformer equal to the geometrical mean of both impedances. Also notice that the transformation causes an inversion in the nature of  $Z_L$ . Thus, if  $Z_L$  is a parallel series resonant element,  $Z_{in}$  will be a parallel resonant element. If  $Z_L$  is a low impedance,  $Z_{in}$  is a high impedance and vice versa.

$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (4.53)$$

#### 4.4.2 Single Stub L Section

The conventional single distributed L-matching network, also known as single stub matching, can present reasonable results. An example in Figure 4.26, depicts the matching of a drain impedance to  $50\Omega$ . Let us start with the normalization of the complex gate admittance  $Y_d = G_d + jB_d$  and disregard the shunt stub for the moment.

The conventional graphic solution consists in starting from the normalized admittance  $y_g$  in the Smith chart. We rotate clockwise along a line of constant  $g_d$  towards the source, until the admittance becomes equal to  $y_{in} = 1 - jb_{in}$ . At that point, we can add a stub with a susceptance  $+jb$  to cancel the imaginary part. The normalization on the Smith chart needs to be 20 mS to obtain a final match to



**Figure 4.26** Schematic of a series line and a short stub matching a drain impedance.

50Ω. The characteristic impedance of the shunt stub is any value that can be built on SiC substrate.

The analytical solution is obtained by imposing the same conditions to the transmission line equation [7]. Therefore, if we make  $Y_{in} = 1/Z_{in}$  to the transmission-line impedance equation, we obtain (4.54). Equating the real part to  $1/Z_0$ , we obtain a second-order degree equation with the tangent as the unknown in (4.55).

$$\begin{aligned} Y_{in} &= G_{in} + jB_{in} \\ &= \frac{R_L(1 + \tan^2 \theta_1)}{Z_0(R_L^2 + (X_L + Z_0 \tan \theta_1)^2)} + j \frac{R_L^2 \tan \theta_1 - (Z_0 - X_L \tan \theta_1)(X_L + Z_0 \tan \theta_1)}{Z_0(R_L^2 + (X_L + Z_0 \tan \theta_1)^2)} \end{aligned} \quad (4.54)$$

$$Z_0(R_L - Z_0) \tan^2 \theta_1 - 2X_L Z_0 \tan \theta_1 + R_L Z_0 - R_L^2 - X_L^2 = 0 \quad (4.55)$$

If the parameter  $R_L = Z_0$ , then the particular condition gives  $\tan(\theta_1) = X_L/2Z_0$ . For  $R_L \neq Z_0$ , the tangent is given by (4.56). There are two solutions for the tangent of angle  $\theta$ . If the tangent is positive, then  $\theta_1 = \tan^{-1}(t)$ . If the tangent is negative, then  $\theta_1 = \pi + \tan^{-1}(t)$ .

$$\tan(\theta_1) = \frac{X_L \pm \sqrt{R_L \frac{(Z_0 - R_L)^2 + X_L^2}{Z_0}}}{Z_0 - R_L} \quad (4.56)$$

The susceptance to be canceled at that point is obtained by entering the tangent value into the imaginary part of (4.54). Notice that the imaginary part is a susceptance and needs to be inverted to obtain the reactance. It is then the designer's choice to use a shunt short or open stub.

An application example for matching the drain circuit is described next, using the drain parameters from Figure 4.26. These parameters are inserted in (4.56), resulting in two solutions for the circuit. The shorter series line provide better bandwidth performance. The first solution is a series line of impedance equal to 50Ω and angle  $\theta_1 = 18.7^\circ$ . The shunt short stub is equal to a line of an impedance of 50Ω and an angle of 39.4°. The load impedance as a function of frequency for this circuit is shown in Figure 4.27. The top traces represent the real part of the

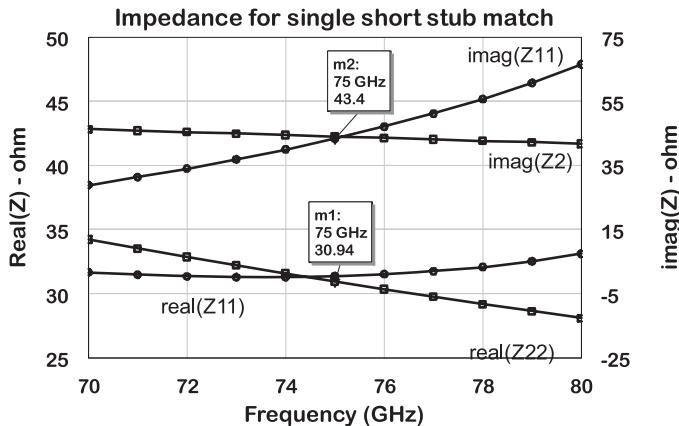


Figure 4.27 Simulation of impedances at ports 1 and 2.

impedance, which crosses each other at the center frequency. The bottom two traces correspond to the reactances. The reactance of the drain circuit was multiplied by  $-1$ . One can see that there is a perfect match near the center frequency, but the performance over frequency is poor. The circuit mismatches are acceptable within the frequency range from 72 to 78 GHz. The parameters for the first and second solutions are shown in Table 4.3.

#### 4.4.3 Three Transmission Lines

One of the simplest matching transmission line matching topologies is the use of three elements: two  $\lambda/8$  lines to resonate the source and load complex impedances and a  $\lambda/4$  line to match the resulting real impedances [8]. Equation (2.23) is used to calculate the impedance for the  $\lambda/8$  lines. An example of the circuit for matching a drain to the gate impedance is in Figure 4.28 at 75 GHz. The circuit parameters are displayed in Table 4.4.

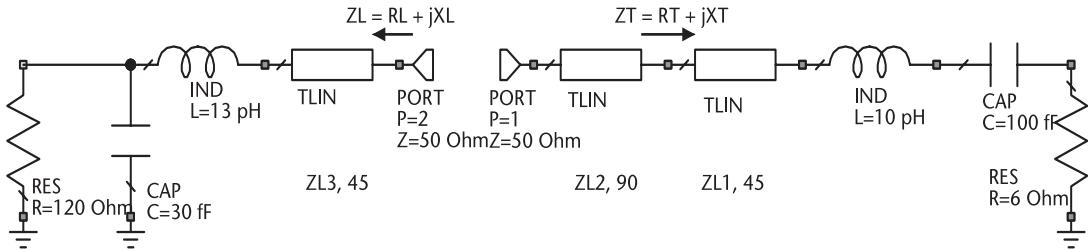
The resulting impedances at ports 1 and 2 are presented in Figure 4.29. The real part of the impedance is matched within 73 to 77 GHz and the reactance is partially compensated within the same range. The imaginary curves are compared with port 1 reactance multiplied by  $-1$ . In spite of limited bandwidth, this simple design is frequently used. There is no restriction on the transformation ratio, when using this approach. Exception is the feasibility of realization on semiconductor substrate, due to width dimensions. The bandwidth of this circuit can be improved with circuit optimization.

Table 4.3 Circuit Parameters for Single Stub Matching

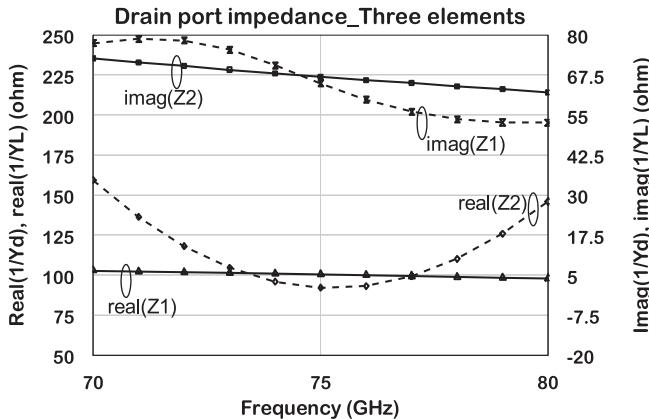
Parameter	Series	Shunt
$Z_0$ ( $\Omega$ )	50	50
$\theta_1$ ( $^\circ$ )	18.6	short 40
$\theta_2$ ( $^\circ$ )	77.4	open 51.6
Frequency (GHz)	75	75

Table 4.4 Circuit Parameters for Three Cascaded Lines

Parameter	Value
$Z_1$ ( $\Omega$ )	18
$Z_2$ ( $\Omega$ )	7.5
$Z_3$ ( $\Omega$ )	57.6
Frequency (GHz)	75



**Figure 4.28** Schematic of a three-line matching network.

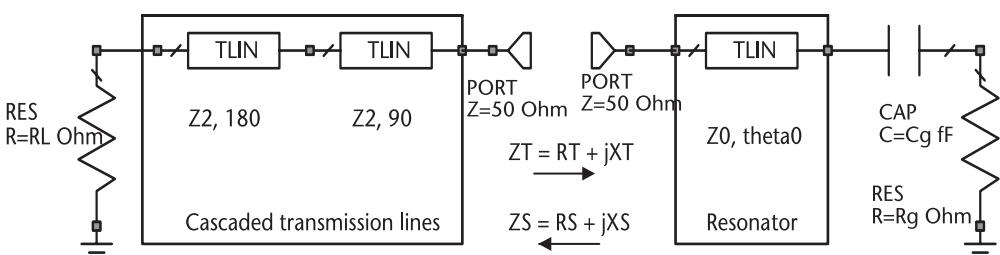


**Figure 4.29** Simulation of impedances at ports 1 and 2 for the three lines' matching.

#### 4.4.4 Selected Matching Topologies

Transmission lines can also be used for compensating the reactance simply by adding a series or parallel resonator to a quarter-wave transformer. Using this technique, four different matching topologies have been reported [9]. The design equations were developed by analytical evaluation of the complex load impedance and the input complex impedance of the matching topology. The four selected topologies are as follows:

**Type A:** In this prototype, we match impedances using a cascade of a quarter-wave transformer, 90°, with a half-wave transformer, 180°. The model is represented in Figure 4.30 for matching a series RLC circuit. In the case of matching a FET gate



**Figure 4.30** Schematic of a Type A distributed network.

to the generator,  $R_g$  corresponds to the gate resistance and  $R_L$  corresponds to an external  $50\Omega$  generator resistance. The resistance  $R_T$  corresponds to the resonated gate impedance. In an ideal RLC series circuit,  $R_T = R_g$ .

In this example, the series inductance is replaced by a short series transmission line, with parameters  $Z_0, \theta_0^\circ$ .  $Z_S$  is the impedance towards the cascade of two transformers terminated by  $R_L$ . At the center frequency,  $R_S = R_T$ . Calculating the derivatives, the Q-factor of  $Z_S$  and  $Z_T$ , and solving the equations, we get the procedure described by (4.57) to (4.60). The first equation calculates the dimension of the quarter-wave transformer,  $Z_1$ , to match  $R_g$  to  $R_L$ . The second equation is a design parameter,  $T$ , defined as a function of  $Q_T$ , the quality factor of the impedance to be matched. The third equation defines the characteristic impedance of the half-wavelength-long line. The slope parameter can be calculated for some simple circuits, but it may be complex to find it analytically. Therefore, it is more straightforward to find it directly by sweeping the impedance over frequency on a linear simulator and calculating the slope. Note that  $Q_T$  follows the polarity of the reactance, so it can be positive or negative. Only positive solutions for  $Z_2$  in (4.60) should be considered:

$$Z_1 = \sqrt{R_T R_L} \quad (4.57)$$

$$T = -\frac{2Q_T}{\pi} - \frac{1}{2} \left( \frac{R_L}{Z_1} - \frac{Z_1}{R_L} \right) \quad (4.58)$$

$$Z_2 = -\frac{TR_L}{2} + \sqrt{\left(\frac{TR_L}{2}\right)^2 + R_L^2} \quad (4.59)$$

$$Q_T = \frac{\omega_0}{2\operatorname{Re}(Z_T)} \left. \frac{d \operatorname{Im}(Z_T)}{d\omega} \right|_{\omega = \omega_0} \quad (4.60)$$

As an example of application, let us transform the gate impedance of a typical unit cell FET, with  $R_g = 5.8\Omega$ , and  $C_g = 220 \text{ fF}$  to  $50\Omega$ . The transmission line resonating the gate measures  $Z_0 = 75\Omega$  and  $\theta_0 = 5.83^\circ$ .  $R_T = 5.74\Omega$  must be transformed to  $R_L = 50\Omega$  and compensates the reactance slope at 95 GHz. The reactance slope is found by plotting  $\operatorname{imag}(Z_T)$  for the FET equivalent input impedance as a function of frequency. Applying (4.61), we obtain a  $Q_T$  factor of 0.29. A positive slope indicates that the circuit is a series RLC. The solution from (4.58) and (4.59) gives  $Z_1 = 17\Omega$  and  $Z_2 = 126\Omega$ . The simulation of S-parameters assumes that the two circuit halves are connected and port 1 is placed at the  $R_L$  terminal, while port 2 is moved to the  $R_g$  terminal. The simulation of insertion and return loss for the two-port circuit is shown in Figure 4.31. The solid line represents the calculated parameters, while the dotted line represents the solution after optimization.

The impedance looking from the  $50\Omega$  node is displayed in the Smith chart in Figure 4.32 for the initial and optimized circuits. The optimized solution trades off perfect match at the center frequency, with an average match within the band. The new circuit values for the optimized network are  $Z_1 = 19\Omega$  and  $Z_2 = 94\Omega$ .

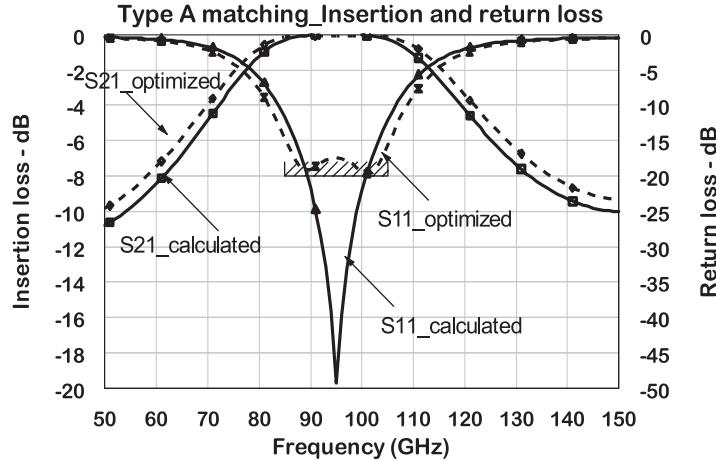


Figure 4.31 Type-A insertion and return loss.

*Type B:* The model is represented in Figure 4.33 for matching  $R_d$  to a load  $R_s$ . The resistor  $R_d$  is part of a parallel RLC circuit. The inductance for resonating the shunt capacitance is achieved by a transmission line with parameters  $Z_0$ ,  $\theta_0^\circ$ , resulting at the resonance frequency  $R_T = R_d$ . The impedance matching at the center frequency is achieved with a quarter-wave transformer, (4.57). The reactance slope parameter is extracted from Figure 4.34. The reactance compensation element is implemented with a transmission line in shunt with the load, with characteristic impedance  $Z_2$ , (4.61). When considering the sign of  $Q_T$ , notice that  $Z_2$  must be positive.

$$Z_2 = \frac{\pi Z_1 R_s^2}{\pi Z_1^2 - \pi R_s^2 - 4 Q_T Z_1 R_s} \quad (4.61)$$

The example of application with regard to the matching of the drain impedance of a typical FET. The device parameters are  $C_d = 30 \text{ fF}$  and  $R_d = 118 \Omega$ , and

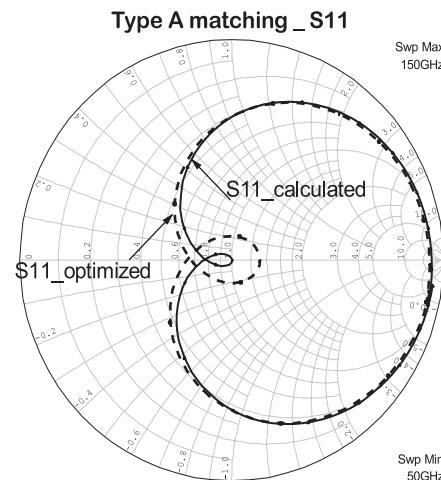


Figure 4.32 Type-A  $S_{11}$  from  $50\Omega$  node.

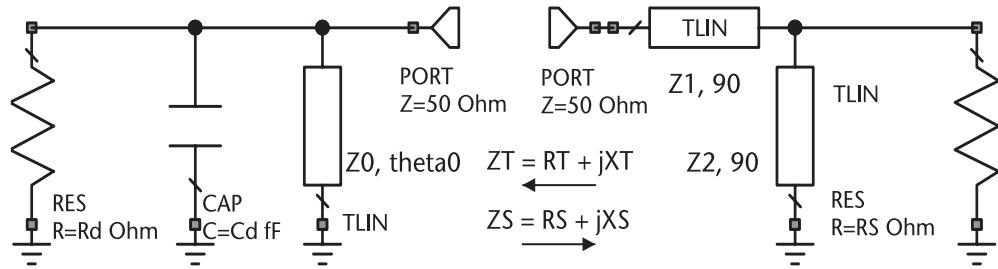


Figure 4.33 Transmission-line circuit for type B.

the frequency of operation is 95 GHz. The shunt transmission line resonating the drain measures  $Z_0 = 75\Omega$  and  $\theta_0 = 36.8^\circ$ . The other design parameters are  $\text{Re}(Z_T) = 118\Omega$  and the quality factor,  $Q_T = -2.4$ .

Taking those values to (4.58) and (4.61), we obtain  $Z_1 = 13\Omega$  and  $Z_2 = 76.8\Omega$ . The simulation of insertion and return losses are obtained by moving ports 1 and 2 to  $R_d$  and  $R_s$  nodes, respectively. Notice that  $R_d$  and  $R_s$  are suppressed for this evaluation. The results are depicted in Figure 4.35, which shows two set of results. The first result, represented by a solid line, corresponds to the calculated parameters and the second, represented by a dotted line, corresponds to the optimized circuit. Figure 4.36 shows the  $S_{11}$  trace on the Smith chart. The optimized circuit enlarged the bandwidth for insertion and return losses, even with a reduction of the center frequency return loss. The new circuit values for the optimized network are  $Z_1 = 17\Omega$  and  $Z_2 = 70\Omega$ .

**Type C:** The impedance matching is achieved with the cascade of two quarter-wave transformers, as depicted in the schematic of Figure 4.37. The first transformer connected to port 1 has a characteristic impedance defined by  $Z_{01}$  and the second transformer has a characteristic impedance defined by  $Z_{02}$ . On the right is the complex impedance to be matched: gate or drain. There are restrictions on the use of this type of network. If the resonated gate impedance is below  $10\Omega$ ,  $Z_{01}$  goes below

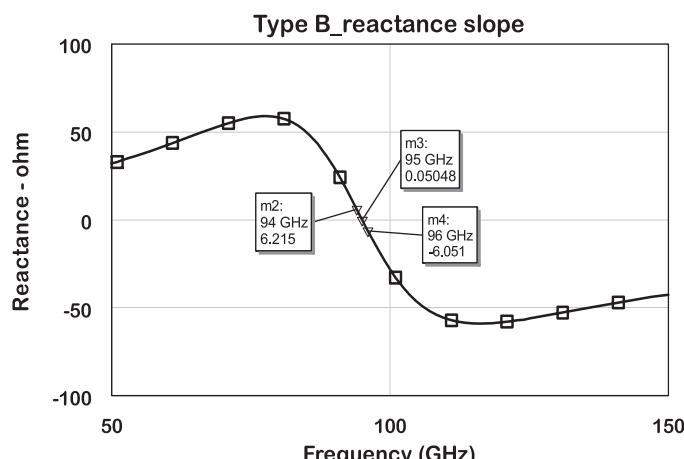


Figure 4.34  $\text{Imag}(Z_T)$  function of frequency for the reactance slope calculation.

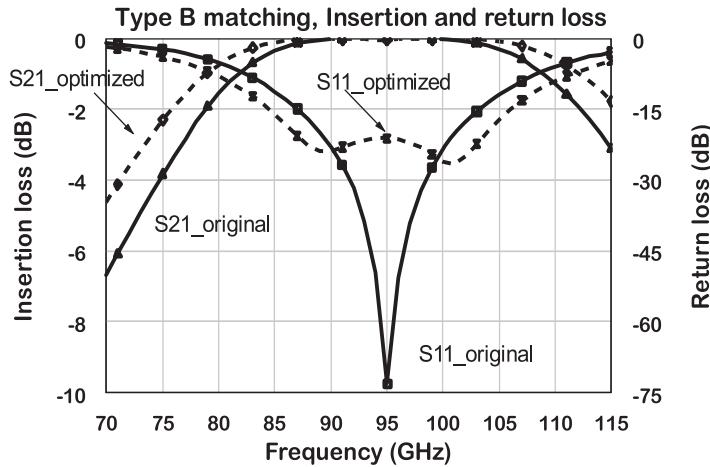


Figure 4.35 Type-B insertion and return loss.

$12\Omega$ , which is not easy to match on MMIC. If the resonated drain impedance is higher than  $60\Omega$ , the characteristic impedances of the matching network will be above  $70\Omega$ , which is also not feasible in MMIC. Frequently, the gate impedance has to be prematched with a shunt element to raise the impedance level, and the drain impedance has to be prematched with a series transmission line in order to lower the impedance.

The procedure in this case is described by (4.62) to (4.65).  $A$  and  $B$  are the intermediate parameters for the design. The example shows the matching for a series RLC impedance but it applies equally to a parallel RLC. The difference affects parameter  $B$  concerning the sign of  $Q_T$ , which is positive for a series circuit and negative for a parallel circuit. Only the positive solutions for  $B$  in (4.64) are valid.

$$Z_2 = BR_L \quad (4.62)$$

$$Z_1 = AZ_2 \quad (4.63)$$

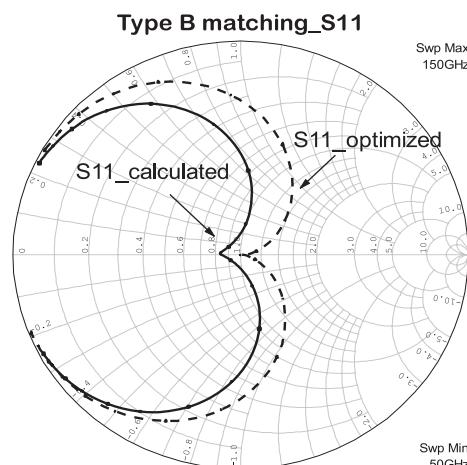


Figure 4.36  $S_{11}$  in the Smith chart.

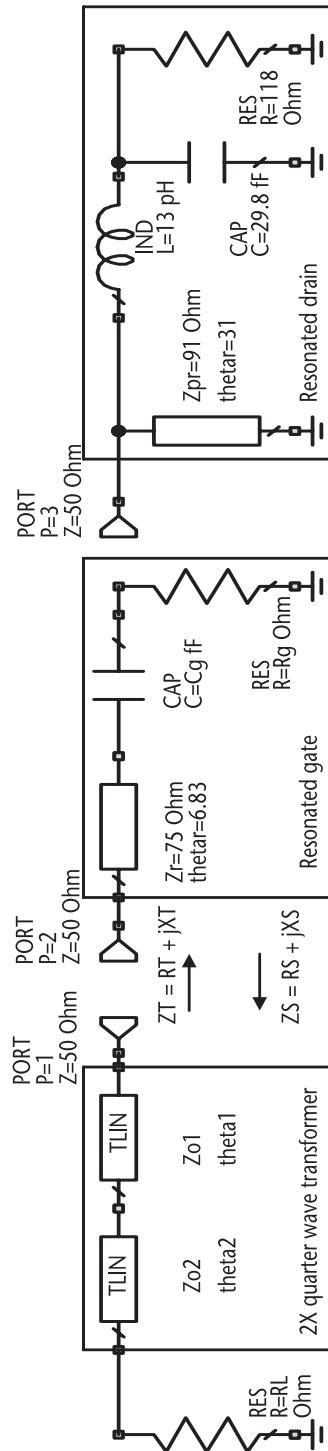


Figure 4.37 Transmission line circuit with a Type-C match.

$$B = \frac{A}{1+A} \left\{ -\frac{2}{\pi} Q_T + \sqrt{\left(\frac{2}{\pi} Q_T\right)^2 + \frac{(1+A)^2}{A}} \right\} \quad (4.64)$$

$$A = \sqrt{\frac{\text{Re}(Z_T)}{R_L}} \quad (4.65)$$

With  $\theta_1 = \theta_2 = \pi/2$ .

Let us investigate the application of these equations to match the gate and the drain impedance of a FET to  $50\Omega$ . The gate circuit is defined by  $R_g = 6\Omega$ ,  $C_g = 0.22\text{ pF}$ ,  $L_g = 10\text{ pH}$ , and a series resonant line with characteristic impedance of  $76.8\Omega$  and an electrical angle of  $5.83^\circ$ . The drain circuit is defined by  $R_d = 118\Omega$ ,  $C_d = 30\text{ fF}$ ,  $L_d = 12\text{ pH}$ , and a shunt resonating stub of characteristic impedance equal to  $77\Omega$  and electrical length of  $25^\circ$ . The center frequency of operation is 95 GHz. The gate series quarter-wave transformers are  $Z_{01} = 8\Omega$ ,  $Z_{02} = 22\Omega$  and  $R_T = 8\Omega$ ,  $Q_T = 2$ . The drain quarter-wave transformers are  $Z_{01} = 129\Omega$ ,  $Z_{02} = 105\Omega$  and  $R_T = 6\Omega$ ,  $Q_T = -2$ . We performed the simulation of these options with unrealizable transmission lines in MMIC to verify the matching properties. The simulated insertion and return losses for the gate matching circuit are shown in Figure 4.38, and the performance for the drain matching is shown in Figure 4.39.

All these circuits are calculated for an optimum match at the center frequency, resulting in a tuned return loss. If we allow the return loss to be better than 20 dB within the band, the circuit parameters can be optimized to improve the return loss bandwidth. This optimization is depicted in the dotted line for the drain circuit.

**Type D:** The schematic of this type of network is shown in Figure 4.40 for matching a resistance  $R_g$  to  $R_L$ . At the center frequency of operation, a quarter-wave transformer of impedance  $Z_1$  is used. The reactance compensation is carried out by shunting two stubs one short and one open, with the same characteristic impedance,  $Z_2$ . The design equations start with (4.58) for the quarter-wave transformer.

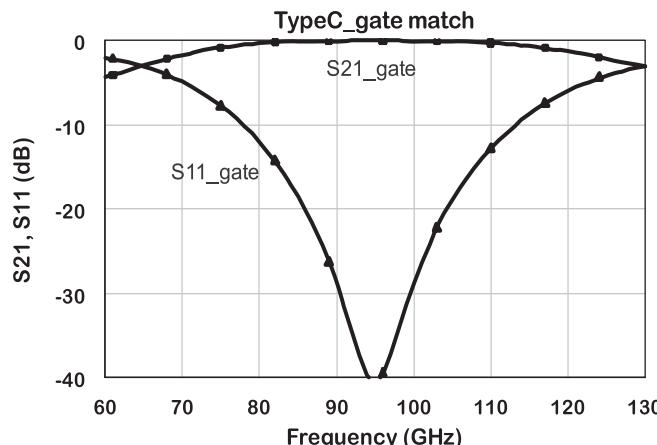


Figure 4.38 Type-C gate performance.

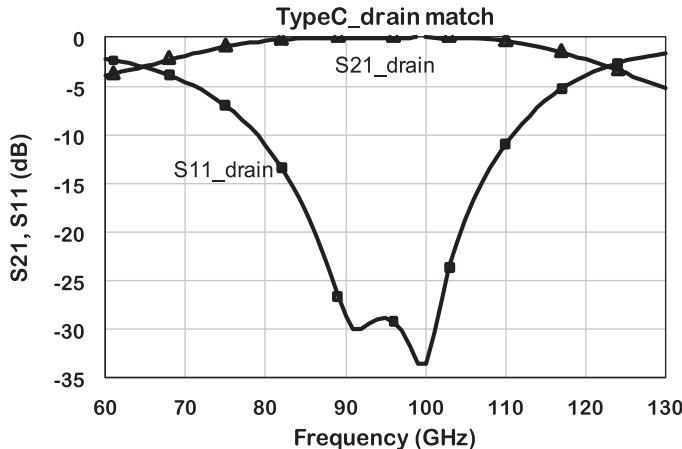


Figure 4.39 Type-C drain performance.

The remaining equations are (4.68) and (4.67). Only positive solutions for  $Z_1$  in (4.70) should be considered.

$$T = \frac{2}{\pi \cos^2 \theta_1} (\theta_1 + \theta_2) \quad (4.66)$$

$$Z_2 = \frac{T Z_1^2}{Z_0} \frac{1}{\left( \frac{R_L}{Z_1} - \frac{Z_1}{R_L} \right) + \frac{4Q_T}{\pi}} \quad (4.67)$$

with  $(\theta_1 + \theta_2) = n\pi/2 \rightarrow n = 1, 3$

$\theta_1, \theta_2$  in radians.

This option has more variable options, so it can match a broader range of impedances. Selecting  $n = 1$ , this option provides quite a narrow band compared to the previous types. For  $n = 3$ , the bandwidth can be adjusted to be larger. The insertion loss performance for matching a gate impedance,  $R_g = 5.8\Omega$  and  $C_g = 220\text{ fF}$ , is shown in Figure 4.41 and the return loss is shown in Figure 4.42.

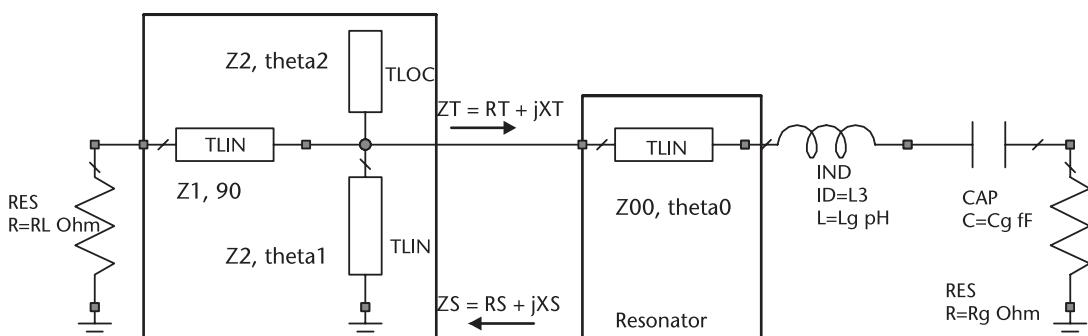


Figure 4.40 Matching of gate circuit with a Type-D network.

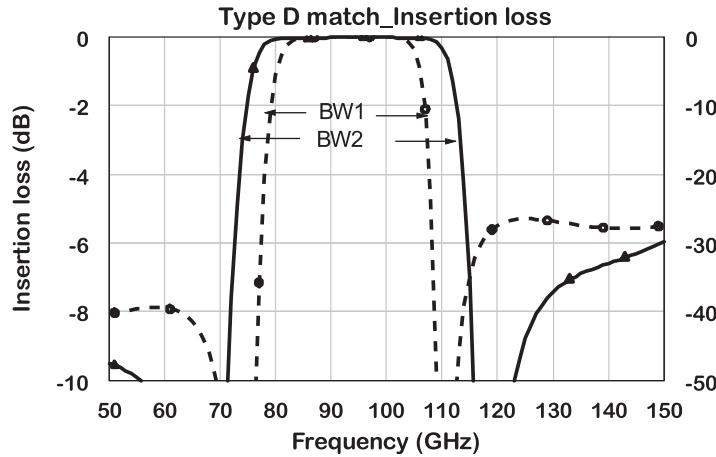


Figure 4.41 Type-D insertion loss.

The transmission-line parameters to resonate the gate capacitance at 95 GHz are  $\theta_0 = 5.5^\circ$  and  $Z_0 = 80\Omega$ . The simulations show two sets of design parameters. In the first parameter, the selected angles are  $\theta_2 = 115^\circ$  and  $\theta_1 = 155^\circ$ , and the calculated characteristic impedances are  $Z_1 = 17\Omega$  and  $Z_2 = 27\Omega$ . This response is identified by the dotted line in the figures. In the second set,  $\theta_2 = 125^\circ$  and  $\theta_1 = 145^\circ$ , and the calculated characteristic impedances are  $Z_1 = 17\Omega$  and  $Z_2 = 20\Omega$ . The response for this option is laid out as solid line curves in the figures, and it can be noticed the increase in bandwidth.

One of the drawbacks of this option is the out-of-band response. It can be seen that the return loss may become positive in an active circuit at 70 GHz, due to the effect of the short shunt stub and at 115 GHz due to the open stub. The short stub effect at 70 GHz can be taken care of by using a capacitor to short-circuit the stub instead of a real short to the ground. The open stub affects the response at higher frequencies where gain is lower. However, a negative resistance may show up in a frequency range between the device  $f_T$  and  $f_{max}$ .

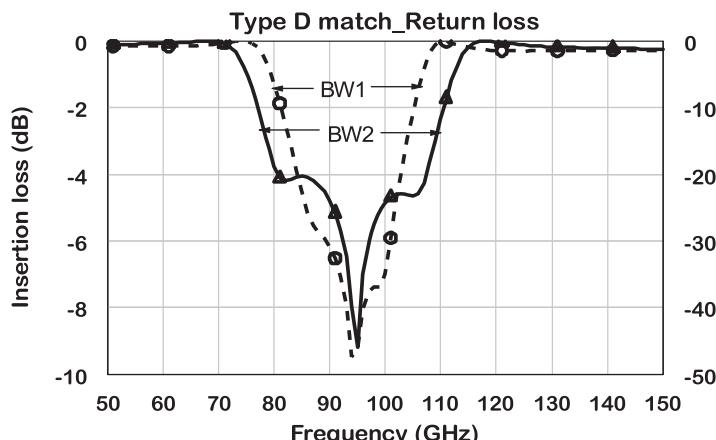


Figure 4.42 Type-D return loss.

## 4.5 Network Frequency Bandwidth

It is difficult to accurately predict the bandwidth of matching circuits with so many variables. The simple equation below is derived for a tuned circuit where bandwidth is taken to be at a 3-dB point. We are interested in bandwidths at the 1-dB point or less, which means that the bandwidth will be lower than the value predicted by (4.7). For a flat band, a better approximation is obtained by dividing  $\Delta f$  from that equation by a factor of 2.

$$\Delta f = \frac{f_0}{2Q} \quad (4.68)$$

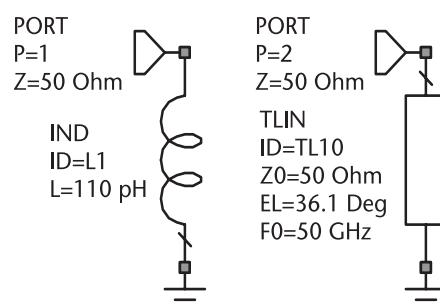
To verify the accuracy of this equation, let us consider the drain equivalent circuit of Figure 4.33 operating at a center frequency of 95 GHz. The  $Q_T$  for that circuit is 2.4, resulting in a bandwidth  $\Delta f = 20$  GHz. The plot in Figure 4.35 shows that the bandwidth for a 1-dB insertion loss relative to the center frequency is indeed close to 20 GHz. In an amplifier, there is a cascade of matching networks and transistor stages. The amplifier bandwidth in this case would be given by the network with the narrower bandwidth.

## 4.6 Conversion from Lumped to Distributed Elements

There is no general method to convert lumped elements to distributed equivalents, and the equivalence in terms of impedance is never ideal. One may have to make approximations and use circuit optimization routines to obtain a true conversion.

### 4.6.1 Shunt Stubs

The conversion equation to transform a shunt lumped inductor into a shunt short stub is given by (4.69) and the schematic representation is in Figure 4.43. For angles less than 30°, the tangent can be replaced by the angle in radians.



**Figure 4.43** Shunt stub and lumped inductance.

$$Z_{in} = j\omega L = jZ_0 \tan(\theta) \quad (4.69)$$

A lumped inductor of 110 pH is compared to a  $50\Omega$  transmission line with an electrical angle of  $36^\circ$  at the frequency of 50 GHz. Figure 4.44 shows the reactance of both components from 1 to 100 GHz. A good agreement is obtained up to nearly 50 GHz. Above that frequency, the tangent law prevails: the reactance is still positive, but it does not follow the lumped element behavior.

The conversion of a short transmission lines to a lumped capacitor connected to ground is obtained through (4.70). The circuit representation is shown in Figure 4.45.

$$Y_{in} = j\omega C = jY_0 \tan(\theta) \quad (4.70)$$

The susceptance in Figure 4.46 shows that the lumped capacitor can be replaced by an open stub up to 60 GHz for the parameter values shown in the figure. Hence, there is a range for the validity of equivalency between open stub and a capacitor, similar to that observed for the inductor and a short stub.

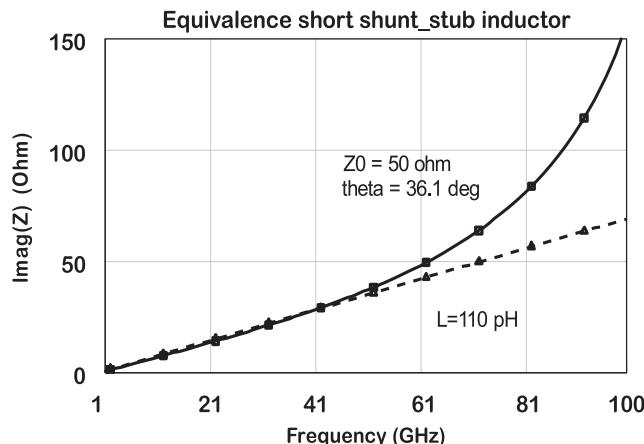


Figure 4.44 Shunt stub compared to lumped inductance.

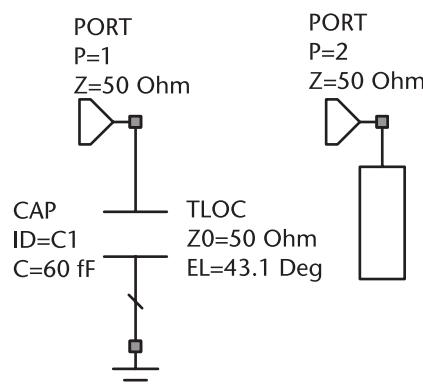
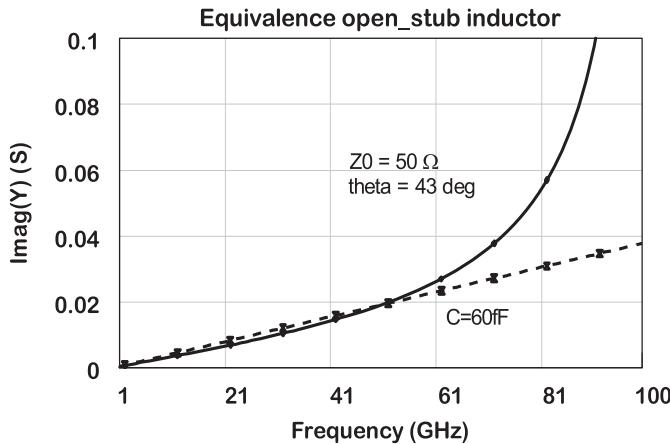


Figure 4.45 Shunt stub and lumped capacitance.



**Figure 4.46** Shunt stub compared to lump capacitance.

#### 4.6.2 Transmission Line

The next important conversion is the replacement of LC matching networks by transmission lines. Instead of converting a single inductor or capacitor, a better solution is to convert a PI or T cell to the transmission line. An elegant solution to this problem, proposed in [10], is to compare the transmission matrix of a lumped network with the transmission matrix of a transmission line. The LC elements are then first converted to  $L'$ ,  $C'$  given by (4.71) and (4.72) for a T section. Then the converted transmission-line electrical length and characteristic impedance can be obtained from (4.73) and (4.74). The reverse conversion, that is, transformation from transmission lines to lumped elements are given by (4.75) and (4.76).

$$L' = \frac{L}{1 - \omega^2 LC} \quad (4.71)$$

$$C' = \frac{C}{1 - \omega^2 LC} (2 - \omega^2 LC) \quad (4.72)$$

$$Z_0 = \sqrt{\frac{L'}{C'}} \quad (4.73)$$

$$\tan \theta = \omega \sqrt{L'C'} \quad (4.74)$$

$$\omega L = Z_0 \sin \theta \quad (4.75)$$

$$\omega C = Y_0 \frac{\sin \theta}{1 + \cos \theta} \quad (4.76)$$

Equations (4.77) and (4.78) are applicable to a PI section. The electrical angle,  $\theta$ , and the characteristic impedance have same definition used in the T section, (4.74) and (4.75). The reverse relationship is in (4.79) and (4.80).

$$L' = \frac{L'}{1 - \omega^2 LC} (2 - \omega^2 LC) \quad (4.77)$$

$$C' = \frac{C}{1 - \omega^2 LC} \quad (4.78)$$

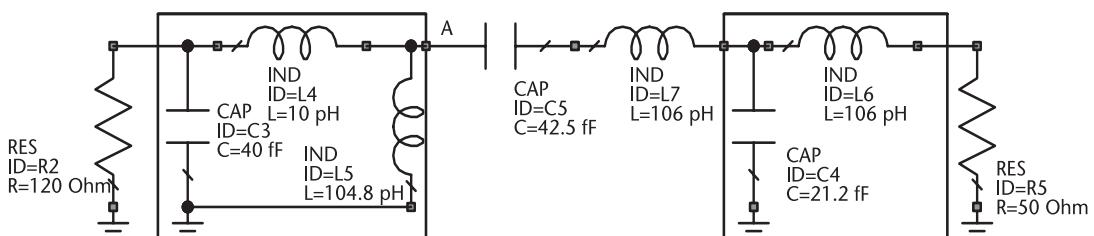
$$\omega L = Z_0 \frac{\sin \theta}{1 + \cos \theta} \quad (4.79)$$

$$\omega C = Y_0 \sin \theta \quad (4.80)$$

An application example for the transformation of a lumped network is used to match a drain impedance to a  $50\Omega$  load. Let us use the schematic shown in Figure 4.9 to transform a drain impedance to  $50\Omega$ . The drain impedance is resonated with a shunt inductor and a single L cell completes the match. The first step was to transform the single L network into a lowpass T-network, by adding an extra inductance as shown in Figure 4.47. A series capacitor is then added to resonate the added series inductor. At the center frequency of operation, the added LC series resonant circuit has no influence in the port impedances.

The final circuit in Figure 4.48 shows the T-section was first transformed into an  $L'$ ,  $C'$  and then used to generate the characteristic impedance and electrical length of the correspondent transmission line. The resonant inductor was replaced by a stub shorted to the ground.

The performance of the converted circuit is presented in Figure 4.49 for the insertion and return loss parameters. The impedance traces at ports 3 and 4 are shown in Figure 4.50. The converted circuit is able to maintain performance within the 70 to 80-GHz band with a return loss of 14 dB.



**Figure 4.47** Procedure for converting lumped network to equivalent distributed network.

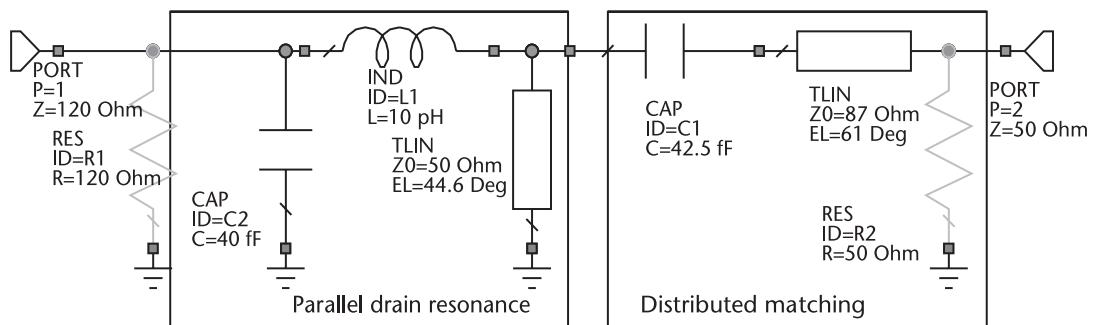


Figure 4.48 Schematic of distributed circuit converted from lumped elements.

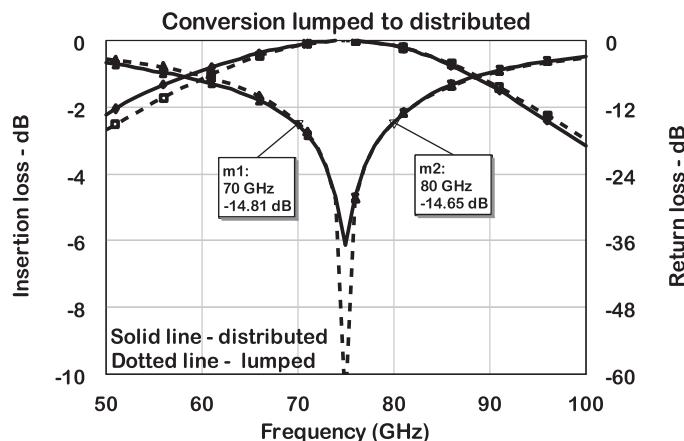


Figure 4.49 Transmission coefficients.

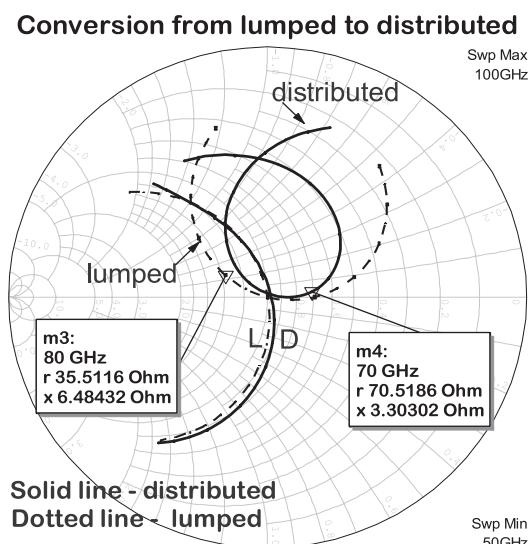


Figure 4.50 Impedance parameters.

## 4.7 Capacitive Loaded Transmission Line

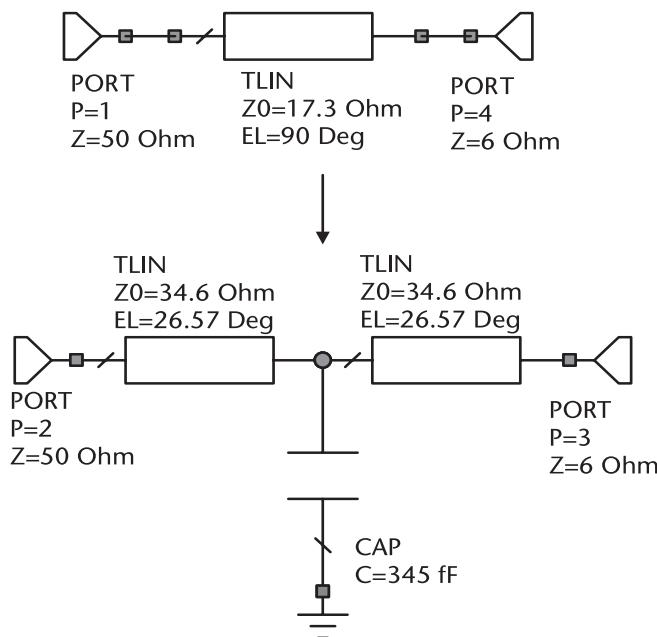
A useful type of equivalence is the replacement of a quarter-wavelength line by two shorter lines with a shunt capacitor in between. That is also a way to increase the characteristic impedance of the original transmission line. Due to the inversion properties of quarter-wavelength lines, it can also be used as an impedance inverter. Let us convert a regular quarter-wave line ( $\theta = 90^\circ$ ) to a capacitive loaded line, described by (4.81) to (4.83).

$$\lambda = \frac{Z_0}{Z_{01}} \leq 1 \quad (4.81)$$

$$\omega C = 2Y_0 \frac{1 - \lambda^2}{2\lambda} \quad (4.82)$$

$$\theta_1 = \frac{1}{2} \cos^{-1} \left( \frac{1 - \lambda^2}{1 + \lambda^2} \right) \quad (4.83)$$

The schematics for the original quarter-wave transformer and for the capacitive loaded transmission line to transform  $6\Omega$  to  $50\Omega$  at the frequency of 20 GHz are shown in Figure 4.51. The quarter-wave transmission-line characteristic impedance is  $17.3\Omega$ . Due to the restriction,  $\lambda < 1$ , the new characteristic impedance must be



**Figure 4.51** Schematic of capacitive loading.

higher than the original. It was decided to double its value. The parameters of the modified circuit are then two lines with  $\theta = 26.56^\circ$ ,  $Z_0 = 34.6\Omega$ , and a loading capacitor of 0.345 fF. Thus, the total length of line was reduced from  $90^\circ$  to  $53^\circ$ . The plots in Figure 4.52 show  $S_{11}$  and  $S_{22}$  for a quarter-wave transformer in the solid line and for the capacitive loaded line in the dotted line. They show the same impedance at the center frequency of operation and are slightly different within a 10% bandwidth. This may be improved with optimization.

## 4.8 Impedance Inverters

An impedance or admittance inverter transforms a series resonant into a parallel resonant circuit and vice versa [11]. There are two general types of inverters:  $K$ , where a series circuit is transformed into parallel, or  $J$ , where a parallel circuit is transformed into series (Figure 4.53). The implementation with quarter-wave transformers is shown in the figure, and the  $K$  and  $J$  parameters are defined by (4.84) and (4.85), respectively. The constants  $K$  and  $J$  are equal to the characteristic impedance and admittance of the quarter-wave transformers. The interesting property for this element is to transform a circuit containing open and shorted stubs in one with all stubs open or shorted to ground. The parameters  $Y_p$  and  $Z_s$  in the figure correspond to the admittance of the parallel-inverting element and the impedance of series inverting element, respectively.

$$K = \sqrt{\frac{L}{C_1}} \quad (4.84)$$

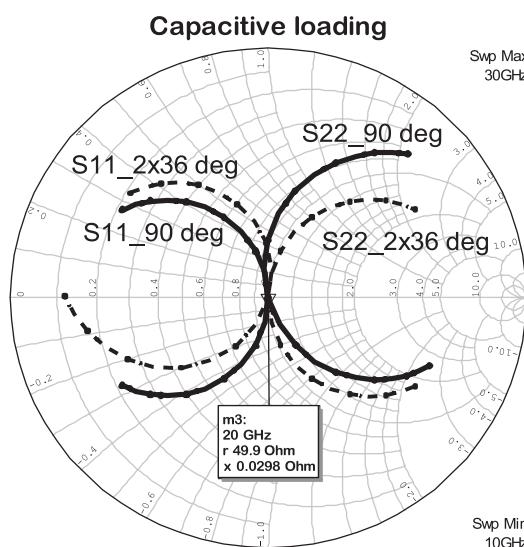
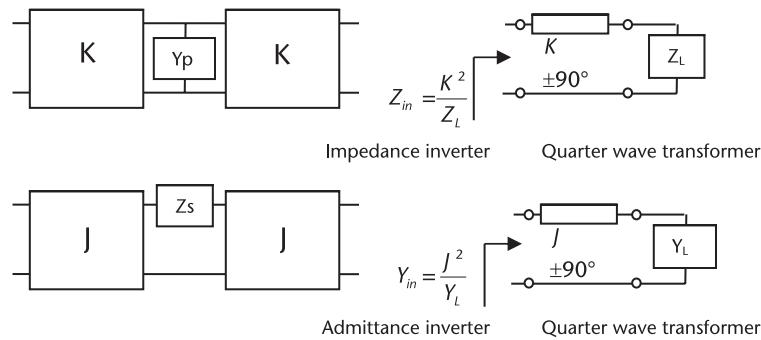


Figure 4.52 Impedances on the Smith chart.

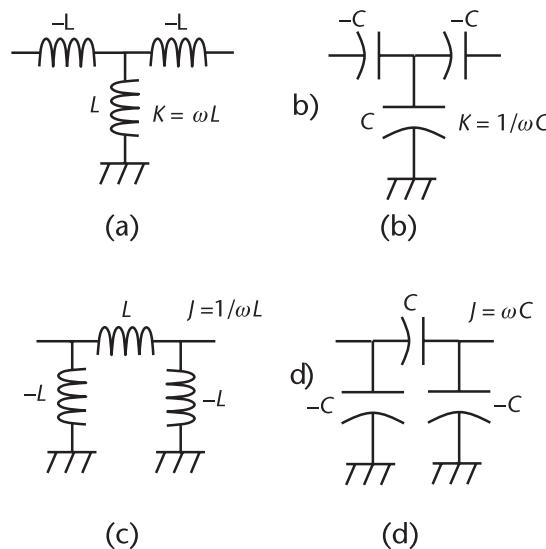


**Figure 4.53** Impedance and admittance inverters. (After: [11]. © 2001 IEEE.)

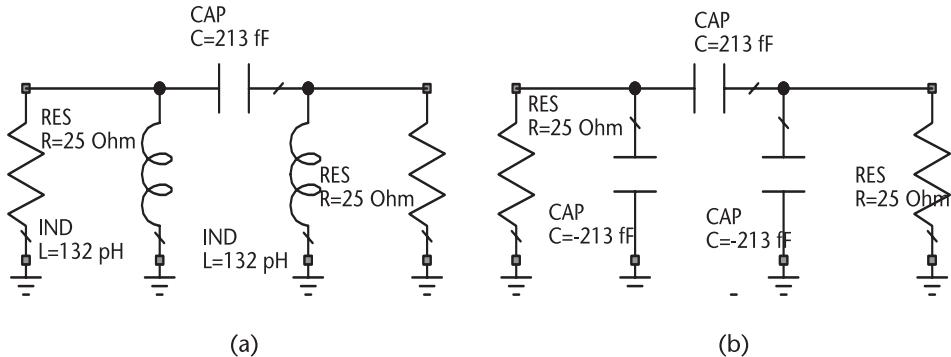
$$J = \sqrt{\frac{C}{L_1}} \quad (4.85)$$

The implementations of impedance inverters with T and PI inductors and capacitors circuits are shown in Figure 4.54. Any of these options with similar reactances and input/output impedances will perform like a matched  $50\Omega$  transmission line.

The input impedance of any of these options is similar to a quarter-wave transformer. It does a similar transformation and inserts a phase shift of  $90^\circ$  at the center frequency of operation. Also, the interest of lumped element transformer is to replace quarter-wave transmission lines in order to minimize the area on the MMIC. The most popular of these applications is the use of series capacitor inverter, J-type, and the shunt inductor inverter, K-type. Let us start with an example of a J-inverter. We started with a highpass PI cell, where the inductor reactances and capacitors are all equal to  $25\Omega$ , as shown in Figure 4.55(a). The equivalent inverter is in Figure



**Figure 4.54** Lumped element inverter. (After: [11]. © 2001 IEEE.)



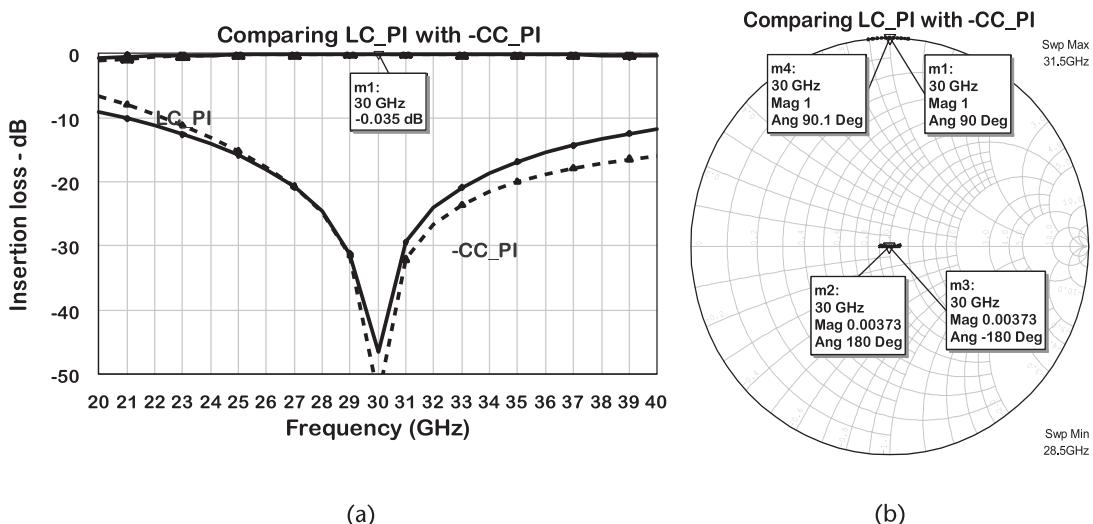
**Figure 4.55** Lumped element PI representation of a quarter-wave transformer: (a) high-pass PI cell, and (b) high-pass with negative parallel capacitors.

4.55(b), with all capacitors of equal value. The insertion loss for both circuits is in Figure 4.56(a), while the transfer phase is in Figure 4.57(b). Notice that both rotate the phase by  $90^\circ$  at the center frequency.

As an example of application, let us consider the circuit in Figure 4.57 to match a gate impedance to the drain, at a frequency of 30 GHz. The impedance at ports 1 and 2 for this circuit is in the Smith chart of Figure 4.58(a). Notice that both circuits have the same parallel RLC behavior, creating a conflict.

The negative capacitive inverter is equal to the resonated value at ports 1 and 2, equal to  $R_T = 24\Omega$ . Making the capacitor reactance equal to  $R_T$ , one finds a value of 221 fF.

Adding a  $-C$ ,  $C$  PI section in cascade with port 2, one finds the impedance curves in Figure 4.58(b). The absorption of negative capacitors by the neighboring elements is a relatively easy task if the element is a shunt open or short reactance.



**Figure 4.56** Impedance of  $L$ ,  $C$  PI-section and of  $-C$ ,  $C$  PI section: (a) insertion loss for the LC and  $-CC$  circuits, and (b) transfer phase for both circuits.

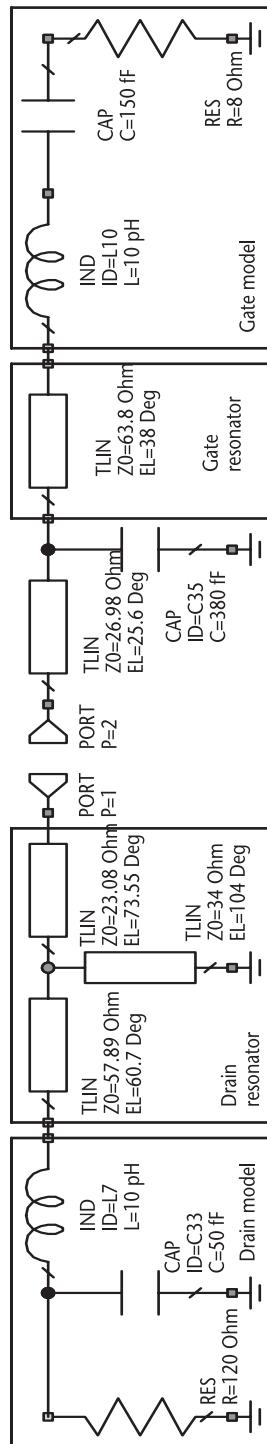
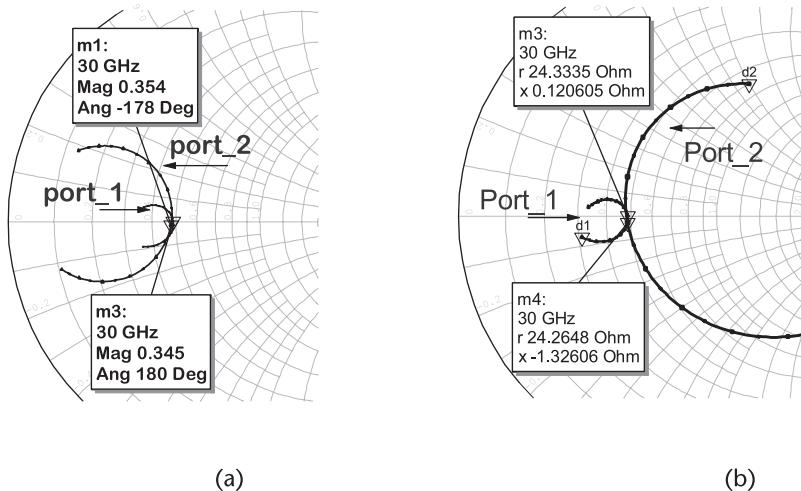


Figure 4.57 Distributed element matching with one shunt capacitor.



**Figure 4.58** Impedances for ports 1 and 2, with and without an inverter: (a) impedance of port 1 equal to port 2, and (b) port 1 conjugated with port 2.

However, if it is a series transmission line, the process becomes a bit more complicated. It may be needed to recalculate the complete circuit.

A faster alternative is to disregard the negative capacitors, retain the series positive capacitor, and reoptimize the complete circuit, maintaining the capacitive inverter constant. That is the approach followed to derive the capacitive inverter circuit in Figure 4.59.

In the same figure, a circuit with a quarter-wave inverter was designed to compare the differences between both circuits. The evaluation of these two approaches is illustrated in Figure 4.60, considering the insertion and return losses. There are differences within the band, which can be absorbed by the other matching elements.

The capacitor version shows a broader band compared to the transformer, with respect to return loss. Notice that the circuit with the capacitor inverter is about  $131^\circ$  shorter.

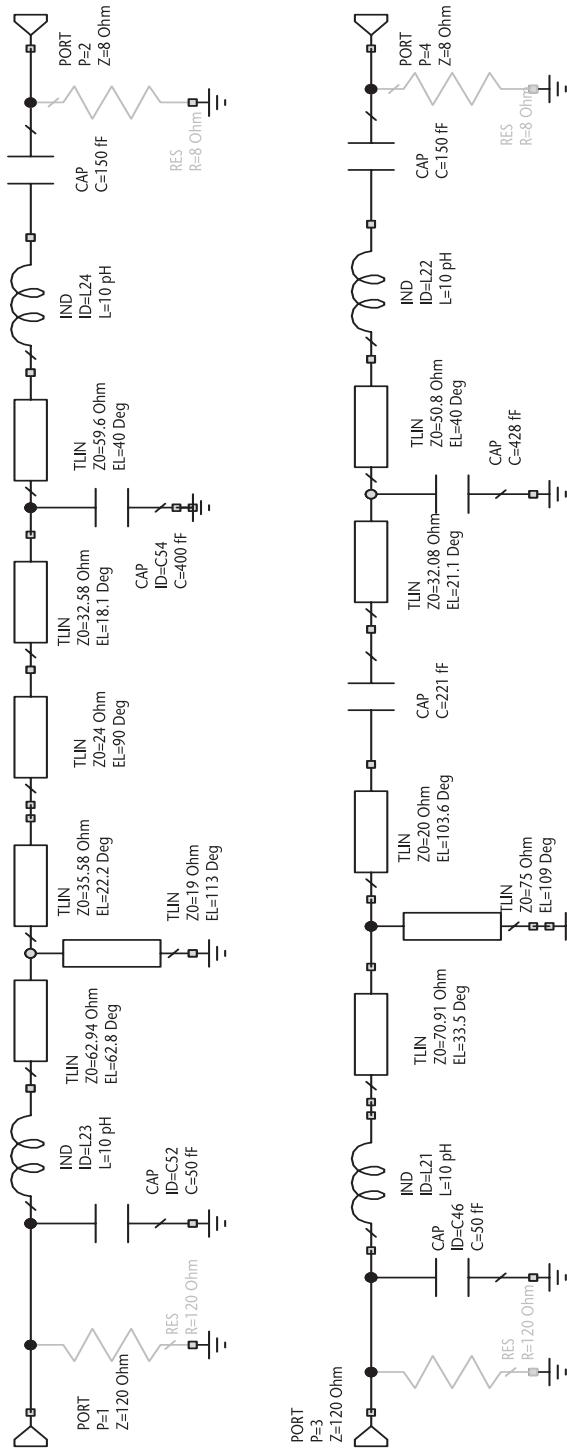
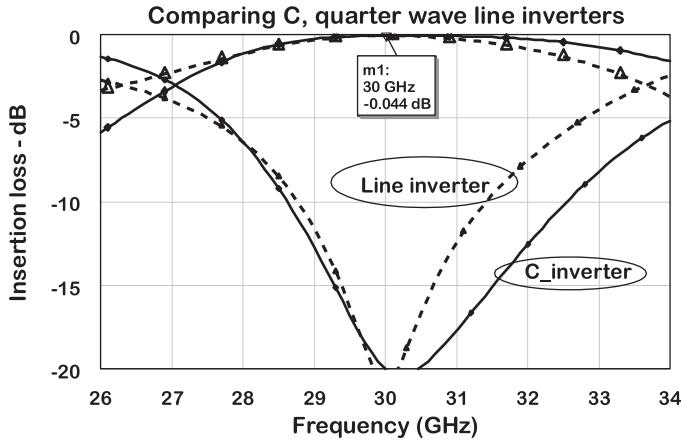


Figure 4.59 The top circuit uses a quarter-wave inverter and the bottom circuit uses a capacitor inverter.



**Figure 4.60** Comparing matching with transformer inverter and capacitive inverter.

## 4.9 Equalizers

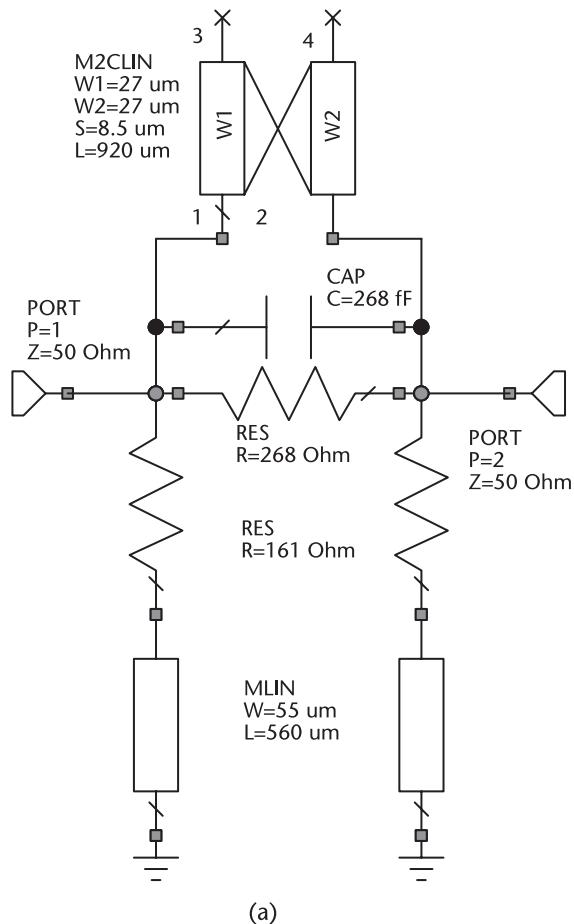
Equalizers are circuits designed to level the gain of an amplifier. In general, this function is part of the amplifier matching circuits. However, in certain cases, the amplifier is already designed except for the negative gain slope. In such a case, this circuit is adequate to level the gain. A resistor in series with a 90° shorted transmission line in shunt with the main signal introduces a positive slope. That circuit is effective to equalize circuits operating at large frequency band.

In the case of narrow band, this element can correct no more than 1 dB of slope. The equalizer in Figure 4.61(a), based on the work of Mellor [12], is effective for bandwidths in the range of 15% to 20%.

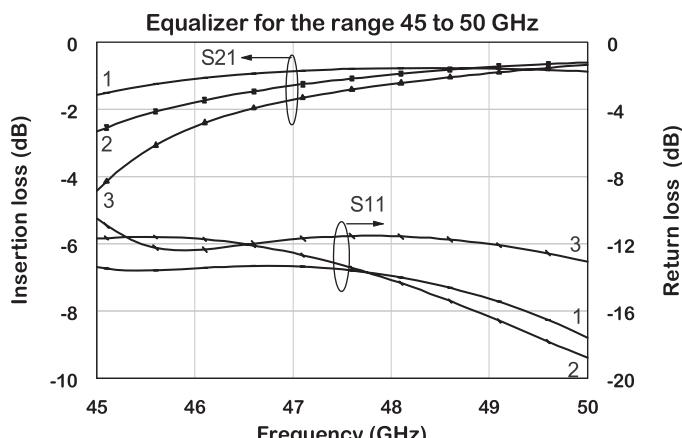
Three different circuits for different attenuation levels were simulated. The parameters are shown in Table 4.5, and the plot of insertion and return loss versus frequency is shown in Figure 4.61(b). Curve 1 shows about 0.7 dB of equalization, curve 2 shows about 2 dB of equalization, and curve 3 shows nearly 4 dB of equalization. The return loss is better than 10 dB.

**Table 4.5** Parameters for Three Different Circuits

Parameters	Circuit 1	Circuit 2	Circuit 3
W <sub>1</sub> (μm)	27	27	27
W <sub>2</sub> (μm)	57	57	57
L <sub>1</sub> (μm)	920	920	920
L <sub>2</sub> (μm)	585	630	560
S <sub>1</sub> (μm)	14	8.9	6.5
C <sub>1</sub> (fF)	192	268	268
R <sub>1</sub> (Ω)	190	244	268
R <sub>2</sub> (Ω)	133	133	161



(a)



(b)

**Figure 4.61** Schematic of the proposed equalizer: (a) schematic of the equalizer, and (b) insertion and return loss.

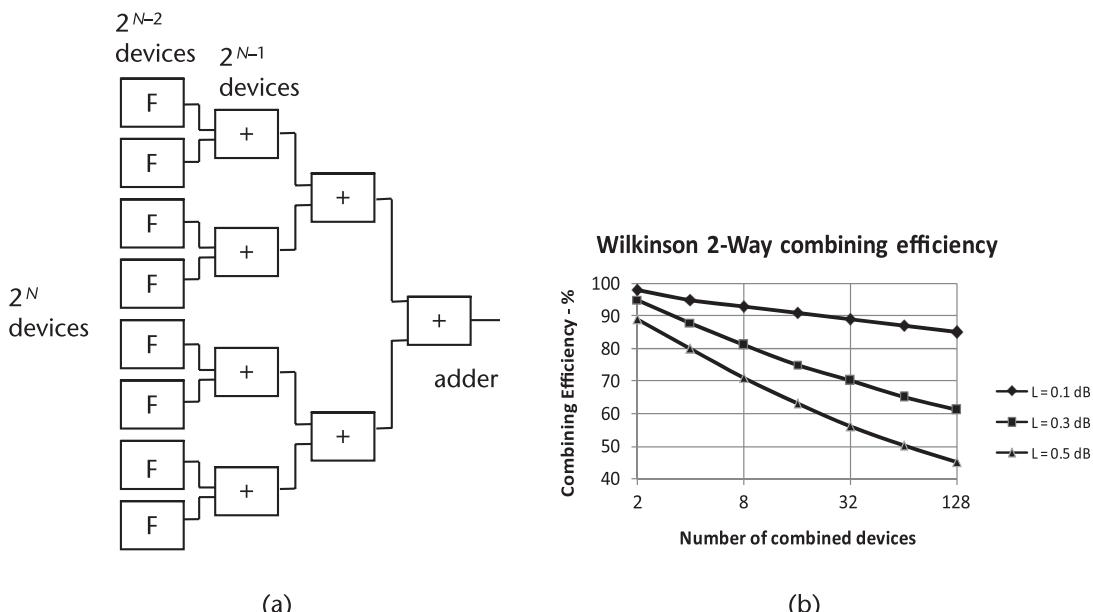
## 4.10 Chip-Level Power Combining

The amount of power that a unit cell can provide is limited. To obtain more power, they must be combined in parallel until the desired power level is achievable. The complexity of matching and associated circuit losses will increase with the number of cells. The most popular method of power combining is the Wilkinson two-way combiner, also called the corporate combiner, shown in Figure 4.62(a) [13]. It consists of combination of various identical two-way combiners connected in a tree shape. In millimeter-wave, the number of combining stages is limited to three. It seldom goes beyond three due to the losses added by each stage. The total output power  $P_{\text{out}}$ , given by (4.86), takes into account the losses introduced by each section, assuming that they are identical. There is a restriction on how close each unit cell can be drawn on a layout, related to how close each via can be built. Hence, the paralleling of unit cells has to follow the foundry design rules. The minimum distance between unit cells is dictated by the condition when the source vias of neighboring unit cells are on top of each other.

$$P_{\text{out}} = P_0 2^N L^N \quad (4.86)$$

where  $L$  is the loss of each stage and  $P_0$  is the output power from each cell.

In majority of power designs at millimeter-wave, the minimum distance between parallel cells results in smaller circuits, shorter lines, and lower losses. The maximum distance is a designer's choice, limited by losses from the lines used to connect the cells. The effect of losses is better appreciated looking into the diagram of Figure 4.62(b).



**Figure 4.62** Corporate tree for three stages of a power combiner: (a) block diagram, and (b) combining efficiency. (After: [13]. © 1979 IEEE.)

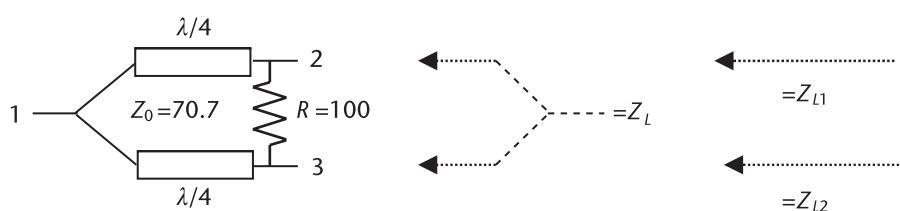
Figure 4.62 shows the combining efficiency versus the number of devices combined in parallel, parameterized by the section loss,  $L$ . Observe that there are three curves: the top one for  $L = 0.1$  dB, the second for  $L = 0.3$  dB, and the third for  $L = 0.5$  dB. Therefore, if a combining efficiency is to be maintained within 90% and losses are in the order of 0.3 dB, no more than four devices should be combined in parallel. The number of parallel devices can be traded by the output power that each device can provide.

#### 4.10.1 Port Impedance

The determination of the impedance presented to the drain from a power combiner network is a key factor to the circuit design. Let us take the case of the two-way Wilkinson combiner in Figure 4.63, composed of two  $\lambda/4$  transformers, each transforming the  $50\Omega$  impedance at ports 2 and 3 to  $100\Omega$  at port 1.

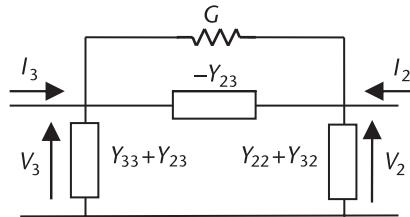
The input impedance is therefore the parallel combination, which is  $50\Omega$ . The isolating resistor, in the differential mode between two and three terminals, is virtually grounded at the middle, resulting in a shunt  $50\Omega$  at each port. However, a signal applied to port 2 drops 3 dB at the input port and an additional 3 dB at port 3, giving an isolation of 6 dB, at the central frequency of operation. In normal, even-mode operation, the resistor does not load the circuit. The conventional method to determine the impedance looking at port 2 or 3 is to tie both of them, measure the impedance, and multiply the result by 2. Therefore,  $Z_{L2} = Z_{L3} = 2Z_L$ . For an electrical circuit with similar circuits in each port, this is a simple and correct method. However, say you have three ports and the circuit layout shows that they are not quite similar. In such a case, the parameter  $Z_L$  will provide an average between the three ports and not the impedance of each port. If we go one step further and consider that we need a power combiner with different impedances between the legs, the average process to determine the port impedance is inadequate. Actually, even if the layout seems symmetrical, one often finds after EM analysis that the impedances have differences. One can think of applying equal voltage generators in magnitude and phase at each port simultaneously and measure the impedance, but there is a simpler way to determine this impedance.

Let us use the arrangement proposed by Collin [14] for a two-way combiner, reproduced in Figure 4.64. In this figure, if  $G$  cancels  $-Y_{23}$ , the impedance is given by the port admittance plus the transadmittance. In the particular case where it



Circuit schematic → Average impedance      Individual impedance

**Figure 4.63** Conventional two-way Wilkinson combiner and port impedance.



**Figure 4.64** Equivalent impedance for a two-way combiner. (After: [14]. © 2001 IEEE.)

is assumed that equal voltages are applied simultaneously to the output ports, the terms  $G$  and  $-Y_{23}$  are not relevant, so we can express the port 2 admittance as  $Y'_{22} = Y_{22} + Y_{23}$  and port 3 admittance as  $Y'_{33} = Y_{33} + Y_{32}$ . We can also extend this principle to multiple coupled ports (concluded after discussions with Trong Phan, MACOM Tech, Santa Clara, 2019).

Thus, given an  $n$ -way output combiner, the S-parameter at a given port, taking into account the effect of all other ports, is obtained by adding the admittance between the given port and all others. Equations (4.87a-d) describes the desired reflection coefficients for a 4:1 combiner.

$$S'_{22} = S_{22} + S_{23} + S_{24} + S_{25} \quad (4.87a)$$

$$S'_{33} = S_{32} + S_{33} + S_{34} + S_{35} \quad (4.87b)$$

$$S'_{44} = S_{43} + S_{42} + S_{44} + S_{45} \quad (4.87c)$$

$$S'_{55} = S_{54} + S_{53} + S_{52} + S_{55} \quad (4.87d)$$

From the port  $S'_{ii}$  S-parameters, the equivalent impedance and admittance are obtained from the definition of reflection coefficient at a given port with reference to  $50\Omega$ . The port impedance can be directly obtained from (4.88) and the admittance can be directly obtained from (4.89). If the S-parameters are for a drain admittance, it is represented by a resistance in parallel with a capacitance. These parameters are obtained from the transformations defined by (4.90) and (4.91). All subsequent simulations for drain and gate impedances in this book use these equations.

$$Z'_{ii} = \frac{50 \cdot (1 + S'_{ii})}{(1 - S'_{ii})} \quad (4.88)$$

$$Y'_{ii} = \frac{(1 - S'_{ii})}{50 \cdot (1 + S'_{ii})} \quad (4.89)$$

$$R_d = \frac{1}{\text{real}(Y'_{ii})} \quad (4.90)$$

$$X_d = \frac{1}{\text{imag}(Y'_{ii})} \quad (4.91)$$

#### 4.10.2 Two-Way Combiner

The classical two-way combiner has to be modified to add power from the drain of two cells and provide impedance matching simultaneously. Let us start with a one-way circuit consisting of a series resonator and cascaded with two transmission lines, as represented in Figure 4.65. The resonator transforms the complex impedance to a resistive impedance,  $R_T$ , at node A. The next two lines transform the impedance  $R_T$  to  $R_L$ . The characteristic impedance of the first element from left to right,  $Z_1$ , is given by (4.93) and a similar equation is valid for  $Z_2$ , with  $R_T$  replaced by  $Z_L$ . They can be designed to obey relation (4.92) or, in the case of a Type-C network, are determined by (4.62) to (4.65).

$$\frac{R_L}{R_{\text{int}}} = \frac{R_{\text{int}}}{R_T} \quad (4.92)$$

$$Z_1 = \sqrt{R_T \cdot R_{\text{int}}} \quad (4.93)$$

There are two ways to merge that circuit with a two-way combiner. One can parallel two sections of this circuit and combine them at the output node. One can also parallel two sections containing line 0 and line 1 and add them at node B. Both options are detailed in Figures 4.66(a) and 4.66(b). The decision on which one to use in the design is dependent on layout convenience, as both options provide similar results.

In option (a) in Figure 4.66(a), the characteristic impedance of line 2 is increased for matching port 2 to a  $100\Omega$  load. The paralleling of two networks will give an output matched to  $50\Omega$ . The problem of this option is that line 1 in the real layout is usually a low-impedance line, requiring circuit modifications to take this fact into account. In option (b) in Figure 4.66(b), the characteristic impedance of line 1 is increased from  $10\Omega$  to  $20\Omega$  to account for the doubling of the node A impedance. Port 2 and port 3 impedances are calculated from (4.90) to (4.91). The impedances from both circuits are close, so only the performance of Figure 4.67(a) is represented in Figure 4.67(b).

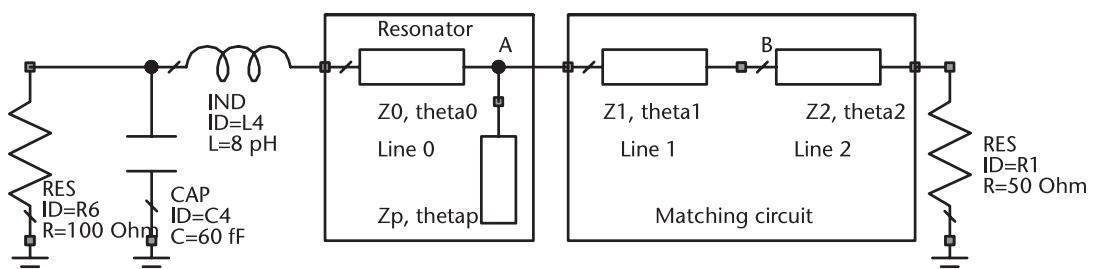
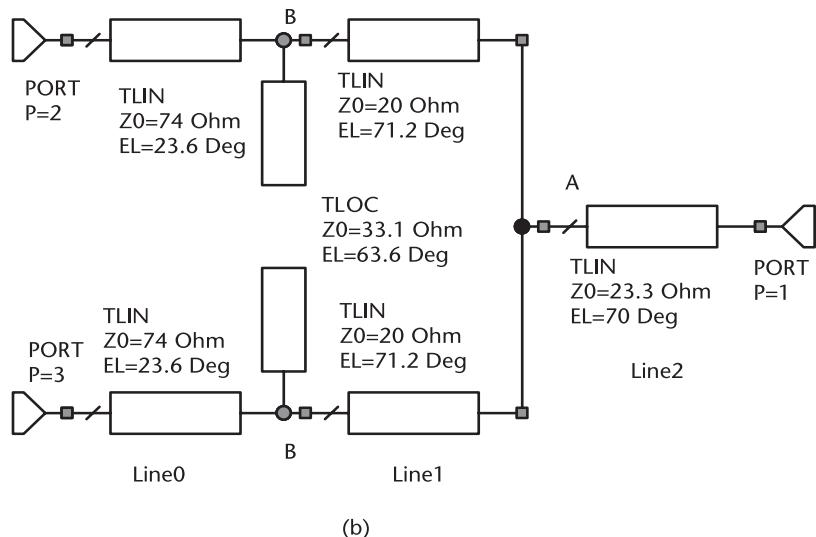
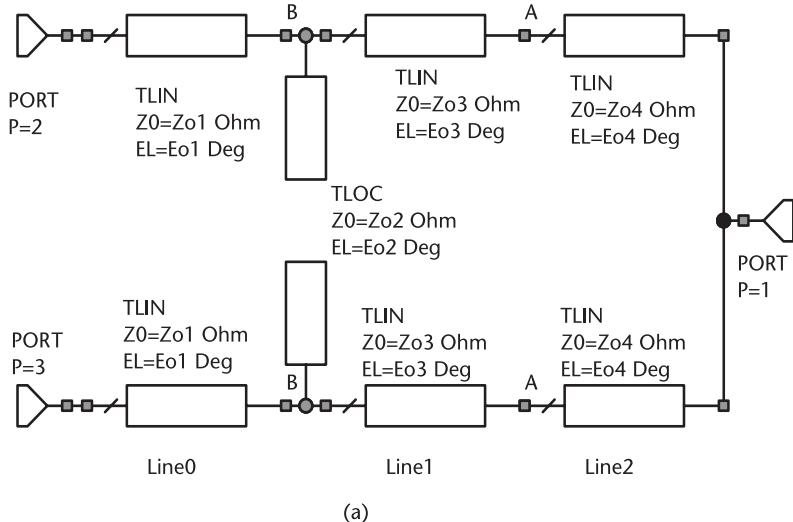


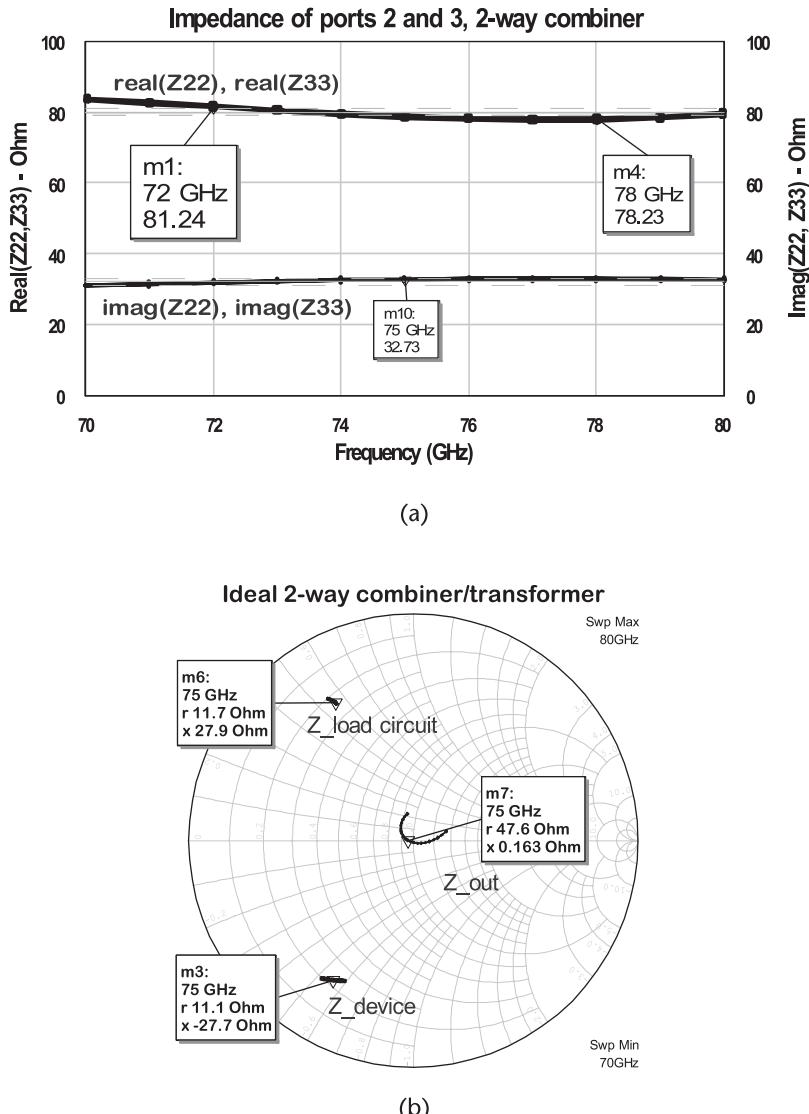
Figure 4.65 The first step to design an n-way combiner.



**Figure 4.66** Transformation of a single-ended to two-way combiner: (a) power combining at the port, and (b) power combining within the compensation.

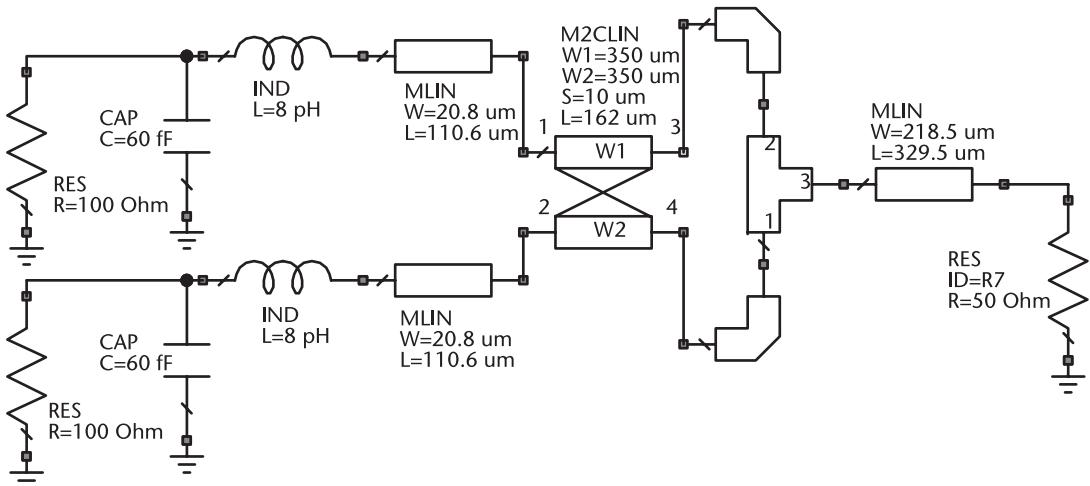
The real part of the drain impedance on the top plot of Figure 4.67(a) has a maximum of  $82\Omega$  at 70 GHz, decreasing to  $77.8\Omega$  at 78 GHz. The reactive part shows a slight increase from the beginning of the band up to  $j32.5\Omega$  at the middle of the band. It becomes flat for the remaining part of the band. Figure 4.67(b) shows at the top the S-parameter from ports 2 and 3 calculated from (4.88) modified for two ports.

That representation corresponds to the series equivalent impedance of the port impedance looking towards the load. At the bottom, we can see the series equivalent impedance of the drain port. It is close to the conjugate of the top impedance. The S-parameter at the center corresponds to the impedance looking towards the drain.



**Figure 4.67** Impedance at ports 2 and 3 of an ideal two-way combiner/transformer: (a) impedance in rectangular form, and (b) impedance on the Smith chart.

The circuit in Figure 4.66(b) was modified from ideal transmission lines to real microstrip lines on SiC, 50- $\mu\text{m}$ -thick substrates, shown in Figure 4.68. One can see the addition of a coupled-line section and two microstrip bends. The coupled-line model takes into account the coupling effects of two lines close to each other. The most important added element is the MTEE, which represents the point in the circuit where the power is combined. The models either can be provided by the foundry or are available from commercial simulators. The connection elements between lines 2 and 3 increase the length of the matching quarter-wave lines and have to be compensated.



**Figure 4.68** The building of a two-way power combiner/transformer.

The impedance of ports 2 and 3, based on the microstrip EE model, is represented in Figure 4.69(a). The representation of real impedance is at the top, with traces of ports 2 and 3 on top of each other.

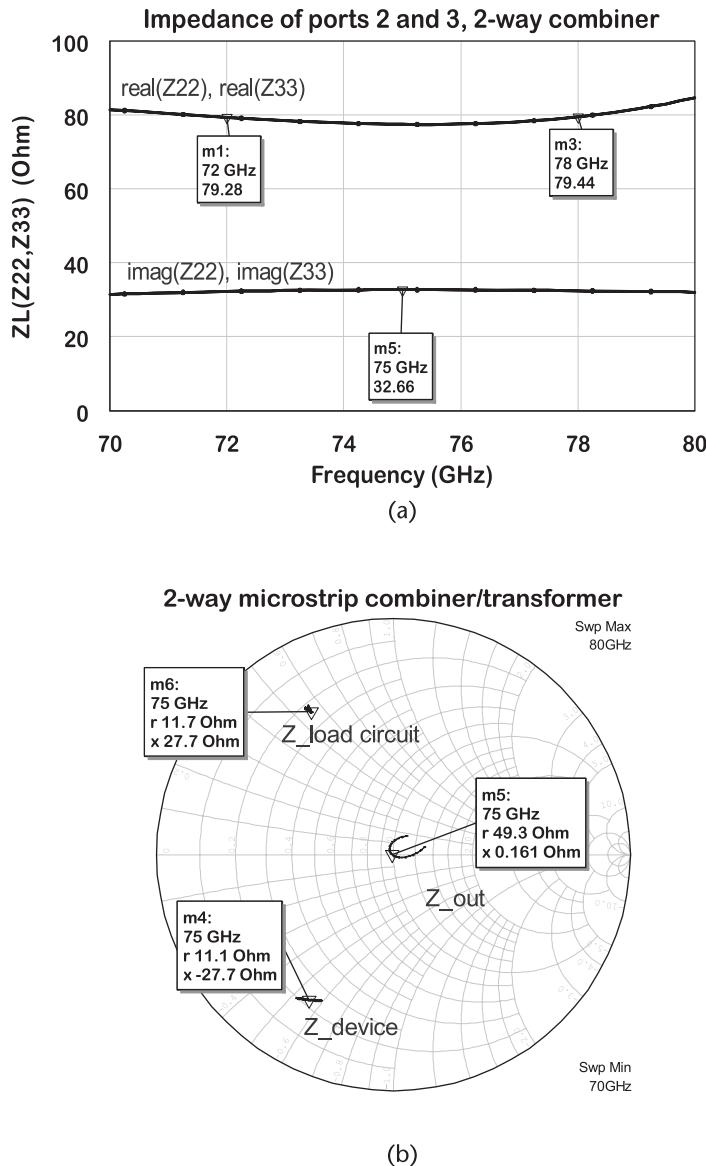
The same observation is valid for the imaginary part located at the bottom. The reactive part shows a flat value over the band. Therefore, the reactance is partially compensated. Figure 4.69(b) shows the impedance at the single-ended output.

The characteristic impedance of line 1 is  $21\Omega$ , which means a microstrip line with a large width, which should be avoided at high millimeter-wave with multiple ports. However, in the case of just two unit cells, it is not a problem to use larger width lines. One can offset the transmission-line contact from the center of the line to match the minimum distance from unit cells. Impedance will not be the same as predicted by electrical circuit simulation, but one can adjust the transformer for the desired impedance using electromagnetic analysis.

#### 4.10.3 Three-Way Combiner

Let us consider the problem of generating a three-way combiner capable of simultaneously transforming the impedance. We start with the same one-way circuit from (4.65). Similar to the two-way network, there are two options to merge the matching network with the combiner network. Either makes the reactance compensation and then combines the power or does the power combining within the reactance compensation network.

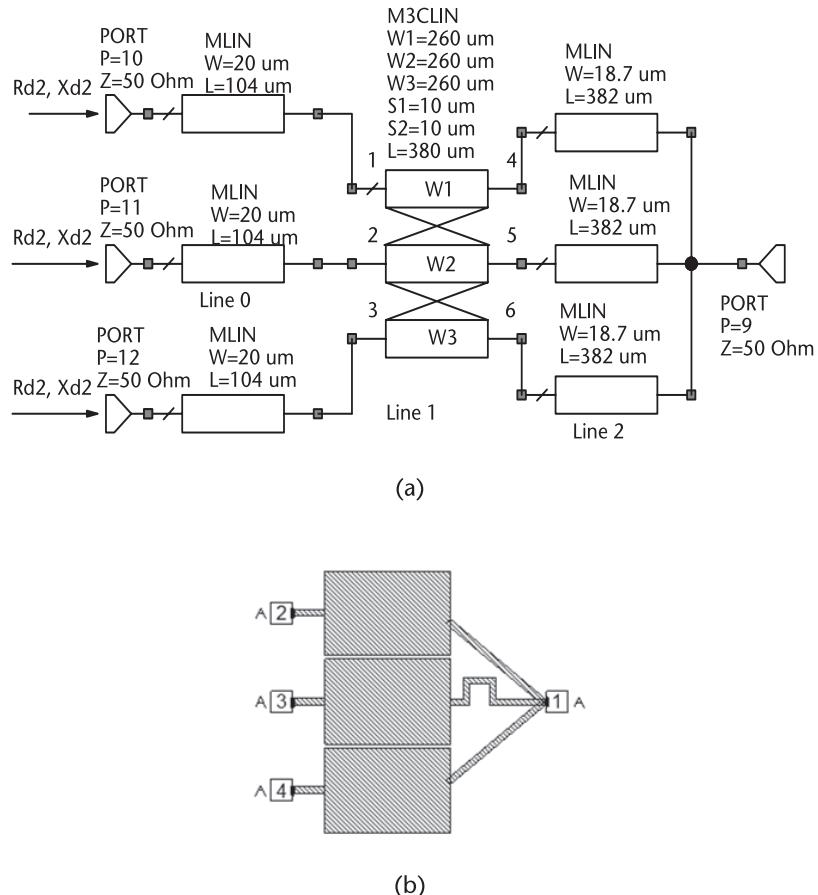
The first approach is illustrated in Figure 4.70(a) where the three cascaded lines are paralleled at the output port. Each matching circuit is calculated for transforming the input impedance,  $Z_s$ , to the load resistance at the joining point,  $150\Omega$ . That makes the impedance  $Z_{11}$  and  $Z_{22}$  larger than the original value  $Z_1, Z_2$ . In this case,  $Z_{22}$  is higher than  $50\Omega$ , resulting in a narrow line width,  $17.8 \mu\text{m}$ . The calculated low-impedance line, ( $Z_0 = 15\Omega$ ), calls for a line width of  $350 \mu\text{m}$ . By optimization, we reduced the large line width to  $260 \mu\text{m}$ . The joining of these three high



**Figure 4.69** Impedance of a two-way combiner using a microstrip EE model: (a) impedance of ports 2 and 3, microstrip model, and (b) combiner with microstrip model.

impedance lines at the output port introduces a low amount of parasitic, as is the case with shunt elements. A possible layout is represented in Figure 4.70(b).

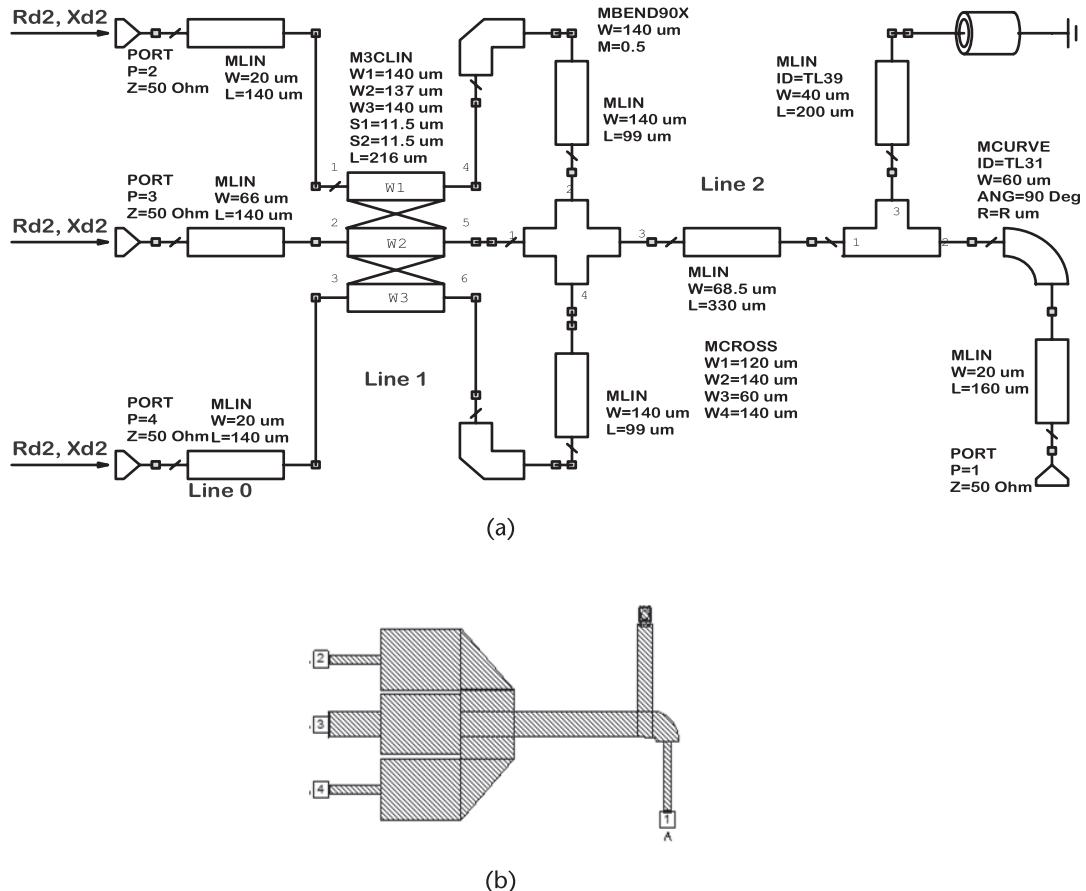
In the second approach, shown in the schematic of Figure 4.71(a), lines 0 and 1 are paralleled and connected between the drain ports and node B. The corresponding layout is shown in Figure 4.71(b). The impedance of line 1 needs to change to account for the higher intermediate resistance, now multiplied by 3. The paralleling requires adding external lines to the joining point by a connecting line with the parameters  $Z_p$ ,  $\theta_p$ . Therefore, the parasitics introduced by



**Figure 4.70** Microstrip line version of a three-way power combiner: (a) compensation before combining, and (b) layout for corresponding circuit.

connecting line is not negligible, and its effect has to be compensated. If we add the admittance of these lines, the total sum at the joining point will be equal to the admittance of each line, plus a reactive term corresponding to line  $Z_p$ . If the center line is  $90^\circ$ , the top and bottom lines will be longer, resulting in a negative imaginary term at the joining point. If the top and lower lines are made equal to  $90^\circ$ , the center line will be smaller, resulting in an additional imaginary term with opposite sign. That means that the impedance can be matched either by a series capacitance or by a series inductor. However, the phase mismatch has to be taken into account by the combiner impedances. An approach that has been found to be efficient is to make the center arm impedance different than the impedance of the outer arms.

Finding an analytical solution to this problem is too complex with distributed elements, but it can be managed by using optimizer routines. The circuit shows the addition of a short shunt stub and additional series lines. The former is necessary to compensate the addition of the connecting lines and the latter to enable the

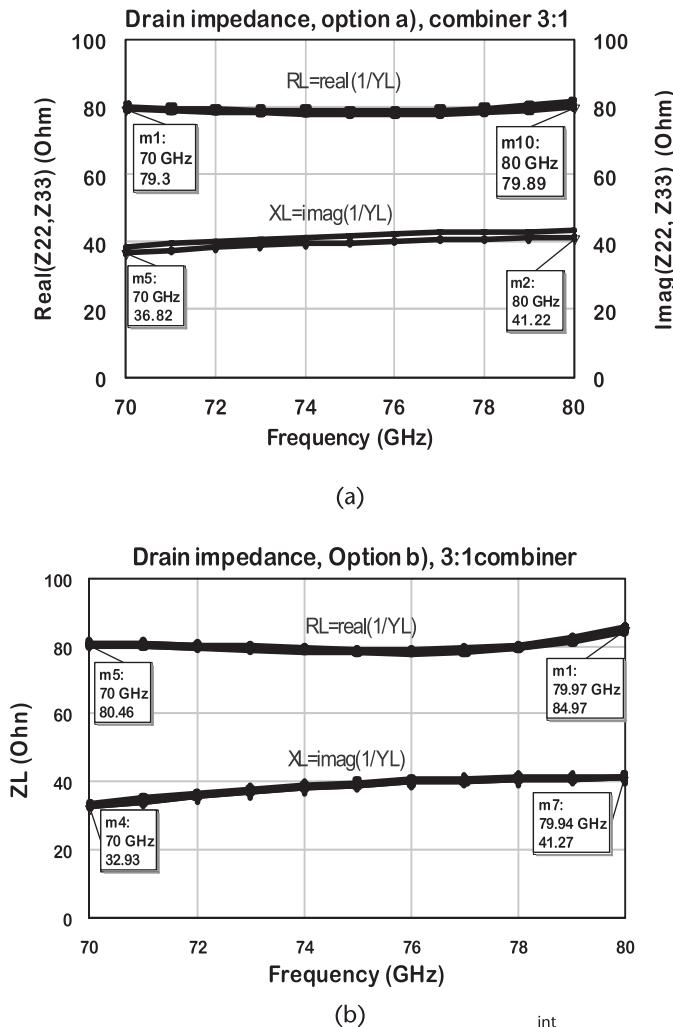


**Figure 4.71** Layout describing the differences between the options: (a) layout for option a, and (b) layout for option b.

connection to an image circuit in order to build a 6:1 combiner. The impedance at the drain ports connected to the FETs is obtained from EE simulation for both options and is represented in Figures 4.72(a, b).

The impedance in the figures corresponds to an impedance of  $80\Omega$  in parallel with an inductive reactance of  $j40\Omega$ . Ideally, the reactive part should show a slight negative slope for perfect compensation. The curves indicate a small positive slope, causing a mismatch at the edges of the frequency band, with respect to the best impedance for power.

Another parameter of importance is the amplitude and phase balance for the divider. The results are presented in Figure 4.73 for conjugate matched ports. The S-parameters are simulated from the internal drain resistor,  $100\Omega$  in this case, to the load resistor, equal to  $100\Omega$ . Option (a) is shown in Figure 4.73(a) and shows a magnitude of total insertion loss between 5.18 and 5.38 dB. The phase balance between ports is less than  $1^\circ$ . For option (b) shown in Figure 4.73(b), the minimum insertion loss is equal to 5.16 dB and the maximum is 5.5 dB.



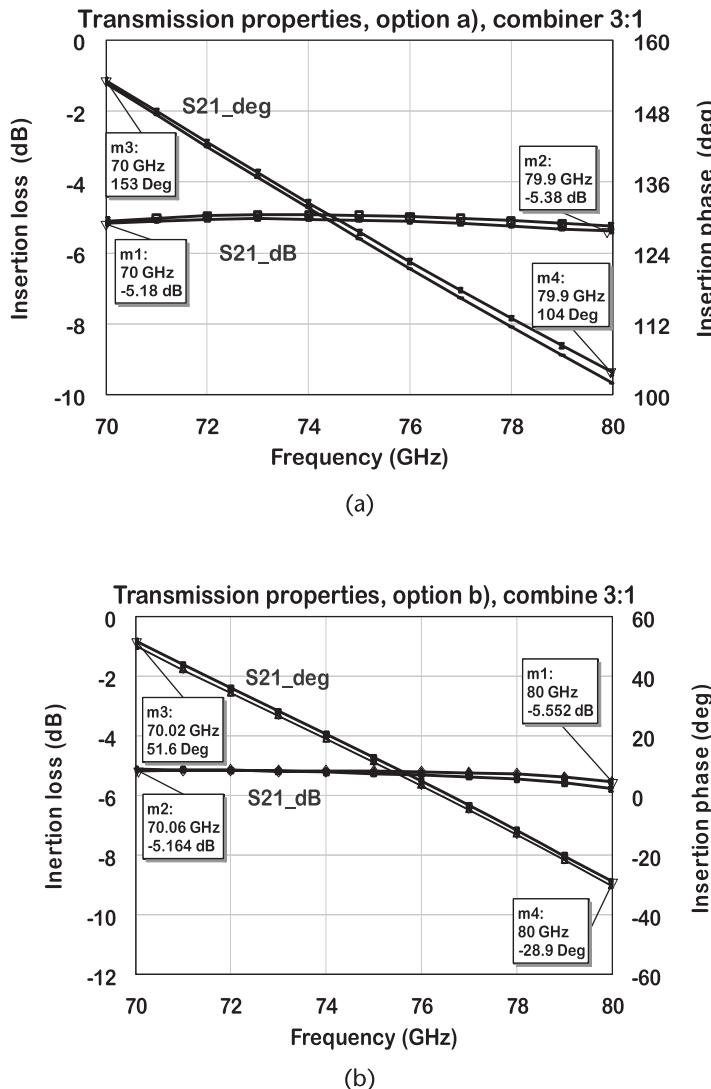
**Figure 4.72** Simulation of port impedances for the circuit options: (a) three lines combined at the load, and (b) two series lines combined at  $R_{\text{int}}$ .

The ideal 3:1 coupler shows an insertion loss of 4.8 dB. Therefore, the option (a) combiner gives an insertion loss of 0.4 to 0.6 dB and the option (b) combiner gives an insertion loss of 0.7 compared to the ideal combiner.

#### 4.10.4 Four-Way Combiner

A single section of a four-way combiner may be built with a single bus connecting the four transmission lines matching the drain port impedance to four times the output impedance. This solution is fine if the distance between the FET devices is at least 10 times lower than the frequency of operation. Otherwise, the circuit will perform with power imbalance between the ports.

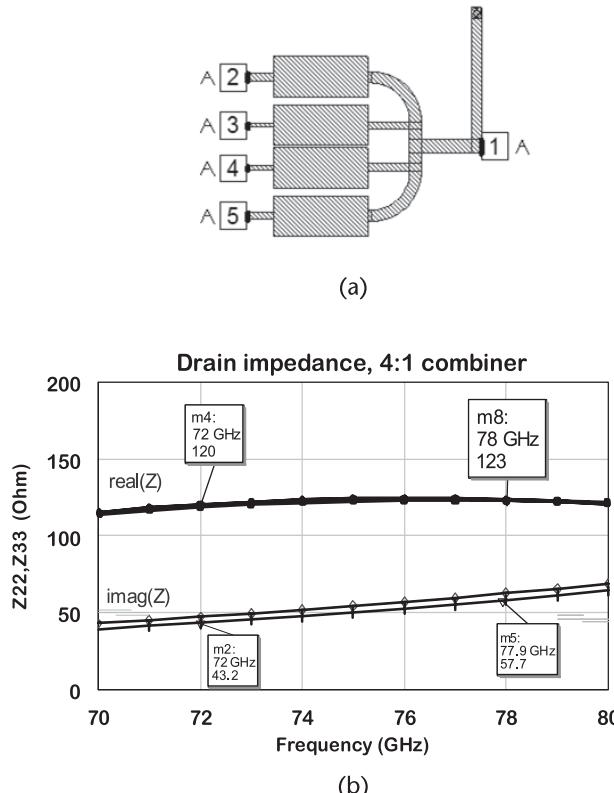
An alternative is to add after the quarter-wave transformer a short high-impedance line that can be directly joined with minimum parasitic. Besides the



**Figure 4.73** A three-way combiner balance between the ports: (a) balance between ports 2 and 3, and (b) balance between ports 2 and 3.

series lines, a shunt short stub was added to the circuit. The layout for this circuit is represented in Figure 4.74(a) and the corresponding port impedances are in Figure 4.74(b). The drain impedance parameters are  $R_{Lout} = 160\Omega$ ,  $C_{out} = 40\text{ fF}$ , and series inductance  $L_d = 12\text{ pH}$ . The EM analysis may improve this performance. For instance the curved line can be replaced by a straight line in angle, reducing the length of the curved line compared to the center lines.

The schematic of a four-way combiner consisting of two stages of two-way combiners is shown in Figure 4.75. In view of the symmetry, the design was initially made for half the circuit. Then the two halves were combined. Line 0 is the drain resonator, and lines 1 and 2 correspond to the cascaded series lines for impedance

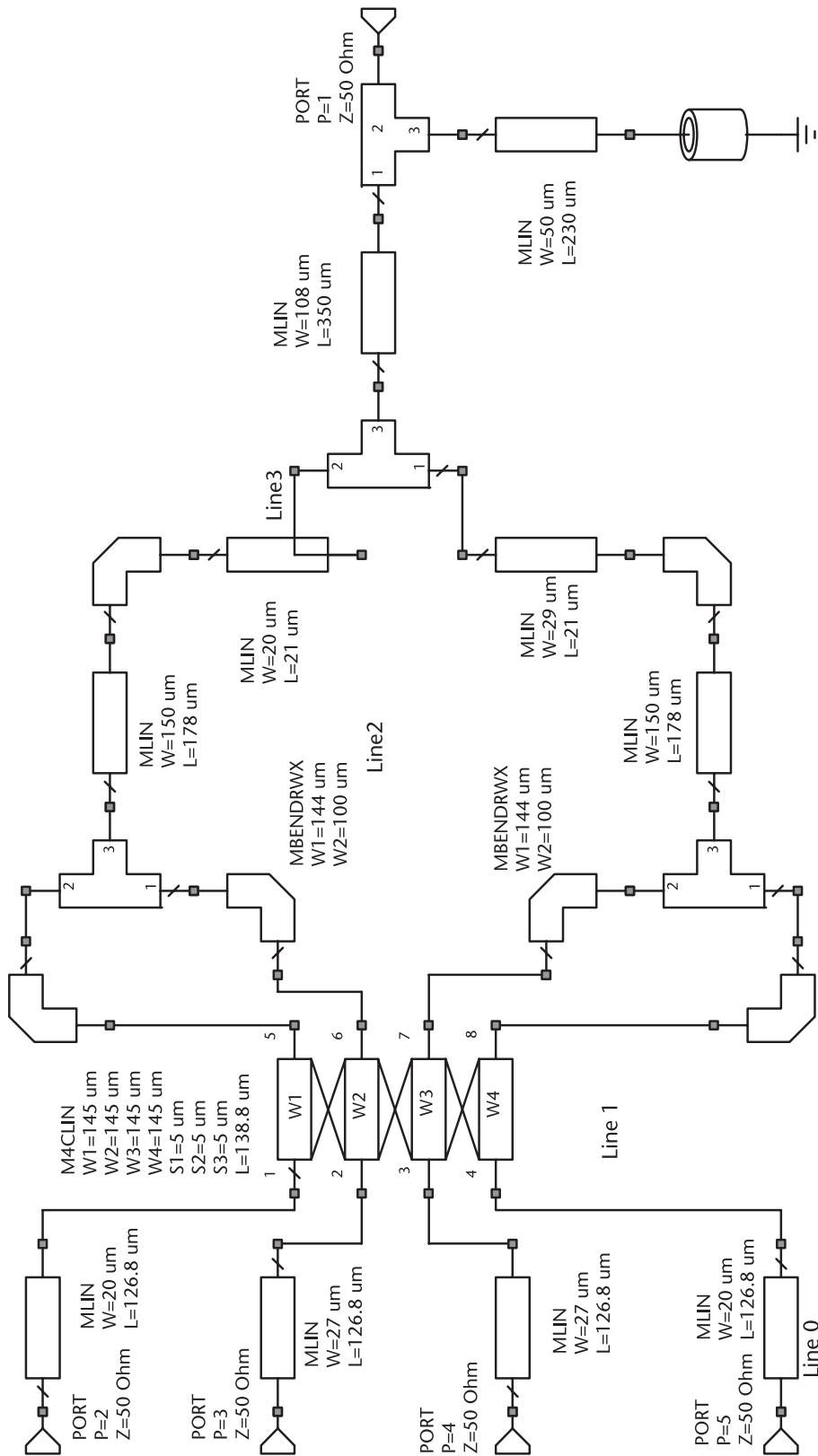


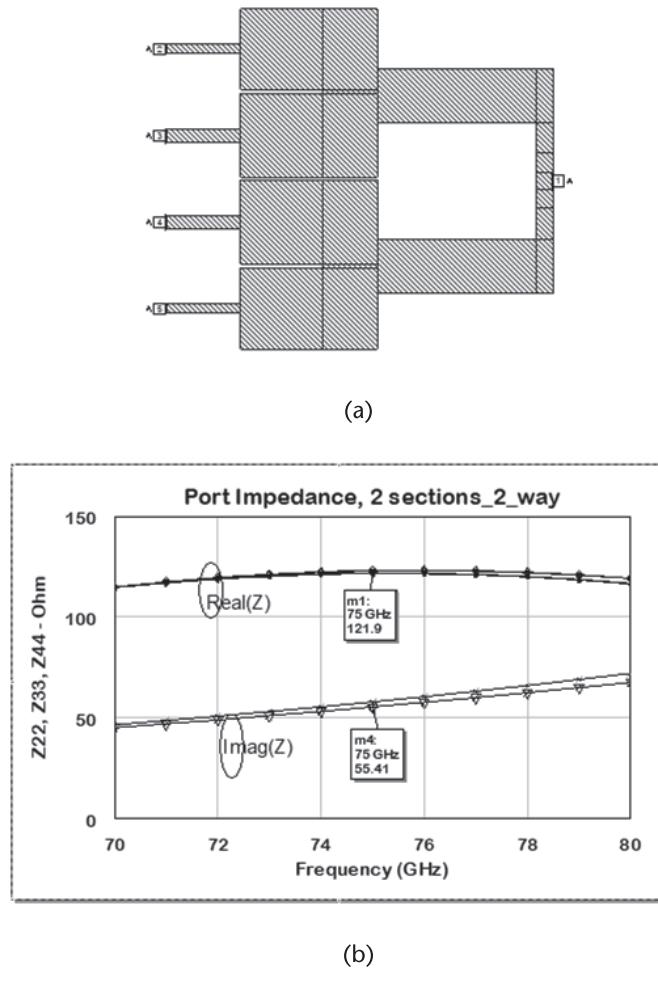
**Figure 4.74** Layout of the four-way and correspondent impedances: (a) layout of the circuit, and (b) drain impedance.

match to a  $100\Omega$  termination. Line 3 and the shunt stub were added to the final circuit. After optimizations are carried out for the EE circuit, it was converted to an EM layout and it was iteratively optimized to match the desired terminations. The final layout is shown in Figure 4.76(a) and the corresponding port impedances are shown in Figure 4.76(b).

Ports 4 and 5 are not shown, for they are mirror impedances of ports 3 and 2, respectively. The results are for a frequency range between 70 and 80 GHz. The real part of impedance is well-balanced, with a variation of a few ohms over the band. This will cause less than a couple of tenths of a decibel difference in power within the band. The reactive part is linear with frequency from 74 to 80 GHz. From 75 to 89 GHz, there is a small imbalance in the reactances.

The combiners addressed in this chapter can be further combined to parallel more devices. A four-way combiner can be easily generated from 2 two-way combiners and a six-way combiner can be generated from 2 three-way combiners. The paralleling of 8 unit cells has been reported at high millimeter-wave frequencies [15]. At Ka-band, depending on the technology, more devices with larger power capability can be paralleled. Actually, 16 cells in parallel has been reported [16] to generate 20W of RF power. The main limitation of device paralleling is how to evacuate the heat generated by so much power. In [16], a special diamond heat sink had to be used.





**Figure 4.76** Final layout and corresponding port impedance for a four-way combiner using 2 two-way stages: (a) layout for the paralleled 2-way, and (b) simulation of impedance at the ports.

#### 4.10.5 Port Impedance

The rectangular representation of the load impedance often shows a resistance as a slow function of frequency. That causes a fluctuation in the output power. In order to estimate the effect of these fluctuations, we can use (4.94). That expression relates load impedance and drain current to output power, assuming that the current is approximately constant and that the reactive part is conjugated-matched.

$$\frac{P_{\text{out}}}{P_{\text{nom}}} = \frac{R_L}{R_{\text{nom}}} \quad (4.94)$$

In the equation,  $P_{\text{nom}}$  and  $R_{\text{nom}}$  correspond to the design goals for the project.

## References

- [1] Abrie, P. L. D., *Design of RF and Microwave Amplifiers and Oscillators*, Norwood, MA: Artech House, 1999, pp. 239–316.
- [2] Aitchison, C. S., and J. C. Williams, “Active Reactance Compensation of Parametric Amplifiers,” *Electronic Letters*, Vol 5, No. 7, April 1969, pp. 139–140.
- [3] Aitchison, C. S., and R. V. Gelsthorpe, “A Circuit Technique for Broad Banding the Electronic Tuning Range of Gunn Oscillators,” *IEEE Journal of Solid State Circuits*, Vol. 12, No. 1, February 1977, pp. 21–28.
- [4] Grebennikov, A. V., *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2005, pp. 122–300.
- [5] Grebennikov, A. V., *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2005, p. 123.
- [6] Schwan, K. P., “Matching: When a Single Line Is Sufficient?” *Microwaves*, December 1975, pp. 58–63.
- [7] Pozar, D. M., Chapter 5 in *Microwave Engineering*, Third Edition, New York: John Wiley & Sons, 2005.
- [8] Grebennikov, A. V., “Create Transmission-Line Matching Circuits for Power Amplifiers,” *Microwaves & RF*, October 2000, pp. 113–172.
- [9] Camargo, E., D. Consoni, and R. Soares, “Reactance Compensation Matches FET Circuits,” *Microwave*, Vol. 24, 1985, pp. 93–95.
- [10] Abrie, P. L. D., *Design of RF and Microwave Amplifiers and Oscillators*, Norwood, MA: Artech House, 1999, pp. 338–340.
- [11] Collin, R. E., *Foundations for Microwave Engineering*, New York: IEEE Press, 2001, pp. 604, 614.
- [12] Mellor, G. J., “On the Design of Matched Equalizers of Prescribed Gain versus Frequency Profiles,” *IMS1977*, 1977, pp. 308–311.
- [13] Russell, K. J., “Microwave Power Combining Techniques,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 27, No. 5, May 1979, pp. 472–478.
- [14] Collin, R. E., *Foundations for Microwave Engineering*, New York: IEEE Press, 2001, p. 445.
- [15] Camargo, E., et al., “F-Band, GaN Power Amplifiers,” *IMS2017*, 2017.
- [16] Din, S., M. Wojtowicz and M. Siddiqui, “High Power and High Efficiency Ka Band Power Amplifier,” *IMS 2015*, 2015.



# Power Amplifiers

The purpose of this chapter is to cover the aspects involved in the design of millimeter-wave power amplifiers, sometimes also called solid-state power amplifiers (SSPAs). The methodology tries to minimize the time to design such complex amplifiers. Therefore, the matching equations described in Chapter 4 are inserted in Excel templates, and gain and power contours are avoided but are used to model the device ports. The matching circuit parameters are determined using the Smith chart as a calculator as much as possible. Another point of interest in this chapter is the conversion of electrical to electromagnetic models. The design of a microwave power amplifier up to 20 GHz can be successful with electrical models. However, for higher frequencies, electromagnetic analysis is mandatory. This is one of the main distinctions between a microwave design and a millimeter-wave design.

Section 5.1 presents the methodology involved in an MMIC design. That is where it is shown how the design flows from the start-up to the mask ready for fabrication. In Section 5.2, a preliminary analysis to determine the device sizes is carried out, based on the specified amplifier output power. Section 5.3 contains a brief discussion on the criteria used for the design. That includes the three main parameters of an amplifier: power, linearity, and efficiency. These are followed by four case studies, in Sections 5.4 to 5.7, that address the practical realization of a power amplifier using solely EE models. Section 5.8 covers the techniques to convert the circuit EE models to EM models. Even though automatic conversion is now available from software houses, this process is performed manually. Section 5.9 completes the design process, discussing the stability issues.

## 5.1 Design Methodology

The objective of this section is to introduce the design flow to build MMIC millimeter-wave power amplifiers. The methodology comprises three different phases, as described next.

### 5.1.1 Design Phase I

In this phase, preliminary design decisions are made. We start by reviewing the proposed performance goals for the project and the technologies available in the market capable of delivering the target goals. That is also the time when the technology models have to be confirmed, with foundry information and basic DC and S-parameter evaluation from test cells. If possible, obtain device test cells from

the foundry selected. The next decision to make is about the number of stages, mainly dependent on the FET gain, which, in turn, is dependent on the size of the active devices. Obviously, the number of stages should be as low as possible. Unnecessary stages cause more gain variation over temperature. In order to make these decisions, one should create a spreadsheet to trade off the amplifier parameters, such as power, gain efficiency, and device size. Another basic decision to be made at this point is the type of amplifier to be designed. We start with the choice of class of operation, selected after the classes discussed in Chapter 3. We will concentrate on the design of single-ended amplifiers, as balanced or push-pull configurations are a combination of single-ended designs.

The process continues with the definition of topology and preliminary considerations for the matching blocks. The output matching network (OMN) circuit needs to be designed for the specific application for power, efficiency, or linearity. The interstage matching network (ISMN) can be designed for gain when the gain of the power device is high, or for power when the gain of the power device is low. The size of the output stage is primarily determined for a specific power or for a trade-off between power, efficiency, and linearity. The size of the driver device is selected for a  $P_{\text{sat}}$  about 3 to 6 dB higher than the required value for power and linear application. For efficiency, it is designed with sufficient power to overcome the interstage losses.

### 5.1.2 Design Phase II

After the preliminary decisions have been made, we start the design from the power stage and move towards the input. This is a natural procedure, as the power is determined mainly by the power stage load. The preceding stage is also as important: the reason for concentrating the design on these two stages, called the core amplifier. The stages preceding the core amplifier are, in general, at a power level 10 to 15 dB below and are, in general, designed for gain. That means that the source and load impedance are modeled based on the conjugate match impedance determined from the S-parameter theory, as described in Chapter 2. It could also start with source and load impedances determined by a load-pull system. The load impedance for the power stage is used to design the OMN circuit block. The same load and respective source are used to design the ISMN circuit block, assuming that the same unit cell is used. Moving towards the input, there are other interstage blocks and the input matching network (IMN) circuit block, in general, designed for gain.

### 5.1.3 Design Phase III

The main objective of this section is to convert the matching blocks based on EE models to EM models, which is also a phase where a detailed stability analysis is carried out for the complete amplifier. The reason to emphasize the stability analysis at this point is due to the circuit losses and coupling effects that are better estimated from EM compared to EE analysis. This design step used to take a long time to generate the desired EM models, due to the time involved in modifying the element dimensions, resimulating, and comparing with the electrical models. Currently, some

of these tasks have been automated by commercial software packages, considerably reducing the design time. Even though automated EM optimization is available in some simulators, it still takes a long time to deliver. The automated methods are not addressed in this book. Hence, the optimization of the EM circuits is done by a manual process.

## 5.2 Transistor Cell Size

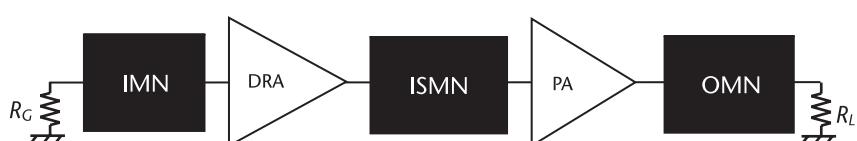
The power amplifier core can be considered the combination of a driver amplifier (DRA) and a power amplifier, including the matching networks as shown in Figure 5.1. The important effects for power output and efficiency occur in these two stages. It may not be obvious, but the output power, linearity, and/or efficiency are also dependent on the driver stage performance.

We verified that the unit cells available from most foundries specifically for higher millimeter-wave frequencies are either with 2 fingers measuring  $2 \times 20 \mu\text{m}$  up to  $2 \times 75 \mu\text{m}$  or with 4 fingers measuring  $4 \times 20 \mu\text{m}$  up to  $4 \times 50 \mu\text{m}$ . Devices with larger periphery in current technologies are applicable to Ka-band, located at the low end of the millimeter-wave spectrum. The unit cell measuring  $4 \times 25 \mu\text{m}$ , whose DC parameters from our idealized process were extracted in Figures 2.19 and 2.20, was selected for the applications demonstrated in this chapter. The maximum linear power for the unit cell can be found from (5.1), with the following assumptions: drain bias of 12V, knee voltage of 2.5V, and an effective  $I_{\max}$  of 136 mA.

$$P_{\text{out}} = \frac{(V_{DS} - V_k)I_{\max,\text{eff}}}{4} = \frac{(12 - 2.5)136}{4} = 323 \text{ mW} \quad (5.1)$$

This would give a power density of 3.2 W/mm for this idealized technology. The nominal power for the power stage, considering circuit losses,  $L_{\text{out}}$ , margin for temperature,  $C_{\text{temp}}$ , and margin for process,  $C_{\text{pro}}$ , is obtained from (5.2). The driver size estimation involves the power stage gain,  $G_p$ , and the interstage circuit losses,  $L_{\text{int}}$ , (5.3).

$$P_{\text{out},pa} \geq \frac{P_{\text{out},HPA}}{L_{\text{out}}} C_{\text{temp}} C_{\text{pro}} \quad (5.2)$$



**Figure 5.1** Block diagram of driver and power stage.

$$P_{\text{out},dr} \geq \frac{P_{\text{out},dr}}{G_{P,pa} L_{int}} C_{\text{temp}} C_{\text{pro}} C_{P_{\text{out}}} \quad (5.3)$$

The preliminary output device size ( $^1W_p$ ) for an amplifier delivering 1W of power at a frequency in the middle of the W-band, assuming an insertion loss of 0.8 dB for the matching circuits, is shown in Table 5.1. A typical small signal gain of 9 dB is assumed in the calculations and the correction coefficients are all equal to 1.

This estimation is based on linear equations and does not take into account the gain compression. A better size estimation can be made by considering the compression, using (5.4) [1]. This function was used in the construction of the spreadsheet presented in Table 5.2. The size of output stage was adjusted to provide the desired output power. Then several driver sizes ( $^2W_{dr}$ ) were assumed for a fixed power stage size.

$$P_{\text{out}} = P_{\text{max}} \left( 1 - e^{-\frac{\text{SSG}P_{\text{in}}}{P_{\text{max}}}} \right) \quad (5.4)$$

Different choices of gain and efficiency are obtained with the analysis in Table 5.2. From these options, one can build up several lineup alternatives as presented in

**Table 5.1** Parameters for Device Sizing

Parameters	Driver	Power
SSG (dB)	9.5	9
Losses (dB)	0.7	0.7
I <sub>max</sub> (mA/mm)	1200	1200
P <sub>max</sub> (mW/mm)	2200	2200
P <sub>out</sub> (dBm)	22.1	30.8
TGW (μm)	75	546

**Table 5.2** Power and Driver Device Options

W <sub>p</sub> /W <sub>dr</sub> ratio	W <sub>dr</sub> (μm)	P <sub>in</sub> (dBm)	P <sub>out,dr</sub> (dBm)	P <sub>DC,dr</sub> (mW)	Gain <sub>dr</sub> (%)	PAE <sub>dr</sub> (%)	P <sub>out,pa</sub> (dBm)	P <sub>DC,pa</sub> (mW)	Gain <sub>pa</sub> (%)	PAE <sub>pa</sub> (%)	HPA (dB)	HPA (%)
4	170	-10	-1.20	446	8.80	0.14	7.09	1,849	8.29	0.24	17.09	0.22
4	170	18	24.08	456	6.08	41.66	29.62	1,849	5.55	35.75	11.62	36.93
3	227	18	24.69	609	6.69	37.55	29.88	1,849	5.19	36.68	11.88	36.90
2.5	272	18	25.02	730	7.02	34.37	30.00	1,849	4.99	36.94	12.00	36.21
2	340	18	25.35	913	7.35	30.25	30.12	1,849	4.77	37.02	12.12	34.76
1.6	401	18	25.63	1,156	7.63	26.14	30.22	1,849	4.58	36.93	12.22	32.78
1	680	18	26.05	1,826	8.05	18.38	30.32	1,849	4.27	36.48	12.32	27.43

W<sub>p</sub> stands for power stage periphery.

W<sub>dr</sub> stands for driver stage periphery.

**Table 5.3** Amplifier Lineup Options

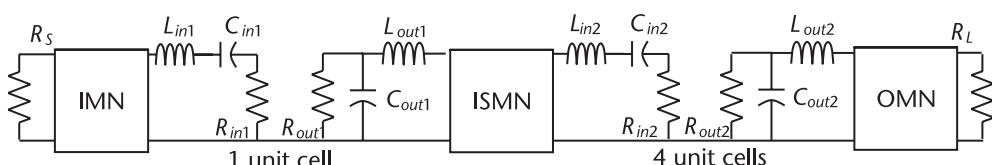
Options	First Stage ( $\mu m$ )	Second Stage ( $\mu m$ )	Third Stage ( $\mu m$ )	Gain (dB)	$P_{out}$ (dBm)	PAE (%)
4	$4 \times 25$	$4 \times 37.5$	$4 \times (4 \times 37.5)$	21.62	29.62	36.96
3	$4 \times 25$	$2 \times (4 \times 25)$	$6 \times (4 \times 25)$	21.88	29.88	36.9
2.5	$4 \times 25$	$2 \times (4 \times 30)$	$6 \times (4 \times 25)$	22.00	30	36.21
2a	$4 \times 25$	$2 \times (4 \times 37.5)$	$4 \times (4 \times 37.5)$	22.12	30.12	34.76
2b	$4 \times 25$	$3 \times (4 \times 25)$	$6 \times (4 \times 25)$	22.12	30.12	34.76
1.6	$2 \times (2 \times 25)$	$4 \times (4 \times 25)$	$4 \times (4 \times 37.5)$	22.20	30.2	32.78

Table 5.3, which considers an additional input stage of 8 dB to increase the overall amplifier gain. Comparing the device sizes from these options to the sizes estimated in Table 5.1, it is found that the output device needs to be 50  $\mu m$  larger and the driver is at least 100  $\mu m$  larger. Options 2.5 to 4 show similar efficiency, with a maximum power variation of 0.4 dB. The effect on efficiency starts to be important for ratios lower than 2. If linearity is important, option 1.6 is the best choice. The gain and efficiency values from this table are frequency-dependent. They increase at the low end of W-band and decrease at the high end.

### 5.3 Design Criteria

Let us establish the criteria to design the amplifier options of Table 5.3 by considering the diagram for the core amplifier, as detailed in Figure 5.2. As an example, it contains 4 unit cells in the power stage and 1 unit cell in the driver stage. In order to start the amplifier design, the equivalent circuit models must be available.

The source and load equivalent circuits at each stage, represented in Figure 5.2, are determined at the center frequency of operation and are assumed to be valid within a 10% bandwidth. Therefore, the equivalent resistances, inductances, and capacitances are assumed to be constant and are used as the target in the optimization process. If the bandwidth is larger, then the source and load equivalent circuits must be determined for three or more frequencies within the band. The design methodology consists of optimizing the ISMN and OMN circuit blocks to match specific impedances. The IMN block is then optimized for a specific gain, preferably by fixing the ISMN and OMN blocks. For a two-stage amplifier, it may be necessary to optimize the ISMN block for both power and gain. For three or more stages, the gain is adjusted by the IMN and other interstage blocks.

**Figure 5.2** Core amplifier model.

The amplifier power, efficiency, and linearity parameters are a function of how these circuit blocks are designed on the active device properties. From the active device side, one can say that the sources of nonlinearity in FETs, discussed in Chapter 3, are on the drain current source and in the gate-source and gate-drain capacitances. The power is mainly controlled by the current source and external load impedance. The efficiency depends on the losses in the devices and circuit blocks as well the unavoidable impedance mismatches. The linearity is a function of the relation between output current and input control voltage. It is also a function of the relation between the capacitances and voltages on the capacitor nodes.

### 5.3.1 Linear Amplifiers

Linear amplifiers are expected to introduce a minimum distortion to amplitude modulated signals, which is the case of digital waveforms. These signals have a high peak to average power ratio (PAPR) requiring operation at a certain backoff level from the  $P_{1\text{dB}}$  point, to avoid the amplifier peak voltage/current to hit the rail supply, but this is detrimental to the efficiency. Several approaches have been proposed to improve efficiency at high backoff levels and the Doherty scheme [2] is the most popular. Traditionally, amplifiers are designed by biasing all devices in class A and allowing only the power stage to compress. Besides, the driver is designed to provide a power 4 to 6 dB above the power required by the output stage. The objective is to avoid amplifying distortion signals from stages before the output and use terminations at the drain and gate causing minimum distortion. That technique results in low efficiency due to high DC power dissipation. Another design approach is to use different bias approaches to improve efficiency and still maintain a reasonable linearity. For instance, there have been reported amplifiers with the output stage biased in class A and the driver biased in class AB such that gain expansion is created, compensating the gain compression of the output stage [3]. That approach solves the linearity but degrades efficiency, thus against the trend of key requirements on a handset. Some means of linearization are required, following one of the many techniques found in the literature. The specifications for linearity in amplifiers for base stations are more stringent, and the problem has been solved by breaking the problem in two. The linearity is guaranteed by digital linearization performed at baseband, and the amplifiers are designed for best efficiency. The best load and source impedance can be measured with a load-pull system and the results can be applied to the design of the core amplifier. Additional relevant parameters in the design of amplifiers for digital applications are found in [4].

Ideally, a linear FET device has a flat transconductance over a wide range of input gate voltages. That means a perfectly linear relation between the drain current and the gate voltage,  $I_{ds}(V_{gs})$ . Unfortunately, this relation is only reasonably linear around a bias point and becomes mild and strongly nonlinear before reaching the limits. Therefore, the load delivering better power is not exactly the best for linearity. Hence, a trade-off between linearity and power is needed, optimizing both parameters. An important point to consider is that the input capacitance is more nonlinear in GaN HEMTs compared to GaAs pHEMT. The design has therefore to consider the input matching for better linearity. That means that conjugate matching at the gate may not be the best approach. In this case, the gain is traded off with linearity.

Before starting the design process, the engineer needs to carefully verify the linearity specifications. The conventional linear amplifier specification is the  $P_{1\text{dB}}$  power and the corresponding intercept point of the products of the third order,  $IP_3$ . The power of the intermodulation distortion (IMD), in particular the third and fifth, is, in general, specified for a desired output power. In modern applications, the signals are digitally modulated and other parameters are used to qualify an amplifier. The most important are the adjacent channel power ratio (ACPR) and error vector magnitude (EVM) detailed in Chapter 3. The ACPR characterizes the distortion levels in adjacent channels. It is expressed in dBc and is determined by the ratio between the total integrated power adjacent to the signal band and the total power contained within the signal band. The EVM describes how distortion affects the quality of signals contained within the signal band. It is expressed by the ratio between the sum of all vector errors and the sum of ideal signal vectors.

### 5.3.2 Power Amplifiers

Nonlinear, saturated, GaN amplifiers showing gain and efficiency over wide bandwidths have been successfully realized in the past two decades in monolithic technologies. Hence, broadband power amplifiers are now employed in a number of modern military and commercial applications. The trend in using GaN HEMT power amplifiers to improve power and efficiency is very intense at this time. For this class of amplifiers, the linearity correction is left to the digital linearization techniques, usually applied at baseband.

Power amplifier requirements are similar to those of linear amplifiers, except that the output stage is biased in class AB and the driver is biased in class A or class AB. The ratio between the output device size and the driver should be 2 to 3 dB higher than the  $P_{1\text{dB}}$  required for the driver. Fortunately, the peak of  $g_m$  for GaN HEMTs occurs at a bias point not too far from pinch-off, making this the right bias for class AB. The efficiency can be made better than class A and the amplifier can be used at a higher compression level for higher power and efficiency.

The load impedance determined in Chapter 2 (or by load-pull), properly scaled to device size is used to design the OMN. The ISMN uses the same equivalent impedances. Both circuit blocks should be designed with low insertion losses. A power amplifier can be designed solely based on an accurate linear model. However, if the nonlinear model is available, it can help to improve the performance, and obtain parameters like efficiency and DC per stage.

### 5.3.3 High-Efficiency Amplifiers

In the design of a high-efficiency amplifier, the efficiency is specified for a particular output power. An important point to consider is the saturation of the driver stage as well, as there is no need for a sinusoidal waveform to be applied to the gate of the power stage [5]. Up to 5% more efficiency can be achieved if the driver is also designed to operate under saturation.

Both the driver and output stages are biased in class AB. The power stage is assumed to operate under saturation, between 3 and 6 dB of gain compression, while the driver is expected to saturate up to 2 dB. These numbers need to be adjusted to

the gain that the devices can deliver at the specific frequency of operation. Under compression, the core amplifier (i.e., both driver and power stages) should have a compressed gain higher or equal to 10 dB. The size ratio between the devices should be as high as possible, depending on the frequency of operation. The load value for efficiency starts with the load value for power. Its value is then increased trading off power and efficiency. More than 8% improvement is expected when the class A load is increased by 20%, at the cost of 1-dB reduction in power.

### 5.3.4 Design of OMN

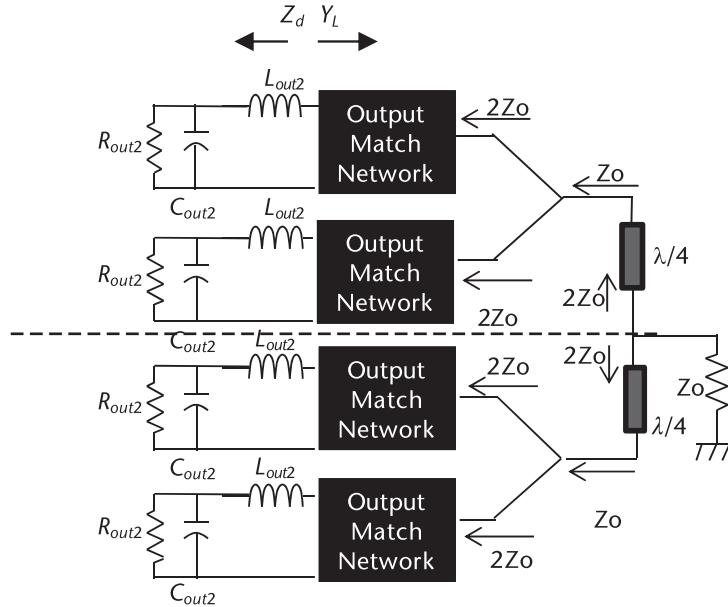
As mentioned, the OMN can be designed for a reference load, and optimized for power, efficiency, or linearity. The best way to determine these values is with the use of load-pull systems. The alternative, when such equipment setup is not available, is to rely on accurate linear and nonlinear FET models. It has been experimentally determined for GaAs FETs [6] that a drain load close to conjugate drain match delivers better linearity. This condition results in a severe reduction on the power performance. Simulations, using the EEHEMT model biased in class A, shows that a load resistance 15% higher than the value for power improves intermodulation performance with a reasonable 0.5 dB of power reduction.

The OMN detailed in Figure 5.3 is composed of four subblocks in parallel. Usually, we separate the output load at the center line of symmetry, as discussed in the section of combiners in Section 4.10.4. A simple solution contained in the OMN block is a resonator for the drain impedance, followed by a first section quarter-wave transformer to  $100\Omega$ . Both ends are tied to make a  $50\Omega$  impedance. The second section consists of a quarter-wave transformer connecting the resulting  $50\Omega$  to the output impedance of  $100\Omega$ . The ends of both sections, one from the top and one from the bottom, are connected together resulting in the  $50\Omega$  output impedance.

There are other approaches for the output match, which are discussed in Sections 5.4 to 5.7. The matching networks are, in general, designed for the central frequency of operation and will perform within bandwidths of less than 5%. To enlarge the band, computer optimization is employed for this purpose.

The drain impedance parameters  $R_{out2}$ ,  $C_{out2}$ ,  $L_{out2}$  are modeled according to the type of amplifier. The optimization goals are defined comparing the drain power impedance,  $Z_d$ , with the impedance looking towards the load,  $Z_L$ . The load impedance is inverted to obtain the load admittance, generating the equivalent output resistance in parallel with the output capacitance. Therefore, the admittance of each one of the four ports, connected at the drain, is extracted from the OMN S-parameter block, and modified by (4.87) to (4.91).

The first error function for optimization is obtained by comparing  $(R_d - R_L)$  over the band. Notice that  $R_d$  is not independent of frequency, due to its parallel configuration. However, as we are interested in narrow bands, we assume it to be constant. The second error function is obtained by comparing  $(X_d - X_L)$ . Both parameters are frequency-dependent and cannot be assumed to be constant. A third error function has to be set in place, related to the impedance at the output port looking towards the drain. The equivalent drain impedance is still given by the same circuit, but  $R_{out2}$  and  $C_{out2}$  values are different. The resistance is assumed to be constant up to the point of gain compression. Above that point, an average



**Figure 5.3** OMN with two sections of a two-way combiner.

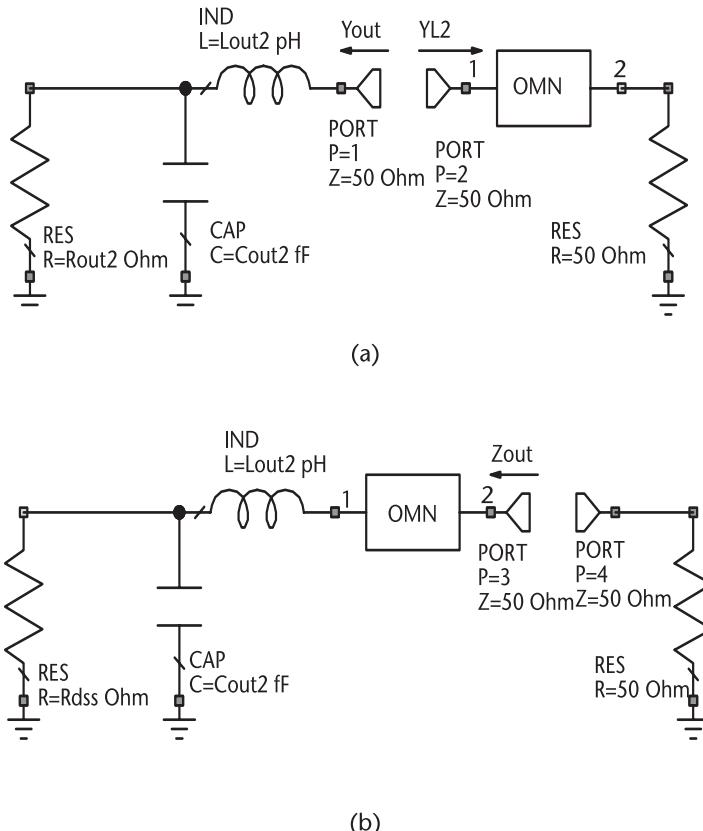
value is used, which is not so simple to determine. A similar effect happens with  $C_{out2}$ . We shall restrict our study by replacing  $R_{out2}$  by a small-signal resistance  $R_{dss} = 1.5$  to  $2R_{out2}$ . We also assume  $C_{out2}$  to remain constant. It is obvious that it is not possible to obtain a network that matches the drain load  $R_{out2}$  to  $50\Omega$  and, at the same time, matches  $50\Omega$  to  $R_{dss}$ .

Hence, we give priority to a perfect match to  $Y_L$ , maintaining the output port within a controlled mismatched value. Thus, the error function at the output termination is defined by a maximum output VSWR. In general, we use a return loss of 10 dB, corresponding to a circle of a VSWR equal to 2 on the Smith chart. The circuit in Figure 5.4 illustrates the test benches used in the optimization of the matching networks.

### 5.3.5 Design of the ISMN

The ISMN is designed for trading off gain, linearity, efficiency, and power, depending on the amplifier purpose. The driver can be designed such that its  $P_{1dB}$  is 2 to 6 dB higher than the power required to feed the power stage. There remains the problem of dissipating the heat generated by GaN HEMT amplifiers biased in class A. That may limit how much power an MMIC will be able to provide under reliable operation. This block is as important as the OMN. For an amplifier designed for power and efficiency applications and presenting a high gain in the power stage, say, above 13 to 16 dB, then the ISMN can be optimized for gain. Thus, the OMN is optimized for the impedance delivering the desired power, and the remaining part of the circuit is optimized for maximum and flat gain.

If the power stage has gain below 10 dB, there are restrictions in the ISMN design. The objective is to match the drain impedance of the driver to the gate impedance of the power stage as well as possible. However, there is an impossibility



**Figure 5.4** Defining goals for circuit optimization: (a) determination of  $Y_L = Y_d^*$ , and (b) determination of output return loss.

to carry on the design with such goals. To verify this statement, let us analyze the circuit of Figure 5.5, starting from the gate of the power stage. Let us assume that both devices are of the same size.

The ISMN should transform the power gate impedance,  $Z_{g,pa}$ , to the impedance presented to the drain,  $Z_{L,dr}$ . Starting from the driver stage drain impedance,  $Z_{d,dr}$  towards the power stage gate, the resulting source impedance for the power gate stage,  $Z_{s,pa}$ , is different from  $Z_{g,pa}$  affecting power stage gain. The only condition when a reasonable match is achieved is when the driver drain and power stage gate are conjugate matched. In such a case, the  $Z_{s,pa} = Z_{g,pa}^*$ , and,  $Z_{L,dr} = Z_{d,dr}^*$ . This condition is not feasible over the frequency band; besides, there is a natural mismatch required for power, which implies  $Z_{L,dr} \neq Z_{d,dr}^*$ . This situation is more critical in the ISMN compared to OMN, where one side of the circuit block is a  $50\Omega$  termination. The ISMN has to match two complex impedances. The solution to design the interstage match involves design with circles of constant gain, for each frequency, which is time-consuming and is not necessary.

The first design goal is to conjugate match the gate impedance,  $Z_{g,pa}$  to  $Z_{s,pa}$ , assuming that the drain termination is conjugate matched to the small signal  $Z_{dss,dr}$ . The second goal is to optimize the drain impedance for a fixed mismatch between  $Z_{dss,dr}$  and  $Z_{L,dr}$ , assuming that the gate side is conjugate matched. Two benches are used for this optimization, one for each goal.

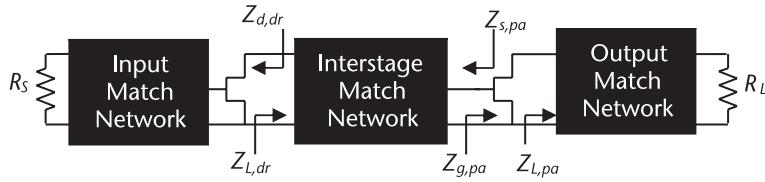


Figure 5.5 Matching block representation.

For a linear amplifier, the interstage is more complex. A recent publication pointed out the importance of the gate match on the linearity of a GaN HEMT device [7]. In order to verify this proposal, let us use the model in Figure 5.6 to represent the transistors in Figure 5.5.

The input capacitance represents the effect of the gate-source capacitor and the contribution of gate-drain capacitor after applying the Miller theorem. Because the voltage gain,  $A_v$ , is greater than 1, we can neglect the effect of the gate source capacitance on  $C_{\text{out}}$ . However, it does increase the value of  $C_{\text{in}}$ .

The gain of the output stage, including OMN, the load  $R_L$ , and the ISMN driven by an equivalent Thévenin generator with impedance  $R_S$ , is given by (5.8). The parameter  $Y_{22}$  in the equation represents the Y-parameter of the ISMN circuit block, while  $Y_{21}$  represents the device transadmittance. The phase response for the circuit is given by (5.9).

$$A_v = g_m R_L \quad (5.5)$$

$$C_{\text{in}} = C_{gs} + C_{gd} (1 - A_v) \quad (5.6)$$

$$C_{\text{out}} = C_{ds} + C_{gd} \left( 1 - \frac{1}{A_v} \right) \quad (5.7)$$

$$\frac{V_L}{V_S} = \frac{Y_{21}}{Y_{22} + j\omega C_{\text{in}}} g_m R_L \quad (5.8)$$

$$\angle \left( \frac{V_L}{V_S} \right) = \tan^{-1} \left( \frac{\text{Im}(Y_{21})}{\text{Re}(Y_{21})} \right) - \tan^{-1} \left( \frac{\text{Im}(Y_{22}) + \omega C_{\text{in}}}{\text{Re}(Y_{22})} \right) \quad (5.9)$$

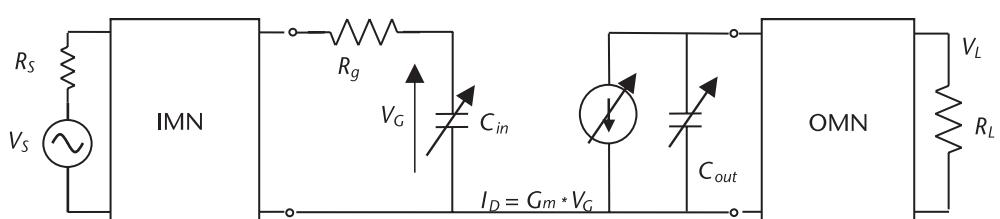


Figure 5.6 Nonlinear model for the FET. (After: [7]. © 2016 IEEE.)

The AM-to-PM is defined as the variation of the phase of the voltage gain  $V_L/V_S$  as a function of the signal drive level. The sensitivity of the  $\tan^{-1}(x)$  is maximum for  $x = 0$ , so that maximum variation on the phase occurs at the conjugate matched conditions when  $\text{Im}(Y_{22}) + \omega C_{\text{in}} = 0$ , assuming that the other terms are constant. The proposal in [7] is to mismatch the gate of the output device to minimize AM-to-PM distortion. The trade-off is the reduction on the amplifier gain. This is an interesting technique to minimize distortion when the amplifier gain is high. The effect of distortion coming from the driver as proposed by the same reference can be minimized by using a larger device size and a lower drain load. According to (5.10), this will minimize the effect on the input capacitance. Therefore, this requirement is in agreement with the conventional process of using a device with 6 dB of power margin for the driver amplifier, in the case of linear amplification.

A typical block diagram for the ISMN of a high power amplifier is in Figure 5.7 composed of two subblocks. One is located next to the gate consisting of four parallel matching networks, and the other is located next to the drain. The joining of both networks can be defined as the intermediate node point. An inverter is also shown at this point to be used in case of conflict between the resonant circuits. Both subblocks are assumed to contain a resonator and a quarter-wave transformer. In such a circuit, it may be difficult to control the mismatch on the gate impedance.

### 5.3.6 Design of Complete Amplifier

If the complete amplifier has only two amplification stages, the IMN has to match the amplifier input impedance and equalize the gain. It is unlikely that only one ISMN and one IMN circuit block can fulfill these objectives. One solution would be to optimize the ISMN for gain as well. An alternative is to add an equalizer circuit to

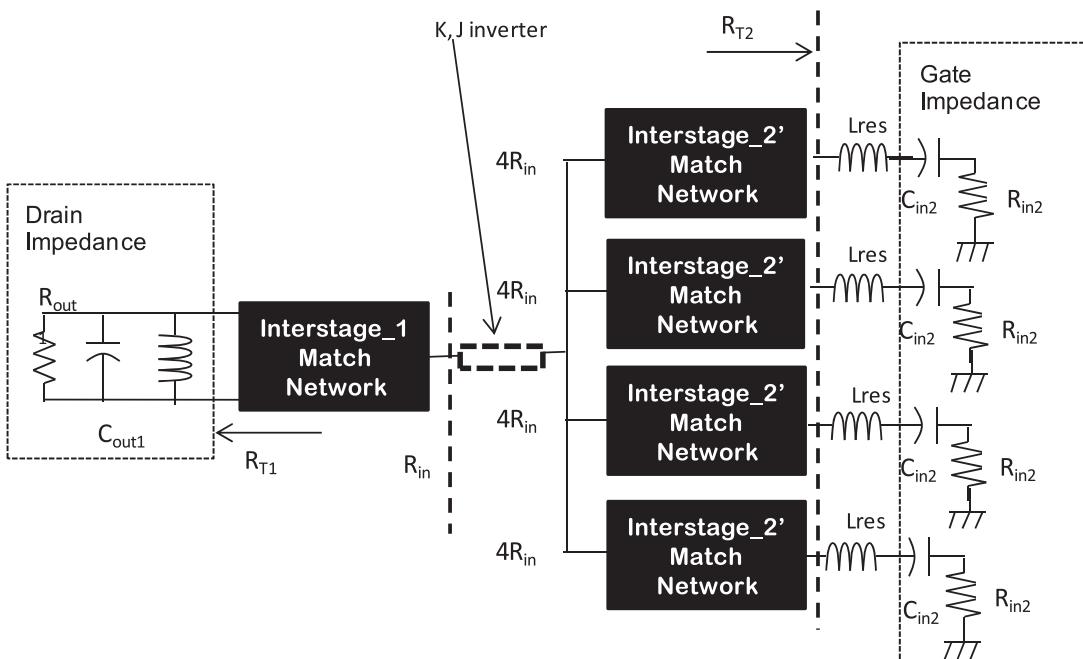


Figure 5.7 ISMN impedance match and power divider.

the input of IMN, where the excess gain at lower frequency is absorbed by resistive elements. If the amplifier has three or more stages, then there are more matching blocks to share the task of flattening the gain. The amplifier stages placed before the drivers are considered linear and are optimized following conventional methods.

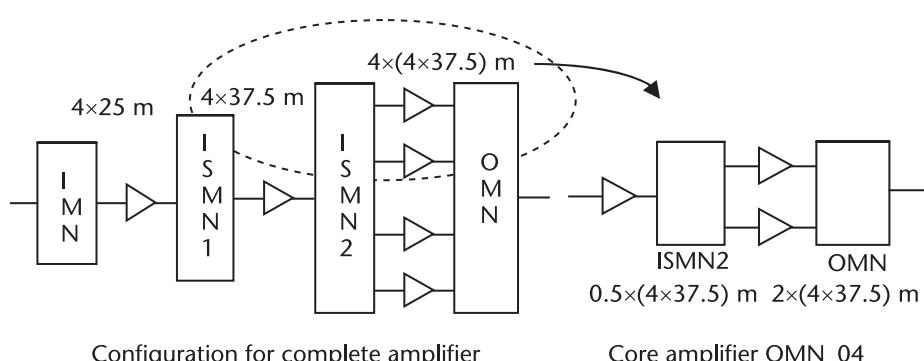
Once the equivalent drain and source impedances are determined, we can proceed to the design of the matching networks. They can be synthesized using the application tools available in commercial software packages. In this book, we make use of the Smith chart as it gives a better sense of the purpose of the elements used in the matching. In order to clarify the design methodology, a few case studies will be addressed, based on the circuit options listed in Table 5.3. The first case study will introduce the design details of a complete amplifier following option 4. The second case study will be concerned with the design of the circuit blocks OMN and ISMN2 for a 3:1 transformer/combiner. The third case study discusses the design approach of a linear amplifier, and the last case study is on the design of an amplifier for application on 5G New Radio.

## 5.4 Case Study: High-Efficiency Amplifier

In this section, we will describe the design process for a high-efficiency amplifier, operating at 75 GHz. The bias was selected to be at  $V_{GS} = -1.75V$  for maximum small signal gain and efficiency. The transistor lineup was taken from option 4 of Table 5.3. This is the option with the highest ratio between the driver and the power device size, more adequate for high efficiency. The block diagram in Figure 5.8 illustrates the amplifier topology.

We can extract from this block a core amplifier composed of two output parallel devices driven by a device half the normal size. It is easier to design half the circuit and then parallel both halves. After paralleling, adjustments are made to account for coupling effects.

Another important trade-off is on the real part of the power device input impedance. It decreases with the increase in the drain load, and in this particular case, it drops from  $4\Omega$  to  $3\Omega$ . This fact causes losses and bandwidth reduction in the interstage circuit. To facilitate distinction between the complete amplifier and the core amplifier, the former will be denominated 4 and the latter 04.



**Figure 5.8** Amplifier topology for option 4.

### 5.4.1 OMN\_04

The OMN is developed as two sections of two-way combiners, similar to the two-way circuit of Figure 4.65. The DC load resistance for this size of device for best power performance is equal to  $100\Omega$ . If we increase this value by 20%, we can increase the efficiency by 5% at the cost of a 0.8-dB drop in the output power. The other elements in the equivalent drain circuit are in Figure 5.9. This one-way circuit is useful in the determination of the basic matching elements. The equivalent drain circuit is resonated with a series transmission line and a shunt open stub. The shunt stub makes the trace of the impedance on the Smith chart to be closer to an ideal RLC series circuit, as discussed in the topic on source/load resonance circuits. A shunt lumped capacitor can be used instead and, in particular, a capacitor on top of a via if it is available in the foundry process. Notice that the external load is  $100\Omega$ , because this circuit is designed to be paralleled forming a 4:1 transformer/combiner.

In this example, the open stub was eliminated because there is no space in the layout to insert an open stub when three or more unit cells are paralleled. The matching circuit is a Type-C prototype.

The impedance from both ports is shown in the Smith chart of Figure 5.10. It shows clearly that port 1 behaves close to a series RLC circuit and port 2 behaves as a parallel RLC. The  $Q$  of the resonated circuit is equal to 3, given according to (4.68), a flat bandwidth of 12.5 GHz for a center frequency of 75 GHz.

The schematic in Figure 5.9 is a convenient format to represent resonant circuits, but it does not inform the impedance at the device terminal. Therefore, the resonant circuit is moved to the matching circuit side, resulting in the representation of Figure 5.11. The transmission-line parameters are determined from equations presented in Chapter 4 and are reported in the figure.

The optimization is performed with two test benches. In the first bench, represented in Figure 5.12(a), the circuit parameters are optimized for the parallel equivalent impedance at port 2. The drain impedance is defined as  $R_{L2} = 1/\text{real}(Y_L) = 100\Omega$  in parallel with  $X_L = 1/\text{imag}(Y_L) = j32\Omega$  at the central frequency. In the second bench, represented in Figure 5.12(b), the impedance at port 2 is defined for the drain terminated with a small-signal resistance, estimated to be  $177\Omega$  for this device. The goal is a return loss of 10 dB, corresponding to a VSWR circle of radius equal to 2. For this particular circuit, the initial parameters in Figure 5.12 already met the required impedance. Notice that the optimization is made for the circuit impedance and not the reflection coefficient.

The rectangular representation of impedance is more convenient for the impedance at port 2; thus, the real and imaginary parts of the parallel equivalent

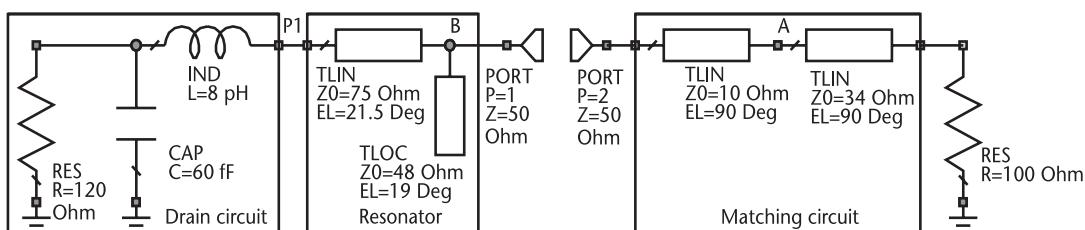


Figure 5.9 OMN\_04 one-way matching circuit.

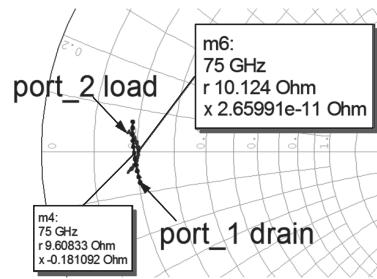


Figure 5.10 OMN\_04 impedance traces on the Smith chart.

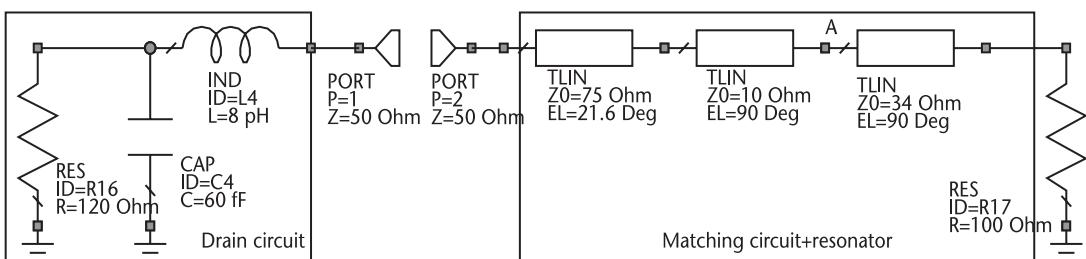
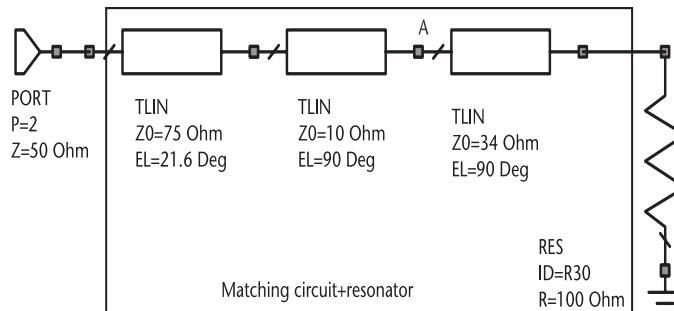
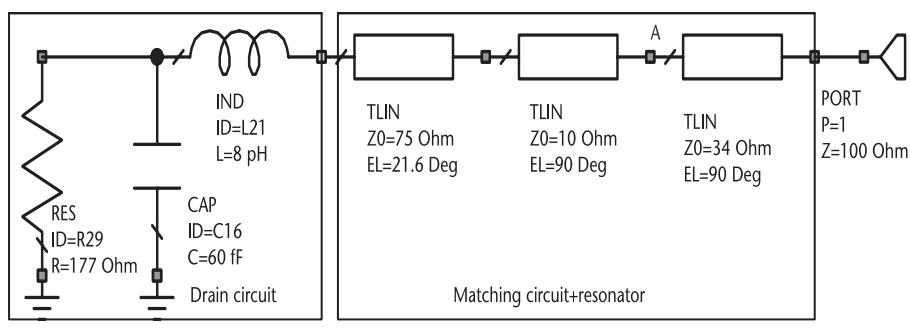


Figure 5.11 OMN\_04 modified output circuit.



(a)



(b)

Figure 5.12 OMN\_04 for the initial and optimized circuit: (a) measurement of  $Y_2$ , and (b) measurement of dB ( $S_{22}$ ).

impedance for the initial circuit are shown in Figure 5.13. The top curve represents the drain load resistance, showing a variation between  $95.6\Omega$  and  $107\Omega$ . According to (4.94), we can expect a power variation of  $\pm 0.2$  dB over the band. The bottom curve shows the load reactance, relatively flat at  $j32\Omega$ . Ideally, this line should have a slope opposite to the slope of the drain circuit. The results show that the bandwidth specification can be met.

The next step is to transform the 1:1 circuit to a 2:1 combiner/transformer. This process was discussed in Chapter 4 on the topic of a two-way combiner design where two options were presented. We selected the option from Figure 4.66(b), which shows a low characteristic impedance for the transmission line between nodes A and B. Therefore, we added a short shunt stub close to the  $50\Omega$  termination to raise the characteristic impedance of that line.

The modified ideal transmission line circuit was converted to a 2:1 microstrip version, as shown in Figure 5.14. A TEE microstrip element was used to function as a 2:1 combiner. A series capacitor was added for DC blocking purposes. The values indicated in the figure were obtained after the circuit optimization, following the same targets used for the ideal transmission-line circuit. The shunt stub can also be used for bias insertion in the circuit.

When designing stubs for bias insertion, in particular, on the drain side, one needs to account for the amount of DC current. The transmission-line thickness, besides the line width, determines how much current can be allowed. It is specified by most foundries in mA/ $\mu\text{m}$ . We assumed this value to be  $15\text{ mA}/\mu\text{m}$ . The microstrip-line circuit for the complete 4:1 combiner, obtained by paralleling two circuits contained in Figure 5.14, is shown in Figure 5.15.

The following modifications were performed in the combined circuit. After attaching the mirror image to the circuit, the termination was changed to  $50\Omega$ . Then the element representing two coupled lines was replaced by the representation of four coupled lines. The center arms of power combiner were allowed to have different impedances relative to the external arms during the optimization process.

The impedances at the device terminals, ports 2 to 5, are shown in Figure 5.16(a), expressed in terms of resistive and reactive components. The top curves

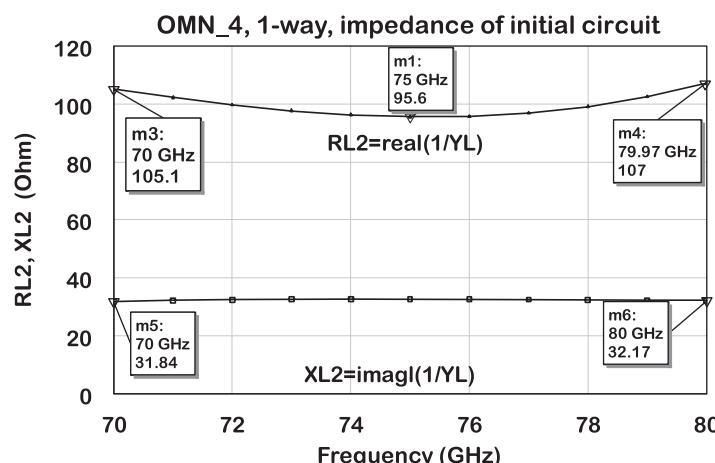
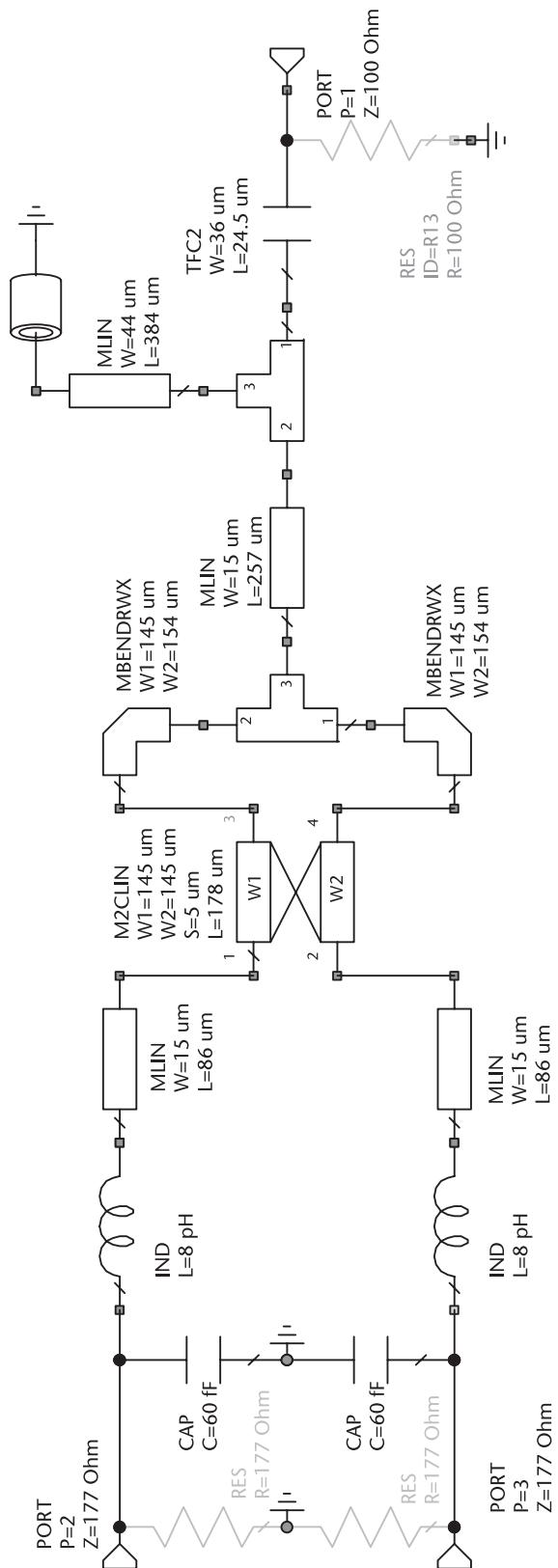


Figure 5.13 OMN\_04 load impedance of the initial circuit.



**Figure 5.14** OMN\_04 microstrip line version.

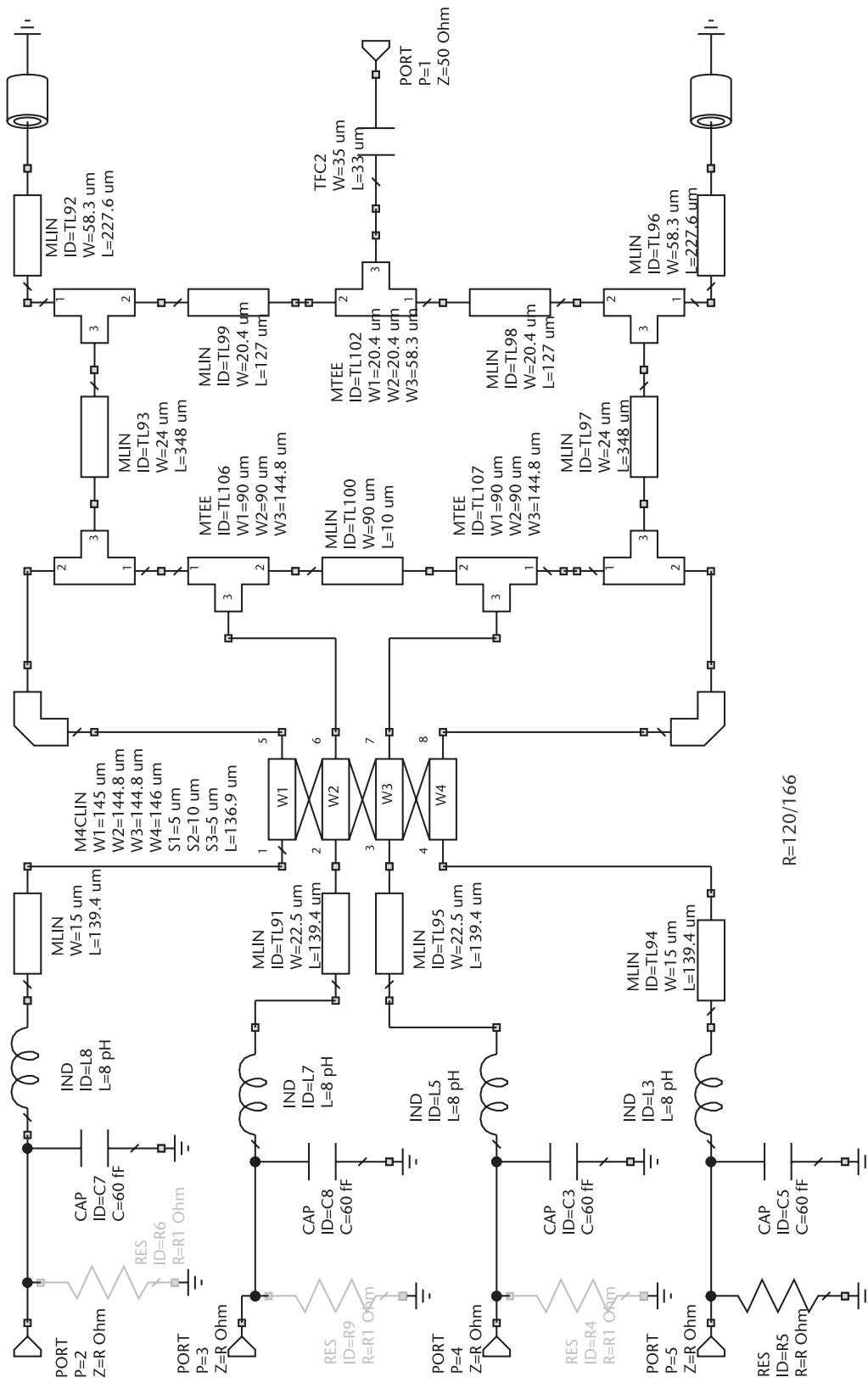
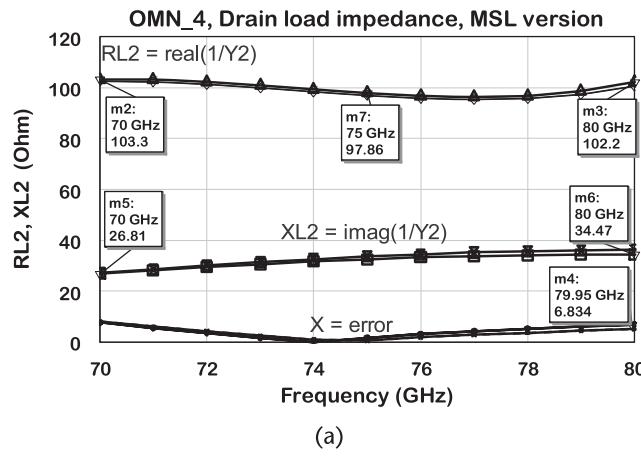


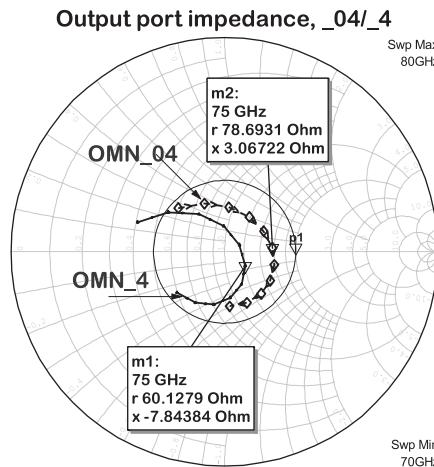
Figure 5.15 OMN\_4 complete 4:1 combiner/transformer.

show that the real part changes from  $97\Omega$  to  $103\Omega$ . The middle curve shows the reactive part, which is equal to  $j26.8\Omega$  at the low end and  $j34.7\Omega$  at the high end. The bottom curve shows that the maximum reactance error compared with ideal case is equal to  $+j6.8\Omega$ .

The impedance at the output port looking towards the drain is shown in Figure 5.16(b), compared to the impedance of half the circuit. The drain termination for this evaluation is near the device  $S_{22}$ . Power is determined by the amplifier external load. Thus, a mismatched load changes the output power. In order to check the effect of the external load VSWR on the drain impedance, we applied a tunable load in place of the  $50\Omega$  termination. The mismatch was adjusted for a VSWR of 1:1.2 and the phase was rotated from  $0^\circ$  to  $360^\circ$  with  $20^\circ$  steps. This setup was applied to port 1 of the circuit in Figure 5.16 to investigate the effect of an external termination on the FET load,  $Z_L$ .



(a)

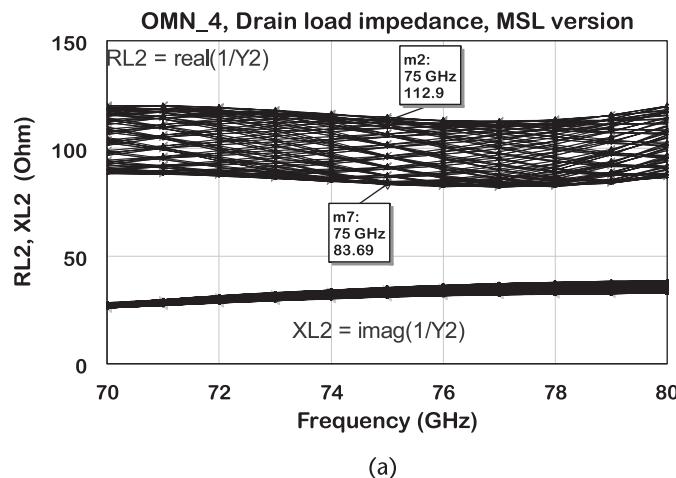


(b)

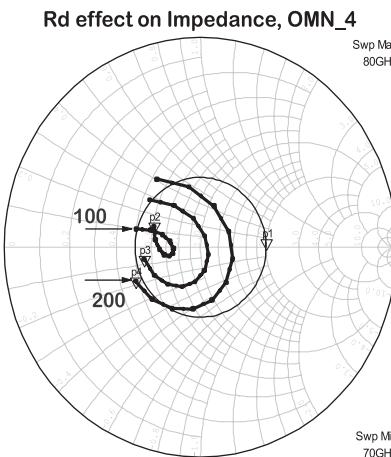
**Figure 5.16** Impedances for the circuit block OMN\_4: (a) drain load impedance versus frequency, and (b) output port drain matched to  $S_{22}$ .

The effect on the external load resistance on the internal drain load is observed in Figure 5.17(a). That corresponds to a variation from  $-0.68$  to  $+0.7$  dB on the nominal power. The effect of a VSWR of 1.5 may degrade power by more than 1.5 dB. However, the effect of internal load on the output impedance is shown in Figure 5.17(b). The drain resistor was changed from the best match for power to a small-signal equivalent, corresponding to  $R_d = 200\Omega$ . In the plot, that resistor was changed from  $100\Omega$  to  $200\Omega$ . The best match corresponds to  $100\Omega$ , corresponding to the resistor for power.

It is also important to verify the circuit balance in terms of amplitude and phase. In principle, if the impedances are correct, one would expect a good balance. Verification requires evaluating the transfer parameters between the four drain ports to the  $50\Omega$  port in Figure 5.15. Notice that the port impedance is a small-signal value, in this case, equal to  $177\Omega$ . The S-parameters are then measured in relation to port 1 terminated in  $50\Omega$ . The circuit balance in terms of insertion loss for that circuit is shown in Figures 5.18(a) and 5.18(b).



(a)



(b)

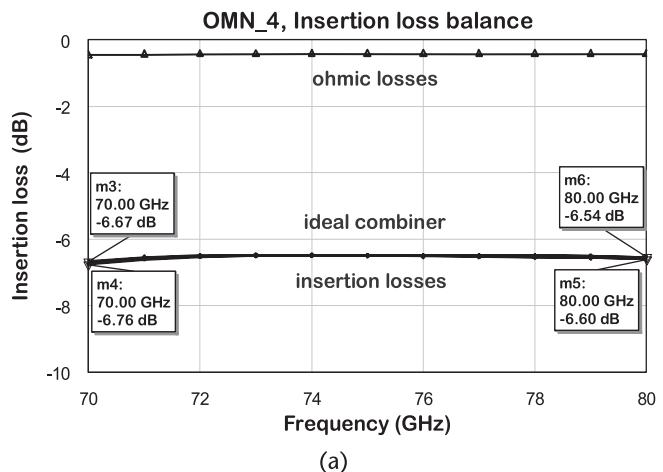
**Figure 5.17** Effect of terminations on the impedances: (a) effect of load of VSWR 1.2 on load impedance, and (b) output impedance vs internal load.

Figure 5.18(a) shows a maximum insertion loss of 7.0 dB at the low end and reaches a minimum of 6.6 dB at the center of the band. Comparing with the theoretical loss for a 4:1 divider, that is, 6 dB, we find an insertion loss ranging from 0.5 to 0.9 dB.

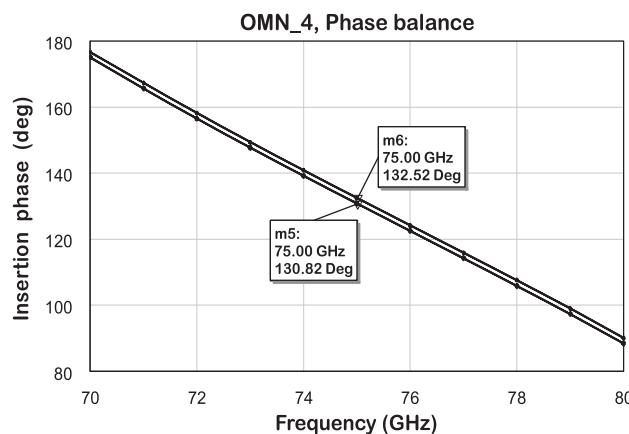
The ohmic losses were found by tying all four ports of the combiner and calculating the circuit MAG. There is 0.5 dB of ohmic losses in the circuit, showing perfect match between 72 and 78 GHz and 0.5 dB due to mismatch near the band edges. The phase balance is depicted in Figure 5.18(b). It shows about 2° difference over the band between all four ports.

#### 5.4.2 ISMN2\_4

The design of the ISMN starts by resonating the driver drain to the gate of the power stage. The resulting impedance at the center frequency is real and can be designated by  $R_g$  for the gate circuit and  $R_d$  for the drain circuit. In case we use a transformer/divider in the amplifier design, it is convenient to define an intermediate reference



(a)



(b)

**Figure 5.18** OMN\_4 port amplitude and phase balance: (a) insertion loss balance for the output circuit, and (b) insertion phase for the output circuit.

resistance at the point where the divider is created. This resistance is defined by the equation,  $R_{ref} = \sqrt{R_g R_d}$  relating  $R_d$  and  $R_g$ . Part of the circuit matches  $R_d$  to  $R_{ref}$  and another part of the circuit matches  $R_{ref}$  to  $R_g$ . In the case of this project, half of the driver corresponds to  $R_d = 200\Omega$  and two paralleled power devices correspond to  $R_g = 2\Omega$ . Thus, the first value for  $R_{ref}$  is  $20\Omega$ .

Let us start with the representation of drain and gate impedance. Figure 5.19 shows the driver equivalent circuit on the left consisting of half of  $4 \times 37.5 \mu\text{m}$ . The gate equivalent circuit is on the right representing the parallel association of  $2 \times (4 \times 37.5 \mu\text{m})$  unit cells. In the same figure, one can observe on the left, a series transmission line and a shunt capacitor that resonates the drain circuit impedance. On the right, a series transmission line resonate the impedance at node B. The real part of impedance at port 1 is equal to  $14.2\Omega$ . The impedance at node B without the shunt capacitor is  $1.92\Omega$ . The low impedance on the gate side needs to be increased by means of a shunt capacitor. A short transmission line is inserted between node B and port 2 for the best fit to RLC trace. The capacitor is determined by making use of a lumped single cell matching to raise the impedance to  $20\Omega$ . A shunt capacitor of  $320 \text{ fF}$  and a series inductor of  $12 \text{ pH}$  are required for the matching. The series inductor is absorbed by the series resonant line. The additional short line to port 2 is for best fit into a parallel RLC circuit.

The resulting impedances at each port are shown in the Smith chart of Figure 5.20(a), resulting in  $14.2\Omega$  on the drain side and  $20\Omega$  on the gate side, at the resonant frequency. Inserting a Type-C network consisting of two quarter-wave transformers with characteristic impedances of  $Z_1 = 20\Omega$  and  $Z_2 = 17\Omega$ , we obtain the matched impedance shown in Figure 5.20(b). Notice that  $Z_1$  was inserted in port 1 and  $Z_2$  was inserted in port 2.

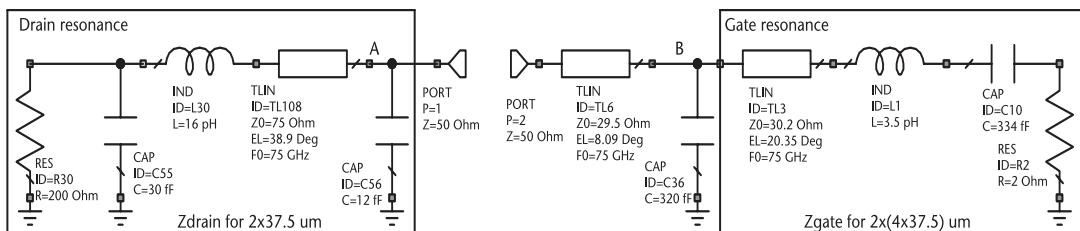


Figure 5.19 One-way interstage circuit.

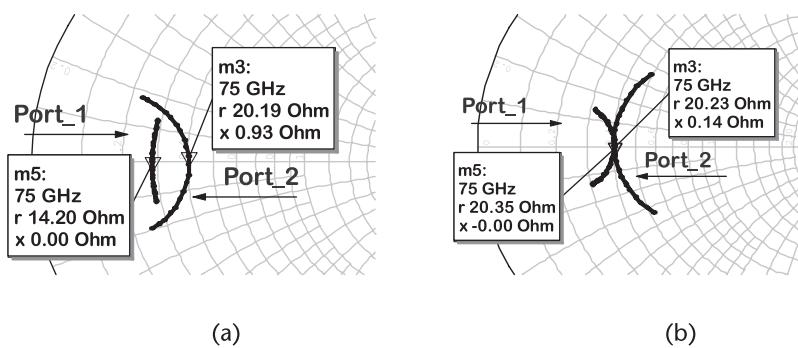


Figure 5.20 Drain load and gate source impedance in the Smith chart: (a) circuit of 1-way interstage, and (b) Type-C matched circuit.

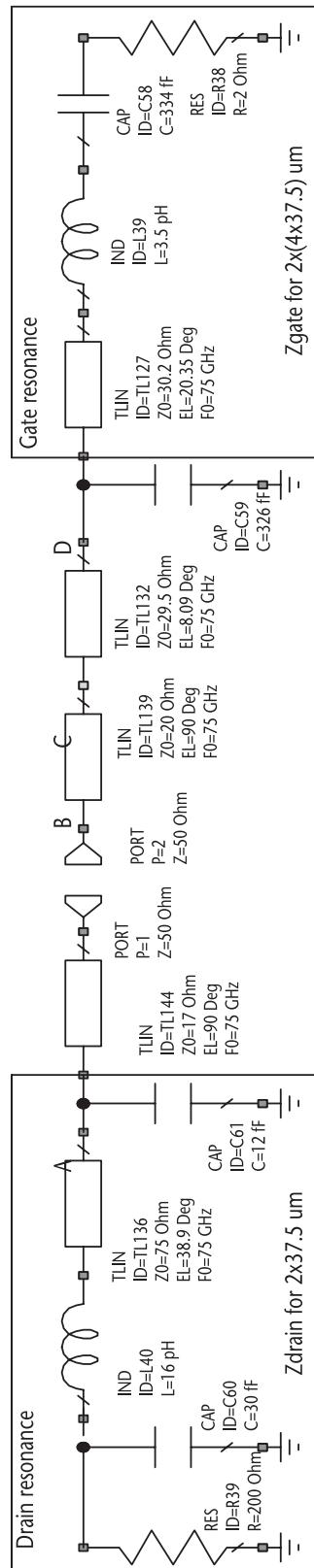


Figure 5.21 Schematic of ISMN2\_04 matching circuit block with ideal lines.

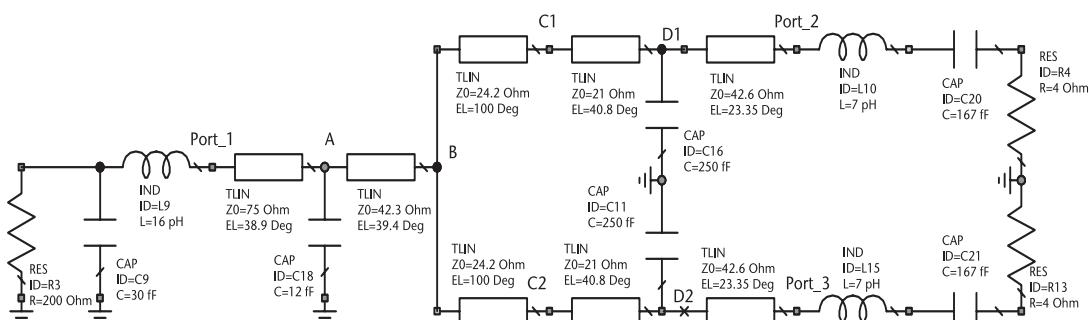
The circuit in Figure 5.21 can be transformed into a power divider, by splitting the circuit at node B, in the desired divider. The circuit was transformed into the format illustrated in Figure 5.22. The selected node B for the power divider is at the  $R_{ref} = 20\Omega$  level. The shunt capacitor attached to node A can be replaced by an open stub. The shunt capacitors on nodes D<sub>1</sub>, D<sub>2</sub> are more problematic. The distance between gates is around 100  $\mu\text{m}$  to 200  $\mu\text{m}$ , so there is not much space between the ports to insert an open stub. Virtually, it is the same problem found in the design of OMN circuit block. The shunt capacitor on top of via is a good solution for a parallel reactance, but one has to evaluate the following factors. This form of capacitor has been proposed as a DC bypass, where a large capacitance is built on top of the bias.

As a result, some foundries have restrictions to build small-size capacitors over via. If the circuit performance is too sensitive to the capacitance and cannot tolerate the variation with process, then it is not adequate for impedance matching. This two-way circuit was converted to a microstrip (MS) equivalent, shown in Figure 5.23. The divider core itself is a T-junction connecting the lines from the drain to the two gate lines. A couple of bends were also added to facilitate the building of the layout.

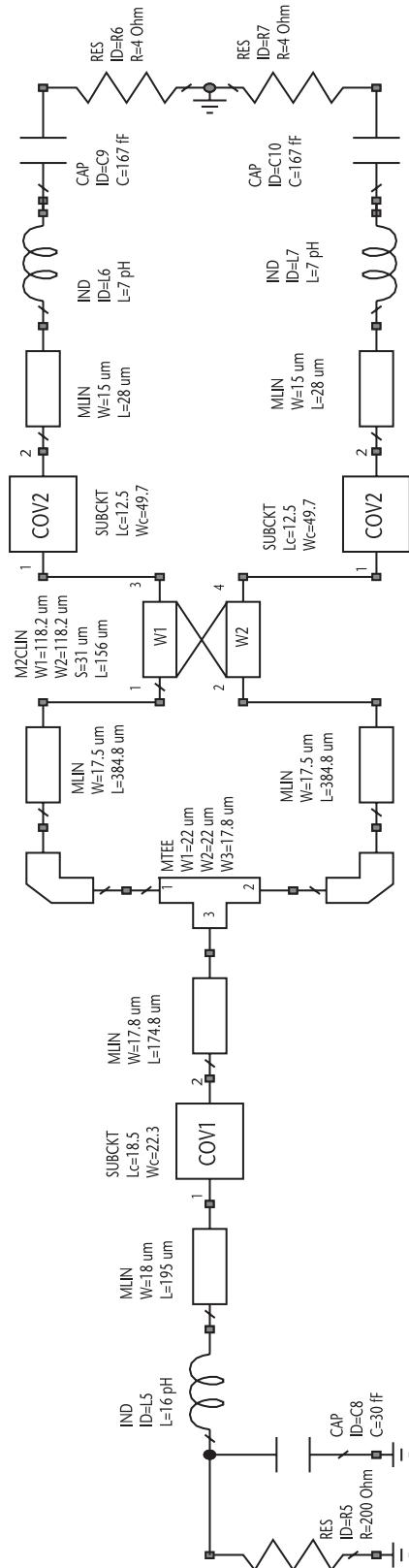
A coupled-line model was also introduced to take into account the coupling between the large-width transmission lines. This circuit was submitted to optimization to provide the desired impedances at the ports. The final step for this block is to parallel two of these circuits in order to obtain a full 1:4 divider/transformer. The schematic for the complete microstrip version is shown in Figure 5.24. It consists essentially of the same circuit in (5.23) with the addition of lines to build the input two-way power splitter, and modifications in the coupled lines from 2 to 4.

The final parameters for the microstrip elements are in the same figure. Notice the only connection between the two halves is in the coupled area. In some instances, two Tee elements are used to connect node D<sub>1</sub> to node D<sub>2</sub>. This connection, in general, affects the circuit balance. Therefore, the decision to use a connection is made when checking the balancing of amplitude and phase. In this particular circuit, there is no need to connect the two nodes.

Let us look at the performance of the circuit shown in Figure 5.24. The gate source impedance in Figure 5.25(a) shows a real part ranging from  $3.8\Omega$  to  $4.2\Omega$ . However, the minimum value for the imaginary part is  $j8.2\Omega$  and the maximum



**Figure 5.22** Building the 2:1 combiner by paralleling the circuit at node B on the right.



**Figure 5.23** MS EE schematic for the half ISMN2\_04 circuit.

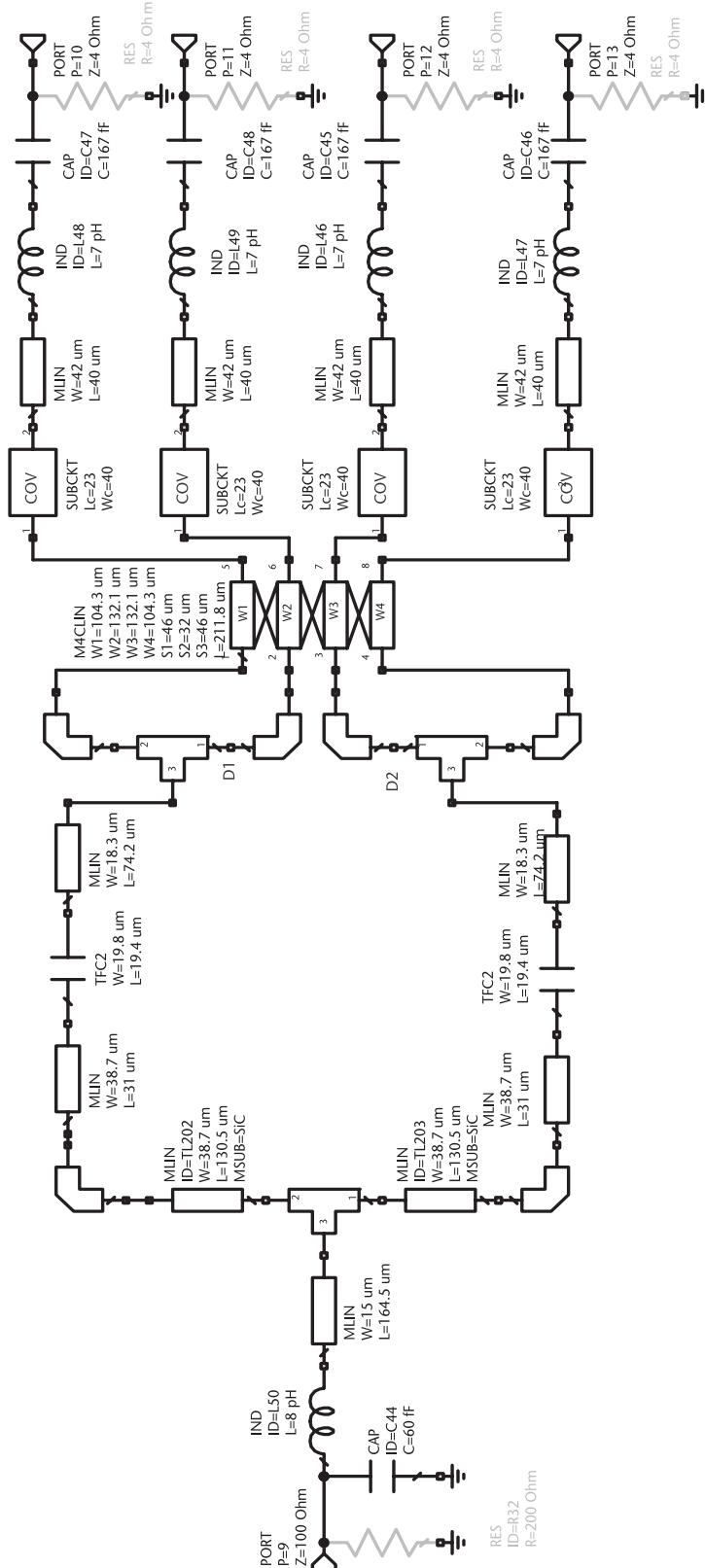
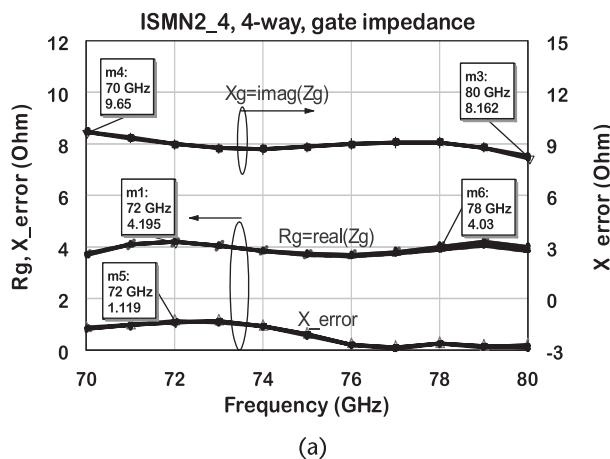


Figure 5.24 MS EE version of the ISMN2\_4 circuit block.

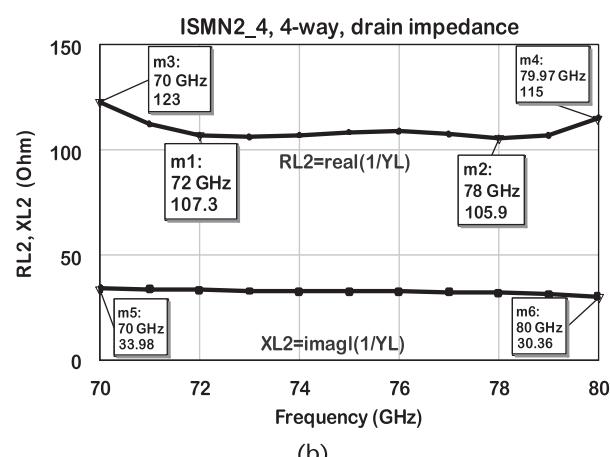
value is  $j9.65\Omega$ . These variations, taken to the linear circuit of Chapter 2, show a 0.5-dB gain variation, relative to the ideal value.

This variation can be absorbed by the gain compression of the driver and power stages. The drain impedance in Figure 5.25(b) shows a real part ranging from  $106\Omega$  to  $123\Omega$ . Compared to the value for maximum power,  $80\Omega$ , 0.9-dB reduction from the maximum power over most of the band is expected. The effect of drain resistor on the gate impedance is illustrated in Figure 5.26(a). It can be observed that a variation of  $\pm 15\%$  in  $R_d$  does not much affect the real and imaginary parts of the gate impedance.

However, the circuit is more sensitive to gate capacitance. A variation of  $\pm 5\%$  on the gate capacitance is shown in Figure 5.26(b) to cause  $\pm 15\%$  variation on the resistance presented to the drain. The gate resistance can change by  $\pm 10\%$  with negligible effects on the drain impedance. In general, if the designed circuit performs well over the desired frequency band, it should also show a good balance between the ports. The balance can be verified by simulating  $S_{21}$  in magnitude and

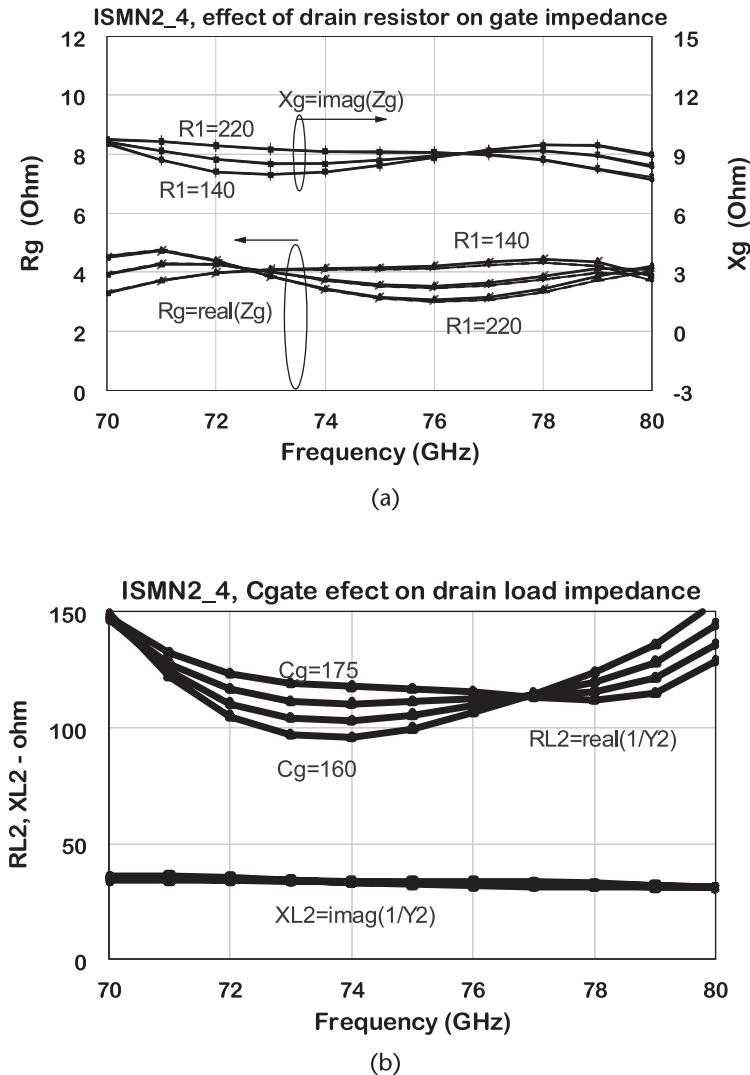


(a)



(b)

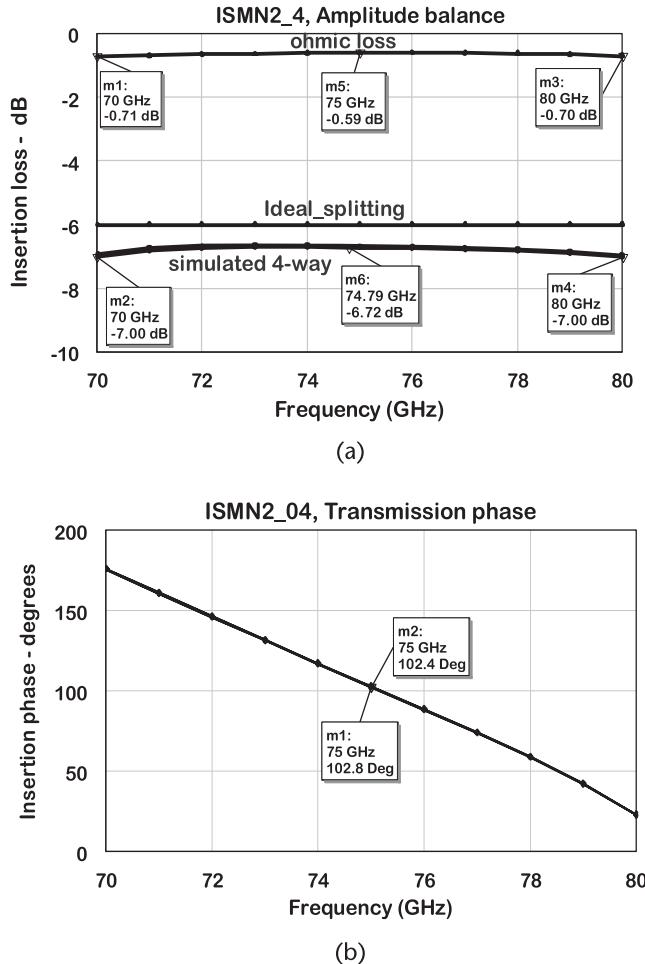
**Figure 5.25** Impedance curves for ISMN2\_4: (a) gate impedance for  $R_{dss} = 177\Omega$ , and (b) drain impedance for a matched gate.



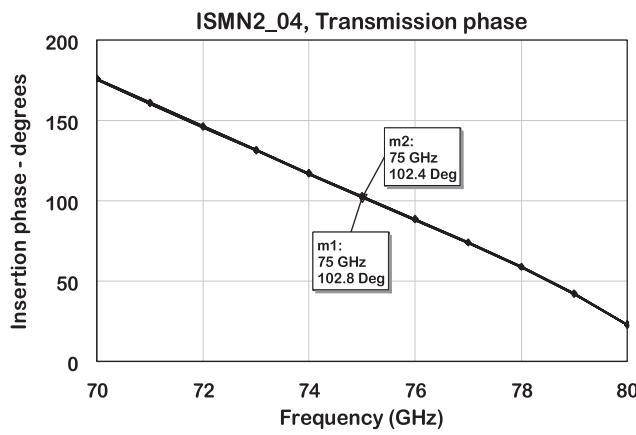
**Figure 5.26** The effect of terminations on the ISMN2\_4 port impedances: (a)  $Z_{s,pa}$  with a small signal impedance at the drain, and (b)  $Z_{L,dr}$  impedance for matched gate.

phase from the internal drain resistance to the internal gate resistance. The insertion loss in Figure 5.27(a) shows an insertion loss between 7.0 and 6.7 dB. This result compares favorably with the ohmic losses, averaged to be equal to 0.6 dB plus the ideal power splitter loss of 6 dB, so there are a total of 6.6-dB losses for most of the band. The insertion losses falls off by 0.4 dB at the edges of the frequency band. The insertion phase appears in Figure 5.27(b), showing a well-balanced circuit, causing a phase shift of 102° at the center of the band. The insertion loss is measured with  $R_d = 100\Omega$  and  $R_g = 4\Omega$ .

In case the amplitude and balance of the circuit are more than 1 dB, one should add the insertion parameters to the optimizer and run the software to improve the overall performance. If it cannot be minimized, then the driver device needs to be increased in size, in order to give at least more power. We can choose another



(a)



(b)

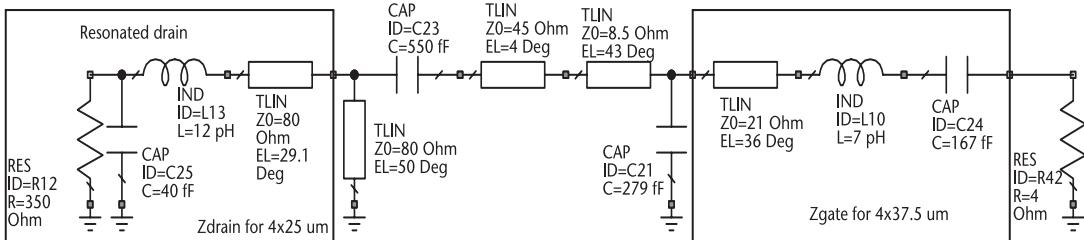
**Figure 5.27** Amplitude and phase balance of ISMN2\_4: (a) balance of insertion loss, and (b) balance of the insertion phase.

configuration from Table 5.3 with a lower ratio between the driver and power devices. For instance, if we change the ratio of 1:4 to 1:3, one can obtain about 1 dB more power from the driver.

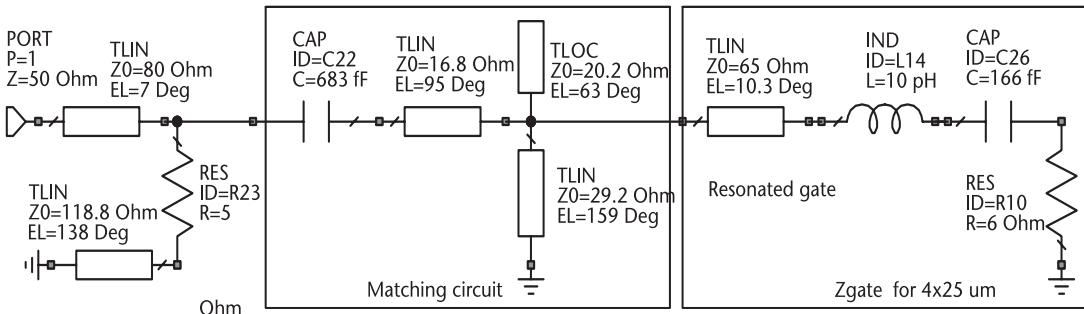
#### 5.4.3 ISMN1 and IMN

The circuit block ISMN1 is inserted between a predriver device measuring  $4 \times 25$   $\mu\text{m}$ , and the driver device measuring  $4 \times 37.5$   $\mu\text{m}$  (shown in the block diagram of Figure 5.8). The basic circuit schematic for ISMN1 is in Figure 5.28. The drain circuit is resonated with a series line and a shunt short stub.

The gate is resonated by a series transmission line and is prematched with a shunt capacitor. A Type-C network does the matching between the ports. The series capacitor was added for DC blocking purposes. The input circuit, IMN, is shown in Figure 5.29. A Type-D network was used to match the gate to  $50\Omega$ . The series capacitor was used for the DC block and a selective lossy circuit (shunt



**Figure 5.28** Schematic for the matching block ISMN1.



**Figure 5.29** Schematic for the input matching block IMN.

resistive-terminated transmission line) was employed to improve low-frequency return loss and input match.

Once all blocks are designed, they are assembled together following the topology in Figure 5.8 and modified to the format in Figure 5.30. The first simulation showed a gain ranging from 20 to 15 dB with poor input and output return losses.

Then the amplifier was submitted to optimization with the following objectives: minimum gain of 20 dB and input/output return losses of 10 dB. The circuits contained in blocks ISMN2 4 and OMN were fixed during the optimization process. The layout of the final circuit is illustrated in Figure 5.31.

The bias for the devices is introduced through the short stubs in the circuit. The short at the shunt stubs is created by a capacitor on top of the via, resonated at the center frequency. One can observe that a radial stub is used to bias the drain of the power stages. That is an alternative when the current on top of the capacitors is limited by the metallization thickness. More details about the biasing networks design are shown in the Appendix A.

The amplifier gain from 60 to 90 GHz is shown in Figure 5.32(a). It is reasonably flat at 20 dB within 70 to 80 GHz, with an input return loss better than 10 dB over the band. The output return loss is a bit lower than 10 dB at the low end of the band and near the high end, an expected result based on impedance matching for power. The circuit is stable showing a  $\mu$ -factor above 3 dB within the band.

The same amplifier is simulated over the frequency band of 1 to 100 GHz as depicted in Figure 5.32(b). There is no out-of-band peak or spurious response in the gain or in the return loss that would indicate a circuit instability. The input return loss is better than 10 dB from 1 to nearly 90 GHz. The output return loss goes to

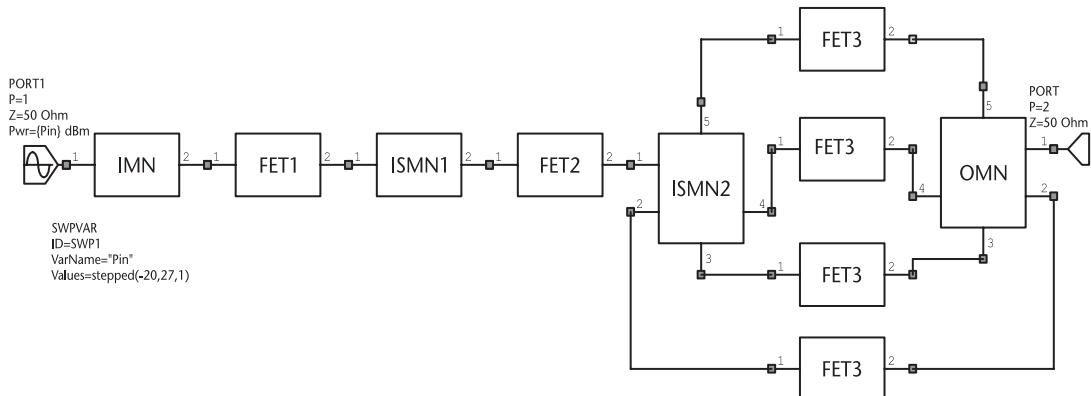
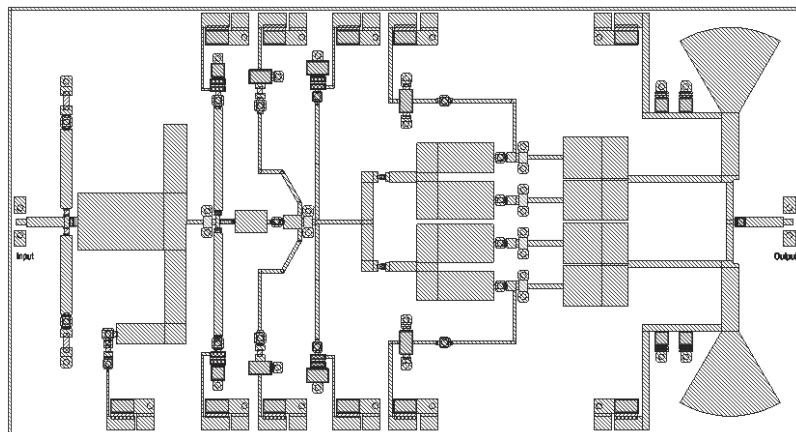
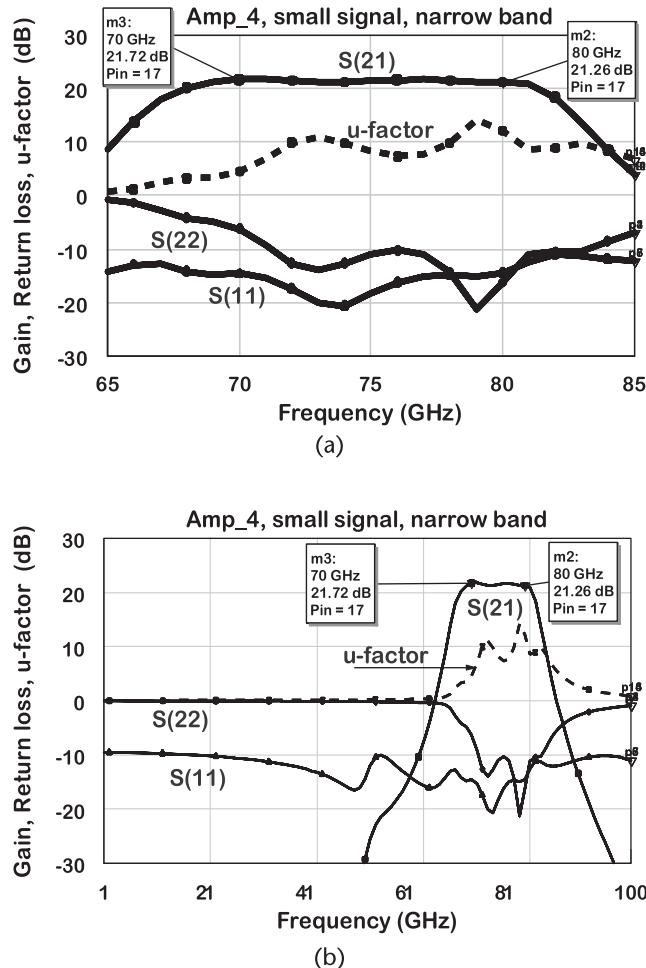


Figure 5.30 Block diagram of complete amplifier option 4.

Figure 5.31 Layout of the amplifier 4. Approximate dimensions  $2.7 \times 1.5 \text{ mm}^2$ .

0 outside the band, which probably causes the  $\mu$ -factor to go down to 0 dB outside the amplifier bandwidth. A more detailed analysis of stability will be covered at the end of the chapter. The large-signal simulations using the EEHEMT model from Chapter 2 are shown in Figure 5.33. There are some differences between the small-signal and large-signal models. Even though the differences are small, the result to trust is the one based on the linear model. The power performance versus frequency for three drive power levels between 17 and 20 dBm is shown in Figure 5.33(a). The output power is reasonably flat at 31 dBm. In Figure 5.33(b), one can see a plot of the performance versus the input drive at 75 GHz. The small-signal gain with the nonlinear model is 23 dB, about 1.5 to 1.7 dB above the gain with a linear model. The best efficiency is at an input drive of 19 dBm. The output power at this point is 31.5 dBm and the gain is equal to 15.5 dB. One can tell the gain is compressed by 6 dB at the input drive power of 17 dBm. The PAE is about 32% between 72 and 78 GHz and goes down to 27% at the band edges. These results are considered preliminary, as they are derived from the EE type of circuit model. It does include losses, but a better prediction is made from the EM type of the circuit model.



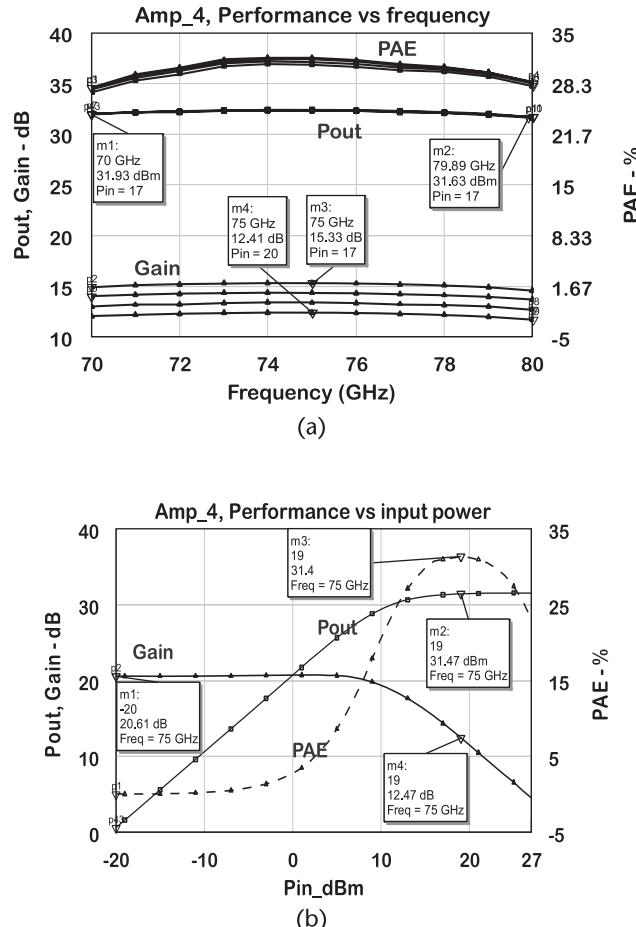
**Figure 5.32** Gain, stability, and return loss for amplifier option 4: (a) in-band amplifier small signal, and (b) broadband response.

## 5.5 Case Study: Core Amplifier

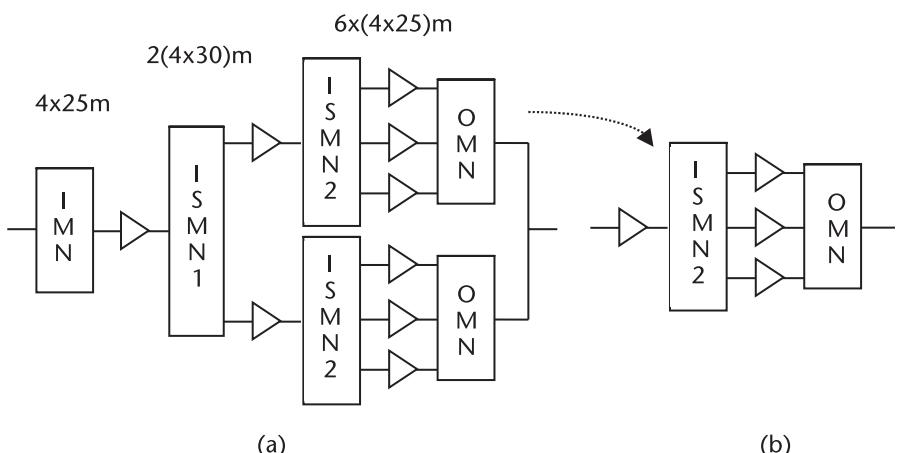
In this section, we are going to analyze the design option of a core amplifier listed as option 2.5 in Table 5.3. The objective is to investigate power combiner/transformers with 3:1 and 6:1 ratios; thus, we address only the design of the circuit blocks OMN and ISMN2. The amplifier topology for option 2.5 is shown in Figure 5.34(a) along with the transistor lineup. Assuming that the output stage delivers 1.5W, the driver will deliver 600 mW, and, thus, this option uses a 4-dB margin for the driver power. All unit cell devices measure  $4 \times 25 \mu\text{m}$ . The core amplifier is shown extracted from the complete amplifier.

### 5.5.1 OMN\_03

The design process follows the same path described in previous case study. The one-way circuit represented in Figure 5.35 uses a series line and a shunt capacitor



**Figure 5.33** Large-signal simulations option 4. Bias  $V_{DS} = 12V$ ,  $V_{GS} = -1.75V$ , and  $I_{DS} = 250$  mA: (a) power, gain, and PAE vs frequency, and (b) power, gain, and PAE vs  $P_{in}$ .



**Figure 5.34** Configuration for the amplifier after option 3: (a) complete option 3 amplifier, and (b) core amplifier OMN\_03.

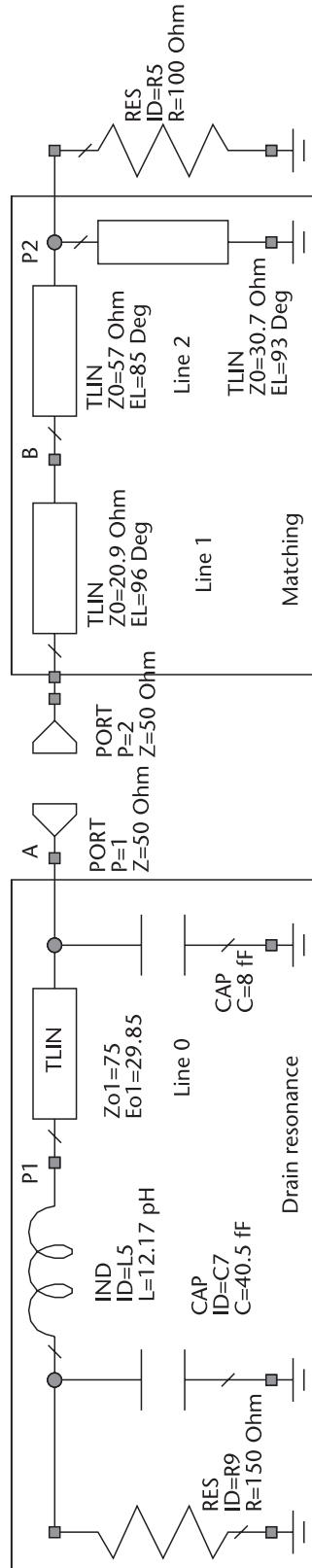
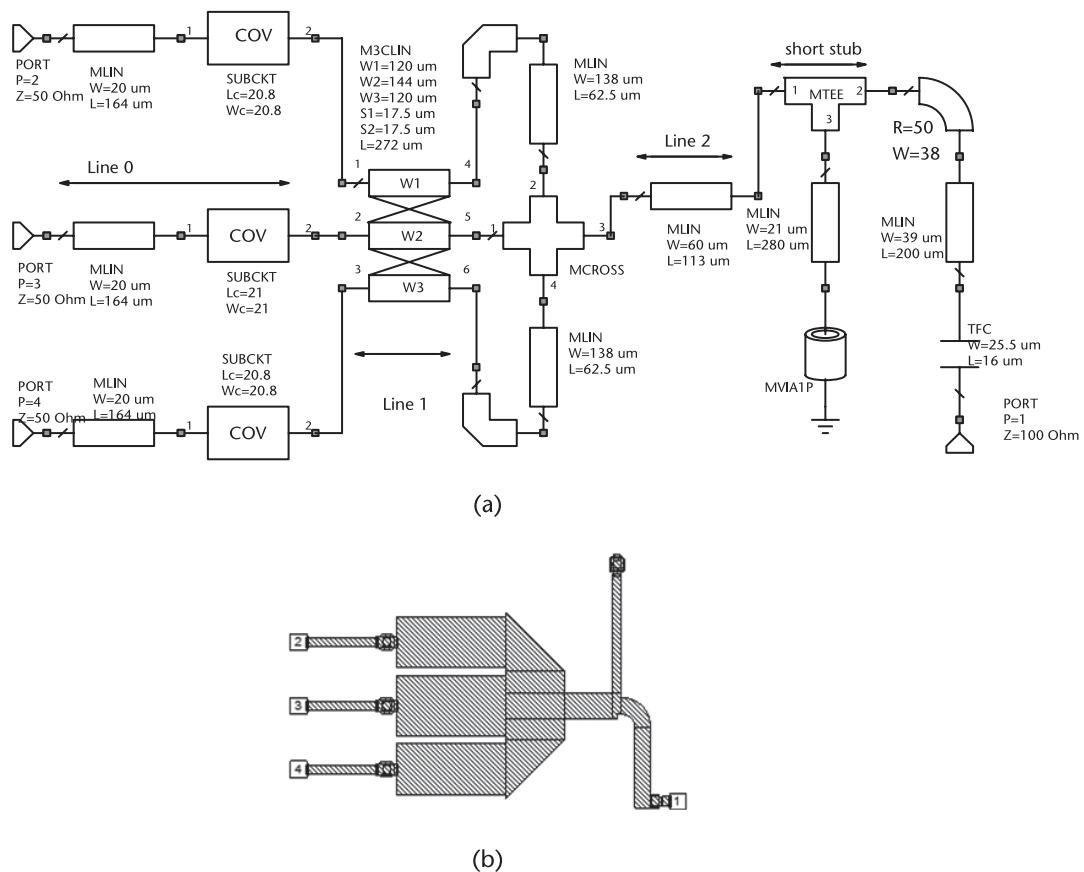


Figure 5.35 Matching of OMN\_03 with a cascade of transmission lines and a shunt stub.

over a via between port 1 and the drain. Between port 2 and the load, a Type-C matching network is used with the addition of a  $90^\circ$  shunt short line.

We already discussed the pros and cons of using the shunt capacitor in MMIC design, and the same arguments are valid in this case. At resonance, the resistance of port 1 is  $R_T = 12\Omega$  and the quality factor is  $Q_T = 2.8$ . With this information, the Type-C network was used to match  $12\Omega$  to  $100\Omega$ . The resulting transmission-line characteristic impedances are  $10\Omega$  and  $28\Omega$ , nonrealizable in this MMIC process. The line impedance was increased to  $21\Omega$  and a shunt short stub was added to the circuit. Tuning the circuit using the Smith chart, the parameter values in Figure 5.35 were found.

The transformation of the circuit in Figure 5.35 to a three-way combiner follows option (b) of the circuit in Figure 4.71, meaning that the elements between nodes  $P_1$  and  $B$  are paralleled. The conversion to a microstrip equivalent circuit can be viewed in Figure 5.36(a). Line 0 represents the line between  $P_1$  and A. Line 1 corresponds to the line between nodes A and B. The shunt capacitor attached at port  $P_1$  in Figure 5.35 is close to the coupler in Figure 5.36. Line 2 corresponds to the line between node B and  $P_2$ . The combiner core is the cross element, representing the connection between the four circuit paths. Two series lines were added after

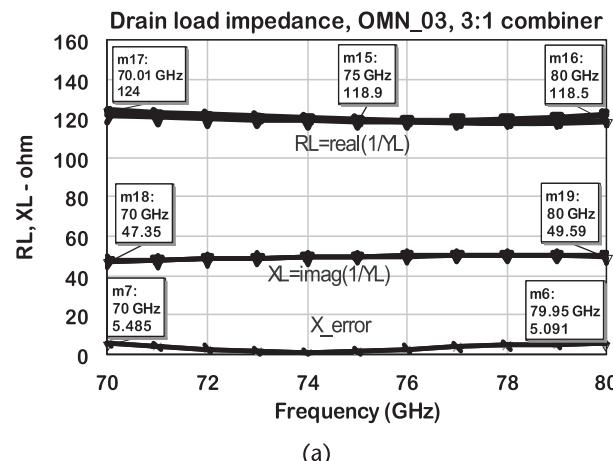


**Figure 5.36** The EE schematic and layout for OMN\_03: (a) microstrip schematic\_OMN\_03a, and (b) corresponding layout.

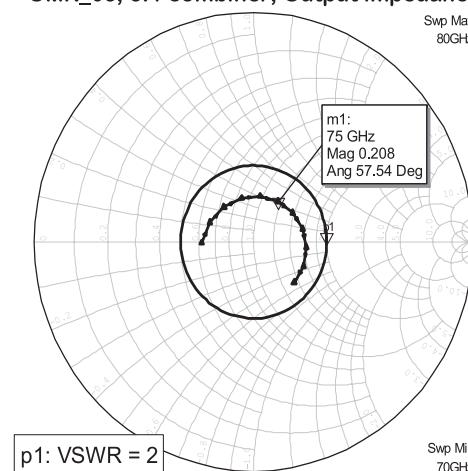
the shunt inductor: a bended line by  $90^\circ$  and an additional series line to allow a connection to the mirror image of the circuit. A series capacitor was added to the circuit for DC blocking, and the spacing between unit cells is set at  $150\ \mu\text{m}$ . The corresponding layout for the schematic is shown in Figure 5.36(b).

The optimization was set for a load impedance at the drain port equal to  $\text{real}(1/Y_L) = 120\Omega$  and  $\text{imag}(1/Y_L) = j48\Omega$  at the center frequency. The output impedance was held at a 10-dB return loss for a  $100\Omega$  termination. As discussed in Chapter 2, the external arms have the same dimensions, while the center arm was allowed to be different in the optimization process to improve the combiner performance.

The corresponding impedance for the drain side of the circuit block is shown in Figure 5.37(a). The real part of impedance at ports 2, 3, and 4 is  $120\Omega - 1/+3\Omega$ , which corresponds to a power fluctuation of less than  $+/-0.1\ \text{dB}$ . Thus, it demonstrates



OMN\_03, 3:1 combiner, Output impedance



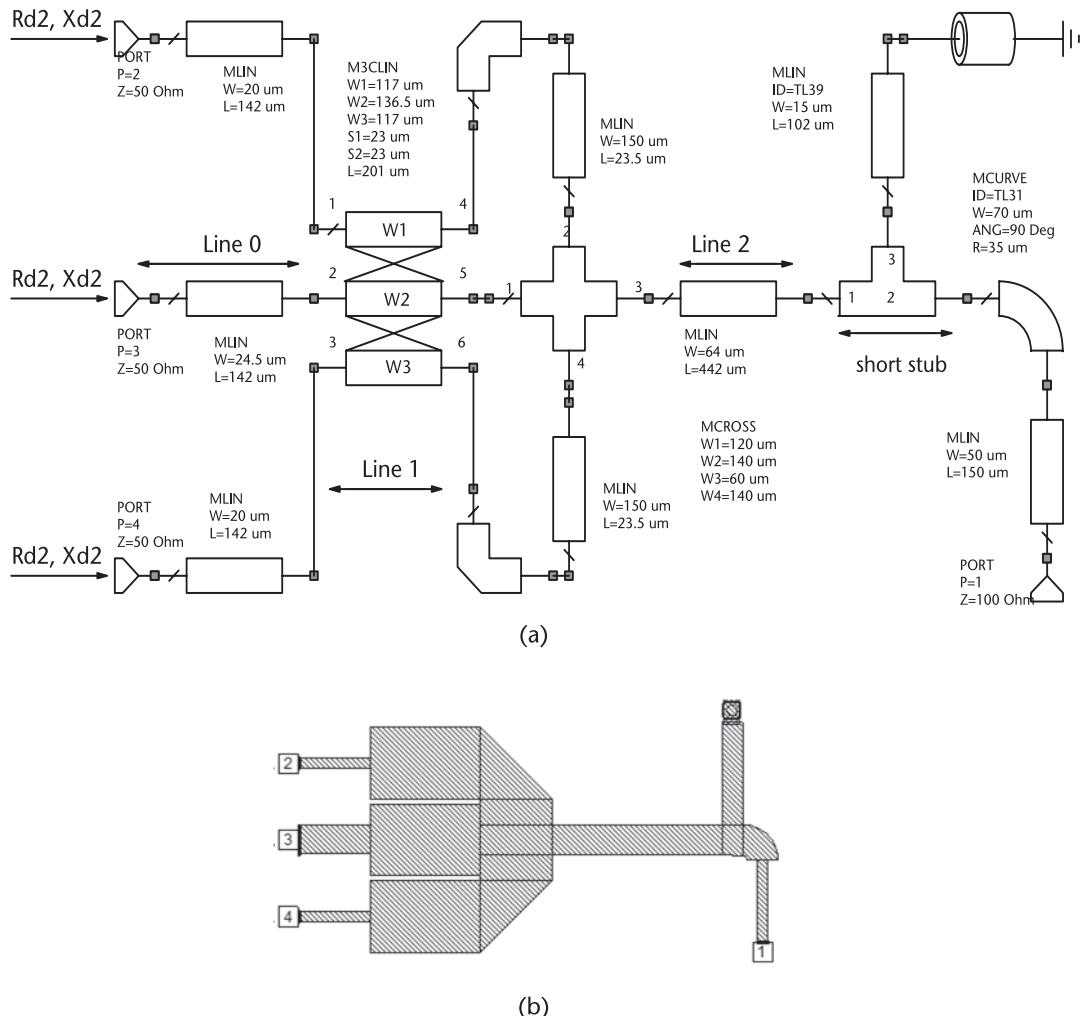
(b)

**Figure 5.37** Impedance at the OMN\_03 ports: (a) drain load impedance for the OMN\_03 block, and (b) OMN\_03 output impedance.

the feasibility of combining an odd number of ports and confirms the validity of working with the impedance asymmetries to compensate for the magnitude and phase unbalance of the 3:1 combiner.

The reactive part is nearly constant over the band. The difference between the ideal reactance and the one simulated from the circuit is shown at the bottom of Figure 5.37(a), which shows a maximum value of  $j5.4$  at the band edges. Figure 5.37(b) shows the impedance from the output port, with the drain terminated with  $250\Omega$ . The trace of the impedance is contained within the circle for  $VSWR = 2$ .

For the sake of comparison, a similar circuit without the shunt capacitor was investigated. The design started with the basic circuit contained in Figure 5.9, with the capacitor removed. The circuit schematic is shown in Figure 5.38(a) and the corresponding layout is shown in Figure 5.38(b). The circuit impedances looking into ports 2 and 3 are in the plots shown in Figure 5.39. The real part of impedance

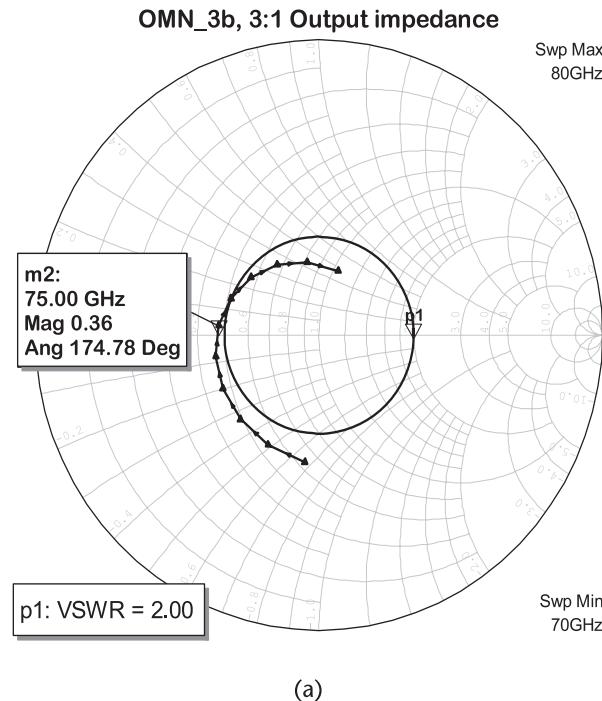


**Figure 5.38** The EE schematic and layout for the circuit OMN\_03b: (a) OMN\_03EE circuit schematic, and (b) corresponding layout.

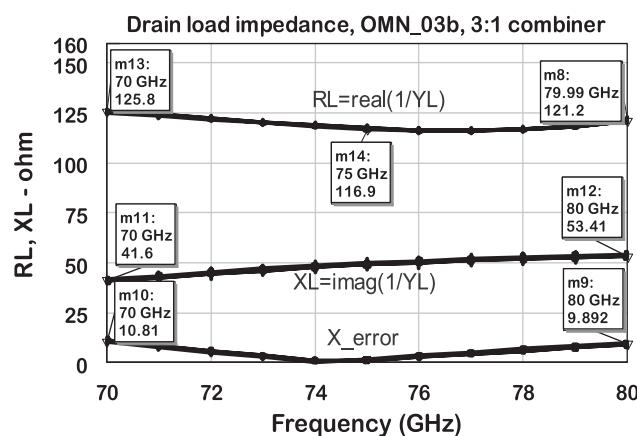
is at the top and ranges from  $118.5\Omega$  to  $122.7\Omega$ . The reactance is in the middle, showing a range from  $40.7\Omega$  to  $54.1\Omega$ .

The plot at the bottom shows the comparison of the reactance from the circuit with the ideal value. It shows a value as high as  $j10.8\Omega$ . Comparing this value with the error shown in Figure 5.39(a),  $j4.8\Omega$ , it is obvious that the circuit with a shunt capacitor performs better. Figure 5.39(b) illustrates the output impedance in the Smith chart, which is outside the circle for  $\text{VSWR} = 2$  for a  $100\Omega$  reference.

A more complex microstrip circuit can improve the impedance, probably with higher losses as a penalty. However, if the circuit bandwidth is between 72 and



(a)



(b)

**Figure 5.39** Impedances for the circuit option OMN\_03b: (a) load impedance for the microstrip version, and (b) output impedance on the Smith chart.

78 GHz, the difference in the performance of both circuits is small. Let us now combine the circuit in Figure 5.38 with its mirror image to achieve a 6:1 combiner/transformer, as illustrated in Figure 5.40. The three coupled-line model was changed to a six coupled-line model.

The asymmetries are introduced such that the pair of outer arms is assumed to be equal, as are the internal arms. The overall circuit was reoptimized and the element parameters are contained in the figure. Notice that in this case nodes  $D_1$  and  $D_2$  are connected for better amplitude and phase balance. However, this is not always true; in other combinations of circuit parameters, it is found that the nodes should be separated.

The drain impedance results are shown in Figure 5.41(a). The top traces indicate that the resistive part varies from  $123\Omega$  to  $126\Omega$ . The middle trace represents the reactive part that is nearly constant and equal to  $j50\Omega$ . The bottom trace shows the drain reactance difference between the OMN\_3 and the ideal circuit. The maximum value at the band extremes is in the order of  $j5.1\Omega$ . Figure 5.41(b) show that the output VSWR is less than 2.0 over the band. The amplitude and phase balance of the 6:1 combiner are shown in Figure 5.42. Figure 5.42(a) represents the amplitude balance, showing an insertion loss maximum of 8.7 dB and a minimum of 8.2 dB. Adding the losses from an ideal 6:1 combiner gives a coupling of 7.8 dB; adding the ohmic losses of 0.5 dB results in a total expected loss of 8.3 dB.

The simulation shows a value between 8.2 and 8.7 dB within the band. Therefore, the circuit block OMN\_3a shows about 0.5-dB excess losses, and the balance is between 0.4 and 0.5 dB. The insertion phase is shown in Figure 5.42(b), showing an average difference of  $3.4^\circ$  over the band.

### 5.5.2 ISMN2\_03

The objective is to verify the design of a transformer/divider employed by a core amplifier for power applications. The driver amplifier uses a single  $4 \times 30 \mu\text{m}$  cell. The power stage is composed by three  $4 \times 25\text{-}\mu\text{m}$  unit cells in parallel. It is assumed that the drain and gate impedances are resonated, as represented in Figure 5.43. The matching circuits are then inserted to match the impedances from port 1 to port 2.

A few matching options will be addressed as follows. The first proposed alternative to match both resonated impedances is to use a lumped LC network. For instance, a double L-type highpass/lowpass network is ideal and capable of matching over a wide frequency band. The lumped prototype can then be converted to a distributed version. A second alternative is to match directly with distributed elements. A quarter-wave transformer is the most popular element for this function, and it can also be used to compensate for variations in the reactance over frequency. A third alternative is similar to the second, adding a shunt capacitor in the matching.

#### Option (a): Lumped Elements

In this example, the drain impedance from Figure 5.43 gave a resonated resistance of  $RT_d = 11.5\Omega$ . The gate was initially series-resonated with a short series transmission line, giving a  $RT_g = 2\Omega$ . Thus, a shunt capacitor was employed to increase the gate resistance and introduced an inversion in the circuit impedance. The new gate

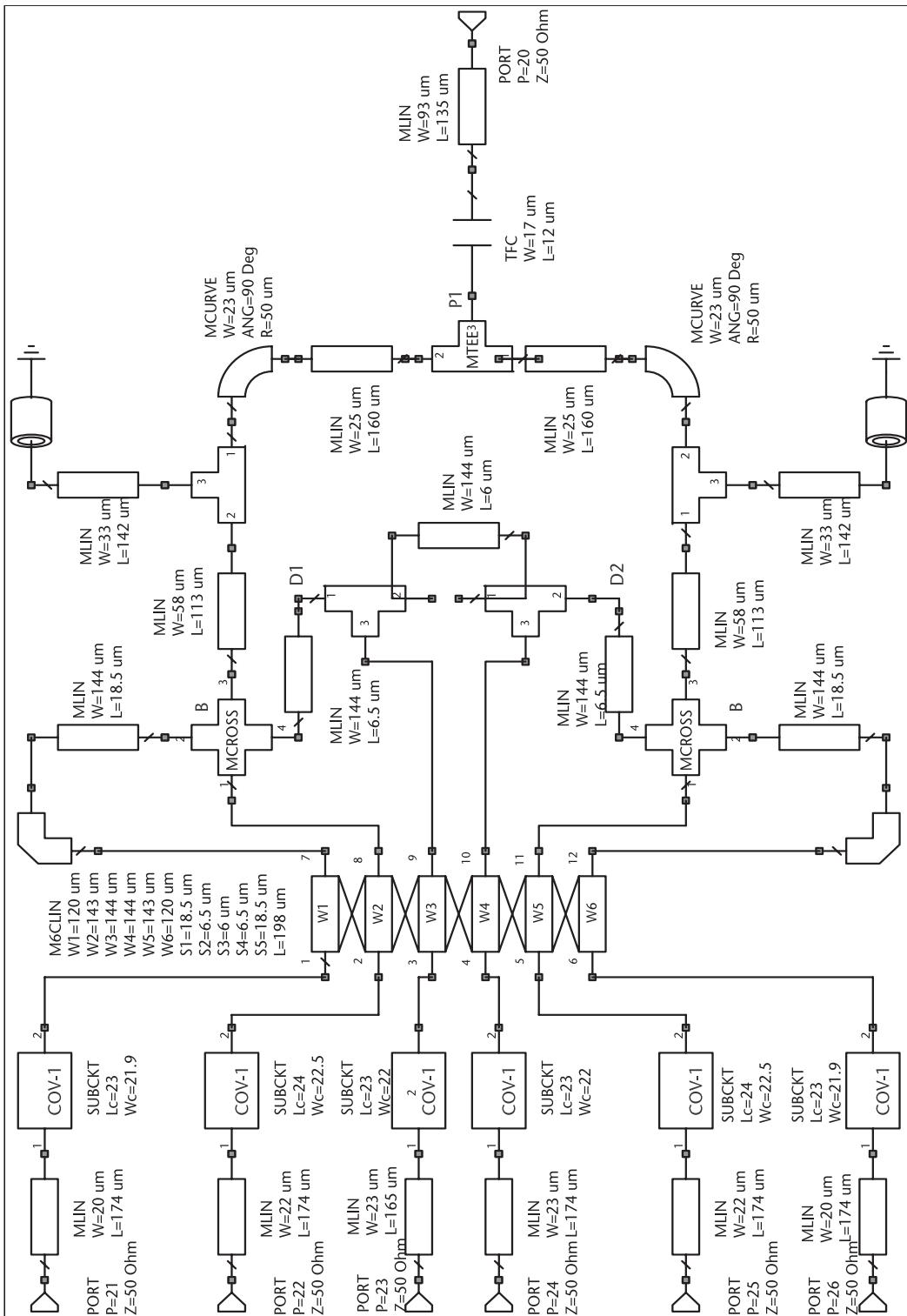
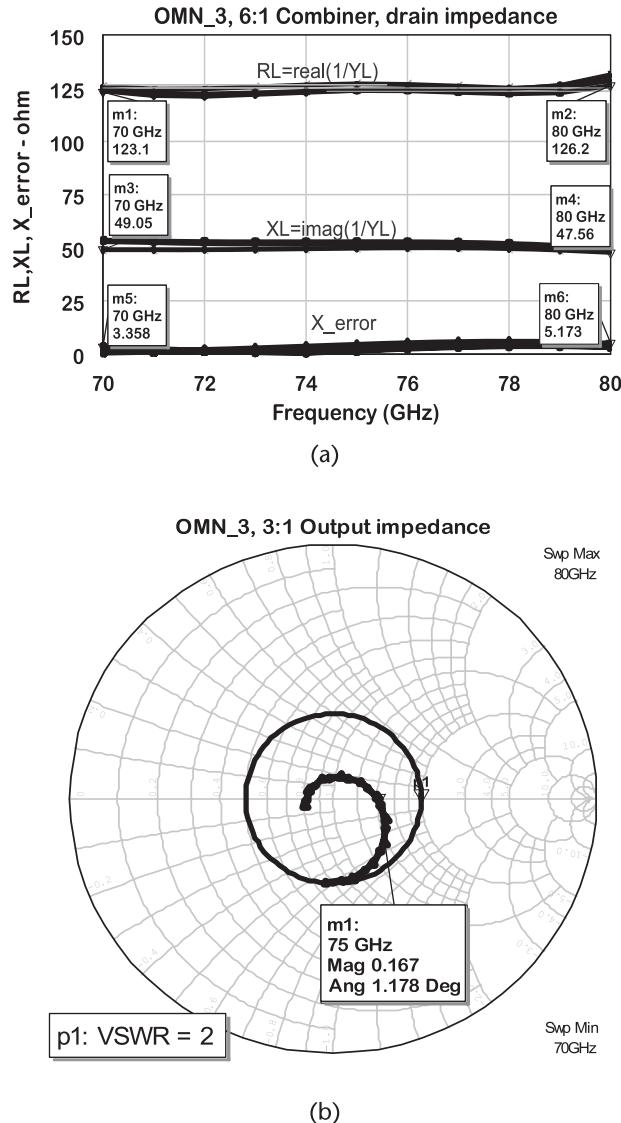
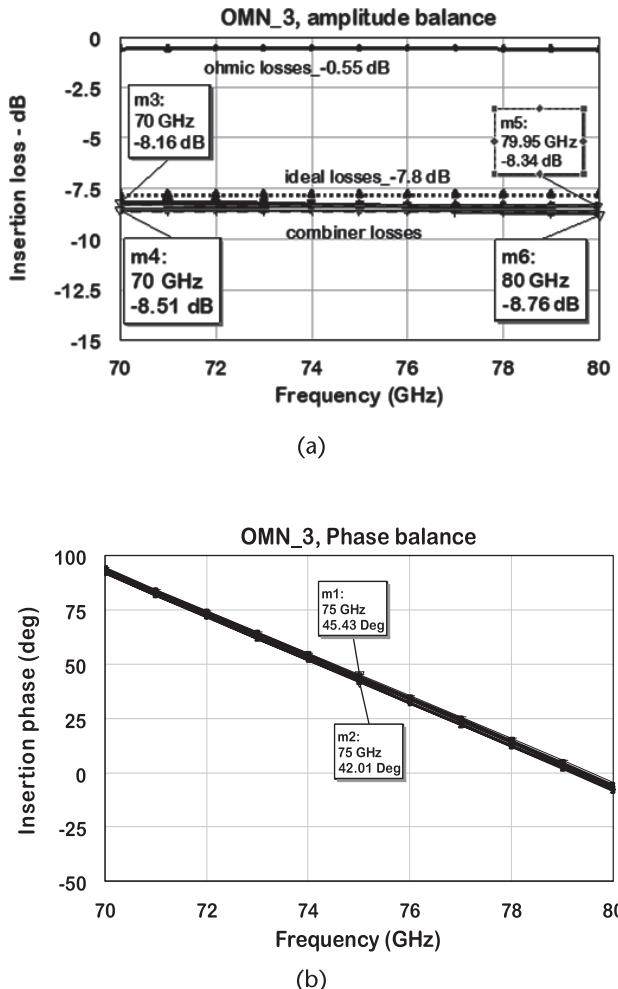


Figure 5.40 Schematic of a microstrip version for the OMN\_3 circuit block.



**Figure 5.41** Impedance at the OMN\_3 ports: (a) drain load impedance of the OMN\_3, and (b) output impedance for the OMN\_3.

resistance was  $RT_g' = 118\Omega$ . Let us verify the case of matching the impedances of ports 1 and 2 with a double-L matching highpass/lowpass prototype network. The lumped element network was calculated for the central frequency of operation and then optimized to provide the required impedances at the drain and gate terminals. The resulting lumped circuit is shown in Figure 5.44. Before converting this circuit to microstrip equivalent, some adjustments were required. In Figure 5.45, we added a capacitor from node B to the ground of same value as the capacitance from node C to the ground. That made a PI cell that is equivalent to a series transmission line, after (4.71) to (4.74). The added capacitor needed to be resonated with an additional shunt inductor.



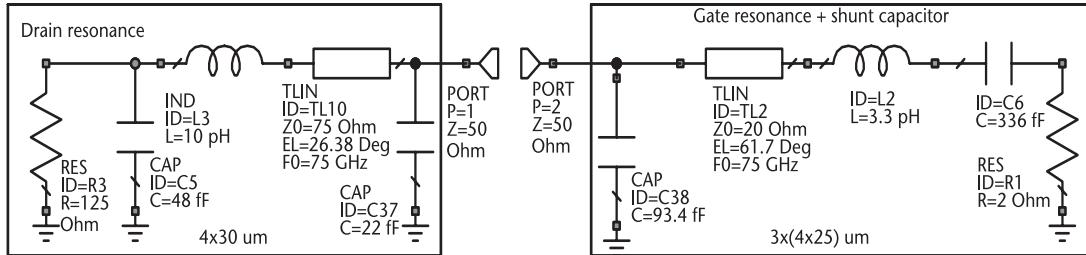
**Figure 5.42** Balancing between the OMN\_3a ports: (a) magnitude of insertion loss, and (b) magnitude of insertion phase.

After we merged the resonant inductor with the one already present in the circuit, it was replaced by a shunt short stub. The shunt stub parameters are straightforward to calculate, using the equation  $jX = jZ_0 \tan(\theta)$ .  $Z_0$  is the impedance of the stub line and  $\theta$  is its electrical angle.

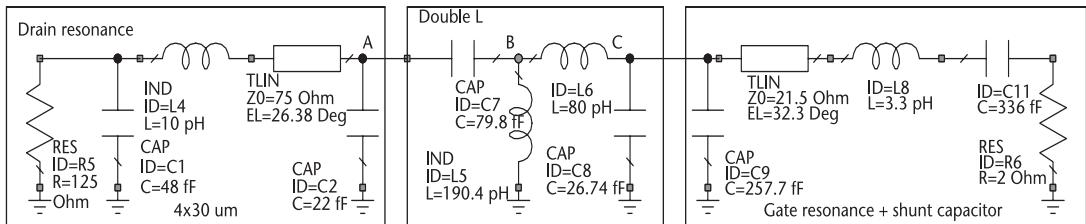
The series matching capacitor can be maintained and can be used as a DC block. The one-way ideal circuit is shown in Figure 5.46. Looking at port  $P_1$  impedance towards the gate, assume that the gate at  $P_2$  was terminated in the series RLC gate circuit. When looking at port  $P_2$  towards the drain, the internal resistance of  $125\Omega$  was replaced by  $250\Omega$  to simulate the small-signal conditions.

The next step is to transform the circuit into a 1:3 power divider. Therefore, the circuit to the right of node B, excluding the shunt stub, was replaced by three paralleled similar circuits. These elements then had their parameters modified to take into account the higher impedance of node B, looking towards the gate. The ideal circuit was then replaced by microstrip lines, as shown in Figure 5.47.

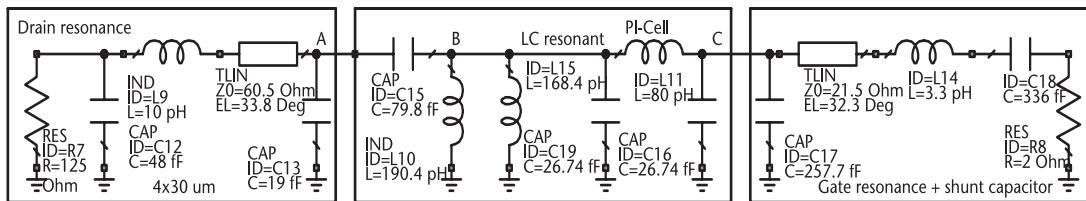
An interesting property of this approach is that different topologies can result from the same lumped prototypes, depending on how the T and PI cells are associated.



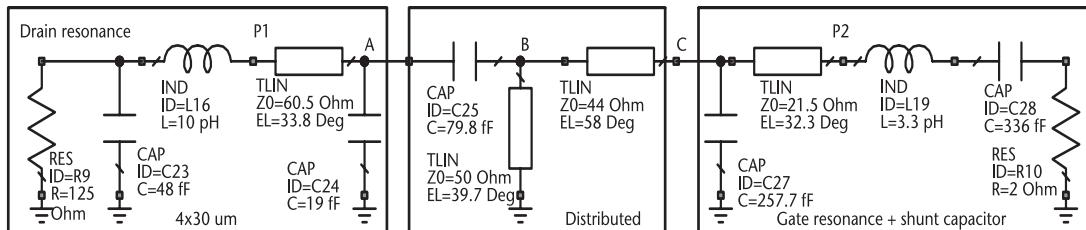
**Figure 5.43** ISMN2\_03, resonated drain and gate schematics.



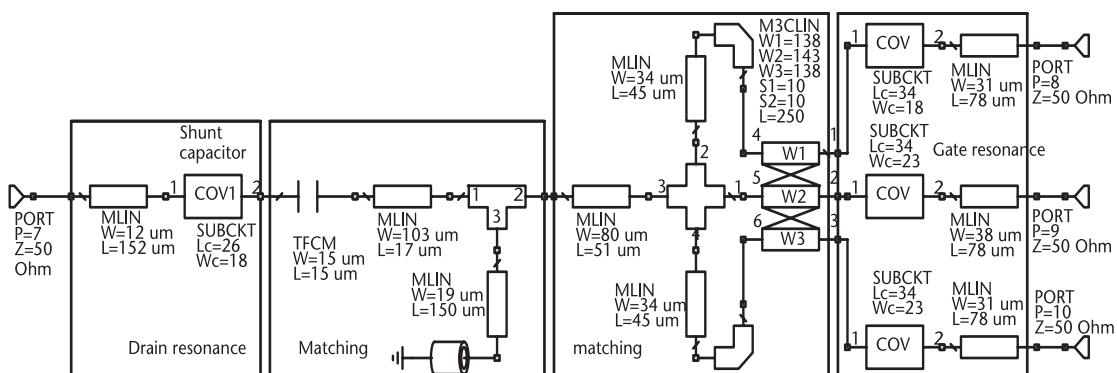
**Figure 5.44** Matching with lumped elements.



**Figure 5.45** Circuit prepared for conversion to distributed elements.



**Figure 5.46** Matching with distributed elements converted from lumped elements.



**Figure 5.47** ISMN2\_03a MS circuit generated from lumped elements.

### Option (b): Distributed Elements

The schematic for the initial design with ideal transmission lines is shown in Figure 5.48. The gate and drain impedance were resonated by a series transmission line. The resonated resistances were  $RT_{\text{gate}} = 5.6\Omega$  and  $RT_{\text{drain}} = 11.5\Omega$ . A Type-C network resulted in lines with low characteristic impedance. Thus, in order to find the  $R_{\text{ref}}$  that gives realizable lines, let us employ (5.10) and (5.11). They are derived by adding a quarter-wave transformer to each port to a common  $R_{\text{ref}}$  to be defined. The equation takes into account the fact the gate impedance is multiplied by 3, corresponding to the number of parallel devices in the power stage.

$$Z_{01} = Z_{02} \sqrt{\frac{RT_{\text{drain}}}{3RT_{\text{gate}}}} \quad (5.10)$$

$$R_{\text{ref}} = \frac{Z_{01}^2}{RT_{\text{drain}}} \quad (5.11)$$

In (5.10),  $Z_{01}$  is the impedance of the transmission line on the drain side, and  $Z_{02}$  is the impedance of the transmission line on the gate side. Selecting  $Z_{02} = 25\Omega$  for feasibility with multiple unit cells in parallel, we obtain  $Z_{01} = 21.7\Omega$ . The reference impedance is then  $R_{\text{ref}} = 37.7\Omega$ , greater than the ideal value,  $R_{\text{ref}} = 27\Omega$  calculated from the geometrical mean between  $R_d$  and  $R_g$ . The impedances of ports 1 and 2 are both for the RLC series resonant type of circuit; thus, an inverter is necessary to transform one side into RLC parallel, which means that the circuit will have three quarter-wave transformers in cascade. To minimize the circuit dimensions, the middle transformer was replaced by an inverter capacitor of 70 fF. The microstrip circuit is illustrated in Figure 5.49.

### Option (c): Distributed and Shunt Capacitor

The topology of this approach starts with the same basic resonated drain and gate elements from Figure 5.43. The shunt capacitors use capacitor over via, and a cascade of quarter-wave transformers performs the matching. Following a similar design procedure, the initial circuit is transformed into a 1:3 divider/transformer circuit. After converting the ideal transmission-line circuit into a microstrip circuit, we obtain the schematic in Figure 5.50. The series capacitor in the circuit has the purpose of DC blocking.

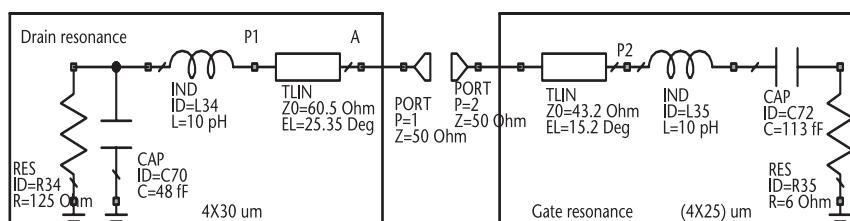


Figure 5.48 Resonance with transmission lines.

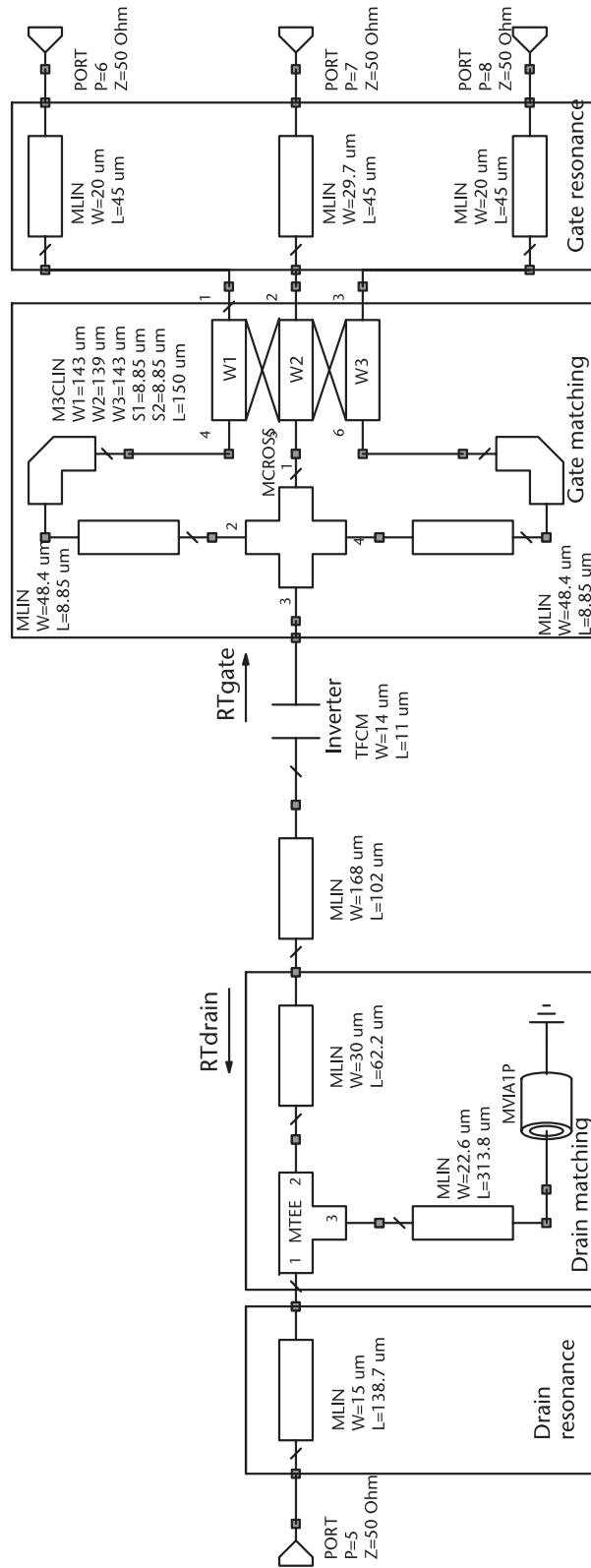


Figure 5.49 Representation of the ISMN2\_03b.

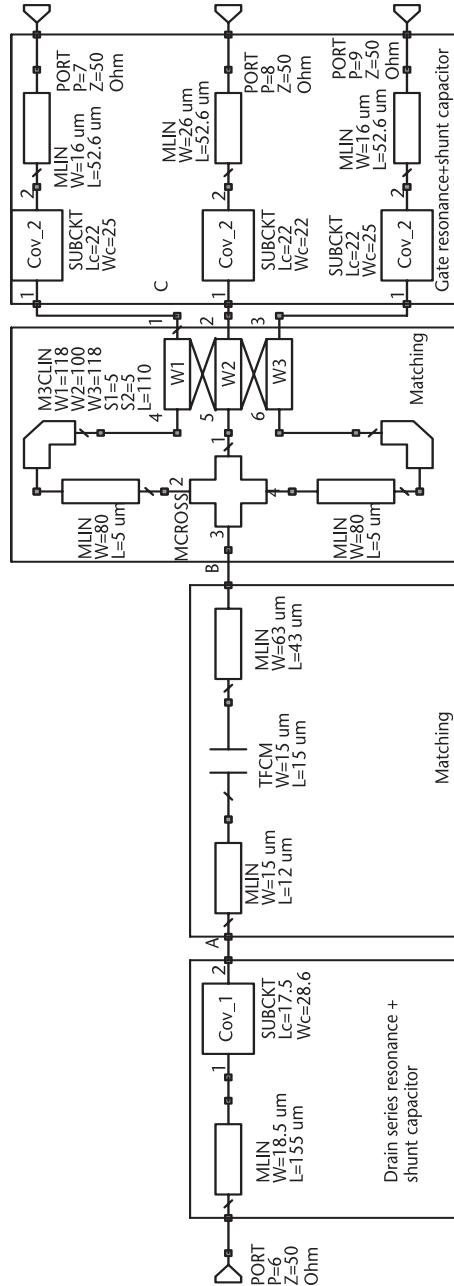


Figure 5.50 MS circuit for option ISMN2\_03c.

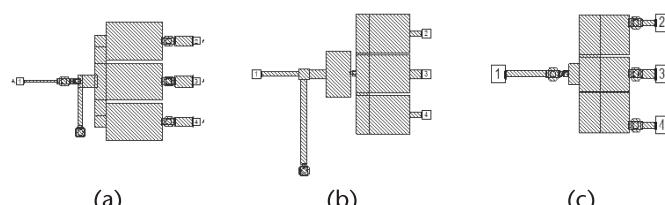
The corresponding layout for options (a), (b), and (c) are shown in Figure 5.51. The short shunt stubs are used for matching and bias. Additional bias elements must be added so that each ISMN2 can bias the drain and gate. The additional elements are high-impedance quarter-wavelength-long lines.

The main difference between the options is the absence of shunt capacitors in option (b). The second difference is the need for shunt inductors for matching in options (a) and (b), while there is no need of one in option (c). The common feature of all three is the series drain and gate resonator lines. The other differences are specific to the design.

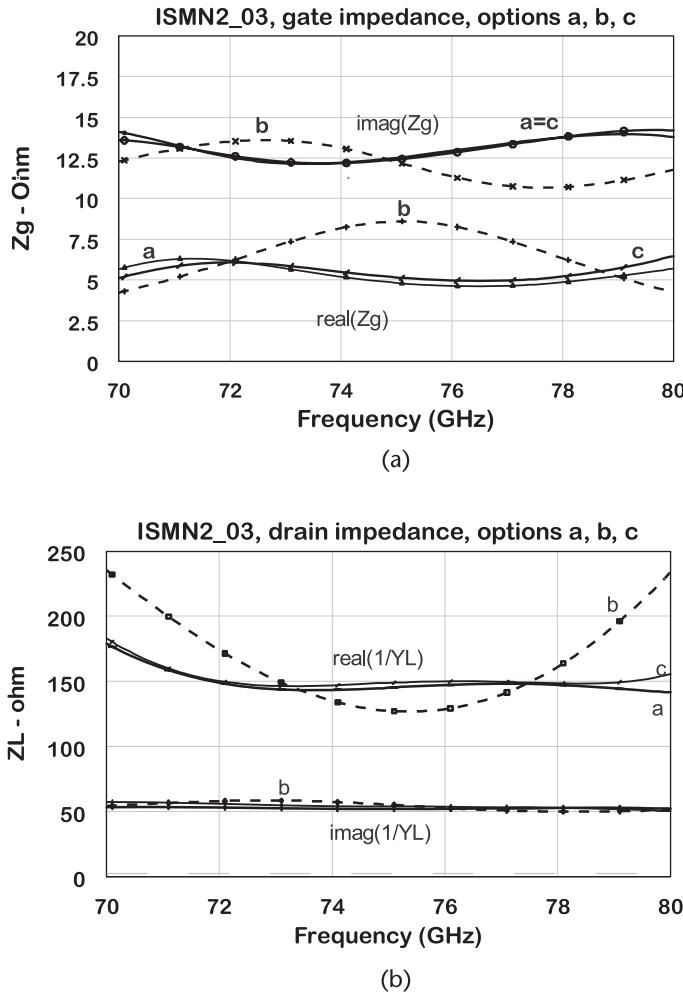
Let us compare the impedance performance of the options (a), (b), and (c) for the ISMN2\_03 circuit block. Figure 5.52(a) shows the gate source impedance, where the dotted lines represent option (b) and the solid lines represent options (a) and (c). The top curves represent the imaginary part, showing that options (a) and (c) are equivalent. The bottom set of curves shows the real part of gate impedance, where options (a) and (c) are again close to each other and flatter than option (b) over the band. These variations may affect the gain of the power stage, but they can be compensated by matching networks from previous stages. Figure 5.52(b) shows the drain load impedance. The top curves represent the real part of the load, where option (b) stands as the one with more variation over frequency. That results in 2.3 dB of power variation over the band, while options (b) and (c) cause 1.3 dB. If one adds 1.7 dB of power due to the power mismatch from  $100\Omega$  to  $150\Omega$ , the driver needs a power margin of 4.0 dB. The reactive part at the bottom is relatively insensitive in all the three versions. Options (a) and (c) are designed with shunt capacitors in the matching circuit, while option (b) uses no shunt capacitor. Most of the circuits found in the literature are actually built like option (b), which can operate within 72 to 78 GHz. This preliminary analysis for the interstage circuit is useful in the decision to which circuit should be used in the design. It also leads us to conclude that using a shunt capacitor in the matching circuit results in a better performance.

Shunt inductors could also be used, but there are a couple of drawbacks. First, its  $Q$  is inferior compared to the MIM capacitor  $Q$ . Second, it takes more space in the circuit layout. Another option to consider is to move  $R_{ref}$  right at the drain port of the driver amplifier. That would mean that all three matching arms would be joined at the drain. This makes the circuit more complex and is not so common.

The 1:3 power divider/transformer can be transformed to a 2:6 divider transformer by paralleling the two halves. In principle, after paralleling the two halves, minor modifications and only a few iterations are needed in the simulation test bench to optimize the circuit. The option ISMN2\_03a was submitted to this process,



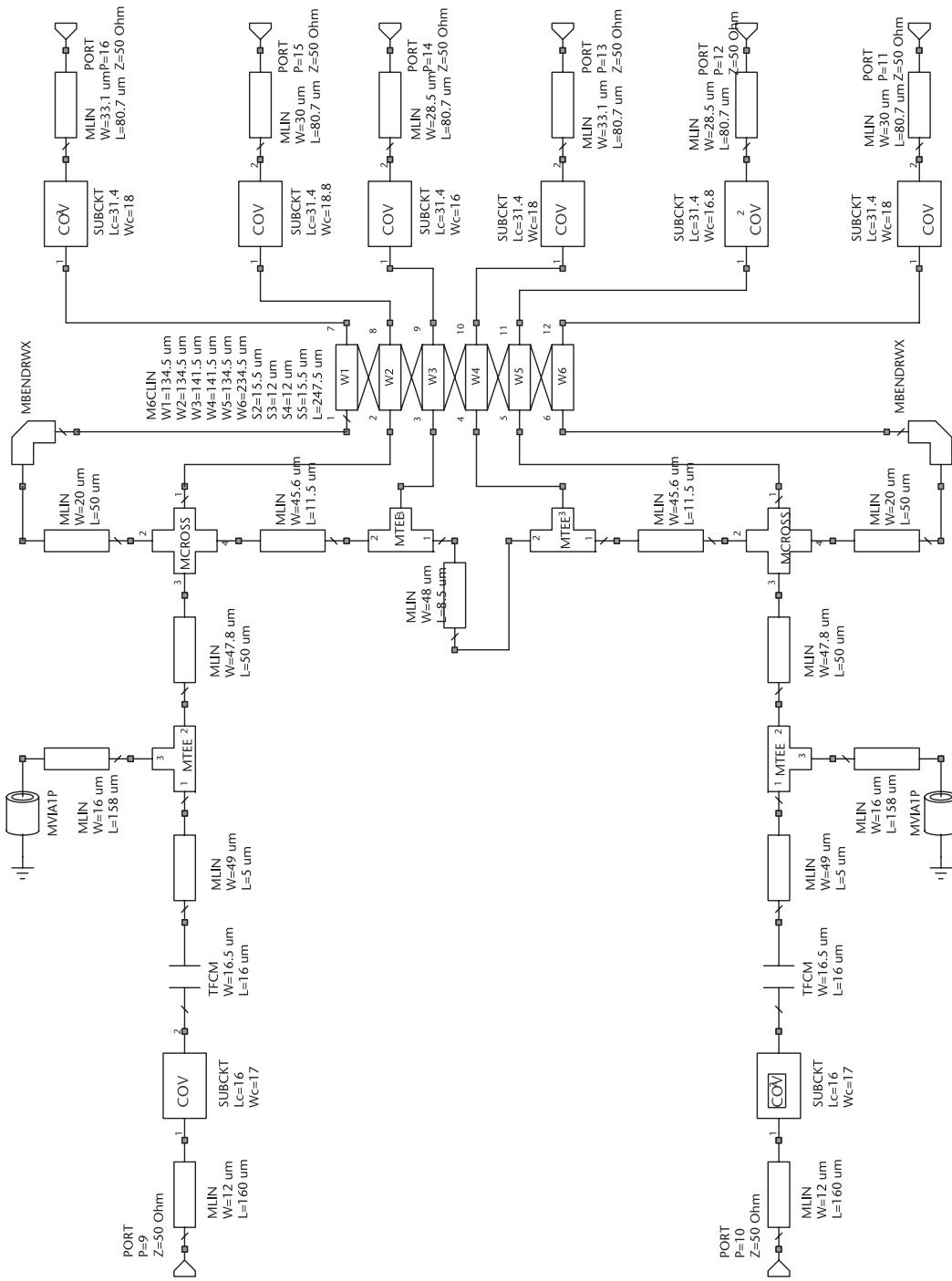
**Figure 5.51** Layout for the ISMN2 matching options: (a) ISMN2a, (b) ISMN2b, and (c) ISMN2c.



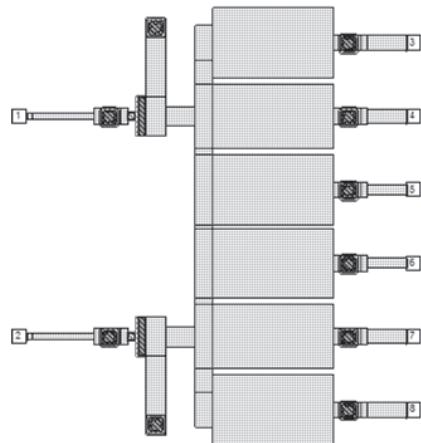
**Figure 5.52** Impedance results for ISMN: options (a), (b), and (c): (a) source gate impedance over frequency, and (b) drain load impedance over frequency.

resulting in the schematic shown in Figure 5.53 and in the layout shown in Figure 5.54.

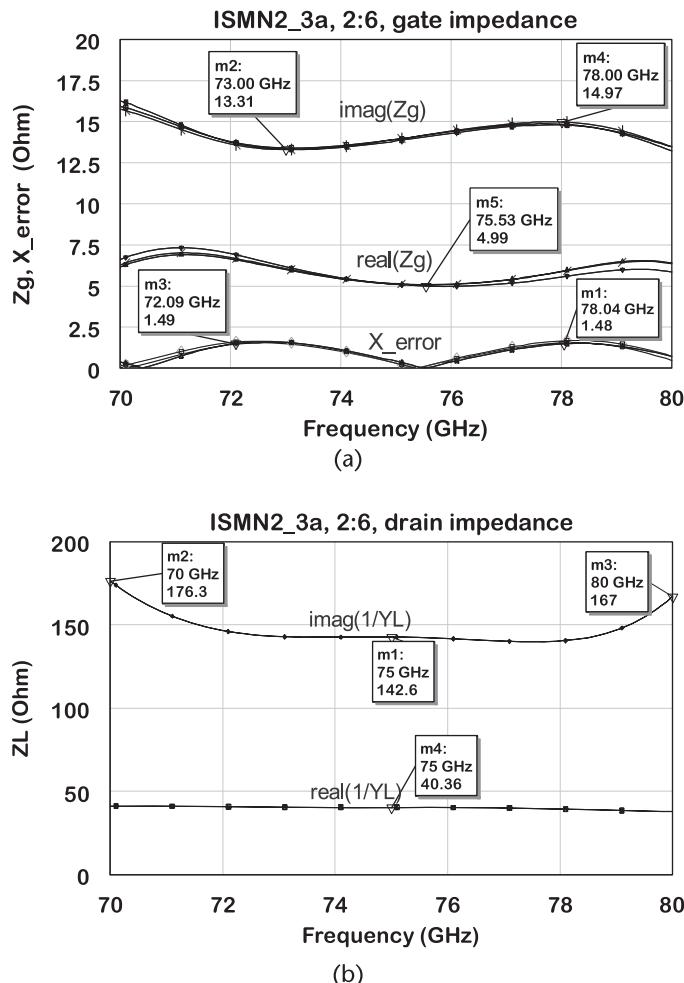
The impedance results in Figure 5.55 for the 2:6 divider are comparable to the impedance in Figure 5.53 for the 1:3 divider option (a) or (c). The real part of gate impedance in Figure 5.55(a) is between  $5.5\Omega$  and  $7.5\Omega$  while the reactive part ranges from  $j13\Omega$  to  $j15\Omega$ . The error compared to the ideal is  $1.5\Omega$  for the real and reactive parts. The drain impedance in Figure 5.55(b) shows a flat, real impedance value of  $142\Omega$  between 72 and 78 GHz. At the low end, it goes up to  $176\Omega$  and  $167\Omega$  at the high end. That means a power reduction at the driver drain of 1.5 dB within the flat section and it goes up to 2.4 dB at the low end. The 4-dB power margin for the amplifier can provide the required power before entering into compression.



**Figure 5.53** Generation of a 2:6 circuit by paralleling two 1:3 circuits.



**Figure 5.54** Layout for the 2:6 power divider/transformer.



**Figure 5.55** Impedance results for the ISMN2\_3a: (a) source gate impedance, and (b) drain load impedance.

## 5.6 Case Study: Linear Amplifier

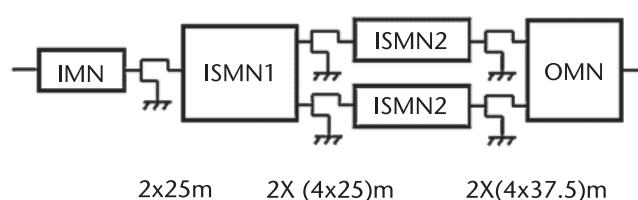
The objective is to analyze the design of a low distortion amplifier operating at 30 GHz with a bandwidth of 10% with a small-signal gain of 30 dB. The amplifier is expected to deliver a  $P_{1\text{dB}}$  of +27 dBm and a corresponding  $IP_3$  of +37 dBm. The  $IM_3$  power level is expected to be lower than  $-10$  dBm at a power of single carrier (PSC) of 24 dBm. These numbers are consistent with a PAPR of 3 dB for the case of a two-tone signal.

We selected a lineup similar to option 1.6, with an output power 3 dB lower to meet the power requirement. The resulting topology is depicted in Figure 5.56. Hence,  $2 \times (4 \times 37.5)$   $\mu\text{m}$  are needed for the output stage and  $2 \times (4 \times 25)$   $\mu\text{m}$  are needed for the driver stage. Thus, the ratio of 1:1.5 is employed by the core amplifier. Notice that the power splitting is not within ISMN2 so that losses can be minimized in this circuit block.

Also, fewer matching elements are needed, minimizing the network phase shift contributing to minimize AM-to-PM. This topology is also an approach to be followed when building amplifiers at higher frequencies when the device gain is low.

The design starts with the selection of a device from a technology offering best linearity between drain current and gate voltage. The next step is to determine the source and load impedance for linearity and efficiency. The preferred approach is to perform load-pull analysis. The alternative approach is to perform a numerical load-pull using a nonlinear model from the selected device. If neither of those two is available, the third alternative is to start from a load for power and increase the internal resistor by 50% and consider all other elements constant.

We followed the second alternative, using the EEHEMET model for the device, scaled to the  $4 \times 37.5$ - $\mu\text{m}$  size. The load-pull template illustrated in Figure 2.62 was merged with the circuit template for  $IM_3$ ,  $IM_5$  evaluation provided by Cadence AWR. The search was made for a single frequency at 30 GHz and the power level where the intermodulation levels should be reduced was at a 6-dB backoff from  $P_{1\text{dB}}$ . The results selected to represent the source and load optimum terminations are described in Table 5.4. It is interesting to note that, for the device biased in class A, the load resistor in the model for best  $IM_3$  rejection is 50% larger than the value for power. Moving the bias for class AB, this difference dropped to 16% higher than the value for class A power. The reactive elements are nearly constant. We shall refer to IMD to consider the third-order and fifth-order distortion components; otherwise,  $IM_3$  and  $IM_5$  define the distortion level for that particular order.



**Figure 5.56** Linear amplifier lineup.

**Table 5.4** Numerical Load-Pull for the Best  $IM_3$  Rejection

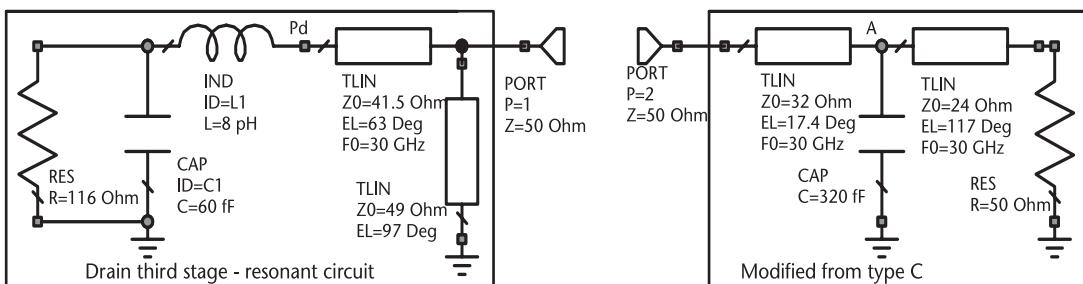
Parameter	$V_{GS} = -1V$	$V_{GS} = -1.75V$
$R_d (\Omega)$	156	116
$C_d (fF)$	60	60
$L_d (pH)$	8	8
$R_g (\Omega)$	12	12
$C_g (fF)$	170	173
$L_g (pH)$	6.5	6.5

The gate impedance in Table 5.4 includes a resistor in series with the gate to stabilize the circuit and a source inductance in series with the source to stabilize the device at 30 GHz. They may be modified or eliminated later in the design if stability is not compromised. For this particular device, a  $10\Omega$  resistor and 10-pH inductance were initially included in the circuit.

### 5.6.1 OMN Linear Amp

The initial drain circuit is depicted in Figure 5.57, employing the values from Table 5.4. The drain is resonated with a series and a shorted shunt transmission line, resulting in a resistance of  $R_T = 12.5\Omega$ . The matching to  $50\Omega$  employs a cascade of quarter-wave transformers. In order to reduce the circuit dimensions, a shunt capacitor was added to the cascade, reducing the electrical angle of the complete OMN from  $180^\circ$  to  $134^\circ$ . Port 1 is a parallel RLC with  $R_{T1} = 13\Omega$  and port 2 is a series RLC with  $R_{T2} = 12.5\Omega$ . The ideal transmission lines were converted to microstrip lines and the circuit from node  $P_d$  to node A was paralleled, transforming the one-way circuit to a two-way combiner as depicted in Figure 5.58. The parameters for the microstrip circuit are in Table 5.6, in the column IMD, Section 5.7, page 249.

Without optimization, the circuit provides the desired impedance at the drain port of  $R_L = 116\Omega$  and  $X_L = -j77\Omega$  reasonably flat within the 26 to 34-GHz band.



**Figure 5.57** Schematic of the drain circuit with ideal components.

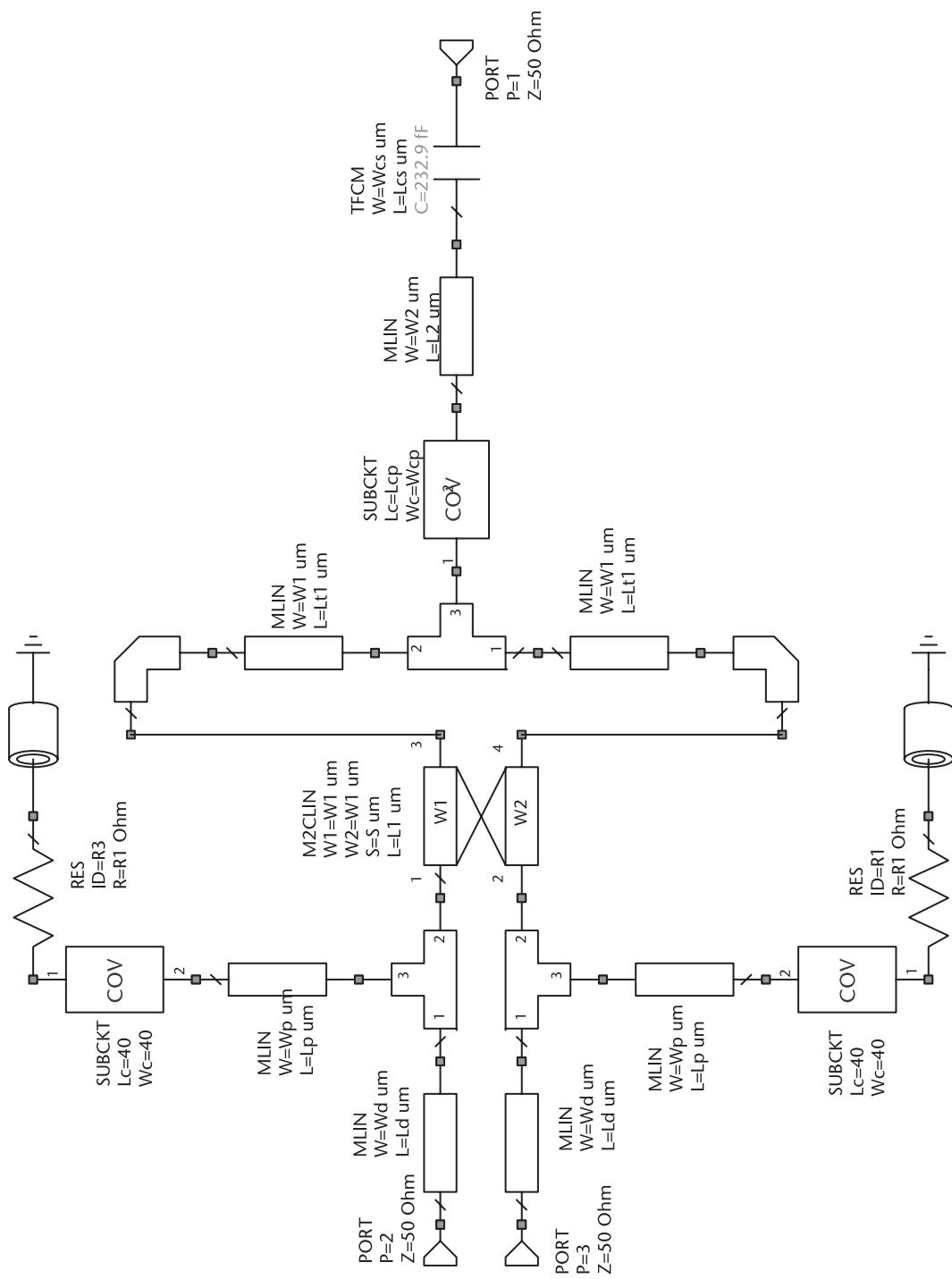


Figure 5.58 OMN for the linear amplifier.

A series capacitor was added at the output for DC blocking purposes. The drain bias is inserted through the shunt short stub.

### 5.6.2 ISMN2 Linear Amp

The initial matching for the gate of the power stage to the drain of the driver stage uses the same impedances from Table 5.4. The values for the driver device were scaled for the  $4 \times 25\text{-}\mu\text{m}$  device. The microstrip version of the circuit is shown in Figure 5.59 and the parameter values are shown in Table 5.6, page 249. The gate and drain impedances were resonated with a single series line. Two shunt short stubs were employed to serve as bias injection and are also part of the matching. A series capacitor was added to isolate DC and became part of the matching as well. Only one quarter-wave transformer was used to match  $RT_g$  to  $RT_d$  to minimize losses. The drain load impedance simulation assumes a conjugate match at the gate port. The gate source impedance simulation assumes that the internal drain resistor is  $250\Omega$  to represent the small-signal condition. That causes difficulty to obtain matching on both the drain and gate side. The resulting ISMN2 impedances are somewhat close to the predicted values. The resistive drain impedance showed  $145\Omega$  from 28 to 32 GHz. The drain reactive impedance is more or less constant and equal to  $j90\Omega$ .

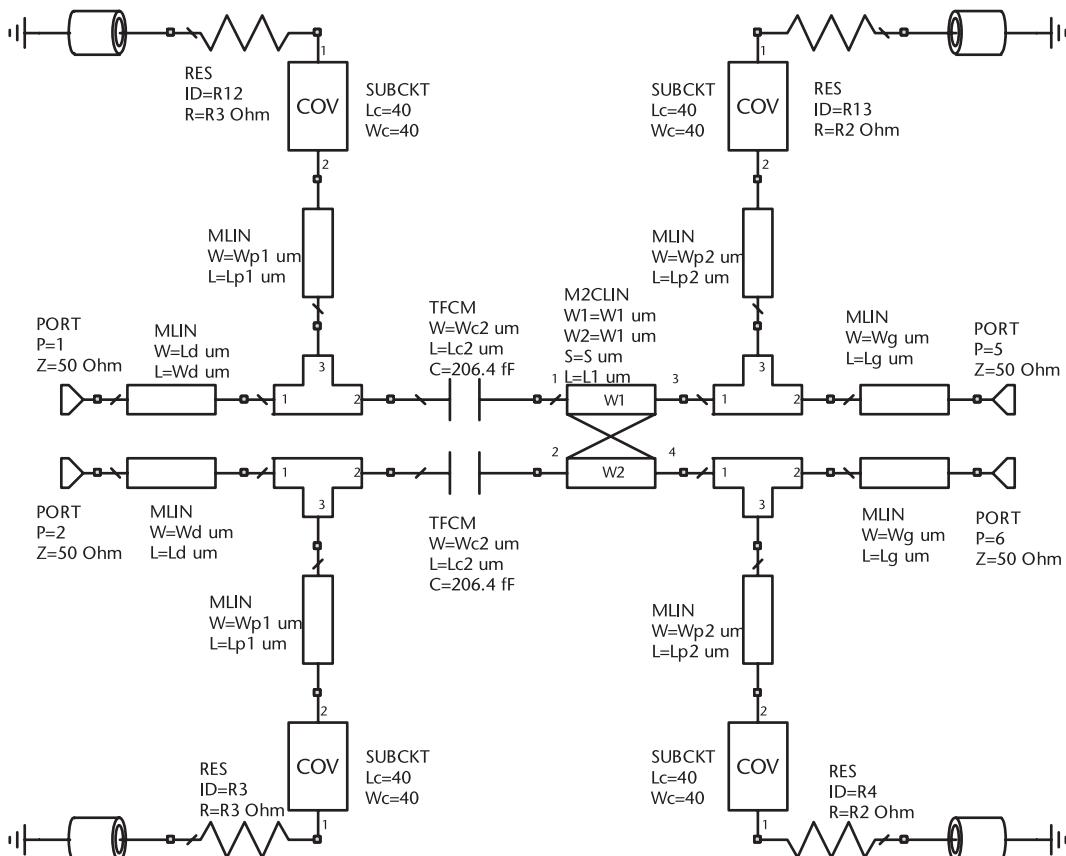


Figure 5.59 Microstrip schematic ISMN2 circuit block.

The best the optimizer could do is a gate impedance of  $Z_{s,g} = 9 + j30\Omega$ , including the stabilizing resistor. The mismatch to the impedance simulated in the load-pull is  $Z_g = 12 - j30\Omega$ , showing a significant difference in the real part.

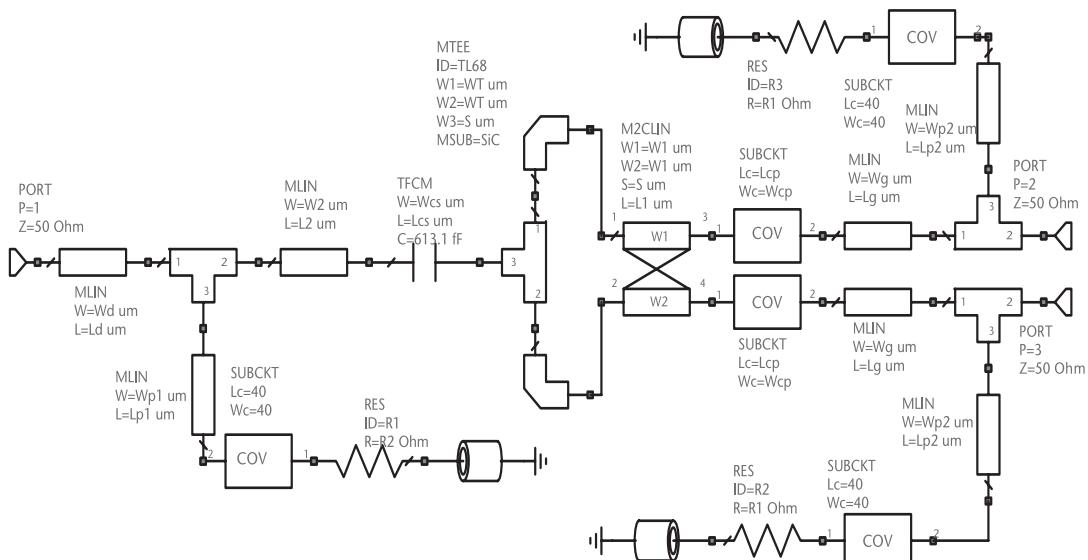
The other circuit elements, IMN and ISMN1, are designed based on the conjugate matched impedances derived from S-parameters. The schematic for ISMN1, shown in Figure 5.60, uses a series resonance at the gate and a capacitor in shunt to improve bandwidth. The drain also uses a series resonant line followed by a quarter-wave-long line for biasing.

The microstrip schematic for IMN is shown in Figure 5.61, showing the gate resonator on port 2, a Type-D matching network and resistor in series with a quarter-wave-long line for low-frequency termination.

### 5.6.3 Optimization Process

The following is the optimization process:

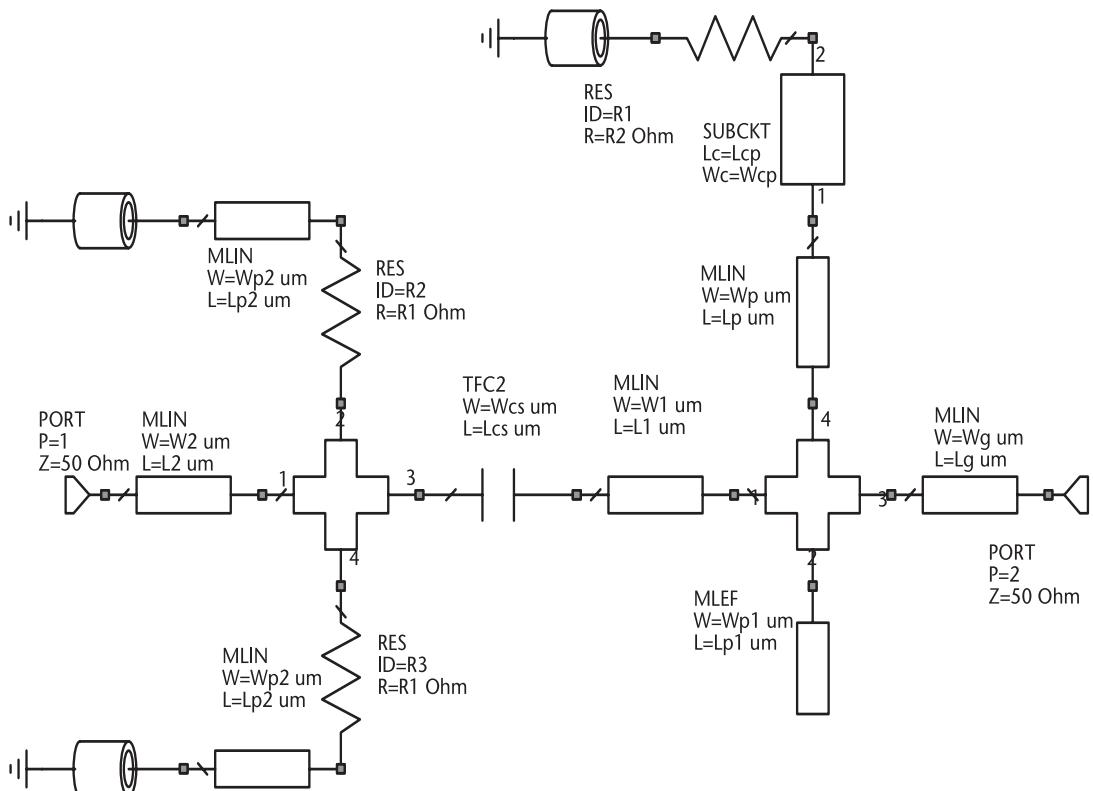
- *First run:* After the preliminary design of the amplifier blocks are made, the ISMN2 and OMN blocks are frozen, and the elements contained in the circuit blocks IMN and ISMN1 are optimized for gain. The target was a small-signal gain of 30 dB and a minimum input/output return loss of 10 dB. Two circuits were optimized, one for class A and another for class AB.
- *Second run:* The matching blocks were designed based on the terminations originating from a load-pull extracted from a nonlinear model. The initial distortion evaluation was made by applying two tones at the gate of the amplifier biased in class A. The rejection of the third-order intermodulation products at an output power of 16 dBm (single tone) was equal to 23 dBc. This is a reasonable value but still not enough for this class of amplifier. Therefore,



**Figure 5.60** Microstrip schematic for an ISMN1 circuit block.

there is a need for a fine-tuning on the impedance of the ISMN2 and OMN blocks. They are needed to compensate for the effects of device reverse gain of cascading gain stages and the nonlinear reactance effects at the gate of the power device. The complete amplifier was submitted to optimization carried out at 5 frequencies in the band for an input drive between  $-3$  and  $+3$  dBm, targeting  $IM_3$  and  $IM_5$  levels of  $-12$  dBm. Notice that  $IM_5$  has to be included in the optimization process to avoid a level higher than  $IM_3$  within the desired power range. Therefore, both  $IM_3$  and  $IM_5$  are expected to be lower than  $-12$  dBm for the power level selected in the optimization process. Initially, only IMN and ISMN1 were optimized and then ISMN2 was also submitted to optimization. That step resulted in a 5-dB improvement.

- *Third run:* The optimization in this step is for all circuit blocks and includes the gate and drain termination at baseband frequency, in this case, 100 MHz. The bias ports are paths for these signals, and the terminations affect the magnitude of the even-order distortions in band. Thus, a resistor is connected at the bias port from the gate and drain of each device to a large capacitor to ground. The effect of these terminations was described in [8]. After the optimization, it was found that the power stage requires a low resistor value at the gate and a high resistor value at the drain. On the other hand, the drain of the driver stage requires a low resistor value. Details of how to include those terminations in the bias circuit are shown in Appendix A. The optimization

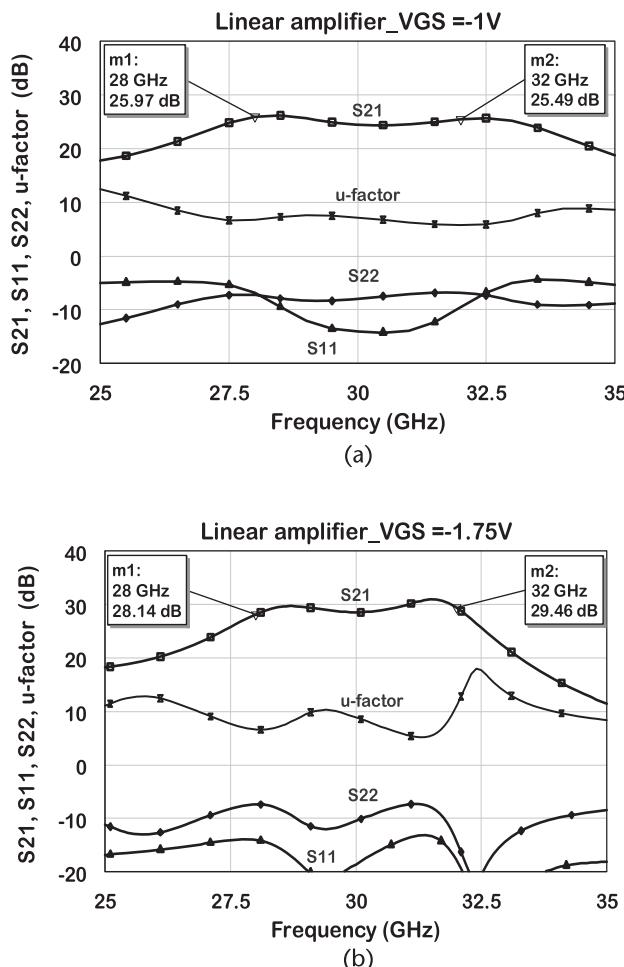


**Figure 5.61** Microstrip schematic for IMN circuit block.

also showed that the best second-harmonic termination for this specific circuit is an open at the drain and a short at the gate. The circuit dimensions shown in previous schematics are the values obtained after optimization. The circuit optimizations searched for a target level of IMD but also tried to maintain the output power, which means that the impedances will be somewhat different than the values determined by the load-pull.

Figure 5.62(a) shows the small signal parameters in decibels for the device biased in class A. Notice that, within the desired band of 28 to 32 GHz, the gain is greater than 26 dB and falls off smoothly. The input return loss is better than 10 dB and output is better than 8 dB.

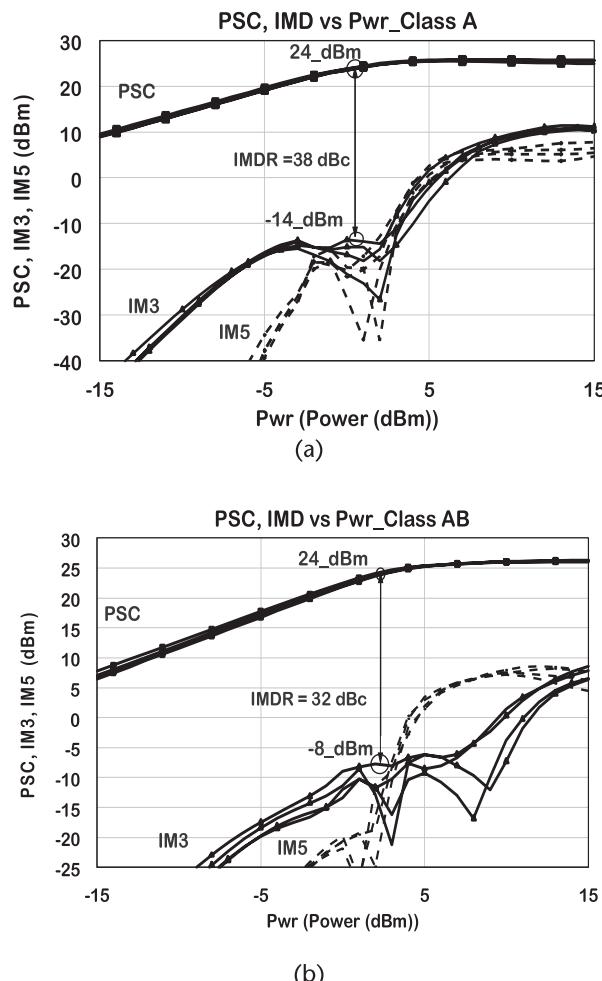
A large margin of stability is observed in the  $\mu$ -factor values. A higher gain is observed in class AB, shown in Figure 5.62(b). Stability was secured by increasing the stabilizing elements, gate resistor and source inductance. In spite of the gain reduction introduced by the stabilizing elements, the device gain within the band



**Figure 5.62** Linear performance for class A and AB bias: (a) S-parameters class A linear amp, and (b) S-parameters class AB linear amp.

is above 28 dB. Stability margin is larger than 5 dB and return losses are overall better than class A.

The linearity performance for class A is shown in Figure 5.63(a). The third-order distortion power level is represented by a solid line and the fifth-order distortion power level is represented by a dotted line. The IMR for both orders is 38 dBc at a single carrier power of 24 dBm. The intermodulation level is fairly constant up to an input power of +2 dBm. This is a remarkable improvement from the initial 20 dBc. The  $IP_3$ , based on the extrapolation from the tangent to low level signals, does not translate the  $IP_3$  improvement caused by the circuit within the range of -5 to +5 dBm of input power drive. Therefore, it is better to use  $IM_{3,5}$ , and  $IP_3$  for specific output power levels. The linearity results for class AB operation are shown in Figure 5.63(b). They are obtained for  $V_{GS1} = -1.25V$ ,  $V_{GS2} = -1.7V$ , and  $V_{GS3} = -1.4V$ . The IMD level increases to a power of -8 dBm, at the same fundamental output power of 24 dBm.

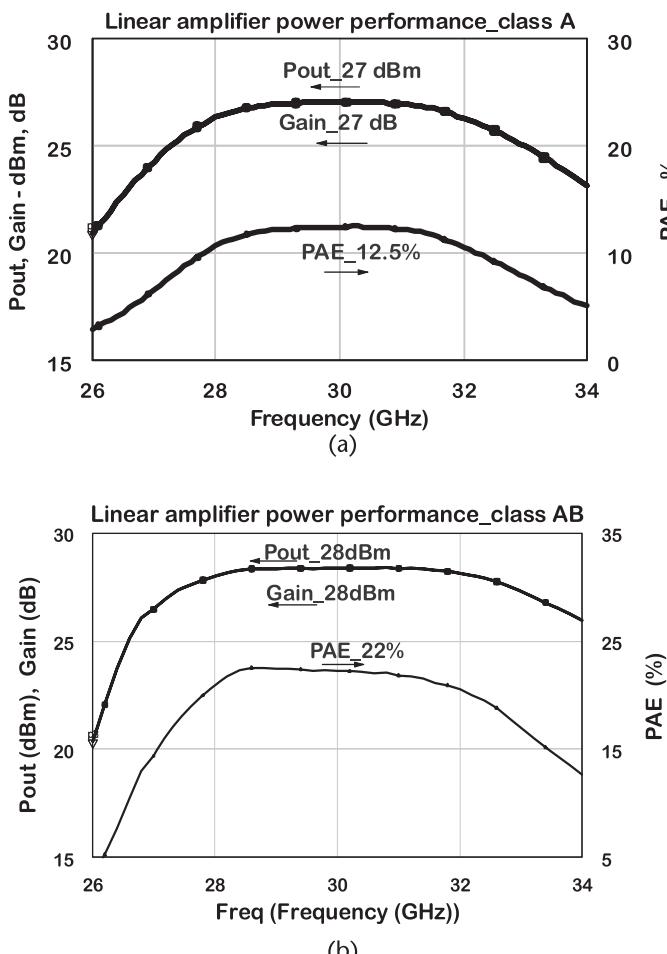


**Figure 5.63** Linearity performance for the linear amplifier: (a) two-tone test, circuit optimized for class A, and (b) two-tone tests, circuit optimized for class AB.

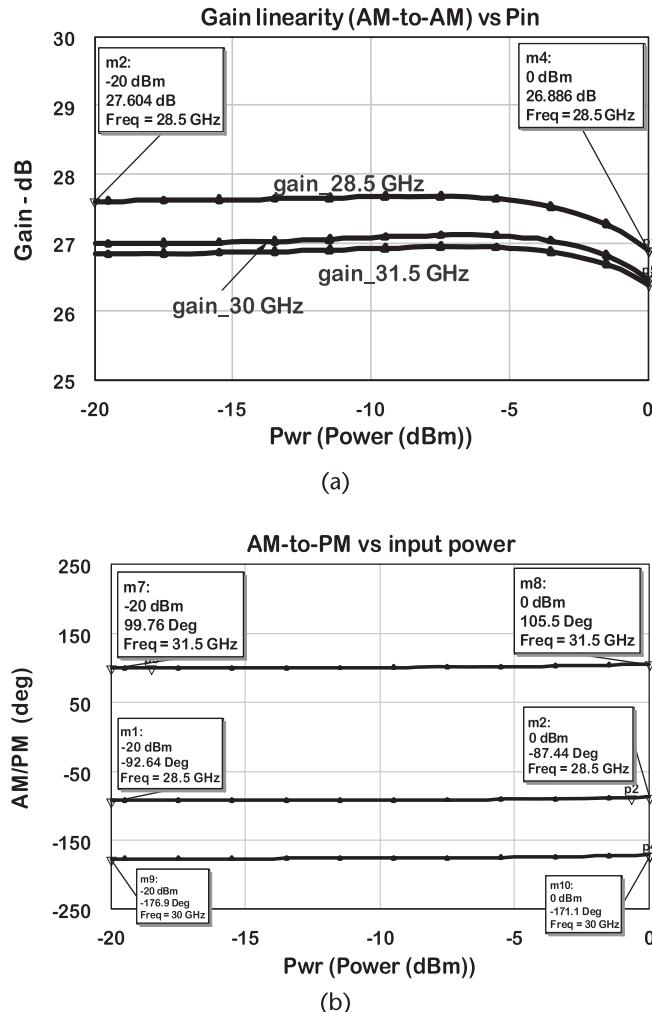
The single-tone tests are shown in Figure 5.64. Class A operation is shown in Figure 5.64(a), showing the power performance for an input drive power of +0 dBm. The output power is equal to 27 dBm, equivalent to two tones of 24 dBm. The gain is equal to 27 dB, and it achieves a PAE of 12.5%.

Figure 5.64(b) shows class AB power performance at the same drive power of 0 dBm. The output power increased to 28 dBm, and the gain also increased to 28 dB. The PAE increased by 9.5% compared to class A. The parameters are also quite flat within the 28.5 to 31.5-GHz band. The lower gain at class A is due to a lower transconductance compared to the value at  $V_{GS} = -1.75V$ .

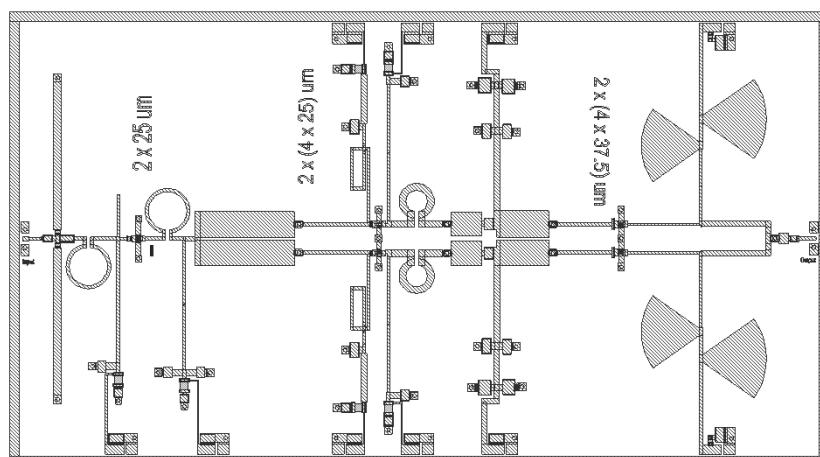
The simulated single-tone AM-to-AM expressed in terms of gain is shown in Figure 5.65(a) for class AB operation at three frequencies within the band. The  $P_{1dB}$  gain compression is at an input drive of  $P_{in} = 0$  dBm. The AM-to-PM is shown in Figure 5.65(b), for three frequencies in the band. There is about 5° modulation over the 20-dB power range.



**Figure 5.64** Power performance for the linear amplifier: (a) single-tone tests, circuit optimized for class A, and (b) single-tone tests, circuit optimized for class AB.



**Figure 5.65** The linearity in terms of AM-to-AM is AM-to-PM: (a) AM-to-AM vs input drive, and (b) AM-to-PM vs input drive.



**Figure 5.66** Layout for the linear amplifier. Chip size  $4.3 \times 2.4 \text{ mm}^2$ .

The resulting circuit layout for the amplifier is represented in Figure 5.66. The circuit dimensions are  $4.4 \times 2.4 \text{ mm}^2$ . The layout does not include the resistors for the circuit stabilization.

## 5.7 Case Study: 5G New Radio (NR) Amplifier

Before starting the design considerations, let us first determine the specifications for the power amplifier for this application. The specifications for the 5G New Radio are published by the Third Generation Partnership Project (3GPP) organization [9]. The EVM requirements are shown in Table 5.5, illustrating the dependency on modulation type. Let us also assume that a handset can support 64 QAM modulation; therefore, according to Table 5.5, a maximum EVM of 8% is accepted. As another specification from the same reference, the ACPR is required to be 28 dBc for frequencies between 22 and 33 GHz. The power parameters are assumed to be the same as the linear amplifier, that is, a  $P_{1\text{dB}}$  of +27 dBm and a signal power of 24 dBm. The digital parameters are assumed to be EVM = 4% and ACPR = 28 dBc for the same signal output power.

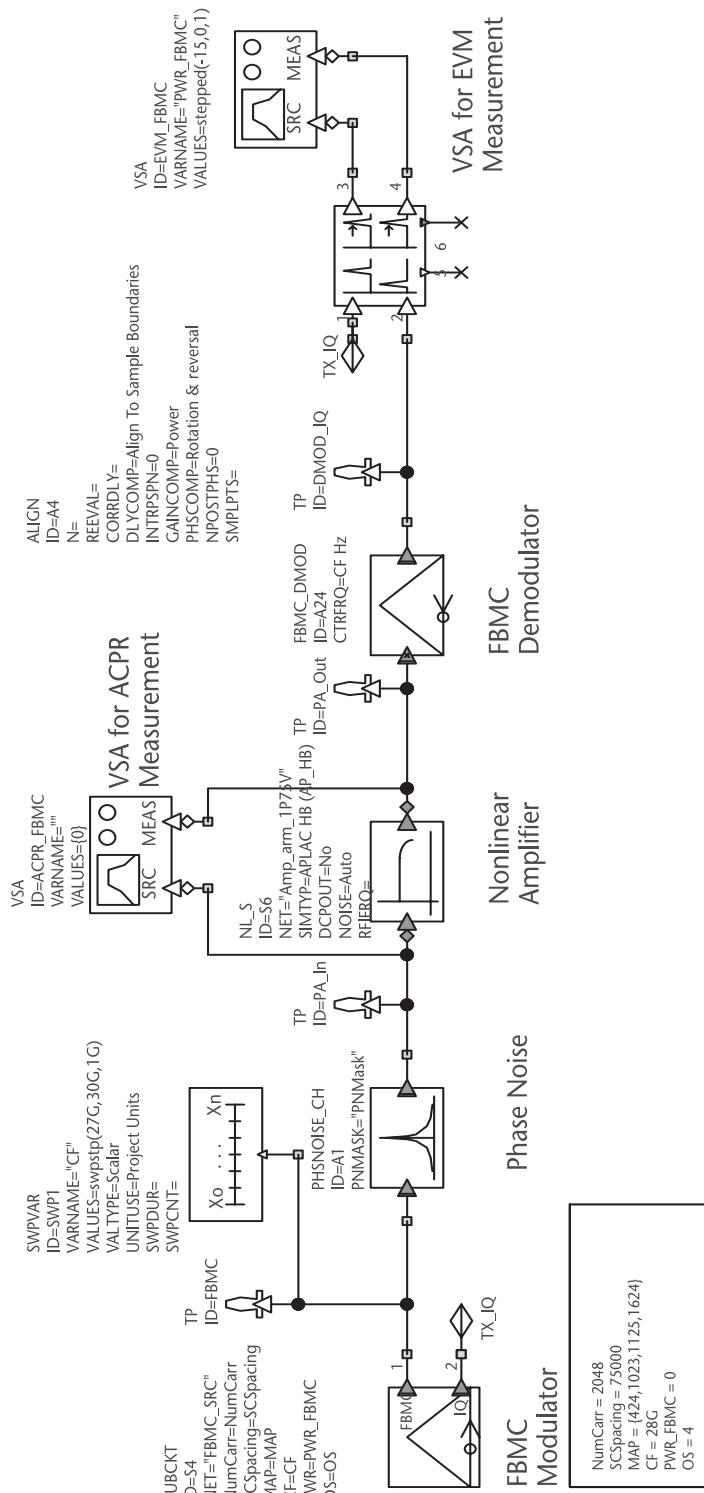
The evaluation of ACPR and EVM from an amplifier requires a series of parameters determined from the circuit simulator. The parameters are generated for a few frequencies in the band and for a power sweep from  $-15$  to  $+15$  dBm, with at least 1 dB per step or less. The single-tone evaluations provide  $P_{\text{sat}}$ ,  $P_{\text{out}}$  (fundamental),  $P_{\text{out}}$  (second harmonic),  $P_{\text{out}}$  (third harmonic), and AM-to-AM and AM-to-PM as a function of  $P_{\text{in}}$ . The two-tone test provides  $IM_2$ ,  $IM_3$ ,  $IM_5$  distortion components. This information is part of a data file used to generate a nonlinear behavioral model. The model is then taken to a system simulator, which evaluates the ACPR, the EVM, and other system parameters. An iterative process is then used with both circuit and system simulators to optimize the amplifier.

Fortunately, the software companies provide templates where the cosimulation between the circuit and system are integrated. Thus, once the system simulator is activated, it does the system simulation and the circuit simulation. The measurement system developed by Cadence\_AWR under license in Figure 5.67. It contains a generator for the 5G signal denominated a filter bank multicarrier modulation (FBMC) modulator and a demodulator. The FBMC is followed by a notch filter [10]. The notch filter is part of the waveform generation and in addition allows determination of NPR for noise power measurement.

**Table 5.5** Modulation Schemes and EVM Requirements for 5G New Radio

Modulation Scheme	Required EVM (%)
QPSK	17.5
16QAM	12.5
64QAM	8
256QAM	3.5

The 256QAM applies to base stations



**Figure 5.67** System schematic for EVM and ACPR, licensed for publication by Cadence\_AWR.

**Table 5.6** Impedance for Best EVM

Parameters	IMN		ISMN1		ISMN2		OMN	
	IMD	5G	IMD	5G	IMD	5G	IMD	5G
W <sub>d</sub>			17	15	16	16	15	15
W <sub>1</sub>	31	21.7	136	136	267	267	23	25
W <sub>2</sub>	38	34.7	15	15			42	42
W <sub>p</sub>	16	15					22	25
W <sub>cs</sub>	25	26	50	43	17	17	38	36
W <sub>cp</sub>			10	10	35	35	22	24
W <sub>g</sub>	63	15	15	15	12.5	12.5		
W <sub>p1</sub>	15	15.6	17	20	10	10		
W <sub>p2</sub>	39.7	39.4	20	20	32	26.6		
L <sub>g</sub>	31.8	34	289	289	393	133.5		
L <sub>d</sub>			748	845	895	728	473	325
L <sub>cp</sub>			29	17			11	11
L <sub>cs</sub>	80	80	47	47	45.6	43	49.5	40
L <sub>p1</sub>	147	102	1,157	1,063	931	834		
L <sub>p2</sub>	602	760	968	1,040	1,594	1,503		
R <sub>1</sub>	63	66	1.5	2.8			2,280	4,000
R <sub>2</sub>	11	8	2,690	70	1,536	1,836		
R <sub>3</sub>					1	1		
S			5	5	5	5	125	125

The block diagram also contains a spectrum analyzer for ACPR evaluation and another spectrum analyzer for EVM. In addition, there is a block to prepare the signal for the EVM constellation. Before starting using the template, tests were made to find the measurement accuracy. The direct connection gives an EVM of 1.5% equivalent to 36 dB. It is dependent on the phase noise characteristics of the notch filter. An additional system block not shown in the diagram consist in the connection of power amplifier to a spectrum analyzer for power control. When using the template, this additional block is connected to the main test bench.

Out of curiosity, the linear amplifier from the previous case study was tested in this system and it was found it is quite close to the desired results. The resulting performance for the class AB amplifier is a power of 21 dBm for an EVM of 4% and 22.5 dBm for an EVM of 6%. These results are remarkably close to the desired objective. Class A was not considered for its lower efficiency.

The design of an amplifier for 5G applications starts with the determination of the optimum source/load for the best EVM and ACPR parameters for a unit cell FET. In addition, other parameters such as gain, input/output match, power, and efficiency are also evaluated. It has already been mentioned that a real load-pull system should be employed to determine these parameters. If a nonlinear model is available, then a numerical load-pull is performed, using the templates provided

by the major software companies. One can determine the contours for power, efficiency, gain, EVM, ACPR, BER, and so forth. Then the optimum impedances are used to generate the matching circuits, following the procedures of the first case study. After the design is completed, the amplifier is then evaluated by the system simulator. In general, there is a need for some small adjustments in the circuit for best performance.

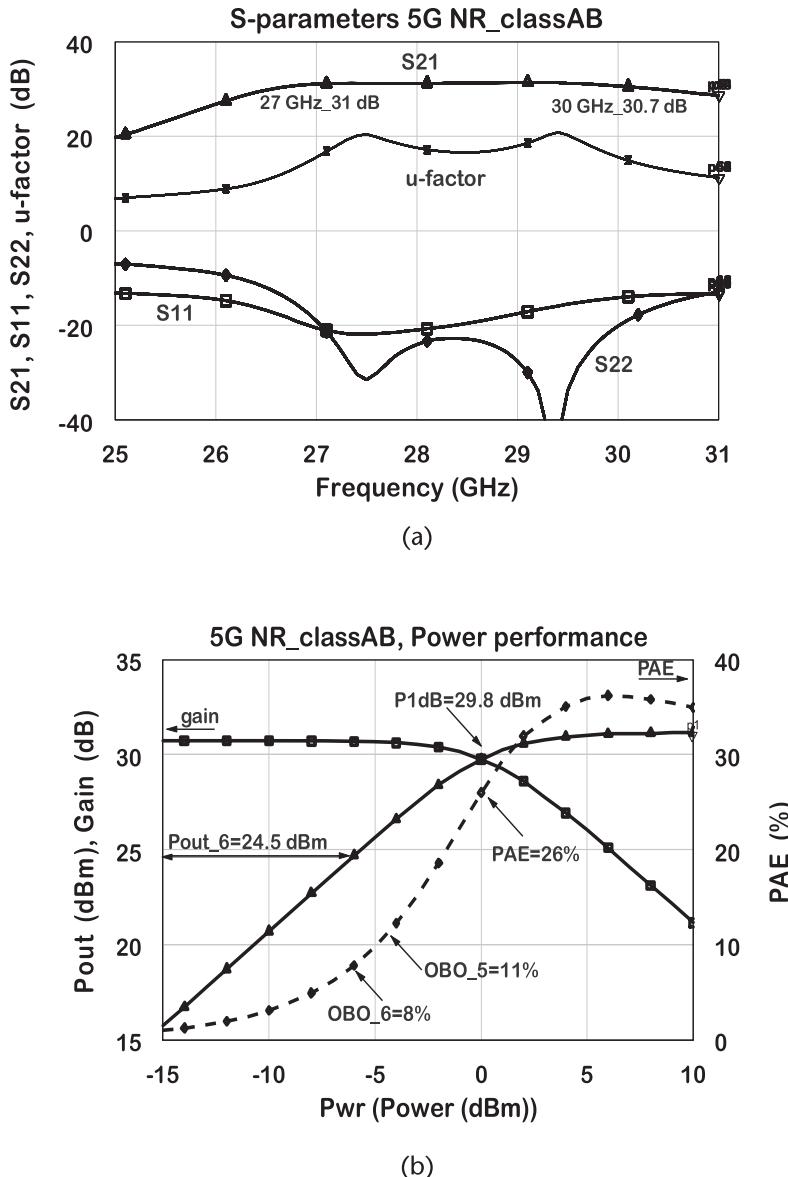
An alternative faster process is proposed in this book. Instead of optimizing the amplifier EVM and ACPR directly with the cosimulator, it is more practical to first optimize the amplifier in the circuit simulator, for low  $IM_{3,5}$ . Then the optimized amplifier can be fine-tuned for the digital signal in the system simulator. We applied this option to the class AB low distortion amplifier. The EVM and ACPR was evaluated and the amplifier parameters were manually tuned in the system simulator. The tuning was mainly applied to the OMN and ISMN2 circuit blocks. After a reasonable number of iterations, we obtained the parameters listed in Table 5.6. The circuit parameters for both the IMD and 5G circuits are shown in the table to make it easier to compare what changed from the amplifier optimized for IMD. Major changes occurred on elements  $L_p$ ,  $R_1$  from the OMN block, and  $L_1$ ,  $L_g$  from ISMN2 block.

The small-signal amplifier performance for the optimized 5GNR amplifier is shown in Figure 5.68(a) for the 25 to 31-GHz band. The gain within the 27 to 30-GHz signal band is 30 dB with better than 1-dB flatness. The large-signal performance at the center frequency of 28 GHz is shown in Figure 5.68(b). A  $P_{1\text{dB}}$  power of 29.8 dBm is depicted, with a respectable 26% PAE.

The EVM measured for a 16QAM signal is shown in Figure 5.69(a) as a function of output power for four frequencies within 27 to 30 GHz. The EVM shows a value of  $-28$  dB (4%) at an output peak power of 24 dBm and  $-24$  dB (6.3%) at a power level of 25.7 dBm. Those numbers are below the specified worst case of 8%, per 3GPP specifications. With a 64QAM signal, those numbers are maintained, but the EVM level at a low output power increases by a couple of decibels. The ACPR is illustrated in Figure 5.69(b), showing a value of  $-38$  dBc for an EVM of 4% for the same frequency range. The effect of baseband termination from open to short shows no effect on EVM and no more than 4-dB improvement in the ACPR, similar to the value found in the IMD amplifier. We also verified that a 64QAM does not change the ACPR at the same power level.

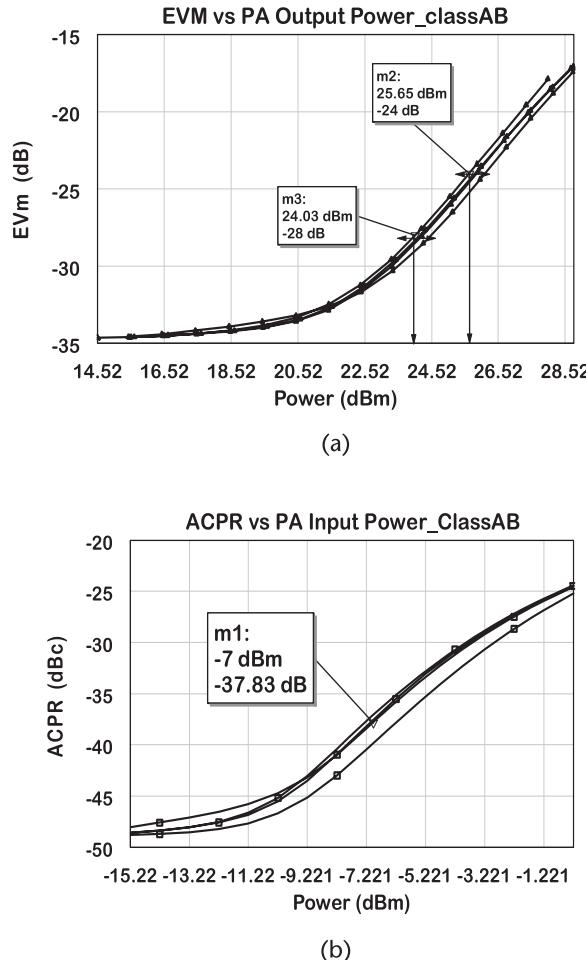
Additional curves of interest are the output amplifier spectrum and the constellation evaluated by the test bench. The spectrum is displayed in Figure 5.70(a) for the input drive level of  $-7$  dBm for 64QAM modulation. The power spectrum shows that the intermodulation products are visually 30 dB down from the peak output power. The NPR shows a value of 30 dBc. The constellation in Figure 5.70(b) shows a clear identification of the symbols at an input power of  $-7$  dBm, corresponding to an EVM of 4%.

Visually, the constellation is still clear at this power level. However, at  $-4$  dBm, the symbols are merging to each other. Another result not shown is the AM-to-AM measured by the digital system, which is similar to the  $P_{\text{out}}(P_{\text{in}})$  simulated by the single tone in Figure 5.68(b). It has been demonstrated that the procedure used for the design of amplifiers for digital signals provides sufficient performance for use in



**Figure 5.68** S-parameters and single-tone power simulations: (a) small signal 5GNR performance, and (b) large signal 5GNR performance.

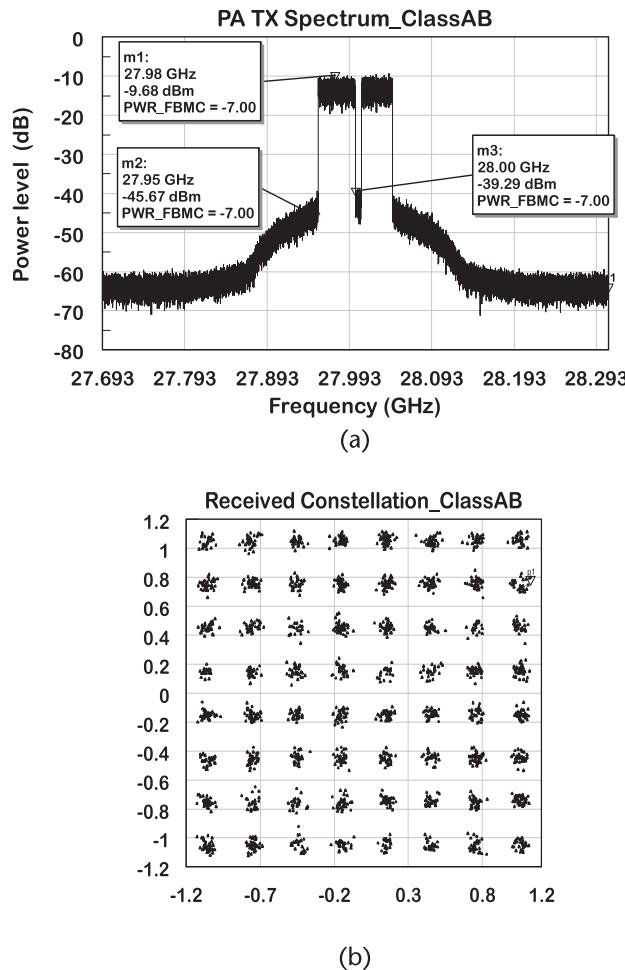
5G New Radio applications. However, one can see that the best this technology can do with the amplifier operating around a 6-dB backoff from the  $P_{1\text{dB}}$  power is a PAE below 20%. Therefore, there is a need to use some means to improve efficiency from the device technology side and from the circuit design side. An example to improve both linearity and efficiency is demonstrated in Chapter 6, with the application of the Doherty architecture. There are other means to improve efficiency, such as the EER, envelope elimination and restoration techniques [11]. The amplifiers designed for linearity can be used in any of these architectures.



**Figure 5.69** Evaluation of the amplifier digital parameters between 27 and 30 GHz: (a) EVM as a function of output power, and (b) ACPR as a function of input power.

## 5.8 EM Analysis Methodology

The use of electrical models has been successfully applied to the design of microwave amplifiers, without the need of electromagnetic analysis. This approach does not work when the frequency of operation is higher than 20 GHz. At millimeter-wave frequencies, the coupling and radiation effects are more severe compared to microwaves. In addition, the elements often are used above the restrictions imposed by the equations describing their electrical performance. That is the key difference between microwave and millimeter-wave design. For example, when one compares the EE models for specific microstrip elements to the models generated by EM analysis, there is not much difference between them. However, when they are assembled to make an OMN or ISMN, discrepancies are found. Hence, EM analysis is essential to any millimeter-wave design.



**Figure 5.70** Illustration of the power spectrum and constellation at the power amplifier output: (a) spectrum to measure ACPR, NPR, and (b) constellation for  $P_{in} = -7$  dBm.

The EE models are essential to design any circuit function. At this point, the EM technology is not advanced enough to be able to design circuits directly with EM models. The problem is the coupling effect is a function of the circuit that is not yet decided how it is going to be. The alternative then is to optimize the circuits with EE models, convert the models to EM, find the discrepancies, and correct the layout in such a way that they emulate the EE models. This design phase used to take a long time to generate the desired EM models for the difficulty in modifying the element dimensions, resimulating, and comparing with the electrical models. Currently, some of these tasks have been automated by some commercial software, considerably reducing the design time. In this book, it is shown how this optimization is done manually, giving an insight into how different EE and EM models can be.

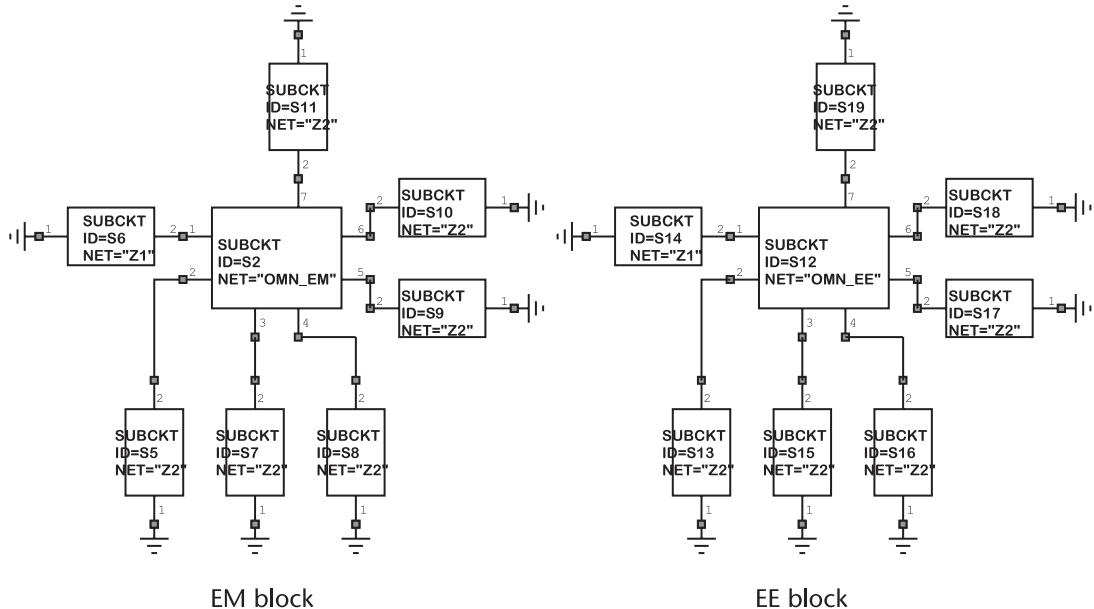
I used several methods, and the one selected in this book is the most robust in the sense that it does not take the direction of unrealizable circuits and does not incur convergence issues. The method used in this context is based on a step-by-step process. It consists of comparing the EE and EM for each circuit element and correcting the differences in impedance by changing the EE layout using the tuning tool, until they produce approximately the same results. However, the objective is to vary the EM parameters so that they match the EE performance. The direction of change of parameter is equal to the reverse direction used to modify the layout so that EM matches the EE model. The description is to correct the port impedances, but it should also be used to correct the transfer parameters. The process starts with two blocks, an EE block containing one circuit element plus an EM block containing the corresponding EM S-parameters. After a solution is found, another element is added to each block and the process is repeated. Thus, the differences between the EM and EE models are addressed by small increments simplifying the solution process. The process finishes when all elements have been corrected.

Before starting the EM analysis, the settings of the EM solver are important in this process. One should set the accuracy for the iterative solvers and the matrix compression as high as possible, checking if the simulation time does not become excessive. Considering the dimensions for the shunt capacitors, it is advisable to use a grid size cell of  $1 \times 1 \mu\text{m}^2$ . Increasing the size to  $2 \times 2 \mu\text{m}^2$  reduces the simulation time, with nearly the same accuracy as long as the elements do not use layout dimensions that do not fit on the grid. Using thin metal speeds up the analysis compared to using thick metal. When analyzing the EM of an OMN circuit block, it may be adequate to use thick metal for the traces on the RF path. Usually, the simulated losses are lower for this condition and also closer to measurement results obtained from real test circuits.

It is convenient for the analysis to separate the EE and EM S-parameters into two distinct circuit blocks in the manner shown in Figure 5.71. If  $Z_1$  is a  $50\Omega$  termination, then the circuit is a 6:1 power combiner to be used as an output matching network. Then  $Z_2$  is the impedance to be connected to the drain. Port 1 is a regular S-parameter port, while all the other 6 ports represent the port impedance plus the coupling to the other ports, given by (4.87). In order to read the drain impedance,  $Z_2$  is replaced by  $50\Omega$  ports. To read the impedance at port 1,  $Z_2$  is replaced by the drain impedance  $Z_d$ .

If  $Z_1$  represents the drain impedance, then  $Z_2$  can represent the gate impedance and the circuit is a 6:1 transformer/divider for an interstage application. In this case, to read the impedance of port 1, the 6 gate ports are terminated with  $Z_g$ . To read the gate impedance accounting for the coupling between each port, the drain is terminated with  $Z_d$ .

Another useful comparison is the balance between both circuit blocks, using the circuit arrangement in Figure 5.72. Because this evaluation has to be done with the ports conjugate-matched, the insertion loss is measured from a specific  $R_g$  resistor in relation to the  $R_d$  resistor. The balancing is not measured from circuit block ports as it is conventionally done, but we avoid the conjugate match issue at port. Both approaches give approximately similar results.



**Figure 5.71** Circuit for comparing  $S'$ -parameters from EE and EM circuit blocks.

### 5.8.1 EE-to-EM Conversion of 3:1 Combiners

Let us use the circuit of Figure 5.36 to demonstrate how to convert EE to EM. The result of the EM analysis to the aforementioned circuit is shown in Figure 5.73(a), where the differences between the S-parameter values are illustrated. We can also see in Figure 5.73(b) the drain load impedance for the circuit. One of the ports shows an impedance above  $400\Omega$ . It is obvious that the  $R_L$  EM for this circuit cannot be used for the power amplifier. One of the causes for this behavior is related to the capacitor on top of the via model.

This element is located close to large-width transmission lines and the coupling affects its capacitance compared to the capacitance from the EE model. Therefore, the EM model is different from an isolated shunt capacitor. In this specific case, the capacitance from the EE model is found to be 15% larger in the EM simulation. One can also observe in Figure 5.73(b) that the circuit is out of balance and each port has a different value.

We started the conversion with the core for the 3:1 converter, consisting of the cross-element joining 3 input lines and 1 output line. The EE is shown in Figure 5.74(a). The corresponding EM layout is in Figure 5.74(b). Figure 5.74(c) anticipates the modification made to the S-parameters of the EE and EM models to be as close as possible.

The EM simulation results for the initial EM model is a direct generation from the EE model and exhibits the S-parameters shown in Figure 5.75(a). The curves show the S-parameters for one external and one center arm. The  $S_{44}$  port is similar to port  $S_{22}$ . In this particular case, we observe that the EE shows a difference between the outer and center arms. The final objective is to eliminate this difference.

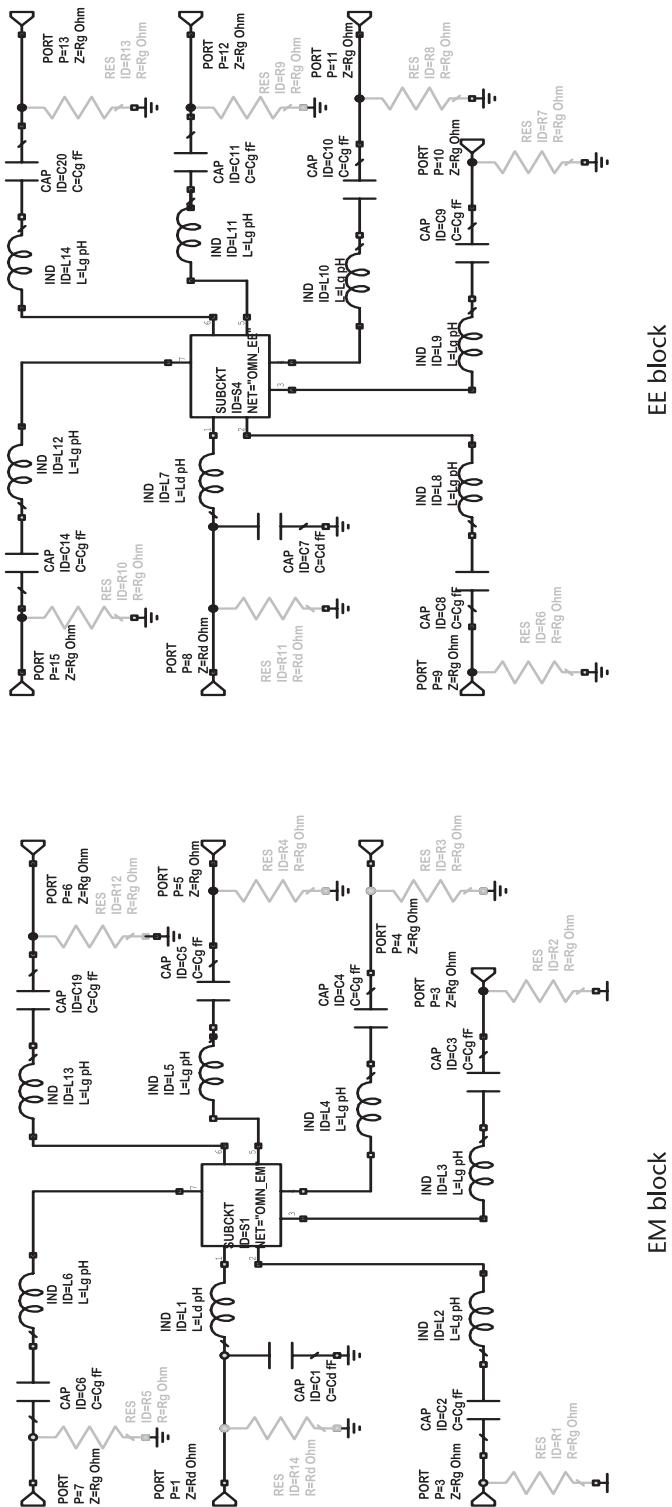
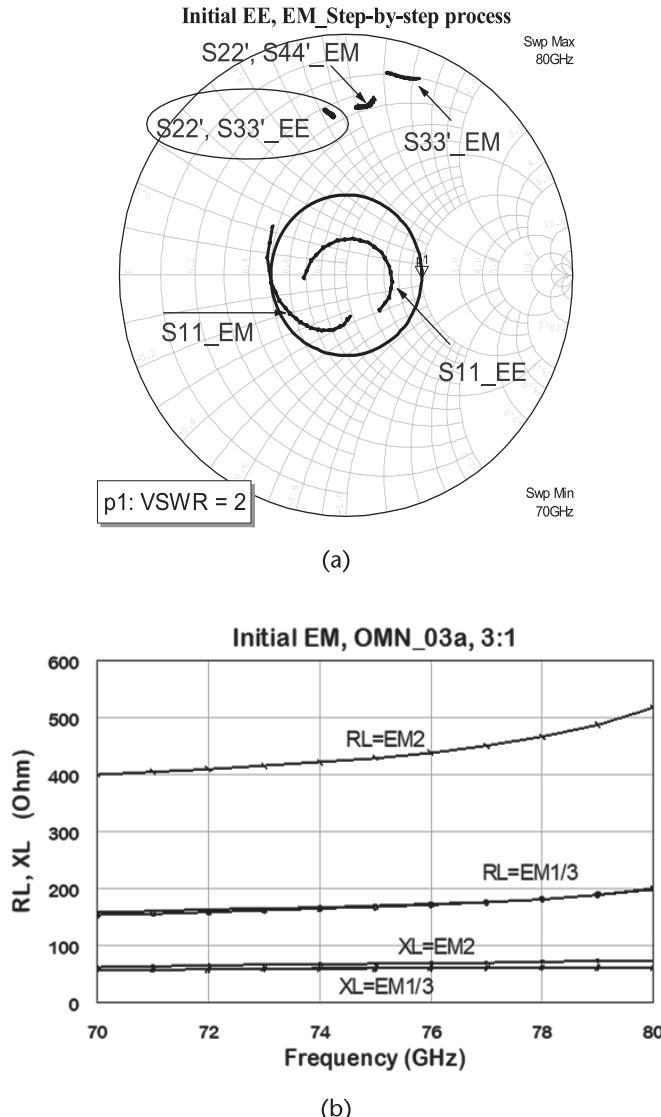


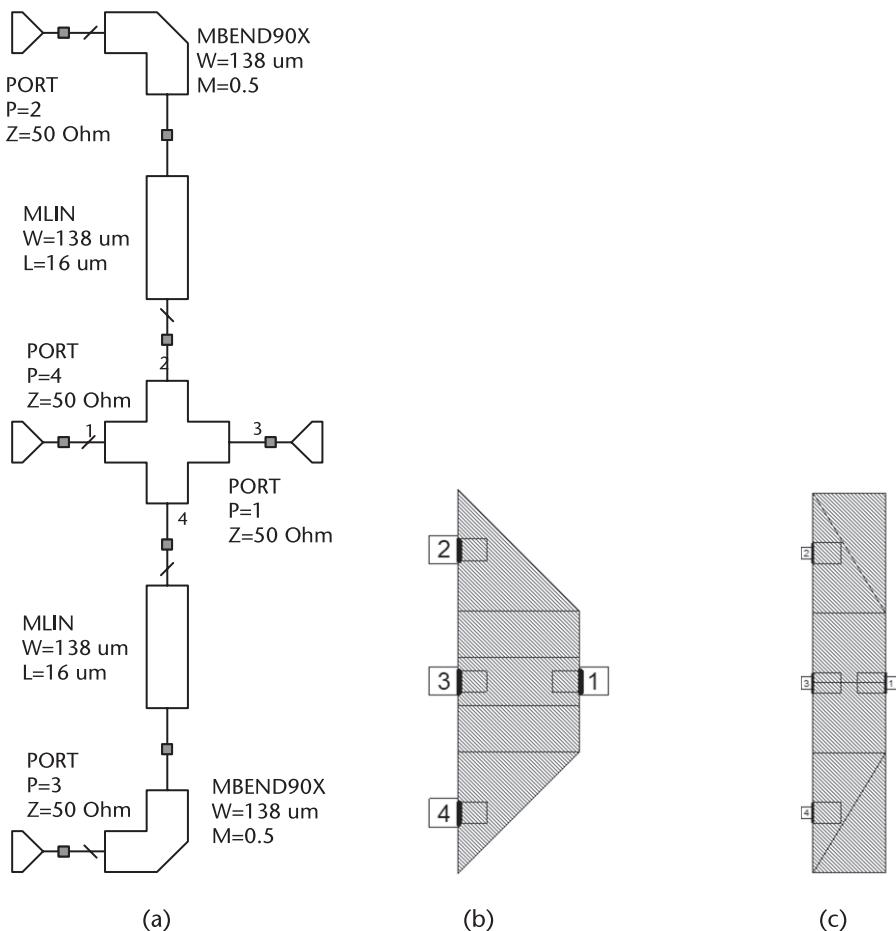
Figure 5.72 Circuit for evaluating transfer parameters from EE and EM circuit blocks.



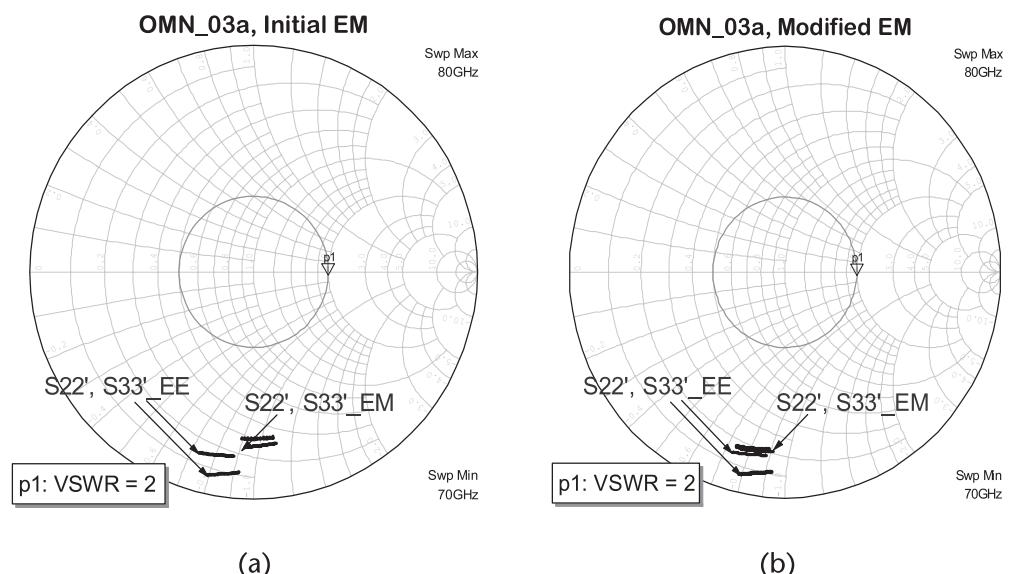
**Figure 5.73** Impedances measured on EM and EE blocks: (a) comparing the SEE an SEM, and (b) resulting curves for RL, XL at each port.

The following modifications were performed in the initial EM model represented in Figure 5.74(b).

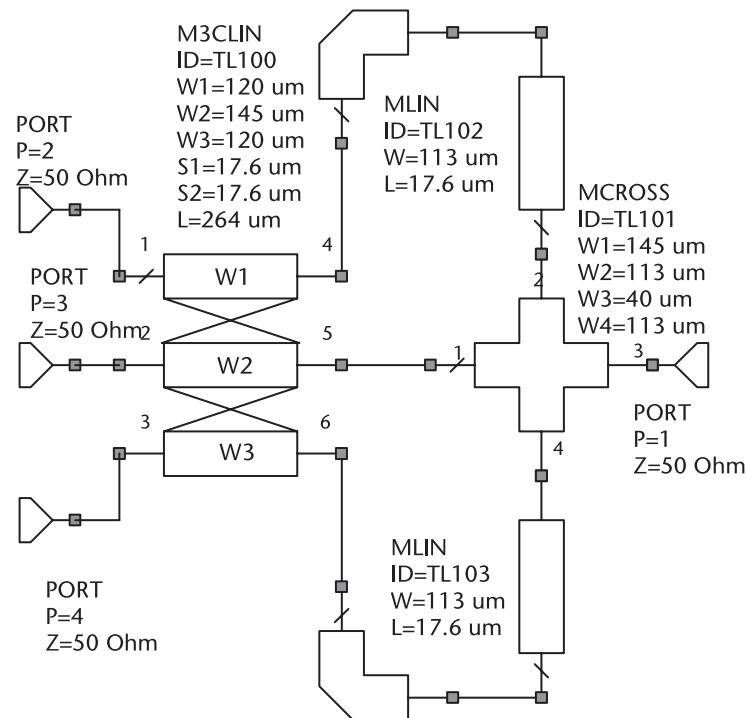
The EM magnitude was increased by eliminating the chamfer in the circuit. The phase difference between EM and EE was decreased by narrowing the x-dimension of the cross. The resulting S-parameters for the modified EM model is represented in the Smith chart of Figure 5.75(b). In the second step, we added the three-line coupler, generated the layout, and a new EM analysis was carried out. The representation of the respective EE microstrip circuit and the respective layout blocks are shown in Figures 5.76(a, b), respectively. The initial EM simulation for this layout shows the impedance represented in the Smith chart of Figure 5.77(a).



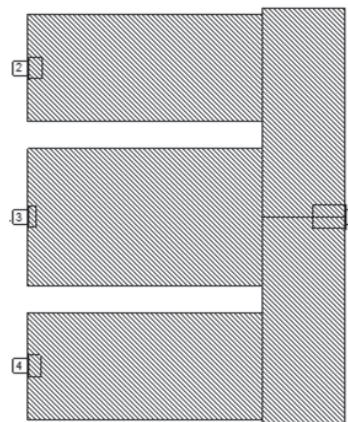
**Figure 5.74** Beginning of the step-by-step procedure: (a) EE model, (b) initial EM model, and (c) modified EM model.



**Figure 5.75** EM simulations for the first step: (a) EM for the initial layout, and (b) EM for the modified layout.



(a)

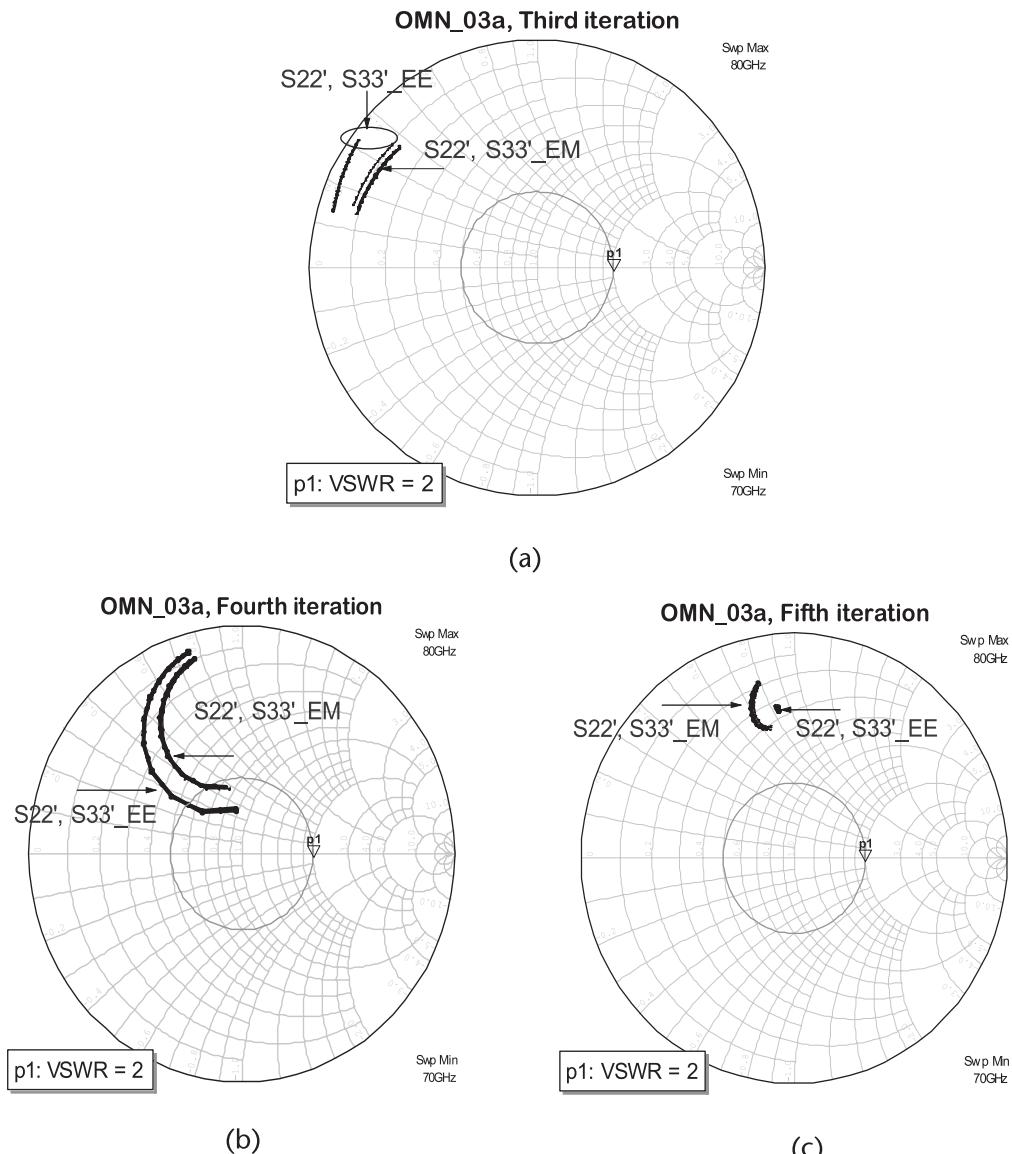


(b)

**Figure 5.76** Preparation for the second step: (a) EE for the second step, and (b) layout for the EM analysis.

In Figure 5.77(a), one can see two set of traces: one for  $S'_{22}$  and another for  $S'_{33}$  corresponding to the EE model. The two traces from the EM model are superposed to each other. In the fourth iteration, we added the shunt capacitors and the input drain resonating lines, resulting in an  $S'_{22}, S'_{33}$  EM curve with a close shape to EE in Figure 5.77(b). The fourth iteration EE model is illustrated in Figure 5.78(a) and the EM model is shown illustrated in Figure 5.78(b).

In the fifth iteration represented in Figure 5.77(c), we can see that the EM is not too far from the EE circuit and the EM is not too far from the solution. After the fifth iteration, we changed the representation from the Smith chart to the rectangular

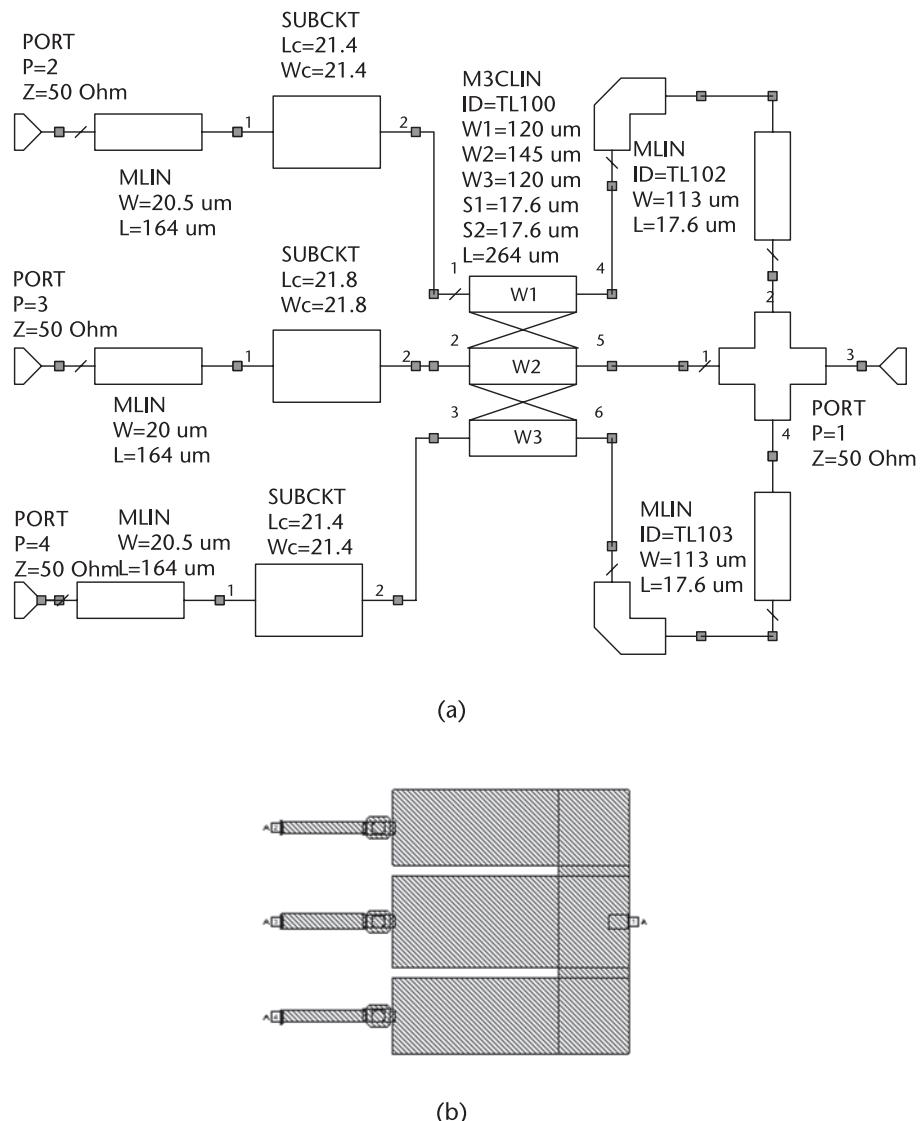


**Figure 5.77** EM simulations for the third steps and above: (a) third iteration, (b) fourth iteration, and (c) fifth iteration.

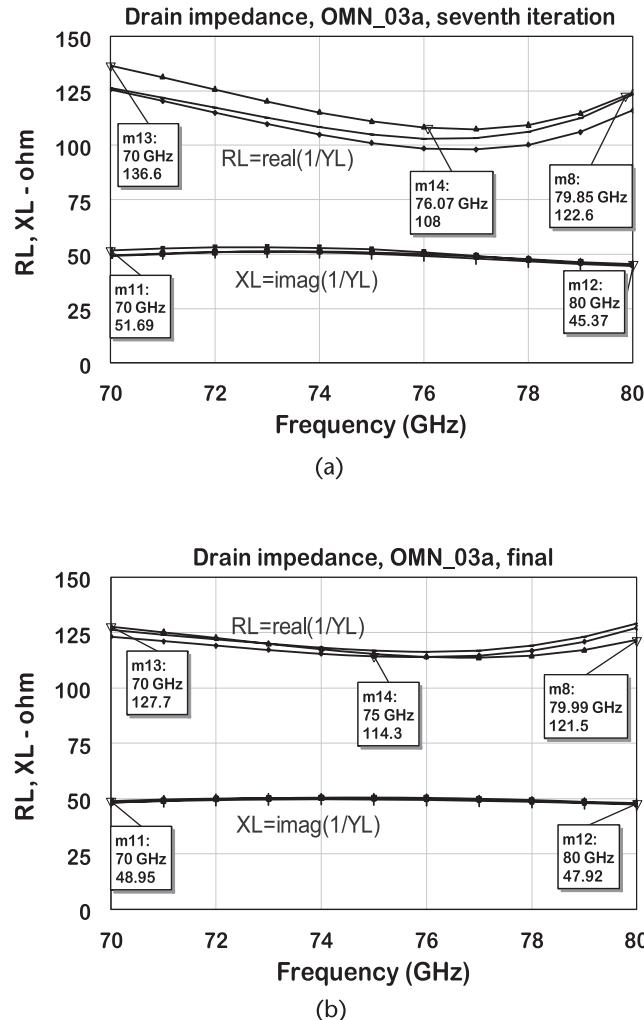
impedance plot. The curves in Figure 5.79(a) are now quite close to the final target of  $R_L = 118\Omega$  in parallel with  $j50\Omega$ .

The shunt capacitors and the width of the resonator lines were adjusted through a cut-and-try method to improve the balancing between the ports. Then the shunt capacitors, the shunt stub, and the output series lines were fine-tuned. This takes a few more iterations, depending on the experience of the designer. The final results are shown in Figure 5.79(b) for the drain load impedance simulation.

A faster alternative process is to consider the complete circuit from Figure 5.46 and its corresponding impedances represented in the Smith chart of Figure 5.73(a). One can see that the EE impedances are nearly a point, while the EM shows phase



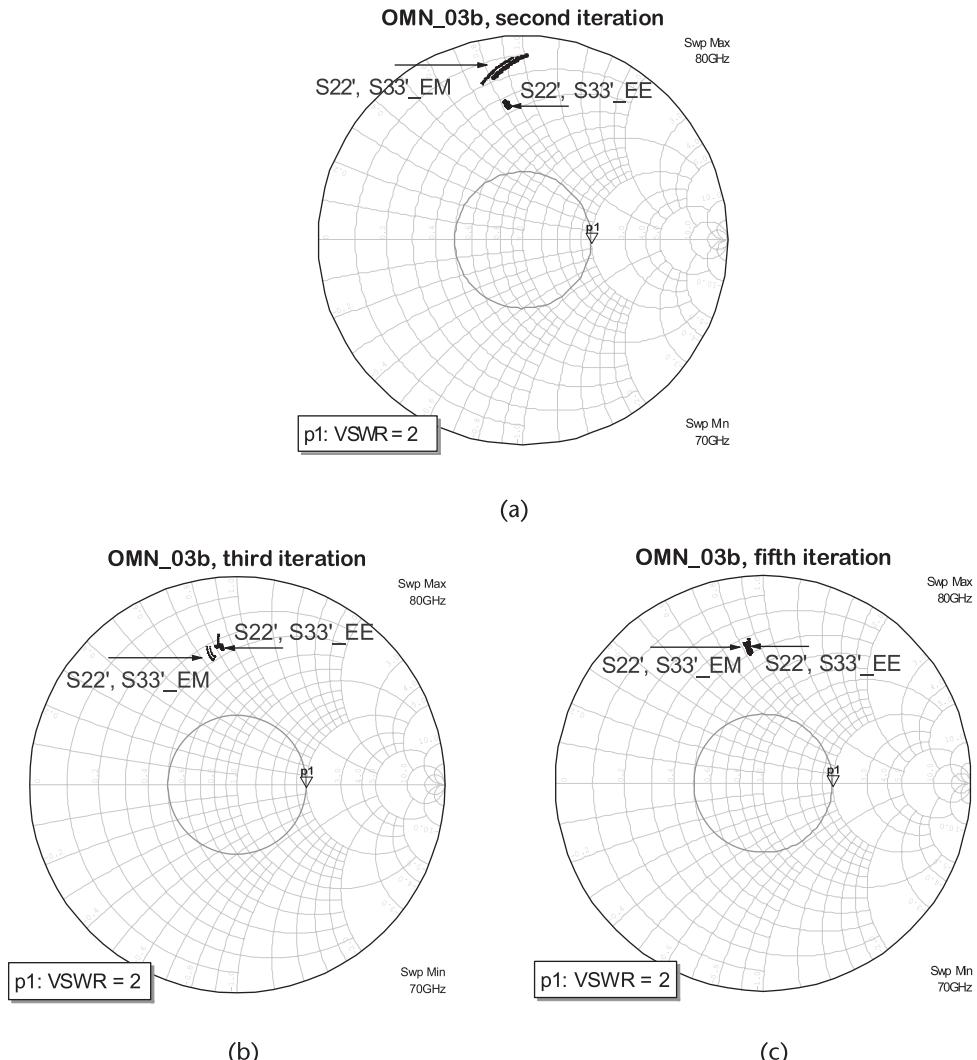
**Figure 5.78** Preparation for the fourth step: (a) EE for the fourth step, and (b) corresponding layout for the EM analysis.



**Figure 5.79** Impedances measured on the final EM block: (a) load impedance after correction, and (b) impedance after tuning shunt capacitors.

and amplitude variations. The phase can be adjusted by first checking which EE parameter moves the impedance trace over the EM trace, using the tuning tool. It was found that, by shortening the length of the resonator series lines, the length of the coupled lines, or the dimension of the junction, they all cause that effect. We changed the first two, which resulted in Figure 5.80(a). To change the amplitude, we focused on the shunt capacitors, which we know is overestimated by the shunt capacitor model. They were shortened by 4.5  $\mu\text{m}$  at each side, resulting in Figure 5.80(b). That was obviously too much, so we increased the capacitor dimensions by 1  $\mu\text{m}$ , resulting in the trace in Figure 5.80(c).

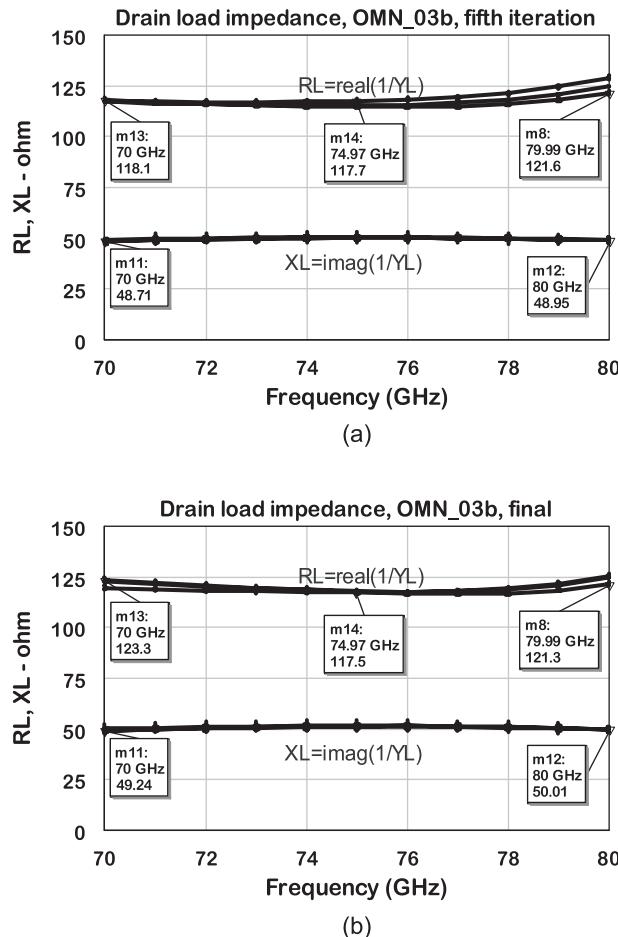
After the fifth iteration, the circuit impedance is as shown in the rectangular plot of Figure 5.81(a). A few tuning cut-and-try iterations were performed by adjusting



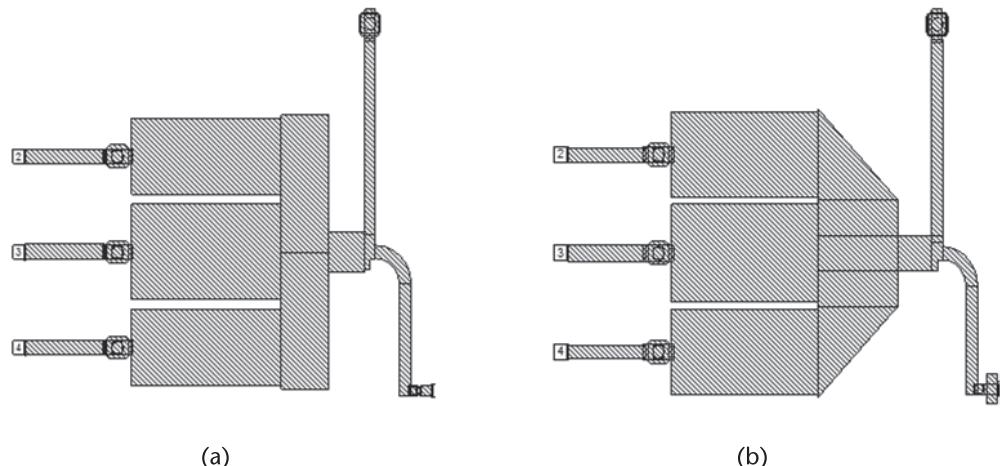
**Figure 5.80** Drain impedances measured on EM and EE blocks: (a) second iteration, (b) third iteration, and (c) fifth iteration.

the resonator lines and the shunt capacitor to obtain the result shown in Figure 5.81(b). The different conversion approach resulted in slightly different topology. The first approach resulted in the topology shown in Figure 5.82(a), and the second approach resulted in the topology in Figure 5.82(b).

The conversion time using the second alternative is much shorter compared with the first approach and it works well for circuits with reduced number of elements. In circuits containing a larger number of variables, it may be difficult to localize the source of differences in the circuit. In these cases, it is best to start with the first approach, described above, in spite of the longer design time involved.



**Figure 5.81** Drain impedances in rectangular form. All three port impedances are superposed: (a) impedance at the fifth iteration, and (b) impedance for the final circuit.



**Figure 5.82** Drain impedances in rectangular form: (a) first conversion approach, and (b) second conversion approach.

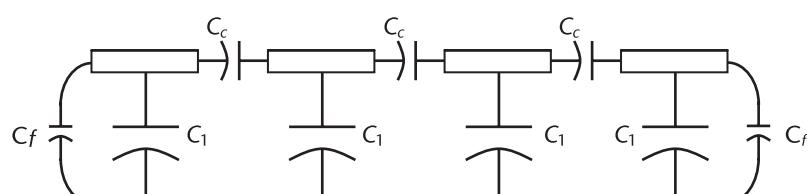
### 5.8.2 Shunt Capacitors

The advantages of using lumped shunt capacitors on the electrical performance have already been demonstrated. However, it is the EM analysis that will test its feasibility. As already discussed, if the size of the capacitor plates is a multiple of the grid size, it will help layout design and the EM solver simulation. If we use the proposed grid size of  $1 \times 1 \mu\text{m}^2$ , the capacitor dimensions become integer in the range of microns. Smaller grid size requires computers with larger memory to obtain a solution. In general, for high millimeter-wave frequencies, the capacitor sizes are limited to a minimum of  $10 \times 10 \mu\text{m}^2$ , but ultimately, their size is determined by the foundry design rule. If smaller capacitors are needed, the use of open stubs is a good alternative. One may also consider modifying the circuit by moving the capacitor to a location where a larger value can meet the circuit and design rules.

### 5.8.3 Fringing Capacitance

Let us discuss the fringe fields from large-width transmission lines. Figure 5.83 represents the cross-section of four coupled transmission lines, where one can notice the internal plates have lower capacitance to ground, also called even-mode capacitance. The capacitance between the plates, also called odd-mode capacitance, does not contribute to the even-mode impedance. The drawing also shows that the even-mode capacitance of the external plates are higher due to the fringe fields adding up to the capacitance. This is not critical for three-way or less combiners, but it becomes a problem for four-way and higher combiners. A solution to balance the capacitances is to decrease the width of the external plates to decrease the value of  $C_1$  towards  $C_{10}$ , making the external capacitance equal to  $C_{10} = C_1 - C_f$ . The amount of reduction is made by carefully trimming the width of the external plates while simultaneously checking the transmission coefficients of the structure. That means iteratively making EM simulations of the circuit.

Therefore, when we parallel three or more circuits with significant coupling to each other, it will result in less capacitance to ground compared to a single block. Another action to consider is when we parallel two halves of a circuit block. The center plates that have a capacitance  $C_{10}$  must have the dimension modified to be back equal to the  $C_1$  value to account for the symmetry of the structure. In case there is a need to eliminate the chamfer from the center plates and attach them physically, there is an additional capacitance added to ground in the circuit. That requires changing the plate dimension. Usually, the EE model of the circuit must be available to optimize these effects.



**Figure 5.83** Fringing capacitance in multiple coupled microstrip lines.

#### 5.8.4 EE to EM Conversion of 6:1 Circuits

The OMN 6:1 combiner for case study 2 can be generated by paralleling the EE circuit contained in Figure 5.36 and converting to its corresponding EM. That means to go over all phases of the step-by-step process. An alternative to skip this lengthy process is to connect the two 3:1 EM blocks together and work only in the EM layout. After joining the two halves, we made the changes in the center plates as discussed above in the fringing capacitance section (Section 5.8.3). The width of all plates are now similar except for the ones at the edges.

The layout for the 6:1 combiner is shown in Figure 5.84(a). After a few iterations of EM analysis to obtain the same response obtained by a single 3:1 combiner, we obtained the impedances shown in Figure 5.84(b). The performance is adequate for application in real circuits. The reactance is reasonably flat, which means that it is partially compensated. A remainder on the EM simulation time for the a 6:1 combiner. It has more S-parameter ports and more vias, so the simulation time is longer compared to the time to simulate a 3:1 combiner.

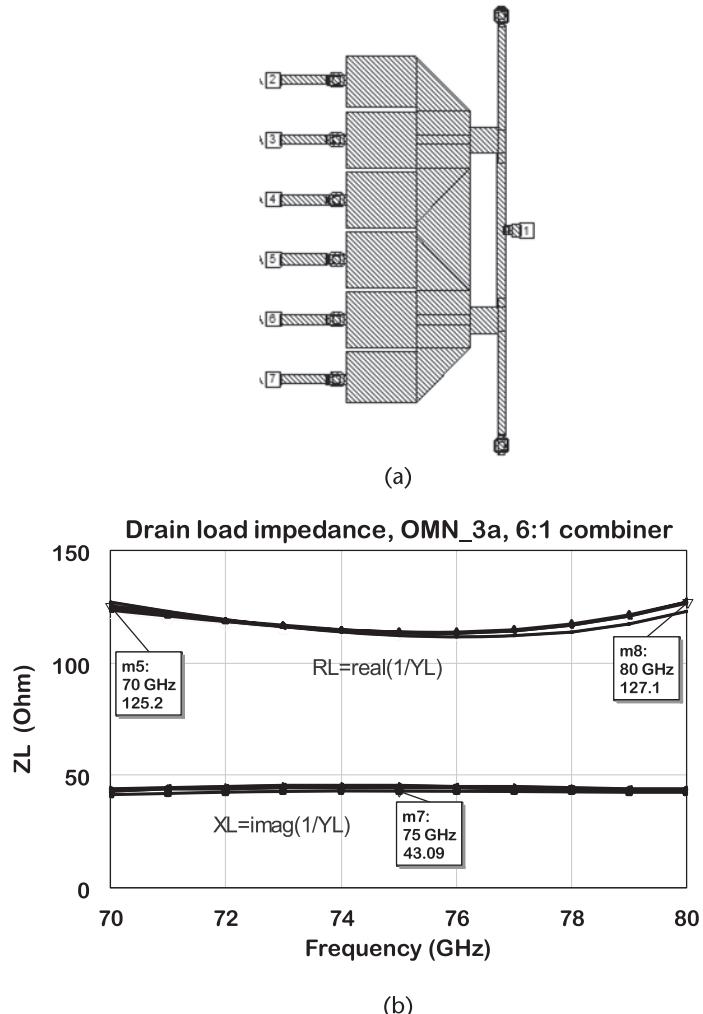
The balance of this power combiner in terms of insertion loss and insertion phase is obtained from the test bench shown in Figure 5.72. The drain model used is  $R_d = 150\Omega$ ,  $C_d = 40 \text{ fF}$ , and  $L_d = 12 \text{ pH}$ . One can observe the amplitude balance between the ports in the insertion loss plots shown in Figure 5.85(a). The ohmic losses were obtained by tying all six ports and calculating the MAG. The ohmic loss is in the same figure and shows a value of 0.87 dB. The dotted curve represents the ideal 6:1 coupler, corresponding to 7.8 dB. The total measured loss matches the sum of ideal plus coupling losses. The phase in Figure 5.85(b) shows a difference of  $3.5^\circ$  over the band.

For the sake of comparison, let us evaluate the circuit block OMN\_3b that does not use shunt capacitors, represented in Figure 5.86(a), and compare it with OMN\_3a in Figure 5.84(a). The impedance performance for option (b), obtained from EM analysis, is presented in Figure 5.86(b). The real part of the impedance shows a range from  $117\Omega$  to  $120.5\Omega$ . The reactive impedance ranges from  $j48\Omega$  to  $j51\Omega$  and shows a positive slope, which means there is no reactance compensation.

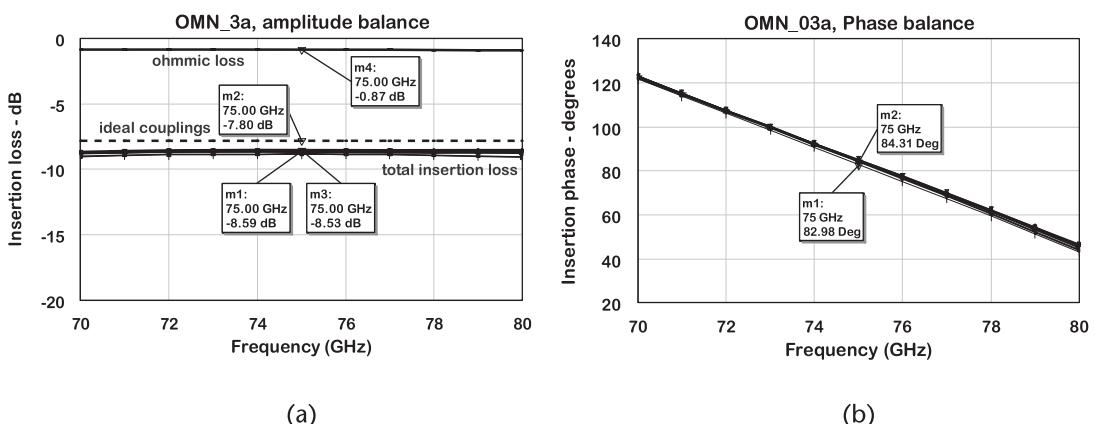
The balance simulation results for this OMN circuit block is in Figure 5.87. The circuit shows about 0.2-dB lower ohmic losses compared with option (b). The total loss is in agreement with the ohmic and coupling losses. Both circuits will deliver similar results with a potential wider band for power with option 3a. The phase balance for both options is similar.

#### 5.8.5 EM Conversion of 2:6 Circuits

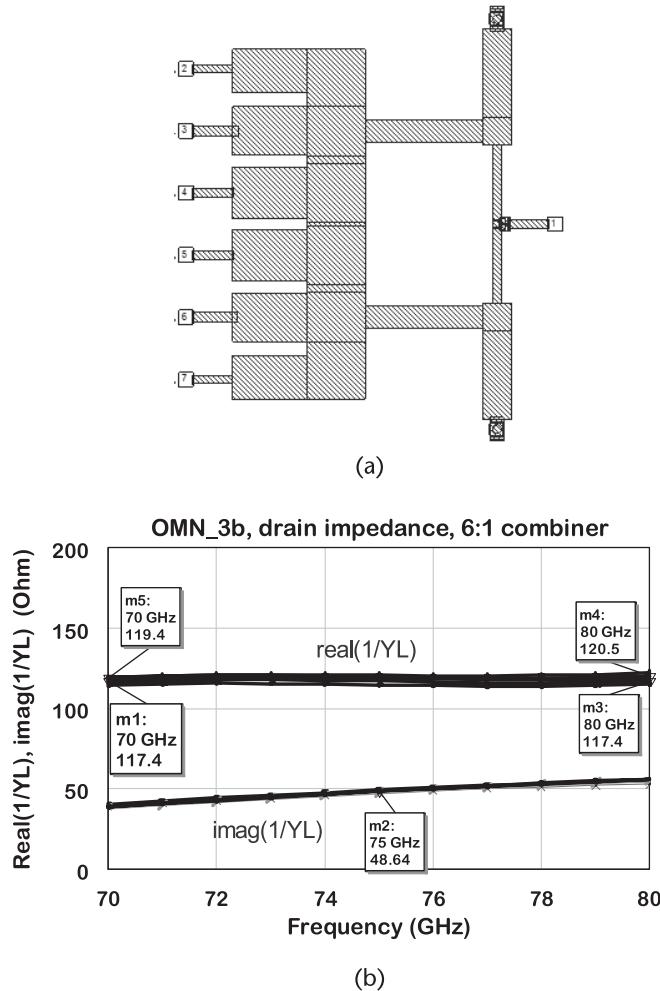
An additional example of EM conversion is for a 2:6 transformer/divider ISMN2 circuit block. The procedure is similar to the one employed in the OMN EM modeling. The 2:6 divider EM layout was constructed by paralleling two ISMN2 3a 1:3 circuit blocks. The microstrip lines at the center were modified, so that the internal ports have similar dimensions. The EE layout for this circuit block, shown in Figure 5.54, is reproduced in Figure 5.88(a). The EM layout for the same circuit including bias filters, and stabilizing resistors are shown in Figure 5.88(b).



**Figure 5.84** OMN\_3a combiner layout and corresponding impedance: (a) 6:1 combiner layout, and (b) EM 6:1 combiner impedance.



**Figure 5.85** Balancing between the OMN\_3a ports: (a) Magnitude of insertion loss, and (b) magnitude of insertion phase.

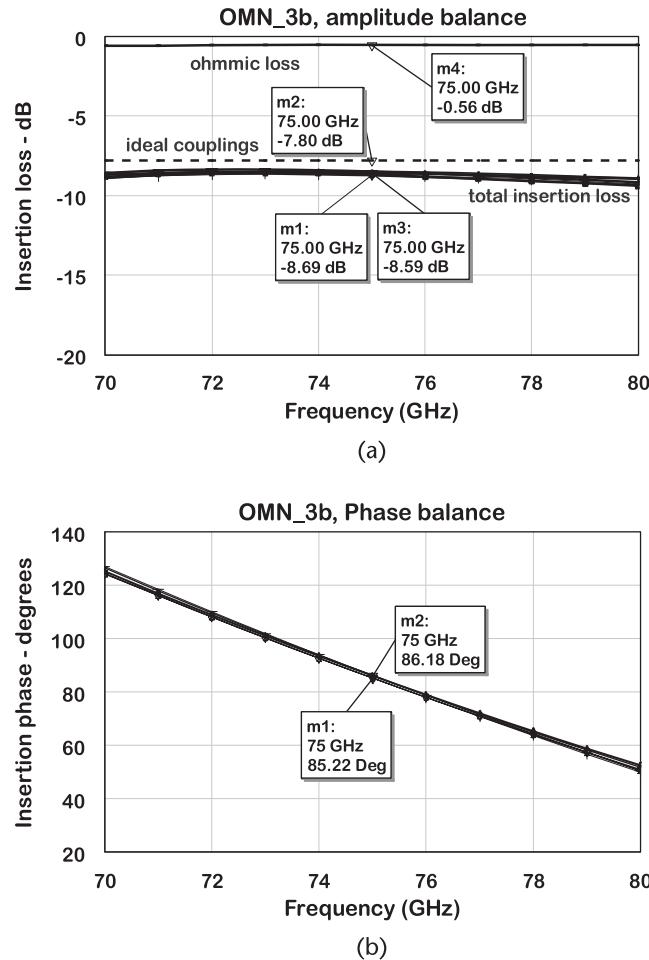


**Figure 5.86** OMN\_3b combiner layout and corresponding impedance: (a) 6:1 combiner layout, and (b) 6:1 EM combiner impedance.

The general shape of both layouts is the same, but it is observed that dimensions for the gate access lines are different. This was a requirement to make  $S_{EM}$  match  $S_{EE}$ . The short stubs were paralleled to avoid using a single stub with short electrical length and larger width. That also helps improve performance. Notice that the short stubs are offset from the center to avoid layout conflict due to the connection of two 1:3 dividers.

The source impedance performance at the gate ports for the EM circuit is shown in Figure 5.89(a). All 6 output ports are represented and they fall close to each other. One can see that there are two major traces: one for the real part, from  $5.0\Omega$  to  $7.3\Omega$ , and another for the imaginary part,  $j13.3$  to  $j15\Omega$ .

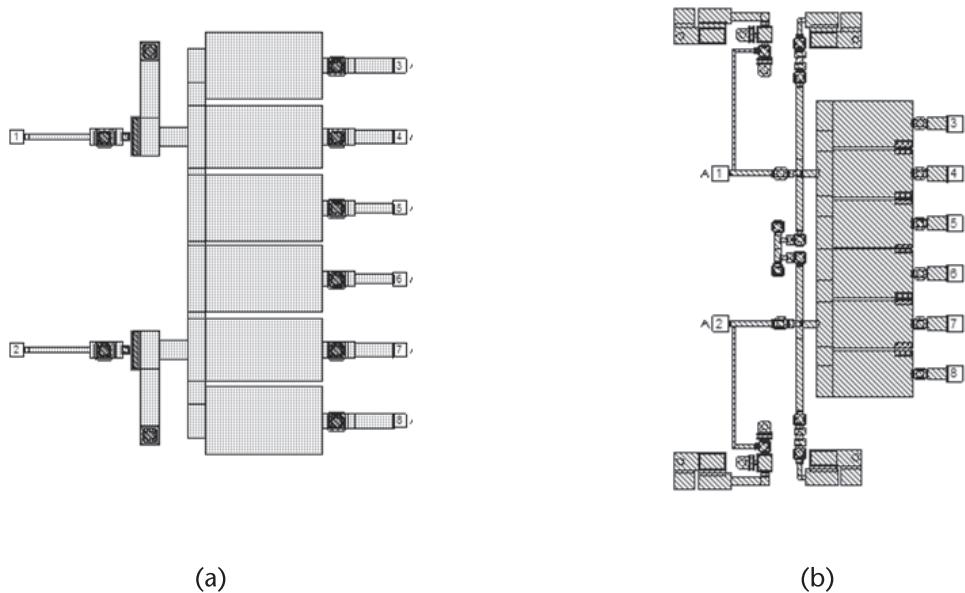
The drain load impedance in both ports is shown in Figure 5.89(b). The real part has a minimum of  $143\Omega$  from 72 to 78 GHz. It increases to  $170\Omega$  at the edges of the band. That may cause a power variation of 0.9 dB at the band edge.



**Figure 5.87** Balancing between the OMN\_3b ports: (a) magnitude of insertion loss, and (b) magnitude of insertion phase.

### 5.8.6 Fine-Tuning the EM Circuit Block

After the EM conversion of all blocks are finished, they do not necessarily represent an exact replica of its corresponding EE block. They do not need to be, as long as the simulation of the complete amplifier shows that it meets the requirements. In certain cases, it can be better than the original EE, but in case they are off by a small amount, there is a quick way to correct. Insert a transmission line between the gate and input circuit and drain circuit with the same impedance as the line on the EM block. Then allow its variation within, say,  $-10$  to  $+10 \mu\text{m}$  and run the optimizer. For positive signs, increase the length of the series line within the EM block and redo the EM. For negative signs, decrease the length of that line. In certain cases, the first element is a shunt element where this does not apply. In these cases, the EM block needs to be modified.

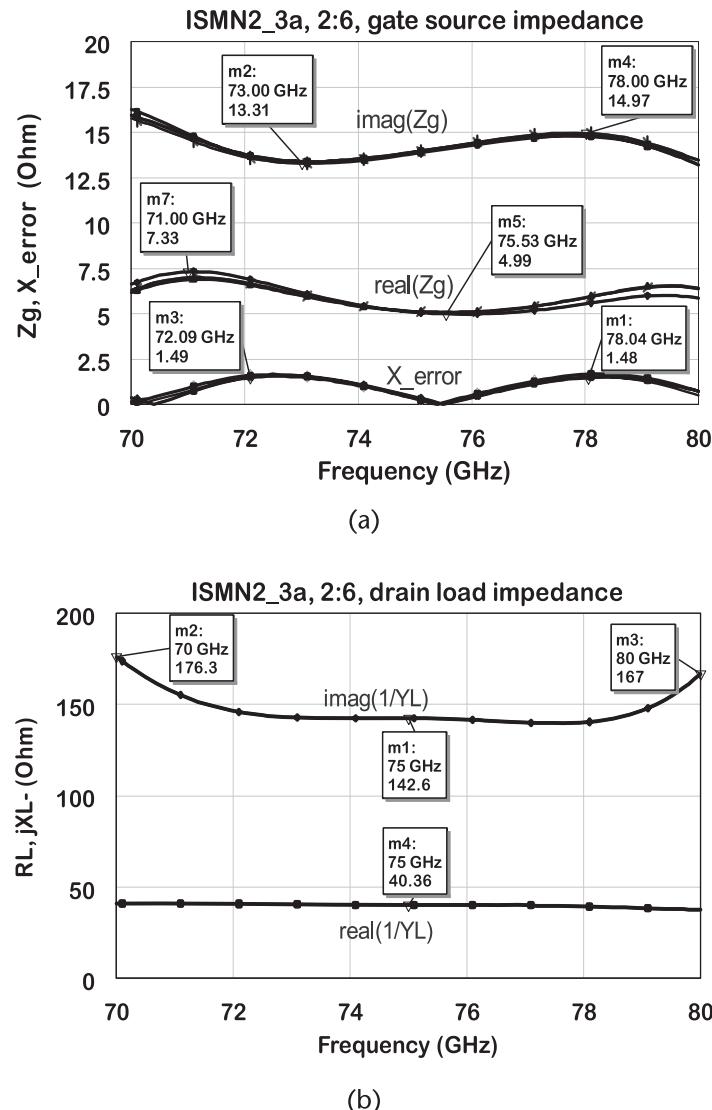


**Figure 5.88** ISMN2\_3a EE and EM layouts: (a) 2:6 divider EE layout, and (b) 2:6 divider EM layout with bias filters.

### 5.8.7 Large-Width Transmission Lines

In order to illustrate the possibility of using wider transmission lines, let us assume that we are using 0.18- $\mu\text{m}$  gate length technology on a 100- $\mu\text{m}$ -thick substrate for operation at 30 GHz. Let us also assume a power density of 3.5 W/mm at a drain voltage of 28V. Thus, a unit cell with  $8 \times 75$ - $\mu\text{m}$  fingers can deliver 2W of power. With higher drain voltage, the optimum drain resistance for power will be higher compared to lower drain bias technologies, which means that it is possible to reduce losses in the output circuit. However, there is no advantage on the gate side, where gate resistance can be very small. We have already seen in previous case studies that this means a demand for low characteristic impedance lines.

To overcome the line width limitation, let us first group the unit cells in a group of two devices sharing a common via. Then we offset the device connection from the transmission-line center to a point close to the edge where the drain-to-drain pitch is not violated. The EE schematic and corresponding layout are shown in Figure 5.90(a). The EE assumes that the connections to the large-width lines are at the center. One can see in the layout of Figure 5.90(b) that the gate connections are off-center. The differences between are corrected by modifying the line dimensions per the results of EM analysis.



**Figure 5.89** ISMN2\_3a 2:6 impedance results: (a) 2:6 divider EM gate impedance, and (b) 2:6 divider EM drain impedance.

The matching required a line of  $25\Omega$  corresponding to a width of  $313\ \mu\text{m}$  in this technology. The gate side uses a short resonator series line and a low-impedance, quarter-wave-long line. On the drain side, a series and parallel line is used to resonate the drain to a low  $R_T$ . The two circuits are tied and a quarter-wave-long transmission line is used to match the impedance of the joining point to the output termination.

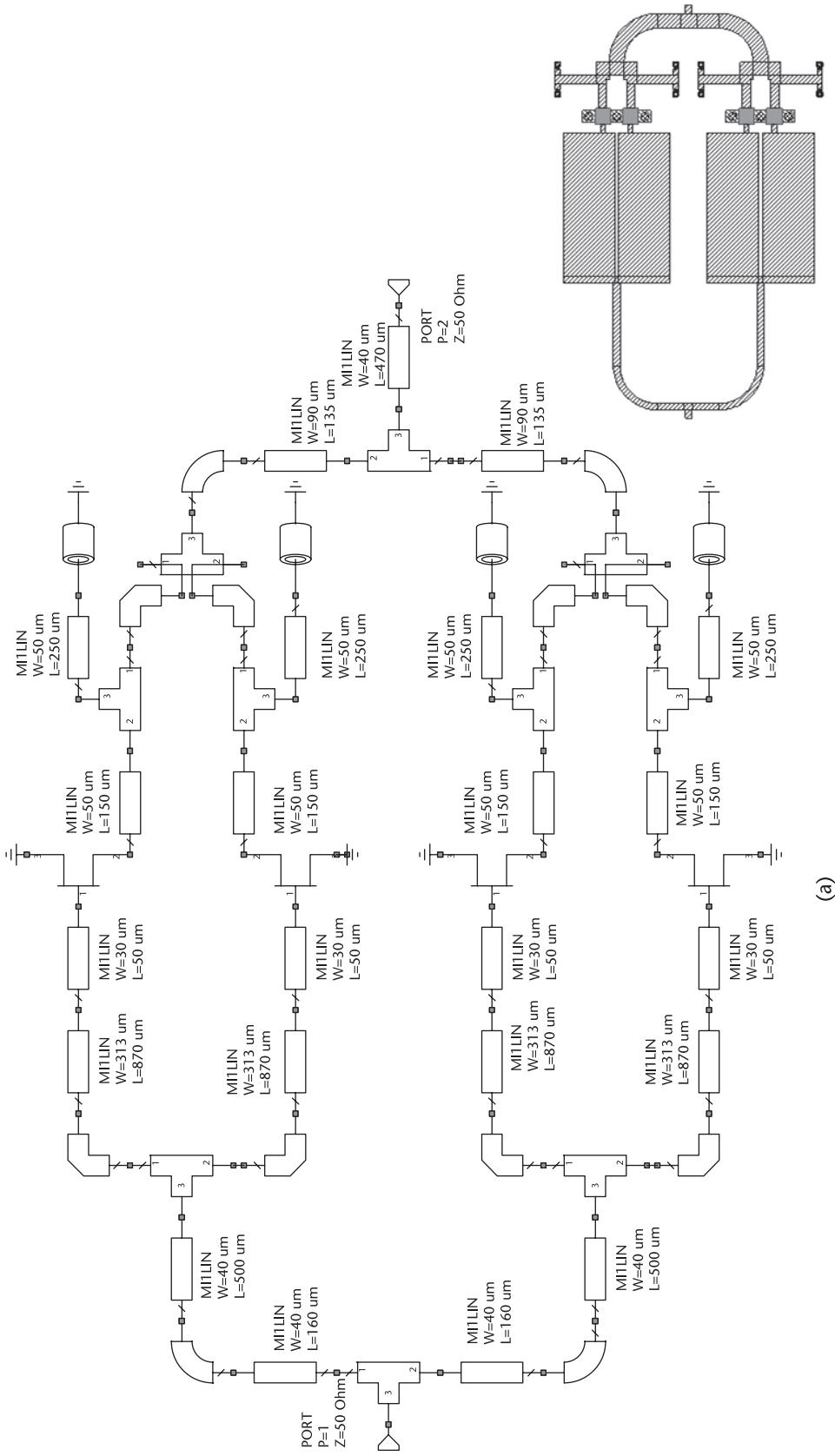


Figure 5.90 The solution for large-width transmission-line Ka-band: (a) microstrip schematic for output stage, and (b) corresponding layout.

## 5.9 Multistage Stability Analysis

Stability is an important property of an amplifier. MMIC amplifiers are meant to be unconditionally stable, which implies that the real parts of input and output impedances of the circuit remain positive for all passive load and source terminating impedances. There are two phases where it is important to check the stability and stabilize the amplifier if that is the case. In the initial phase of the design, the stability of the unit cells need to be verified. If the circuit is unstable in the band, the unit cell needs to be stabilized before proceeding with the design. The next important design phase where stability is mandatory is just after the EM version of the amplifier is completed. The reason is that the circuit losses are better defined and if the circuit is still marginally stable, it has to be modified to guarantee unconditional stability. Obviously, during the design steps, the stability must be checked every time the complete amplifier is modified. In order to verify the amplifier stability, we use the procedures described in this section.

### 5.9.1 K-Factor and $\mu$ -Factor

The most traditional method of testing stability is the  $K$ -factor, using (2.15) and (2.18). In general, the  $K$ -factor alone is used to determine stability, but the correct way requires calculation of the parameters  $D$  or  $B_1$  as well. A more simple condition is provided by the  $\mu$ -factor expressed by (2.15). There is actually an  $\mu_1$  factor for the input side and an  $\mu_2$  factor for the output side. As far as determining the  $f_k$  frequency, either  $\mu_1$  or  $\mu_2$  provides the same frequency. These formulations are great to guarantee the stability of single-stage amplifiers. It is also valid for the multistage as a necessary but not sufficient condition. For instance, if there is an indication of  $\mu < 1$  within the band, it does not tell you which device is responsible for the instability. However, in power amplifiers, it is common to parallel devices in order to get more power and that creates internal loops. Those loops are not considered by the  $K$ -factors or  $\mu$ -factors.

### 5.9.2 Loop Stability

This type of stability test, also called internal stability, can be verified by inserting a stability test probe in series with the gate and the drain of each active device in an amplifier circuit. These probes consist of ideal dual directional couplers used to collect incident and reflected waves to and from the device nodes. They do not interfere with the normal amplification process, as they use a very small sampling resistor, and provide a good insight about the impedance behavior inside the amplifier. They are now available in most commercial microwave software packages. With such measurements, we have at each port a pair of reflection coefficients,  $G_g$  and  $G_d$  from the gate and the drain, respectively. If they obey the condition (5.12), then there is no negative impedance within the loops and the circuit is stable. The loop stability condition can also be determined by checking the product and the phase of the reflection coefficients, (5.13). Its modulus has to be lower than 1 and its phase must be far from  $0^\circ$  or  $360^\circ$ . These are the limits of unstable to stable circuit operation.

$$\Gamma_g < 1 \text{ and } \Gamma_d < 1 \text{ or } \operatorname{Re}(Zg) > 0 \text{ and } \operatorname{Re}(Zd) > 0 \quad (5.12)$$

$$|\Gamma_g \Gamma_d| < 1 \text{ and phase } (\Gamma g) + \text{phase } (\Gamma d) \neq 0, 2\pi \quad (5.13)$$

Equation (5.13) defines the stability index, which can be easily represented in a rectangular plot as a function of frequency. The advantage of this process is that it can be applied to the design file S-parameters and show exactly which area needs stabilization. The same condition in terms of admittance and impedance are expressed by (5.14) and (5.15).

$$Y_d + Y_g > 0 \quad (5.14)$$

$$Z_d + Z_g > 0 \quad (5.15)$$

Figure 5.91 illustrates a three-stage amplifier containing 9 unit cells, each requiring two testing probes. In principle, 18 stability simulations are needed to cover all possibilities. A first simulation is made with  $50\Omega$  at the input and output ports. Once the instability spots are detected and the circuit is stabilized, a second simulation is needed, removing the  $50\Omega$  terminations and replacing them with variable tuners at the source and at the load terminals.

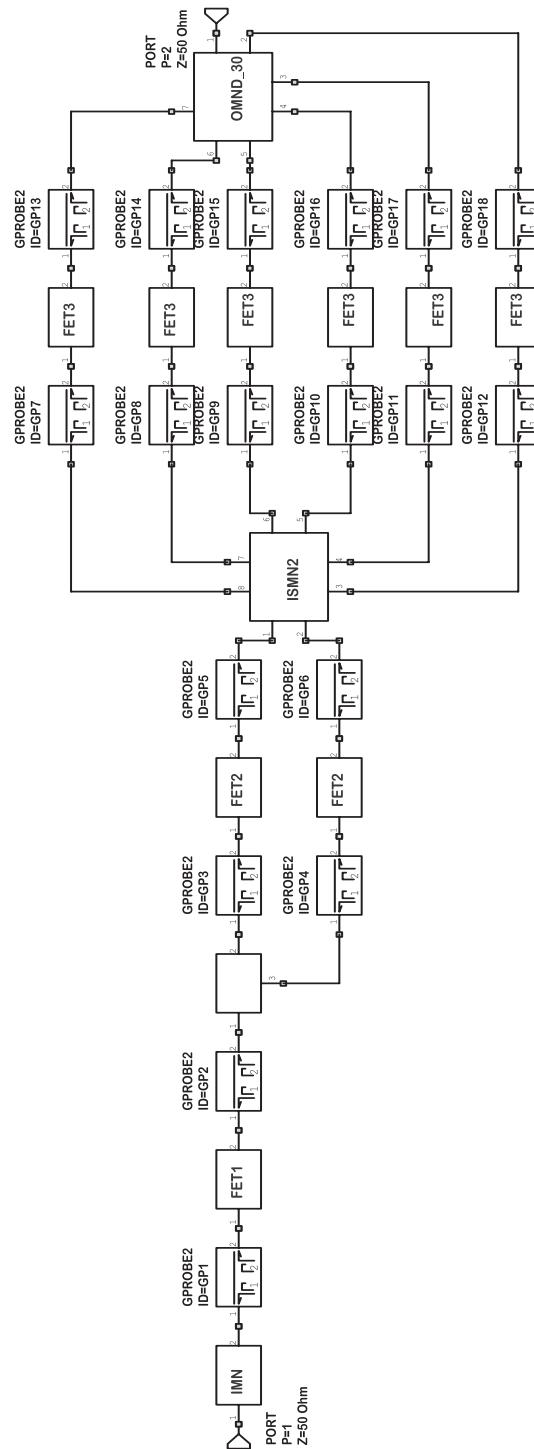
The loop stability is obtained with input and output terminated in the standard  $50\text{-W}$  impedance. In order to verify the stability when the output terminations are different, this circuit is inserted in between two tuners, represented in Figure 5.92, available in Cadence\_AWR and reproduced under license. The tuners are set with a magnitude of 0.99 and the phase is changed from  $0^\circ$  to  $360^\circ$  with a certain number of steps.

The phase increment description is included in the “Global Definitions” file contained in the Cadence AWR simulator. The verification bandwidth is from a low frequency, say, 1 GHz, to the  $f_{\text{MAX}}$  of the device. The term *stability index* is defined by (5.13), considering only its magnitude. If the stability index is less than 1 for all input and output terminations, the circuit is stable.

### 5.9.3 Odd-Mode Stability

This is a necessary stability test to be made in any circuit containing parallel unit cell devices, forming multiple loops inside the amplifier. Even though the loop stability can detect problems occurring around a loop, it does not detect the odd mode. In such a test, a pair of nodes is connected to a balun transformer, in the manner shown in Figure 5.93.

Excitation is applied and if there is a negative resistance detected, it will show up in the reflected signal. The solution to avoid this unwanted mode of operation is to introduce a lossy element between the two gates and/or between the two drains.



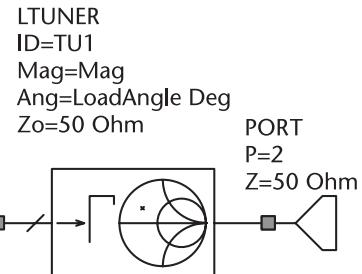
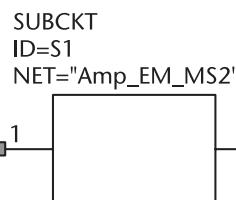
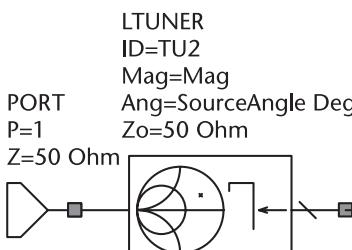
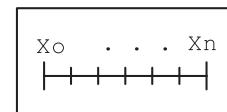
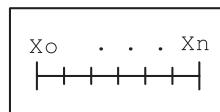
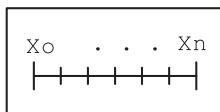
**Figure 5.91** Test probe for checking loop stability.

SWPVAR  
ID=Mag1  
VarName="Mag"  
Values={0,0.9}

Mag=0.99  
SourceAngle=0  
LoadAngle=0

SWPVAR  
ID=SourceAngle1  
VarName="SourceAngle"  
Values=AngSweep

SWPVAR  
ID=LoadAngle1  
VarName="LoadAngle"  
Values=AngSweep

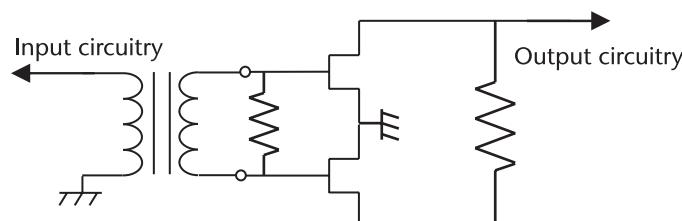


**Figure 5.92** Test bench for internal stability test by Cadence AWR.

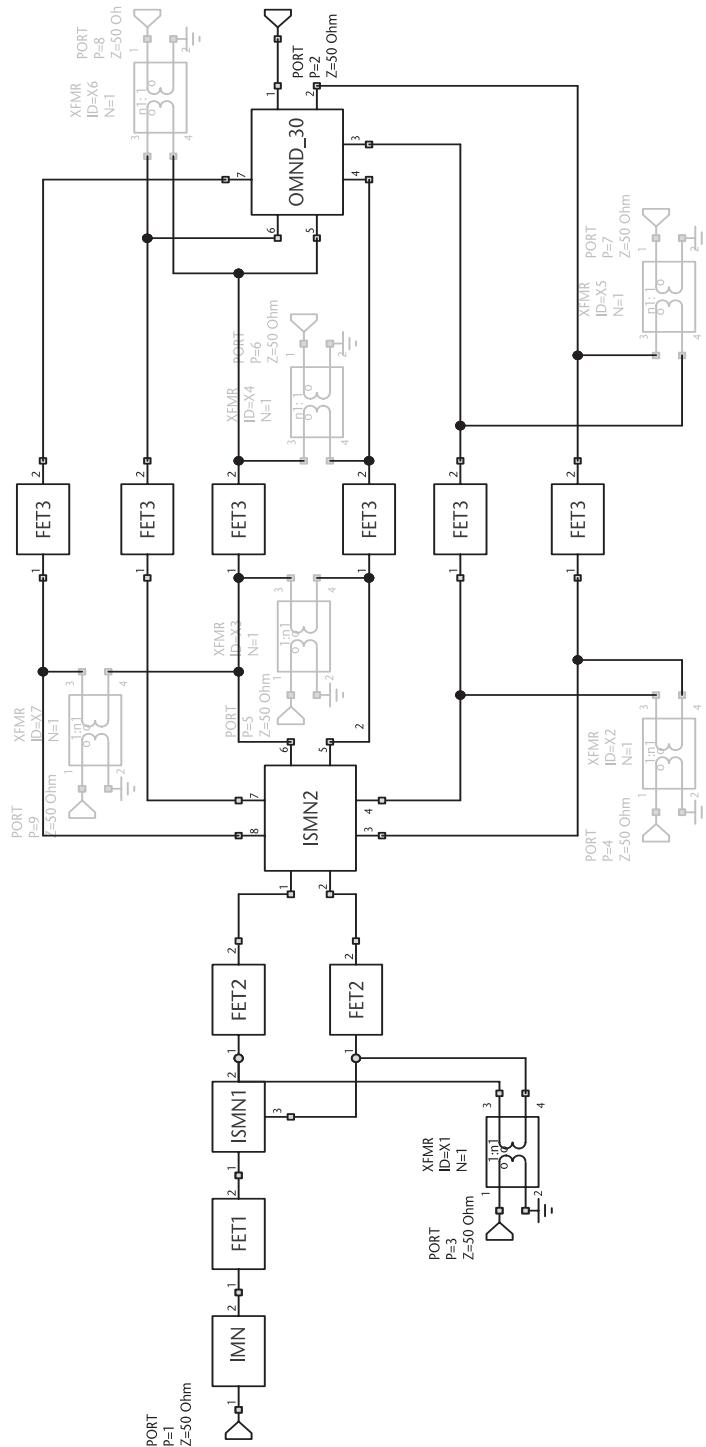
They will not interfere with the normal even-mode operation, but will load signals with a tendency to generate positive feedback. The amplifier block diagram of Figure 5.94 shows the presence of 7 possible loops that can create odd-mode instability. There are more 6 loops considering the nonadjacent devices in the output circuit, not shown in the figure. It also highlights the connection of only one ideal transformer to analyze the stability of the loop 1 gate. The other transformers are disabled.

#### 5.9.4 MMIC Stability Example

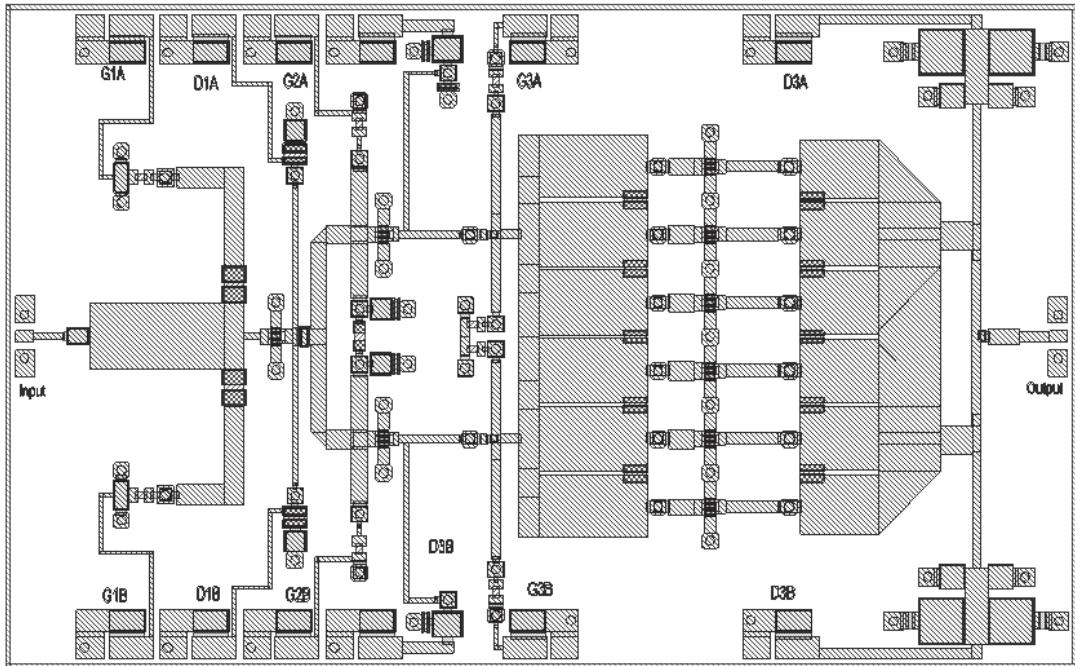
The circuits, in general, show a stable or near stable operation in band. If there are in-band stability issues, they are solved by stabilizing the unit cells or group of unit cells. Out-of-band stability, in particular, at lower frequencies, is determined by out-of-band terminations controlled by the bias filters. That specific topic is addressed in Appendix A. We selected an example amplifier, using blocks discussed in previous sections and represented by the schematic of Figure 5.91. The corresponding layout is shown in Figure 5.95, where all stabilizing resistors and filters are included.



**Figure 5.93** Odd-mode stability measurement and loading.



**Figure 5.94** Measurement of the odd-mode stability with a transformer.



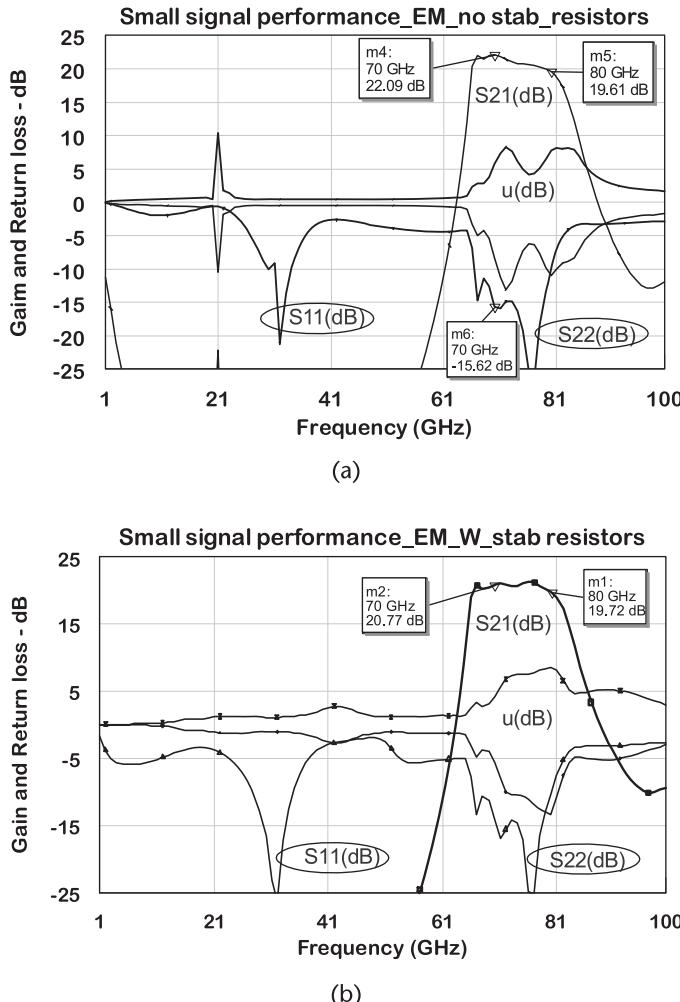
**Figure 5.95** Example of a three-stage amplifier for the 70 to 80-GHz band. Die size =  $2.4 \times 1.5 \text{ mm}^2$ .

The resistors at the edge of large-width transformers not only suppress odd-mode instabilities but also suppress unwanted propagation modes. The capacitors used for shorting the shunt stubs to the ground are self-resonant at the center frequency. The remaining bias filters provide in-band isolation and lower-frequency termination for the devices.

In Figure 5.96(a), we verify the circuit  $\mu$ -factor stability over the band from 1 to 100 GHz for the circuit in Figure 5.90 with no stabilizing resistors. The circuit is stable for most frequencies, except for a negative peak on the output return loss at 21 GHz. The simulation of the  $\mu$ -factor in Figure 5.96(b) is for the same circuit with stabilizing resistors. The peak disappeared and the performance is quite similar. In band, there is an improvement on the input and output return loss.

The second test is the loop instability test. Instead of showing the stability of each one of the loops, we selected only the two most representative. Initially, the test does not include the stabilizing resistors and biasing networks. Figure 5.97(a) shows the stability with the probes at the gate and drain of the second stage. The test was made with the amplifier terminated with a  $50\Omega$  resistor. One can observe  $\Gamma < 1$  for most of the band, except for the interval 14.7 to 25 GHz. Both gate and drain show a negative resistance within that frequency range. The point that goes out of the unit circle is not far from phase 0. This means that the circuit can become unstable depending on process variations and temperature.

The next test corresponds to the application of a loop test probe to one of the 6 gates and another to one of the 6 drains of the third stage. For this stage, there are four frequencies where it is indicated that  $\Gamma > 1$ , namely at 8.6, 28.6, 30.1, and 62.6 GHz. It is more convenient to look first in the stability index, as shown



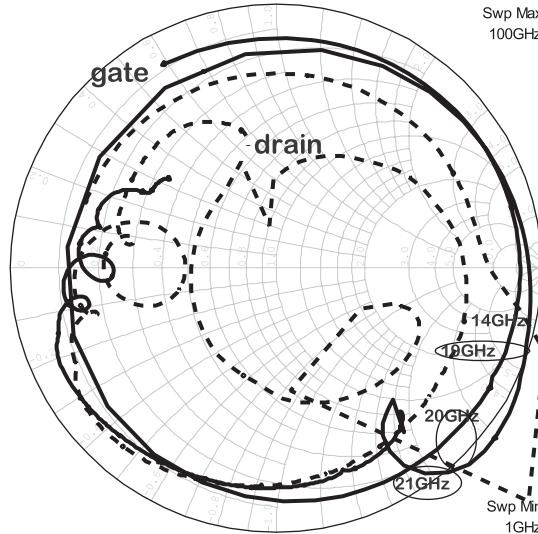
**Figure 5.96** Example of a three-stage amplifier for the mid-W-band: (a) stability for layout without stabilizing resistors, and (b) stability for layout with stabilizing resistors.

in Figure 5.97(b) corresponding to the product of  $\Gamma_1 \times \Gamma_2$  in magnitude only in a rectangular plot. Then, in a second analysis, look in the Smith chart for the loop stability around the frequencies where the circuit is unstable.

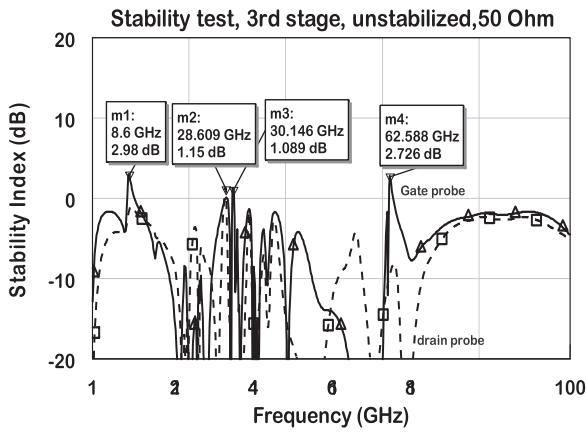
In the next verification, all the stabilizing resistors, filters, and bias networks in Figure 5.91 were included in the stability simulations. In this test, the source and load magnitudes are equal to 0.99 with phases changing with  $20^\circ$  steps between  $0^\circ$  and  $360^\circ$ . The plots in Figures 5.98(a, b) show the second and third stages stable under  $50\Omega$  terminations and under the load with  $VSWR = 0.99$  all phases. One can clearly see that the circuit is now completely stable, as all the curves are contained within a radius lower than 1.

The odd-mode oscillation was checked for all eight loops in the circuit of Figure 5.93. The first loop showed no instabilities. The transformer probed the stage-3 gate and the results are shown in Figure 5.99(a), depicted by a solid line for one specific set of gate and drain. Between 28.5 and 29.7 GHz, it shows  $G > 1$ . With

Probes at 2nd stage. Unstabilized, Term = 50 Ohm



(a)



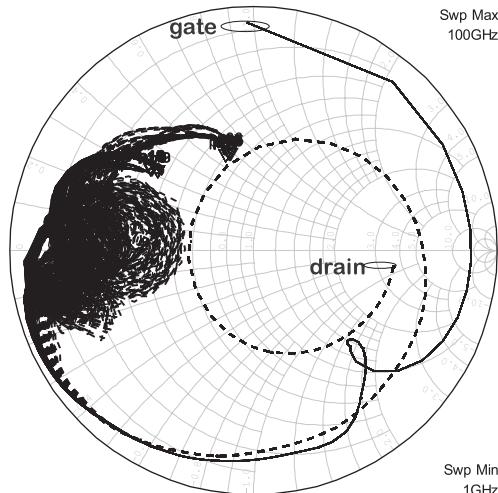
(b)

**Figure 5.97** Loop stability test with no stabilization resistors: (a) stability with probes at second stage, and (b) stability index with probes at third stage.

the stabilizing resistors, all of the circuit is stable indicated by the dotted line. The probing of the odd mode, on the drain side in Figure 5.99(b), showed an unstable area at 28 GHz. The curves with stabilizing resistors indicate stable operation. This particular test is not sensitive to source and load terminations. This is to be expected, as the tests are performed in the odd mode and the source/load terminations are in the even mode.

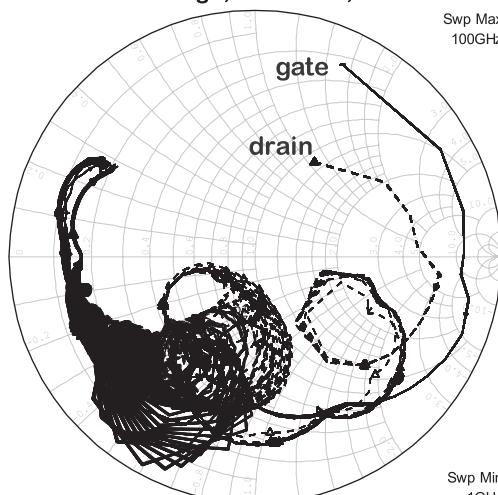
A final note on stability is the coupling between the circuit blocks. They are usually located with respect to each other by a distance greater than the substrate height. The circuit blocks below are within this distance with a certain margin. The circuit in Figure 5.100 is prepared for the EM analysis of the complete amplifier.

Probes at 2nd stage, stabilized, Term = tuner



(a)

Probes at 3rd stage, stabilized, Term = tuner

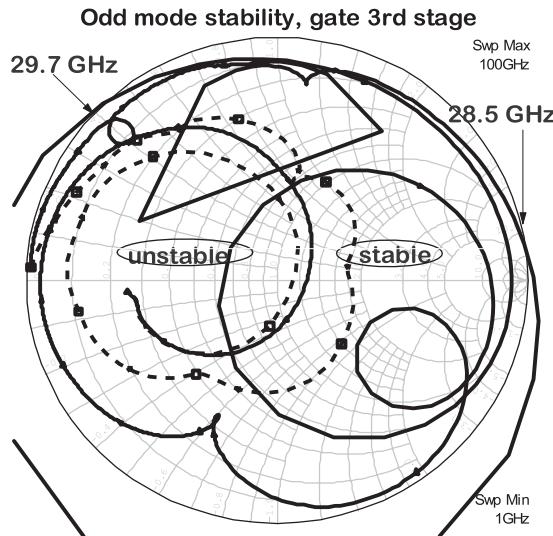


(b)

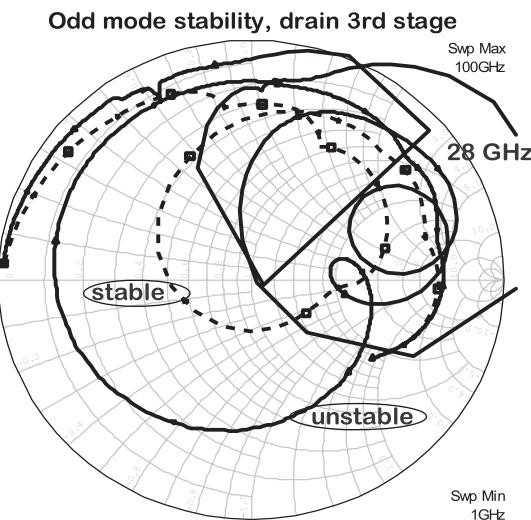
**Figure 5.98** Loop stability test with tuner, stabilized circuit: (a) probes at second stage, and (b) probes at third stage.

It contains 20 ports and takes about 1 day to simulate, depending on the type of computer used. What has been observed is a slight shift down in frequency response.

The shift is around 100 MHz, easily considered within the guard band of the design. Therefore, for an amplifier where all the biases are decoupled externally with wire bonds and a 100-pF parallel plate capacitor, this long simulation test is not necessary. However, a trend in the market is to have fewer external bias connections. That forces the designers to build bias networks on the chip derived from the output stage main bias. In that case, this simulation is mandatory to be sure that the circuit is oscillation-free.

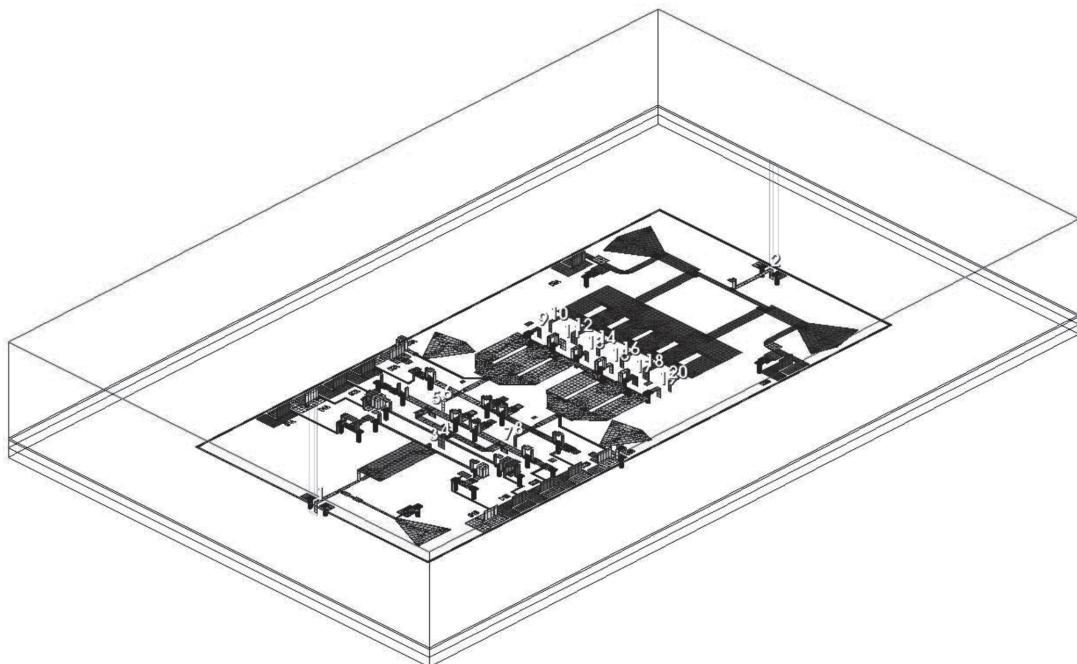


(a)



(b)

**Figure 5.99** Odd-mode stability check on the gate and drain: (a) probes at gate of third stage, and (b) probes at drain of third stage.



**Figure 5.100** Layout of a complete amplifier prepared for a full EM analysis.

## References

- [1] Rauscher, C., “Large-Signal Technique for Designing Single-Frequency and Voltage-Controlled GaAs FETs Oscillators,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 29, No. 4, April 1981, pp. 293–304.
- [2] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 290.
- [3] Darwish, A. M., et al., “Improved Linearity of Power Amplifier GaN MMIC for Ka-Band SATCOM,” *IMS2012 International Microwave Symposium Digest*, 2012.
- [4] Lozhkin, A. N., T. Maniwa, and, M. Shimizu, “RF Front-End Architecture for 5G,” *2018 IEEE 29th Annual International Symposium on Personal, Indoor, and Mobile Radio Communications*, 2018.
- [5] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 62.
- [6] Crosman, A. M., and S. A. Maas, “Minimization of Intermodulation in GaAs MESFET Small Signal Amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 37, No. 9, September 1989, pp. 1411–1417.
- [7] Giofre, R., P. Colantonio, and F. Giannini, “A Design Approach for Two Stages GaN MMIC PAs with High Efficiency and Excellent Linearity,” *IEEE Microwave and Wireless Components Letters*, Vol. 26, No. 1, January 2016, pp. 46–48.
- [8] Pedro, J. C., and N. N. Carvalho, *Intermodulation Distortion in Microwave and Wireless Circuits*, Norwood, MA: Artech House, 2003, p. 351.

- [9] 3GPP A Global Initiative, “3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; Base Station (BS) Radio Transmission and Reception (Release 12 and 15),” May 2019.
- [10] Schellmann, M., et al., “FMC-Based Air Interface for 5G Mobile Challenges and Proposed Solutions,” *2014 9th International Conference on Cognitive Radio Oriented Wireless Networks*, 2014.
- [11] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, p. 309.

# State-of-the-Art MMIC Amplifiers

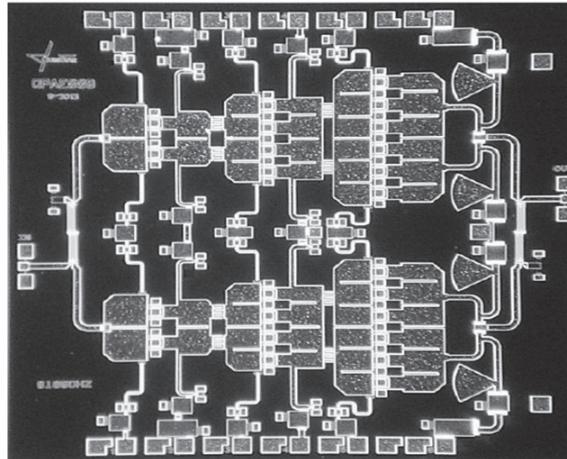
The objective of this chapter is to present a survey of recent publications on amplifiers operating at millimeter-wave frequencies that achieved a high degree of performance. They are considered to be state-of-the-art, for a particular achievement, at the time of publication. For power amplifiers, we can mention the following achievements as of interest for the state of the art: maximum peak power, PAE, frequency of operation, frequency bandwidth, and chip dimensions. We also selected publications where the design techniques confirm the validity of the methodologies discussed in previous chapters.

## 6.1 E-Band Amplifier

The first publication to be addressed is on an E-band amplifier, reported in 2014, as a state-of-the-art MMIC relative to saturated output power. It was designed on a 0.1- $\mu\text{m}$  GaAs pHEMT technology by WIN Semiconductors [1]. This process exhibits devices with  $f_T$  and  $f_{\text{MAX}}$  equal to 100 and 220 GHz, respectively. Its power density capability is 0.45 W/mm, with a small signal gain of 9 dB at 85 GHz.

The MMIC chip is shown in Figure 6.1 and measures  $3 \times 3 \text{ mm}^2$ . It is a balanced structure where the single-ended amplifier counts 6 output devices, each measuring 200  $\mu\text{m}$ , for a total periphery of 1,200  $\mu\text{m}$ . The MMIC contains two amplifiers combined with Lange couplers. The single-ended amplifier can be further divided into two halves by a line of symmetry that separates the top and bottom parts. Three amplification stages were designed with the following lineup, 2:4:6, and that makes a ratio of 1.5 between the driver and output stages. The OMN is a 3:1 transformer/combiner with a series resonance line, a cascade of two quarter-wave transformers, and a shunt stub. The ISMN2 follows a similar methodology. The three gate impedances are combined to an  $R_{\text{ref}}$ , and then two drain impedances are combined to the same  $R_{\text{ref}}$ . A capacitive inverter was employed to join both circuits. Instead of using a small lumped capacitor, we decided to use an interdigital capacitor. That approach avoids concentration of fields on a small area capacitor. The interdigital model from Figure 2.21 was used to generate the initial EE model, which was corrected by EM analysis, before inserting in the ISMN2 circuit block. The ISMN1 circuit block was designed following a similar approach. The IMN consists of a gate resonator, and a simple quarter wave transformer.

The single-ended S-parameters for this design are presented in Figure 6.2(a). A minimum gain of 17.6 dB was measured within the bandwidth from 81 to 86 GHz and matches the simulation. One can also observe a shift down in the measured



**Figure 6.1** State-of-the-art E-band, 0.1- $\mu\text{m}$  GaAs pHEMT MMIC amplifier. (From: [1]. Courtesy of QuinStar.)

band compared with the simulation. That was an effect predicted by simulating a complete single-ended amplifier with all matching and bias networks included.

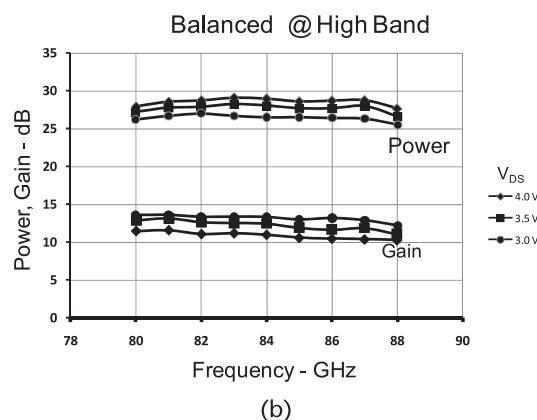
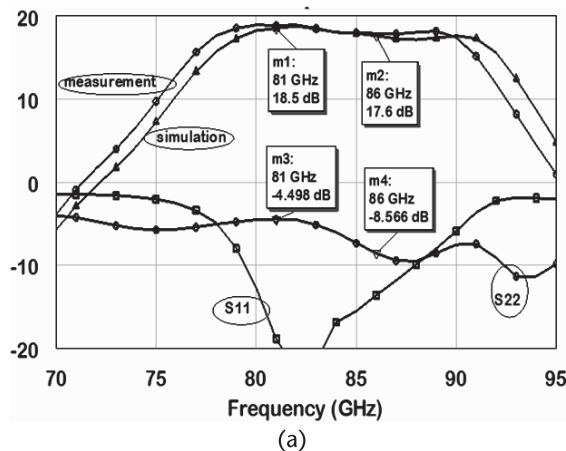
The power performance for the balanced version is shown in Figure 6.2(b) for three different drain bias conditions. The maximum power is obtained at  $V_{DS} = 4.0\text{V}$ , achieving 28.5 to 29.2 dBm within the 81 to 86-GHz band. The gain is compressed by 4 dB at this power level. The DC quiescent bias current ranges from 1,180 to 1,550 mA. The amplifier efficiency for maximum power is around 10%.

## 6.2 F-Band Amplifier

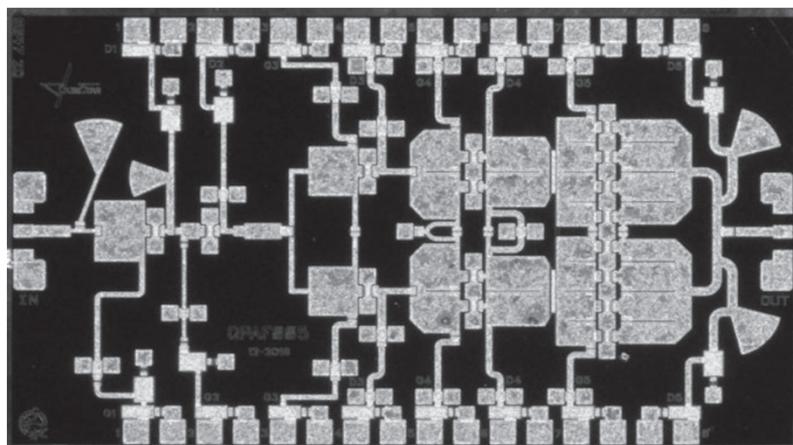
The second example of a GaN HEMT MMIC amplifier was reported in 2017 [2] with power levels at F-band that qualifies this design as state-of-the-art. The MMIC was fabricated by HRL, in Malibu, California, using their 0.14- $\mu\text{m}$  process. Their devices have a typical  $f_{\text{MAX}}$  and  $f_T$  of 214 GHz and 87 GHz, respectively. They are designed to operate at 12V and their saturated power density is typically 1.9 W/mm.

The amplifier was designed to provide 20 dB of gain between 105 and 115 GHz. The photograph of the MMIC is shown in Figure 6.3. It contains an  $8 \times (4 \times 25)$   $\mu\text{m}$  device in the output stage. The unit contains 5 amplification stages with the following ratios 1:1:2:4:8, which gives a ratio of 2 between driver and power stage. The OMN uses a 4-way combiner, initially designed as two sections of a 2-way combiner. However, after the EM analysis, it was found that the circuit inserted more losses than a single 4-way combiner at these frequencies. The OMN is complemented with a series line and a short shunt stub. The EM simulation showed the combiner insertion loss (above the ideal 8-way power division loss) is typically 0.7 dB and the amplitude balance between the ports is about  $\pm 0.5$  dB.

The ISMN2 was halved with a driver feeding two power devices. The drain was matched in a first step to  $R_{\text{ref}}$  and in a second step matched to the gate of two power devices. The DC block between the stages is an interdigital capacitor, which also



**Figure 6.2** Measured small and large signal between 81 and 86 GHz MMIC: (a) small signal performance, and (b) pout and gain at 3 drain bias voltages. (After: [1].)

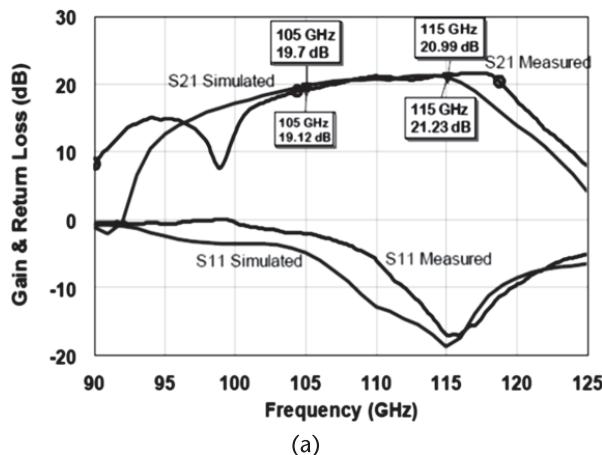


**Figure 6.3** F-band MMIC designed for the band 105 to 115 GHz. Chip size ( $3.3 \times 1.94 \text{ mm}^2$ ). (From: [2]. Courtesy of QuinStar.)

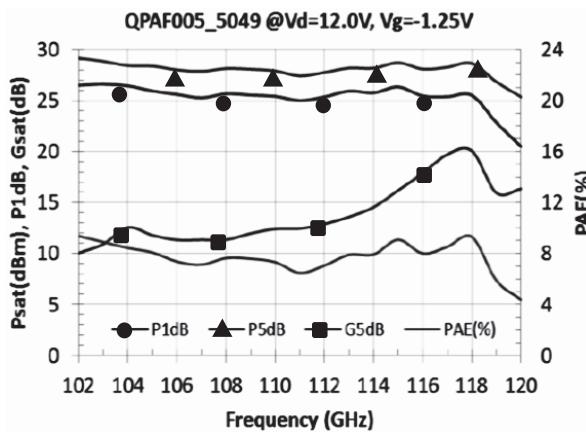
does the function of an impedance inverter. The predrivers and input stage uses a shunt short inductor to resonate the drain and a series MIM capacitor to block DC.

The MMIC small signal gain and return loss is shown in Figure 6.4(a). A simulated gain of 19.7 to 20.9 dB is achieved from 105 to 115 GHz. It compares favorably with the measured values within the same band. A resonance at lower frequencies was identified in the simulations at 91 GHz. The measured results showed that the resonance moved to 98 GHz. It also shows an extended band going up to 119 GHz. The simulated input return loss showed a value between 5 and 18 dB, which degraded by a couple of decibels at the low end.

The power was measured with the die properly attached to a base plate with high value ceramic off-chip capacitors, wired to the bias ports. The power performance is illustrated in Figure 6.4(b), showing a power range from 28 to 29 dBm (5-dB saturation) from 102 to 118 GHz. The bias voltage is indicated at the top of the figure. The power between 118 and 120 GHz shows a sharp drop-off with frequency, believed to be caused by measurement equipment. The efficiency is typically 8% over the band with a peak of 9.3% at 118 GHz.



(a)

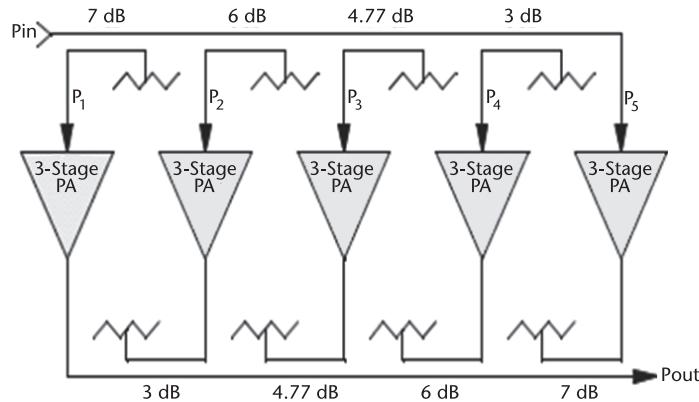


(b)

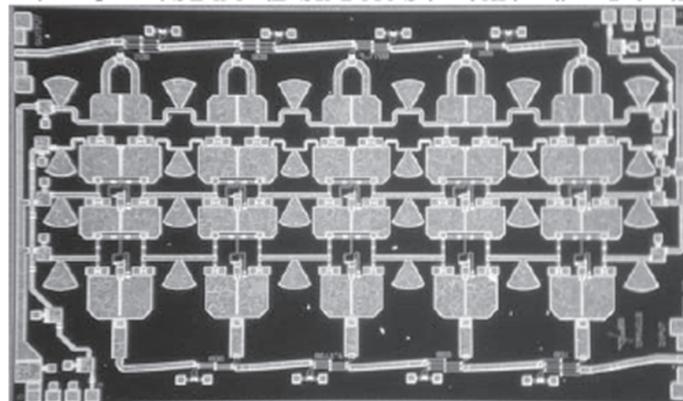
**Figure 6.4** F-band MMIC performance: (a) measured and simulated S-parameters, and (b) power performance measured at 5-dB compression. (After: [2].)

### 6.3 W-Band Amplifier

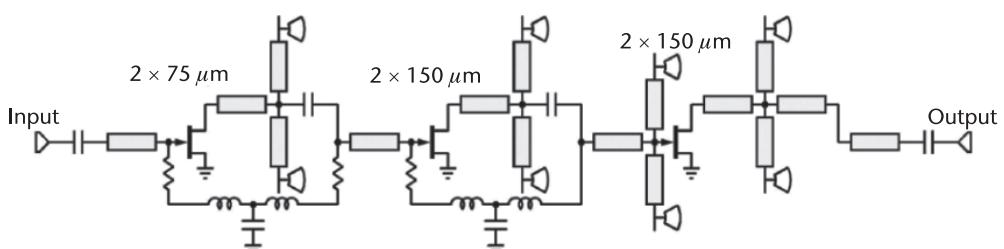
A broadband amplifier covering the entire W-band was reported in 2015 [3], with a minimum power of 2W, qualifying this design as a state-of-the-art amplifier. The technology employed in the design is a  $0.14\text{-}\mu\text{m}$  gate length process by HRL. The concept architecture is a traveling amplifier, using Lange couplers and a unit amplifier



**Figure 6.5** Schematic of the traveling amplifier with 5 unit amplifiers. (After: [3]. © 2013 IEEE.)



**Figure 6.6** W-band broadband MMIC. Chip size ( $3.2 \times 5.4 \text{ mm}^2$ ). (After: [3]. © 2013 IEEE.)



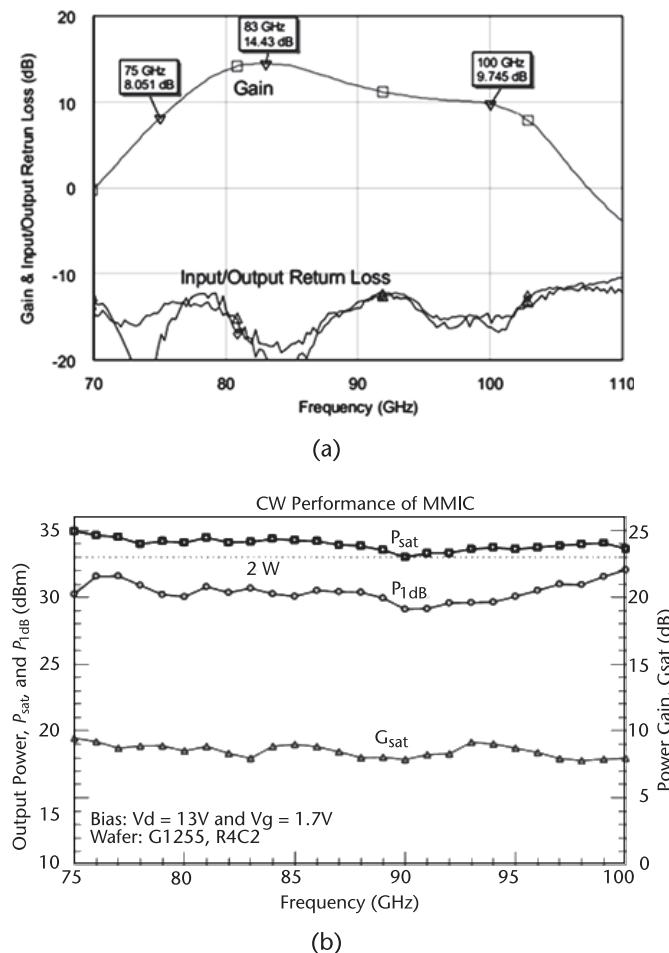
**Figure 6.7** W-band broadband MMIC. Chip size ( $3.2 \times 5.4 \text{ mm}^2$ ). (After: [3]. © 2013 IEEE.)

capable of covering the W-band. In this design, the power of five unit amplifiers are combined, according to the block diagram of Figure 6.5. More details on the coupler design are found in [3].

The schematic for half the unit amplifier is represented in Figure 6.7, partially depicting the bias circuit. One can also observe that the lineup ratio is 1:2:2, which means that the ratio between driver and power devices is 1:1.

The amplifier's small signal performance is shown in Figure 6.8(a), where a minimum gain of 8 dB and maximum of 14 dB is achieved within the 75 to 100-GHz band. The amplifier is biased at  $V_{DS} = 10V$ .  $V_{GS} = -2.2V$  and  $I_{DS} = 1A$ . The input and output return losses are better than 15 dB over the band.

The power performance presented in Figure 6.8(b) was achieved with the device biased at  $V_{DS} = 13V$  and  $V_{GS} = -1.7V$ . One can observe a minimum output power of 2W near 90 GHz and a maximum of 3.2W at 75 GHz. The same device was

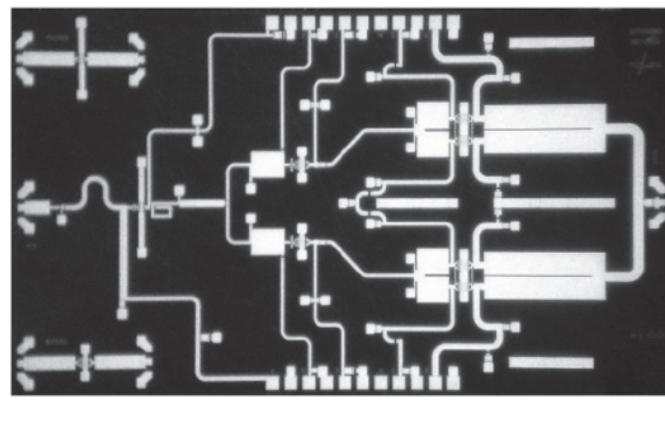


**Figure 6.8** W-band coverage with a single GaN MMIC amplifier: (a) measured small signal gain and return loss, and (b) measured  $P_{sat}$ ,  $P_{1dB}$ , and  $G_{sat}$ —75–100 GHz. (After: [3]. © 2013 IEEE.)

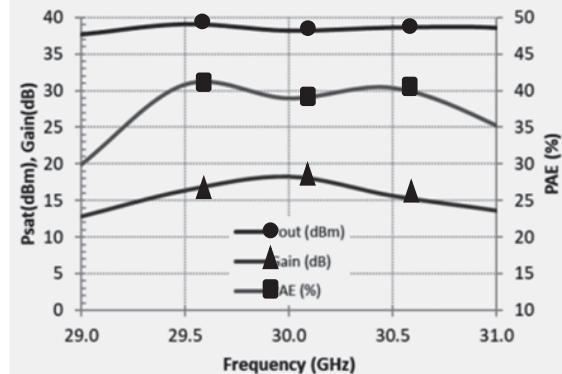
biased with a 16-V pulse with a duty cycle of 10% and a pulse width of 100  $\mu$ s, providing 3.6W at 83 GHz.

## 6.4 Ka-Band Class F Amplifier

An example of a class F amplifier applied to millimeter-wave was reported in 2018 [4], showing an output power of 10W and a PAE of 42%, which qualifies this design as state-of-the-art. The drain impedance at the fundamental frequency and at the harmonic terminations is tuned to improve power and efficiency. This amplifier was manufactured with a GaN HEMT technology, by Northrop Grumman, featuring a gate length of 0.2  $\mu$ m. The process yields devices with a breakdown of 90V and  $f_T$  and  $f_{MAX}$  of 40 and 100 GHz, respectively. The output power density for drain bias between 24V and 28V is 4 W/mm. A photograph of the MMIC measuring  $5.4 \times 3.1$  mm<sup>2</sup> is in Figure 6.9(a).



(a)



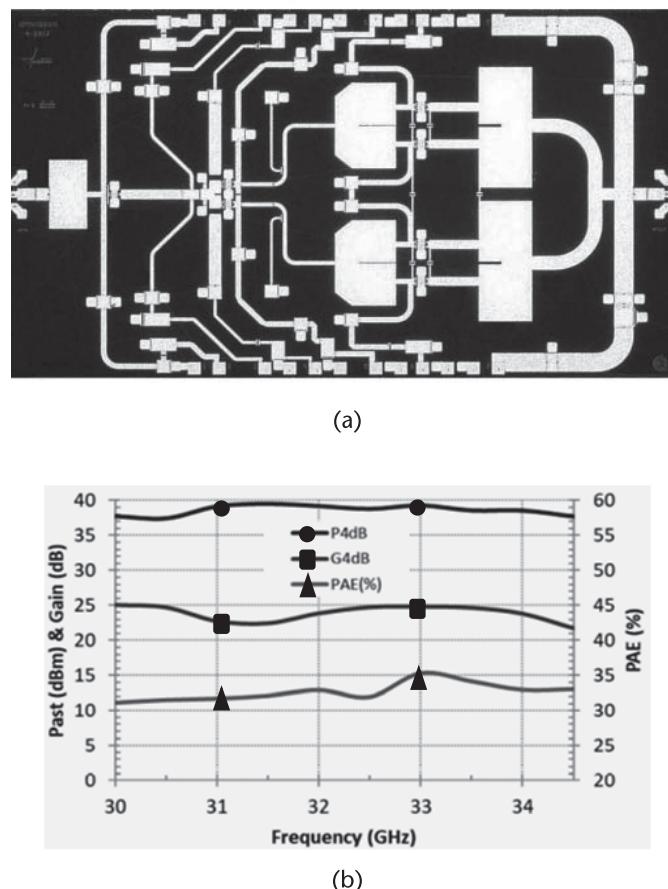
(b)

**Figure 6.9** Class F GaN amplifier for a 30-GHz operation [4]: (a) layout of amplifier, and (b) large signal performance. (Courtesy of QuinStar.)

Three amplification stages are employed in the design and the power performance over frequency is shown in Figure 6.9(b). With the device biased at 28V, the MMIC achieves an average output power of 38.6 dBm from 29 to 31 GHz (39.1-dBm peak at 29.5 GHz). The PAE is greater than 38.6% over the 29.5 to 30.5-GHz band, peaking at 42% at 29.5 GHz. The results are for a gain compressed by 7 dB over the band. Those measurements are at fixed bias. With pulsed bias, some increase in power and efficiency is expected.

Another project of importance from same reference, using the same technology, was the realization of an amplifier targeting power and bandwidth. Its photograph is shown in Figure 6.10(a). The design uses two sections of a 2-way transformer, with a short shunt stub for biasing. The ISMN2 uses a shunt short stub to resonate the driver drain impedance. This die has the same dimensions as the previous one and delivers the performance shown in Figure 6.10(b).

The typical power performance is a power ranging from 39 to 40 dBm (10W) over the 31 to 34-GHz band, with an associated gain of 24 to 25 dB. The PAE is greater than 30% across the band and reaches a peak of 36% at 33 GHz. This performance is obtained with the gain compressed by 4 dB.

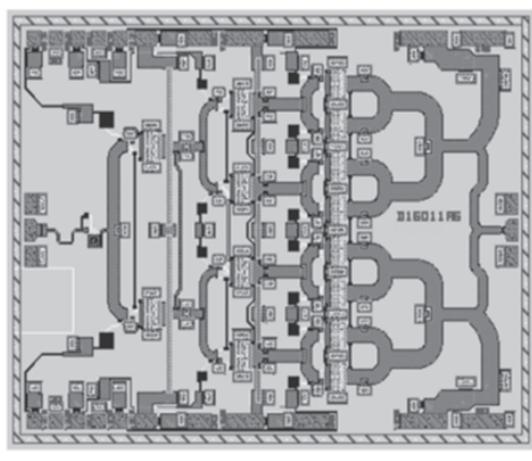


**Figure 6.10** Large-band GaN amplifier for an operation within 30 to 35 GHz [4]: (a) layout of amplifier, and (b) large signal performance. (Courtesy of QuinStar.)

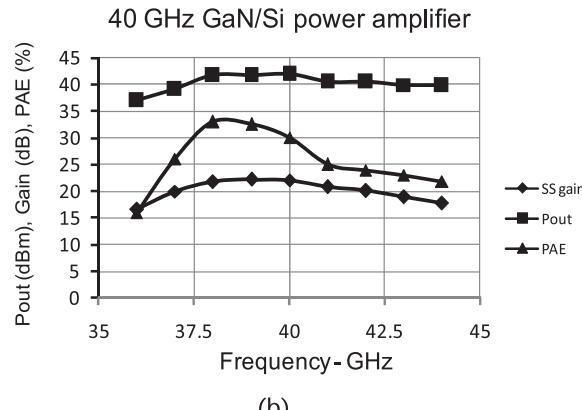
## 6.5 GaN/Si Ka-Band Amplifier

This work was considered state-of-the-art in 2018, not exactly for its absolute power capability, but rather being produced by a commercial foundry [5], on a silicon wafer, and showing good power performance. This is a 0.1- $\mu\text{m}$  gate length technology, with a breakdown voltage of 40V, a power density of 3.3 W/mm, and an  $f_T$  of 105 GHz. A first drawback to design on the Si substrate is the via impedance. Moron et al. reported a resistance of  $5\Omega$  in series with an inductance of 20 pH measured at 40 GHz. The amplifier design combines 8 unit cells probably measuring  $6 \times 65 \mu\text{m}$ . That gives enough power to overcome the output circuit losses. A second drawback is to control the maximum channel temperature, set at 200°C. They were able to achieve this goal by controlling the load line presented to the device current source.

The OMN is composed of conventional two sections of 2-way combiners, with a short stub for biasing and additional matching, as shown in Figure 6.11(a). The ISMN2 uses a parallel shunt short stub resonator in the drain and lumped capacitors to ground. The measured results for the amplifier, depicted in Figure 6.11(b),



(a)



(b)

**Figure 6.11** GaN/Si power amplifier: (a) amplifier layout, and (b) performance at a gain compressed by 4.5 dB. (After: [5]. © 2018 IEEE.)

is a minimum power of 13.5W between 28 and 40 GHz. The PAE is above 30% within 38 to 40 GHz. The MMIC is biased at 12V and total quiescent current is 890 mA. The current at 4.5-dB compression goes up to 3,800 mA.

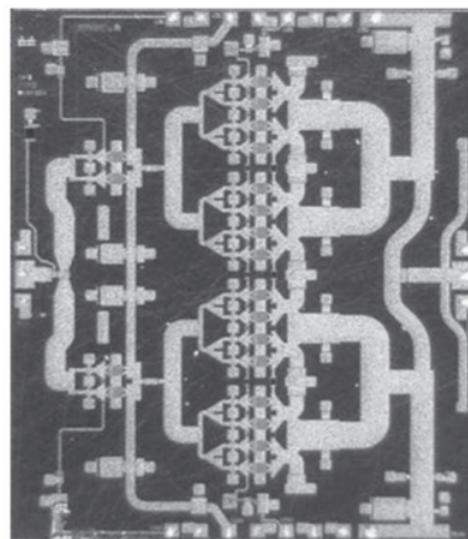
## 6.6 Ka-Band High-Efficiency Amplifier

There are a number of state-of-the-art amplifiers that have been reported in recent years. In particular, the design of this chip by Northrop Grumman, reported in 2015 [6], was considered state-of-the-art in terms of power, efficiency, and small die size. The GaN HEMT technology is a gate length of a 0.2- $\mu$ m process also employed in the Class F amplifier. The photograph of this MMIC is in Figure 6.12.

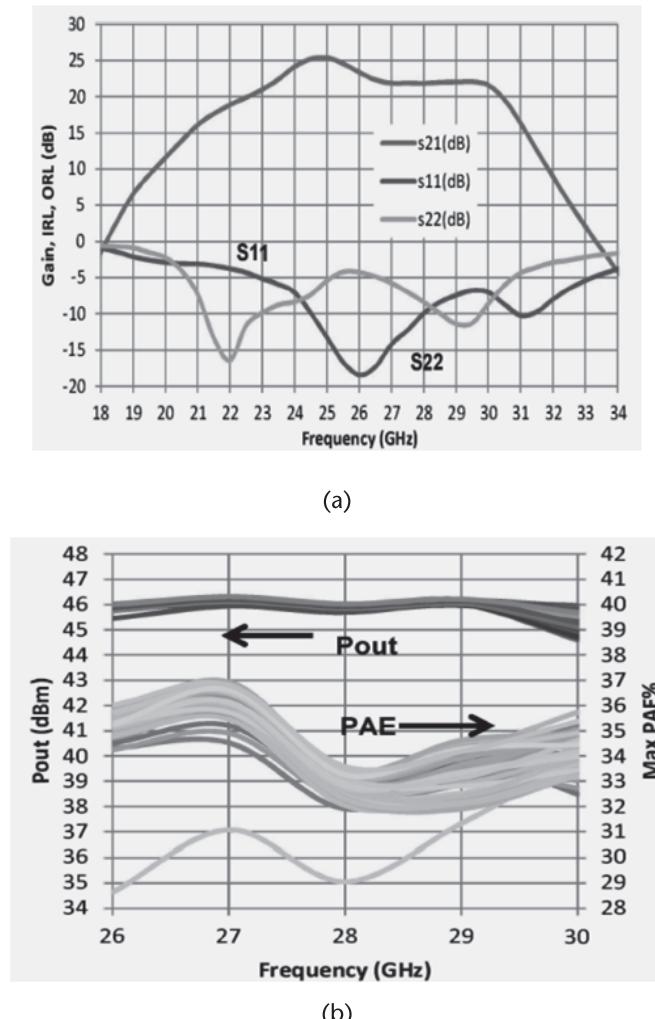
An analysis of this figure shows that the drain matching of this amplifier combines two unit cells with a series line followed by a shunt capacitor. Two of these cells are then combined with a low-impedance quarter-wave transformer followed by a short shunt stub.

On the gate side, we can verify the use of shunt capacitors close to the gate for impedance matching. The capacitors are connected to ground by means of vias. The figure shows that each via is shared between two capacitors, except for the capacitors located at the top and bottom. The small signal performance for this design is shown in Figure 6.13(a), where a gain greater than 20 dB is obtained from 23 to 30 GHz.

The power performance over a number of samples is shown in Figure 6.13(b), measured on wafer using a pulsed system with a drain biased at 28V. The output power corresponds to 40W over the 27 to 29-GHz band, with a PAE ranging from 32% to 37%. Most samples meet a PAE minimum of 32%, except for one device that measured 29%. A peak power of 43W is achieved at 27 GHz with a PAE at that point greater than 36%. The estimated drive power for these evaluations is 30



**Figure 6.12** Ka-band GaN MMIC amplifier for a 30-GHz operation. Chip size estimation ( $3.0 \times 4.5 \text{ mm}^2$ ). (After: [6]. © 2015 IEEE.)

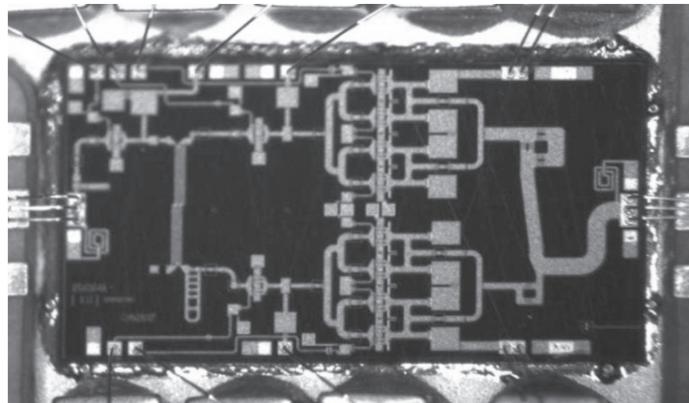


**Figure 6.13** Ka-band MMIC performance: (a) measured small signal S-parameters, and (b) large signal performance for a number of samples. (From: [6]. © 2015 IEEE.)

dBm, giving a compressed gain of 6 dB. The power variation is less than 0.5 dB and the PAE is less than 5%.

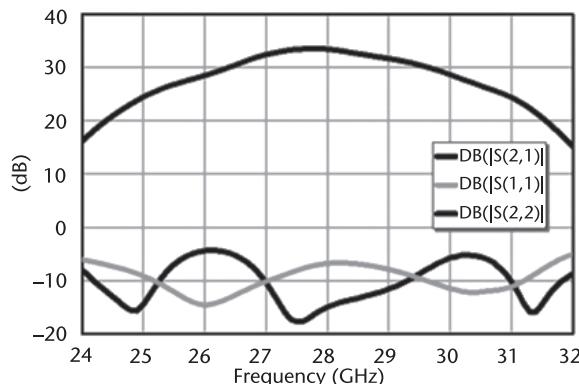
## 6.7 Ka-Band Doherty Amplifier

This design uses the 0.15- $\mu$ m GaN HEMT Qorvo technology, reported in 2019 [7]. Typical DC characteristics of the transistors are 1.15 mA/mm, and  $V_P = -2.9V$  at  $V_{DS} = 10V$ . The breakdown voltage at  $I_{GD} = 1$  mA/mm is 75V. The MMIC amplifier results are a 20% PAE at 6-dB output power backoff (OBO) from saturated power, within the 27 to 29.5-GHz band. A power density of 3 W/mm was measured on a prematched circuit at a PAE of 48%. The MMIC photograph is shown in Figure 6.14.

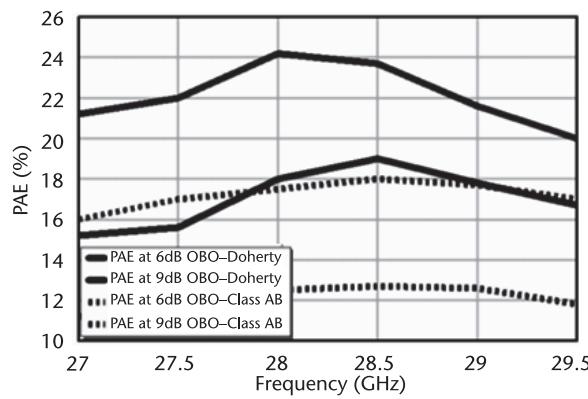


**Figure 6.14** Doherty GaN MMIC amplifier. Die size is  $4.33 \times 2.3 \text{ mm}^2$ . (From: [7]. © 2019 IEEE.)

The drain matching circuit has a series line and shunt short stub and makes use of a shunt capacitor over via. The gate matching uses a series line and also a shunt capacitor over via. Both drain and gate use 2 sections of a 2-way combiner/divider.



(a)



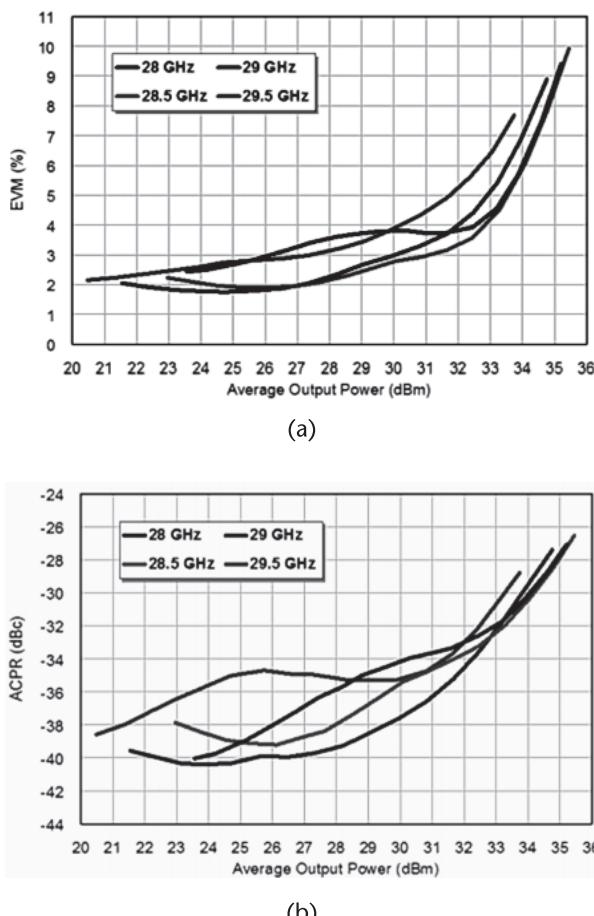
(b)

**Figure 6.15** Ka-band Doherty MMIC performance: (a) measured small signal S-parameters, and (b) PAE at different back-off values. (After: [7]. © 2019 IEEE.)

The impedances for this design were measured with a load-pull scheme on a prematched device measuring  $8 \times 50 \mu\text{m}$ . The evaluation was made with the device biased at Class AB and Class C. The total dimension of the output device is  $4 \times 8 \times 50 \mu\text{m}$ .

The MMIC Doherty amplifier S-parameters are shown in Figure 6.15(a). A gain of 30 dB is observed between 26.5 and 29.5 GHz. The input return loss is better than 5 dB and the output is better than 10 dB within the same frequency range. The saturated peak power is near 8W and the corresponding PAE varies from 28.5% to 30.5%. The PAE under backoff modes is shown in Figure 6.15(b). The solid line indicates the PAE at 6 and 9-dB OBO. The first curve shows 24% between 28 and 28.5 GHz and the second 18% over the same band. The dotted line corresponds to PAE for a regular class AB amplifier at the same OBO levels. The MMICs are biased at 28V.

The digital performance of this amplifier was measured with an unclipped 64-QAM CP-OFDM 5G NR signal with a 400-MHz instantaneous bandwidth and 120-kHz subcarrier spacing. The resulting EVM in Figure 6.16(a) shows a maximum of 4% at an average output power of 30 dBm. The ACPR in Figure 6.16(b) is below -34 dBc up to an average power of 30 dBm.



**Figure 6.16** Digital parameters for the Ka-band Doherty MMIC performance: (a) measured EVM, and (b) measured ACPR. (After: [7]. © 2019 IEEE.)

## References

- [1] Camargo, E., et al., “Power GaAs MMICs for E-Band Communications Applications,” *IMS2014*, 2014.
- [2] Camargo, E., et al., “F-Band, GaN Power Amplifiers,” *IMS2018*, 2018.
- [3] Schellenberg, J., “A 2-W W-Band GaN Traveling Wave Amplifier with 25 GHz Bandwidth,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 63, No. 9, September 2015, pp. 2833–2840.
- [4] Estella, N., et al., “High-Efficiency, Ka-Band Power Amplifiers,” *IMS2018*, 2018.
- [5] Moron, J., et al., “12W, 30% PAE, 40 GHz Power Amplifier MMIC Using a Commercially Available GaN/Si Process,” *IMS2018*, 2018, pp. 1457–1460.
- [6] Din, S., M. Wojtowicz, and M. Siddiqui, “High Power and High Efficiency Ka Band Power Amplifier,” *IMS2015*, 2015.
- [7] Wohlert, D., et al., “8-Watt Linear Three-Stage GaN Doherty Power Amplifier for 28 GHz 5G Applications,” *2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium*, Nashville, TN, 2019.

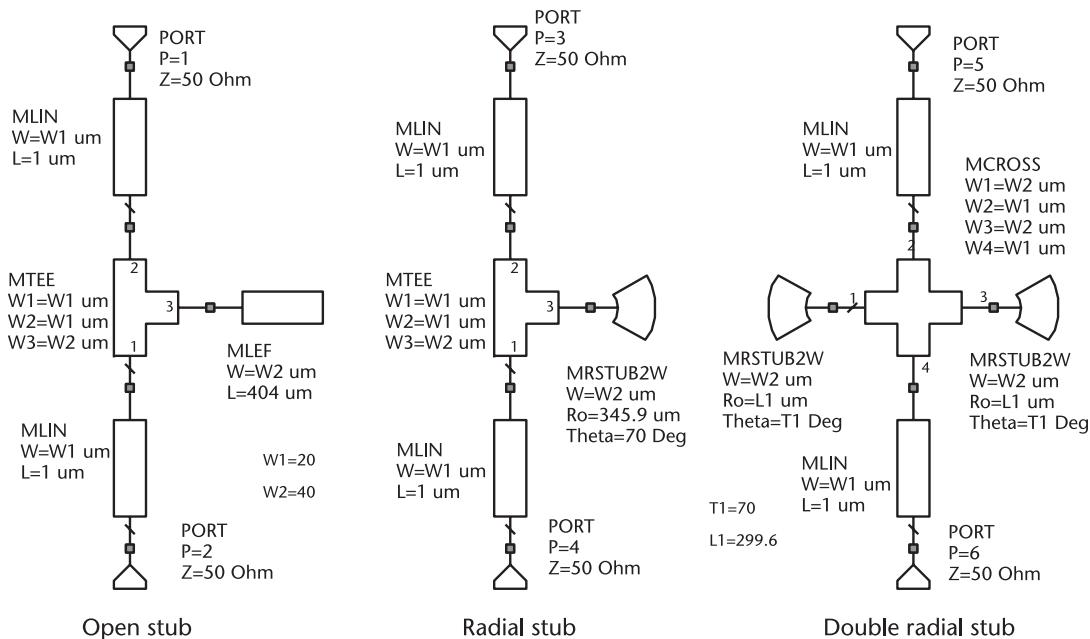
## APPENDIX A

# Bias Filters

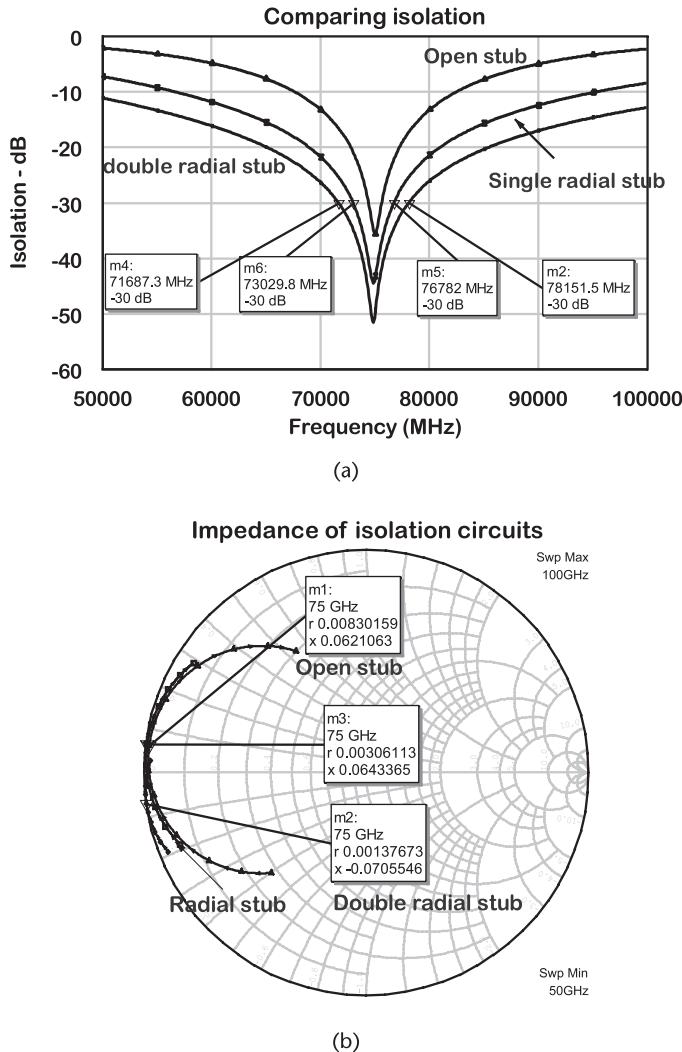
## A.1 In-Band Filters

In-band filters are expected to create a high isolation within the amplifier bandwidth. The distributed filters options are shown in Figure A.1. The first option is to use a quarter-wave length open stub to invert the open circuit into a short circuit. The second option uses a radial stub, following the same principle as the open stub. It does have the advantage of larger bandwidth and shorter length compared to the open stub. Further isolation is obtained by paralleling two radial stubs.

Assuming an isolation of 30 dB between the ports, one can observe in Figure A.2(a) a bandwidth of 3.75 GHz for the single radial stub and 6.5 GHz for the double radial stub at the central frequency of 75 GHz. The impedance displayed in Figure A.2(b) shows that none of these options gives a short impedance at the center frequency. It is either slight inductive or capacitive. The most important property of the filter is to maintain a high isolation between the ports. The residual reactance can be absorbed by the length of the quarter-wave bias line connecting the filter to the device port.



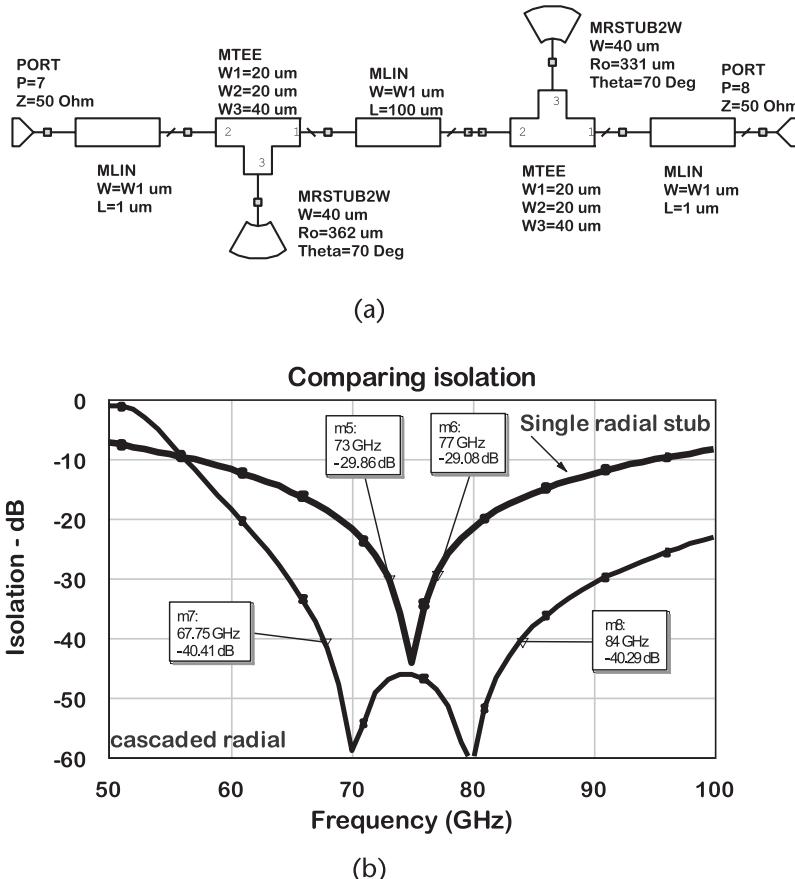
**Figure A.1** Bias filters using open stub elements.



**Figure A.2** Isolation and impedance of the different filter options: (a) comparing isolation, and (b) comparing the impedance.

One can see that the double radial stub has larger bandwidth, but in certain applications it is not enough. An alternative is to cascade two single radial stubs in the manner represented in Figure A.3(a). In order to avoid resonance between the open stubs, a series line is inserted between them. One can observe in Figure A.3(b) a bandwidth of 16 GHz considering a minimum rejection of 40 dB.

The use of radial stubs in an MMIC requires a careful consideration of their coupling. That degrades performance and can potentially generate instabilities. In principle, laying out open stubs such that the open areas are not close to each other minimizes the coupling. An EM analysis of the bias circuit helps to solve the



**Figure A.3** Schematic for the cascade of radial stubs and isolation results: (a) circuit schematic, and (b) isolation curves.

coupling problem. The design parameters to consider are the radius and the aperture angle. Another point to consider is the size taken by a radial stub compared to a lumped filter option.

A capacitor on top of a via is a convenient means to obtain a resonant short, by adding the proper capacitor dimensions on top as described in Figure 2.7 in Chapter 2. The minimum resonance frequency will occur with largest plate dimensions, in this case about  $45 \times 45 \mu\text{m}^2$ . In Figure 2.15, that resonance takes place at 79 GHz. At lower frequencies, the alternative is to use two shunt capacitors, one at each side of a line depicted in Figure 2.16. The schematic for this option is indicated in Figure A.4(a), and isolation is shown in Figure A.4(b). Considering a minimum isolation of 30 dB, the bandwidth is equal to 7.25 GHz at the center frequency of 40 GHz, resulting in a fractional bandwidth of 18%. The design parameters are the capacitor length and width.

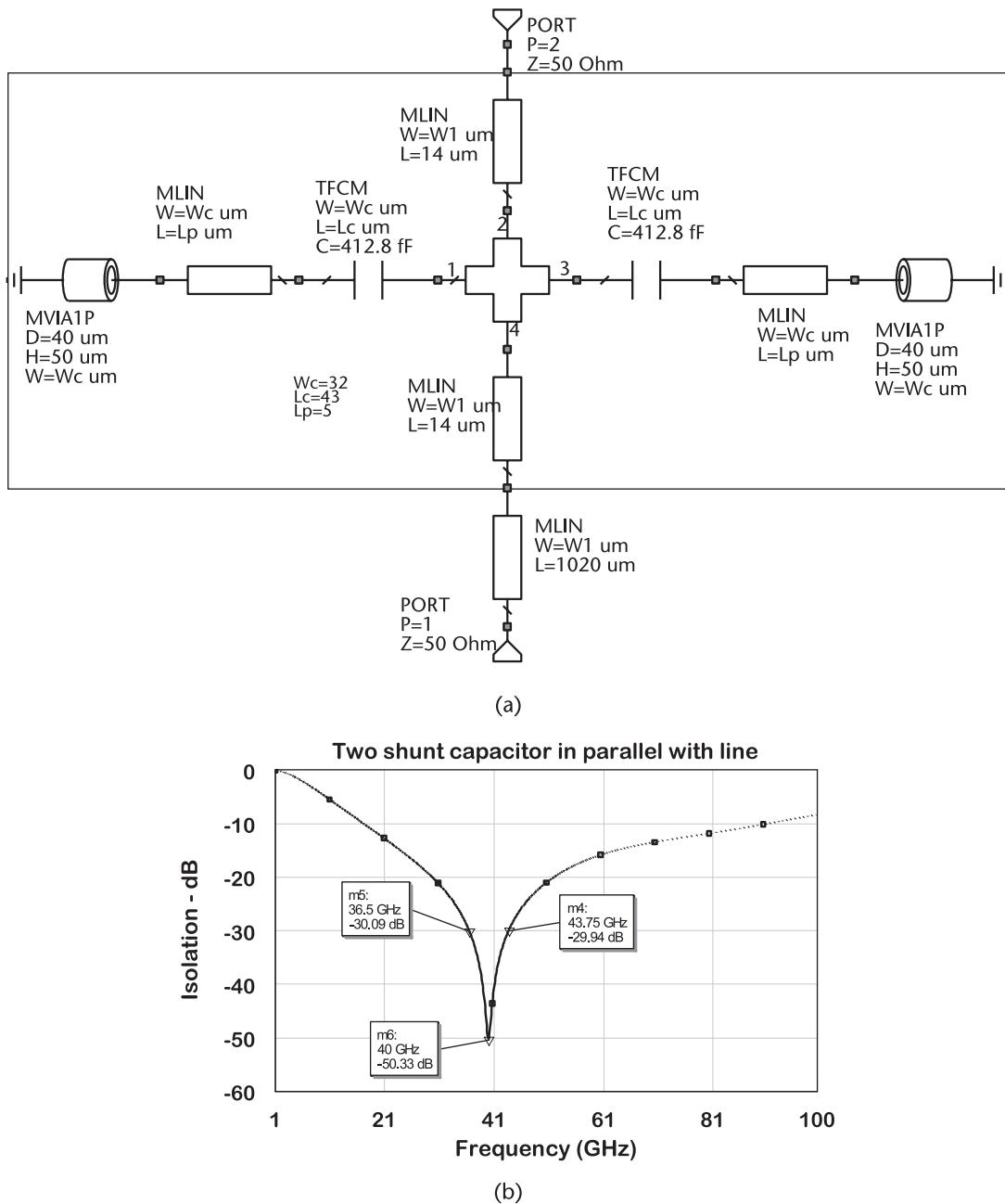
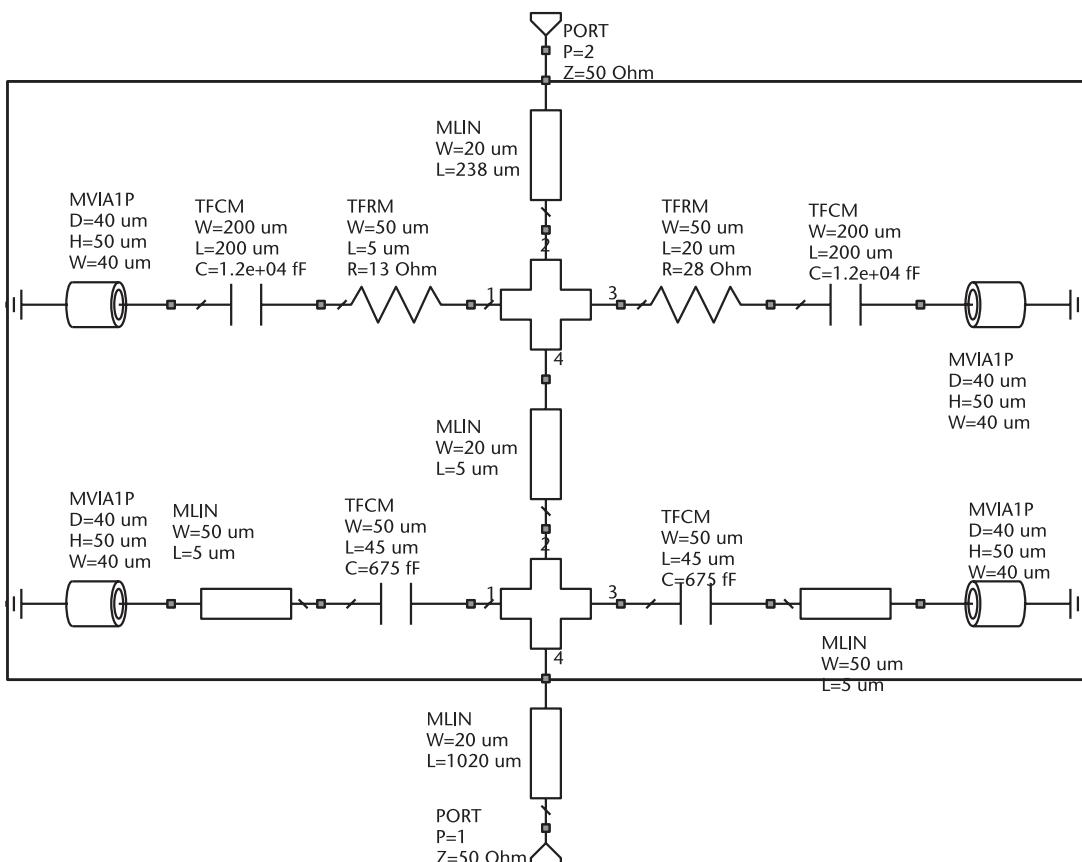


Figure A.4 Use of a capacitor in series with a via: (a) circuit schematic, and (b) simulation of isolation.

## A.2 In-Band/Out-of-Band Filters

The main problem of out-of-band is the possibility of unstable operation. Ideally, the filter should present a termination to the gate and to the drain that guarantee a stable operation. In general, the devices have a tendency to oscillate in the low microwave region, due to high gate impedance and to an increase of the device gain. That is the reason to add another filter, comprising a resistor in series with a shunted capacitor at each side of the main bias line. The circuit in Figure A.5 contains an in-band filter and is cascaded to another filter containing two series RC circuits to ground, one at each side of the transmission line. The series transmission line connecting the two filters improves isolation and avoid resonances between the two filters.

The determination of the RC filter needs to take into account the device size. Let us assume that the output stage has 8 unit cells, each one measuring  $8 \times 50 \mu\text{m}$  for a total periphery of 3.2 mm. The device capacitances will be in the order of  $C_{gs} = 2.54 \text{ pF}$  and  $C_{ds} = 0.6 \text{ pF}$ . The capacitor of the RC filter should be much larger than the device capacitance to effectively shunt the resistor below the microwave range, say, 1 GHz. Therefore, the 3-dB cutoff RC circuit is given by  $f = 1/(2\pi RC)$ . If  $C = 10 \times C_{gs} = 25.4 \text{ pF}$ , the cutoff frequency is 1 GHz and the resistor is  $R = 6.5\Omega$ .

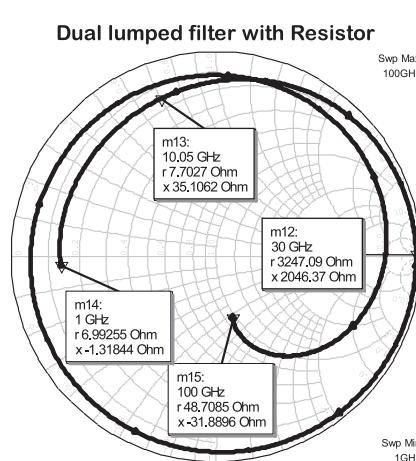
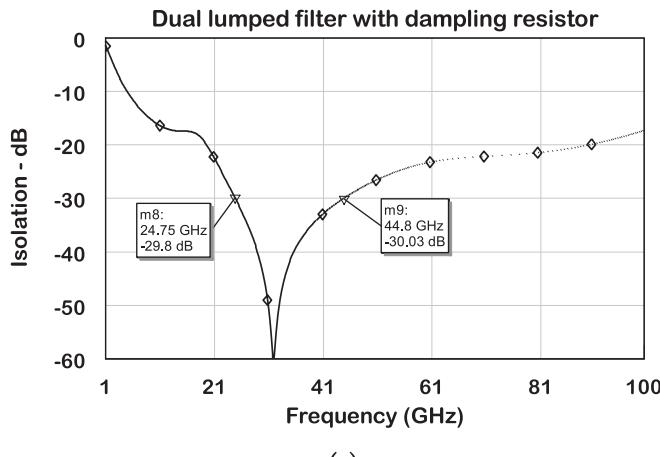


**Figure A.5** Schematic for the dual lumped filter.

The frequency response is in Figure A.6(a), depicting 20 GHz of band, considering an isolation of 30 dB. The impedance at port 1 is represented in Figure A.6(b). It is an open circuit at the center frequency of 30 GHz and between 1 to 10 GHz shows a real part impedance of  $7\Omega$ . The circuit also has a resistive component between 80 and 100 GHz. If during stability tests a negative resistance is located at a specific frequency but out-of-band, then the filter parameters have to be changed.

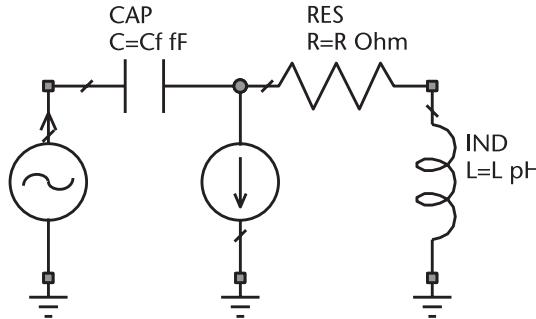
### A.3 Filtering Below 1 GHz

The low-frequency range requires a more detailed analysis due to its importance in stability and on linearity. This problem was modeled in [1] with a simple DC model for the device, represented in Figure A.7. The input impedance is given by (A.1), also valid for the output impedance.



(b)

**Figure A.6** Performance of the dual lumped filter: (a) isolation response, and (b) impedance of port 1.



**Figure A.7** Representation of a device DC model with a load  $Z$ .

$$Z_{in} = \frac{Z + \frac{1}{j\omega C_f}}{1 + g_m Z} \quad (A.1)$$

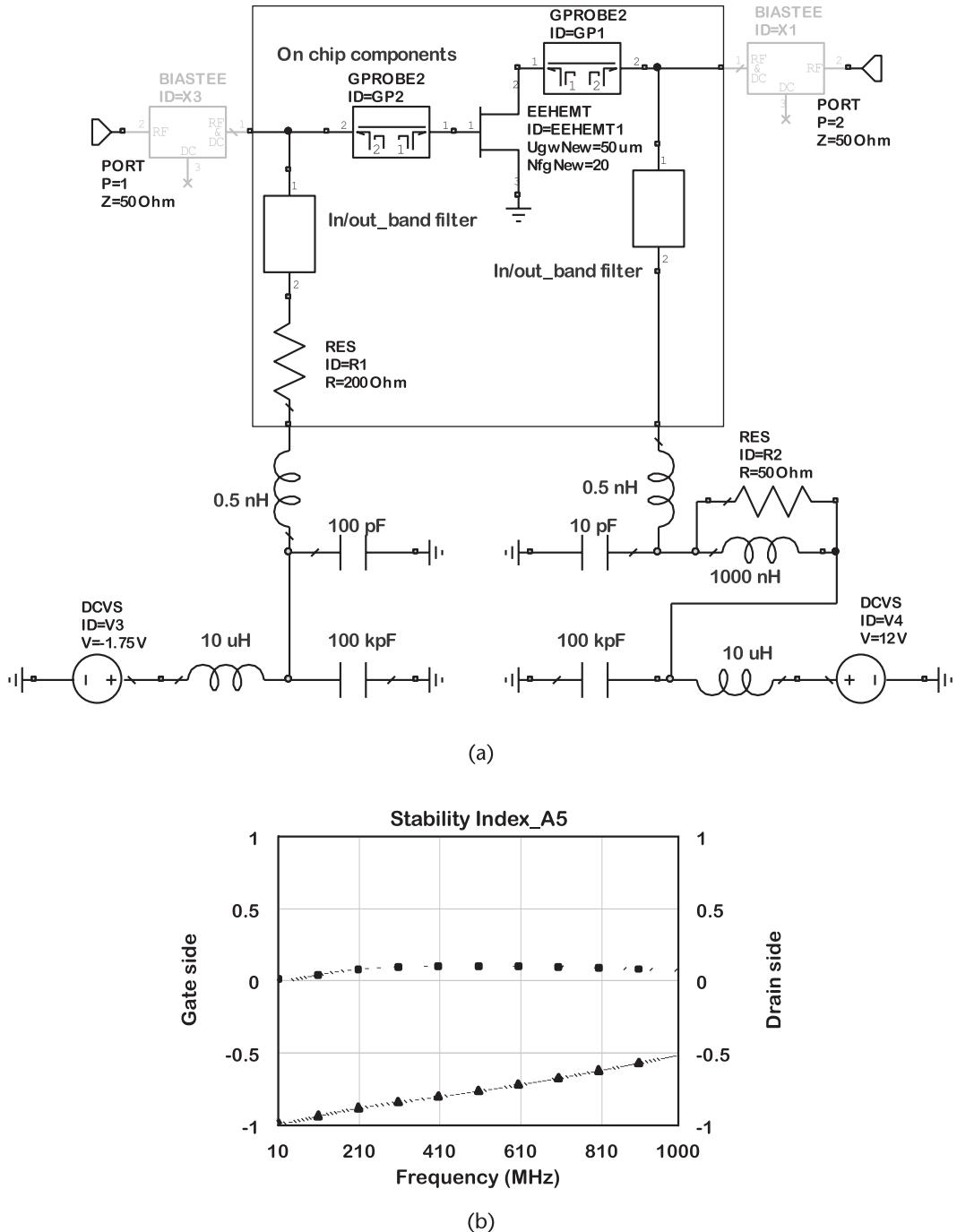
Developing (A.1), making the assumption that  $1/(\omega C_f) \gg (\omega L)$ , a simple condition for the negative resistance is obtained from (A.3). For a 2-mm device,  $g_m = 375$  mS, and using an inductor  $L = 10$  nH, one obtains a negative resistance for frequencies above 15 MHz.

$$Z_{in} = \frac{1}{1 + (g_m \omega L)^2} \left( \frac{1}{j\omega C_f} - \frac{g_m L}{C_f} \right) \quad (A.2)$$

$$g_m \omega L \gg 1 \quad (A.3)$$

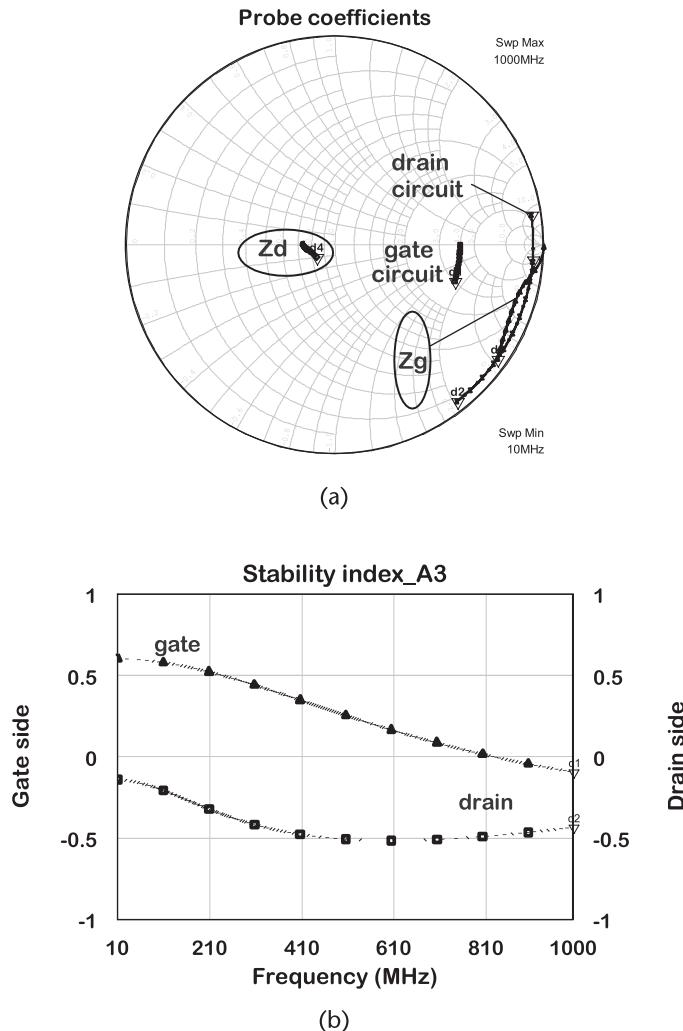
The filtering at this frequency range is off-chip, as shown in Figure A.8. Parallel plate ceramic capacitors in the order of 10 to 100 pF are epoxy-attached close to the die. Wire bonds are used to attach the DC contact on chip to the off-chip capacitor. The wire bond inductance is, in general, less than 1 nH. To improve isolation to lower frequencies, additional chip capacitors of 1 mF are connected in shunt with the parallel plate capacitor. Such a circuit makes  $Z_{in} \approx 0$ . This arrangement works for most cases. The insertion of a resistor in the gate circuit improves the low-frequency stability. In the drain circuit, it has to be applied in shunt with a large capacitor to ground. Notice that the probes used to check loop stability are also useful to verify the low-frequency stability. The bias T is disconnected from the circuit to avoid interference with low-frequency impedance.

Let us assume that the baseband uses the 10 to 1,000-MHz frequency range. To obtain a high impedance within that frequency range, first, we need to modify the cutoff frequency from the in/out band filter from 1 to 5 GHz. Second, the capacitor close to the die is replaced by 1 to 5 pF. The overall circuit is similar to the one shown in Figure A.8. One can observe in Figure A.9(a) a high impedance for the drain circuit. The low device impedance  $Z_d$  is also shown in the same Smith chart.



**Figure A.8** Bias circuit and stability results: (a) typical FET bias circuit, and (b) gate and drain stability index.

On the other hand, the device gate impedance  $Z_g$  has a high value, and the gate circuit impedance is also high. The stability index is shown in Figure A.9(b), where both the drain and gate have a G factor much lower than 1, hence stable operation. One can see that, at both gate and drain, the resulting impedances are quite high and adequate to present a high impedance to the port terminals. The low impedance condition is easier to produce with a large capacitor at the MMIC terminals. However, the full band has to be considered, which makes this type of filter more difficult to design.

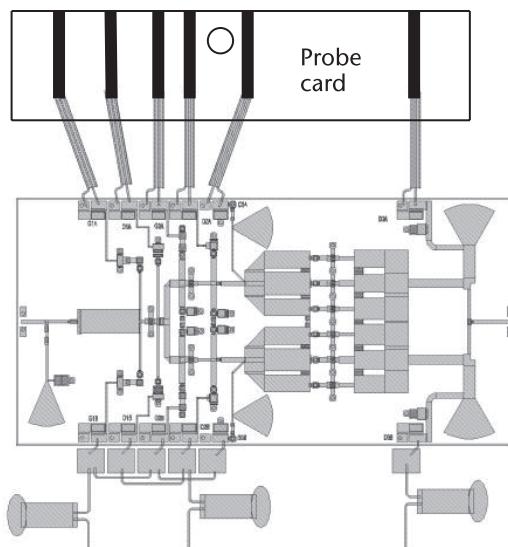


**Figure A.9** Circuit for high impedance drain bias at baseband: (a) high baseband impedance filter, and (b) stability index for the high impedance filter.

## A.4 MMIC Assembling for Evaluation

An example of an MMIC die attached to thermal metallic carrier (preferably a metal with similar temperature properties as the SiC substrate) is represented in Figure A.10. The south side of the die shows the assembling prepared for testing the MMICs using simple DC probes. Notice that the first two gates and first two drains are tied together at the parallel plate capacitor level. The large parallel capacitors are in the same figure. If a metal carrier is used, one side of the capacitor is epoxy-attached to the carrier and on the other side a wire bond connects the parallel plate capacitor to the large multilayer chip capacitor. The carrier is then taken to a probe station with RF probes. The DC probes are used to contact the parallel plate capacitors in the probe side, and are connected to a cable in the other side to be connected to a power supply.

It is important to be able to evaluate the die in the wafer before they are separated into individual chips. This is a desirable option, for one can separate the failed devices from the good ones. It is a much faster way to test an MMIC, since the bias are applied by means of a probe card, represented in Figure A.10 by the circuit connected at the north side of the MMIC. In this case, the low-frequency capacitors are assembled on the probe card, containing on one side access for bias cables and on the other side the coaxial probes. At millimeter-wave frequencies, it is important to use coaxial probes with a center contact for conveying the DC supply and a ground contact to connect to the MMIC ground. In this way, the connections are properly ground close to the device avoiding instabilities caused by the long cables connected to the power supplies. The probe cards on the north and south sides of the MMIC are lowered with a micrometer control to touch the pads. The RF probes are then lowered and contact is made at DC and RF. The probe cards can also be



**Figure A.10** MMIC testing. The top represents the option to use a probe card for wafer testing. The option to attach the die to a metal carrier and wire bond to capacitor filters is represented at the bottom.

used to test the MMICs in the wafer before they are separated. For a power device, it can be tested at reduced bias to avoid thermal dissipation effects. In a production environment, the machine is programmed to test each one of the MMICs and ink the dies that do not meet the specifications.

The real problem in the filter is the application in linear amplifiers. The FET in this case behaves as a mixer, where the termination at the harmonic frequencies and at baseband frequencies affects the distortion. Thus,  $Z_{in}$  must be considered in conjunction with a two-tone test. If best linearity requires  $Z_{in} = 0$ , then the circuit from Figure A.1 may be employed. However, if it requires  $Z_{in} = \infty$ , it may be difficult to design a stable circuit.

## Reference

- [1] Cripps, S., *RF Power Amplifiers for Wireless Communications*, Norwood, MA: Artech House, 2006, pp. 338–343.



## APPENDIX B

# Evaluation of MMICs

## B.1 Large Signal Measurements

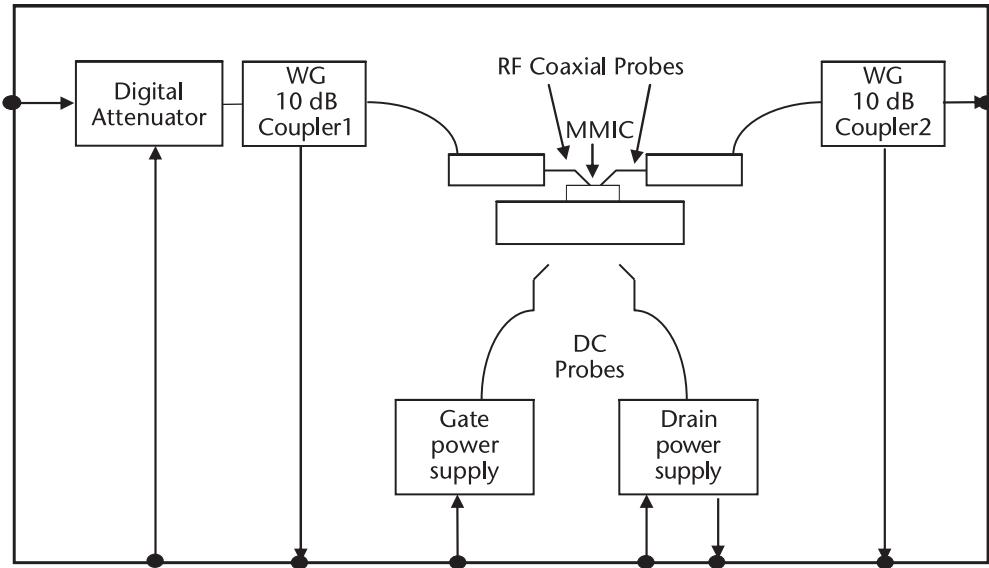
The measurements set up at millimeter-wave frequencies are made with waveguide components, which are divided in subbands according to Table B.1. WR stands for rectangular waveguide, and the associated number reflects the waveguide base dimensions in mils divided by 10.

The core setup for the evaluations of power MMICs starts with the probe station in Figure B.1. It contains a waveguide digital attenuator that provides attenuation from 1 dB to 50 dB in 0.1-dB steps. The step 0 corresponds to a minimum loss, in general, less than 0.5 dB. Therefore, an accurate variable input signal is applied to the device under test (DUT). The input and output signals are coupled by means of a waveguide coupler. The coupling is determined by the power levels under measurement. In general, a 10-dB coupler is used at both input and output. In some cases, a lower coupling ratio is employed at the input and higher at the output, depending on power levels.

The signal probes are, in most cases, coaxial. Therefore, a waveguide to coaxial transition is needed. It is common to make the connection with semirigid coaxial cables. The cable capable to operate up to 110 GHz has a diameter of 1 mm. The cable length should be kept as short as possible to minimize losses. There are also probes available with waveguide input so that one can skip the coaxial cables and use a waveguide connection. There are problems of cost and stiffness in the mechanical assembling. It is relatively easy to pull down the probes on the MMIC

**Table B.1** Standard Rectangular Waveguides

Frequency	Denomination	Waveguide
30–50	Q	WR-22/28
40–60	U	WR-19
50–75	V	WR-15
60–90	E	WR-12
75–110	W	WR-10
90–140	F	WR-8
110–170	D	WR-6
140–220	G	WR-5



**Figure B.1** MMIC probe station.

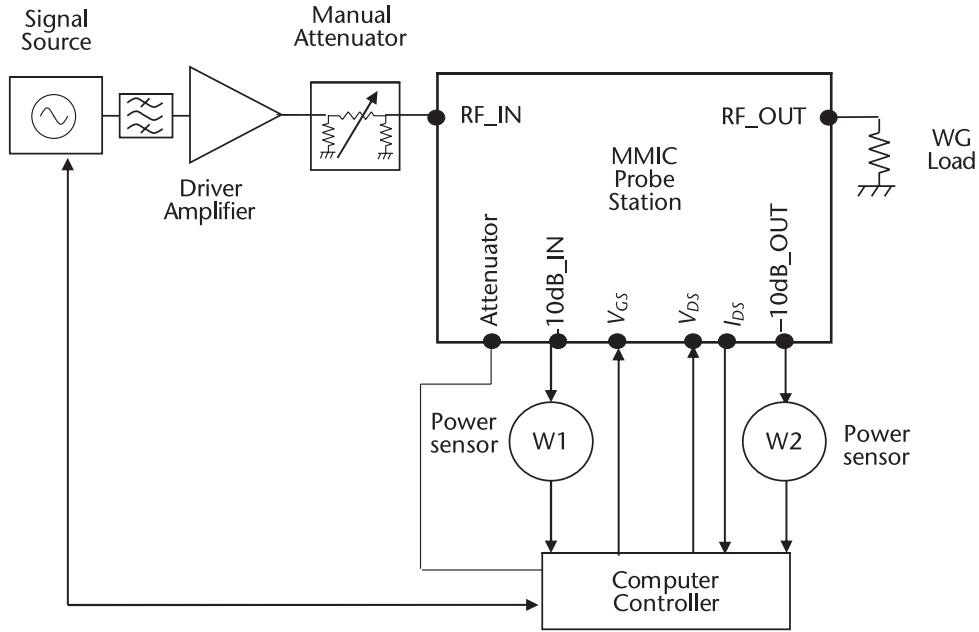
pads with a semirigid coaxial cable. It is not so simple to do the same operation with a waveguide connection. Notice the presence of two DC probes that usually are orthogonal to the RF probes represented in the figure.

The measurement setup shown in Figure B.2 is used to evaluate output power, gain, power at the 1 dB gain compression point, DC, and efficiency. Today signal generators capable of covering the full W-band are available from major microwave instrument suppliers. A cheaper solution is to use low-frequency signal generators followed by a frequency multiplier. In any case, it is desirable to use a bandpass filter to be sure that a clean spectrum is obtained.

A driver amplifier is needed to compensate the losses in the setup, which can be greater than 10 dB from the amplifier output up to the MMIC probe terminal. In principle, the driver amplifier is set to operate under saturation, maintaining a constant output power. A manual variable waveguide attenuator is used to set up the maximum signal at the MMIC. Power sensors are connected to the output of input/output to sample the power. The instruments are computer-controlled via an HP-VEE software or any other equivalent software. A Standard IEEE-488 cable is used to connect the computer to the equipment. They include the signal generator to control the frequency, the power sensors, and bias supplies. The results can be provided in an Excel format allowing the build of several types of plots.

### B.1.1 Calibration

The first step in the calibration process is to add a calibration power meter at the end of waveguide coupler1. This is done by removing the RF coaxial probe. The power meter W1 remains in place. The manual attenuator is adjusted for a power level at RF\_IN equal to 10 dBm. The digital attenuator is set to 0. The system is then run within the frequency range of interest. The losses between the calibration



**Figure B.2** Setup to measure power, gain, and efficiency.

power meter and power meter  $W_1$  are entered in the offset, making both power meters read the same power. In the second step, coupler 1 is directly connected to coupler 2 and the calibration power meter is connected to the RF\_OUT terminal. Another run is made and another set of loss is determined and inserted in the offset of power meter  $W_2$ . Thus, the power reading is the same as the calibration power meter. The third calibration step consists in the connection of the RF coaxial probes to the waveguides. Also, a short coplanar through line, similar to the one used to calibrate VNAs, is inserted between both probes. Another run is made to determine the total losses between coupler 1 and coupler 2. The losses now correspond to the coaxial cable losses, the probe loss, and through-line losses. An assumption is made that input and output losses are the same. Therefore, half the losses are added to the offset of power meter  $W_1$  and half to the offset of power meter  $W_2$ . The reading of  $W_1$  provides the power at the tip of the input probe and  $W_2$  provides the power at the tip of output probe.

### B.1.2 Evaluation

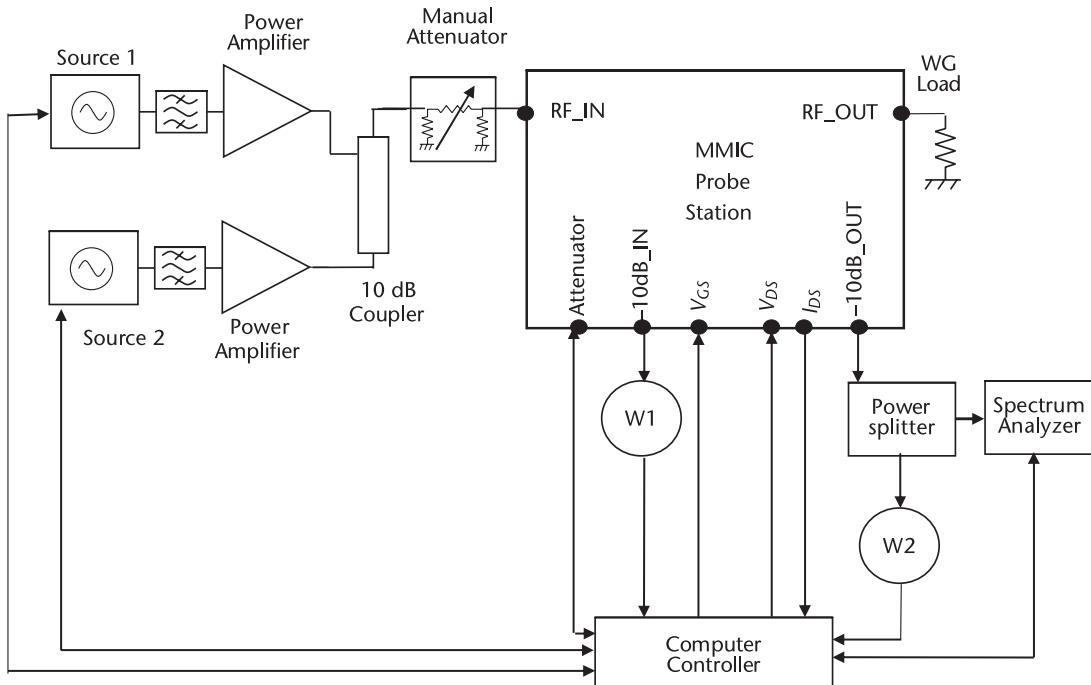
The calibration line is then replaced by the MMIC, and the power meter located at RF\_OUT is replaced by a waveguide load capable of dissipating the power level coming out from the DUT. The manual attenuator is readjusted to a level such that the power sensors operate below the maximum power. The range of the digital attenuator is set to run at an estimated maximum power minus 15 to 20 dB. The maximum power is the estimated MMIC output power. After applying bias, a first evaluation is made under small signal conditions and a check is made if the measurements are within the expected values. Then the controller is set to run a series

of evaluations, ranging from small signal to full compression, which can be in the order of 10 dB. At least 10 power levels are used in the evaluations. The resulting data file is then processed by the computer, using the Excel spreadsheet functions or any other tool. The losses are extracted from the evaluations, so that  $P_{\text{out}}$ , drain current, gain, and efficiency versus input driver are determined. The  $P_{1\text{dB}}$  is determined by extrapolation from the measured  $P_{\text{out}}$  versus  $P_{\text{in}}$  data.

## B.2 Two-Tone Linearity Test

The setup to determine the amplifier linearity is in Figure B.3. Observe that two signal generators are combined with a 10-dB waveguide coupler. This component offers a high isolation between the two signal sources. At the output, the sampled signal is split into two parts, a power meter and a spectrum analyzer. With the controller, it is possible to select the desired signals from the analyzer. It will provide the second, third, or fifth intermodulation levels. The calibration is similar to the process described above, using a single tone. Besides the calibration of the power meters, the spectrum analyzer is also calibrated to read the same power as  $W_2$ . Notice that the manual attenuator is now adjusted for the sum of power from each source. After calibration, the MMIC is inserted in the probe station and a test run is made for a selected number of power levels over the frequency band. The controller will read  $P_{\text{out}}$  versus  $P_{\text{in}}$  and the  $IM_2$ ,  $IM_3$ , and  $IM_5$  in the spectrum analyzer.

The cost of a millimeter-wave spectrum analyzer is, in general, much higher than a microwave spectrum analyzer. The alternative is to use a mixer with a fixed



**Figure B.3** Two-tone test measurement.

stable LO driver to transfer the spectrum to a lower frequency, measurable by a lower-frequency spectrum analyzer. It is important to maintain the mixer operating within a linear power range.

### B.3 AM-to-PM

To evaluate this parameter, the simplest means is to replace the power meters in Figure B.2 by sampling heads of a millimeter-wave VNA. The system is calibrated similarly to the previous measurement, using a through line to connect both ends of the millimeter-wave probes. The equipment will measure S-parameters from the device or the MMIC installed in the probe station.

That can be an expensive solution to evaluate this parameter. One possibility to cut the cost is to use mixers to step down the sampled signals and use a low-frequency VNA. However, a simpler and cheaper solution was proposed in [1]. It is based on the properties of a 90° millimeter-wave waveguide hybrid represented in Figure B.4. This type of coupler is popular in the application of balanced amplifiers, used to split and combine signals with a 90° phase difference between them. It is demonstrated by the equations below in that it can also measure phase differences between two incoming signals. For this coupler, the following properties are valid.

The input power at ports 1 and 2 can be expressed by the following equations:

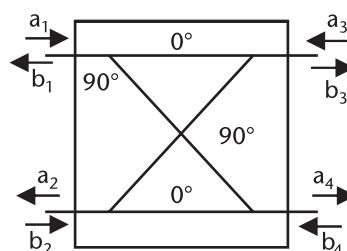
$$P_1 = |a_1|^2 \quad (\text{B.1})$$

$$P_2 = |a_2|^2 \quad (\text{B.2})$$

Using the S-parameters of an ideal 4-port hybrid coupler, the coefficients  $b_3, b_4$  are related to  $a_1, a_2$  with the following equations:

$$P_3 = |b_3|^2 = \frac{P_1}{P_2} + \frac{P_2}{2} - \sqrt{P_1 P_2} \sin(\phi) \quad (\text{B.3})$$

$$P_4 = |b_4|^2 = \frac{P_1}{2} + \frac{P_2}{2} + \sqrt{P_1 P_2} \sin(\phi) \quad (\text{B.4})$$



**Figure B.4** 90° hybrid coupler. (After: [1]. © 2013 IEEE.)

where the angle  $\phi$  represents the phase between the signals  $a_1$  and  $a_2$ . Working these relations, one obtains the two basic relations:

$$P_1 + P_2 = P_3 + P_4 \quad (\text{B.5})$$

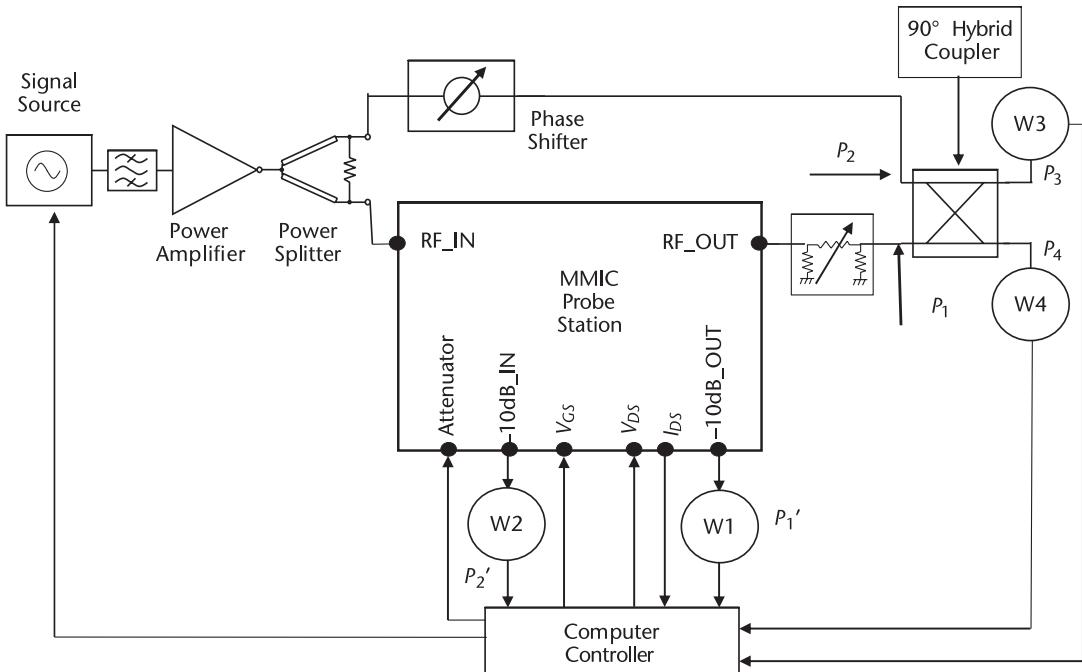
$$P_4 - P_3 = 2\sqrt{P_1 P_2} \sin(\phi) \quad (\text{B.6})$$

The angle between the incoming signals can be extracted by inverting the sinus function. Therefore, the angle is expressed as a function of the input power,  $P_1$ , and the power measured at the output ports,  $P_3$  and  $P_4$ .

$$\phi = \sin^{-1} \left( \frac{P_4 - P_3}{2\sqrt{P_1 P_2}} \right) \quad (\text{B.7})$$

$$\phi = \sin^{-1} \left( \frac{P_4 - P_3}{2\sqrt{P_1(P_3 + P_4) - P_1^2}} \right) \quad (\text{B.8})$$

The proposed measurement setup is in Figure B.5. Ideally, waveguide should be used as much as possible to minimize losses. The first step in the calibration is to find the losses in the system using  $P'_1$  and  $P'_2$ . The second step is to adjust the reading at  $P_1$  to be equal to  $P'_1$  and the reading of  $P_2$  to be equal to  $P'_2$ . The third



**Figure B.5** AM-to-PM test bench. (After: [1]. © 2013 IEEE.)

adjustment step requires a further analysis of (B.8). The angle  $\phi$  can be considered to be part of two terms; the first  $\phi_0$  corresponds to a constant phase difference, and the second is a term related to the AM to PM that is of interest.

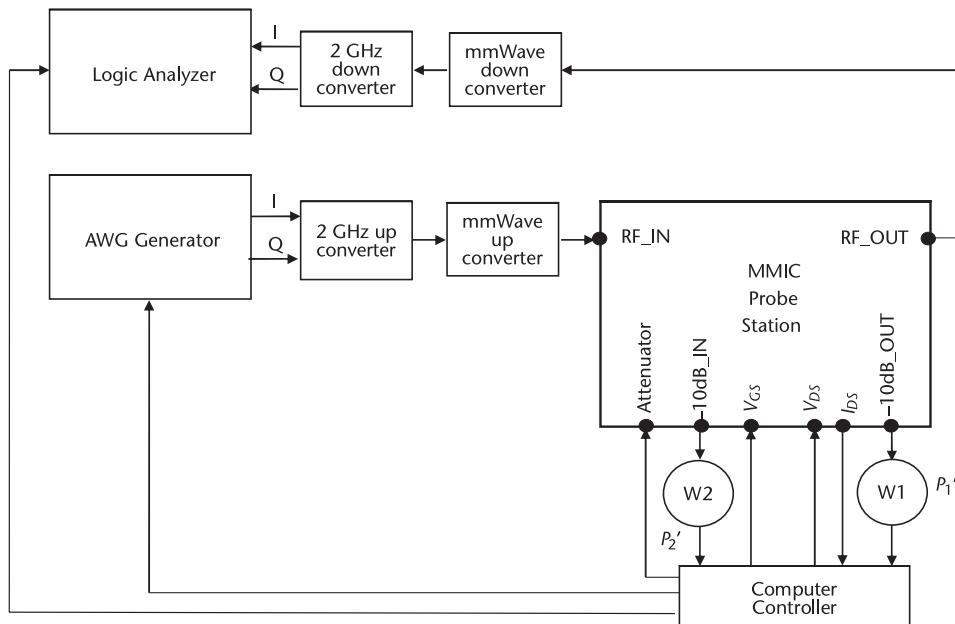
$$\phi = \phi_0 + \Delta\phi(P_{\text{in}}) \quad (\text{B.9})$$

The term corresponds to the amplifier linear response and should be offset from the power results. The offset is obtained by adjusting the phase shifter to make  $P_3 = P_4$ , with the amplifier operating at low levels. It is assumed the phase shifter adjustment is fixed and does not change within the frequency band of interest. That is approximately true for narrowband amplifiers.

The evaluation now is made by sweeping the power within a range large enough to drive the amplifier beyond the point of 1-dB gain compression. The system run will repeat this process for a number of frequencies within the band. The controller will determine the AM to PM at each measured frequency.

## B.4 EVM and ACPR

When EVM started to be popular, the signal waveform was usually generated with MATLAB on a PC. The output signal in the I,Q format was then converted to a single signal on an intermediate frequency and subsequently converted to millimeter waves. The signal was applied to the DUT and the output signal was converted back to the I,Q format. The ACPR and EVM information was then extracted from the measured data by a special PC application program. More recently, the instrumentation



**Figure B.6** ACPR and EVM test.

industry offered the test setup shown in Figure B.6. A special generator called the Arbitrary Wave Generator (AWG) provides the input signal waveform and the data processing is performed by a Logic Analyzer from the measured data. The DUT is the MMIC probe station from Figure B.1.

The test equipment for the testing of 5G systems is available in the market from major instrumentation companies. For example, Rohde & Schwarz provides signal vector generators and signal analyzers [2]. Keysight offers the PNA-X Network Analyzer that performs the same functions up to 67 GHz [3].

## References

- [1] Danieli, R., et al., “Low Cost AM/AM and AM/PM Characterization Setup Based on Scalar Measurements,” *Proceedings of the 43rd European Microwave Conference*, 2013, pp. 1367–1370.
- [2] Rohde & Schwarz, “5G UE PA R&D Testing,” Application Note 1SL365, July 2020.
- [3] Keysight Technologies, “Create Accurate EVM Measurements with the PNA-X Series Network Analyzer,” [www.keysight.com/us/en/assets/3120-1022/applicationnotes](http://www.keysight.com/us/en/assets/3120-1022/applicationnotes), January 2020.

## About the Author

**Edmar Camargo** received his master's and PhD degrees from the University of São Paulo, Brazil, in 1976 and 1985, respectively. Within this time, he took a leave of absence to work at the Centre National d'Études des Telecommunications (CNET) in Lannion, France, in 1977 and 1982. He was a teacher assistant and research engineer in the same university in Brazil until 1993, when he emigrated to the United States. Dr. Camargo worked for Hewlett-Packard on millimeter-wave transceiver design and for Fujitsu Compound Semiconductor Inc., where he took the lead on frequency converter projects, in particular, the patented FMM5107 for satellite receivers and high linearity millimeter-wave mixer FMM5116/17. From 2000 to 2004, he was the director of engineering at Fujitsu, coordinating the millimeter-wave and handset developments. From 2005 to 2009, Dr. Camargo worked at iTerra Communication, Watkins Johnson Communications, on power amplifiers for infrastructure applications and at RF Micro Devices on power amplifiers for handsets. From 2009 to 2012, was an MMIC design consultant in the San Francisco Bay Area, and in 2013 he became a principal engineer at QuinStar Technology in Torrance, California. He retired from QuinStar in 2017 and has since worked as a consultant. Dr. Camargo is a senior member of the IEEE-MTT Society and has served on the technical symposium committees from 1996 to 2008 and from 2015 to 2017. He has also served as a member of the MTT-22 Signal Generation and Frequency Conversion and is currently in the Coastal Los Angeles Chapter of the MTT. He and his wife, Marcia, reside in Lomita, California, and have two sons, Marcel and Regis, and three granddaughters, Maeve, Chloe, and Nia.



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EM, short for electromagnetic, 11  
EVM, error vector measurement, 90

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GaN HEMT, gallium nitride HEMT, 1  
GaN DHEMT, gallium nitride double hetero junction HEMT, 24, 25  
GEO, geosynchronous equatorial orbit, for satellites, 4

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 HPA, High power amplifier, 3

**I**

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 $I_{D\text{MAX}}$ , maximum drain current, 26  
 $I_{DSS}$ , drain-source current at  $V_{GS} = 0$ , 26  
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 IMR<sub>3</sub>, ratio of intermodulation to the fundamental component, 88  
 InAlGaN, indium aluminum nitride, 26  
 Inductor as a shunt short stub, 140  
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 IP<sub>3</sub>, intercept point third order products, 88  
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 MEMS switch, micro electro-mechanical system, 4  
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 MMMIC, monolithic mmWave integrated circuit, 2  
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RT, RLC resistance at the resonance frequency,  
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RX, receiver, 4

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$S$ , spacing between coupled lines, 21

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SiC, silicon carbide, substrate for the GaN layers  
and passive layers, 1

SiGe, silicon germanium semiconductor, 9

SiN, silicon nitride dielectric material, 15

SiO<sub>2</sub>, silicon dioxide dielectric material, 15

SLOT, short-open-load-through, calibration  
technique, 35

SSG, small signal gain, 39

SPDT, single pole double throw, for a switch, 7

SSPA, solid state power amplifier, 4, 161

Stability factor

$\mu$ -factor, 37

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## T

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TC, temperature coefficient, 32

$T_{\text{chan}}$ , channel temperature, 31

TEM, transverse electrical mode, mode of  
propagation, 12

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Thin film, 12

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34

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