# The Use of Spreadsheets in Packaging Thermal Calculations

Tutorial
Semitherm-XIV
San Diego

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### **Outline**

#### **Overview**

#### Analytical formulas for 1-D and 2-D heat flow

- Conduction
- Conduction + constant heat transfer coefficient

#### Package environment

- Representation of test board
- Calculation of heat transfer coefficient

#### Thermal resistance network

Numerical solution: non-linear boundary conditions

#### **Spreadsheet structure**

**Case studies** 

**Summary and Conclusions** 



## **Examples of Plastic Packages**

#### **MQFP**



#### **SuperBGA®**



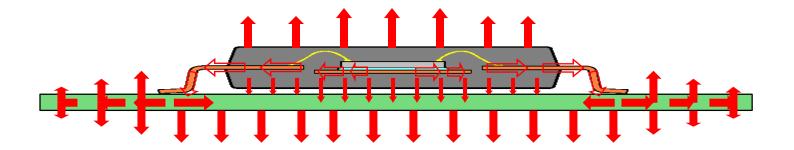
#### Layered structures

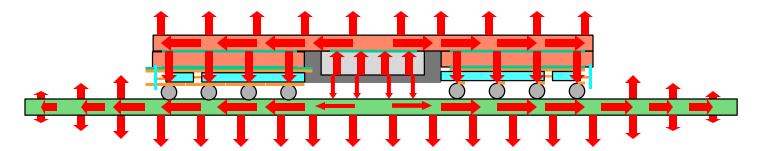
- High conductivity metals
- Low conductivity dielectrics
- Lateral dimensions much greater than thickness

## **Heat Flow in Plastic Packages**

#### **Heat Flow Patterns**

- In-plane flow in metals
- Thru-plane flow in dielectrics





## **Approach to Analytical Modeling**

In plastic packages, complicated heat flow patterns can be reduced to a series of heat flow building blocks that can be arranged in a thermal circuit diagram



#### **Definition of Thermal Resistance**

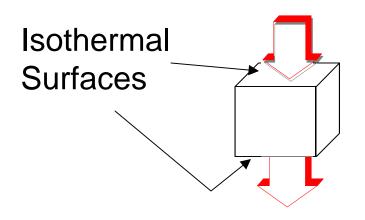
$$\Theta = \frac{T_A - T_B}{P_{AB}}$$

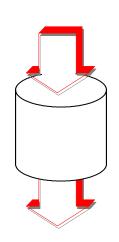
 $T_A$ ,  $T_B$  = Temperatures of isothermal surfaces

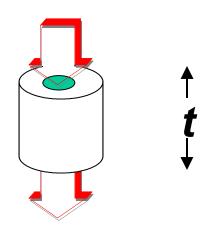
P<sub>AB</sub> = Total thermal energy flowing between these surfaces per unit time



### 1-Dimensional Heat Flow







**Examples:** 

Die **Die Attach** 

**Bond Wire** 

Via

Block

$$A = L \times W$$

Cylinder

$$A = p r^2$$

Hollow Cylinder

$$A = p \times (r_{Outer}^2 - r_{Inner}^2)$$

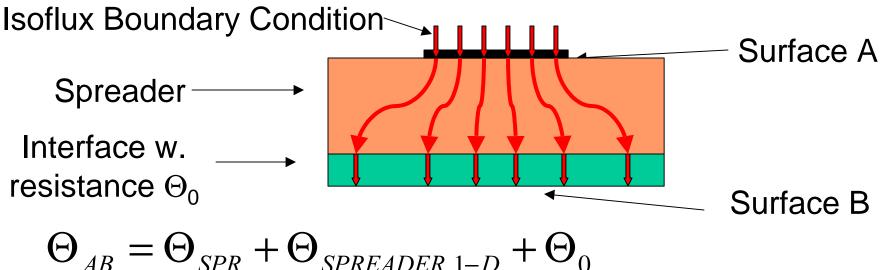
A = Cross-Sectional Area

 $\kappa$  = Thermal Conductivity

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## 1-Dimensional Heat Flow with Spreading Resistance Correction



Where: 
$$\Theta_{SPR} = \frac{\sqrt{A_{SPR}} - \sqrt{A_{SOURCE}}}{k_{SPR}\sqrt{p} A_{SPR}A_{SOURCE}} \times \frac{\text{lk}_{SPR}A_{SOURCE}\Theta_o + \tanh(\text{l}_{SPR})}{1 + \text{lk}_{SPR}A_{SPR}\Theta_o \tanh(\text{l}_{SPR})}$$

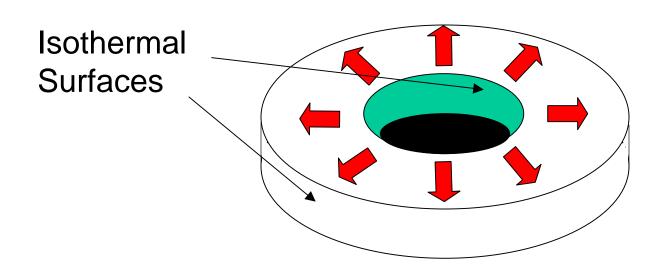
 $\Theta_0$  = Boundary or Conduction Thermal Resistance, and

[Ref: Seri Lee, "Calculation Spreading Resistance in Heat Sinks," Electronics Cooling Magazine, Vol. 4, No. 1 (Jan., 1998), pp. 30 - 33]

$$I = \frac{p^{3/2}}{\sqrt{A_{SOURCE}}} + \frac{1}{\sqrt{A_{SPR}}}$$

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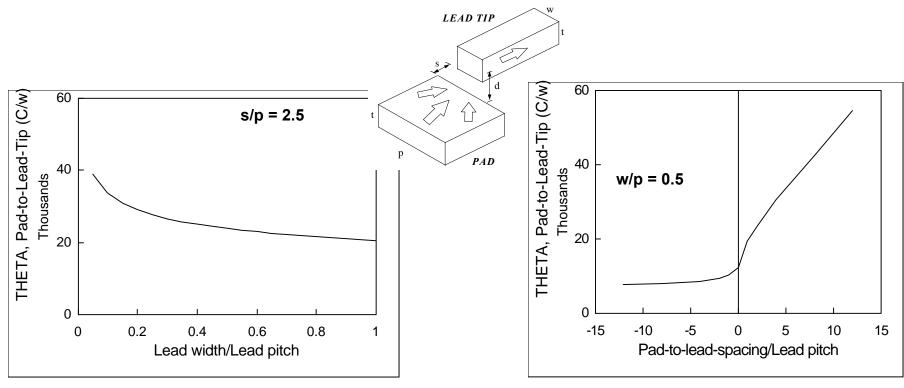
### 2-Dimensional Heat Flow



$$\Theta = \frac{1}{2pk t} \ln \left( \frac{r_{OUT}}{r_{IN}} \right)$$



## FEA Solution: Pad-to-Lead Thermal Resistance



(a) Dependence on w/p

#### (b) Dependence on s/p

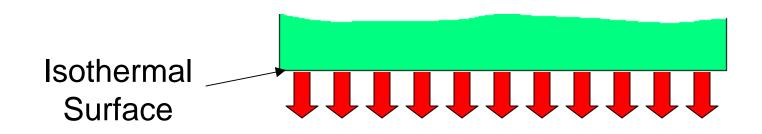
L/F thickness=0.15 mm, d=0.2 mm, p = 0.25, k(m/c)=0.6 w/m-K, k(L/F)=390 w/m-K

[Reference B. S. Lall, B. M. Guenin, R. C. Marrs, and R. J. Molnar, "Parametric FEA Thermal Model for QFP Packages," *Proceedings, SEMI-THERM XII Conference*, March, 1996, pp. 105-110.]

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# Heat Transfer From Constant Temperature Surface



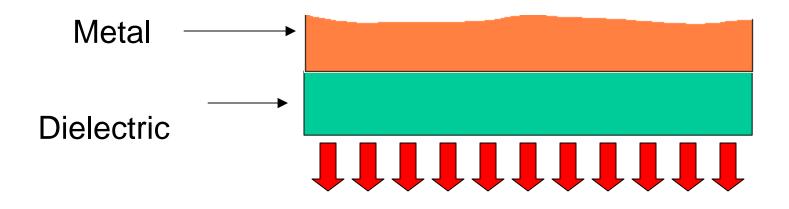
$$\Theta = \frac{1}{hA}$$

h = Heat Transfer Coefficient A = Surface Area



# Heat Transfer to Ambient from Composite: Derating h

Temperature of metal may vary locally



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$$h_{EFF} = \frac{hK_{DIELECTRIC}}{k_{DIELECTRIC} + ht_{DIELECTRIC}}$$

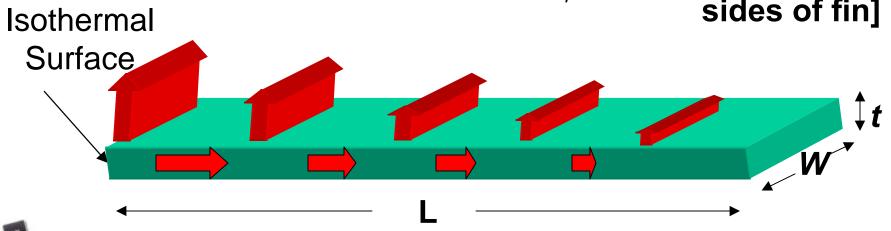
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## 1-D Distributed Conduction/ Convection/Radiation (Finite Fin)

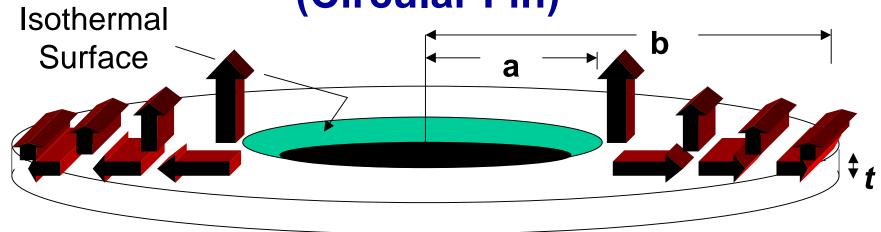
$$\Theta = \frac{a}{hW} \times \frac{e^{aL} + e^{-aL}}{e^{aL} - e^{-aL}}$$

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 $a = (2h/kt)^{1/2}$  [For h on both sides of fin]



## 2-D Distributed Conduction/ Convection/Radiation (Circular Fin)



$$\Theta = \frac{1}{2p \, ak \, ta} \left( \frac{K_1(a \, b)I_0(a \, a) + I_1(a \, b)K_0(a \, a)}{I_1(a \, a)K_1(a \, b) - I_1(a \, b)K_1(a \, a)} \right)$$

Where  $\alpha = (2 \text{ h/kt})^{1/2}$  [For h on both sides of fin]

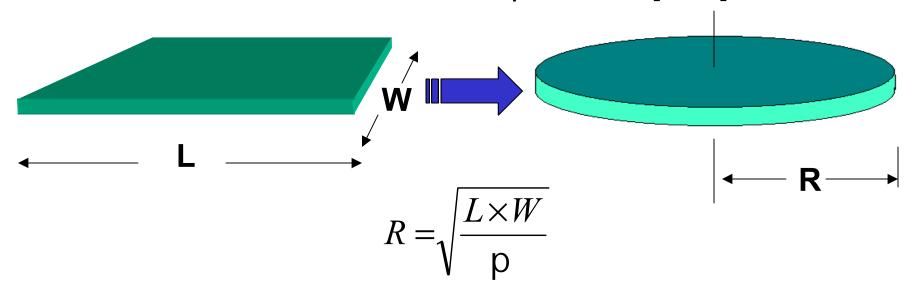
 $I_0$   $I_1$  ( $K_{0,}$   $K_1$ ): modified Bessel functions of the 1st (2nd) kind, order 0 and 1

**Reference:** B. M. Guenin, R. C. Marrs, and R. J. Molnar, "Analysis of a Thermally Enhanced Ball Grid Array Package," *IEEE Trans. Comp., Packaging, Manuf. Technol.* - Part A, Vol. 18, No. 4, December 1995, pp. 749-757.

## 2-D Heat Flow: Transform Rectangular to Circular Geometry

#### Transform rectangle into circle

- Equal area and thickness
- 1-D, 2-D, and Circular Fin problems [Ref.]



**Reference:** B. Lall, A. Ortega, and H. Kabir, "Thermal Design Rules for Electronic Components on Conducting Boards in Passively Cooled Enclosures," *Proceedings, Fourth InterSociety Conference on Thermal Phenomena in Electronic Systems*, May, 1994, pp. 50-61.]

### **Heat Transfer Coefficient**

$$h_{T} = (h_{NC}^{3}(W,T) + h_{FC}^{3}(W,V_{AIR}))^{1/3} + h_{RAD}(T)$$

#### **h**<sub>T</sub> = Total Heat Transfer Coefficient

- Predicts heat loss to ambient in industry-standard windtunnel environment
- Deals with natural, mixed, and forced convection regimes
- Includes effect of radiation

#### **References:**

1) H. Shaukatullah, M.A. Gaynes, and L.H. White, "A Non-dimensional Correlation for the External Thermal Characteristics of Surface Mount Metal Quad Flat Packs," *Proceedings of the 4th Intersociety Conference on Thermal Phenomena in Electronic Systems*, 1994, pp. 237-244.

2) B. M. Guenin, A. Chowdhury, R. Groover, and E. J. Derian, "Analysis of Thermally-Enhanced SOIC Packages," *Proceedings, SEMI-THERM XII Conference*, March, 1996, pp. 1-13.

## **Heat Transfer Coefficient (Cont.)**

$$h_{NC} = 8.66 \left( \frac{\Delta T_{Surface Air}(^{\circ}C)}{D_{CHAR}(mm)} \right)^{0.25} W / m^{2} \circ C$$

$$h_{FC} = 119.9 \left( \frac{V_{AIR}(m/s)}{D_{CHAR}(mm)} \right)^{0.5} W/m^2 \circ C$$

$$h_{RAD} = 5.67 \times 10^{-8} \, \mathrm{e} \left( \frac{T_{Surface}^{\phantom{Surface}}(K^4) - T_{Air}^{\phantom{Air}}(K^4)}{T_{Surface}(K) - T_{Air}(K)} \right) \quad \begin{array}{l} n_{\mathrm{NC}} \text{ assumes nonzontal orientation} \\ D_{\mathrm{CHAR}} = \mathrm{Characteristic} \\ \mathrm{Dimension} \end{array}$$

Assumes simple, standard package, board configuration

- Single package mounted centrally on test board
- h<sub>NC</sub> and h<sub>FC</sub> are area averages

h<sub>NC</sub> assumes horizontal board

Dimension

 Set equal to package width in direction of air flow

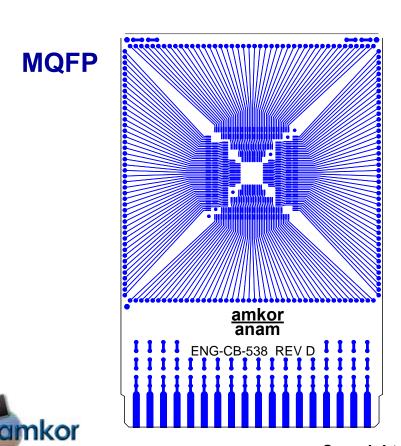
#### References:

**h**<sub>EC</sub>:G.N. Ellison, Thermal Computations for Electronic Equipment, Krieger Publishing, Malabar, Florida, 1989.

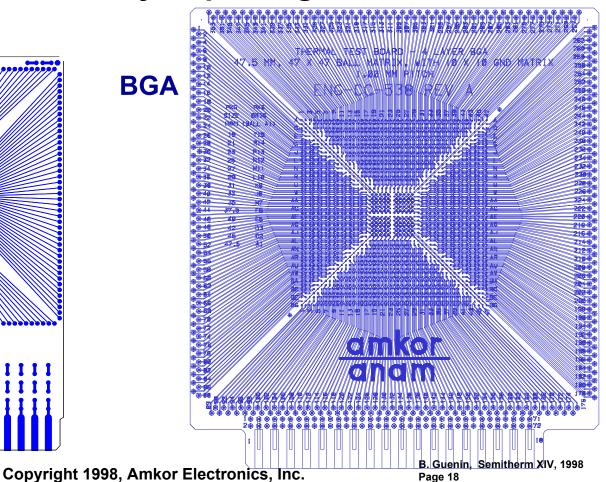
h<sub>NC:</sub> B. S. Lall, B. M. Guenin, R. C. Marrs, and R. J. Molnar, "Parametric FEA Thermal Model for QFP Packages," *Proceedings, SEMI-THERM XII Conference*, March, 1996, pp. 105-110.

## **Examples of JEDEC-Standard Thermal Test Boards**

Both boards shown are nested designs, to accommodate a variety of package sizes

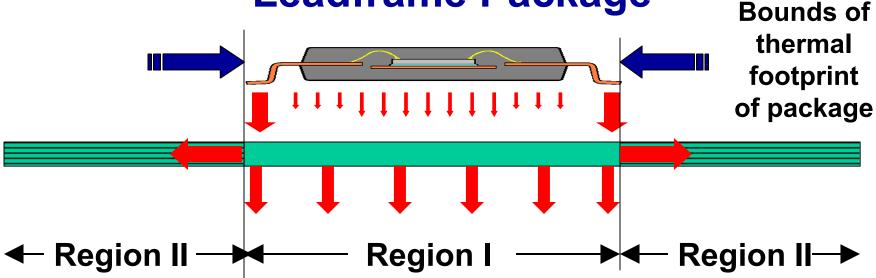


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Representation of Test Board:

Leadframe Package



Region I represented as a Control Volume

- •No internal thermal gradients
- •Transmits heat to convective surface under footprint and to Region II

Region II represented as

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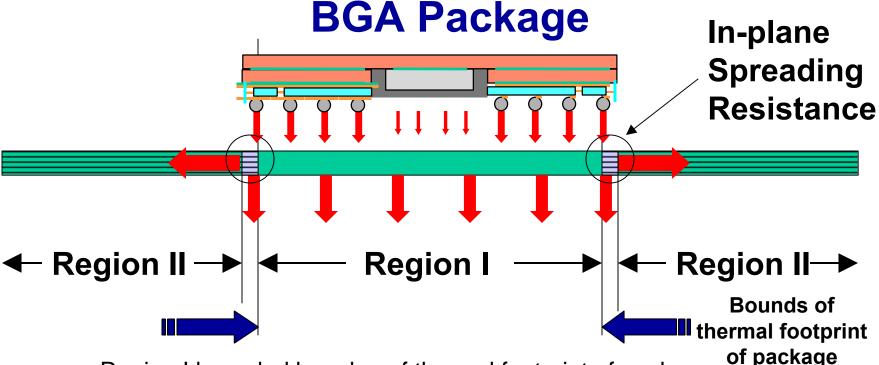
- •A circular fin (for boards containing internal planes
- •4 parallel finite fins (for single-layer test boards)

**Reference:** B. M. Guenin and D. Mahulikar, "Methodology for the Thermal Characterization of the MQUAD® Microelectronic Package," *Proceedings, SEMI-THERM IX Conference*, February, 1993, pp. 176-185.

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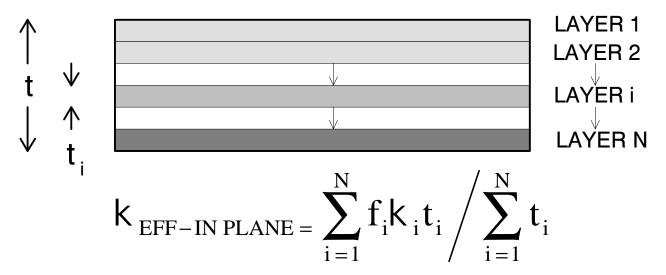
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Representation of Test Board:



- •Region I bounded by edge of thermal footprint of package
- Region II bounded by edge of package
- •When thermal footprint < package width, in in-plane spreading resistance is placed in series with heat flow from Region I to II.
- •Functional form of spreading resistance depends on board construction:
  - •2-D circular heat flow (for boards containing internal planes)
  - •4 parallel 1-D heat flow paths (for single-layer test boards)

## Calculating Thermal Conductivity of Test Board



 $\mathbf{f_i}$  is the fractional coverage of copper in layer  $\mathbf{i}$   $\kappa_i$  and  $\mathbf{t_i}$  - thermal conductivity and thickness For application boards, only include planes in calculation [Ref.]

**Reference:** K. Azar and J.E. Graebner, "Experimental Determination of the Thermal Conductivity of Printed Wiring Boards," *Proceedings, SEMI-THERM XII Conference*, March, 1996, pp. 169-182.

## **Definition of a Spreadsheet**

#### Mathematical, financial, engineering software

- Table structure
- Cells can contain

Text

**Numbers** 

**Formulas** 

Formulas

Result is output in cell in which formula is located Inputs come from other cells through linking

C	A	В	C	D	E	F	G	Н
1	1-Dimensional Hea	at Flow Calcu	ılation					
2	COMPONENT	MAT'L	WIDTH	LENGTH	THICKNESS	TH.COND/	Theta \	
3			(mm)	(mm)	(mm)	(w/mm-°C)	(°C/W)	
4	Die	Si	12	12	0.61	0.092	0.91	
5						_		
6								
7								

+E4/(F4\*C4\*D4)

### **Capabilities of Spreadsheets**

Advanced mathematical and engineering functions

Macro (programming) languages

**Graphing capabilities** 

**Data table formatting** 



## **Special Functions in Spreadsheets**

#### Partial Listing (Lotus 5.0 and Excel 97)

- Bessel Functions, Std. And Modified 1st and 2nd Kind
- Beta and Incomplete Beta Function
- Error and Complementary Error Functions
- Gamma and Incomplete Gamma Function
- Exponential Function
- Natural Logarithm
- Common Logarithm (Base 10)
- Trig and Inverse Functions
- Hyperbolic Trig and Inverse Functions
- Complex Variable Analysis
- Statistical Functions

#### **Additional Functions (Excel 97)**

Fast Fourier Transform



## Motivation for Analytical Resistor Models

Promotes a high level of insight into how thermal performance of a package is related to its design

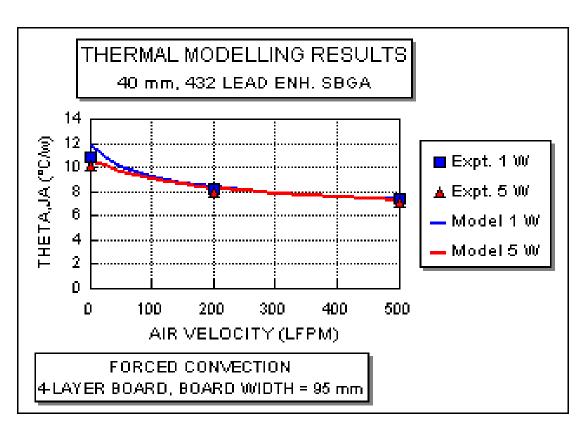
 Each package component individually represented in thermal circuit diagram

Can produce accurate, rapid solutions.

Readily incorporates non-linear boundary conditions.



## **Solution Accuracy**



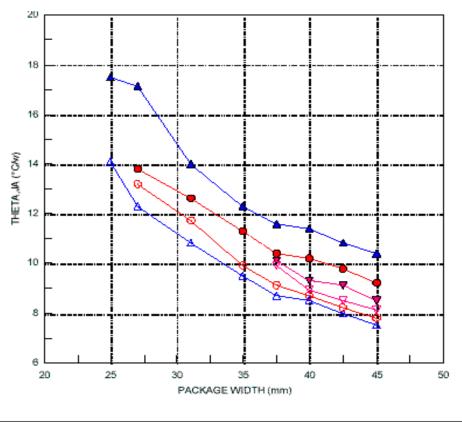
#### **Model Curves**

- •15 points each
- •10 sec/point
- •Calculation completed in 5 min on 120 MHz Pentium

Accurate solution in natural, mixed, and forced convection regimes

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## **Solution Productivity**

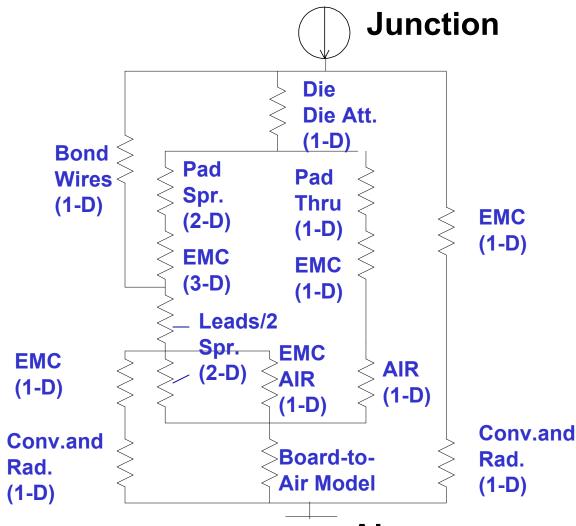


34 SBGA package designs analyzed in under 2 hours

- Natural convection
- $\Delta T_{JA} = 60$ °C
- Multilayer test board

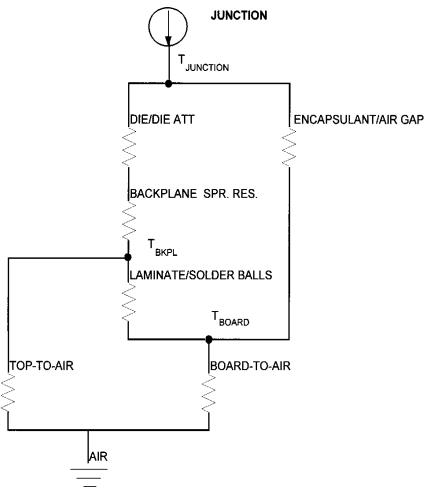


# Thermal Circuit Diagram for MQFP Package



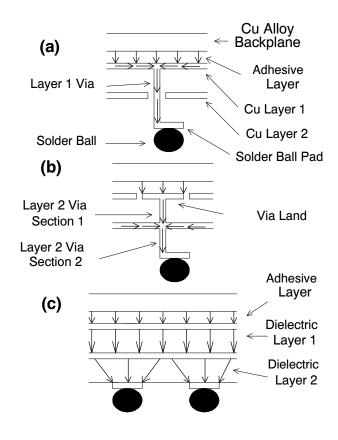
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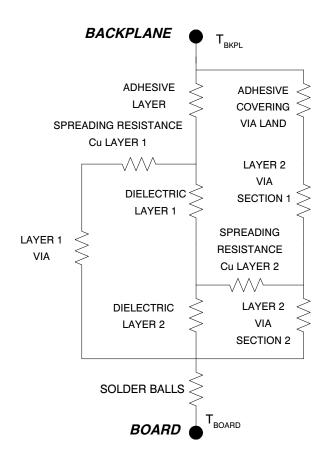
# Thermal Resistor Network for SBGA Package





## Submodel to Calculate Thermal Resistance of Laminate







## Solution of Thermal Resistance Network

## Use successive approximations technique to solve for

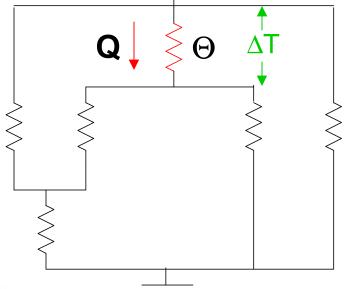
- Temperatures on all surfaces with temperaturedependent heat transfer coefficients
- Simplify resistance networks by eliminating current loops: solution of equivalent resistors
- Size of thermal footprint of package (PBGA package)



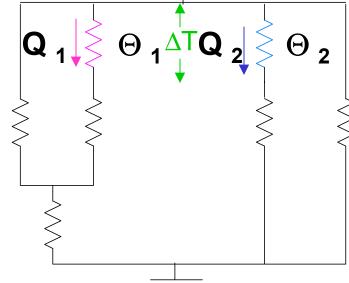
### **Elimination of Current Loops**

To simplify circuit into simple series and parallel resistor networks

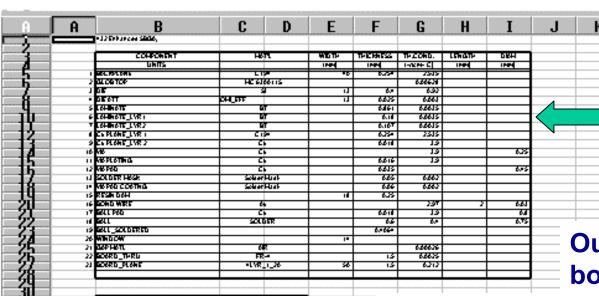
Iterate f until  $\Delta T$  across  $R_1$  and  $R_2$  is the same as across R



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### Structure of Spreadsheet



IPP

hø

LEVOCOUNT BULL PITCH

BOLL HOTEIX

MUHROWS **10186** LVR BOSED

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list, materials, and dimensions -- given range name:\$tbl\_inputs

Package component

Therm. cond. values from @vlookup link to separate file

Outputs:  $\Theta_{JA}$ ,  $\Theta_{JC}$ , board conductivity, heat transfer coefficient

**Package** parameters

	INTUIS				_			currurs	$-$ / $^{\prime}$		
BOARE PROPERTE	MEDITOREMONS		RACHAGERARAMETERS		BONE PROPERTY						
TARC	V.E.TII	POV.TEX IWI	UDBH UBBH	MMD.T	1 CH1	THETA LC	1,000	TILCOLE.	TIIK.	NCORN Harrist	N, TOTAL I-mer244
IVE_SCI_IS_SE_IJIS	2 2	5.75	6	8	163	65	(6) (2)	10.7	16	13	113
LVR_35_1_16_36_1_16 LVR_35_1_16_36_106	- %	5.5 5.75	i	ŝ	163	6.5	65.2	18.7	15	13	10.2
LVR_35_1_16_36_1_166 LVR_35_1_16_36_1_166	*	635	6	8	16.4	65	199	16.7	15	13	10.1
	+				_						

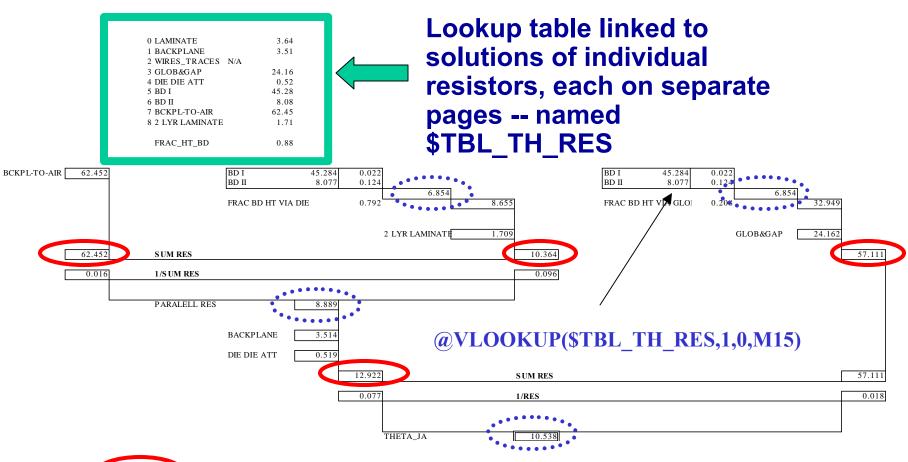
Application-specific inputs: board type, power, air velocity,... We re Packaging the Futu

## **Example of Thermal Resistance Calculation: Circular Fin**

G	A	В	С	D	E	F	G
1			INPUTS			LOCAL	
3		Components	INPUIS			OUTPUTS	
		COMPONENT	Typo	THICKNESS	TH.COND.	OUIFUIS	
5		COMPONENT	Туре		(w/mm-°C)		Value of Width obtained by
6		Board	LYR_1S_1_20_2P_1_100		2.50E-02		linking to table on input page
7		20413	PETA_10_1_20_271_100	1.01	2.002 02		
8		COMPONENT	WIDTH			R,equiv	thru special function:
9			(mm)			(mm)	
10		Package Body	28			15.80	<b>@XINDEX(\$TBL INPUTS,</b>
11							C12,\$B10)
12		COMPONENT	WIDTH			R,equiv	C12,3D10)
13			(mm)			(mm)	
14		Board	50			28.21	
15							
16		Environmental					
17		h					
18		(/V//mm^2-K)					
19		2.00E-05					
20							
21			LC	DCAL OUTPUT	S		
22		Parameter				Value	+@BESSELK(F23*F14,1
23		alpha		<u></u>		0.032	
24		K,1(alpha b)*l,0(alp				1.22	
25		l,1(alpha a)*K,1(alp	qha b) - I,1(alpha	b)*K,1(alpha a	)	-0.63	
26		1/(2 pi a t k alpha)				8.04	(*CM) @BESSELI(F23*F14,1)*
27			GL	OBAL OUTPU	IS		@BESSELK(F23*F10,0)
28		Theta,board-to-air				15.58	(°CM) (CDESSELK(F25 F10,0)



## Spreadsheet Solution of Resistance Network



= Series Resistor Solution

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= Parallel Resistor Solution

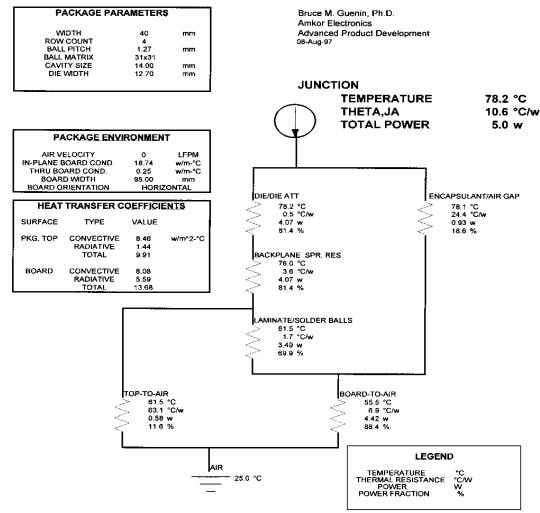
## **Example of Macros to Solve Non- Linear Resistor Network**

MACRO: /ITER_LOOP {FOR \$J\$6,1,50,1,/LOOP}	START STOP STEP 1 50 1/LOOP	COUNTER 9
MACRO: /LOOP {IF MAX_ERROR<0.1}{RETURN} {FOR \$J\$11,1,5,1,/ITER_T_DIE} {FOR \$J\$12,1,5,1,/ITER_T_BOARD} {FOR \$J\$13,1,5,1,/ITER_FRAC_DIE} {FOR \$J\$14,1,5,1,/ITER_FRAC_BD}	START         STOP         STEP           1         5         1 /ITER_T_DIE           1         5         1 /ITER_T_BOARD           1         5         1 /ITER_FRAC_DIE           1         5         1 /ITER_FRAC_BD	COUNTER  1 1 1 1
MACRO: /ITER_T_DIE {LET \$T_BKPL_TRIAL,63.1744} {CALC} {IF 0.0459<0.100}{FORBREAK} {RETURN}	\$T_BKPL_'\$DEL_T_B	
MACRO: /ITER_T_BOARD {LET \$T_BOARD_TRIAL,56.7619} {CALC} {IF 0.0336<0.100}{FORBREAK} {RETURN}	\$T_BOARD\$DEL_T_B 25  \$DEL_T_B 0.1	
MACRO: /ITER_FRAC_DIE {LET FRAC_DIE,0.8162} {CALC} {IF 0.2463<0.100}{FORBREAK} {RETURN}	FRAC_DIE \$DEL_T_J 5000  \$DEL_T_J 0.1	
MACRO: /ITER_FRAC_BD {LET FRAC_DIE_HT_BD,0.8573} {CALC} {IF 0.1156<0.100 }{FORBREAK}	FRAC_DIE_\$DEL_T_B 2500  \$DEL_T_B 0.1	



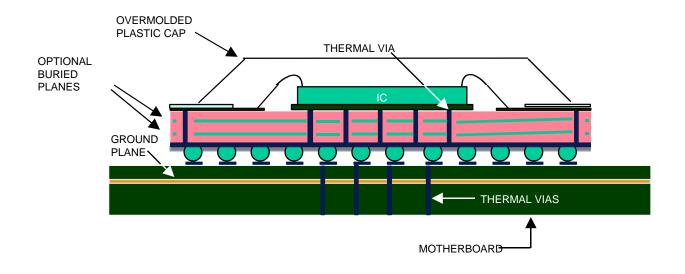
# **Example of Solved Resistor Network: SBGA® Package**

THERMAL RESISTANCE NETWORK FOR 432 LEAD SBGA PACKAGE





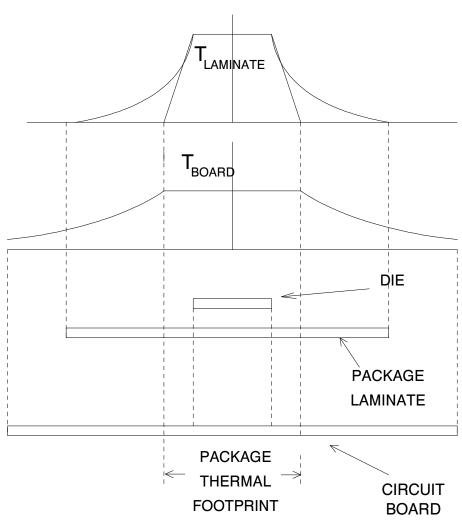
# **Another Example -- PBGA Package**



**Reference:** B. M. Guenin, B. S. Lall, R. J. Molnar, and R. C. Marrs, "A Study of the Thermal Performance of BGA Packages," *Proceedings, International Flip Chip, Ball Grid Array, TAB, and Advanced Packaging Symposium*, February, 1995, pp 37-46.



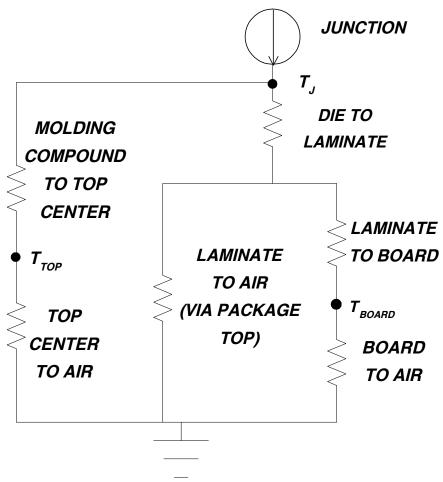
## **PBGA** Temperature Distribution



Size of Package Thermal
Footprint Determined by
Competition Between Heat
Spreading and Heat
Extraction

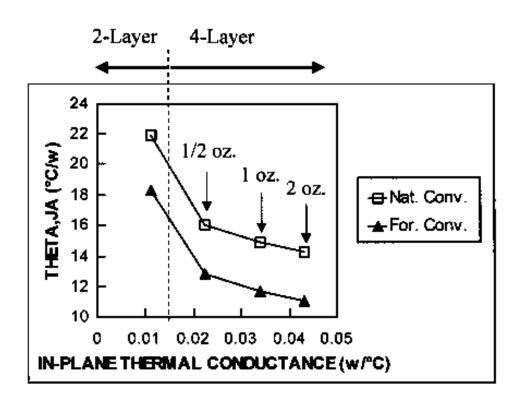


# Thermal Resistance Network for PBGA Package





### **Effect of Laminate Metal Content**



#### **Model Assumptions:**

313 Lead, 35 mm PBGA Pkg.

**Full Matrix Array** 

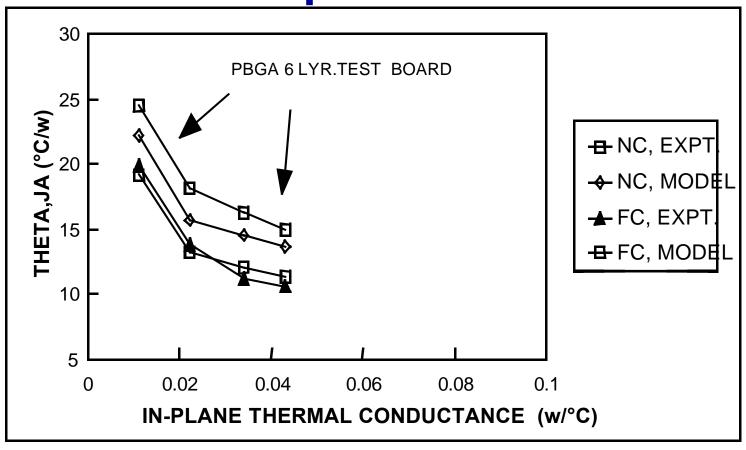
**Natural Convection: 4 watt** 

Forced Convection: 2.5 m/s

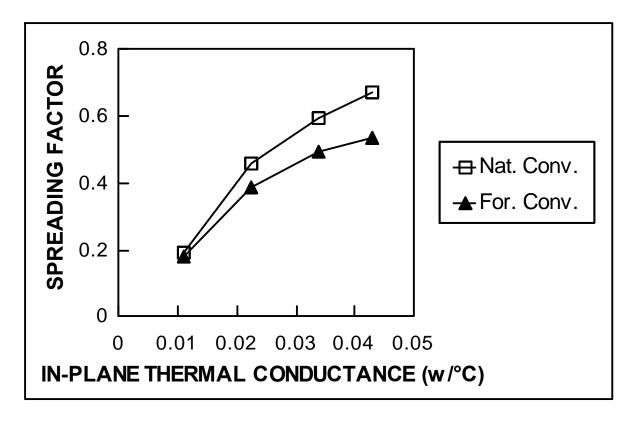
6-Layer Board, 80 mm width



## PBGA Model -- Comparison with Experiment



### **Effect of Laminate Metal Content**



#### **Model Assumptions:**

313 Lead, 35 mm PBGA Pkg.

**Full Matrix Array** 

**Natural Convection: 4 watt** 

Forced Convection: 2.5 m/s

6-Layer Board, 80 mm width

Spreading Factor = 
$$\frac{W_{FOOTPRINT} - W_{DIE}}{W_{PKG} - W_{DIE}}$$

## **Tradeoffs in Modeling Approaches**

Analytical conduction models can adequately predict package thermal performance in simple configurations.

When a package design follows a fixed format, analytical models can be very efficient, justifying the time to develop.

When there are frequent variations in package design, the use of a finite element analysis code is more practical than an analytical approach.

For complicated configurations, dominated by convective heat transfer, a computational fluid dynamics code is most efficient.

### **Summary**

Conduction in leadframe and BGA plastic packages can be described in terms of simple thermal resistive elements, calculated analytically

Convective and radiative heat transfer in a standard thermal test environment can be accounted for using simple analytical expressions

Resistor networks lend themselves to efficient solution of non-linear problems and to rationalizing the thermal performance of a package

Spreadsheets are efficient tools for solving analytical thermal resistance networks