Electronic package characterization per JEDEC standard

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Introduction

With the increase in power density resulting from advancements in semiconductor packaging technologies comes the issue of heat dissipation. Heat is generated as a result of electrical energy being converted to thermal energy during circuit activities. The junction temperature of a chip directly affects the performance of the circuits and the reliability of packages.

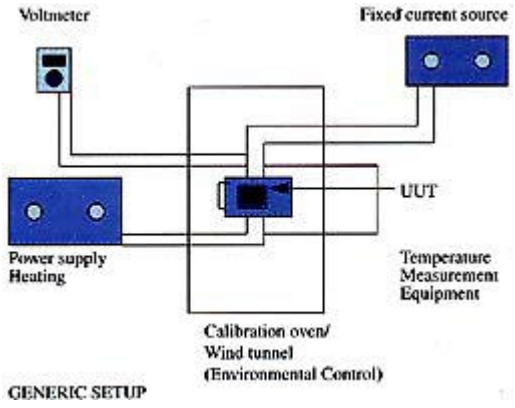

Figure 1: Diagram of electrical test method (ETM)

It is very important therefore that the junction temperature of each package be known as accurately as possible through direct measurement. It is further important that such measurement be repeatable, and comparable to measurements made on other packages since it constitutes a measure of performance. And lastly, it is important that the technique of measurement be universally applied in the industry in order to achieve meaningful and unbiased comparison of similar packages. To this end, the Joint Electron Device Engineering Council (JEDEC), under the Electronic Industries Association (EIA), is creating a thermal measurement standard for IC packages. The Council has recently published the first phase of this standard that is expected to achieve the above goals upon completion.

The purpose of this article is to briefly summarize the essence of this standard, and evaluate some of the issues that are yet to be addressed.

JEDEC Standard

The JEDEC standard is being developed to create a uniform method of characterizing IC packages in order to establish a frame work by which the performances of different packages housing similar devices, or different devices in similar packages, can be compared.

The choice of measurement technique is the electrical measurement method (ETM). ETMs are not new. They involve the use of forward voltage in temperature sensitive devices such as diodes to determine the temperature of the junction. Many companies have been using this method in one form or another, with custom setups or standard available equipment, depending on the sophistication of the user and the complexity of the device. Data from tests using this technique have been well published. Some of them are referenced at the end of this article [1, 2 & 3]. What the JEDEC standard does differently, however, is to clearly recommend specific environmental conditions, measurement techniques, fixturing, heating power guidelines, and specific wiring and connection configurations for both thermal dice and active devices.

A unique aspect of the standard is that it calls out for specific test board design. This design specifies the geometry and contacts of the board based on the number of pins, pin sizes and package body sizes. This is aimed at standardizing the impact of printed circuit boards on the thermal performance of the package itself.

The standard consists of different documents some of which are still being developed. The approved documents to date include JESD51(Overview), JESD51-1(The Electrical Test Method), JESD51-2 (Natural Convection Environment Standard) and JESD51-3 (Low Thermal Conductivity Test Board for Leaded Surface Mount Packages). So far, only surface mount boards have been addressed. The JEDEC JC-15.1 subcommittee which is responsible for developing this standard, is presently working on board specification for through-holes and other packages.

Other documents that are yet to be completed and approved include Infrared Test Method, ETM Implementation, Forced Convection, Heat Sink, High Conduction Thermal Test Boards, Resistive Heating Thermal Test Die, Active Device Thermal Test Die, and Thermal Modeling. The list may grow in the future to accommodate inputs from the industry and changes in packaging technologies.

Industry Review

Since the approval of the first phase of the standard, reviews have been very positive. Most of the major semiconductor companies have either started to use it or are gearing up to comply. There have also been some issues raised by some potential users of the standards. The JEDEC-JC15 Committee plans to address most of them in subsequent developments of the standards, but we can look at a few of them now.

Issues Raised on Standard

The issues discussed herein are from the author's personal experience in designing to the standard and from questions raised by colleagues in the industry:

1. Relevance to non-JEDEC packages

Should non-JEDEC package designers worry about this standard? Since the purpose of the standard is primarily to create a framework against which "different packages carrying similar devices, or similar packages carrying different devices" can be compared and evaluated, it is essentially not package-specific. Thus, the author suggests that in order to give an industry-wide validation to their test data, non-JEDEC packages should also be tested to the same standard.

2. Non traditional packages

Does the standard address complex, advanced packages? The JEDEC committee intends to cover as

many packages as possible in future revisions of the standard. However, for packages that are highly customized and specialized, the test method, wiring configurations, environmental conditions and powering guidelines, can still be applied to comply with the standard. In such cases, the publication of the results must comply with the requirements for data correction and presentation in the standard.

3. Ball Grid Array (BGA) test board design

Overwhelmingly most of the questions have been on this topic. In their publication: "Thermal Resistance Characterization of the 225 BGA" 4, John Pursel and Tom Tarter discuss some of these issues. The standard is very clear on single layer test boards.

However, the committee has not yet addressed the issue of multiple layer printed circuit boards (PCB's). The design of these boards pose special challenges, especially BGA test boards. Depending on the number of balls and the ball pitch, the PCB can quickly get very complicated. BGAs are a special case because the PCB is very critical to the cooling of the package, particularly in plastic BGAs because the board is the principal means of removing heat from these packages.

The issue is how to standardize BGA test boards. An important use of thermal data is to enable System Designers to predict the thermal performance of their systems. Since the chip vendor cannot predict the board designs of all possible users, the vendor will like to evaluate the package itself, as independent from the influence of the board as possible. To achieve this, some companies use the absolute minimum number of layers that the design will allow. This is the vendors's perspective for worst case. However, from the users' perspective, the setup should reflect actual operating conditions, especially if this is significantly different from the vendor's test conditions. Lastly, there is cost. Trying to reduce the layers to a minimum often involves having to use minimum trace widths and air gaps. In the PCB industry, any trace width less than 6 mils could exponentially increase the cost of fabrication; therefore, even from the vendor's perspective, the choice of design must also reflect the cost of fabrication. The question then is: which perspective should be used in obtaining test results for publication and comparing with similar device/package performances? The JEDEC Committee might consider the minimum layer approach using standard trace widths and air gaps, and no thermal enhancements such as thermal vias, for the Vendors' Perspective Test (VPT). For a System Designer who wants to evaluate his package for operational conditions, this may be unrealistic. To design for a User Perspective Test (UPT) the board must reflect the user's operating specification.

JEDEC is still working on finalizing this aspect of the standard. In anticipation of some of these issues the standard calls out for a "complete statement of test conditions and environmental conditions" for presentation of thermal data to be complete and meaningful. What JEDEC may consider as most critical could be that the instrumentation be set up properly, the Device Under Test (DUT) be designed to spec, the test be performed exactly as specified, and all non-specified parameters be clearly documented and published with the result such that the test can be repeated by another person.

Test Methodology

The JEDEC JC-15. ETM (Electrical Test Method) application can be dynamic or static. Dynamic Mode involves switching from electrical parameter measurement condition to a heating condition during which power is applied to the DUT for a specific period of time, and then switching back to the temperature-sensitive electrical parameter measurement. Static mode involves heating the package to steady state and then making temperature measurements.

The temperature sensitive electrical parameter usually takes the form of a voltage drop across a forward biased diode designed into the DUT which could be a thermal die or an active device. The measurement current for this diode is selected carefully, so that it is large enough to be reliably measured, but low enough not to create significant package heating. This current often ranges from 100µA to 5mA. Thermal dice may contain multiple diodes, strategically located to monitor the temperature of different parts of the die. These chips are also specifically designed to provide uniform heating for the purpose of measuring the thermal resistance of the package. When measuring thermal resistance, total heating over the die surface should be in compliance with standards of the Semiconductor Equipment Manufacturers International (SEMI)#G46-88 and EIA-JEDEC standards.

Thermal measurement involves initial calibration of the thermal dice in a steady, uniform temperature environment such as a liquid bath or a tightly controlled small oven. Calibration is done by measuring the electrical parameters of the measurement diode, such as the forward voltage, at a known temperature. Measurements of voltages at different temperatures are then made (at least two points) to obtain a proportionality constant, K(□T/□V, the chip calibration factor.) as shown in fig 2.

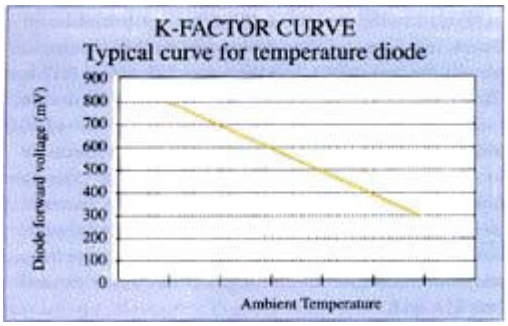

Figure 2 K-factor curve

The device is then placed in still air within a specific size box (defined in the standard,) or environment of known air velocity and temperature (yet to be defined in the standard). Junction temperature in this known environment is determined by measuring the diode forward voltage and using Equation (1) to determine the junction temperature first with no power to the device, and then with the device powered up.

$$K = \Delta T_J \, \Delta T_{Sp} \quad (1)$$

Where ΔT_J *= change in junction temperature*

ΔT_{Sp} *= change in electrical parameter* $K = \Delta T_J \, \Delta T_{Sp}$ *Constant*

The sequence of powering and taking measurement partially depends on the type of test being performed (static or dynamic). Thermal resistance (or impedance, for dynamic test) is the ratio of the difference between the junction and a reference temperature, to the power added as shown in Equation (2).

$$\Theta_{Jx} = \frac{\Delta T_j}{P_H} \quad (2)$$

Where Θ_{Jx} = thermal resistance junction to reference

ΔT_j = change in temperature sensitive parameter value

P_H = power dissipation that produced change in junction temperature

The reference temperature could be ambient for $\Theta_{j\text{-}a}$, case temperature for $\Theta_{j\text{-}c}$ or board temperature for $\Theta_{j\text{-}b}$. If significant heating of the ambient air occurs as a result of powering up the device, the temperature change should be factored into the equation as outlined in the JEDEC standard. Reference 1 contains more discussions on the ETM.

Equipment that can automatically perform this test is available in the market. There are also companies that design and supply the JEDEC Thermal Test Boards and perform the tests.

Conclusion

This standard is a very welcome step towards creating uniformity in the characterization of packages. The review of the standard so far confirms this fact. Package thermal performance is becoming increasingly significant as chips become faster and packages get denser. All the more reason to establish a universal method of measuring this important aspect of electronic packaging.

The approved documents and information on the others, questions about the standard, details of data collection, integrity and accuracy can be obtained by contacting the Electronic Industries Association (EIA), 2500 Wilson Blvd., Arlington, Virginia 22201, USA. The JEDEC JC15 Committee also encourages inputs in the form of comments, suggestions, or desire to participate in the shaping of the standard.

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