McGill University
ECSE 425
COMPUTER ORGANIZATION AND ARCHITECTURE
Fall 2011
Midterm Examination

10:35-11:25, October 12th, 2011

Duration: 50 minutes

- **Write your name and student number in the space below. Do the same on the top of each page of this exam.**
- **The exam is 11 pages long. Please check that you have all 11 pages.**
- **There are four questions for a total of 100 points. Not all parts of all questions are worth the same number of points; read the whole exam first and spend your time wisely!**
- **This is a closed-book exam. You may use one double-sided sheet of notes; please turn this sheet in with your exam.**
- **Calculators are permitted, but no cell phones or laptops are allowed.**
- **Clearly state any assumptions you make.**
- **Write your answers in the space provided. Show your work to receive partial credit, and clearly indicate your final answer.**

Name: _____

Student Number: _____

Q1: _____ **Q3:** _____

Q2: _____ **Q4:** _____

Name: ID:

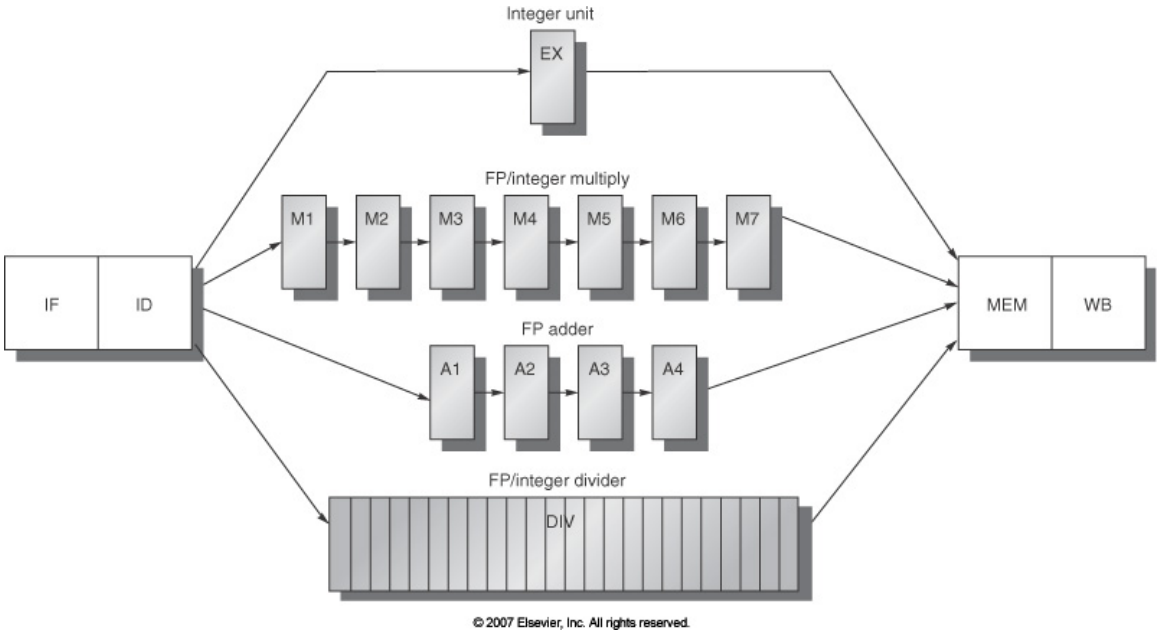
Total:

Name: ID:

Question 1: MIPS Floating Point Pipeline (30 pts) Consider the following loop that computes the dot product of two vectors.

```
Loop:  L.D      F2, 0(R1)
       L.D      F4, 0(R2)
       MULT.D   F2, F2, F4
       ADD.D    F0, F0, F2
       DADDUI   R1, R1, #8
       DADDUI   R2, R2, #8
       SUBUI    R4, R3, R1
       BNEZ     R4, Loop
```

This code will run on the standard MIPS floating point pipeline, illustrated below.



(a) (20 pts) Assume:

- Full hazard detection and forwarding logic;
- The register file supports one write and two reads per clock cycle;
- Branches are resolved in ID;
- Branches are handled by flushing the pipeline;
- Memory accesses take one clock cycle;
- Structural hazards are resolved by giving priority to older instructions.

Fill in the chart on the next page to show the timing of one loop iteration.

Name: ID:

																		Instr.
																		1
																		2
																		3
																		4
																		5
																		6
																		7
																		8
																		9
																		10
																		11
																		12
																		13
																		14
																		15
																		16
																		17
																		18
																		19
																		20
																		21
																		22
																		23
																		24
																		25

(b) (3 pts) If initially R3-R1 = 160, how many cycles are required to execute the loop given the assumptions in part (a)?

(c) (3 pts) What about the MIPS FP pipeline makes maintaining precise exceptions challenging? Give a brief example.

(d) (2 pts) Give two reasons why maintaining precise exceptions is important.

(e) (2 pts) *Briefly* describe one way of extending the MIPS FP pipeline to support precise exceptions.

Name: ID:

Question 2: Loop Unrolling and Code Scheduling (30 pts) Consider the code in Question 1 once more.

```
Loop:  L.D      F2, 0(R1)
       L.D      F4, 0(R2)
       MULT.D   F2, F2, F4
       ADD.D    F0, F0, F2
       DADDUI   R1, R1, #8
       DADDUI   R2, R2, #8
       SUBUI    R4, R3, R1
       BNEZ     R4, Loop
```

(a) (5 pts) Indicate which pairs of instructions have RAW, WAR, and WAW hazards in the above code segment (specify the pair of instructions and hazard type).

(b) (5 pts) Perform register renaming on the above code segment to eliminate as many of the hazards in part (a) as possible without violating true dependencies.

Loop:	L.D	
	L.D	
	MULT.D	
	ADD.D	
	DADDUI	
	DADDUI	
	SUBUI	
	BNEZ	

(c) (20 pts) Unroll the loop as many times as necessary to schedule it without any delays (you need not decompose the loop into two loops with different termination conditions, as a compiler would). Assume the branch delay is managed using a delayed branch slot. Show your unrolled, scheduled loop. How many clock cycles are required to do the work of a single iteration in the original loop?

Assume the pipeline latencies and initiation intervals in the table below.

Functional unit	Latency	Initiation interval
Integer ALU	0	1
FP add	3	1
FP multiply	6	1
FP divide	24	25

Name: ID:

Additional page for Question 2

Question 3: Amdahl's Law, Cost, and Yield (20 pts)

Three enhancements with the following speedups are proposed for a new architecture: S_1=2, S_2=8, S_3=32. The enhancements are mutually exclusive, and may be applied 40%, 20% and 10% of the time, respectively.

(a) (10 pts) What is the best speedup that can be achieved using any pair of enhancements?

(b) (10 pts) Unenhanced, the architecture requires 200 mm^2. Enhancements 1, 2 and 3 increase the area of the processor by 10, 25, and 100 mm^2 respectively. When multiple metrics are important, we can combine them to determine the best possible trade-off. Determine which pair of enhancements strikes the best trade-off in performance improvement and yield by maximizing the objective function:

$$\text{Speedup} \times \text{Yield}.$$

Assume that wafer yield is 1, defect density is 0.04/cm^2, and $\alpha = 4$.

Name: ID:

Additional page for Question 3

Name: ID:

Question 4: Branch Prediction (20 pts) Consider a simple program with one branch. Given the different predictors and the following sequence of branch outcomes, complete the tables below.

(a) (10 pts) What is the branch prediction accuracy of a 1-bit predictor? Assume all predictor state is initialized to "not taken," or N.

Prediction	Outcome	Update
N	T	
	T	
	T	
	N	
	T	
	N	
	T	
	T	
	T	
	N	
	T	
	N	

(b) (10 pts) What is the branch prediction accuracy of a (1, 1) correlating predictor? The branch history register (BHR) is used to store the direction of the last branch. Assume all predictor state is initialized to "not taken," or N.

Pred.: last branch N	Pred.: last branch T	BHR	Pred.	Outcome	Update: last branch N	Update: last branch T
N	N	N		T		
				T		
				T		
				N		
				T		
				N		
				T		
				T		
				T		
				N		
				T		
				N		

Extra blank page