YANJUN YANG

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EDUCATION

The University of Edinburgh Sept, 2022 - present
PhD Candidate, IMNS *Edinburgh, Scotland*

- Supervisors: Alex Serb, Themis Prodromakis
- Research theme: Cognitive processing system implementation based on memristor associative memory

Nanyang Technological University Aug, 2021 - Aug, 2022
MSc (Electronics) *Singapore*

- Core units taken: Digital Integrated Circuit Design, Electromagnetic Compability Design, Genetic Algorithms and Machine Learning, Advanced Wafer Processing, Integrated Circuit Packaging

Tongji University Sept, 2017 - July, 2021
BEng. in Electronic Science and Technology *Shanghai, China*

- Core units taken: Design and Analysis of Digital Integrated Circuits, Computer Architecture, Principles for Design of Integrated Circuit Chips, Embedded Systems

CURRENT PROJECTS

ASOCA3-FPGA Jan, 2024 - present
The University of Edinburgh *PhD Sub-project*

- Developing a graph database accelerator system at million-entry level
- Fully in charge of architecture iterating

ASOCat Sept, 2022 - present
The University of Edinburgh *PhD Sub-project*

- Building a Copycat-based cognitive model compatible with an associative memory chip
- Designing and implementing its software/hardware interface

PUBLICATIONS

A Resource-efficient Dually-addressable Memory Architecture on FPGA Apr, 2023 - Dec, 2023
The University of Edinburgh *ISCAS 2024 (under review)*

- Presented a resource-efficient BRAM-based DAM architecture on FPGA
- Implemented onto Virtex-7/Virtex UltraScale+ FPGAs with 100% storage efficiency

A Single-layer Wideband Microwave Absorber with Reactive Screen, and A Novel Design of Microwave Absorber for Reduction of Radar Cross Section July, 2020
Tongji University *AP-S/URSI 2020*

- Carried out antenna simulation under HFSS and experimental data analyses

RESEARCH EXPERIENCE

Saliency detector Feb, 2024 - July, 2024
The University of Edinburgh, STMicro *PhD Sub-project*

· Developed a hybrid defect detection and classfication prototype
· Produced a result analysis and development report

ASOCA2 Nov, 2022 - Dec, 2023
The University of Edinburgh *PhD Sub-project*

· Successful tape-out of a memristor-based associative memory SoC
· Core digital hardware developer and verification engineer

ReMap: a Mitchell-based logarithmic conversion circuit Aug, 2021 - July, 2022
Nanyang Technological University *MSc Dissertation Project*

· Optimised a Mitchell-based binary logarithmic approximation method
· Implemented and evaluated corresponding integrated circuits

Design of a hierarchical memory management mechanism Aug, 2021 - Jan, 2022
Tongji University *Part-time Internship*

· Led a hierarchical SRAM-flash interface design with page replacement algorithm
· Applied the design on an automobile-orientated MCU

CoNM: Core of Normal Microarchitecture Mar, 2021 - Jun, 2021
Tongji University *Graduation Design*

· Designed a four-stage RV32I CPU core with static branch prediction in Verilog
· Implemented onto PYNQ-Z1 FPGA board for a successful verification

PROFESSIONAL SKILLS

Familiar with both FPGA and digital ASIC design flows.

Programming Languages

· Proficient in SystemVerilog/Verilog
· Skilled in Bash, Tcl, Python
· Competent in C/C++, VHDL
· Developing skills in CHISEL

Professional Software

· Skilled in Synopsys, Vivado, Cadence
· Good command of MATLAB, ModelSim
· Good knowledge of HFSS, ISE, Keil

Languages
Native in Mandarin and New Xiang, proficient in English

· IELTS 8.0/9.0 (2020), equivalent to CEFR level C1
· Elementary reading proficiency of French

SEMINARS & TALKS

IMNS Seminar November, 2024
Edinburgh, Scotland

Title: Graph Database Acceleration in Digital Hardware

2nd International Workshop on Deep Learning meets Neuromorphic Hardware September, 2024
Vilnius, Lituania

Presentation title: A modular graph database accelerator

TEACHING

The University of Edinburgh 1st Semester, 2024

· Demonstrator - Digital Systems Design 2
· Marker - Embedded Systems Design 2

Digital Systems Design 3 2nd Semester, 2024

· Demonstrator - Digital Systems Design 3

HONOURS AND AWARDS

Tongji University 1st Semester, 2017
Advanced Summer Internship Individual

· Awarded for the great performance during summer internship

Tongji University 1st Semester, 2019
Outstanding Student Cadre

· Awarded for the outstanding work as minister of Rights and Welfare Department in Students' Union

INTERESTS

Prefer *Scotches*.

$\frac{1}{2}$ geek, $\frac{1}{2}$ bartender.

Neovim user under WSL2.

Jay Chou and Aska Yang fan.

(Was) Practising the harmonica.

Reads Kafka, Hai Zi, Shelley and Allan Poe.

Always plannig to do something in film criticism and lyric writing.