YANJUN YANG

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EDUCATION

Tongji University Sept, 2017 - July, 2021
BEng. in Electronic Science and Technology *Shanghai, China*

· Core units taken: Design and Analysis of Digital Integrated Circuits, Computer Architecture, Principles for Design of Integrated Circuit Chips, Embedded Systems

Nanyang Technological University Aug, 2021 - Aug, 2022
MSc (Electronics) *Singapore*

· Core units taken: Digital Integrated Circuit Design, Electromagnetic Compability Design, Genetic Algorithms and Machine Learning, Advanced Wafer Processing, Integrated Circuit Packaging

The University of Edinburgh Sept, 2022 - present
PhD Candidate, IMNS *Edinburgh, Scotland*

· Supervisors: Alex Serb, Themis Prodromakis
· Research theme: Cognitive processing system implementation based on memristor associative memory

RESEARCH EXPERIENCE

ReMap: a Mitchell-based logarithmic conversion circuit Aug, 2021 - July, 2022
Nanyang Technological University *MSc Dissertation Project*

· Optimised a Mitchell-based binary logarithmic approximation method
· Implemented and evaluated corresponding integrated circuits

Design of a hierarchical memory management mechanism Aug, 2021 - Jan, 2022
Tongji University *Part-time Internship*

· In charge of a hierarchical SRAM-flash interface design with page replacement algorithm
· Applying the design on an automobile-orientated MCU

CoNM: Core of Normal Microarchitecture Mar, 2021 - Jun, 2021
Tongji University *Graduation Design*

· Designed a four-stage RV32I CPU core with static branch prediction in Verilog
· Implemented onto PYNQ-Z1 FPGA board for a successful verification

A Single-layer Wideband Microwave Absorber with Reactive Screen, A Novel Design of Microwave Absorber for Reduction of Radar Cross Section Dec, 2019 - May, 2020
Tongji University *Second Author*

· In charge of HFSS antenna simulation and analyses of experimental data
· Published two academic papers accepted by IEEE AP-S/URSI 2020 as the second author

ASOCA2 Nov, 2022 - Dec, 2023
The University of Edinburgh *PhD Sub-project*

· Design and verification of digital peripheral modules
· Design and verification of bus and interface

CURRENT PROJECTS

ASOCA3-FPGA Jan, 2024 - present
The University of Edinburgh *PhD Sub-project*

· Designing associative memory and random-access memory in FPGA
· Development of a graph database accelerator architecture

ASOCat Sept, 2022 - present
The University of Edinburgh *PhD Sub-project*

· Building a Copycat-based cognitive model compatible with an associative memory chip
· Designing and implementing its software/hardware interface

HONOURS AND AWARDS

Tongji University 1st Semester, 2017
Advanced Summer Internship Individual

· Awarded for the great performance during summer internship

Tongji University 1st Semester, 2019
Outstanding Student Cadre

· Awarded for the outstanding work as minister of Rights and Welfare Department in Students' Union

PROFESSIONAL SKILLS

Familiar with both digital ASIC and FPGA design workflows.

Programming Languages

· Proficient in SystemVerilog/Verilog
· Competent in Python, C/C++, VHDL
· Developing skills in CHISEL

Professional Software

· Skilled in Synopsys, ModelSim, MATLAB
· Good command of Vivado, Cadence
· Good knowledge of HFSS, ISE, Keil

Languages
Native in Chinese, proficient in English

· IELTS 8.0/9.0 (2020), equivalent to CEFR level C1
· Elementary reading proficiency of French

INTERESTS

Half geek.

Prefer *Scotches*.

A Jay Chou and Aska Yang fan.

Practising the harmonica and mixology.

Had thought of becoming a writer and polyglot.

Very interested yet rather ignorant in lyric writing and classical music.