|  |  |  |  |
| --- | --- | --- | --- |
| **Name:** | **Lee Yan Cheng** | **Lab Group#:** | **B10** |
| **Student Id:** | |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **A** | **0** | **1** | **9** | **9** | **1** | **4** | **1** | **B** | |  | |

Step 1. Truth Table **[ 4 pts ]**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | | | | | |
| ***A*** | ***B*** | ***C*** | ***S*4** | ***S*3** | ***S*2** | ***S*1** | ***S*0** | ***V*** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | **0** | **0** | **1** | **1** | **0** | **1** |
| 0 | 1 | 0 | **0** | **1** | **1** | **0** | **0** | **1** |
| 0 | 1 | 1 | **1** | 0 | 0 | **1** | **0** | **1** |
| 1 | 0 | 0 | **1** | **1** | **0** | **0** | **0** | **1** |
| 1 | 0 | 1 | **1** | **1** | **1** | **1** | **0** | **1** |
| 1 | 1 | 0 | **X** | **X** | **X** | **X** | **X** | **0** |
| 1 | 1 | 1 | **X** | **X** | **X** | **X** | **X** | **0** |

Step 2. K-Map and Simplified SOP **[ 5 pts ]**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | | **B** | | |
|  | **0** | | **0** | **1** | | **0** |
| **A** | **1** | | **1** | **X** | | **X** |
|  |  | **C** | | |  | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | | **B** | | |
|  | **0** | | **0** | **0** | | **1** |
| **A** | **1** | | **1** | **X** | | **X** |
|  |  | **C** | | |  | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | | **B** | | |
|  | **0** | | **1** | **0** | | **1** |
| **A** | **0** | | **1** | **X** | | **X** |
|  |  | **C** | | |  | |

**S4 = A + B.C S3 = A + B.C’ S2 = B’.C + B.C’**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | | **B** | | |
|  | **0** | | **1** | **1** | | **0** |
| **A** | **0** | | **1** | **X** | | **X** |
|  |  | **C** | | |  | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | | **B** | | |
|  | **0** | | **0** | **0** | | **0** |
| **A** | **0** | | **0** | **X** | | **X** |
|  |  | **C** | | |  | |

**S1 = C S0 = 0**

|  |
| --- |
|  |

**Step 3. Logic Diagram using 4-bit Parallel Adder and NAND gate [ 7 pts ]**