

Coordinated Control Strategy of Hybrid AC/DC Microgrid for Power Quality Improvement Under Unbalanced AC Conditions

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Abstract—In a hybrid AC/DC microgrid (MG), power quality issues arise when an unbalanced load connects to the AC subgrid, which are not confined to the AC subsystem but extend to affect the DC subsystem as well. This paper investigates the potential power quality issues caused by AC imbalance, including DC voltage fluctuation and AC current harmonics. Multiple control objectives are developed, aiming to eliminate DC fluctuation, reduce AC distortion and imbalance, and achieve negative sequence current sharing among distributed generations in the AC subgrid. To realize these control objectives, a two-layer coordinated control strategy is proposed. The first layer involves local interlinking converter (IC) control to improve the power quality of the DC subgrid, while the second layer focuses on distributed unbalance compensation control to improve the power quality of the AC subgrid. Finally, several experiments are conducted to verify the effectiveness of the proposed control strategy.

Index Terms—distributed control, hybrid AC/DC microgrid, power quality improvement, unbalance compensation

I. INTRODUCTION

MG provides a flexible way to integrate distributed generations (DGs) [1], [2]. This kind of grid can operate independently without relying on the power utility. In a single AC or DC configuration, each DG requires a power converter to standardize different power outputs into a unified form, which decreases the power conversion efficiency [3]. The emergence of hybrid AC/DC MG facilitates the aggregation of DC power. The established DC bus is interconnected with the AC subsystem through an interlinking converter (IC), which links two distinct subgrids: AC subgrid and DC subgrid. The IC plays a crucial role in managing power transfer and providing voltage and frequency support between these subgrids [4].

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Due to the lack of external support, MG often suffers from various power quality issues, particularly under unbalanced AC condition. These issues include voltage/frequency deviation [5]–[8], AC harmonics [9], [10], and DC voltage fluctuation [11], [12]. Such problems can disrupt the normal operation of sensitive loads connected to AC/DC buses. In critical situations, the imbalance may result in stability issues [13] or significant degradation in switching devices [14]. In [13], a novel impedance model is proposed to analyze potential instability of AC MG under unbalanced loads, along with a corresponding solution to enhance the stability. In [14], an optimization approach is introduced to solve the frequent switching issues caused by unbalanced loads, which can effectively reduce the number of switch operations. However, the above-mentioned studies commonly explore the phenomena induced by unbalanced conditions but rarely involve the compensation strategies which is also helpful to figure out the causes of these issues.

To address power quality decline, static var generators (SVG) and active power filters (APF) are commonly employed [15], which increase the cost of equipment investment and maintenance. However, cost-effective control strategies can achieve similar objectives. Coordinated control among DGs can be utilized for unbalance compensation [16]–[20], harmonic current sharing [21], [22], and harmonic voltage compensation [23], [24]. Specially, regarding the unbalance compensation, several effective approaches are employed, which can be classified into two main categories: virtual impedance-based method [16], [17] and negative sequence current (NSC) injection-based method [18]–[20], which are illustrated in Fig.1. In the virtual impedance-based method, unbalance compensation can be achieved by emulating virtual impedance for different phases as illustrated in Fig.1a. On the other hand, in the NSC injection method, DG outputs NSC based on the degree of voltage imbalance. Comparing these two methods, the virtual impedance-based method introduces a certain voltage drop, and voltage restoration is necessary to avoid excessive voltage deviation. In contrast, the NSC injection method avoids the additional voltage drops caused by the virtual impedance.

In the context of a hybrid AC/DC MG, the interplay between the AC and DC subgrids complicates power quality management. One possible solution is to design an effective IC control strategy. In [10], NSC and harmonic current of

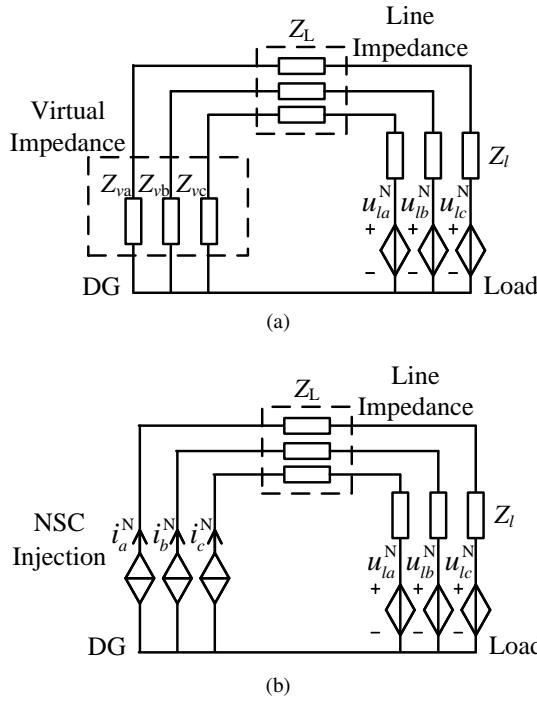


Fig. 1. Control strategies for unbalance compensation. (a) virtual impedance, (b) NSC injection.

the IC are regulated under unbalanced AC loads. This study primarily focuses on the power quality improvement of AC subgrid, but it does not sufficiently analyze the DC voltage fluctuation caused by the unbalanced condition. In [25] and [26], an extra DC active power filter is utilized to eliminate DC voltage fluctuation. This filter is connected between the DC-side of the IC and the DC bus. With this configuration, the AC and DC buses can achieve decoupling. The power quality decline in one subgrid will not affect the other. In [27] and [28], control strategies to eliminate DC voltage fluctuation are presented for single IC and multi-paralleled ICs respectively. These strategies aim to improve the power quality of the DC subgrid but do not address unbalance compensation in the AC subgrid. An effective way to improve the power quality in both subgrids is to coordinate the IC with DGs in the AC subgrid (ac-DGs). The IC can be utilized to regulate the power quality in the DC subgrid, and the ac-DGs can be employed to compensate for the unbalanced AC voltage.

In order to efficiently manage power quality in a hybrid AC/DC MG, this paper investigates the mechanisms of power quality decline under unbalanced AC conditions and proposes a two-layer coordinated control strategy to improve the power quality in both the AC and DC subgrids. The main contributions of this paper are summarized as follows.

- 1) The power quality issues attributed to the unbalanced AC voltages are analyzed both theoretically and numerically to provide insights into their underlying causes. Compared to the existing research about power quality improvement in hybrid MGs [25]–[28], this paper presents the interrelation among DC voltage fluctuation, AC current harmonics and the AC imbalance. The reasons for power quality decline in the hybrid MG are explained

from different perspectives.

- 2) Four different control objectives for power quality improvement are formulated. These objectives aim to eliminate DC voltage fluctuation, reduce AC distortion and imbalance, and achieve NSC sharing among ac-DGs simultaneously. Unlike existing studies that are confined to a single subgrid [19], [20], the designed control objectives encompass power quality improvement in both AC and DC subgrids.
- 3) A two-layer control strategy is proposed to address the potential decline in power quality. This strategy includes a local IC control and a distributed unbalance compensation control, each developed to achieve specific control objectives. Compared to the control strategies in [25] and [26], the proposed IC control strategy can suppress DC fluctuation without requiring an additional DC-DC converter. Additionally, a method based on NSC injection is designed for unbalance compensation, which can mitigate the extra voltage drops caused by virtual impedance [16], [17].
- 4) The proposed control strategy is validated through laboratory experiment using real converters. The control performance is tested under different operating conditions, and comparisons are conducted between the proposed method and the state-of-the-art approaches.

The rest of this paper is organized as follows. The system architecture of a hybrid AC/DC MG is presented in Section II and the power quality analysis under the unbalanced AC subgrid is conducted in Section III. In Section IV, a two-layer coordinated control strategy is proposed for power quality improvement. Experiments are carried out to validate the performance of the proposed control strategy under various operating conditions in Section V. Finally, conclusions are given in Section VI.

II. SYSTEM ARCHITECTURE

A typical structure of the hybrid AC/DC MG is illustrated in Fig.2. In the traditional control strategy, the ac-DGs adopt $P_{ac} - f_{ac}$ and $Q_{ac} - U_{ac}$ droop control, while the dc-DGs adopt $P_{dc} - U_{dc}$ droop control. Different droop control can be denoted by Eq.(1).

$$\begin{cases} \omega_{aci} = \omega_{acref} - n_p(P_{aci} - P_{acref}) \\ U_{aci} = U_{acref} - n_q(Q_{aci} - Q_{acref}) \\ U_{dcj} = U_{dcref} - n_{dc}(P_{dcj} - P_{dcref}) \\ i = 1, 2, \dots, N_{ac} \\ j = N_{ac} + 1, N_{ac} + 2, \dots, N_{ac} + N_{dc} \end{cases} \quad (1)$$

where ω_{acref} , U_{acref} and U_{dcref} are the reference of angular frequency, AC voltage and DC voltage. n_p , n_q and n_{dc} are the droop slopes. P_{ac}/P_{acref} , Q_{ac}/Q_{acref} and P_{dc}/P_{dcref} are the output power and their reference. N_{ac} and N_{dc} are the number of ac-DG and dc-DG. The ac-DGs are indexed from 1 to N_{ac} and the dc-DGs are indexed from $N_{ac} + 1$ to $N_{ac} + N_{dc}$.

The IC establishes the connection between electrical quantities in the AC and DC subgrids. Typically, dual-droop control, as discussed in [29], is employed to regulate the output power

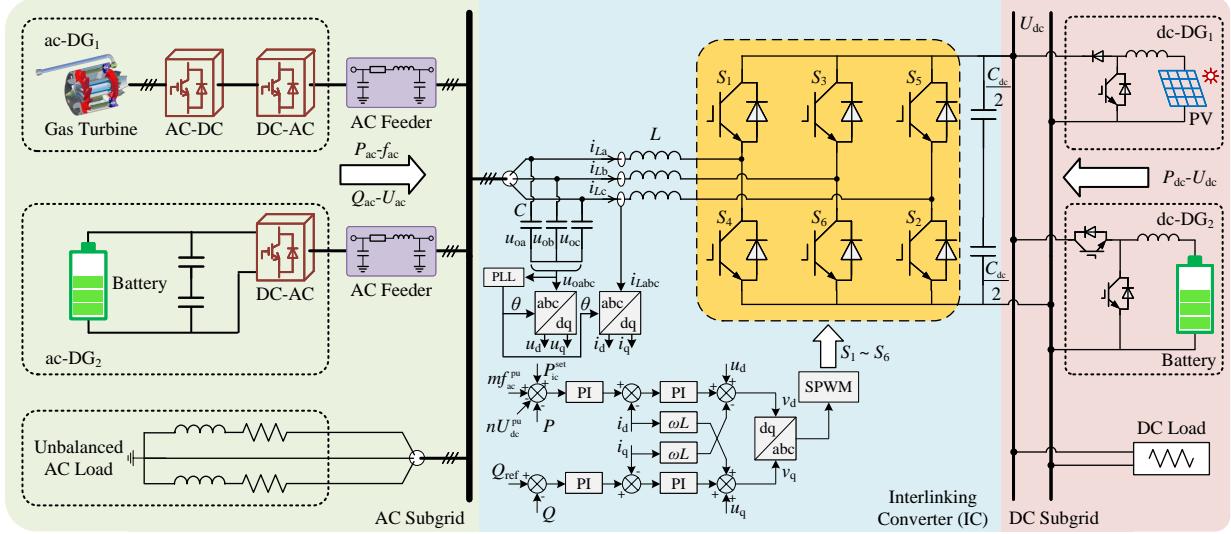


Fig. 2. Structure of a hybrid AC/DC MG and traditional control strategy.

according to the normalized frequency in the AC subgrid and the normalized voltage in the DC subgrid. This relationship is represented by Eq.(2).

$$P_{ic}^{ref} = P_{ic}^{set} + mf_{ac}^{pu} - nU_{dc}^{pu} \quad (2)$$

where m and n represent the dual-droop coefficients. P_{ic}^{set} and P_{ic}^{ref} denote the setting value and the reference of IC's active power. Considering the AC frequency f_{ac} within the range of $[f_{ac}^{\min}, f_{ac}^{\max}]$ and the DC voltage U_{dc} within the range of $[U_{dc}^{\min}, U_{dc}^{\max}]$, the normalized value f_{ac}^{pu} and U_{dc}^{pu} are defined as follows.

$$\begin{aligned} f_{ac}^{pu} &= \frac{f_{ac} - 0.5(f_{ac}^{\max} + f_{ac}^{\min})}{0.5(f_{ac}^{\max} - f_{ac}^{\min})} \\ U_{dc}^{pu} &= \frac{U_{dc} - 0.5(U_{dc}^{\max} + U_{dc}^{\min})}{0.5(U_{dc}^{\max} - U_{dc}^{\min})} \end{aligned}$$

III. POWER QUALITY ANALYSIS UNDER UNBALANCED AC CONDITION

A. DC Voltage Fluctuation

Considering the negative sequence component, the AC voltage and current of the IC can be expressed by Eq.(3).

$$\begin{cases} u_o = u_{o\alpha} + ju_{o\beta} = U_p e^{j\omega_s t} + U_n e^{-j(\omega_s t + \varphi_n)} \\ i_L = i_{L\alpha} + ji_{L\beta} = I_p e^{j(\omega_s t + \varphi_s)} + I_n e^{-j(\omega_s t + \varphi_n + \varphi_{sn})} \end{cases} \quad (3)$$

where U_p and U_n represent the amplitude of positive and negative sequence voltage. I_p and I_n denote the amplitude of positive sequence current and NSC. ω_s is the angular frequency of the AC subgrid. φ_n , φ_s and $\varphi_n + \varphi_{sn}$ are respectively the initial phase angle of negative sequence voltage, positive sequence current and NSC (suppose that the initial phase angle of positive sequence voltage is 0).

According to Eq.(3), the active and reactive power of the IC can be derived as Eq.(4). This equation indicates that the output power of the IC consists of two components: a constant component and a fluctuation component. The constant component follows the power reference (P_{ref} or Q_{ref}) and

the fluctuation component oscillates at twice the fundamental frequency.

$$\begin{cases} P_{ic} = Re\left(\frac{3}{2}\mathbf{u}_o \bar{i}_L\right) = P_0 + \tilde{P} \\ \quad = P_0 + A_P \cos(2\omega_s t + \varphi_n + \varphi_p) \\ Q_{ic} = Im\left(\frac{3}{2}\mathbf{u}_o \bar{i}_L\right) = Q_0 + \tilde{Q} \\ \quad = Q_0 + A_Q \cos(2\omega_s t + \varphi_n + \varphi_Q) \end{cases} \quad (4)$$

where P_0 and Q_0 are the constant components of the output power. A_P and A_Q are the amplitudes of the fluctuation components, which can be expressed as follows.

$$\begin{aligned} A_P &= \frac{3}{2} \sqrt{(U_p I_n \sin(\varphi_{sn} - \varphi_s))^2 + (U_p I_n \cos(\varphi_{sn} - \varphi_s) - U_n I_p)^2} \\ A_Q &= \frac{3}{2} \sqrt{(U_p I_n \sin(\varphi_{sn} - \varphi_s))^2 + (U_p I_n \cos(\varphi_{sn} - \varphi_s) + U_n I_p)^2} \end{aligned}$$

According to Eq.(4), the fluctuation component of the active and reactive power cannot be eliminated simultaneously. The active power fluctuation can be eliminated if $U_p I_n = U_n I_p$ and $\varphi_s = \varphi_{sn}$ are satisfied, while the reactive power fluctuation can be eliminated if $U_p I_n = U_n I_p$ and $\varphi_s = \varphi_{sn} + \pi$ are satisfied.

Fig.3a and Fig.3b respectively depict the variations in the amplitude of active power and reactive power fluctuation components with respect to the negative sequence voltage and current. These negative sequence components indicate the degree of imbalance in the AC subgrid. Overall, there is a positive correlation between the power fluctuation and the negative sequence components. It implies that an increase in the imbalance of the AC subgrid corresponds to a simultaneous rise in the power fluctuation through the IC. In particular, the NSC has a more significant impact on power fluctuation.

Considering the power equation of the DC-side capacitance in the IC as shown in Eq.(5), it is evident that a fluctuation component with twice the fundamental frequency exists in the

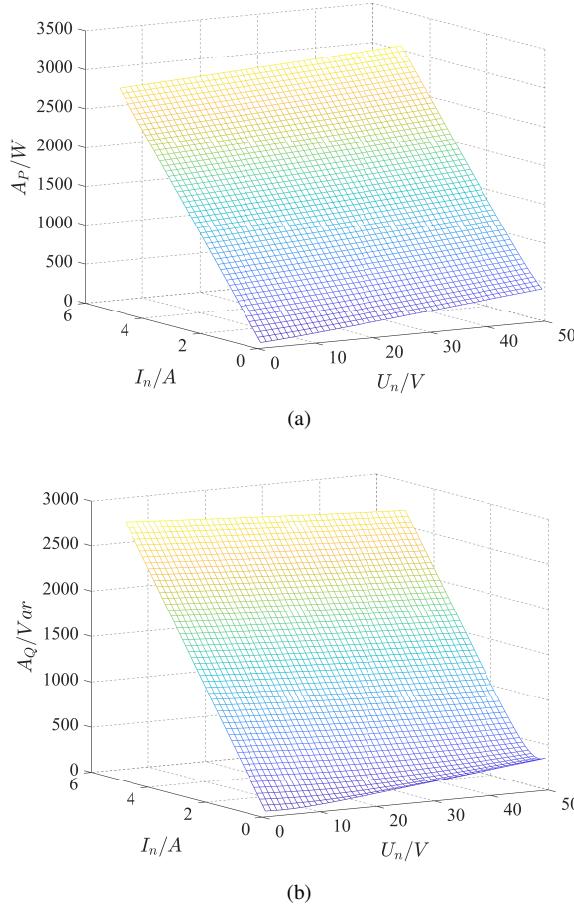


Fig. 3. The relationship among the amplitude of fluctuation components, negative sequence voltage, and NSC ($U_p = 380V$, $I_p = 5A$, $\varphi_{sn} - \varphi_s = 2\pi/3$). (a) A_P , (b) A_Q .

DC voltage [26]. Without loss of generality, the DC voltage u_{dc} can be represented by Eq.(6).

$$C_{dc} u_{dc} \frac{du_{dc}}{dt} = P_{ic} - P_{DC} = P_0 + \tilde{P} - P_{DC} \quad (5)$$

$$u_{dc} = U_{dc0} + \tilde{U}_{dc} \cos(2\omega_s t + \varphi_{dc}) \quad (6)$$

where U_{dc0} is the average value of the DC voltage, \tilde{U}_{dc} is the amplitude of the DC voltage's fluctuation component, which corresponds to the power fluctuation \tilde{P} in Eq.(5).

In Eq.(5) and Eq.(6), several factors affect the magnitude of the fluctuation component, including the size of the DC-side capacitance C_{dc} and the power fluctuation \tilde{P} . In particular, \tilde{P} correlates directly with the degree of AC voltage imbalance, as depicted in Fig.3a. Herein, a numerical result shown in Fig.4 illustrates the fluctuation component of the DC voltage. The parameters of the IC used in the numerical analysis are presented in TABLE I. The unbalanced AC voltage can be quantified by the voltage unbalance factor (VUF) [30]–[32], which is defined by Eq.(7).

$$\epsilon = 100 \frac{U_n}{U_p} \% \quad (7)$$

According to Fig.4, higher voltage imbalance contributes to an increase in the fluctuation component of DC voltage,

TABLE I
PARAMETERS OF THE IC IN THE NUMERICAL ANALYSIS

Parameter	Value	Parameter	Value
AC RMS voltage	173V	Frequency	50Hz
DC voltage	300V	DC capacitance	1645μF
Filter inductance	1.2mH	Filter capacitance	16μF
f^{\min}	49.5Hz	f^{\max}	50.5Hz
U_{dc}^{\min}	280V	U_{dc}^{\max}	320V
m	0.5kW	n	0.5kW

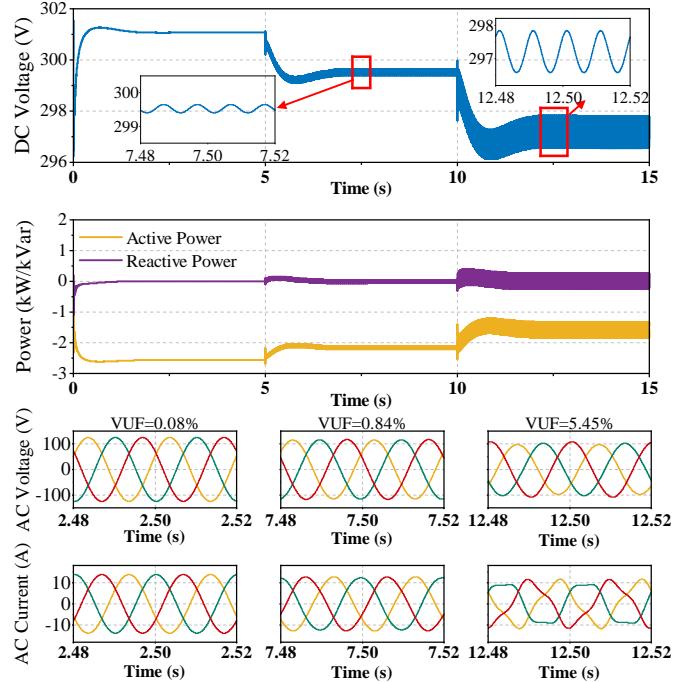


Fig. 4. Numerical results for *DC Voltage Fluctuation* under different AC loads. A balanced load is connected from $t = 0s$ to $t = 5s$ with VUF = 0.08%. A slightly unbalanced load is connected from $t = 5s$ to $t = 10s$ with VUF = 0.84%, and a heavily unbalanced load is connected from $t = 10s$ to $t = 15s$ with VUF = 5.45%.

active power and reactive power, which is consistent with the analytical results shown in Fig.3. In the meantime, the distortion of AC current is more significant as the VUF increases.

It should be noted that the DC-side capacitance is able to suppress the DC voltage fluctuation. Fig.5 illustrates the relationship between the DC voltage fluctuation and the DC-side capacitance C_{dc} . The peak-to-peak value is used to quantify the degree of DC fluctuation. The results indicate that increasing the DC-side capacitance can reduce the fluctuation. Therefore, it's feasible to design an appropriate C_{dc} based on the extent of AC voltage imbalance. However, this hardware modification approach poses two main challenges: 1) achieving zero-fluctuation DC voltage is impractical, 2) additional expenses are required.

B. AC Current Harmonics

1) *Third Harmonics Induced by DC Voltage Fluctuation:* According to the switching function model of the IC, the

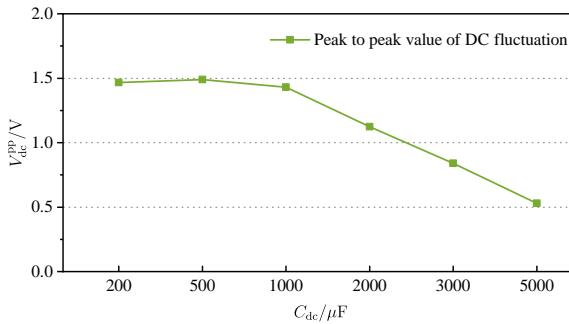


Fig. 5. The relationship between the fluctuation of DC voltage and the DC-side capacitance C_{dc} .

converter-side voltage u_{cx} can be expressed by Eq.(8).

$$u_{cx} = \frac{1}{2} S_x u_{dc} = \frac{1}{2} S_x (U_{dc0} + \tilde{U}_{dc} \cos(2\omega_s t + \varphi_{dc})) \quad (8)$$

where S_x is the switching function and $x \in \{a, b, c\}$ represents different phases.

The switching function S_x can be expressed by Eq.(9).

$$S_x = D_x \cos(\omega_s t + \varphi_x) \quad (9)$$

where D_x is the duty ratio of phase x and φ_x represents the initial phase angle.

By combining Eq.(8) and Eq.(9), the converter-side voltage u_{cx} can be expressed by Eq.(10). The third AC voltage harmonics are generated, which are proportional to the DC voltage fluctuation component. The voltage harmonics on the converter-side directly impact the output current of the IC, resulting in the current distortion.

$$\begin{aligned} u_{cx} = & \frac{1}{4} D_x (2U_{dc0} \cos(\omega_s t + \varphi_x) + \tilde{U}_{dc} \cos(\omega_s t + \varphi_{dc} - \varphi_x)) \\ & + \frac{1}{4} \tilde{U}_{dc} D_x \cos(3\omega_s t + \varphi_{dc} + \varphi_x) \end{aligned} \quad (10)$$

A numerical analysis is performed to demonstrate the presence of third harmonics in the AC current. Herein, the phase of the IC is directly settled instead of utilizing the PLL. At $t = 7.5$ s, an unbalanced load is connected to the AC subgrid, and the IC will experience an unbalanced AC voltage. The results are depicted in Fig.6, which illustrates the AC voltage, DC voltage, AC current and its spectrum. Consistent with the previously discussed theoretical analysis, the DC voltage fluctuation caused by unbalanced AC voltage contributes to the presence of third harmonics in the IC's output current. Therefore, eliminating the DC voltage fluctuation is conducive to minimize the AC current harmonics.

2) Odd Harmonics Induced by Synchronization Error:

Apart from DC voltage fluctuation, harmonic distortion can also arise from synchronization errors in PLL. The structure of the commonly used synchronous reference frame PLL (SRF-PLL) is illustrated in Fig.7. In this configuration, a PI controller is utilized to keep the q-axis voltage u_q at 0 in order to synchronize with the voltage phase angle θ^* .

Considering the unbalanced AC voltage in Eq.(3), the expression for the phase angle acquired by the SRF-PLL can be depicted as Eq.(11).

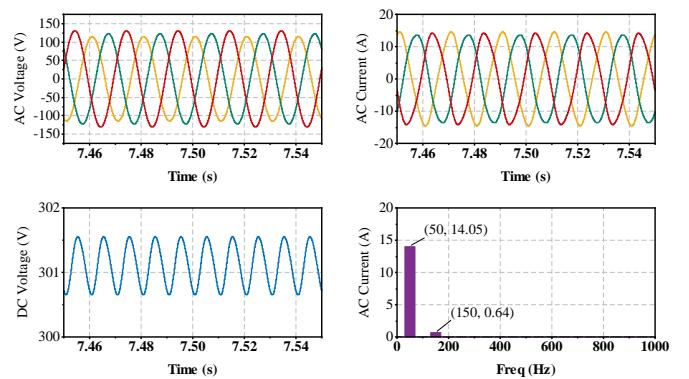


Fig. 6. Numerical results to illustrate the third harmonics induced by DC voltage fluctuation.

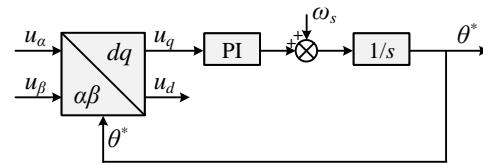


Fig. 7. Block diagram of SRF-PLL.

$$\left\{ \begin{array}{l} \cos(\theta^*) = \frac{U_p \cos(\omega_s t) + U_n \cos(\omega_s t + \varphi_n)}{\sqrt{U_p^2 + U_n^2 + 2U_p U_n \cos(2\omega_s t + \varphi_n)}} \\ \sin(\theta^*) = \frac{U_p \sin(\omega_s t) - U_n \sin(\omega_s t + \varphi_n)}{\sqrt{U_p^2 + U_n^2 + 2U_p U_n \cos(2\omega_s t + \varphi_n)}} \end{array} \right. \quad (11)$$

Therefore, a phase-locking error $\Delta\theta$ is generated, which can be expressed by Eq.(12).

$$\Delta\theta = \theta^* - \omega_s t = \cos^{-1}\left(\frac{U_p + U_n \cos(2\omega_s t + \varphi_n)}{\sqrt{U_p^2 + U_n^2 + 2U_p U_n \cos(2\omega_s t + \varphi_n)}}\right) \quad (12)$$

According to Eq.(12), the relationship between synchronization error and negative sequence voltage can be derived. Since the error $\Delta\theta$ in Eq.(12) represents a component at twice the fundamental frequency, the maximum value of $\Delta\theta$ within one cycle is selected for analysis. Fig.8 illustrates the impact of negative sequence voltage on the maximum synchronization error $\max \Delta\theta$. The results clearly indicate that as the negative sequence voltage U_n increases, the associated synchronization error increases accordingly, regardless of the phase angle φ_n . This synchronization error ultimately results in distortion in the AC current flowing through the IC.

To demonstrate the impact of synchronization error on the current distortion, a numerical analysis is implemented to support the theoretical results. In the numerical analysis, the DC voltage of the IC remains constant without any fluctuation, and the resulting third harmonics can be avoided. The numerical results, presented in Fig.9, illustrate the AC voltage, synchronization error, AC current and the corresponding spectrum. The results indicate that synchronization error induces odd-order harmonics in the AC current, with third and fifth harmonics being the most prominent.

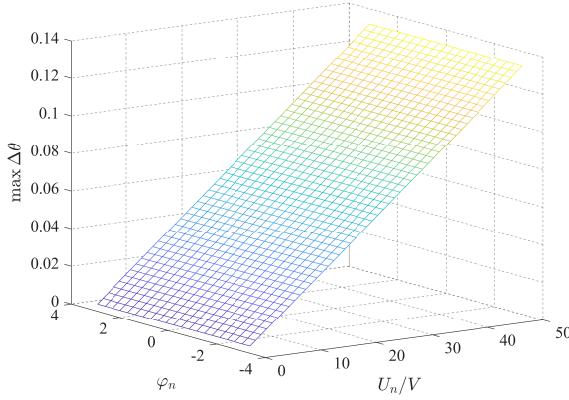


Fig. 8. The relationship between the maximum synchronization error and negative sequence voltage ($U_p = 380V$).

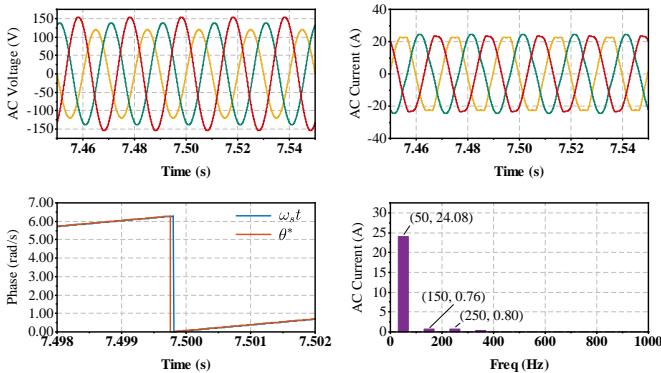


Fig. 9. Numerical results to illustrate the relationship between distortion and synchronization error.

C. Control Objectives for Power Quality Improvement

According to the above analysis, it's essential to design a control strategy to improve the power quality of a hybrid AC/DC MG under unbalanced AC conditions. The control objectives include suppressing DC fluctuation, minimizing AC distortion, compensating for imbalance, and sharing NSC. An overview of these control objectives and their implementation methods is provided below.

1) *DC Fluctuation Suppression:* As a key indicator of power quality in the DC subgrid, it is necessary to mitigate the DC voltage fluctuation. This control objective can be denoted by Eq.(13).

$$\tilde{U}_{dc} = 0 \quad (13)$$

In order to achieve this control objective, the IC is controlled to inject NSC into the AC subgrid, which ensures $A_p = 0$ as indicated by Eq.(4). By doing so, the active power fluctuation component \tilde{P} transmitted between the AC and DC subgrids can be eliminated, and ultimately the DC fluctuation is suppressed.

2) *AC Distortion Minimization:* The AC harmonics caused by the unbalanced load need to be minimized. According to the standard [31], it is recommended to restrict the total harmonic distortion (THD) to a maximum of 4%.

3) *Unbalance Compensation:* As a key indicator of power quality in the AC subgrid, the unbalanced AC voltage supplied

to the load should not be excessive, as it can lead to abnormal operation of loads which are sensitive to voltage imbalance. In other words, the VUF of the AC bus should be limited. Additionally, as analyzed in Section III-A, unbalance in the AC subgrid can also deteriorate the power quality in the DC subgrid. Therefore, reducing the VUF can help address DC voltage fluctuation simultaneously. Although the control objectives 1) and 2) will naturally be satisfied if the unbalanced AC voltage is fully compensated ($VUF = 0$), it is impractical to achieve complete unbalance compensation at each AC bus due to the local characteristic of bus voltage. Generally, the VUF at the AC bus should be kept below a predefined threshold. According to standards [31] and [32], this threshold is set at 2%.

4) *Negative Sequence Current Sharing:* During unbalance compensation, the generated NSC occupies the capacity of the ac-DGs. To address potential overload concerns, the distribution of NSC among different ac-DGs is considered. Herein, an even sharing approach is adopted, which can be expressed by Eq.(14).

$$I_i^N = I_j^N \quad (14)$$

where I_i^N and I_j^N represent the NSC amplitudes of ac-DG_i and ac-DG_j, respectively.

IV. TWO-LAYER COORDINATED CONTROL STRATEGY

In this section, a two-layer coordinated control strategy is proposed for the power quality improvement in the hybrid MG. The first layer is designed to regulate the power fluctuation of the IC, which relies on local information without the need for communication. The second layer is responsible for unbalance compensation, which is achieved through a distributed communication network.

A. Layer I: Local Control Strategy of IC

To achieve flexible regulation of power fluctuation, the output current of the IC can be controlled based on orthogonal signals generated by the AC voltage signals. The control block is illustrated in Fig.10. According to the analysis in Section III-A, the fluctuation of the output power is effectively regulated by controlling I_n and φ_{sn} . It allows for three different control modes: zero-fluctuation active power, zero-NSC and zero-fluctuation reactive power. The output current under different control modes is expressed in a unified form through an adjustment parameter λ , as denoted in Eq.(15).

$$\begin{cases} i_L = i_{LP} + i_{LQ} \\ i_{LP} = I_p \cos(\varphi_s)e^{j\omega_s t} + I_n \cos(\varphi_{ns})e^{-j(\omega_s t + \varphi_n)} \\ \quad = z_1(U_p e^{j\omega_s t} + (1 - 2\lambda)U_n e^{-j(\omega_s t + \varphi_n)}) \\ i_{LQ} = j(I_p \sin(\varphi_s)e^{j\omega_s t} - I_n \sin(\varphi_{ns})e^{-j(\omega_s t + \varphi_n)}) \\ \quad = jz_2(U_p e^{j\omega_s t} - (1 - 2\lambda)U_n e^{-j(\omega_s t + \varphi_n)}) \end{cases} \quad (15)$$

where i_{LP} and i_{LQ} are the current components associated with active and reactive power, respectively. The controllable variables include z_1 , z_2 , and λ . The output current given in Eq.(15) allows an expression of IC's output power, which is denoted in Eq.(16). Notably, z_1 and z_2 are used to regulate the

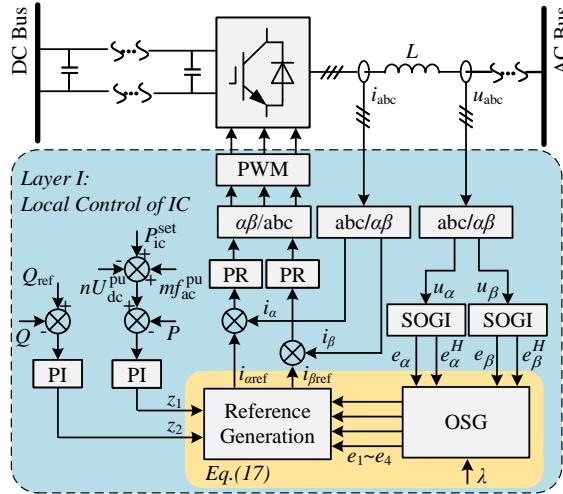


Fig. 10. Block diagram of Layer I: Local Control Strategy of IC.

constant parts of active and reactive power, while the parameter λ , ranging from 0 to 1, is used to regulate the fluctuation component. By setting $\lambda = 1$, the fluctuation component of active power can be eliminated, and the fluctuation component of reactive power can be eliminated if $\lambda = 0$. Additionally, when $\lambda = 1/2$, the output current will not contain the negative sequence component.

$$\begin{cases} P = z_1 U_p^2 + (1 - 2\lambda) z_1 U_n^2 + 2(1 - \lambda) U_p U_n \times \\ \quad (z_1 \cos(2\omega_s t + \varphi_n) + z_2 \sin(2\omega_s t + \varphi_n)) \\ Q = z_2 U_p^2 + (1 - 2\lambda) z_2 U_n^2 + 2\lambda U_p U_n \times \\ \quad (z_2 \cos(2\omega_s t + \varphi_n) - z_1 \sin(2\omega_s t + \varphi_n)) \end{cases} \quad (16)$$

An orthogonal signal generation (OSG) strategy is designed based on the AC voltage signals $e_{\alpha\beta}$ and $e_{\alpha\beta}^H$ to produce the current reference, which can be expressed by Eq.(17).

$$\begin{aligned} i_{L\text{ref}} &= z_1 \underbrace{(1 - \lambda)e_\alpha - \lambda e_\beta^H}_{e_1} + z_2 \underbrace{((\lambda - 1)e_\alpha^H - \lambda e_\beta)}_{e_2} \\ &\quad + j z_1 \underbrace{(e_\alpha^H + (1 - \lambda)e_\beta)}_{e_3} + j z_2 \underbrace{(\lambda e_\alpha + (\lambda - 1)\lambda e_\beta^H)}_{e_4} \\ &= (z_1 e_1 + z_2 e_2) + j(z_1 e_3 + z_2 e_4) \\ &= i_{L\text{aref}} + j i_{L\text{bref}} \end{aligned} \quad (17)$$

where e_1, e_2, e_3 and e_4 are the four orthogonal signals. $e_{\alpha\beta}^H$ are the voltage signals that lag $e_{\alpha\beta}$ 90° , which can be generated by a second-order generalized integrator (SOGI).

Herein, a proportional resonant (PR) controller can be utilized to track the current reference in the $\alpha\beta$ -axis. Its transfer function can be expressed by Eq.(18).

$$G_{\text{PR}}(s) = k_p + \frac{k_r \omega_c s}{s^2 + 2\omega_c s + \omega_s^2} \quad (18)$$

where k_p and k_r are the proportional and resonant gain. ω_c and ω_s are the cut-off and resonant frequency.

Following the generated current reference by Eq.(17), the power transfer between AC subgrid and DC subgrid can be regulated according to Eq.(16). It should be noted that

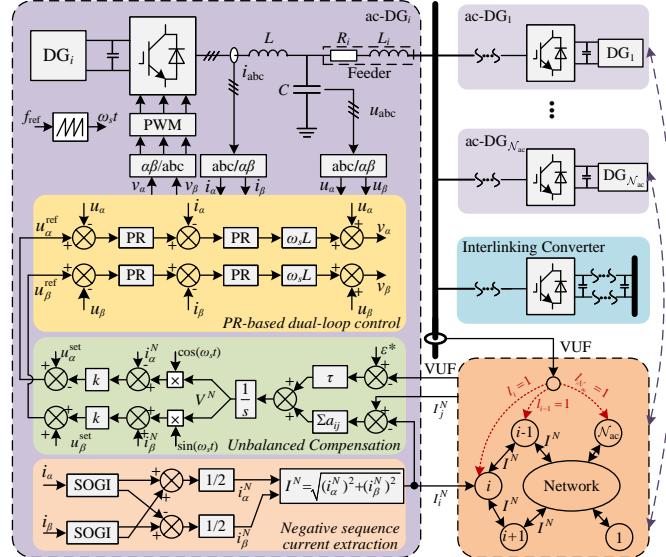


Fig. 11. Block diagram of Layer II: Distributed Unbalance Compensation Control.

with different values of λ , the fluctuation components are altered between active power and reactive power, thus it cannot be completely eliminated. However, since active power directly affects the DC voltage, it is feasible to transfer all the fluctuation components to the reactive power. For example, by setting $\lambda = 1$, the active power transferred by the IC can be expressed as $P = z_1 U_p^2 - z_1 U_n^2$ according to Eq.(16), which excludes the fluctuation component. Furthermore, as shown in Eq.(5), this approach can prevent voltage from fluctuation in the DC subgrid.

B. Layer II: Distributed Unbalance Compensation Control of ac-DG

In the Layer II control, an unbalance compensation controller is designed based on NSC injection. The proposed control strategy is implemented in ac-DGs and relies on a distributed communication network among them. The corresponding block diagram is illustrated in Fig.11. It requires information such as the amplitude of NSC from the neighbor DGs and the VUF of the AC bus needs to be obtained. The control equation can be expressed by Eq.(19).

$$\begin{cases} \dot{V}_i^N = -l_i(\epsilon^* - \epsilon_B) + \sum_{j \in N_i} a_{ij}(I_j^N - I_i^N) \\ u_{\alpha\text{ref}}^{\text{ref}} = V_i^{\text{set}} \cos(\omega_s t) + k(V_i^N \cos(\omega_s t) + i_{\alpha i}^N) \\ u_{\beta\text{ref}}^{\text{ref}} = V_i^{\text{set}} \sin(\omega_s t) - k(V_i^N \sin(\omega_s t) - i_{\beta i}^N) \end{cases} \quad (19)$$

where $u_{\alpha\text{ref}}^{\text{ref}}$ and $u_{\beta\text{ref}}^{\text{ref}}$ represent the AC voltage reference in the $\alpha\beta$ -axis, which will be sent to the PR-based dual-loop control for PWM generation. $i_{\alpha i}^N$ and $i_{\beta i}^N$ are the NSC components, and $I^N = \sqrt{(i_{\alpha i}^N)^2 + (i_{\beta i}^N)^2}$ is the amplitude of the NSC. V_i^{set} is the setting value of the positive sequence voltage. ϵ_B and ϵ^* are respectively the VUF of the AC bus and its targeted value. a_{ij} is the entry in the adjacent matrix of distributed

communication network, and N_i is a set of ac-DGs adjacent to ac-DG $_i$. The binary flag $l_i \in \{0, 1\}$ indicates whether ac-DG $_i$ is responsible for unbalance compensation. It is important to note that not all the ac-DGs are required to compensate for the VUF of the AC bus, but all the ac-DGs must participate in NSC sharing to avoid overload.

The control equation in Eq.(19) adjusts the negative sequence voltage V_i^N according to the VUF of the AC bus and the difference in the NSC of ac-DG $_i$. The compensation process can be categorized into two scenarios: 1) If the unbalanced AC voltage is not completely compensated ($\epsilon^* < \epsilon_B$), it implies that $V_i^N \neq 0$, and the negative sequence voltage V_i^N will be continuously adjusted until full compensation is achieved. 2) If the NSC sharing is not achieved ($I_i^N \neq I_j^N$), $V_i^N \neq 0$ is also valid. In this case, V_i^N will be adjusted until $I_i^N = I_j^N$ is satisfied. It is important to note that the state where $V_i^N = 0$ but $\epsilon^* \neq \epsilon_B$ and $I_i^N \neq I_j^N$ does not always keep because there are N_{ac} control equations in the MG. When one ac-DG might achieve this state, other ac-DGs will alter it. Therefore, if the control equation in Eq.(19) reaches a steady state, the control objectives $\epsilon^* = \epsilon_B$ and $I_i^N = I_j^N$ can be achieved.

With the proposed two-layer control strategy, the four control objectives developed in Section III-C can be achieved. The control strategy of *Layer I* facilitates the alteration of fluctuation between active power and reactive power. Thus, the DC voltage can be regulated without any ripple. Additionally the proposed *Layer I* control strategy utilizes OSG to replace the PLL, effectively eliminating AC harmonics. Consequently, *Layer I* control achieves the objectives 1) and 2). Furthermore, the *Layer II* control strategy collaborates with ac-DGs connected to the AC subgrid for unbalance compensation and NSC sharing in a distributed framework. This ensures the achievement of control objectives 3) and 4).

C. Negative Sequence Equivalent Model

Herein, a negative sequence equivalent model of the AC subgrid is developed to facilitate small-signal stability analysis and parameter design for the proposed control strategy. Fig.12 illustrates the negative sequence equivalent circuit of the AC subgrid. The ac-DGs are represented as negative sequence voltage sources, each generating a negative sequence voltage V_i^N and NSC I_i^N . The IC is represented as a NSC source I_{IC}^N , expressed by Eq.(17). All the ac-DGs are connected to the AC bus through their respective line impedances $Z_i = R_i + j\omega L_i$, and the AC load is equivalently represented as a NSC source I_L^N .

In Fig.12, there are N_{ac} ac-DGs in the AC subgrid. For ac-DG $_i$, the circuit equation, considering the line impedance Z_i , can be expressed by Eq.(20).

$$V_B^N = V_i^N + R_i I_i^N + sL_i I_i^N \quad (20)$$

where V_B^N is the negative sequence voltage of the AC bus.

For the AC bus, Kirchhoff's current law (KCL) equation can be represented by Eq.(21).

$$I_L^N + I_{IC}^N = \sum_{i=1}^{N_{ac}} I_i^N \quad (21)$$

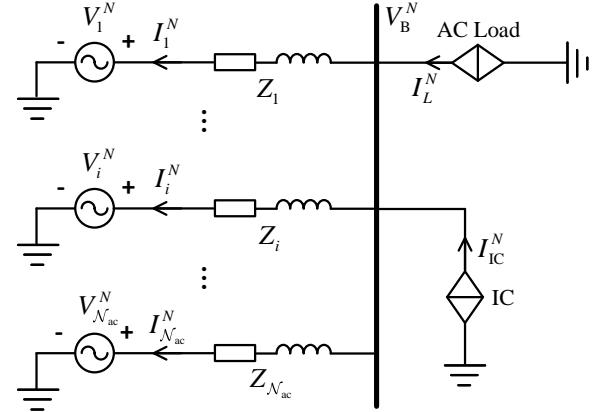


Fig. 12. Negative sequence equivalent model of AC subgrid.

By combining the control equation (Eq.(19)) with the circuit equations (Eq.(20) and Eq.(21)), a negative sequence equivalent model can be established. The detailed small-signal stability analysis is conducted in Section V-D. It should be noted that the voltage/current control loops within the ac-DG and IC are negligible due to their high bandwidth, which is beyond the time scale of the coordinated control.

V. EXPERIMENTAL RESULTS

A. Experiment Setup

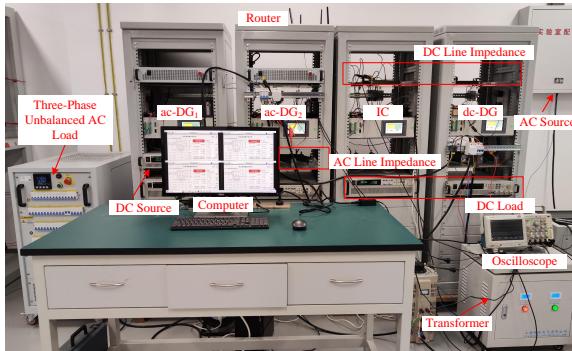
In this section, several experiments are conducted to verify the proposed control strategy. The experiment platform and its topology are presented in Fig.13. Detailed information regarding line impedance and initial load conditions is provided in TABLE II. In the experimental setup, four two-level voltage source converters (VSCs) serve as the ac-DGs, the dc-DG and the IC, respectively. The proposed two-layer control strategy is implemented in the TMS320F28335 DSP controller embedded in the VSCs. The Raspberry Pis manage the communication through a wireless network. The parameters of these VSCs align with those specified in TABLE I.

TABLE II
PARAMETERS OF THE EXPERIMENT PLATFORM

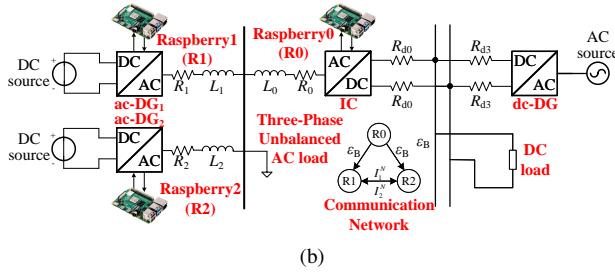
Classification	Parameters	Value
AC subgrid	R_0, L_0	$0.4\Omega, 0.33mH$
	R_1, L_1	$1.1\Omega, 2.67mH$
	R_2, L_2	$0.7\Omega, 1.45mH$
	A-phase load	$200+100j\text{VA}$
	B-phase load	$300+100j\text{VA}$
	C-phase load	$300+100j\text{VA}$
DC subgrid	R_{d0}	0.5Ω
	R_{d3}	1Ω
	DC load	600W

B. Control Performance with Different λ

The performance of the proposed control strategy is validated across different values of λ . The results are depicted



(a)



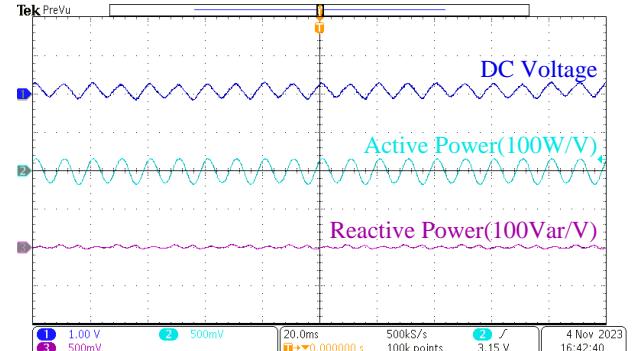
(b)

Fig. 13. Experiment platform of the hybrid AC/DC MG under the unbalanced AC load. (a) instruments, (b) grid overview.

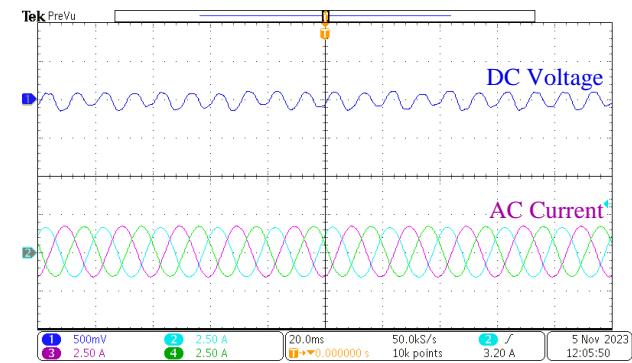
in Fig.14. Fig.14a and Fig.14c demonstrate the effectiveness of zero-fluctuation reactive power control and zero-fluctuation active power control respectively. The DC bus voltage and output power of the IC are monitored to illustrate the power fluctuation component. Herein, the DC component is filtered out, leaving only the fluctuation components for clarity. Furthermore, Fig.14b showcases the validation of zero-NSC control, where the AC current is presented in place of the output power. The results highlight the ability of the proposed control strategy to alter the fluctuation component between active power and reactive power. Specifically, when λ is set to 0, 0.5, and 1, zero-fluctuation reactive power, zero-NSC and zero-fluctuation active power can be achieved. Consequently, the IC demonstrates the capability to suppress double-frequency fluctuation in DC voltage induced by the unbalanced AC subgrids. In order to achieve the control objective outlined in Section III-C, it is necessary to implement zero-fluctuation active power control in the hybrid AC/DC MG. In other words, λ should be set to 1.

C. AC Current Harmonic

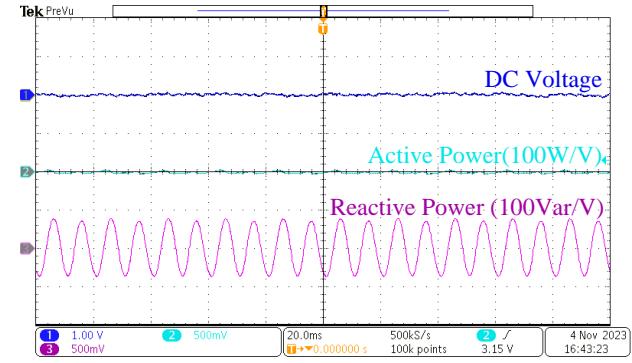
An experiment is conducted to compare the AC current of the proposed control strategy with PLL-based control strategy. In this case, the unbalance compensation (*Layer II* control) is not applied. The AC current waveform and their spectrum are presented in Fig.15. According to the results, PLL-based control strategy induces distortion and generates odd harmonics in the AC current, resulting in a THD of 4.33%. In contrast, the proposed control strategy can maintain a high-quality AC current waveform with small distortion, which achieves the control objectives for AC distortion minimization. The experiment results of the proposed control are consistent with the numerical analysis in Section III-C.



(a)



(b)



(c)

Fig. 14. Experiment results for the proposed control strategy (*Layer I*) with different λ values. (a) $\lambda = 0$, (b) $\lambda = 0.5$, (c) $\lambda = 1$.

D. Unbalanced AC Voltage Compensation

This subsection presents the performance of unbalance compensation, aiming to achieve the control objectives 3) and 4). A small-signal stability analysis is performed based on the negative sequence equivalent model established in Section IV-C. Fig.16 shows the results under different values of control parameter k . The analysis indicates that small-signal stability is ensured for different values of k , with all characteristic roots located on the left side of the complex plane. Specially, when k is chosen to be small, all characteristic roots are located on the real axis, which implies that the steady state can be achieved without additional transient overshoot and oscillation. As k increases, one of the characteristic roots bifurcates, leading to oscillations during the transient process. Considering the impact of k on the transient response, $k = 1$ is selected for

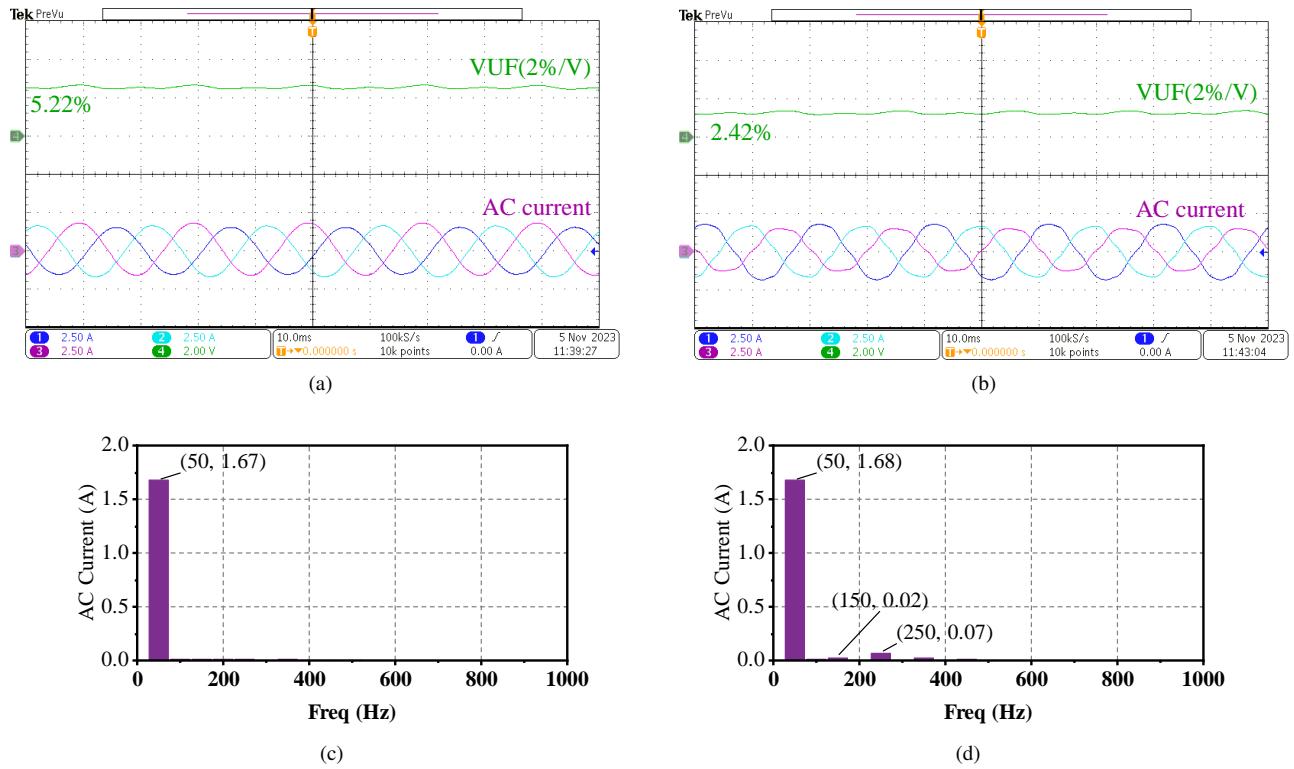


Fig. 15. Experiment results of AC current and its harmonics analysis. (a) and (c) are the waveform and its spectrum under the proposed control strategy, (b) and (d) are the waveform and its spectrum under the traditional control strategy with SRF-PLL.

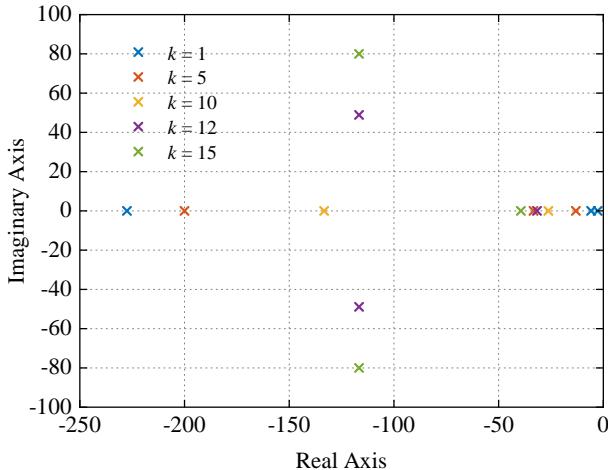


Fig. 16. Small-signal stability analysis of the proposed control strategy.

the experiment.

During the experiment, the target VUF, denoted as ϵ^* , is set at 2%. The experimental process involves two stages: i. At $t = t_1$, the *Layer II* control strategy is implemented; ii. At $t = t_2$, a 100W load reduction in A-phase is applied to exacerbate voltage imbalance. Fig.17 and Fig.18 depict the AC bus voltage and the amplitude of NSC throughout the process. When $t > t_1$, the unbalanced voltage in the AC subgrid is compensated and the VUF reduces from 5.84% to 2%, which achieves the control objectives for unbalance compensation. Furthermore, DGs can effectively share the NSC following

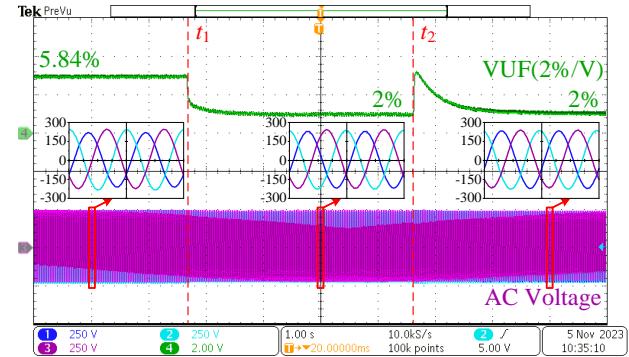


Fig. 17. Experiment results of unbalanced AC voltage compensation.

a predefined 1:1 ratio. Change in single-phase load doesn't impact the NSC sharing, and the overall increase in NSC serves to compensate for the VUF.

E. Comparison

In this subsection, several comparative results are presented to illustrate the advantages of the proposed control strategy. Firstly, a comparison with the state-of-the-art methods under unbalanced AC voltage is presented in TABLE III. The comparative results indicate that the proposed control strategy provides a more comprehensive solution for power quality improvement. It effectively regulates the DC fluctuation and AC imbalance simultaneously, and the power quality of both the AC and DC subgrids can be improved correspondingly.

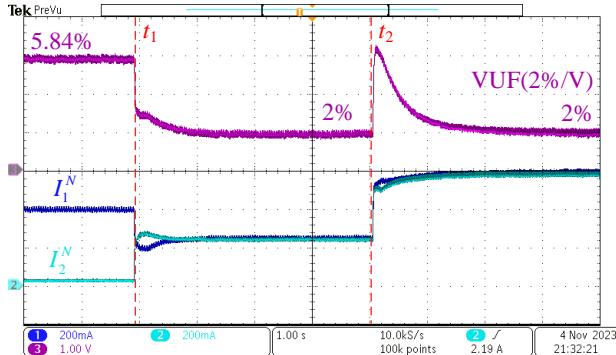


Fig. 18. Experiment results of NSC sharing.

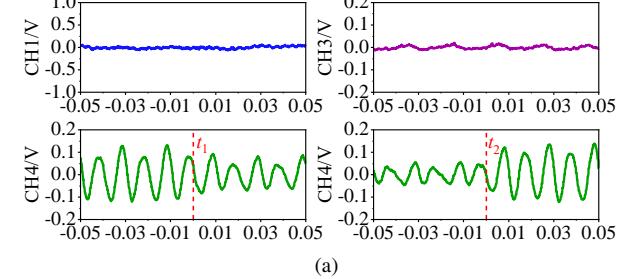
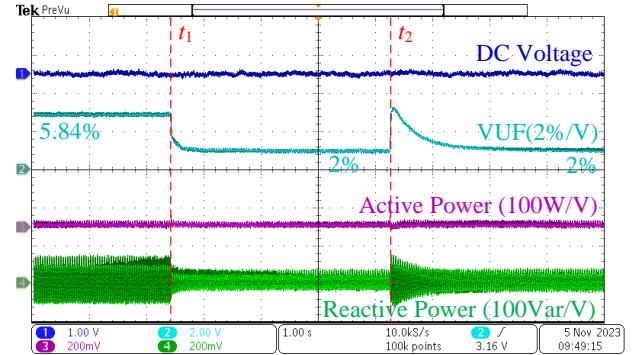
TABLE III
COMPARISON WITH STATE-OF-THE-ART CONTROL STRATEGIES UNDER UNBALANCED AC VOLTAGE

	DC fluctuation suppression	Unbalanced compensation	Active fluctuation	Reactive fluctuation
[10]	✗	✗	not involve	not involve
[15]	✗	✓	not involve	not involve
[25]	✓	✗	zero	not involve
[26]	✓	✗	zero	not involve
[27]	✓	✗	zero	not involve
[28]	✓	✗	zero	not involve
Proposed	✓	✓	adjustable	adjustable

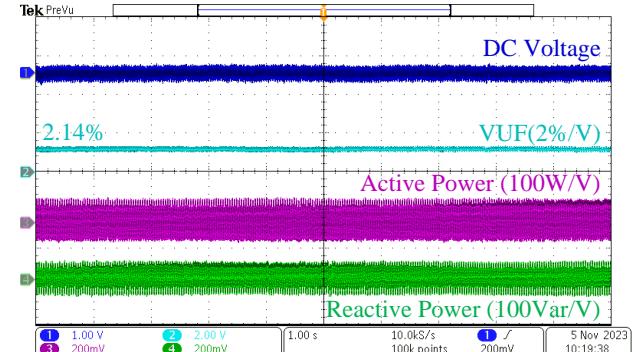
Additionally, the proposed control strategy allows for flexible adjustment of the IC's active and reactive power fluctuation. Consequently, it can switch control modes between zero-fluctuation active power and zero-fluctuation reactive power. It is important to note that achieving zero-fluctuation active power inevitably results in significant reactive power fluctuation if unbalance compensation is not available, and vice versa.

Furthermore, an experiment is conducted to compare the proposed method with the traditional distributed secondary control strategy of hybrid AC/DC MGs without power quality improvement in [6]. The DC voltage and IC's output power before and after unbalance compensation are illustrated in Fig.19, with magnified details of each channel for clarity. In Fig.19a, the same operation as discussed in Section IV-D is conducted, and the traditional control strategy is tested under the situation without AC load change at $t = t_2$. In the proposed control strategy, λ is set as 1. The results show that the reactive power of the IC exhibits significant fluctuation before unbalance compensation. The fluctuation frequency is consistent with the theoretical analysis, being twice the AC rated frequency. However, with the *Layer II* control, the fluctuation component of reactive power is effectively reduced. Compared with the result in Fig.19b, the proposed control strategy can completely eliminate the fluctuation component of the DC voltage and the active power. Besides, the reactive power can be also regulated to a low fluctuation level.

In addition, the proposed control strategy is compared with the virtual impedance-based method to demonstrate the AC voltage level after unbalance compensation. Fig.20 illustrates



(a)



(b)

Fig. 19. Experiment results of IC's DC voltage and output power after unbalance compensation. (a) proposed control strategy ($\lambda = 1$), (b) traditional control strategy without power quality improvement [6].

the RMS line voltages of the AC bus during experiment. Three different scenarios are considered: unbalance compensation under the proposed control strategy, unbalance compensation using the virtual impedance-based method, and no compensation. The results show that, without an AC voltage restoration strategy, the proposed control strategy can compensate for the unbalanced AC voltage and maintain the three-phase voltage close to the rated value. In contrast, the virtual impedance-based method will result in some voltage loss due to the impedance, causing the three-phase AC bus voltage to be slightly lower than the rated value. Therefore, if the virtual

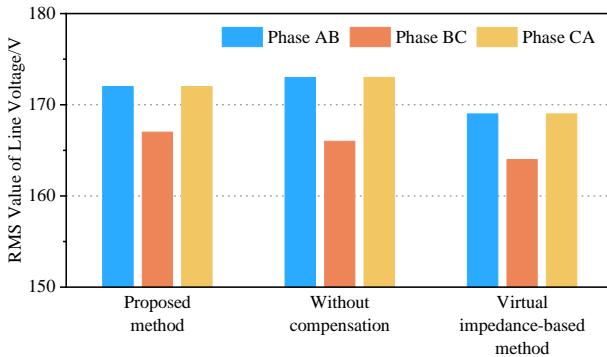


Fig. 20. RMS value of AC bus line voltage under different compensation methods.

impedance-based method is adopted, an additional voltage restoration strategy is necessary to prevent excessive voltage deviation.

VI. CONCLUSION

This paper investigates the power quality issues of a hybrid AC/DC MG under unbalanced AC conditions and proposes a two-layer coordinated control strategy. Theoretical analysis indicates that the unbalanced voltage in the AC subgrid leads to a power quality decline in the DC subgrid. Therefore, multiple control objectives should be involved for overall power quality improvement. In the proposed two-layer strategy, local IC control is employed to eliminate the DC fluctuation and reduce the AC harmonics, while the distributed coordinated strategy for the ac-DGs is to compensate for the unbalanced AC voltage and share the resulting NSC. Experimental results verify the effectiveness of the proposed control strategy and the power quality in both AC and DC subgrid is improved. Comparative results show that the proposed control strategy provides a more comprehensive solution to the power quality issues in hybrid AC/DC MGs, which is superior to the existing methods that only improve the power quality in a single subgrid.

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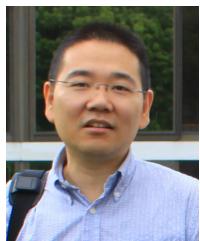
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