Experiment

7

ADC/DAC

Objectives

To study another group of analog IC circuits of great importance, data converters.

Overview

1. Ideal D/A Converter, DAC

Consider the block diagram of an N-bit D/A converter shown in Fig. 1. Here B_{in} is defined to be an N-bit digital signal (or word) such that

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N} \tag{7.1}$$

where b_i equals 1 or 0 (i.e., b_i is a binary digit).

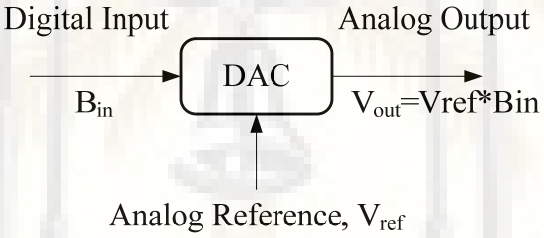


Fig. 1 A block diagram representing a D/A converter.

We also define b_1 as the most significant bit (MSB) and b_N as the least significant bit (LSB). Furthermore, we have assumed here that B_{in} represents a positive value, resulting in a unipolar D/A converter. *A unipolar D/A converter* produces an output signal of only one polarity.

The analog output signal, V_{out}, is related to the digital signal, B_{in}, through an analog reference signal, V_{ref}. For simplicity, we assume that both V_{out} and V_{ref} are voltage signals, although, in general, they may be other physical quantities, such as current or charge. The relationship between these three signals for a unipolar D/A converter is given by

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{ref} B_{in} \tag{7.2}$$

It is useful to define V_{LSB} to be the voltage change when one LSB changes, or, mathematically,

$$V_{LSB} \equiv \frac{V_{ref}}{2^N} \tag{7.3}$$

Also useful (particularly in measuring errors) is the definition of a new "unit," namely, LSB units, which are in fact unitless.

$$1\ \text{LSB} = \frac{1}{2^N} \tag{7.4}$$

The transfer curve for an ideal 2-bit D/A converter is shown in Fig. 2. Note that, although only a finite number of analog values occur at the output, for an ideal D/A converter, the output signals are well-defined values. Also note that the maximum value of V_{out} is not V_{ref} but rather $V_{ref}(1–2^{–N})$, or equivalently, $V_{ref} – V_{LSB}$.

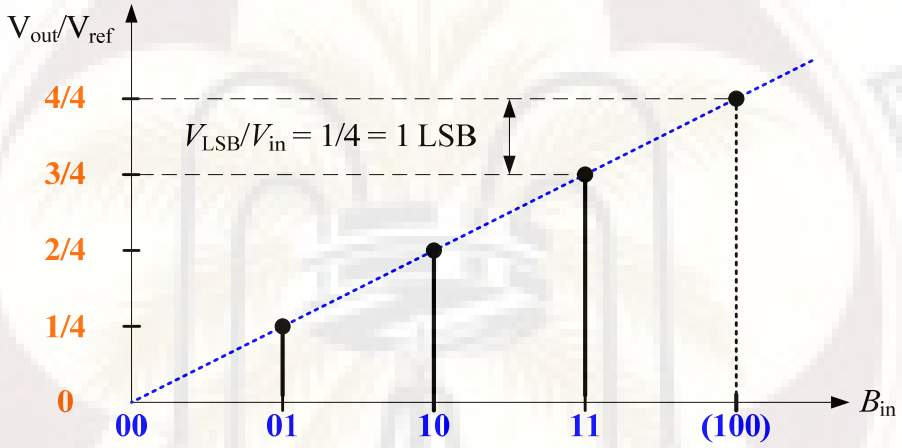


Fig. 2 Input-output transfer curve for an ideal 2-bit D/A converter.

Finally, as we can see from (7.2), a multiplying D/A converter is realized by simply allowing the reference signal, V_{ref}, to be a varying input signal along with the digital input, B_{in}. Such an arrangement results in V_{out} being proportional to the multiplication of the input signals, B_{in} and V_{ref}.

2. Ideal Analog/Digital Converter, ADC

The block diagram representation for an A/D converter is shown in Fig. 3, where B_{out} is the digital output word while V_{in} and V_{ref} are the analog input and reference signals, respectively. Also, we define V_{LSB} to be the signal change corresponding to a single LSB changes as in the D/A case.

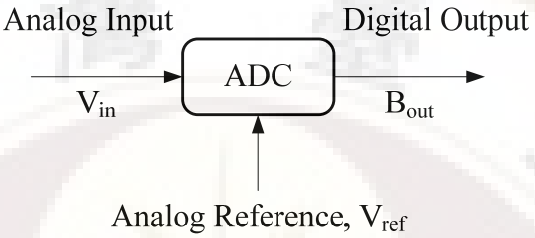


Fig. 3 A block diagram representing a D/A converter.

For an A/D converter, the following equation relates these signals,

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm V_x \tag{7.5}$$

where

$$-\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB} \tag{7.6}$$

Note that there is now a range of valid input values that produce the same digital output word. This signal ambiguity produces what is known as *quantization error*. Also, note that no quantization error occurs in the case of a D/A converter since the output signals are well defined.

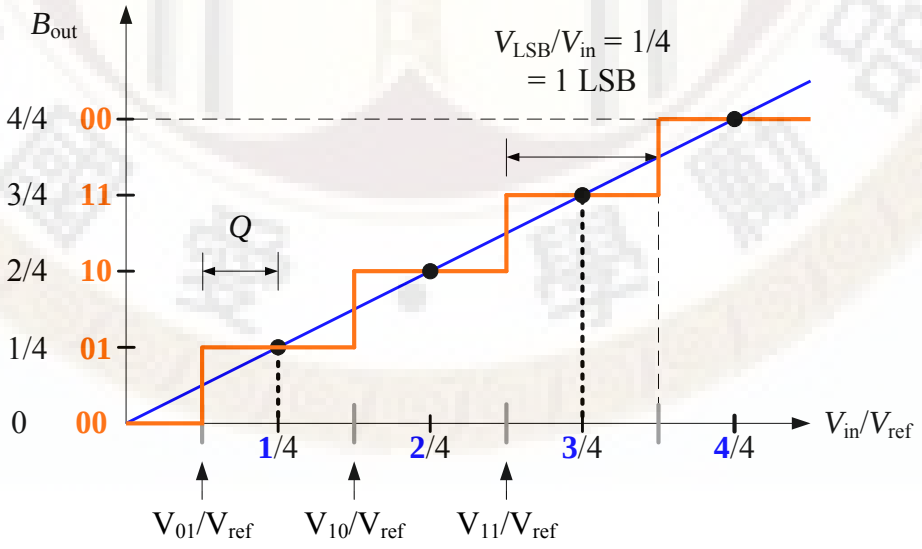


Fig. 4 Input-Output transfer curve for a 2-bit A/D converter.

Of course, quantization errors will occur if a 6-bit D/A converter is used to convert a 10-bit digital signal, but in this case, the quantization error occurs in the conversion from a 10-bit digital signal to a 6-bit digital signal.

A transfer curve for an A/D converter can be sketched as shown in Fig. 4 for a 2-bit converter. Note that the transitions along the Vin axis are offset by 1/2VLSB, so that the midpoints of the staircase curve fall precisely on the equivalent D/A converter curve.

Here, we define the transition voltage at V_{ij}, where the subscript ij indicates the upper Bout value of the transition. For example, V_{01} is shown in Fig. 4 as the voltage (normalized with respect to V_{ref}) for the transition from 00 to 01.

Finally, it should be noted that the relation shown in (7.6) holds only if the input signal remains within 1 LSB of the two last transition voltages. Specifically, for the 2-bit transfer curve shown in Fig. 4, V_{in} should remain less than 7/8 V_{ref} and greater than –1/8 V_{ref}. Otherwise, the quantizer is said to be *overloaded* since the magnitude of the quantization error would be larger than $V_{LSB}/2$.

3. Quantization Noise

As mentioned in section 2, quantization errors occur even in ideal A/D converters. In this section, we model these errors as being equivalent to an additive noise source and then find the power of this noise source.

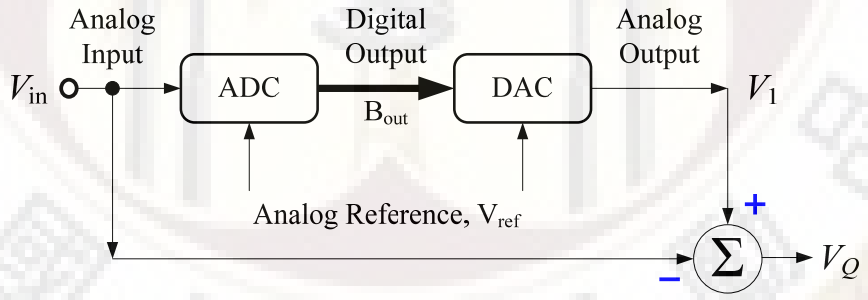


Fig. 5 A circuit to investigate quantization noise behavior

Consider the setup shown in Fig. 5, where both N-bit converters are ideal. Since we have

$$V_Q = V_1 - V_{in} \tag{7.7}$$

we can rearrange this equation as

$$V_1 = V_Q + V_{in} \tag{7.8}$$

Although this rearrangement is trivial, it has important implications because (7.8) shows that the quantized signal, V_1, can be modelled as the input signal, V_{in},

plus some additive quantization noise signal, V_Q.

Note that (7.8) is exact because no approximations have been made here. The quantization noise modelling becomes approximate once some assumptions are made about the statistical properties of V_Q.

4. Resolution

The *resolution* of a converter is defined to be the number of distinct analog levels corresponding to the different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels. Resolution is not necessarily an indication of the accuracy of the converter, but instead it usually refers to the number of digital input or output bits.

5. Offset

In a D/A converter, the *offset error*, E_{off}, is defined to be the output that occurs for the input code that should produce zero output, or mathematically,

$$E_{\text{off(D/A)}} = \left.\frac{V_{\text{out}}}{V_{\text{LSB}}}\right|_{0\ldots0}$$

where the offset error is in units of LSBs.

Similarly, for an A/D converter, the offset error is defined as the deviation of $V_{0..01}$ from 1/2 V_{LSB}, or mathematically,

$$E_{\text{off(A/D)}} = \frac{V_{0\ldots01}}{V_{\text{LSB}}} - \frac{1}{2}\text{LSB}$$

6. Gain Error

The *gain error* is defined to be the difference at the full-scale value between the ideal and actual curves when the offset error has been reduced to zero.

For a D/A converter, the gain error, $E_{gain(D/A)}$, in units of LSBs, is given by

$$E_{\text{gain(D/A)}} = \left(\left.\frac{V_{\text{out}}}{V_{\text{LSB}}}\right|_{1\ldots1} - \left.\frac{V_{\text{out}}}{V_{\text{LSB}}}\right|_{0\ldots0}\right) - \left(2^N - 1\right)$$

Similarly, for an A/D converter, the equivalent gain error, $E_{gain(A/D)}$, in units of LSBs, is given by

$$E_{\text{gain(A/D)}} = \left(\frac{V_{1\ldots1}}{V_{\text{LSB}}} - \frac{V_{0\ldots1}}{V_{\text{LSB}}}\right) - \left(2^N - 2\right)$$

Graphically illustrations of gain and offset errors are shown in Fig. 5

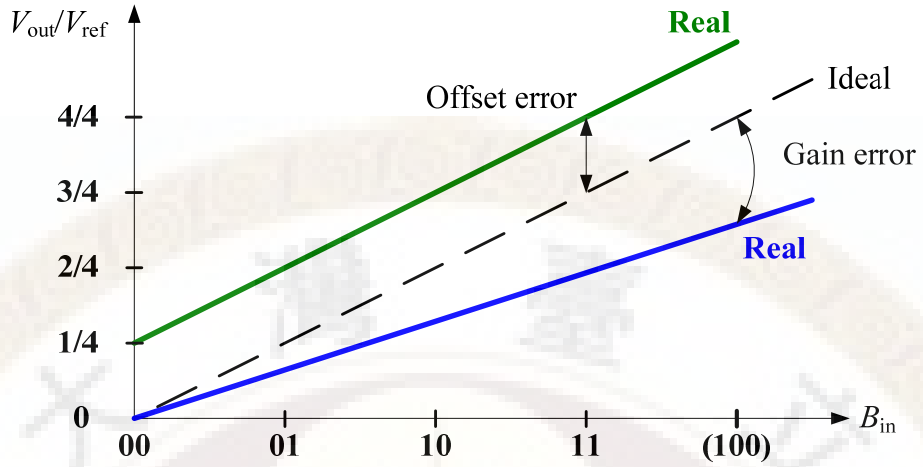


Fig. 5 Illustrating offset and gain errors for a 2-bit D/A converter

7. Accuracy and Linearity

The *absolute accuracy* of a converter is defined to be the difference between the expected and actual transfer responses. The absolute accuracy includes the offset, gain, and linearity errors.

The term relative accuracy is sometimes used and is defined to be the accuracy after the offset and gain errors have been removed. It is also referred to as the *maximum integral nonlinearity error* (described later) and we will refer to is as such.

Accuracy can be expected as a percentage error of full-scale value, as the effective number of bits, or as a fraction of a LSB. For example, a 12-bit accuracy implies that the converter's error is less than the full-scale value divided by 2^{12}.

8. Linearity

Integral Nonlinearity (INL) Error

After both the offset and gain errors have been removed, the integral nonlinearity (INL) error is defined to the deviation from a straight line. However, what straight line should be used? A conservative measure of nonlinearity is to use the endpoints of the converter's transfer response to define the straight line.

An alternative definition is to find the best-fit straight line such that the maximum difference (or perhaps the mean squared error) is minimized.

These two definitions are illustrated in Fig. 6. One should be aware that, we define INL values for each digital word (and thus these values can be plotted for a

single converter), whereas others sometimes define the term "INL" as the maximum magnitude of the INL values (or equivalently, as the relative accuracy).

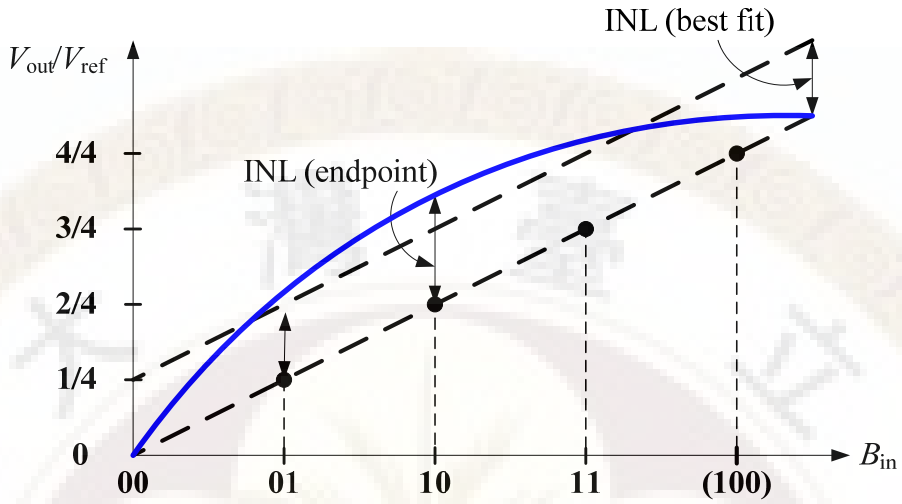


Fig. 6 Integral Nonlinear (INL) Error in a 2-bit D/A converter

Typically INL is measured by slowly sweeping the converter input over its full-scale range; hence it is a measure of the converter's accuracy only at low input signal frequencies.

9. A/D Conversion Time and Sampling Rate

In A/D converter, the *conversion time* is the time taken for the converter to complete a single measurement including acquisition time of the input signal. On the other hand, the maximum *sampling rate* is the speed at which samples can be continuously converted and is typically the inverse of the conversion time.

However, one should be aware that some converters have a large latency between the input and the output due to pipelining and multiplexing, yet they still maintain a high sampling rate. For example, a pipelined 12-bit A/D converter may have a conversion time of 2 ns (i.e., a sampling rate of 500 MHz) yet a latency from input to output of 24 ns.

10. D/A Settling Time and Sampling Rate

In D/A converter, the *settling time* is defined as the time is takes for the converter to settle to within some specified amount of the final value (usually 0.5 LSB). The *sampling rate* is the rate at which samples can be continuously converted and is typically the inverse of the settling time.

Instrument Requirement

Instrument	Quantity	Components	Quantity
Oscilloscope	1	Power supplier	2
Multi-meter	1	Function Gen.	1

Components Requirement

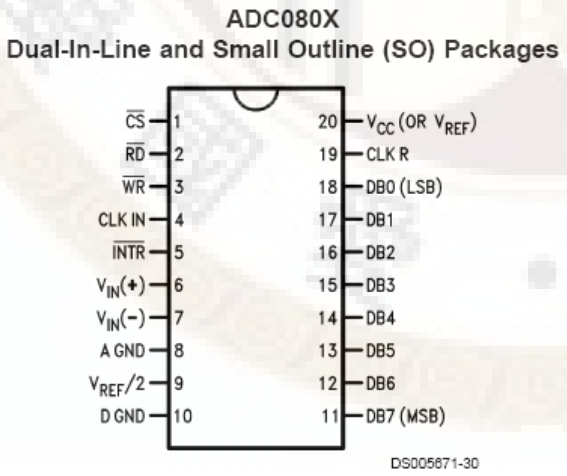
Components	Quantity	Components	Quantity
μA 741	1	100pF (100)	1
DAC 0800	1	10 kΩ	1
ADC 0804	1	3 kΩ	2
0.1 μF (104)	2	VR (10 *k*Ω)	1
10 μF	2	LEDs	8
50 pF (50)	1	1.2 kΩ (or 330~500Ω)	8

Instrument confirmation

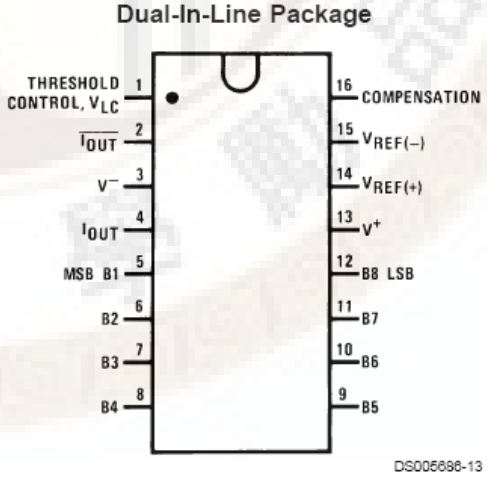
Before you proceed to any part of the experiment, please remember to do the **Instrument Examinations** to the instruments before performing any experiment. The examining procedures are shown in experiment 1.

Components confirmation

1. PINOUT Diagram

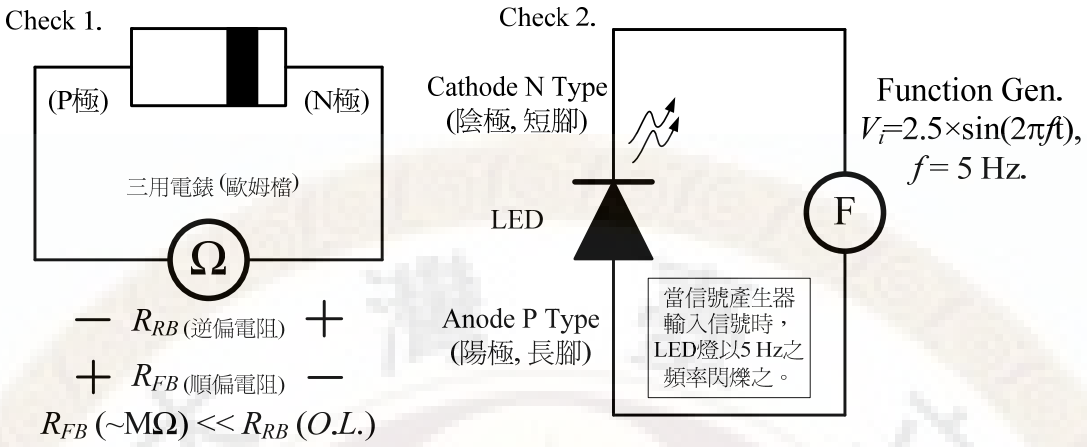


ADC0804



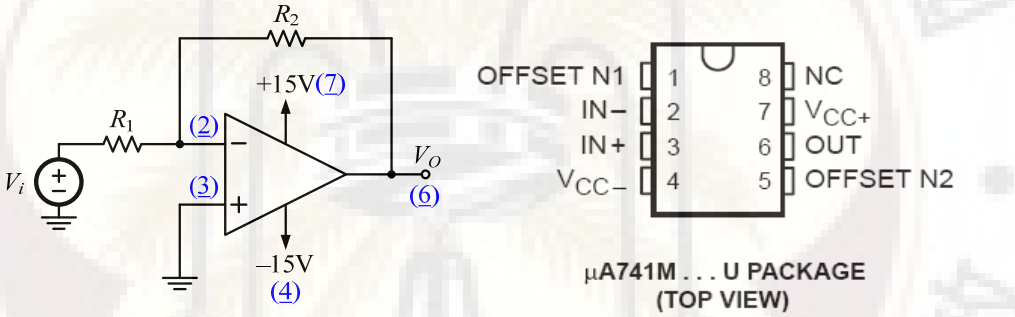
DAC0800

2. Functional confirmation of LED



※ ***Note***: Please do not directly provide DC power with LED. Otherwise it will be easily damaged.

3. μA741－PINOUT & Functional confirmation



$$Check\ 1.\ A_V = \frac{V_o}{V_i} \overset{?}{=} -\left(\frac{R_2}{R_1}\right)$$

$$Check\ 2.\ f_{3dB} \overset{?}{=} 100kHz \sim 500kHz$$

※ ***Note***: Recall the expression of gain－bandwidth product: $A_V \times f_{3dB}$=constant, that is, f_{3dB} will reduce as A_V increases. If the results of confirmation appear the same as those shown in check 1 and 2, the μA741 chip of OP amp is workable.

Lab Work

1. ADC0804 Testing circuit

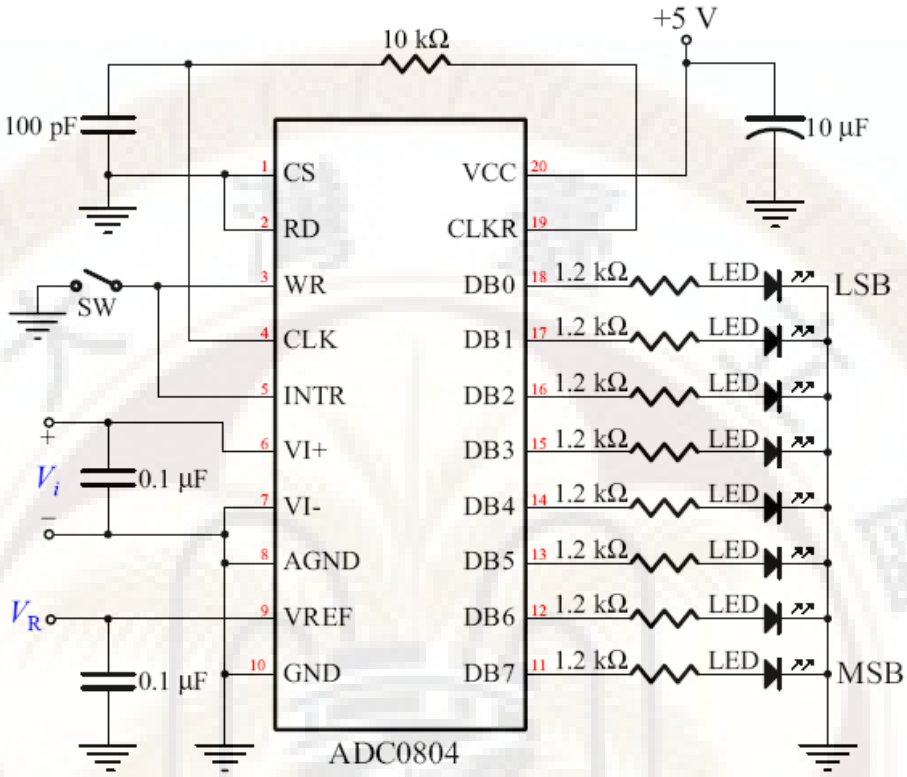


Fig. 1 ADC0804 Testing circuit

Note: If the LEDs are not easy to visualize, try to change the current limited resistance 1.2 *k*Ω to the values from 330 Ω~ 500 Ω.

2. Rest ADC0804
   (1) In Fig. 1, SW open. (i.e., do not connect pin 3 and pin 5 to ground.)
   (2) Supply voltage V_{CC} = +5V.
   (3) At step (2), all the LEDs or part of the 8-LED will turn ON. (亮)
   (4) SW close in a short period (i.e., reset the ADC0804 chip for a second).
   (5) SW open. (i.e., disconnect pin 3 and pin 5 from ground.)
   (6) At step (5), all the LEDs will turn OFF. (暗).

3. Measure the voltage as full load. (No need to perform)
   (1) Supply voltage signal V_{in} = 0V, and V_R.
   (2) Slowly increase V_R from 2.5V to 5V.
   (3) Observe whether the digital output (LEDs) can mutually radiate. If they are not so, try to change a new ADC0804 chip.
   (4) Adjust V_R as the digital output just equals to 1111-1111.

(5) Record V_R = _____V.

4. Measure Analog voltage value to Digital output
   (1) Set V_R = +2.5V and V_{in} = 0 ~ 2.5V.
   (2) Slowly increase V_{in} from 0 to 5V, and record the V_{in} by using the multimeter with the corresponding output in the following table.
   (3) Maintain the circuit in breadboard, and do not disconnect or unplug any devices.

Analog input V_{in} (V) (Use Multimeter)	Digital output (Binary)	Digital output (Decimal)
	0000 0001	1
	0000 0010	2
	0000 0100	4
	0000 1000	8
	0001 0000	16
	0010 0000	32
	0100 0000	64
	1000 0000	128

※ *Homework* #1: Apply the measured data from the above table in the editing software such as EXCEL and MATLAB, and plot the diagram of decimal digital output versus analog input.

5. DAC0800 Testing circuit

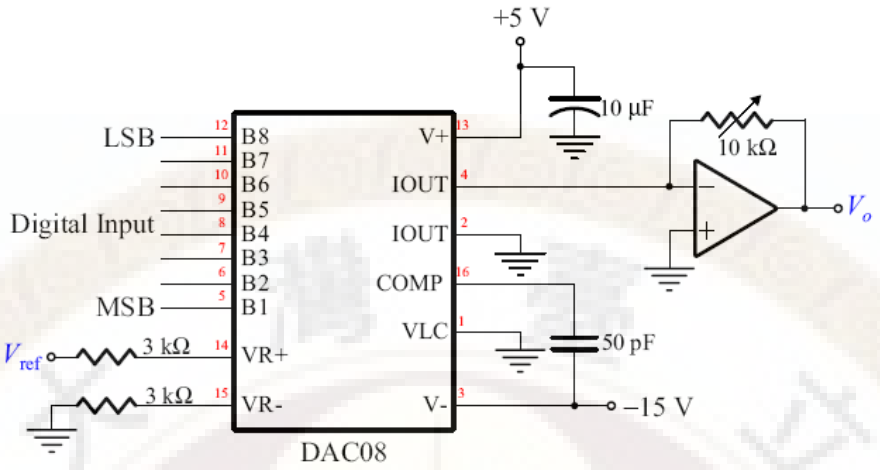


Fig. 2 DAC0800 Testing circuit

(1) In Fig. 2, supply V_{DD} = +5V, V_{ref} = +5V for DAC circuit and V_+ = +15V, V_- = −15V for μA741 OP Amp.

(2) Input 1111-1111 to the digital input terminals.
(Hint: In the circuit, Logic 1 = +5V, Logic 0 = 0V.)

(3) Adjust VR 10 $k\Omega$, use multi-meter ►V_{out} changed ? (Y/N) ► If V_{out} is not changed, try to trouble shoot the circuit in the breadboard.

(4) Carefully adjust VR 10 $k\Omega$ to have V_{out} = +5V.

(5) Record the value of VR = _____ $k\Omega$.

(6) Refer to the following table and change the digital input.

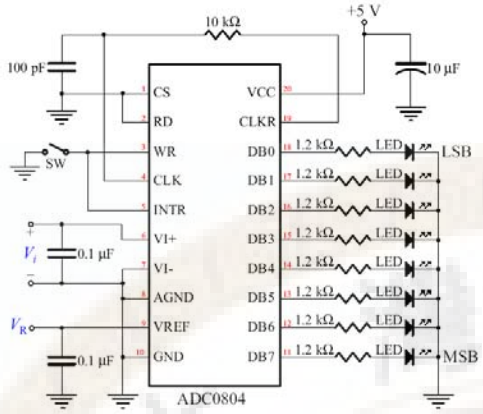
(7) Record the V_{out} by using the multimeter in the following table.

(8) Maintain the circuit in breadboard, and do not disconnect, unplug or adjust any devices.

Digital iutput (Binary)	Digital iutput (Decimal)(V)	Analog output V_{out} (V) (Use Multimeter)
0000 0001	1	
0000 0010	2	
0000 0100	4	
0000 1000	8	
0001 0000	16	
0010 0000	32	
0100 0000	64	
1000 0000	128	

※ *Homework* #2: Apply the measured data from the above table in the editing software such as EXCEL and MATLAB, and plot the diagram of decimal digital input versus analog output.

6. Connection of Fig. 1 + Fig. 2



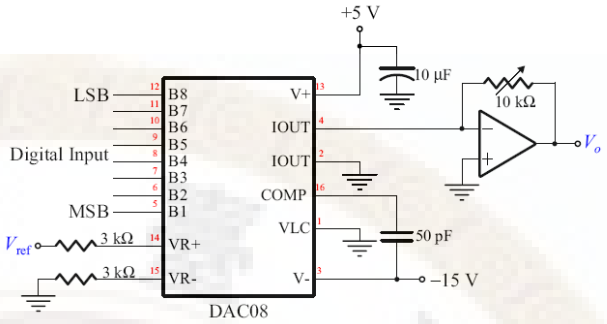


Fig. 1 ADC0804 Testing circuit Fig. 2 DAC0800 Testing circuit

(1) Connect DB7(MSB) in ADC0804 test circuit to B1(MSB) in DAC0800 test circuit, DB6 to B2 ... ,and DB0(LSB) to B8(LSB), respectively.

(2) Short the ground in Fig. 1 and Fig. 2 with each other.

(3) Do not unplug the current limited resistance 1.2 *k*Ω and the LEDs in ADC0804 testing circuit.

7. Rest ADC0804

(4) In Fig. 1, SW open. (i.e., do not connect pin 3 and pin 5 to ground.)

(5) In Fig. 1, supply voltage V_{CC} = +5V.

(6) SW close in a short period (i.e., reset the ADC0804 chip for a second).

(7) SW open. (i.e., disconnect pin 3 and pin 5 from ground.)

8. Measure Analog voltage V_{in} to V_{out}

(8) In Fig. 1, supply voltage V_R = +2.5V.

(9) Slowly increase V_{in} from 0 to 5V just as the LEDs are sparkled as the following table. Record V_{in} and V_{out} by using the same multimeter and fill up the following table.

Analog input V_{in} (use the same meter)	Digital output (Binary)	Analog output V_{out} (use the same meter)	Quantization Error, $V_Q = V_{out} - V_{in}$
	0000 0001		
	0000 0010		
	0000 0100		
	0000 1000		
	0001 0000		
	0010 0000		
	0100 0000		
	1000 0000		

※ *Homework* #3: Apply the measured data from the above table in the editing software such as EXCEL and MATLAB, and plot the diagram of V_Q vs V_{in} and verify what type of the quantization error had occurred in your circuit.

Reference

1. A.S. Sedra and K.C. Smith, *Microelectronic Circuits*, 6th ed., Oxford University Press publishing, New York, 2011.
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4. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer (Author), *Analysis and Design of Analog Integrated Circuits*, 5th ed., Wiley, January 20, 2009.
5. Tony Chan Carusone, David Johns, Kenneth W. Martin, *Analog Integrated Circuit Design*, 2nd International student edition, John Wiley & Sons, April 23, 2012.