Experiment

3

CMOS Operational Amplifier (1)：DC Analysis

Objectives

To make sure all the MOS of the circuit are able to *enter saturation region* so that the circuit can be applied to be an operational amplifier.

Overview

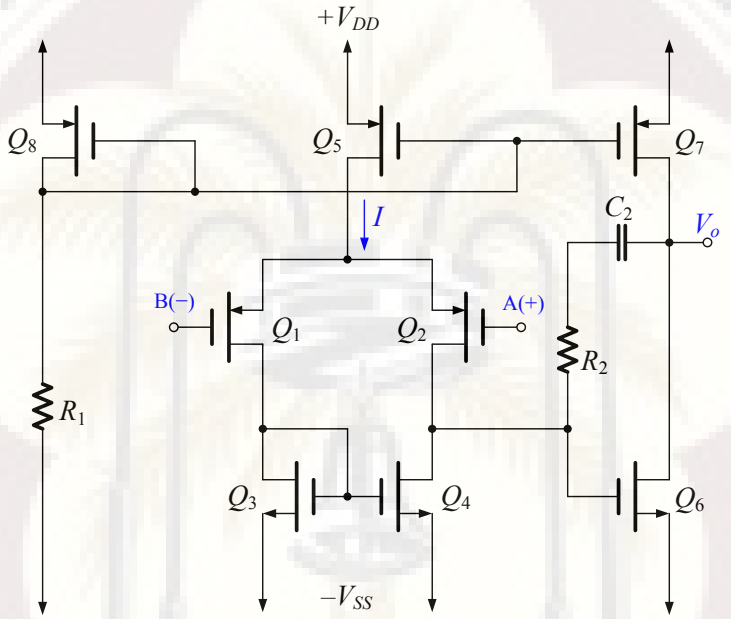


Fig. 1 Two-stage CMOS operational amplifier

In Fig. 1, (Q_5, Q_7, Q_8) is a current mirror which provides the essential current to the differential pair (Q_1,Q_2) and common-source amplifier Q_6. Additionally, (Q_3, Q_4) is another current mirror of the circuit, which is the active load of the differential pair (Q_1,Q_2). The main function of R_2 and C_2 is to compensate the frequency response.

Components and Instrumentation

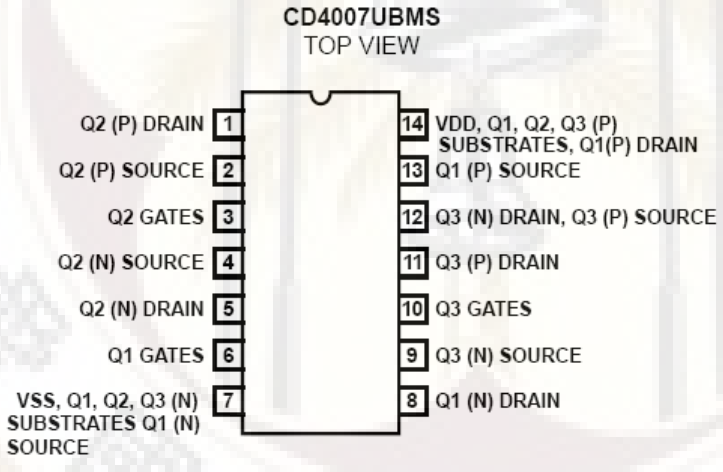
Instrument	Quantity	Components	Quantity
Oscilloscope	1	CD 4007	3
Multi-meter	1	VR (可變電阻) (1 kΩ)	1
Power supplier	1	10 kΩ	1
Function Gen.	1	1 kΩ	1
		18 kΩ	2

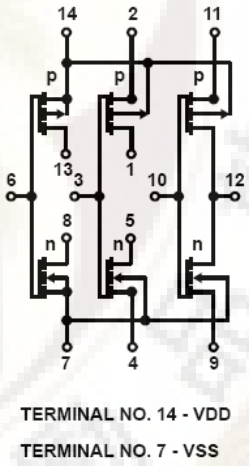
Instrument confirmation

Before you proceed to any part of the experiment, please remember to do the **Instrument Examinations** to the instruments before performing any experiment. The examining procedures are shown in experiment 1.

Lab Work

1. CD4007－PINOUT





※***Note***: Always supply voltage $-V_{SS} = -8V$ in pin 7 and $V_{DD} = +8V$ in pin 14 for every chip of CD4007. The experimental results will be unreasonable if the above notice has not been followed.

2. Circuit implementation

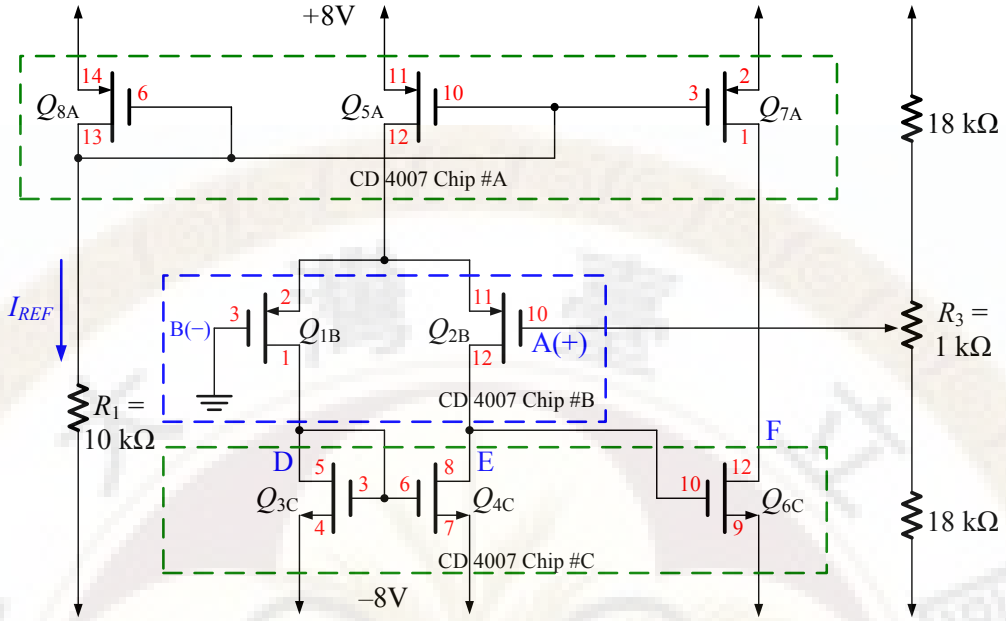


Fig. 2 Circuit implementation of Two-stage OP-Amp

(1) Employ CD4007 Chip #A to implement (Q_5, Q_7, Q_8), Chip #B to implement (Q_1, Q_2), and Chip #C for (Q_3, Q_4, Q_6)

(2) Supply voltage $-V_{SS}$ = –8V (pin7) and V_{DD} = +8V (pin 14) for CD4007 chips.

3. DC Analysis of CD4007

(1) The condition of entering saturation region of NMOS: $V_{GD} \leqq V_T$ (1.8V).

(2) The condition of entering saturation region of PMOS: $V_{GD} \geqq V_T$ (–1.8V).

(3) Supply voltage $-V_{SS}$ = –8V and V_{DD} = +8V to the circuit.

(4) Use digital multi-meter to confirm whether all of the MOS components are able to enter saturation region as adjusting VR 1 kΩ.

(5) If it is so, go to step 6, else go to next step.

4. Detail procedure of DC Analysis of the Two-stage OP-Amp circuit

(1) DC Analysis of the current mirror (Q_5, Q_7, Q_8)

a. In Fig. 3, adjust VR (R_2) 10 kΩ and check whether (Q_5, Q_7, Q_8) are all able to enter saturation region, that is, $V_{GD5,7,8} \geqq V_T$ (–1.8V). If one of them is not so, change the chip of CD4007 #A and recheck again.

b. Use multi-meter (三用電錶) to measure V_{GD5}, V_{GD7}, V_{GD8}

c. Record V_{GD5} = _____V, V_{GD7} = _____V, V_{GD8} = _____V.

Analysis

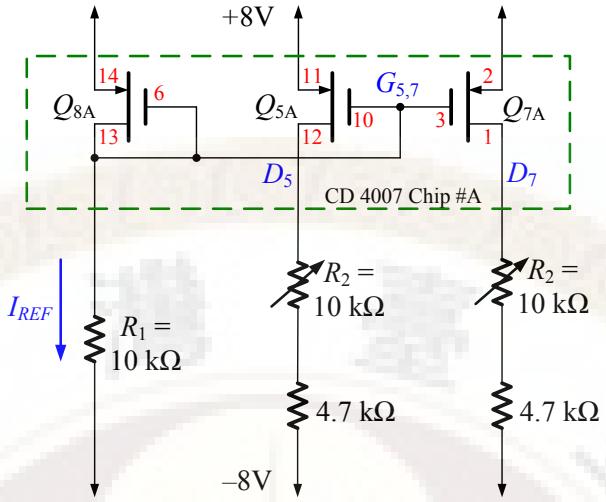


Fig. 3 DC Analysis of the current mirror (Q_5, Q_7, Q_8)

$\because V_{SG8} = V_{SG5} = V_{SG7}$, *If* $Q_8 = Q_5 = Q_7$, *then* $I_{D8} = I_{D5} = I_{D7} = I_{REF}$.

$V_{G5} = V_{G7} = V_{G8} = V_{D8} = -8V + I_{REF} \times R_1$,

$V_{D5} = V_{D7} = -8V + I_{REF} \times (R_2 + 4.7k\Omega)$,

$\rightarrow V_{GD5} = V_{G5} - V_{D5} = I_{REF} \times [(R_1 - R_2) + 4.7k\Omega] ? \geq V_T(-1.8V)$.....(1)

If eq.(1) *can not be true, that means* I_{REF} *is not big enough or* I_{REF} *is equal* 0, *that is, the current mirror does not work.*

(2) DC Analysis of the differential pair (Q_1,Q_2)

a. In Fig. 4, adjust VR (R_2) 10 kΩ and check whether (Q_1, Q_2) are both able to enter saturation region, that is, $V_{GD1,2} \geqq V_T$ (–1.8V). If one of them is not so, change the chip of CD4007 #B and recheck again.

b. Use multi-meter (三用電錶) to measure V_{GD1}, V_{GD2}.

c. Record V_{GD1} = _____V, V_{GD2} = _____V.

Analysis

$\because V_{SG8} = V_{SG5}$ *and* $V_{SG1} = V_{SG2}$, *If* $Q_8 = Q_5$ *and* $Q_1 = Q_2$,

then $I_{D8} = I_{D5} = I_{REF}$, $I_{D1} = I_{D2} = \frac{I_{REF}}{2}$,

$V_{G1} = V_{G2} = 0V, V_{D1} = V_{D2} = -8V + I_{D1} \times R_2$,

$\rightarrow V_{GD1} = V_{G1} - V_{D1} = 8 - I_{D1} \times R_2 = 8 - \frac{I_{REF}}{2} \times R_2 ? \geq V_T(-1.8V)$.....(2)

If eq.(2) cannot be true, that means $I_{D1} \times R_2$ can not be small enough.

It is possibly that R_2 is too big or (Q_1, Q_2) mismatch, try to change smaller R_2 or change a new chip#B.

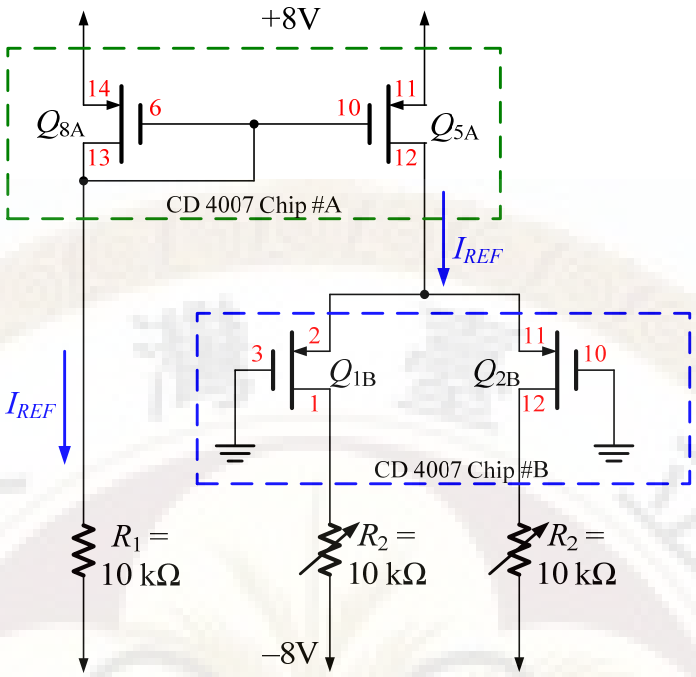


Fig. 4 DC Analysis of the differential pair (Q_1, Q_2)

(3) DC Analysis of the active load (Q_3, Q_4)

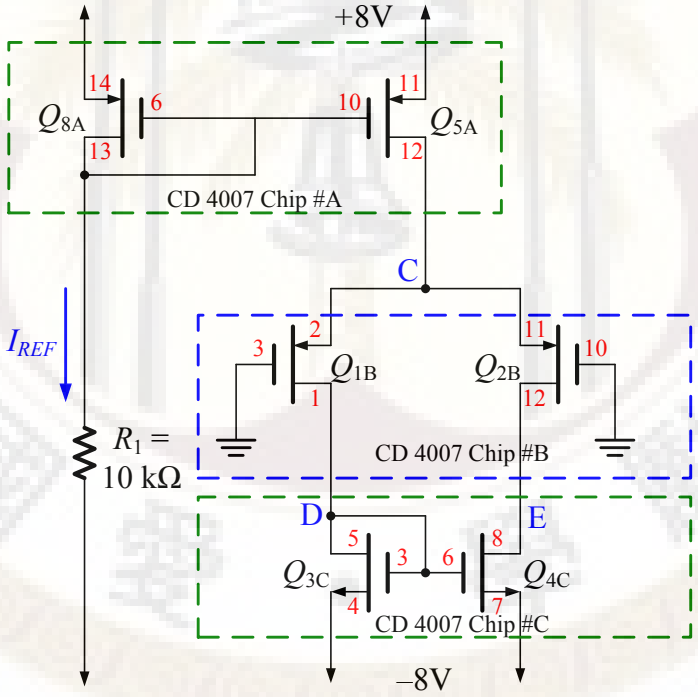


Fig. 5 DC Analysis of the active load (Q_3, Q_4)

a. In Fig. 5, Use multi-meter (三用電錶) to check whether (Q_3, Q_4) are both able to enter saturation region, that is, $V_{GD3,4} \geqq V_T$ (–1.8V). If one of them is not so, change the chip of CD4007 #C and recheck again.

b. Record V_{GD1} = _____V, V_{GD2} = _____V, V_{GD3} = _____V, V_{GD4} = _____V.

c. Record V_C = _____V, V_D = _____V, V_E = _____V.

Analysis

$\because V_{SG8} = V_{SG5}$ *and* $V_{SG1} = V_{SG2}$, *If* $Q_8 = Q_5$, $Q_1 = Q_2$, *and* $Q_3 = Q_4$,

then $I_{D8} = I_{D5} = I_{REF}$, $I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{REF}}{2}$,

$V_{G3} = V_{D3} \rightarrow V_{GD3} = 0 \rightarrow Q_3$ *will always be saturated.*

$V_{G4} = V_{G3} = V_{D1} = -8V + I_{D1} \times R_{DS3}, V_{D4} = -8V + I_{D1} \times R_{DS4}$,

$\rightarrow V_{GD4} = V_{D1} - V_{D4} \approx 0 \ \leq V_T(1.8V)$.....(3)

$$R_{DS4} = \left(\frac{\Delta i_{D4}}{\Delta v_{DS4}}\right)^{-1} = \left(\frac{\partial}{\partial v_{DS4}}\left\{k_n'\left(\frac{W}{L}\right)\left[(v_{GS4} - V_T)v_{DS4} - \frac{1}{2}v_{DS4}^2\right]\right\}\right)^{-1}$$

$$\rightarrow R_{DS4} = \left\{k_n'\left(\frac{W}{L}\right)\left[(v_{GS4} - V_T) - \frac{1}{2}v_{DS4}\right]\right\}^{-1}$$

If eq. (3) *can not be true, that means there is something wrong with* Q_{4C}.
Try to change a new chip#C.

5. DC Analysis of the Two-stage OP-Amp circuit

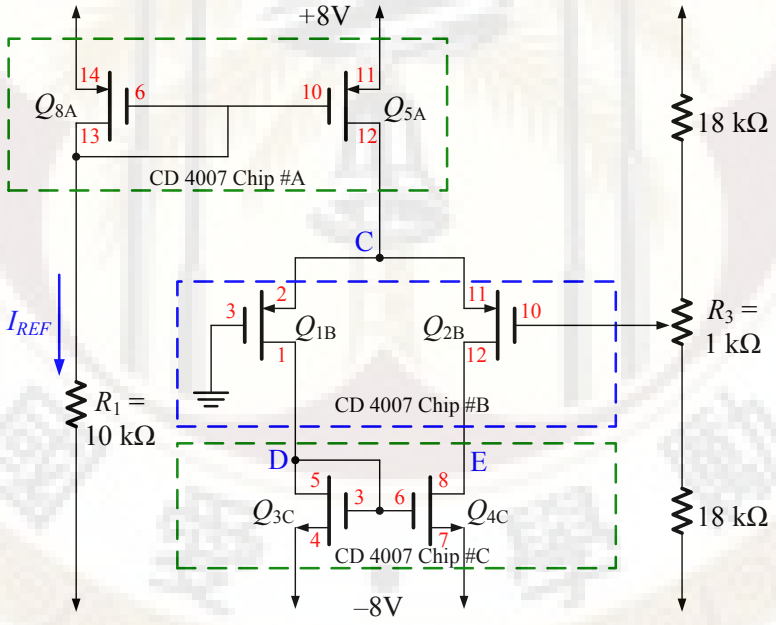


Fig. 6 DC Analysis of Two-stage OP-Amp circuit

a. In Fig. 6, adjust VR (R_3) 1 *k*Ω and use multi-meter to measure V_A and V_E, and check whether V_E is adjustable. If it not so, trouble shoot the circuit. Check whether there is any wrong layout in your breadboard and whether the VR (R_3) is functional by multimeter.

b. Referenced value of V_A is around (-0.25V, 0.25V), V_E is around (0.25V,

-7.5V). Record V_A = (____V, ____V) and V_E = (____V, ____V).

6. Circuit implementation

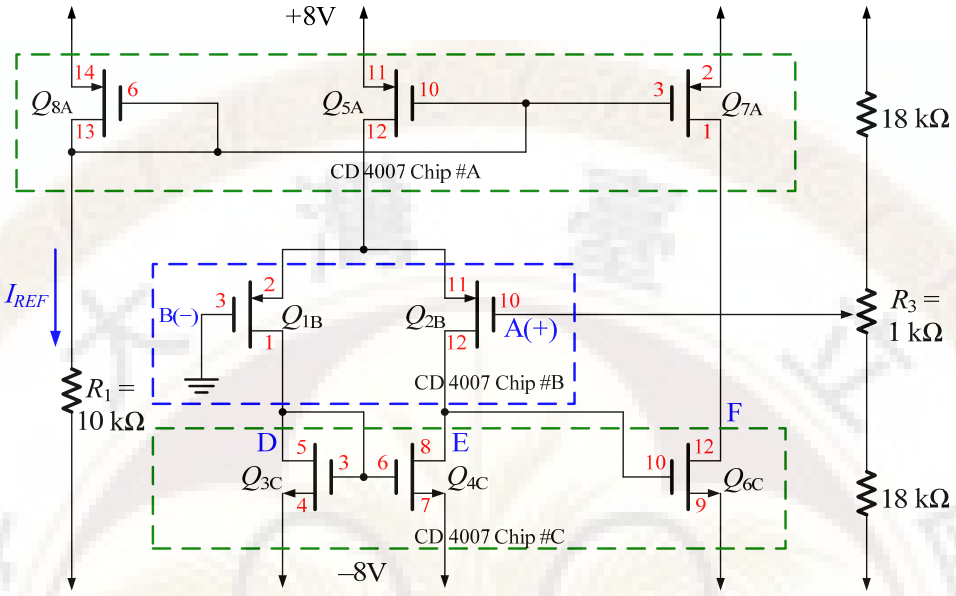


Fig. 2 DC Analysis of Two-stage OP-Amp circuit

a. In Fig. 2, adjust VR (R_3) 1 $k\Omega$ and use multi-meter to measure V_A, V_D, V_E.

b. Referenced value of V_A is around (−0.25V, 0.25V), V_E is around (0.25V, −7.5V), and V_F is around (−7.5V, 7.5V)

c. Adjust VR (R_3), and record V_A, V_E, V_F in the following table.

V_A (V)	V_E (V)	V_F (V)	V_A (V)	V_E (V)	V_F (V)

Homework #1: Apply the measured data from the above table to the editing software such as EXCEL and MATLAB, and illustrate the *DC-sweep diagram* similar to Fig. 7 with marking the corresponding voltage. Try to calculate the *slope rate* of the diagram in the transition region.

7. If the remaining time is allowed to do Exp 4 right away, go directly to the next chapter. Strongly suggest that you perform Exp. 4 right after this experiment.

8. If it is not so, it will be rather time-wasting to restart all the procedures shown in the experiment as you perform Exp. 4 next week, which is mainly to make sure all the MOS components are able to enter saturation region.

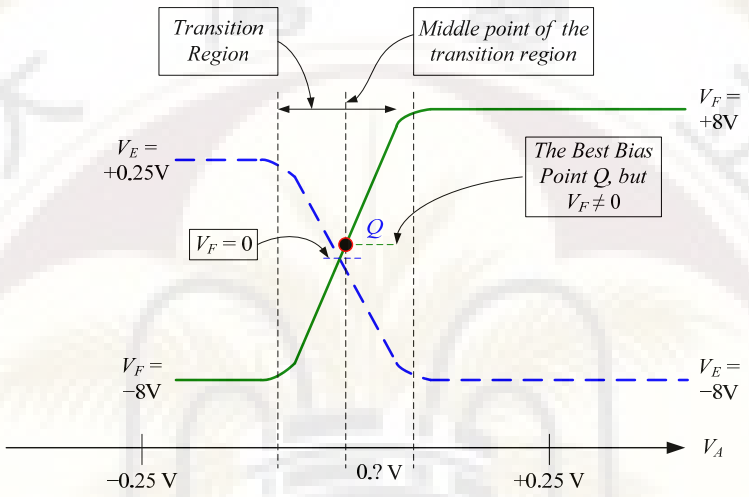


Fig. 7 DC-Sweep diagram

Reference

1. A.S. Sedra and K.C. Smith, *Microelectronic Circuits*, 6th ed., Oxford University Press publishing, New York, August 2011.
2. A.S. Sedra and K.C. Smith, *Laboratory Manual for Microelectronic Circuits*, 3rd ed., Oxford University Press publishing, New York, 1997.