Digital Systems

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ECSE 325

Lab #3: Timing constraint specification and timing analysis using TimeQuest

Winter 2018

Introduction

In this lab, you will practice how to implement a digital FIR filter in VHDL and perform test bench simulations using ModelSim. It is strongly recommended for the students to prepare ahead of time to demonstrate their work during the 2-hour lab session.

Digital Filters

Digital filters are a very important part of digital signal processing (DSP). Digital filters have two uses: signal separation and signal restoration.

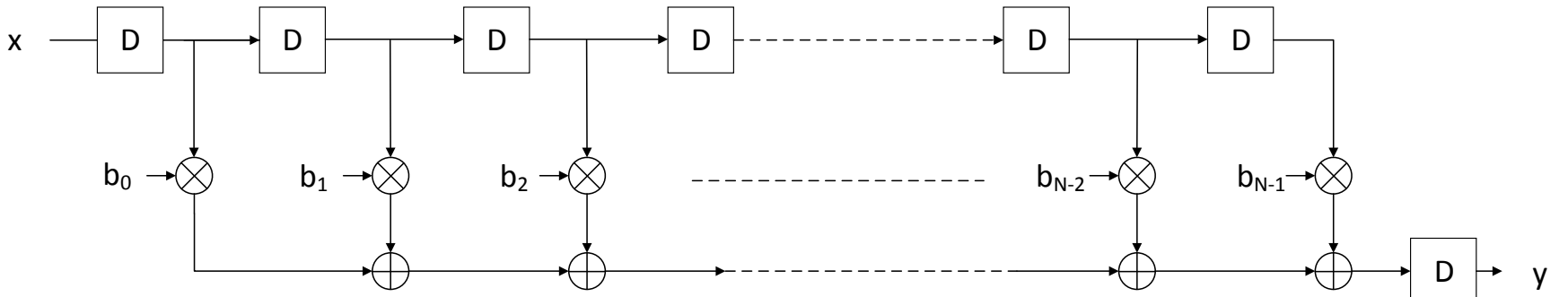
- Signal separation is needed when a signal has been contaminated with interference, noise, or other signals. For example, imagine a device for measuring the electrical activity of a baby's heart while still in the womb. The raw signal will likely be corrupted by the breathing and heartbeat of the mother. A filter might be used to separate these signals so that they can be individually analyzed.
- Signal restoration is used when a signal has been distorted in some way. For example, an audio recording made with poor equipment may be filtered to better represent the sound as it actually occurred. Another example is the deblurring of an image acquired with an improperly focused lens, or a shaky camera.

FIR Filters

The most straightforward way to implement a digital filter is by convolving the input signal with the digital filter's impulse response. Filters carried out by convolution are called Finite Impulse Response (FIR) filters. An FIR filter is a filter whose response to any finite length input is of finite period. For a causal discrete-time FIR filter of order N, each value of the output sequence is a weighted sum of the most recent input values:

$$y(n) = \sum_{i=0}^{N} b_i \times x(n-i),$$

where $x(n)$ and $y(n)$ are input and output signals, respectively. The weights are also denoted by b_i.



FIR Filters–Implementation

In this lab, you will implement a bandpass FIR filter with order 25 (25-tap FIR filter) to restore a sine wave corrupted by a white noise. You are provided with two text files containing the filter's input and weights in floating-point format. Given the block diagram of an N-tap filter in Fig. 1, implement the 25-tap FIR filter in VHDL while representing the filter's input, output signals and weights in the fixed-point representations (1,15), (2,15) and (1,15), respectively.
Note: Use constant parameters to represent the weights.

```
entity gNN_FIR is
port ( x      : in  std_logic_vector (15 downto 0); -- input Signal
       clk    : in  std_logic; -- clock
       rst    : in  std_logic; -- asynchronous active-high reset
       y      : out std_logic_vector (16 downto 0)); -- output signal
end gNN_FIR;
```

FIR Filters–Simulation

Once you have implemented your design in VHDL, you need to verify its functionality by writing a testbech code. In the testbench code, you will read the given test vector in your testbench and obtain an output test vector.

When you have finished the VHDL codes, show them to the TA.

Writeup the Lab Report

You are required to submit a written report and your code to myCourses on the first Friday after the Lab3 period at midnight.

- The report in the electronic file should be in PDF format.
- The report should be written in the standard technical report format.
- Document every design choice clearly.
- Everything should be organized for the grader to easily reproduce your results by running your code through the tools.
- The code should be well-documented and easy to read.
- The grader should not have to struggle to understand your design.

Writeup of the Lab Report - cont'd

Please refer to the example lab report from myCourses content for an example lab report template.

Your report must include:

- An introduction in which the objective of the lab is discussed
- The VHDL code you wrote for the 25-tap FIR filter
- Discussion on the resource utilization of your design (i.e. how many registers are used and why? What changes would you respect in the resource utilization if you increased the bit size of the counter?)
- Testbench VHDL code to verify your filter design

Grading Sheet

Group Number:
Name 1:
Name 2:

Task	Grade	/Total	Comments
VHDL for 25-tap FIR		/50	
Testbench VHDL		/50	