3-V to 36-V Input, 3-A Synchronous Step-Down Regulator with 6-µA Ultra-Low Quiescent Current

Features

- AEC-Q100 Grade 1 Qualified for Automotive Applications
- Wide Input Voltage Range: 3 V to 36 V
- 3-A Continuous Output Current Capability
- 6-µA Ultra-Low Operating Quiescent Current
- 1-V ±1% Reference Voltage Accuracy
- 35-ns Ultra-Low Minimum On Time
- Fixed Switching Frequency: 400 kHz, 1.4 MHz, 2.1 MHz
- Integrated 90-mΩ High-Side and 60-mΩ Low-Side Power MOSFETs
- Optional Frequency Spread Spectrum to Reduce EMI
- Low Drop-out Mode Operation
- Precision Enable and Input Voltage UVLO
- Cycle-by-Cycle Current Limit and Hiccup When Overload or Short Circuit
- Available in the QFN2X3-12 Package

Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance Systems
- Body Electronics

Description

The TPP36307Q is a high-efficiency synchronous step-down regulator with integrated high-side and low-side MOSFETs. It provides up to 3-A output current with peak current mode control for fast loop response.

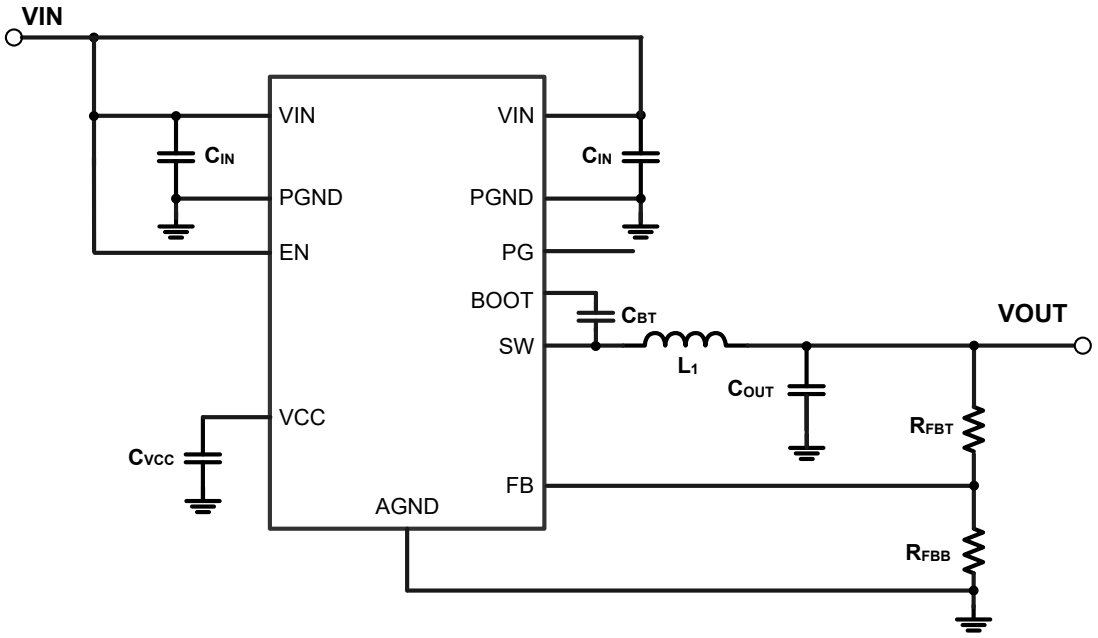
The TPP36307Q operates over a wide input voltage range from 3 V to 36 V with only 6-µA ultra-low quiescent current. It is ideal for automotive environments and battery-powered systems due to its extremely low quiescent current.

The TPP36307Q features 35-ns ultra-low minimum on time and low drop-out mode, which can maintain stable operation for high-frequency automotive conditions. EMI performance is specially optimized in the TPP36307Q. The device features a frequency spread spectrum method, optimized symmetrical pinout, and EMI-friendly package to optimize the EMI emissions.

The TPP36307Q has built-in robust protections such as thermal shutdown, UVLO, enable (EN) control, and power good (PG) indicator. Additionally, during the overload or short circuit condition, the cycle-by-cycle current limit and hiccup protections are provided. Thermal shutdown provides reliable and fault-tolerant operation.

The TPP36307Q is available in the QFN2x3-12 package.

Typical Application Circuit



3-V to 36-V Input, 3-A Synchronous Step-Down Regulator with 6-μA Ultra-Low Quiescent Current

Table of Contents

Product Family Table

Order Number	Switching Frequency
TPP363070Q-FC6R-S	400 kHz
TPP363071Q-FC6R-S	1.4 MHz
TPP363072Q-FC6R-S	2.1 MHz

Revision History

Date	Revision	Notes
2024-12-30	Rev A.0	Initial released.

Pin Configuration and Functions

TPP36307Q
QFN2X3-12
Top View

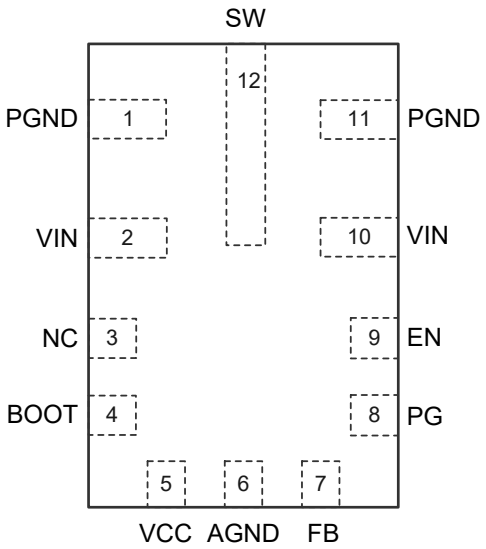


Table 1. Pin Functions: TPP36307Q

Pin No.	Name	I/O	Description
1, 11	PGND	G	Power ground pin. The reference ground of the internal power stage.
2, 10	VIN	P	Input voltage supply pin. Input capacitors should be placed as close to this pin and the PGND pin as possible.
3	NC	-	Not connected inside the regulator.
4	BOOT	O	High-side MOSFET gate supply pin. Recommend to connect a 0.1-μF ceramic capacitor between BOOT and SW pins.
5	VCC	O	Internal LDO output pin. The power supply for the driver and control circuits. Connect a ceramic bypass capacitor from this pin to AGND.
6	AGND	G	Analog ground pin. The reference ground of the internal control circuits. Connect to the power ground plane at the point of the ground of the VCC capacitor.
7	FB	I	Voltage feedback pin. Connect to the middle point of the feedback resistor divider to set the output value.
8	PG	O	Power good indicator pin with open-drain output. Connect a pull-up resistor to the system voltage rail.
9	EN	I	Enable input pin. The input signal to turn the regulator on or off, High = on, Low = off.
12	SW	O	Switching output pin. Connect this pin to the external inductor.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input	VIN	−0.3	42	V
	EN (2)	−0.3	VIN + 0.3	
	FB	−0.3	5.5	
	PG	−0.3	22	
Output	BOOT to SW	−0.3	5.5	V
	SW	−0.3	VIN + 0.3	
	SW (less than 100 ns)	−3.5	VIN + 0.3	
	VCC	−0.3	5.5	
	AGND to PGND	−0.3	0.3	
T_J	Junction Temperature	−40	150	°C
T_S	Storage Temperature	−55	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC-Q100-002 (1)	±2000	V
CDM	Charged Device Model ESD	AEC-Q100-011	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

Parameter		Min	Max	Unit
Buck Regulator	VIN	3	36	V
	VOUT	1	0.95*VIN	
	FB	0	5	
Control	EN	0	VIN	V
	PG	0	18	
T_A	Ambient Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
QFN2X3-12	75.4	20.1	49.5	°C/W

Electrical Characteristics

Unless otherwise noted, the min and max limits apply over the recommended operating ambient temperature range (T_A) of −40°C to 125°C. Typical values are measured under T_A = 25°C and represent the most likely parameters normally for reference. The default test conditions: V_{IN} = 12 V.

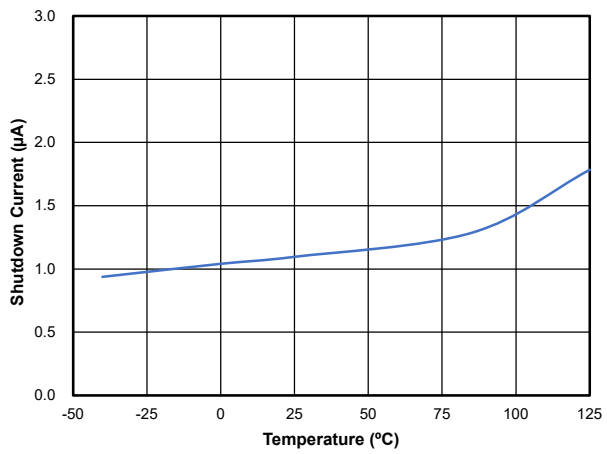
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply						
V_{IN_MIN}	Minimum Input Voltage	T_A = 25 °C			3	V
V_{IN_UV}	Under Voltage Lockout Thresholds	Rising Threshold		2.85	3.2	V
		Hysteresis		200		mV
I_{SD}	Shutdown Supply Current	V_{EN} = 0 V, T_A = 25 °C		0.9	3	μA
I_Q	Non-Switching Quiescent Current	V_{FB} = 1.2 V		3	15	μA
Enable						
V_{EN_H}	Enable High Threshold	Rising Threshold	1.18	1.23	1.31	V
V_{EN_HYS}	Enable Hysteresis Threshold	Hysteresis		200		mV
V_{EN_LKG}	Enable Pin Leakage Current	V_{EN} = 3.3 V		0.2		nA
Soft Start						
T_{ss}	Internal Soft-Start Time			4		ms
Voltage Reference						
V_{FB}	Feedback Voltage		0.99	1	1.01	V
MOSFETs						
R_{DSON_H}	High Side on Resistance			90		mΩ
R_{DSON_L}	Low Side on Resistance			60		mΩ
Current Limits						
I_{LIMIT_H}	High Side Current Limit (1)	Duty Cycle approaches 0 %	4.3	5.5	6.7	A
I_{LIMIT_L}	Low Side Current Limit			3.5		A
I_{PK_MIN}	Minimum Peak Inductor Current			0.9		A
I_{ZC}	Zero Current Detector Threshold			0.1		A
Power Good						
V_{PG_HR}	Power Good High Threshold	Rising Threshold, % of V_{FB}	104	107	111	%
V_{PG_HF}	Power Good High Threshold	Falling Threshold, % of V_{FB}	103	105	109	%
V_{PG_LR}	Power Good Low Threshold	Rising Threshold, % of V_{FB}	92	94	98	%
V_{PG_LF}	Power Good Low Threshold	Falling Threshold, % of V_{FB}	90	92	96	%
R_{PG}	PG Pull-down Resistance	V_{IN} = 12 V, V_{EN} = 4 V		90	250	Ω
		V_{EN} = 0 V		80	200	
t_{PG}	PG Glitch Filter Delay				170	μs
$V_{MIN\text{-}PG}$	Minimum Input Voltage for PG Function	V_{EN} = 0 V, 50 μA			2	V
V_{PG}	PG Logic Low Output	V_{IN} = 1.4 V, V_{EN} = 0 V, 50 μA			0.2	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BOOT Supply						
VCC	Internal LDO Output Voltage			3.5		V
V_{BOOT_UV}	Bootstrap Voltage Undervoltage Threshold			2.2		V
Hiccup Mode						
V_{HC}	FB Voltage to Trip Hiccup Mode			0.5		V
t_{HC}	Interval Time between Hiccup Burst			35		ms
Switching Frequency Timing						
f_{SW}	Switching Frequency	400 kHz Version	365	400	465	kHz
f_{SW}	Switching Frequency	1.4 MHz Version	1.2	1.4	1.6	MHz
f_{SW}	Switching Frequency	2.1 MHz Version	1.8	2.1	2.4	MHz
f_{SS}	Spread Spectrum Span			8		%
T_{ON_MAX}	Maximum On Time			8		μs
T_{ON_MIN}	Minimum On Time			35		ns
T_{OFF_MIN}	Minimum Off Time			100		ns
Thermal						
T_{SD}	Thermal Shutdown			165		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			15		°C

(1) High-side MOSFET current limit is affected by the duty cycle. The high side current limit is higher at a small duty cycle.

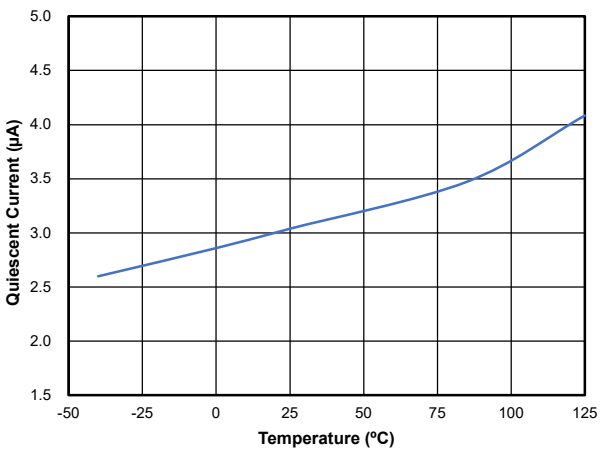
Typical Performance Characteristics

All test conditions: V_{IN} = 12 V, F_{SW} = 2.1 MHz, V_{OUT} = 5 V, T_A = 25 °C, unless otherwise noted.



V_{EN} = 0 V

Figure 1. Shutdown Supply Current



V_{FB} = 1.2 V

Figure 2. Non-Switching Quiescent Current

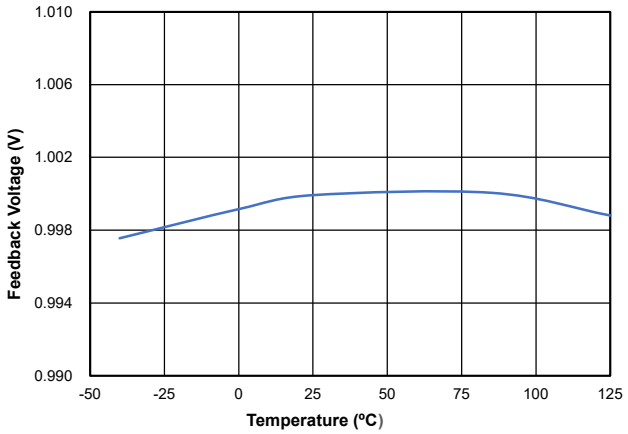


Figure 3. Feedback Voltage

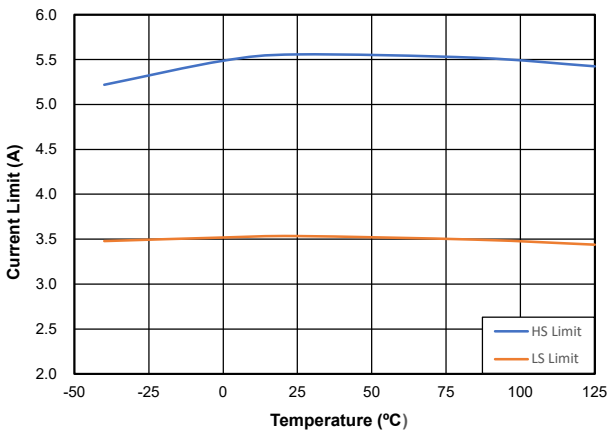


Figure 4. High-Side and Low-Side Current Limits

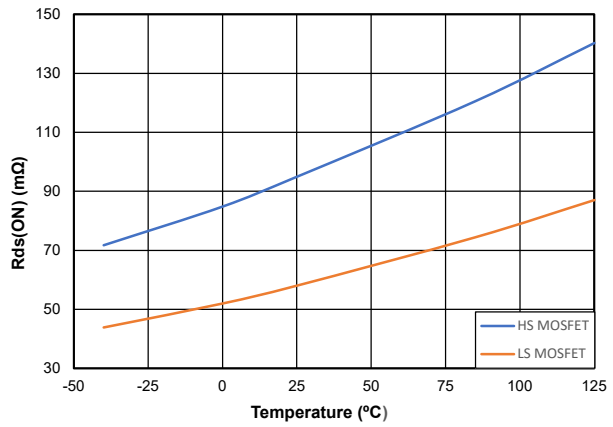


Figure 5. High-Side and Low-Side MOSFET

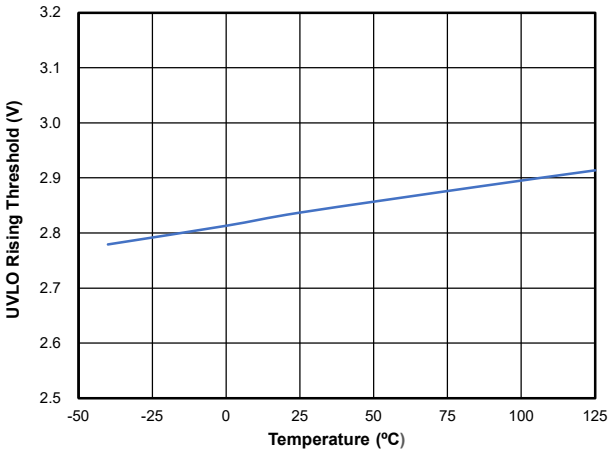


Figure 6. Input UVLO Threshold

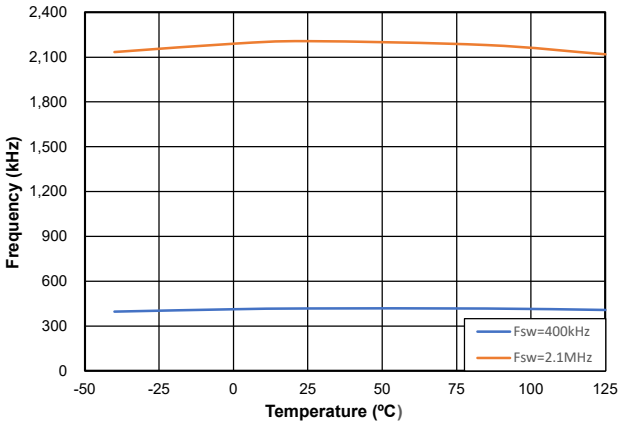
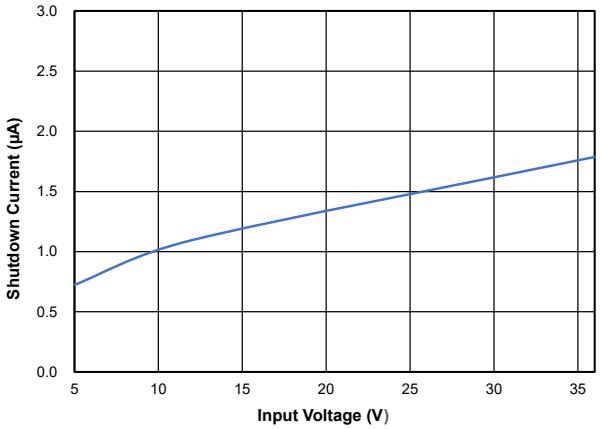
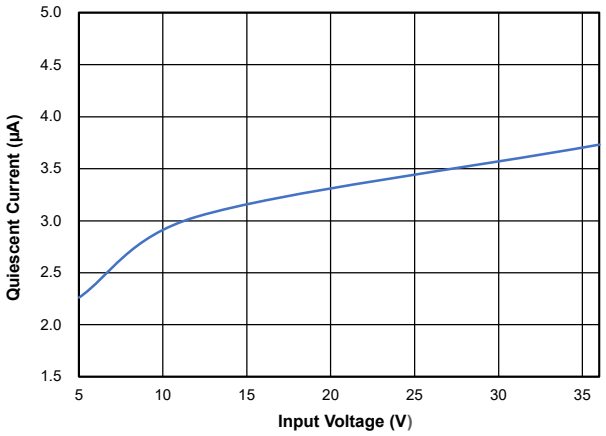


Figure 7. Switching Frequency



V_{EN} = 0 V

Figure 8. Shutdown Supply Current vs. Input



V_{FB} = 1.2 V

Figure 9. Non-Switching Quiescent Current vs. Input

Detailed Description

Overview

The TPP36307Q is a high-efficiency synchronous step-down regulator with integrated high-side and low-side MOSFETs. The TPP36307Q can provide up to 3-A output current with high efficiency from light load to full load operating range. The TPP36307Q features a wide input voltage from 3 V to 36 V, selective switching frequencies 400 kHz, 1.4 MHz, and 2.1 MHz for different version parts.

The internal soft-start limits inrush current during power-on. The TPP36307Q also integrates a compensation circuit inside the chip to simplify the loop design. The TPP36307Q features ultra-low operating quiescent current, which makes it suitable for battery-powered applications.

The TPP36307Q is specially optimized to reduce EMI emissions. The device features a frequency spread spectrum method, optimized symmetrical pinout, and EMI friendly package to optimize the EMI performance. The TPP36307Q integrates full protections such as thermal shutdown, UVLO, enable (EN) control, and power good (PG) indicator. Additionally, during the overload or short circuit condition, the cycle-by-cycle peak and valley current limit and hiccup protections are provided.

Functional Block Diagram

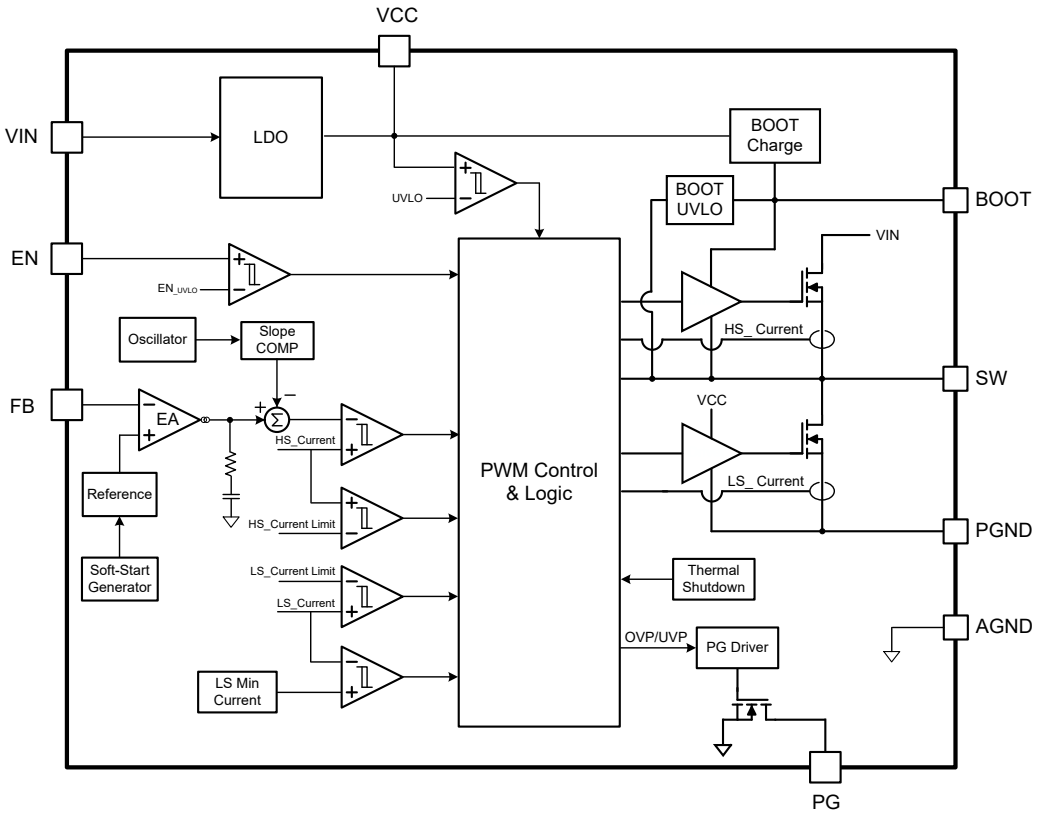


Figure 10. Functional Block Diagram

Feature Description

Fixed Frequency Peak Current Mode Control

The TPP36307Q adopts fixed frequency peak current mode control. The feedback voltage is sensed from the resistor divider through the FB pin to compare with the internal voltage reference by an error amplifier. By adjusting the value of the peak current with different output voltage deviations, this voltage control loop is designed to obtain accurate DC voltage regulation. The output of the error amplifier is compared with the sensed peak current by the PWM comparator and controls the on time of the high-side MOSFET. The device also integrates the compensation of the voltage feedback loop to save external components and ensure the stability of the control loop in various working conditions.

An internal oscillator controls the switching frequency and initiates the turn-on of the integrated the high-side MOSFET in each duty cycle. During this high-side on period, the SW voltage rises to approximately the input voltage, and the inductor current increases linearly. Once the sensed current through the high-side MOSFET reaches the threshold level set by the COMP voltage of the error amplifier, the PWM comparator turns off the high-side MOSFET. The low-side MOSFET is turned on after a short dead time, and the inductor current is discharged linearly by the low-side MOSFET. The device also utilizes an internal ramp compensation control to avoid sub-harmonic oscillations when the duty cycle is larger than 50%. The COMP voltage is also clamped for current limit conditions and light load operation.

Light Load Operation

The TPP36307Q utilizes advanced Pulse Frequency Modulation (PFM) control to improve efficiency in light load working conditions. When the load current decreases, the device approaches discontinuous conduction mode first, and the COMP voltage decreases accordingly. The low-side MOSFET is turned off when the zero current detection is triggered to improve system efficiency. When the COMP voltage drops to the low clamped threshold voltage, the device skips a pulse and decreases the switching frequency by extending the non-switching period. During this period, the output voltage decreases due to the load current and capacitor discharge. The high-side MOSFET resumes to turn on once the COMP voltage is higher than the threshold. The device tries to obtain switching pulses with a minimum peak inductor current to reduce the output ripple and the COMP voltage drops to the clamped value again and triggers another non-switching period.

During the non-switching period, most internal circuits shut down, except for some protection blocks, to reduce power consumption. The TPP36307Q features a typical 6-μA ultra-low quiescent current and can also ensure relatively high efficiency in ultra-low light load conditions and release smooth transitions between CCM, DCM, and PSM modes.

Soft Start with Pre-Biased Capability

The TPP36307Q implements a soft start circuit to prevent the inrush current during start-up. The soft start time is fixed internally. When the start-up period begins, the internal reference voltage slowly ramps up.

The TPP36307Q also supports a monotonic start-up with pre-biased loads. If the output voltage is pre-biased to a certain value during start-up, the device disables switching for both high-side and low-side MOSFETs until the soft start reference voltage exceeds the feedback voltage.

Frequency Spread Spectrum

The TPP36307Q provides a spread spectrum method which reduces the EMI of the power supply over a wide frequency range. The spread spectrum modulates the switching frequency of the regulator periodically with a relatively low-frequency range to spread the EMI emissions across a wider range. In order to minimize output voltage ripple caused by the spread spectrum, the duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled. The spread spectrum function is disabled when the device is in light load, drops out, and triggers minimum on-time conditions.

Low Drop-out Mode

As the duty cycle increases, where the input voltage approaches the output voltage level, the required off time of the high-side MOSFET approaches its minimum off time. When the minimum off time is reached, the TPP36307Q automatically extends the high side on time and reduces the switching frequency. The device can realize 98% max duty cycle in drop-out condition. In this condition, the dropout voltage difference between input and output is influenced by the on-resistance of the high-side MOSFET, the DCR of the power inductor, and the maximum duty cycle achieved. For different load currents, the 5-V output drop-out voltage is shown below.

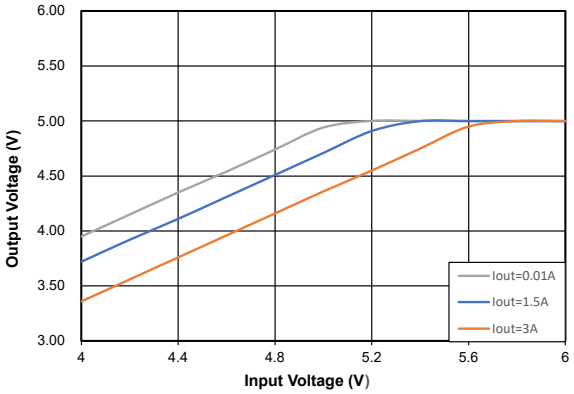


Figure 11. Low Drop-out Voltage

Minimum on Time

As the duty cycle is decreasing, where the conversion ratio is very low, the required on time of the high-side MOSFET approaches its minimum on time. The TPP36307Q features a typical 35-ns ultra-low minimum on time and can support smaller duty cycles for high-frequency power systems. Also, the device can automatically reduce the switching frequency when the minimum on time is reached.

Power Good

The device employs an open-drain output PG signal to check whether the output voltage is operating within the normal range. The external pull-up voltage resource is recommended to be less than 5.5 V (such as VCC) with a 1-kΩ resistor. Once the feedback voltage is within 94% and 107% of the internal reference voltage, the PG is pulled up by the external resistor. Once the feedback voltage is lower than 92% or higher than 105% of the internal reference voltage, the PG is pulled low.

Protection

Undervoltage Lockout (UVLO)

Typically, the device features 2.85-V input undervoltage lockout rising threshold. The UVLO threshold integrates a 200-mV hysteresis to make a desired hysteresis for input voltage. It can be adjusted by using an EN pin with an external resistor divider.

V_{UVLO_R} is the desired system-level undervoltage protection rising threshold voltage, and V_{UVLO_F} is the desired system-level undervoltage protection falling threshold voltage. V_{EN_R} and V_{EN_F} are the rising and falling enable thresholds. R_{UVLO_H} and R_{UVLO_L} can be calculated below.

$$V_{UVLO\_R} = \left(1 + \frac{R_{UVLO\_H}}{R_{UVLO\_L}}\right) * V_{EN\_R} \quad (1)$$

$$V_{UVLO\_F} = \left(1 + \frac{R_{UVLO\_H}}{R_{UVLO\_L}}\right) * V_{EN\_F} \quad (2)$$

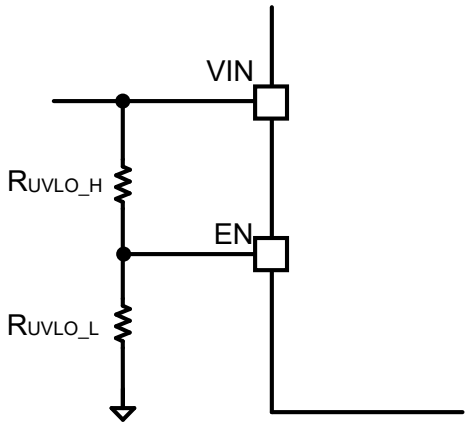


Figure 12. UVLO Adjustment

Current Limits

The TPP36307Q employs both cycle-by-cycle peak and valley current limits to protect the high-side and low-side power switch overloaded. Once the inductor current reaches the high-side peak current limit, the high-side MOSFET is turned off immediately to avoid the inductor current from further increasing. When the low-side valley current limit is triggered, the next duty cycle is held until the inductor current recovers within the valley current limit. Both peak and valley current limits determine the maximum output current of the device, and the valley current limit can prevent inductor current from running away during unexpected overload or short circuit conditions. Also, the device integrates a zero-current detector to turn off the low-side MOSFET at light loads. Delay needs to be taken into account, which may cause the sensed current to be slightly different from open-loop current limits.

Short Circuit Protection

To further ensure the converter's protection during prolonged overload or short circuits, the device features hiccup overload protection. When the inductor peak current is clamped at the peak current limit, the output voltage falls out of normal regulation. Furthermore, if the feedback-sensed voltage drops below one threshold, the device enters the hiccup mode. Entering this mode, the device stops switching and restarts a normal soft-start operation after the recovery time. If the overload condition still exists, the device keeps switching with the peak current limit and turns off the switches again. The device can automatically recover to normal operation when the overload condition is removed. The hiccup function is disabled at the normal soft start period to avoid being mistakenly triggered.

Thermal Shutdown

Once the junction temperature rises above the internal over-temperature shutdown threshold, the internal temperature sensor shuts down the device. The device recovers operating when the junction temperature falls below the threshold with hysteresis.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP36307Q is typically used to convert a wide range of input voltage to the desired output voltage, which can be set by the feedback resistor divider. Because of the ultra-low minimum on time and high efficiency, the TPP36307Q is very suitable for 2.1-MHz high-frequency applications to increase system power density. The device is integrated with the internal compensation and can operate over a wide range of external components and working conditions. However, some typical parameters and external component values are recommended to help speed up the developing process. In most power systems, lower voltage rail such as 5 V/3.3 V is typically used for microcontrollers, I/Os, and other low-voltage components. The following application lists the typical schematic and application information for a 5-V output buck regulator system.

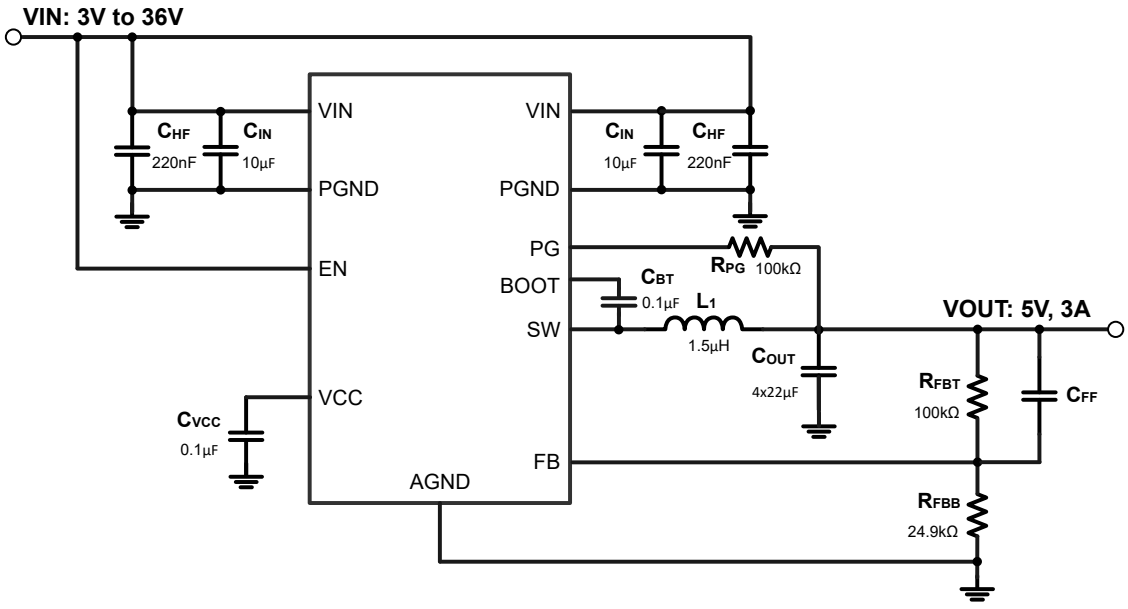


Figure 13. Typical Application Circuit

Choosing Switching Frequency

Switching frequency of the DCDC regulator is a compromise between system efficiency and total solution size. The lower switching frequency can help reduce power losses and usually results in higher system efficiency, while the higher switching frequency allows the selection of smaller external components, such as inductors and output capacitors, and increases the system power density. The TPP36307Q is suitable for high-frequency applications because it is designed with high efficiency and a small minimum on time.

Setting Output Voltage

The external resistor divider network connected to the FB pin sets the output voltage. The resistance of the divider is a compromise between noise suppression and output current consumption. The smaller value resistor reduces noise sensitivity but also increases the quiescent current of the system and reduces light load efficiency. It is typically recommended to select

100 kΩ resistor for the top feedback resistor. If low quiescent current and high light load efficiency are required, a 1-MΩ top feedback resistor can be selected and one feedback capacitor can be used to improve the phase margin. Once the top feedback resistor is selected, the value of the bottom feedback resistor can be calculated with the equation below.

$$R_{FBB} = \frac{V_{FB} * R_{FBT}}{V_{OUT} - V_{FB}} \quad (3)$$

where V_{FB} is the internal reference voltage, which is typically 1 V for TPP36307Q. For a 5 V output, if R_{FBT} = 100 kΩ, R_{FBB} = 24.9 kΩ is chosen. If R_{FBT} = 1 MΩ, R_{FBB} = 249 kΩ is chosen.

Inductor Selection

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance, and saturation current. The inductor value is designed based on the desired peak-to-peak ripple current and is typically chosen to be in the range of 20% to 40% of the maximum output current. Once the desired inductor ripple current is selected, the inductor value can be calculated with the equation below.

$$L = \frac{V_{OUT}}{f_{SW} * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

where f_{SW} is the switching frequency and ΔI_L is the inductor ripple current.

When the inductor current approaches its saturation level, the effective inductance can fall to a fraction of the zero current value. Although one high-side valley current limit is integrated to avoid the current runaway, the inductor current can rise to a high value very rapidly if the inductor is saturated. The inductor saturation current must leave a safe margin from the high-side peak current limit in the worst-case conditions. The inductor's RMS current and peak current can be calculated with the equation below.

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L}{12}} \quad (6)$$

Input Capacitor Selection

The input capacitor of the step-down regulator is used to supply the AC input current and maintain a stable DC input voltage. At least a 10-μF capacitance of ceramic input capacitor is recommended. Additional input capacitance may be required to meet ripple and transient requirements. High-quality ceramic capacitor, X5R or X7R, is recommended because of low equivalent series resistance (ESR) characteristics and small capacitance variations over a temperature range. In addition, one small value and small case size, ceramic capacitor (such as 100 nF, 0603 package) is recommended to be used at the input and be placed as close as possible to the VIN and GND pins. This can provide a high-frequency bypass for the internal control circuits. The input capacitor can be calculated with the equation below when the input voltage ripple is determined.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

where C_{IN} is the input capacitance value.

The input capacitor ripple current rating should be greater than the maximum input current ripple. The RMS current of the input capacitor can be calculated with the equation below.

$$I_{CIN\_RMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (8)$$

The worst case for the input voltage ripple and RMS current occurs when the duty cycle is 50%.

Output Capacitor Selection

The output capacitance is mainly selected to meet the requirement of the output ripple and voltage change during a load transient. Then the control loop is compensated for the output capacitor selected. The output voltage ripple is related to the capacitance and ESR of the output capacitor. Assuming the capacitor with small ESR, the minimum output capacitance needed for a given output ripple voltage can be calculated with the equation below.

$$C_{OUT} > \frac{\Delta I_L}{8 * f_{SW} * \Delta V_{OUT}} \quad (9)$$

where ΔI_L is the inductor ripple current and ΔV_{OUT} is the output voltage ripple.

If a large ESR capacitor is used, it contributes additional output ripple. ESR ripples can be neglected for ceramic capacitors, but must be considered if electrolytic capacitors are used. The maximum ESR for a given ripple can be calculated with the equation below.

$$R_{ESR} < \frac{\Delta V_{OUT}}{\Delta I_L} - \frac{1}{8 * f_{SW} * C_{OUT}} \quad (10)$$

The effective value of the ceramic capacitor decrease should be considered when the output DC bias voltage is added across the capacitors. The RMS current of the output capacitor can be calculated with the equation below.

$$I_{COUT\_RMS} = \frac{V_{OUT} * (V_{IN\_MAX} - V_{OUT})}{\sqrt{12} * V_{IN\_MAX} * L * f_{SW}} \quad (11)$$

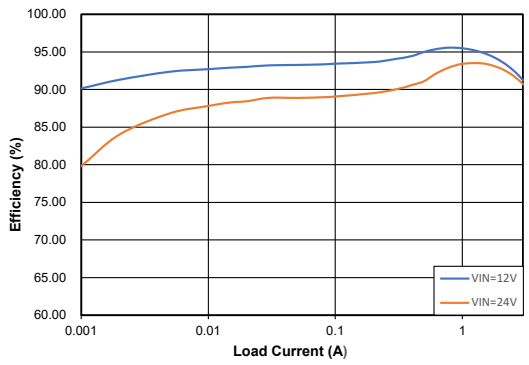
where V_{IN_MAX} is the maximum input voltage, and L is the selected inductor value.

Bootstrap Capacitor Selection

A typical 0.1-μF bootstrap capacitor is connected between the BOOT pin and the SW pin. It is recommended to use a ceramic capacitor with X5R or superior grade dielectric and a voltage rating of 10 V or higher.

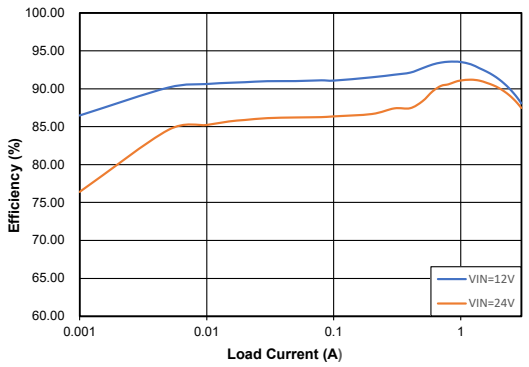
Application Waveforms

All test conditions: V_{IN} = 12 V, F_{SW} = 2.1 MHz, V_{OUT} = 5 V, T_A = 25 °C, unless otherwise noted.



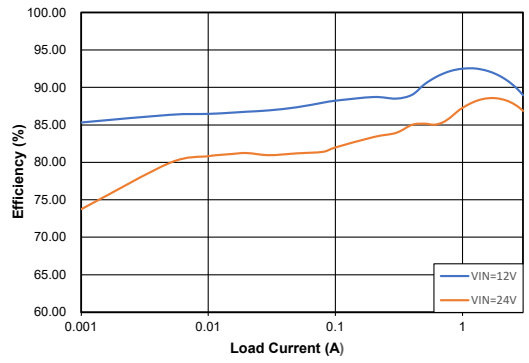
V_{OUT} = 5 V, F_{SW} = 400 kHz

Figure 14. Efficiency



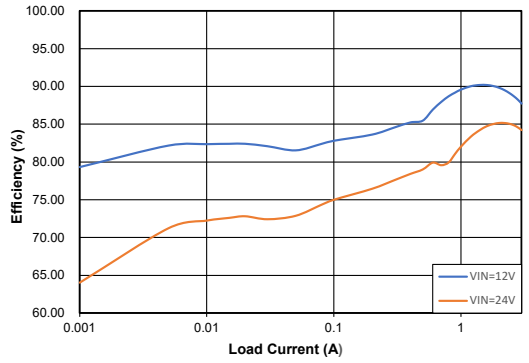
V_{OUT} = 3.3 V, F_{SW} = 400 kHz

Figure 15. Efficiency



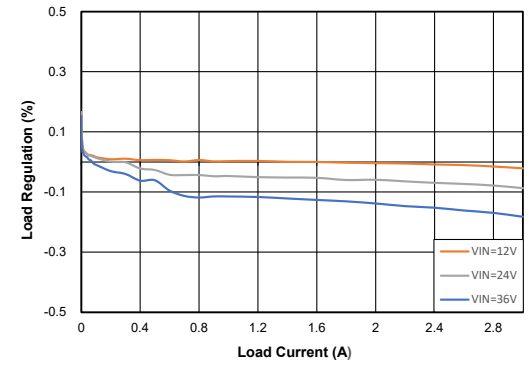
V_{OUT} = 5 V, F_{SW} = 2.1 MHz

Figure 16. Efficiency



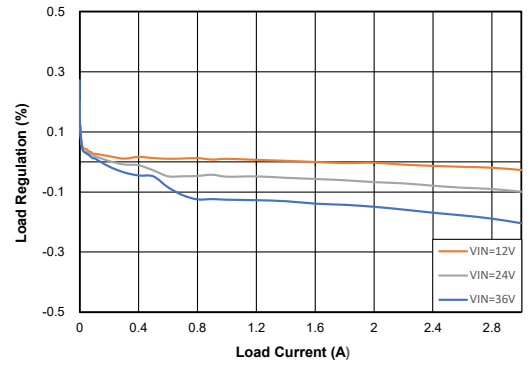
V_{OUT} = 3.3 V, F_{SW} = 2.1 MHz

Figure 17. Efficiency



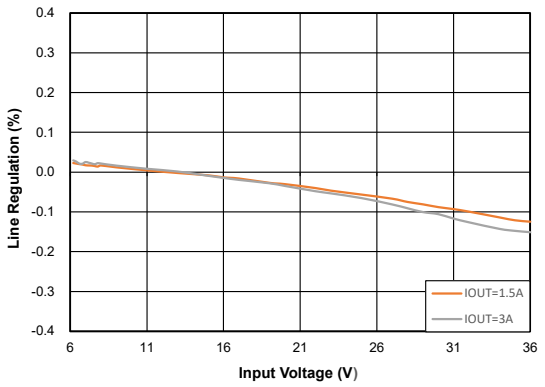
V_{OUT} = 5 V

Figure 18. Load Regulation



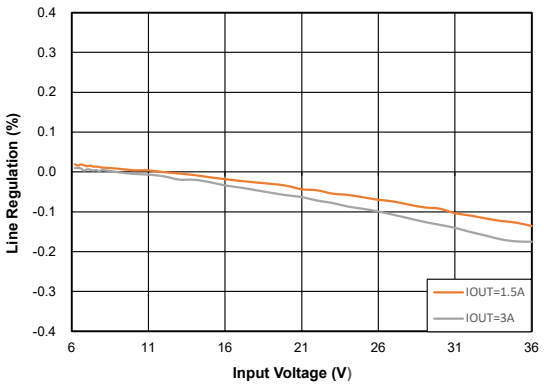
V_{OUT} = 3.3 V

Figure 19. Load Regulation



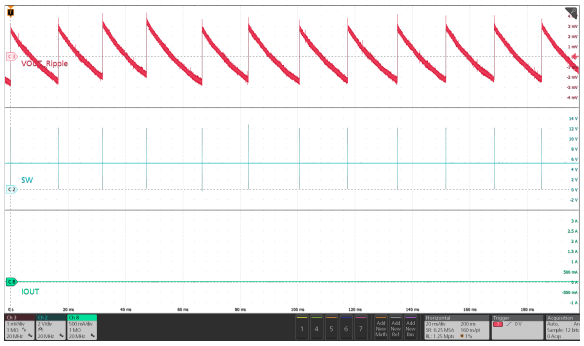
V_{OUT} = 5 V

Figure 20. Line Regulation



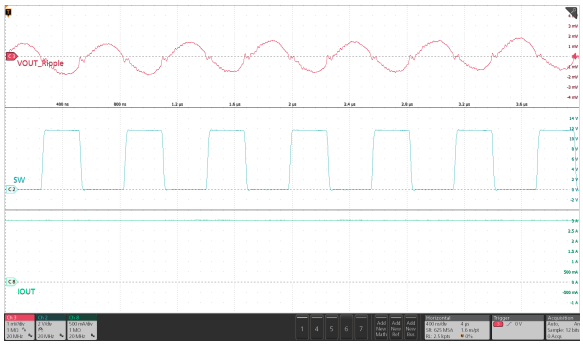
V_{OUT} = 3.3 V

Figure 21. Line Regulation



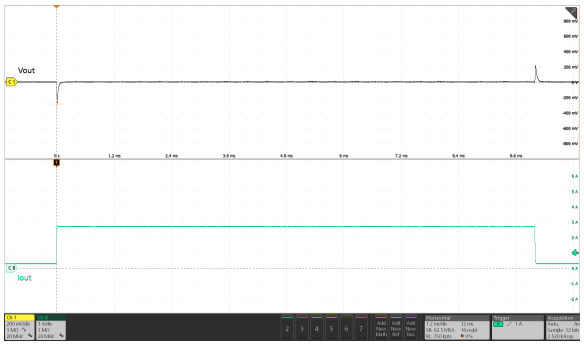
I_{OUT} = 0 A

Figure 22. Switching Waveform and Output Ripple



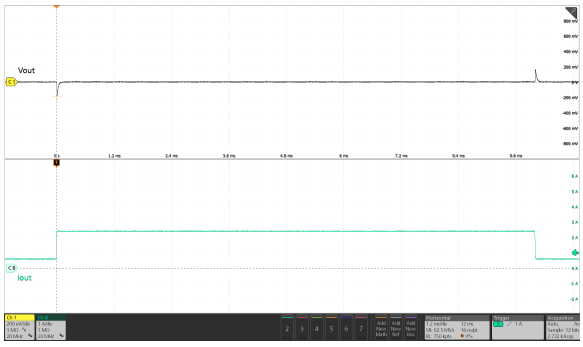
I_{OUT} = 3 A

Figure 23. Switching Waveform and Output Ripple



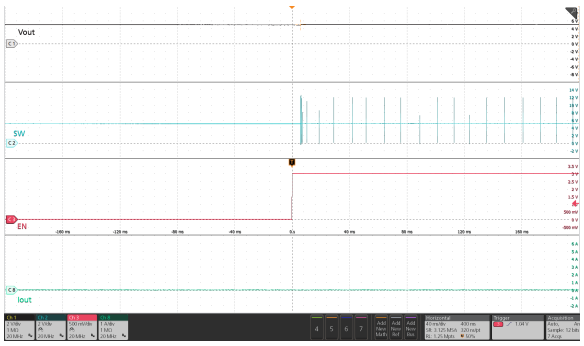
I_{OUT} = 0 A to 3 A to 0 A

Figure 24. Load Transient



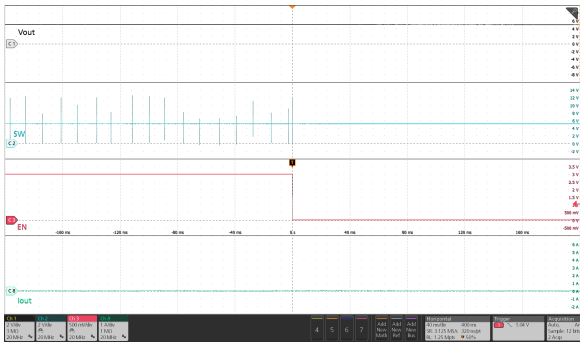
I_{OUT} = 0.6 A to 2.4 A to 0.6 A

Figure 25. Load Transient



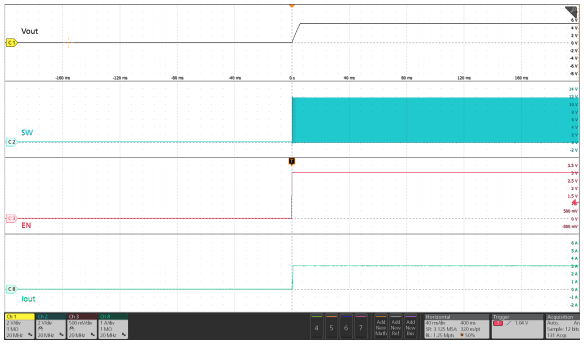
I_{OUT} = 0 A

Figure 26. Power up by Enable



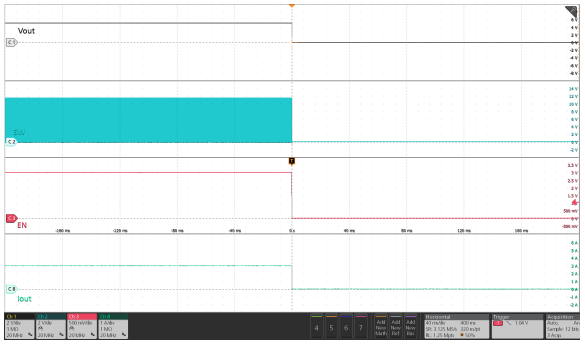
I_{OUT} = 0 A

Figure 27. Power down by Enable



I_{OUT} = 3 A

Figure 28. Power up by Enable

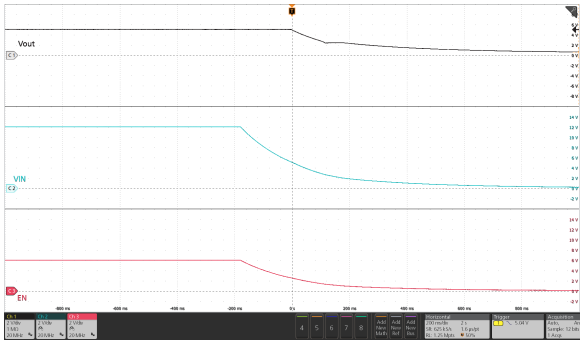


I_{OUT} = 3 A

Figure 29. Power down by Enable

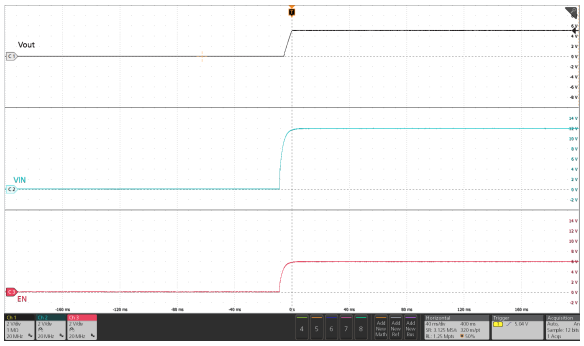
I_{OUT} = 0 A

Figure 30. Power up by Input



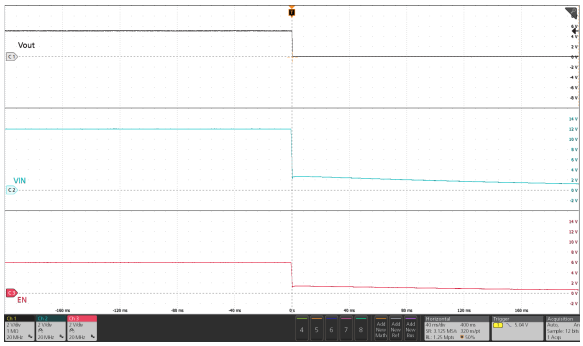
I_{OUT} = 0 A

Figure 31. Power down by Input



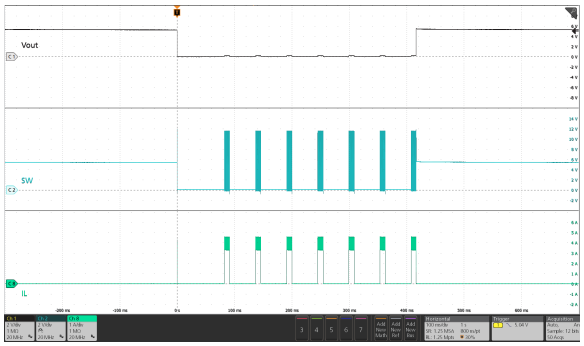
I_{OUT} = 3 A

Figure 32. Power up by Input



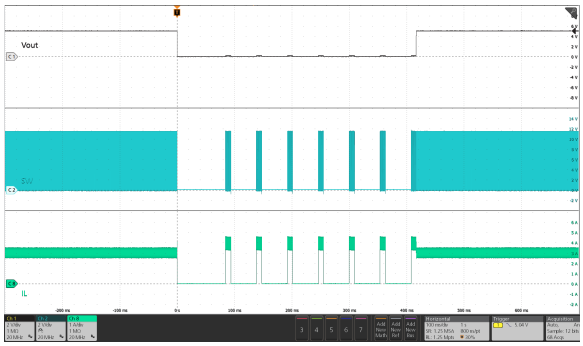
I_{OUT} = 3 A

Figure 33. Power down by Input



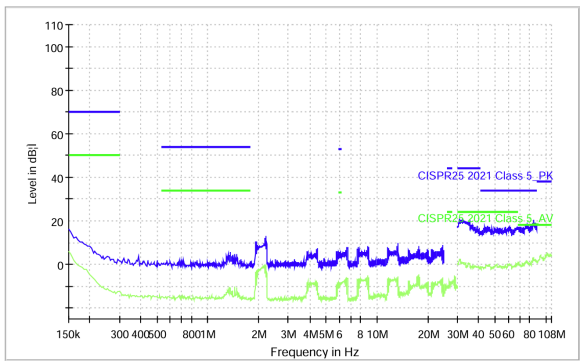
I_{OUT} = 0 A

Figure 34. Hiccup Protection



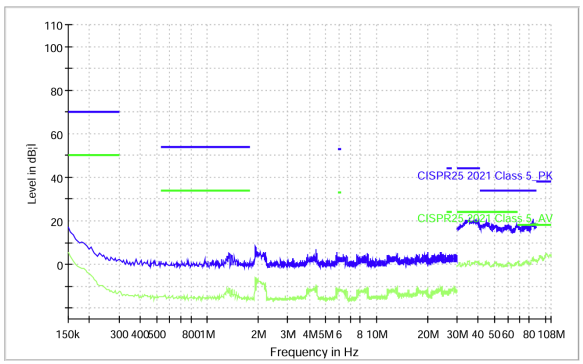
I_{OUT} = 3 A

Figure 35. Hiccup Protection



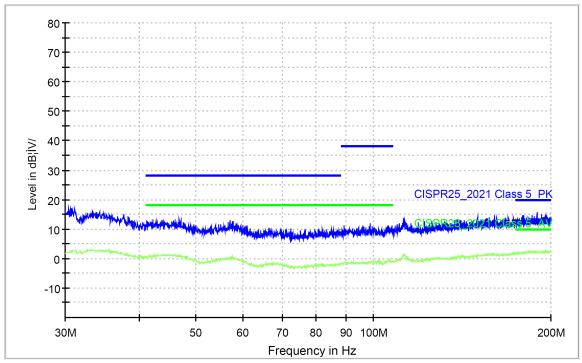
Frequency Tested: 150 kHz to 108 MHz, Positive

Figure 36. Conducted EMI versus CISPR25 Limits



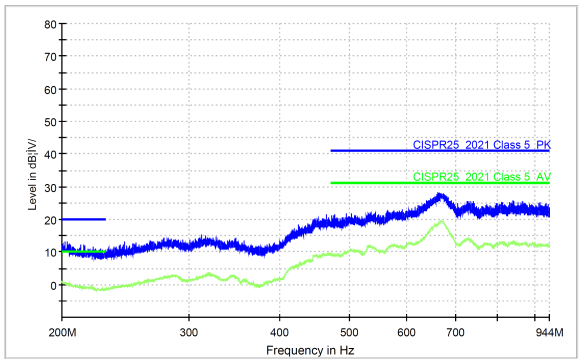
Frequency Tested: 150 kHz to 108 MHz, Negative

Figure 37. Conducted EMI versus CISPR25 Limits



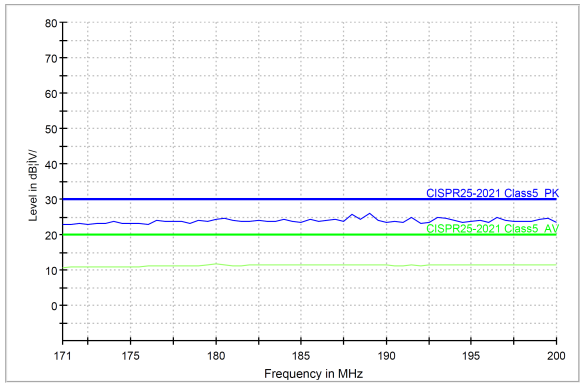
Analog, Frequency Tested: 30 MHz to 200 MHz, Vertical

Figure 38. Radiated EMI versus CISPR25 Limits



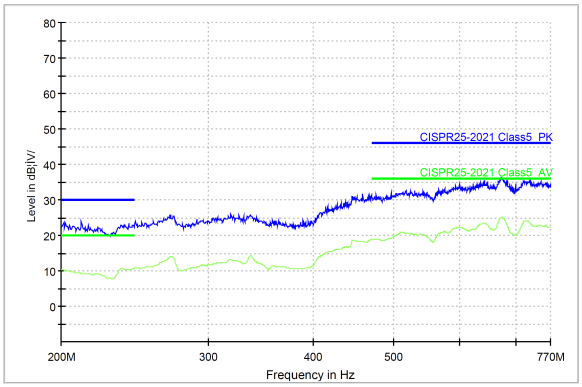
Analog, Frequency Tested: 200 MHz to 944 MHz, Vertical

Figure 39. Radiated EMI versus CISPR25 Limits



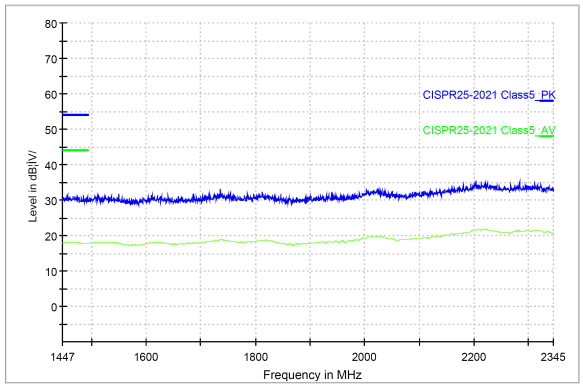
Digital Broadcast, Frequency Tested: 171 MHz to 200 MHz, Vertical

Figure 40. Radiated EMI versus CISPR25 Limits



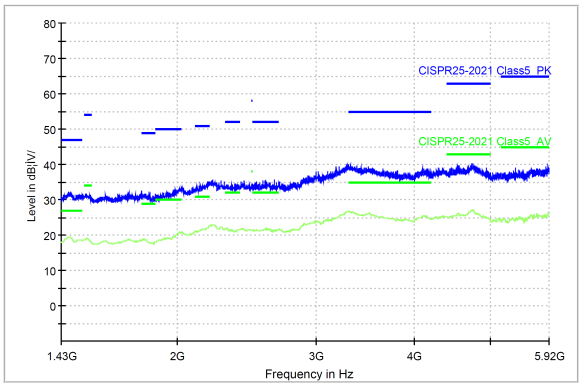
Digital Broadcast, Frequency Tested: 200 MHz to 770 MHz, Vertical

Figure 41. Radiated EMI versus CISPR25 Limits



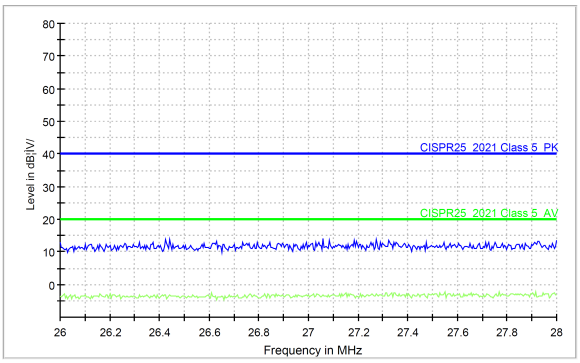
Digital Broadcast, Frequency Tested: 1447 MHz to 2345 MHz, Vertical

Figure 42. Radiated EMI versus CISPR25 Limits



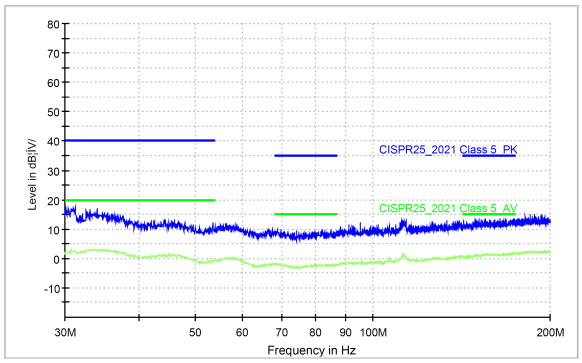
Digital Mobile Phone, Frequency Tested: 1427 MHz to 5925 MHz, Vertical

Figure 43. Radiated EMI versus CISPR25 Limits



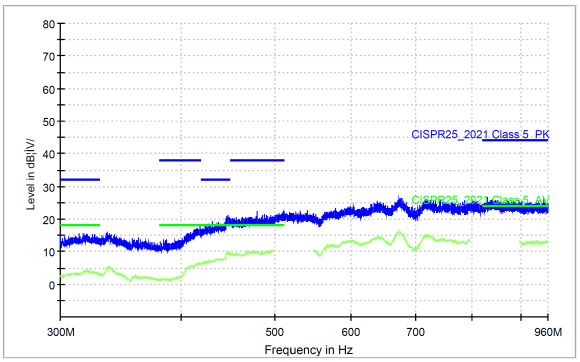
Mobile, Frequency Tested: 26 MHz to 28 MHz, Vertical

Figure 44. Radiated EMI versus CISPR25 Limits



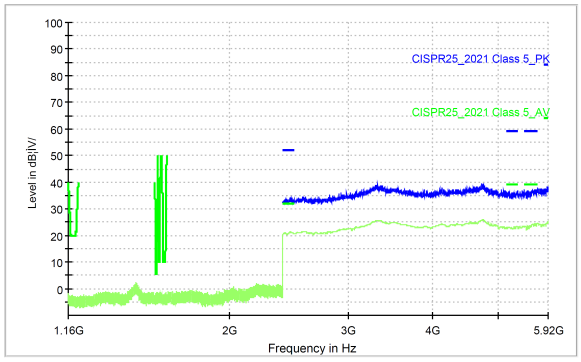
Mobile, Frequency Tested:30 MHz to 200 MHz, Vertical

Figure 45. Radiated EMI versus CISPR25 Limits



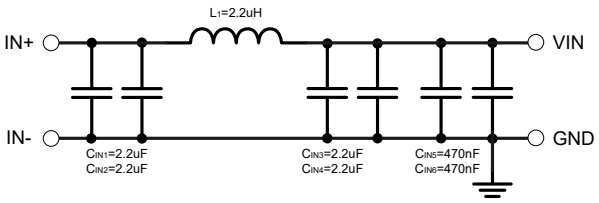
Mobile, Frequency Tested: 300 MHz to 960 MHz, Vertical

Figure 46. Radiated EMI versus CISPR25 Limits



Mobile, Frequency Tested: 1156 MHz to 5925 MHz, Vertical

Figure 47. Radiated EMI versus CISPR25 Limits



F_{SW} = 2.1 MHz

Figure 48. Recommended Input EMI Filter

Layout

Layout Guideline

The performance of switching regulators heavily depends on the quality of the PCB layout, especially for thermal design and EMI design. Even if the schematic design is good, a bad PCB layout can disrupt the operation of the regulator.

1. Place a low ESR ceramic capacitor as close to the VIN pin and the ground as possible.
2. Make sure the top switching loop with power has the lowest impendence of grounding.
3. Use a large ground plane to connect to PGND directly. And add vias near PGND.
4. The inductor should be placed close to the SW pin to minimize the SW area.
5. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the chip.
6. Keep the connection of the input capacitor and the VIN pin as short and wide as possible.

Layout Recommendations

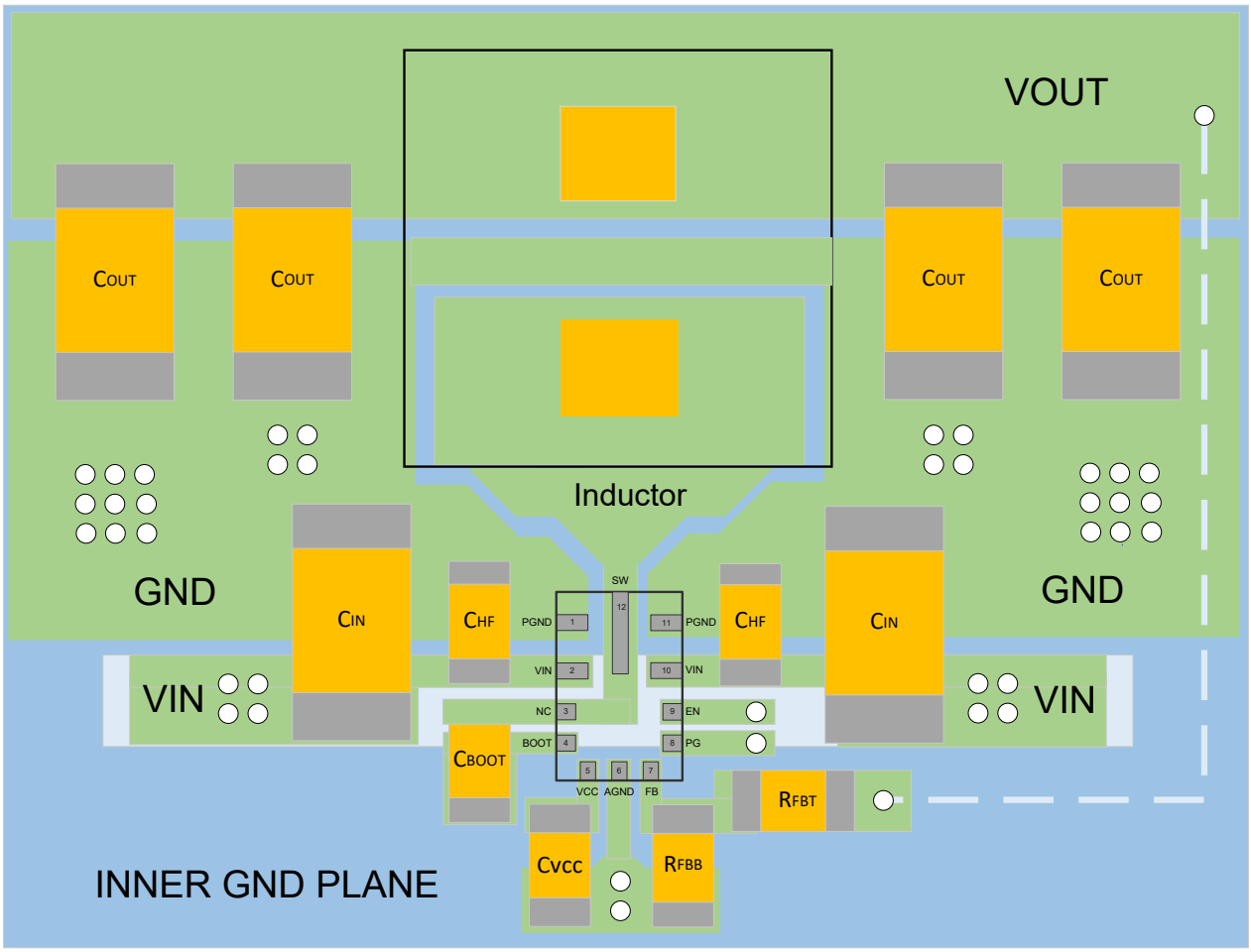
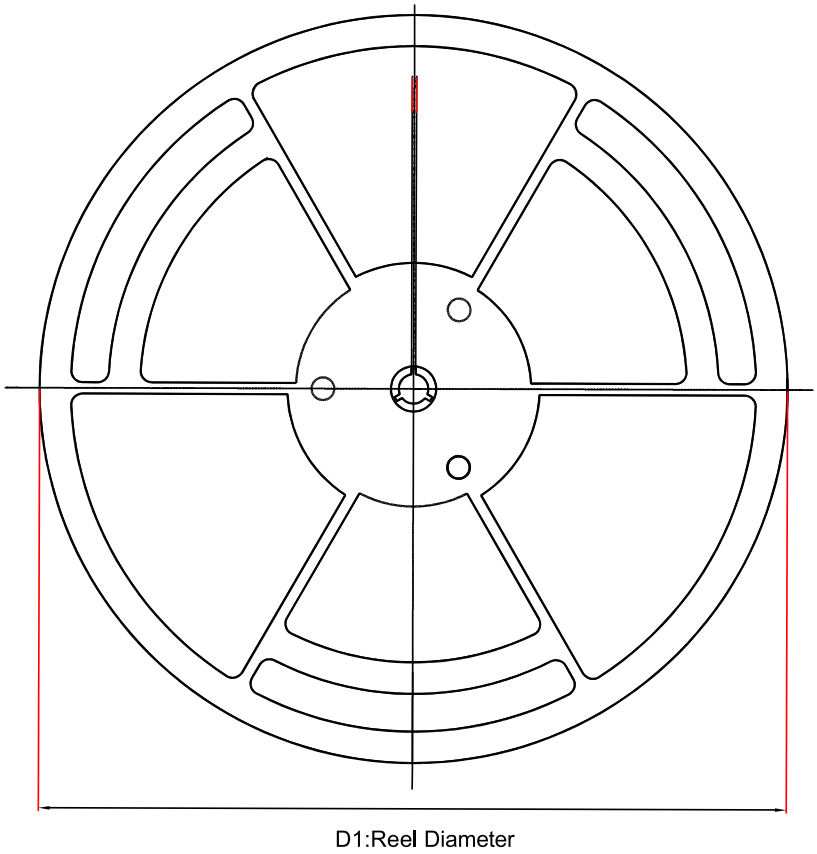
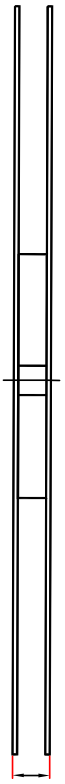
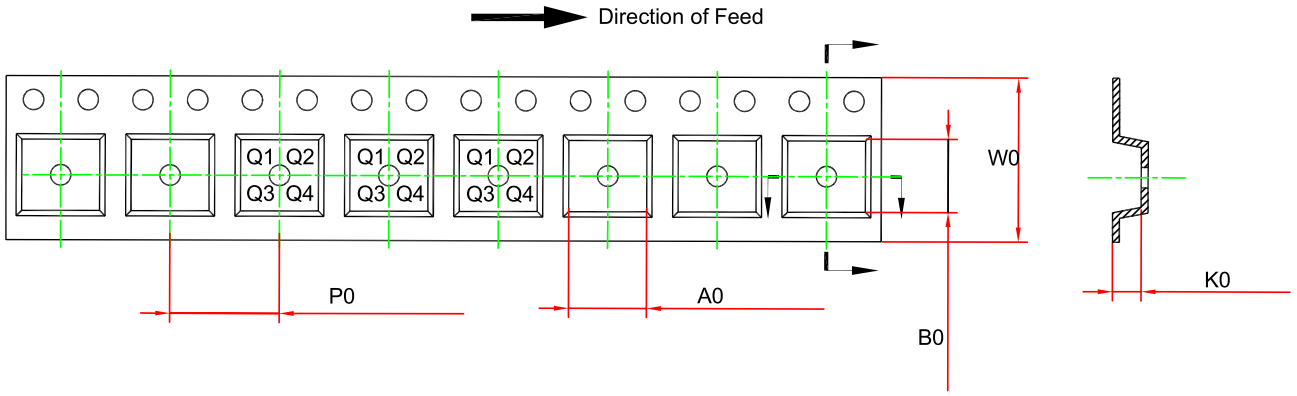


Figure 49. Layout Example

Tape and Reel Information





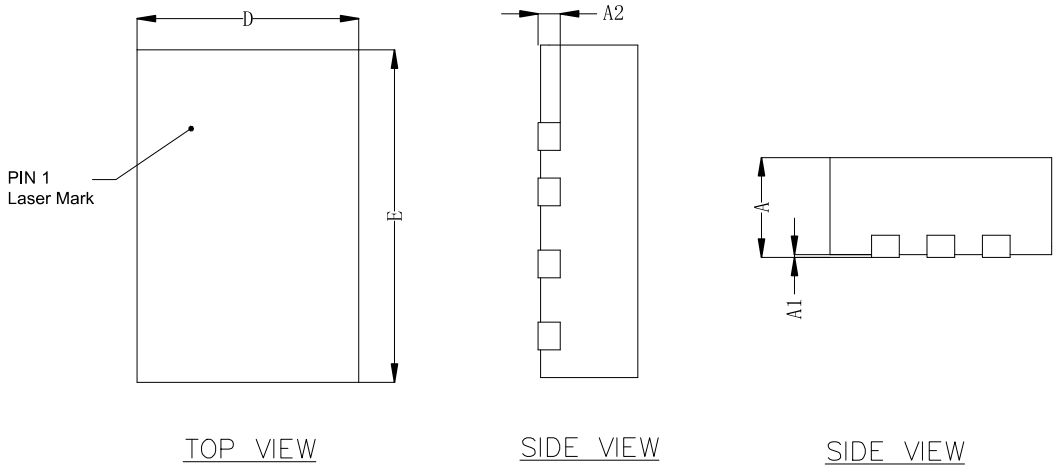


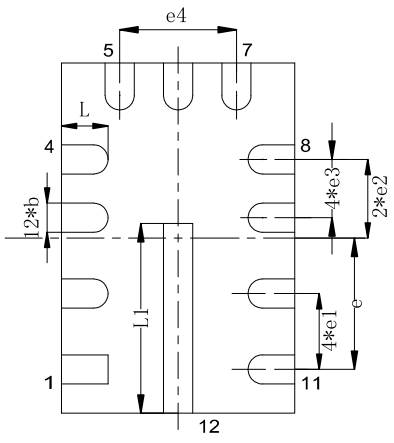
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP363070Q-FC6R-S	QFN2X3-12	178	11.4	2.3	3.2	1.0	4.0	8.0	Q1
TPP363071Q-FC6R-S	QFN2X3-12	178	11.4	2.3	3.2	1.0	4.0	8.0	Q1
TPP363072Q-FC6R-S	QFN2X3-12	178	11.4	2.3	3.2	1.0	4.0	8.0	Q1

Package Outline Dimensions

QFN2X3-12

Package Outline Dimensions FC6(QFN2X3-12-B)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
E	2.900	3.100	0.114	0.122
e	1.025	1.225	0.040	0.048
e1	0.600	0.700	0.024	0.028
e2	0.625	0.725	0.025	0.029
e3	0.450	0.550	0.018	0.022
e4	0.900	1.100	0.035	0.043
L	0.300	0.500	0.012	0.020
L1	1.525	1.725	0.060	0.068

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP363070Q-FC6R-S	−40 to 125°C	QFN2X3-12	370	MSL2	Tape and Reel, 3000	Green
TPP363071Q-FC6R-S (1)	−40 to 125°C	QFN2X3-12	371	MSL2	Tape and Reel, 3000	Green
TPP363072Q-FC6R-S	−40 to 125°C	QFN2X3-12	372	MSL2	Tape and Reel, 3000	Green

(1) Contact 3PEAK representatives for more information.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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