20A Switching Current, Up to 17V Output, Synchronous Boost Converter with Isolation NMOS Driver

1 Descriptions

The SC8329 is a synchronous boost converter fully integrated with a 6 mΩ low side power switch and a 11 mΩ high side power switch. The SC8329 supports wide input range from 2.7 V to 15 V. It has 20A switch current capability and is capable of providing an output voltage to 17 V.

The SC8329 adopts constant-off-time (COT) control topology, which provides fast transient response. It supports operating modes selection for PWM mode and PFM mode. The switching frequency is adjustable ranging from 200 kHz to 2.2 MHz by an external resistor. The SC8329 implements soft-stat and an adjustable output current limit function.

The SC8329 also supports full protections including input under-voltage lockout (UVLO), output over voltage protection at 17V (OVP), programmable cycle-by-cycle overcurrent protection (OCP) and thermal shut down protection. Furthermore, the SC8329 contains an NMOS driver for short circuit protection.

The SC8329 is available in FCQFN-15 package (4.0mm× 3.0mm).

2 Features

- Wide input operating voltage from 2.7 V to 15 V
- Wide output range, from 4.5 V to 17V
- Up to 20-A programmable switching current limit
- Integrated 6 mΩ and 11 mΩ Power MOSFETs
- PFM and PWM mode selection
- 1.0 μA shutdown current
- Adjustable switching frequency: 200 kHz to 2.2 MHz
- Full protection of UVLO, OVP, OCP, OTP
- Short circuit protection with Isolation NMOS driver
- Available in QFN-15 package (4.0mm×3.0mm)

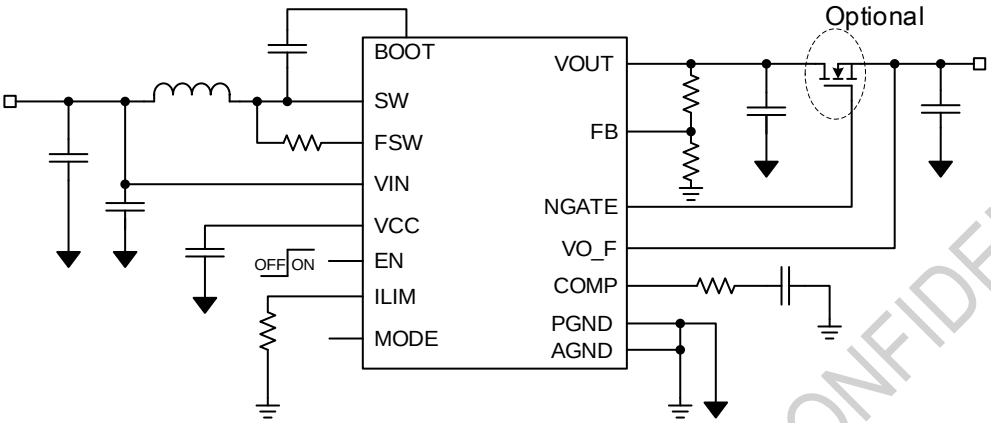
3 Applications

- Portable POS terminals
- Bluetooth Speakers
- E-cigarettes

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8329	15 pin QFN	4mm x 3mm x 0.75mm

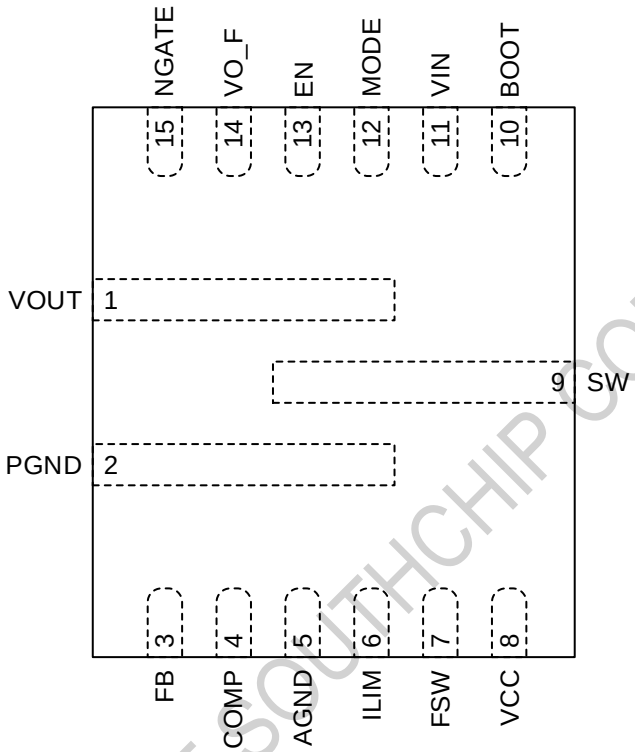
5 Typical Application Circuit



Note: If ISO-FET is not required, left NGATE and VO_F pin floating.

6 Terminal Configuration and Functions

QFN-15 Package
Hotrod
Top view



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VOUT	O	Output node of the boost.
2	PGND	I	Power ground of IC.
3	FB	I	Feedback node for output voltage.
4	COMP	I/O	Connect resistor and capacitor to compensate the control loop.
5	AGND	I/O	Signal ground of IC.
6	ILIM	I	Peak current limit setting pin. Connect a resistor between ILIM and AGND.
7	FSW	I	Switching frequency programming pin. Connect a resistor between FSW pin and SW pin.

8	VCC	O	Output of an internal regulator. Connect a 1μF ceramic capacitor from VCC to AGND pin close to the IC. The regulator provides supply for internal gate driver.
9	SW	I	Switching Node. Connect to inductor.
10	BOOT	O	A 100nF capacitor should be connected between BT and SW to bootstrap a bus voltage for high side MOSFET driver.
11	VIN	I	Power supply to the IC. Place a 1μF capacitor from this pin to PGND as close to the IC as possible.
12	MODE	I	Mode selection pin between PFM Mode and Forced PWM Mode at light load. When this pin is connected to analog ground, the device works in FPWM mode. When this pin is left floating, the device works in PFM mode.
13	EN	I	Enable logic input pin. Logic high level enables the device, nor disables the device. When not in use, connect EN to VIN for automatic start-up.
14	VO_F	I	Connect this pin to the source of NMOS.
15	NGATE	O	NMOS gate driver. This pin drives an external NMOS for short circuit protection.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	BOOT	-0.3	26.5	V
	VIN, SW, FSW, VOUT, VO_F	-0.3	20	V
	SW(3)	-3.5	24	V
	EN, VCC, COMP, MODE, FB, ILIM	-0.3	6.5	V
	NGATE	-0.3	26.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) The operating condition is less than 10ns.

7.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)		-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

PARAMETER	DEFINITION	TYP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, measured on SC8329_EVM_C53, 4 layers 65mm x 65mm x 1.6mm PCB.	29.5	℃/W
$R_{\theta JCT}$	Junction-to-case thermal resistance（top）	26	℃/W
$R_{\theta JCB}$	Junction-to-case thermal resistance（bottom）	3.5	℃/W

7.4 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.7		15	V
V_{OUT}	Output voltage range	4.5		17	V
C_{IN}	Input Capacitance	30			μF
C_{OUT}	Output capacitance	30			μF

L	Inductance		1.5		μH
F_{SW}	Switching frequency range	200		2200	kHz
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

7.5 Electrical Characteristics

T_J = 25℃ and V_{IN} = 3.6V, V_{OUT} = 9V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		15	V
V_{IN_UVLO}	Under Voltage lockout threshold (UVLO)	V_{IN} rising		2.6	2.65	V
		V_{IN} falling	2.25	2.4		V
I_Q	Operating quiescent current from VIN	MODE = 5V, EN = 5V, FB = 2V, VIN = 5V, VOUT = 10V, non-switching			2	μA
I_{SHUT}	Quiescent current from VOUT pin during shutdown	EN = 0V, VIN = 3.6V			1	μA
OUTPUT						
V_{OUT}	Output voltage range		4.5		17	V
V_{FB_REF}	Reference voltage at FB pin		0.980	1.000	1.020	V
Error Amplifier						
I_{SINK}	Comp pin sink current		14	20	26	μA
I_{SOURCE}	Comp pin source current		14	20	26	μA
G_{EA}	Error amplifier transconductance		150	190	250	μA/V
POWER SWITCH						
$R_{DS(ON)}$	High side MOSFET on-resistance			11	12	mΩ
	Low side MOSFET on-resistance			6	7	mΩ
SWITCHING FREQUENCY						
f_{SW}	Switching frequency		200		2200	kHz
t_{ON_min}	Minimum on-time			70		ns
VCC AND DRIVER						
V_{CC}	V_{CC} clamp voltage			5	5.2	V
V_{CC_UVLO}	V_{CC} UVLO threshold			2.5		V
$V_{CC\_UVLO\_HYS}$	V_{CC} UVLO hysteresis			200		mV
V_{NGATE}	NGATE voltage	Respect to VO_F		5		V
I_{NGATE}	NGATE capabilities			10		μA
LOGIC CONTROL						
V_{ENH}	EN high threshold voltage				1.2	V
V_{ENL}	EN low threshold voltage		0.4			V
R_{EN_PD}	EN internal pull-down resistance			800		kΩ
V_{MODEH}	MODE high threshold voltage			1	1.2	V
V_{MODEL}	MODE low threshold voltage		0.6	0.8		V
CURRENT LIMIT						

I_{PK_LIM}	Peak switch current limit. R_{ilim}=62kohm			20		A
SOFT START						
T_{SS}	Soft start time		2.5	4.5	5	ms
PROTECTION						
V_{OVP}	Output over voltage protection threshold	V_{OUT} rising	17.3	18	19	V
V_{OVP_HYS}	Output over voltage protection hysteresis	V_{OUT} falling below V_{OVP}	400	600	800	mV
T_{OT}	Over temperature threshold	T_J rising		165		℃
T_{OT_HYS}	Over temperature hysteresis	T_J falling below T_{OT}		15		℃

8 Feature Description

8.1 Chip enable and under voltage lockout

The SC8329 has an enable control pin EN: pulling it high enables the IC and pulling it low disables the IC. Connect EN to VIN for automatic start-up.

The SC8329 features under voltage lockout (UVLO) to prevent battery from excessive discharging and prevent the chip from malfunctioning at low input voltage. Once the falling voltage at VIN pin below the UVLO threshold (typical 2.4V) is detected, the IC is disabled. The IC resumes to normal operation when the rising voltage at VIN pin is 200mV above the UVLO threshold.

8.2 Soft start

The SC8329 has a fixed soft start function to prevent high inrush current during start-up without any external circuit. During soft start phase, the output voltage is achieved by slowly ramping up the target regulation voltage.

8.3 Mode Selection

The SC8329 integrates two different operating modes: PWM mode and PFM mode.

The SC8329 works in PWM mode when MODE pin is connected to AGND. In PWM mode, the IC always works with constant switching frequency for the whole load range. This helps achieve the best output voltage performance and fast transient response, but the efficiency is low at light load condition because of the high switching loss.

The SC8329 works in PFM mode to improve efficiency at light load when MODE pin is left floating. In PFM mode, the IC still works with constant switching frequency under heavy load condition, but under light load condition, the IC automatically changes to pulse frequency modulation operation to reduce the switching loss. The efficiency can be improved under light load condition while output voltage ripple will be a little larger compared to PWM operation. Below figure 1 shows the output voltage behavior of PFM mode.

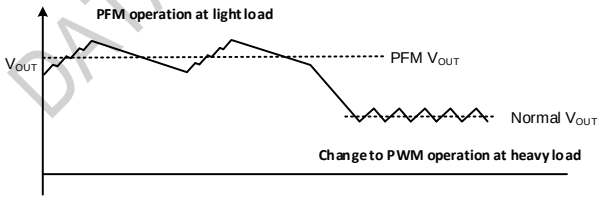


Figure 1. PFM mode illustration

8.4 Output Voltage Setting

The output voltage is fed back to FB pin through an external resistor divider. The output voltage can be set by the resistor divider as following equation.

$$V_{OUT} = V_{FB\_REF} \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

Where:

- V_{FB_REF} = 1.000V
- R_{UP} and R_{DOWN} are the resistances of resistor divider.

8.5 Adjustable Switching Frequency

A resistor should always be connected from the FSW pin to SW pin for proper operation. The switching frequency can be set by a resistor between FSW pin and SW pin. Adjustable switching frequency ranges from 200 kHz to 2.2MHz. The relationship between switching frequency and R_{FSW} plotting as follows.

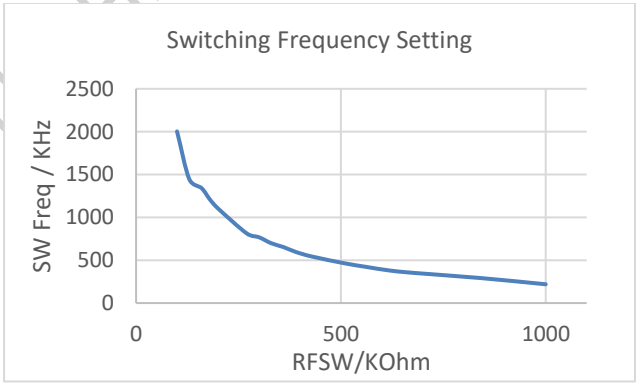


Figure 2 Switching Frequency Setting

8.6 Load Isolation N-MOS Gate Driver

SC8329 builds in load isolation N-MOS gate driver to disconnect VO_F from VOUT when VO_F short happens or SC8329 shuts down. Once SC8329 starts up, NGATE drives external isolation N-MOS with soft-starting. After VO_F goes stable, SC8329 keeps driving external isolation FET fully on.

8.7 Output Overvoltage Protection (OVP)

Output overvoltage protection is available in SC8329 preventing the circuits connected to the output from excessive overvoltage. Once the output voltage is detected above threshold (typically 20V), the SC8329 stops switching immediately until the output voltage drops the hysteresis value lower than output overvoltage protection threshold.

8.8 Overcurrent Protection (OCP)

The SC8329 has a programmable cycle-by-cycle switching peak current limit. The threshold could be set by an external resistor between ILIM and AGND. In each cycle, the internal current circuit monitors the LS-FET current. Once the sensed current reaches to current limit threshold, the LS-FET turns off. R_{ILIM} is recommended as following equation.

$$R_{ILIM} \approx 1.25 * 10^6 / I_L$$

Where I_L is peak current setting.

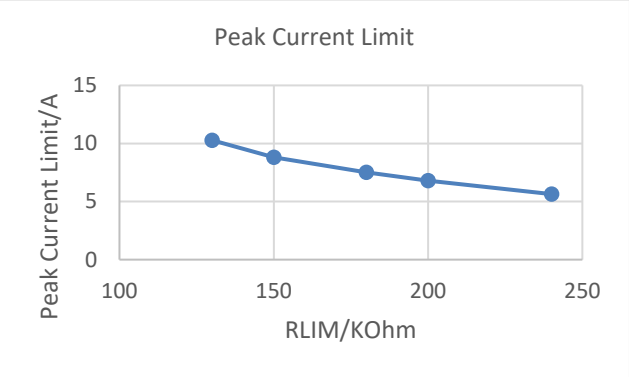


Figure 3 Peak Current Limit Setting

8.9 Short Circuit Protection

The SC8329 integrates a NMOS driver for short circuit protection. Once short circuit is detected, the SC8329 drives external NMOS open and stops switching. After a while, the SC8329 drives external NMOS closed and restart (Hiccup mode).

8.10 Over Temperature Protection (OTP)

The over temperature protection prevents the chip form operating at exceedingly high temperatures. Once the temperature of the die exceeds 165 ℃, the SC8329 shuts down. And resumes normal operation when the die temperature drops below threshold (typically 150 ℃).

8.11 Feedback compensation (COMP)

The feedback loop can be compensated by adjusting the external components to the COMP pin. Typical values are like below.

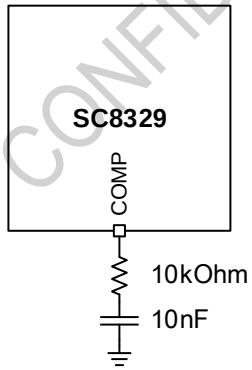


Figure 4. Feedback loop setting

9 Application Information

9.1 Input and output capacitor selection

Because of inductor current ripple, the input voltage changes if there is parasite inductance and resistance between the power supply and the inductor. At least 30µF input capacitance is required for small input voltage ripple and stability. The input capacitor can be electrolytic, tantalum or ceramic. For large switching current application, more input capacitors is recommended. If electrolytic or tantalum capacitor is used, at least 1µF ceramic should be placed close to IC's VIN pin, to improve high frequency performance.

Since MLCC ceramic capacitor has good high frequency filtering with low ESR, above 30µF X5R or X7R capacitors with higher voltage rating than operating voltage with margin is recommended for small output voltage ripple and stability. For example, if the highest operating VOUT voltage is 12V, select at least 16V capacitor, and to ensure enough margin, 25V voltage rating capacitor is recommended.

The high capacitance electrolytic capacitor and tantalum capacitor can be used for stable output but capacitor voltage rating should be higher than the highest operating voltage. When the tantalum capacitor is used, at least 1µF ceramic capacitor is placed in parallel. If the electrolytic capacitor is used, much more ceramic capacitors are required.

For large input current applications, a high capacitance electrolytic capacitor is required to reduce the impact of parasitic parameters of long conductors. Further more, a 100nF MLCC capacitor should be placed close the output of the IC, in order to relax ringing on the SW node and better EMI performance.

9.2 Inductor selection

For the SC8329 system stability, the inductance of 1µH ~ 4.7µH inductor is required. High inductance (3.3µH ~ 4.7µH) is used in the system where the input voltage and output voltage gap is big, such as 3V VIN and 16V VOUT; Low inductance (1µH) is used in the system which the input voltage and output voltage difference is small but high current is required. Typically, 1.5µH inductor is recommended. The inductance can be adjusted for high efficiency and optimization in application.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so around 3mΩ DCR is recommended for the first selection. If the power is relatively small, high DCR inductor can be selected. But if switch on current is high, just like around 10A, select the lowest DCR inductor as much as possible, because 10mΩ DCR also causes 1W power loss.

The inductor saturation current I_{SAT} should be higher than input output current with sufficient margin.

9.3 NMOS selection

The NMOS is connected between the output node of boost converter and subsequent circuits, which protects short circuit.

Considering PCB parasitic parameters during operation, driver voltage can be higher than VCC due to transient overshoot, and ±12V or higher V_{GS} is recommended to secure sufficient margin.

The MOSFET current I_D should be higher than the highest peak current with enough margin.

9.4 Layout Guide

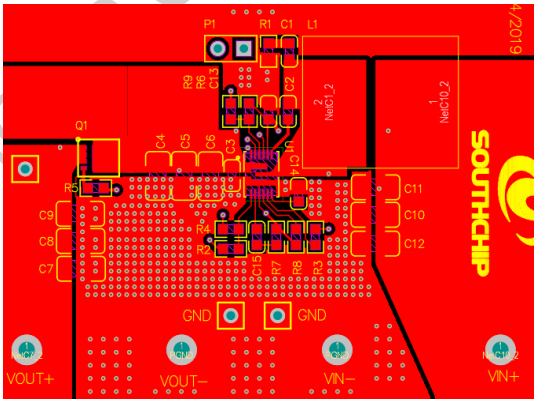


Figure 5 PCB layout reference

Efficient PCB layout can make SC8329 perform well. A poor layout could result in reduced performance. Some tips are suggested as follows to get a good performance.

1. Output capacitor (C3~C6) should be placed as closed as possible. Place a smaller ceramic (100nf) capacitor next to the output node of converter.

2. All traces connected to the SW pin should be as short as possible, and always use a ground plane under the switching regulator to minimize inter plane coupling.

3. Input loop should be as small as possible.

4. Place resistor divider as close to FB pin as possible and make sure traces connected FB far away from SW node.

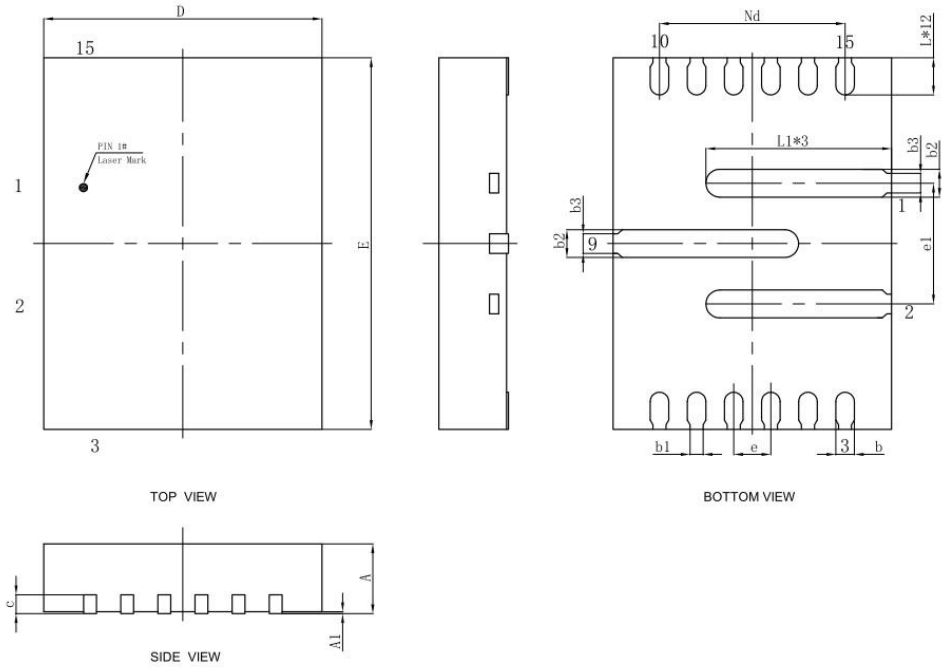
5. Low-side resistor of FB resistor divider or peak current limit setting resistor should be connected to AGND for lower ripple and stable peak current limit. AGND and PGND should be connected with single point.

6. PGND vias closed to SC8329 should be as much as possible for enhanced thermal dissipation.

7. It is essential to adopt 4-layer PCB for high input current application.

MECHANICAL DATA

FCQFN15L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
b2	0.25	0.30	0.35
b1	0.21REF		
c	0.203REF		
D	2.90	3.00	3.10
Nd	2.00BSC		
e	0.40BSC		
e1	1.30BSC		
E	3.90	4.00	4.10
L	0.35	0.40	0.45
L1	1.95	2.00	2.05

RECOMMENDED FOOTPRINT