3V-24V Input, 5.5A Current Limit Switch

GENERAL DESCRIPTION

The PW1558 is an advanced 24V 5.5A rated current limit switch which provides overload, short circuit, input voltage surge, excessive inrush current, overtemperature and reverse current protections to power the system. The built-in 24mΩ ultra low RDS(ON) power switch helps reducing power loss during normal operation. Current limit level can be set 1A to 5.5A with an external resistor. The PW1558 integrates thermal fold-back function and over temperature shutdown protection.

The PW1558 has all time reverse current blocking function regardless of the enable signal EN logic states. A fast role swap function is also implemented to comply the timing requirement defined in the USB Power Delivery Specification. The integrated input and output discharge function which allows the voltage levels at the input and output ports to be discharged to meet the requirement of the USB Power Delivery Specification.

FEATURES

- Adjustable Current Limit 1A~5.5A and Soft-start (SS) Time
- Wide Input Voltage Range from 3V to 24V with Surge Up to 28V
- Adjustable Input Over- voltage Protection (OVP) Threshold
- Support Fast Role Swap Function through a logic signal to bypass Soft-start Time
- All Time True Reverse Current Blocking
- Short-circuit Protection , Fault Indicator , Input and Output Discharge Function
- Thermal Shutdown Protection and Auto Recovery
- QFN2.5×3.2-16L Packages

APPLICATIONS

- Servers and Tablets
- Docking Stations
- Power Accessories
- USB Type-C PD power switch

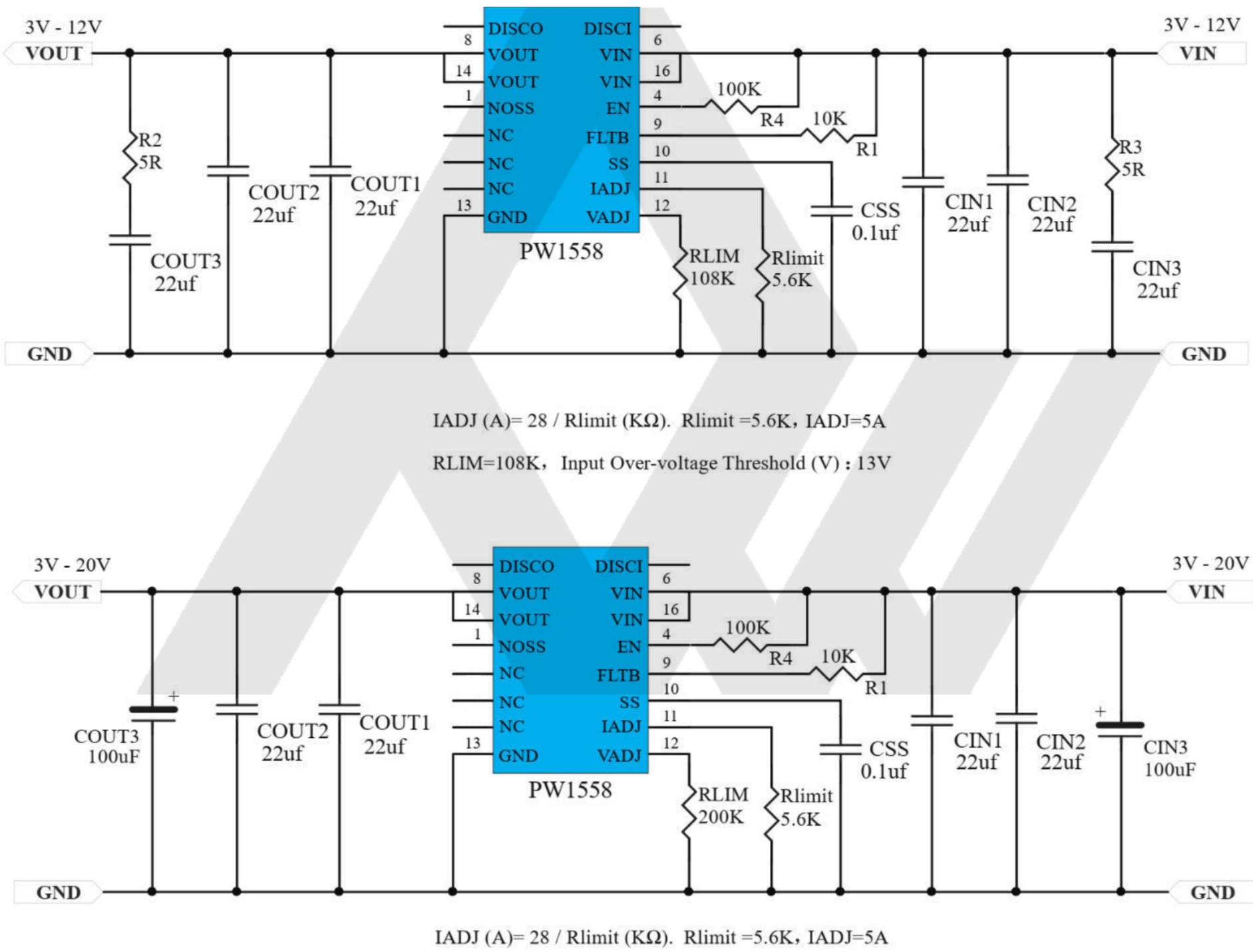
Products

PCB Design Scheme

TYPICAL APPLICATION CIRCUIT

IADJ (A)= 28 / Rlimit (KΩ). Rlimit =7K，IADJ=4A

Application Schematic



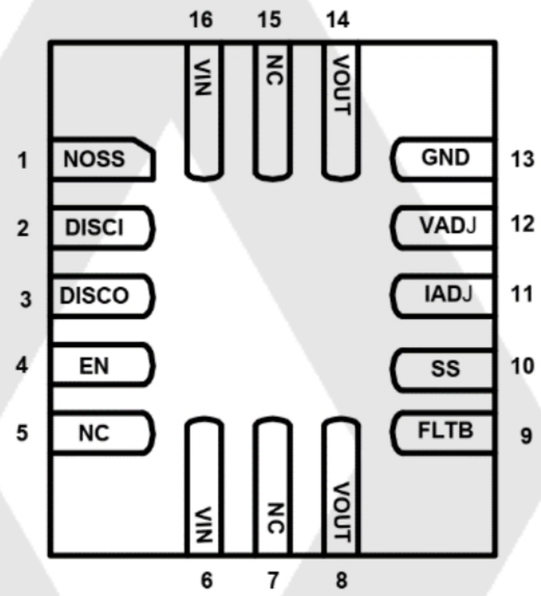
IADJ (A)= 28 / Rlimit (KΩ). Rlimit =5.6K，IADJ=5A

RLIM=108K， Input Over-voltage Threshold (V)：13V

IADJ (A)= 28 / Rlimit (KΩ). Rlimit =5.6K，IADJ=5A

RLIM=200K， Input Over-voltage Threshold (V)：24V

Pin Configuration/ Description



PIN NO	PIN NAME	DESCRIPTION
1	NOSS	Fast Role Swap Function enable pin. Logic Low enables soft-start during startup. The output voltage ramping up rate is set by the capacitor value on the SS pin. Logic High disables soft-start function during startup.
2	DISCI	VIN port discharge control input. Logic High discharges VIN port to GND through an internal 350Ω pull down resistor.

3	DISCO	VOUT port discharge control input. Logic High discharges O VUT port to GND through an internal 350Ω pull down resistor.
4	EN	The enable control pin of thePW1558 chip. To enable the device this pin needs to be pulled high. Pulling this pin low disables the device. This pin has an pull-down resistor of typically 1MΩ when the device is disabled.
5,7,15	NC	Not Connection.
6,16	VIN	Input Supply pin.
8,14	VOUT	Output pin.
9	FLTB	Fault event indicator open drain output pin. A pull-up resistor is connected from FLTB pin to any voltage less than 28V. Active Low indicates input over-voltage, over-current, over-temperature and reverse current fault events.
10	SS	Soft-start time program pin. Connect a capacitor to ground to program the soft start time.
11	IAJD	Current limit program pin. Program the switch current limit by connecting a resister to ground. IADJ pin can't be shorted to GND. If the system requires a single component fail safe, choose 2 resistor in series to program current limit.
12	VADJ	Input over-voltage protection threshold set pin. Program input over-voltage protection threshold by connecting a resister to ground. Recommend to set input over-voltage protection threshold range 5V to 24V.
13	GND	Ground pin.

Absolute Maximum Rating

Parameter	VALUE	Unit
VIN and VOUT ,EN, FLTB to GND	-0.3 to +28	V
VIN to VOUT	-28 to +28	V
The other pins to GND	-0.3 to +6.5	V
Lead Temperature(Soldering 10s)	+260	°C
Maximum Power Dissipation(TA=25°C)	2.6	W
Junction Temperature Range	-40 to +155	°C
Storage Temperature Range	-65 to +150	°C
Thermal Resistance(θJA)	55.12	°C/W
Thermal Resistance(θJC)	15.6	°C/W

Recommend Operating Conditions

Parameter	VALUE	Unit
VIN and VOUT	-0.3 to +24	V
Maximum Switch Continuous Current	5	A
Ambient Temperature Range	-40 to +85	°C
Junction Temperature Rang	-40 to +125	°C

Note:

(1): Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.

(2): The device is not guaranteed to function outside of the recommended operating conditions.

(3): Measured on JESD51-7, 4-Layer PCB.

(4): The maximum allowable power dissipation is a function of the maximum junction temperature TJ_MAX=125°C, the junction to ambient thermal resistance Θja, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD_MAX= (TJ_MAX-TA)/Θja. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Electrical Characteristics

TA = +27°C, VIN= VEN =5V, Rlimit=5.6kΩ, RLIM=200kΩ and CSS=10nf, unless otherwise specified.

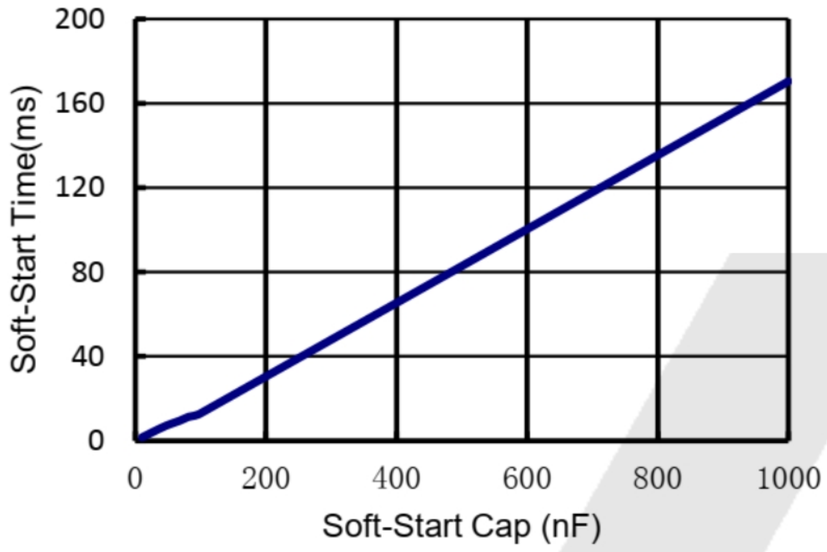
PARAMETER	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	VIN		3		24	V
EN Turn-on Threshold	VEN_ON	EN Rising	1.5		24	V
EN Turn-off Threshold	VEN_OFF	EN Falling			0.4	V
Quiescent Current	IQ	VIN=5V~24V, VEN=VIN		450	600	μA
Shutdown Current	ISHDN	VIN=24V, VEN=0V		10	20	μA
Current Limit IADJ Setting Factor	KIADJ	IILIM=1A~5A		28		A*KΩ
Current Limit	IIADJ	Rlimit =28 kΩ		1		A
Current Limit	IIADJ	Rlimit =9.33kΩ		3		A
Current Limit	IIADJ	Rlimit =5.6 kΩ		5		A
EN Pull-Down Resistance	RENPD			1		MΩ
Input Under-voltage (UVLO) Threshold	VUVLO	VIN Rising		2.75		V
Input Under-voltage Hysteresis	VUVLOHYS	VIN Falling		300		mV
Power On Delay Time	tpwrdly			500		us
Power Switch On Resistance	RDS(ON)	VIN=5V~24V, IOUT=1A		24		mΩ
Reverse Current Blocking Threshold	VRVBINTH	VIN-VOUT	-10	-15	-20	mv
Reverse Current Blocking Response time	Trvb				5	μs
Input Over-voltage Threshold VADJ Setting Factor	KOVP	VOVP =KOVP*VVADJ VOVP=5V~24V		1200		
VADJ Source Current	IVADJ	VIN=5V, RLIM=50kΩ		10		μA
Input Over-voltage Threshold	VOVP	VIN Rising, RILIM=50kΩ		6		V
Input Over-voltage Threshold	VOVP	VIN Rising, RLIM=200kΩ		24		V
Input Over-voltage Threshold Hysteresis	VOVPHYS	VIN Falling, RLIM=50kΩ		5.3		V
		VIN Falling, RLIM =200kΩ		23.3		V

Soft-start Time	TSS	CSS=100nF		16		msec
		SS floating		0.8		msec
SS bias current	ISS	VIN=5V, SS short to GND		2.5		μA
FLTB Output Low Voltage	VFOL	Fault Event, IFLTB=1mA			350	mV
FLTB Leakage Current	IFlkg	No Fault Event, VFLTB=5V		0.01	1	μA
FLTB delay time	TFLTB	Over current or short circuit event		3		mS
FLTB release delay time		Fault Event remove		1.5		mS
NOSS, DISCI, DISCO Logic High Threshold	VIH	VIN=5V~24V	1.5		5.5	V
NOSS, DISCI, DISCO Logic Low Threshold	VIL	VIN=5V~24V			0.4	V
NOSS, DISCI, DISCO Input Leakage Current	ILKG	VNOSS/DISCI/DISCO=0V and 5V	-1		1	uA
VIN, VOUT Discharge resistance	RDISC	VDISCI/DSICO=5V		350		Ω
Thermal Shutdown Temperature	TSD			150		°C
Thermal Shutdown Hysteresis	THYS			25		°C

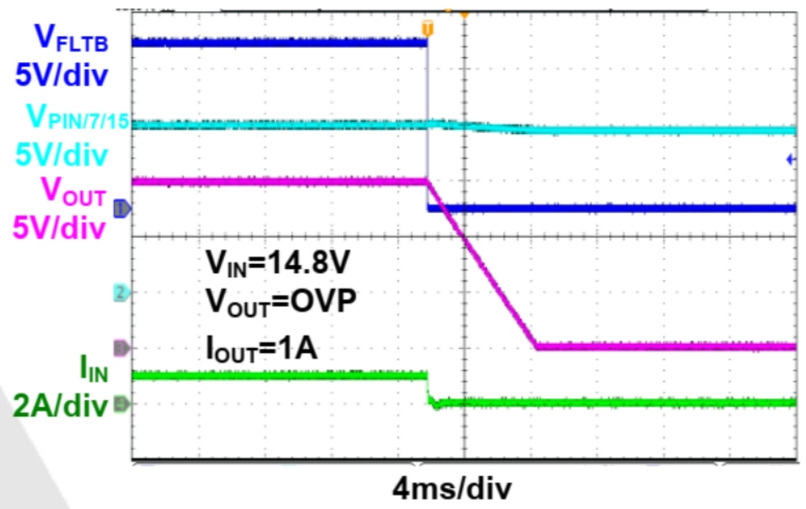
Typical Performance Characteristics

(CIN=22uF*2+100uF, COUT = 22uF*2+100uF TA =+25℃ , unless otherwise noted.)

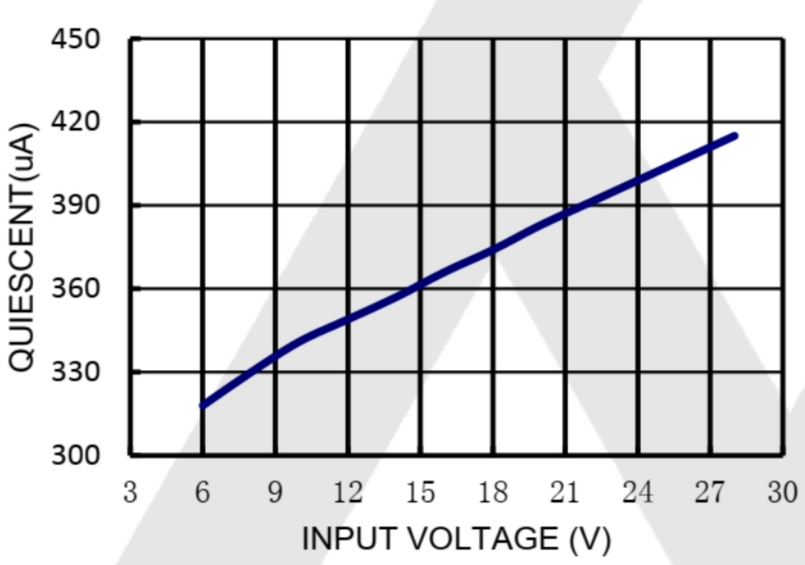
Soft-Start Time Vs. SS Capacitance



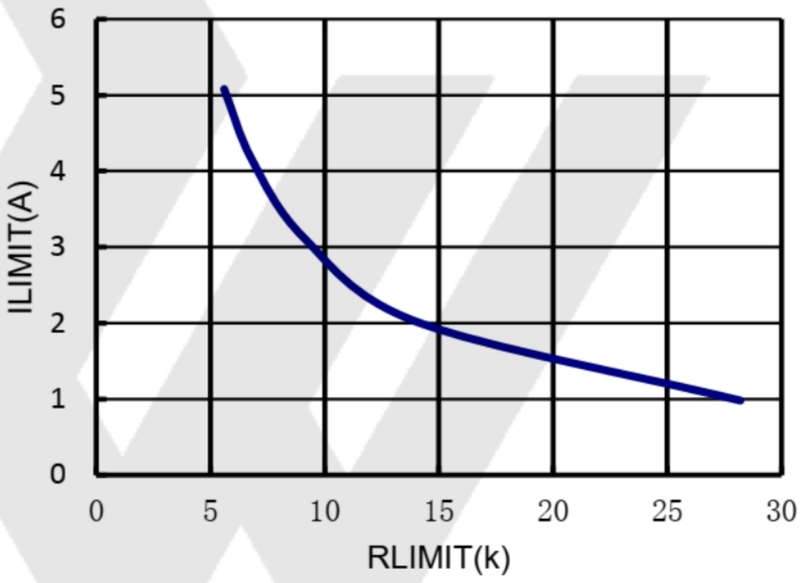
Input Over Voltage Protection



Quiescent Current Vs. Input Voltage



Current Limit Vs. R_{limit} Resistor Value



Detailed Description

ThePW1558 is an advanced current limit power switch with adjustable soft-start, adjustable current limit threshold, input under-voltage, adjustable input over-voltage, over-temperature and short circuit protections. The integrated back to back power switch has true reverse blocking function regardless of the enable pin EN logic states. When EN pin is pulled low, the power switch is turned off to prevent current flowing back from output VOUT voltage to input VIN voltage. A high level on EN pin enables the power switch. The power switch is turned off when the output voltage exceeds the input voltage. The power switch resumes on when the output VOUT voltage drops below the input VIN voltage. A low level on NOSS pin enables the power switch soft-start function. While the input VIN voltage rises, the power switch starts conducting and allows current to flow slowly from VIN to VOUT. Users have the ability to control the output voltage ramp up time by connecting a capacitor between SS pin and GND. A high level on NOSS pin bypasses the power switch soft-start function and turns on the power switch quickly to power the system with fast role swap requirement. After a successful start-up sequence, the device actively monitors its load current to ensure that the overload current limit IADJ programmed by pin IADJ is not exceeded. The device monitors input voltage and turns off the power switch if the input voltage spike exceeds the input over-voltage threshold which is set by pin VADJ. Both current limit and input over-voltage protection keep the output device safe from the harmful input voltage and current transients. The device has a built-in thermal sensor. If the device junction temperature (TJ) exceeds the thermal regulation point +125°C, the current limit will be decreased until TJ is regulated around +125°C. In some deadly output short circuit events, and the device junction temperature (TJ) quickly rises and exceeds the thermal shutdown threshold TSHDN, typically +150°C, the device will shut down the power switch and disconnect the load from the input supply. The PW1558 device remains off during a cooling period until the junction temperature falls below TSHDN –20°C, after the device will attempt to restart.

Application Information

Enable

Enable interface pin EN has ON/OFF threshold of 1.5V(Min) and 0.4V(Max) respectively. Pull EN pin low below OFF threshold (<0.4V) to disable the power switch and all protection circuits, and the device is in the low power shutdown mode and draws only 10μA current from the input supply. Pull EN pin High above ON threshold (>1.5V) to enable the power switch and all protection circuits. There is an internal 1MΩ pull-down resistor to ensure the power switch OFF if EN pin is floated. EN pin can tolerate maximum 28V voltage spike.

Input Under-voltage Lockout

When EN pin is Logic Hi, thePW1558 monitors the input supply voltage VIN and allows the power switch turning on if the input voltage is above input under-voltage lockout threshold VUVLO (Typical 2.75V). If the input voltage is below input under-voltage lockout threshold VUVLO, the device turns off the power switch.

Input Over-voltage Protection

When EN pin is Logic Hi, thePW1558 monitors the input supply voltage VIN . The input over-voltage protection circuit disables the power switch and pulls FLTB pin LOW to report the fault condition If the input voltage is above input over-voltage threshold VOVP. Once the input voltage drops below input over-voltage threshold VOVP and no other protection circuit is active, the power switch resumes ON.

An external resistor RLIM is connected from VADJ pin to GND to set the input over-voltage protection threshold VOVP. The device sources typical 10μA to VADJ pin. The voltage drop VVADJ across the RLIM resistor externally adjusts the input over-voltage threshold from 5V to 24V

$$V_{OVP}=K_{OVP} \times V_{VADJ}=1200 \times 10uA \times RLIM \cdots\cdots\cdots\cdots$$

R_{LIM} (kΩ)	46	75	108	200
Input Over-voltage Threshold (V)	5.5	9	13	24

The recommended input over-voltage threshold setting is shown in the:

Soft Start and Fast Role Swap (FRS)

When EN pin is asserted high, and NOSS pin is asserted low, the soft start control circuitry controls the gate voltage of the power switch in a manner such that the output voltage is ramped up linearly until it reaches input voltage level during power on. The in-rush current at power-on is limited by the regulated output voltage ramp up rate through the soft-start time. The built-in internal soft-start time is typical 0.8msec. If users prefers the soft-start time longer than 0.8msec, connect an external capacitor CSS between SS pin and ground to re-adjust the soft-start time. The external soft-start time is approximately calculated by Equation (2):

$$T_{SS}=C_{SS}\times 1.67\times 10^{5} \quad \cdots\cdots\cdots\cdots\cdots\cdots$$

CSS Value (nF)	None or < 4.7nF	10	33	47	100
Soft-start Time TSS (msec)	0.8	1.6	5.5	7.8	16.7

The recommended soft-start time setting is shown in the:

When both EN pin and NOSS are asserted high, the PW1558 bypasses soft start time and turns on the power switch immediately. This features allows the PW1558 acting as a new power source to support the system with Fast Role Swap (FRS) requirements. Figure 2 shows the FRS timing requirement defined in the USB PD revision 3.0. To support Fast Role Swap operation, connect thePW1558 input supply pin IN to a 5V power source and connect the PW1558 output pin OUT to another power source VBUS which supply voltage range is from 0V to 24V. When the PW1558 output voltage is above the input voltage (VOUT - VIN > 15mV), the power switch is turned off to prevent reverse current flowing from VOUT to VIN. Once the output voltage falls below the input voltage (VIN>VOUT), the reverse current condition is not valid. The Fast Role Swap function is triggered, and the PW1558 power switch is quickly switched ON within 100μs. Figure 3 show the PW1558 FRS control sequence.

Current Limit and Short Circuit Protection

For current limited adaptors or power sources, users can program the input current limit level to prevent the load current overload the source. The PW1558 current limit is set with an external resistor Rlimit connected between IADJ and GND. If over-load occurs, the internal circuitry limits the input current based on the value of Rlimit and pulls FLTB pin LOW to report the fault condition. IADJ pin can't be short to GND. If the system requires a single component fail safe, choose 2 resistor in series to program input current limit. The current limit resistor Rlimit is selected with:

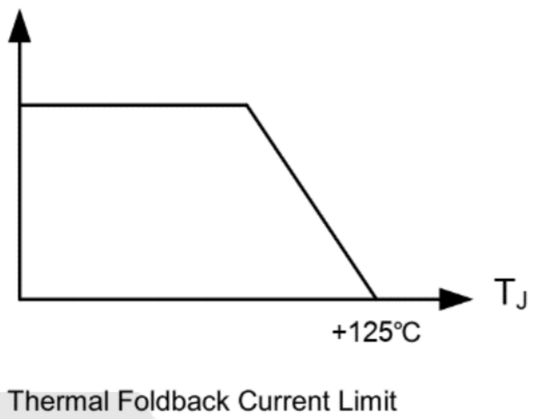
$$Rlimit\ (k\Omega) = 28 / IIADJ \quad (A)$$

The PW1558 also integrates a fast-trip comparator to quickly turn off the power switch when the output voltage is shorted to ground. The device operates hiccup mode in short circuit protection.

Once the short circuit fault is detected, the power switch is turned off and is forced off for a given time. At the end of the predetermined time, a restart attempt is made by soft-starting the power switch. If the over-load condition has been removed, the power switch will turn on and operate normally; otherwise, the device will see another over-current event and shut off the power switch again, repeating the previous cycle. The excess heat due to overload lasts for only a short duration in the hiccup cycle, hence the junction temperature of the power devices is much lower.

Thermal Foldback and Thermal Shutdown Protection

The device continuously monitors the load current and keeps it limited to the value programmed by Rlimit. In the normal operation or current limit protection mode, If power dissipation in the internal MOSFET PD = (VIN – VOUT) × IOUT is too high, PW1558 will engage thermal foldback to reduce the current limit value so that the junction temperature (TJ) is maintained around +125°C. Figure 4. shows thermal foldback current limit. In some deadly output short circuit events, the output voltage drops with current limit IIADJ. It will result in the increasing junction temperature TJ with the increased power consumption and the device junction temperature (TJ) quickly rises and exceeds the thermal shutdown threshold TSHDN, typically +150°C, the device will shut down the power switch and disconnect the load from the input supply. ThePW1558 device remains off during a cooling period until the junction temperature falls below TSHDN –20°C, after the device will attempt to restart.



Thermal Foldback Current Limit

Reverse Current Protection

ThePW1558 has all time reverse current protection regardless of the EN logic level. The voltage difference VIN - VOUT between the VIN and VOUT pin port is monitored continuously. Once the input voltage drops below the output voltage, the device immediately turns off the power switch to prevent the current flowing from the opposite direction and pulls FLTB pin LOW to report the fault condition. When the reverse current condition is no longer valid, the input voltage rises above the output voltage, the power switch resumes ON, and FLTB pin becomes high impedance HiZ.

VIN and VOUT PIN Port Discharge Function

The input VIN and output VOUT port discharge function is controlled via two external control inputs DISCI and DISCO, and the internal discharge resistance is around 350Ω. DISCI=Hi discharges the input VIN port to GND, and DISCI=Lo disables the input discharge function. DISCO=Hi discharges the output VOUT port to GND, and DISCO=Lo disables the output discharge function.

Input Capacitor Selection

Place a high quality 0.1μF in parallel with at least a 22μF or higher ceramic type X5R or X7R bypass capacitor at the VIN pin to ground GND for proper decoupling. The input capacitor voltage rating

should exceed the maximum input voltage range.

Output Capacitor Selection

Place a high quality 0.1μF in parallel with at least 22μFx2 or higher ceramic type X5R or X7R bypass capacitor at the VOUT pin to ground GND for proper decoupling. The output capacitor voltage rating should exceed the maximum input voltage range. In the event of the output short circuit with a long cable, the cable parasitic inductance and the output ceramic forms high Q LC-Tank. The short circuit high current slew rate di/dT causes the output VOUT pin going negative voltage up to -10V. The VOUT pin negative voltage spike triggers ON the VOUT pin ESD diode and put voltage stress on the internal power switch. If the voltage difference between VIN pin and VOUT pin exceeds 28V, the power switch will be permanently damaged. In order to limit VOUT pin negative voltage spike in the short circuit event, recommend to add an additional 100μF or 220μF Electrolytic capacitor in parallel with output ceramic capacitors. Due to high ESR value of Electrolytic capacitor, the output parasitic L-C tank Q is damped.

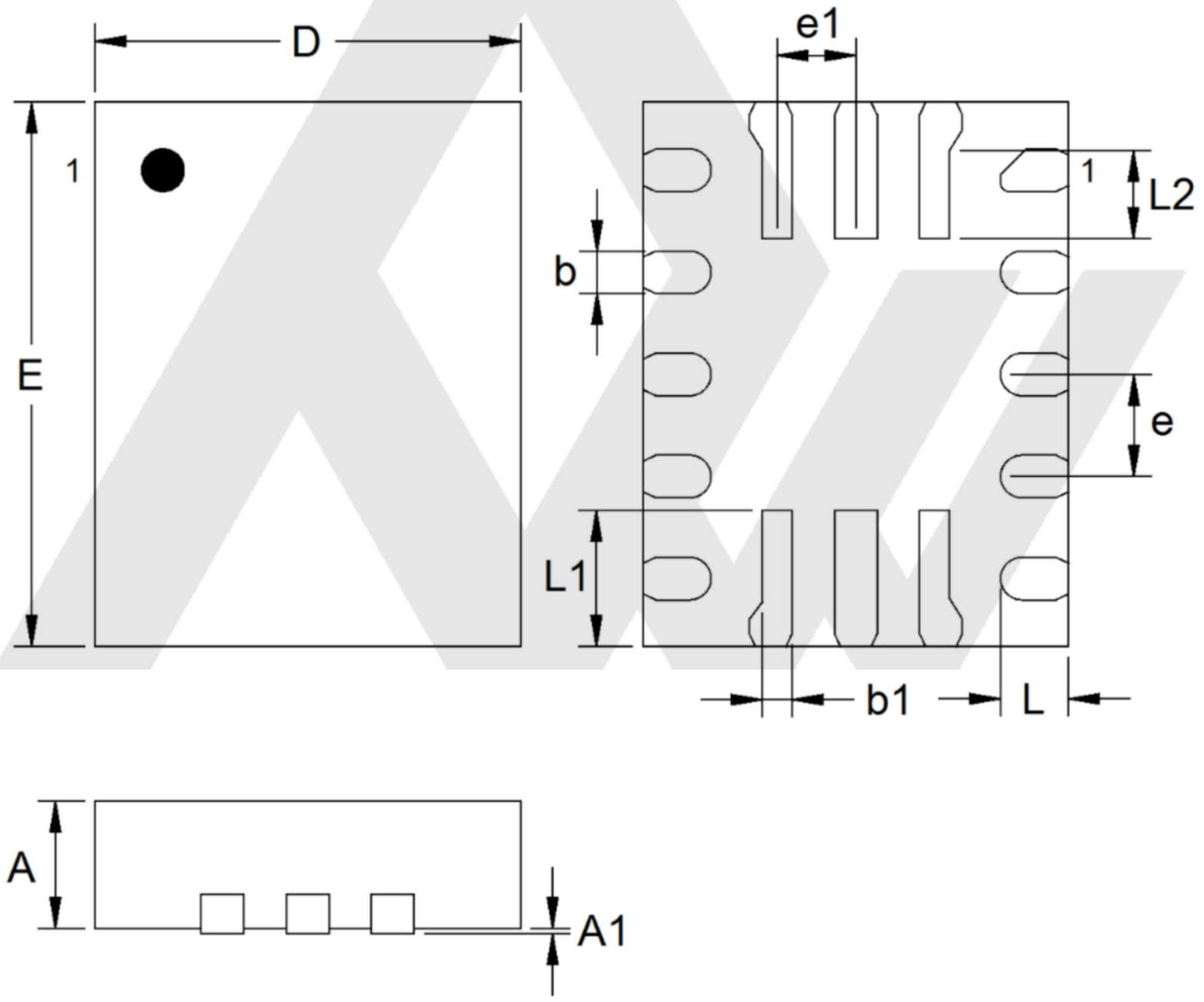
Layout Guidelines

output ceramic forms high Q LC-Tank. The short circuit high current slew rate di/dT causes the output VOUT pin going negative voltage up to -10V. The VOUT pin negative voltage spike triggers ON the VOUT pin ESD diode and put voltage stress on the internal power switch. If the voltage difference between VIN pin and VOUT pin exceeds 28V, the power switch will be permanently damaged. In order to limit VOUT pin negative voltage spike in the short circuit event, recommend to add an additional 100μF or 220μF Electrolytic capacitor in parallel with output ceramic capacitors. Due to high ESR value of Electrolytic capacitor, the output parasitic L-C tank Q is damped.

- Place the input and output bypass capacitors as close as possible to the VIN and VOUT pins.
- VIN and VOUT pins connected as below pattern to reduce impedance improving the power los
- Use a ground plane to enhance the power dissipation capability of the PW1558.

Package Information

QFN 16L 2.5x3.2mm Package Outline Dimensions
Unit: inches/mm



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.30	0.008	0.012
b1	0.12	0.23	0.005	0.009
D	2.40	2.60	0.094	0.102
E	3.10	3.30	0.122	0.130
e	0.60 BSC.		0.024 BSC	
e1	0.50 BSC.		0.020 BSC	
L	0.30	0.50	0.012	0.020
L1	0.70	0.90	0.028	0.035
L2	0.52 REF.		0.020 REF.	

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