Triple-Channel, High-Side Measurement, Shunt and Bus Voltage Monitor with I²C™ Interface

Check for Samples: INA3221

FEATURES

- **Senses Bus Voltages From 0 V to +26 V**
- **Reports Shunt and Bus Voltage**
- **High Accuracy:**
  - **Offset Voltage: ±80 µV (max)**
  - **Gain Error: 0.25% (max)**
- **Configurable Averaging Options**
- **Four Programmable Addresses**
- **Power-Supply Operation: 2.7 V to 5.5 V**
- **Programmable Alert and Warning Outputs**

APPLICATIONS

- **Computers**
- **Power Management**
- **Telecom Equipment**
- **Battery Chargers**
- **Power Supplies**
- **Test Equipment**

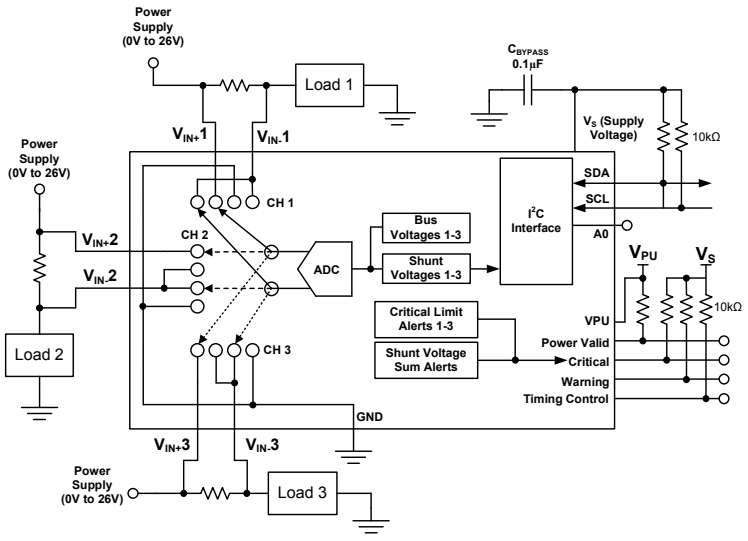
DESCRIPTION

The INA3221 is a three-channel, high-side current and bus voltage monitor with an I²C interface. The INA3221 monitors both shunt voltage drops and bus supply voltages in addition to having programmable conversion times and averaging modes for these signals. The INA3221 offers both critical and warning alerts to detect multiple programmable out-of-range conditions for each channel.

The INA3221 senses current on buses that can vary from 0 V to +26 V. The device is powered from a single +2.7-V to +5.5-V supply and draws 350 µA (typ) of supply current. The INA3221 is specified over the operating temperature range of –40°C to +125°C. The I²C interface features four programmable addresses.

RELATED PRODUCTS

DESCRIPTION	DEVICE
High- or low-side, bi-directional current and power monitor with two-wire interface	INA226
Zero-drift, bi-directional current power monitor with two-wire interface	INA219
Current and power monitor with watchdog, peak-hold, and fast comparator functions	INA209
Zero-drift, low-cost, analog current-shunt monitor series in small package	INA210, INA211, INA212, INA213, INA214



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA3221AIRGV	QFN-16	RGV	INA3221

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			VALUE	UNIT
Voltage		Supply, V_S	6	V
Analog inputs	IN+, IN–	Differential (VIN+) – (VIN–)(2)	–26 to +26	V
		Common-mode	–0.3 to +26	V
	VBUS, VPU		26	V
Digital outputs		Critical, warning, power valid	6	V
		Timing control	26V	V
Serial bus		Data line, SDA	(GND – 0.3) to +6	V
		Clock line, SCL	(GND – 0.3) to (V_S + 0.3)	V
Current		Input, into any pin	5	mA
		Open-drain, digital output	10	mA
Temperature		Storage	–65 to +150	°C
		Junction	+150	°C
Electrostatic discharge (ESD) ratings		Human body model (HBM)	2500	V
		Charged-device model (CDM)	1000	V
		Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) VIN+ and VIN– can have a differential voltage of –26 V to +26 V; however, the voltage at these pins must not exceed the range of –0.3 V to +26 V.

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ELECTRICAL CHARACTERISTICS: V_S = +3.3 V

At T_A = +25°C, VIN+ = 12 V, V_{SENSE} = (VIN+) – (VIN–) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

PARAMETER			CONDITIONS	INA3221 MIN	INA3221 TYP	INA3221 MAX	UNIT
INPUT							
	Voltage input range	Shunt		–163.84		163.8	mV
		Bus		0		26	V
CMR	Common-mode rejection		VIN+ = 0 V to +26 V	110	120		dB
V_{OS}	Offset voltage, RTI(1)	Shunt			±40	±80	µV
			T_A = –40°C to +125°C		0.1	0.5	µV/°C
PSRR			vs power supply, V_S = +2.7 V to +5.5 V		15		µV/V
V_{OS}		Bus			±8	±16	mV
			T_A = –40°C to +125°C			80	µV/°C
PSRR			vs power supply		0.5		mV/V
I_{IN+}	Input bias current				10		µA
$I_{IN–}$					10 || 670		µA || kΩ
	Input leakage(2)		(VIN+ pin) + (VIN– pin), power-down mode		0.1	0.5	µA
DC ACCURACY							
	ADC native resolution				13		Bits
	1-LSB step size		Shunt voltage		40		µV
			Bus voltage		8		mV
	Voltage gain error	Shunt			0.1	0.25	%
			T_A = –40°C to +125°C		10	50	ppm/°C
		Bus			0.1	0.25	%
			T_A = –40°C to +125°C		10	50	ppm/°C
DNL	Differential nonlinearity				±0.1		LSB
$t_{CONVERT}$	ADC conversion time		CT bit = 000		140	154	µs
			CT bit = 001		204	224	µs
			CT bit = 010		332	365	µs
			CT bit = 011		588	646	µs
			CT bit = 100		1.1	1.21	ms
			CT bit = 101		2.116	2.328	ms
			CT bit = 110		4.156	4.572	ms
			CT bit = 111		8.244	9.068	ms
SMBus							
	SMBus timeout(3)				28	35	ms
DIGITAL INPUT/OUTPUT							
C_I	Input capacitance				3		pF
	Leakage input current		0 V ≤ V_{IN} ≤ V_S		0.1	1	µA
V_{IH}	Input logic levels			0.7 (V_S)		6	V
V_{IL}				–0.5		0.3 (V_S)	V
V_{OL}	Output logic levels	SDA, critical, warning, PV	V_S > +2.7 V, I_{OL} = 3 mA	0		0.4	V
		TC	V_S > +2.7 V, I_{OL} = 1.2 mA	0		0.4	V
V_{hys}	Hysteresis voltage				500		mV

(1) RTI = Referred-to-input.
(2) Input leakage is positive (current flows into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
(3) SMBus timeouts in the INA3221 reset the interface whenever SCL is low for more than 28 ms.

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ELECTRICAL CHARACTERISTICS: V_S = +3.3 V (continued)

At T_A = +25°C, VIN+ = 12 V, V_{SENSE} = (VIN+) – (VIN–) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

PARAMETER		CONDITIONS	INA3221 MIN	INA3221 TYP	INA3221 MAX	UNIT
POWER SUPPLY						
Operating supply range			+2.7		+5.5	V
Quiescent current				350	450	µA
	Power-down mode			0.5	2	µA
Power-on reset threshold				2		V
TEMPERATURE RANGE						
Specified range			–40		+125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		INA3221 RGV 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	36.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	42.7	
θ_{JB}	Junction-to-board thermal resistance	14.7	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	14.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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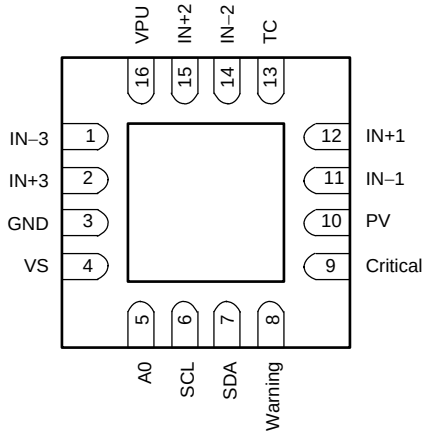
PIN CONFIGURATIONS

RGV PACKAGE
QFN-16
(Top View)



PIN DESCRIPTIONS

PIN		ANALOG OR DIGITAL INPUT/OUTPUT	DESCRIPTION
NAME	NO		
A0	5	Digital input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 7 shows pin settings and corresponding addresses.
Critical	9	Digital output	Conversion-triggered critical alert; open-drain output.
GND	3	Analog	Ground
IN–1	11	Analog input	Connect to load side of the channel 1 shunt resistor. Bus voltage is the measurement from this pin to ground.
IN+1	12	Analog input	Connect to supply side of the channel 1 shunt resistor.
IN–2	14	Analog input	Connect to load side of the channel 2 shunt resistor. Bus voltage is the measurement from this pin to ground.
IN+2	15	Analog input	Connect to supply side of the channel 2 shunt resistor.
IN–3	1	Analog input	Connect to load side of the channel 3 shunt resistor. Bus voltage is the measurement from this pin to ground.
IN+3	2	Analog input	Connect to supply side of the channel 3 shunt resistor.
PV	10	Digital output	Power valid alert; open-drain output.
SCL	6	Digital input	Serial bus clock line; open-drain input.
SDA	7	Digital I/O	Serial bus data line; open-drain input/output.
TC	13	Digital output	Timing control alert; open-drain output.
VPU	16	Analog input	Pull-up supply voltage used to bias power valid output circuitry.
VS	4	Analog	Power supply, 2.7 V to 5.5 V.
Warning	8	Digital output	Averaged measurement warning alert; open-drain output.

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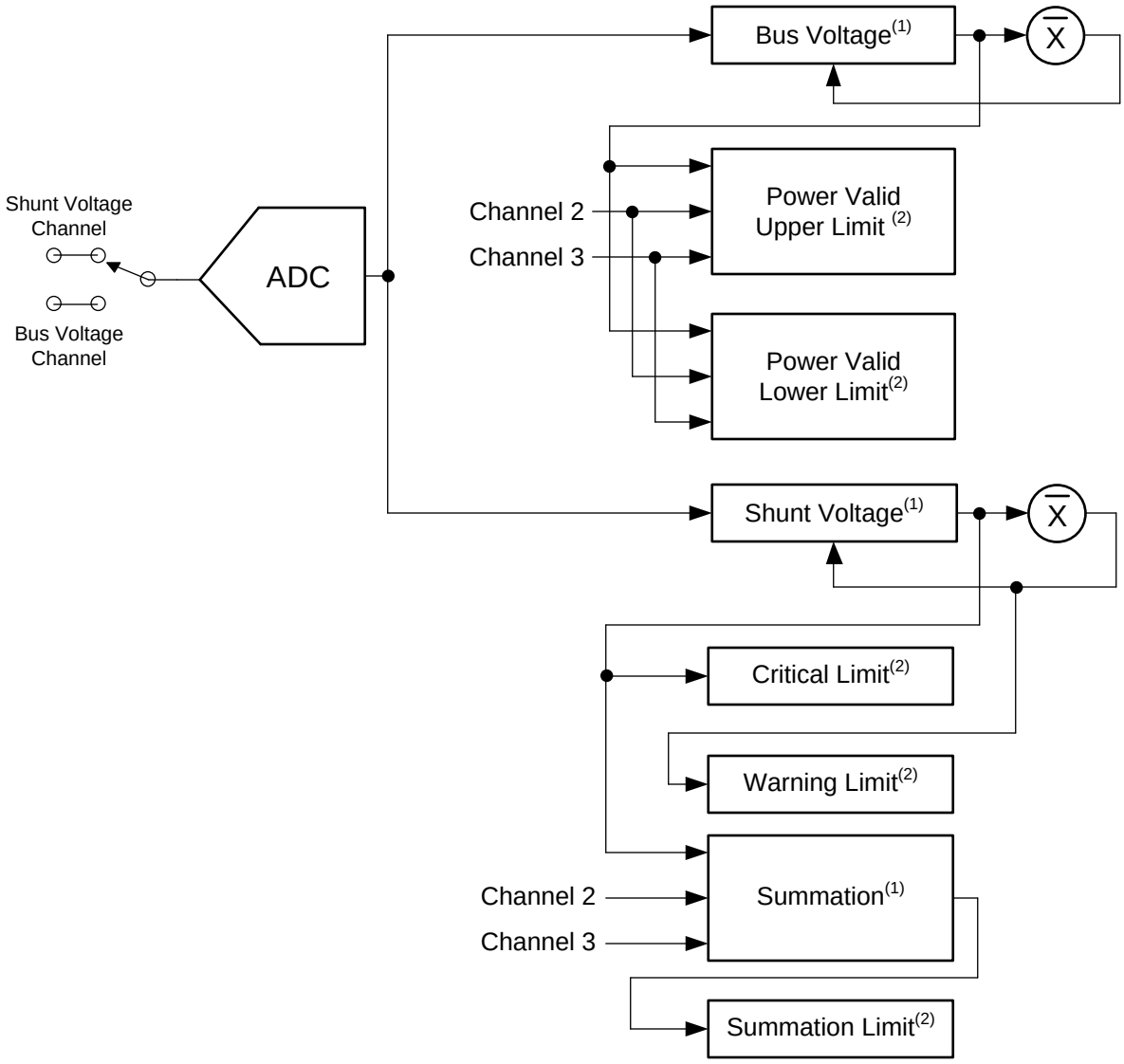
REGISTER BLOCK DIAGRAM



(1) Read-only.

(2) Read/write.

Figure 1. INA3221 Register Block Diagram

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +3.3 V, VIN+ = 12 V, V_{SENSE} = (VIN+) – (VIN–) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

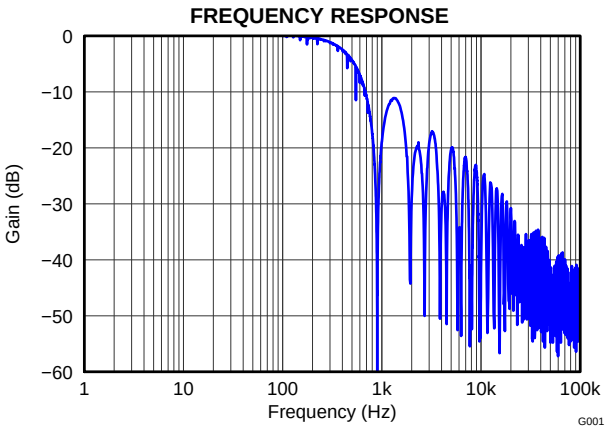


Figure 2.

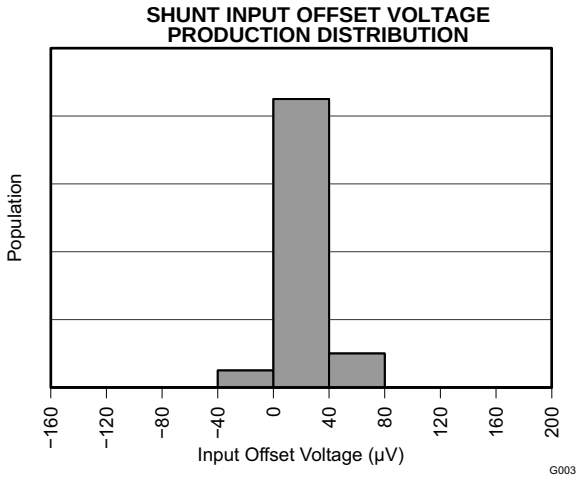
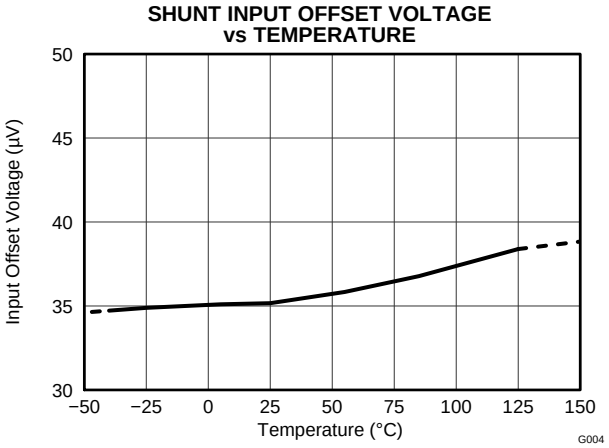


Figure 3.



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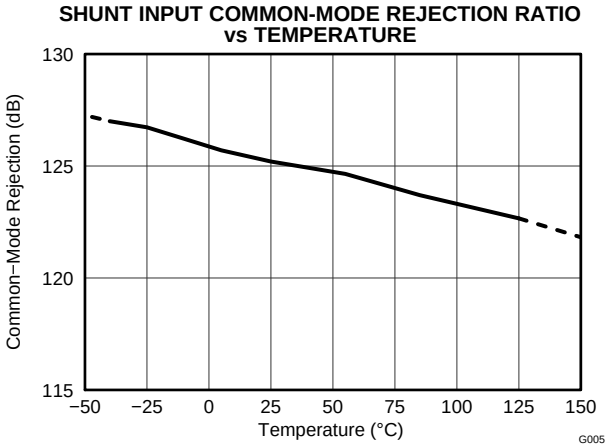
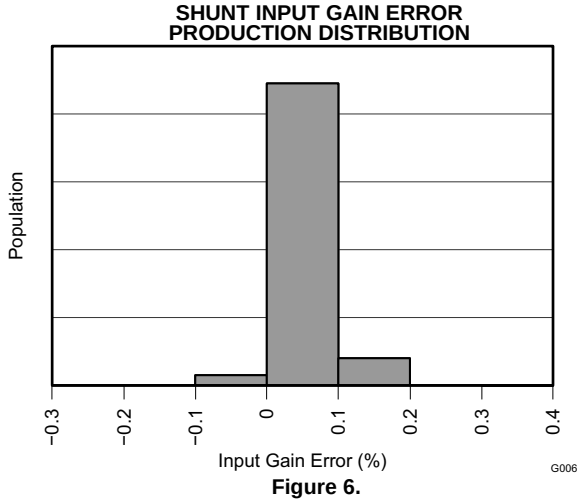


Figure 5.



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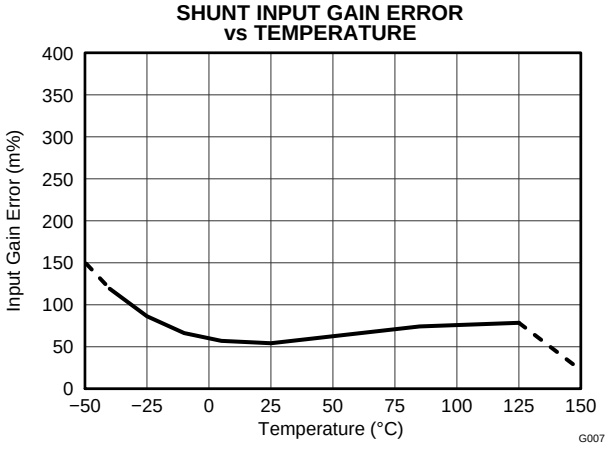

Figure 7.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, VIN+ = 12 V, V_{SENSE} = (VIN+) – (VIN–) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

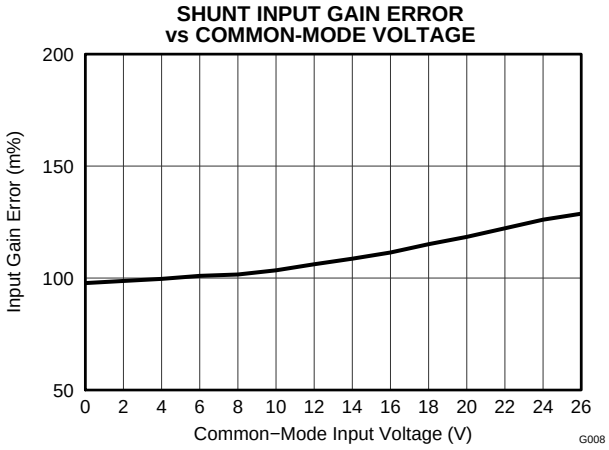


Figure 8.

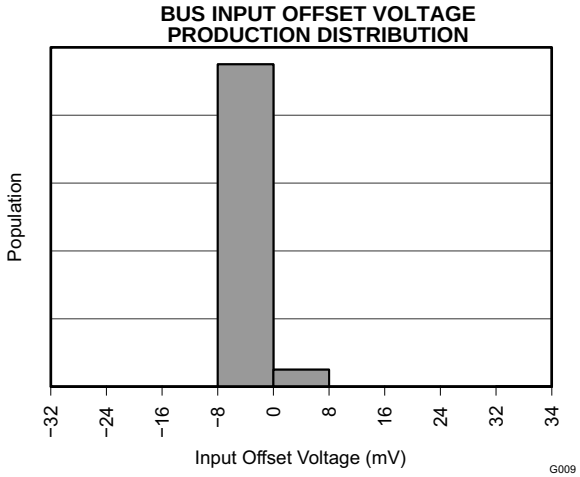


Figure 9.

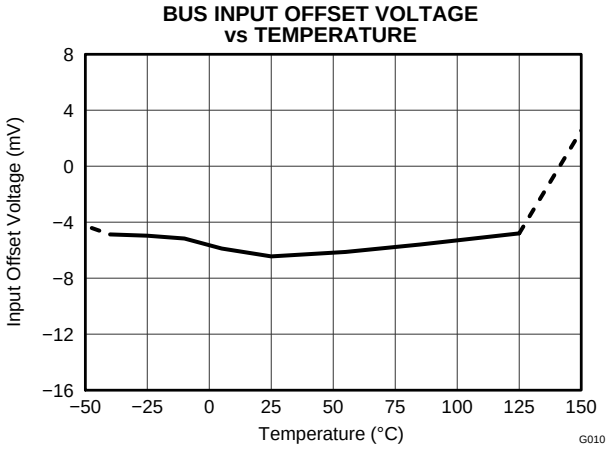
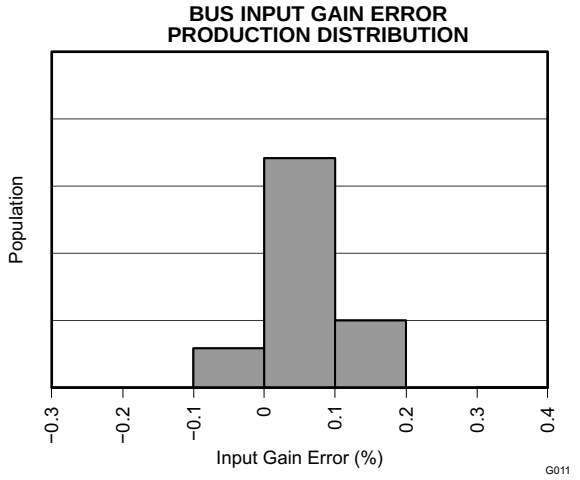


Figure 10.



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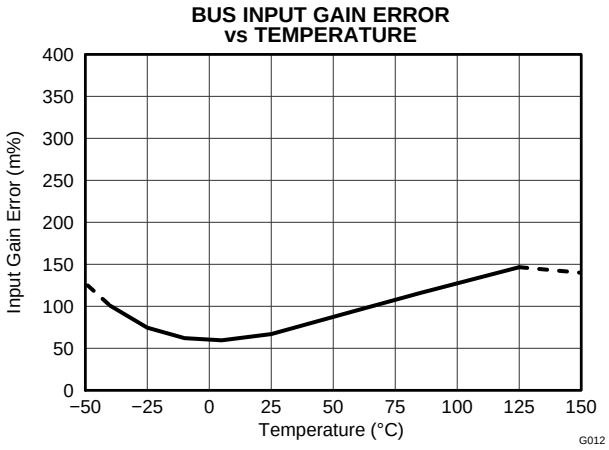

Figure 12.

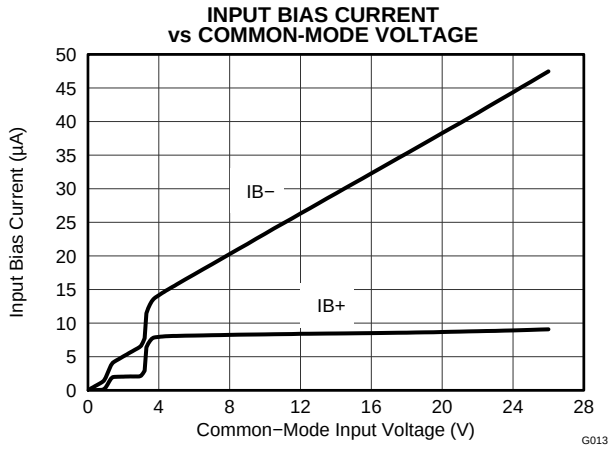

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, VIN+ = 12 V, V_{SENSE} = (VIN+) – (VIN–) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE

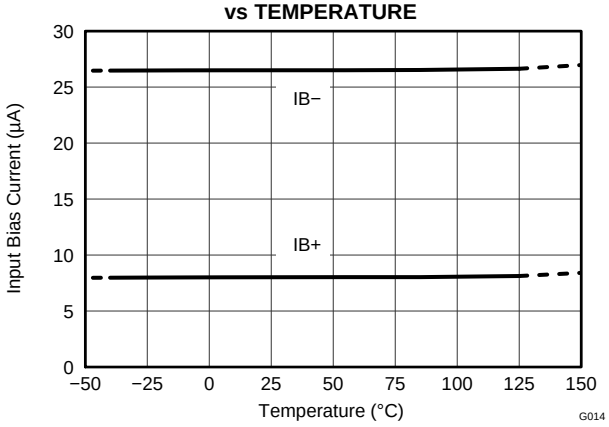

Figure 14.

INPUT BIAS CURRENT vs TEMPERATURE (Shutdown)

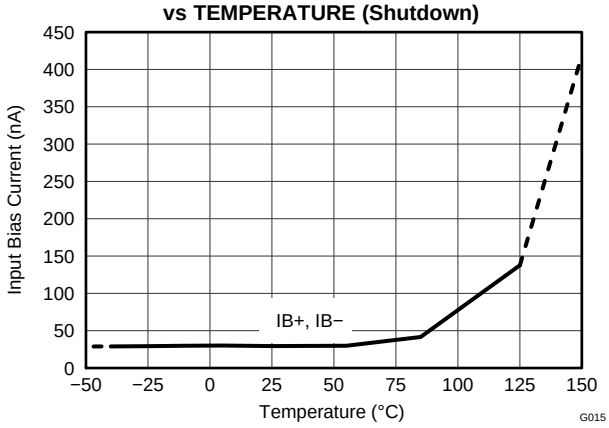

Figure 15.

ACTIVE I_Q vs TEMPERATURE

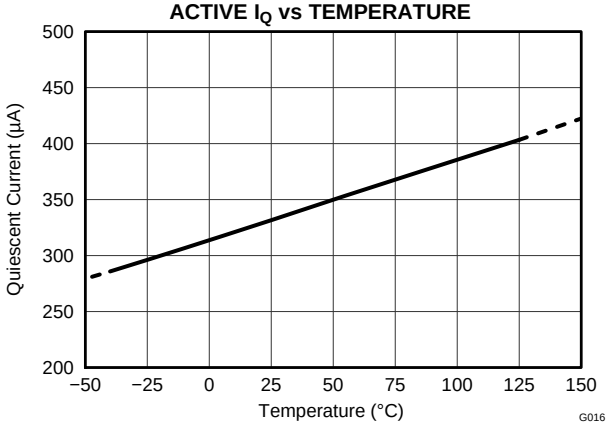

Figure 16.

SHUTDOWN I_Q vs TEMPERATURE

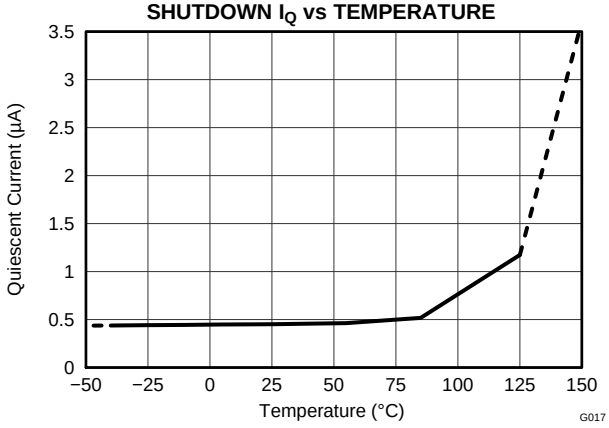

Figure 17.

ACTIVE I_Q vs I^2C CLOCK FREQUENCY

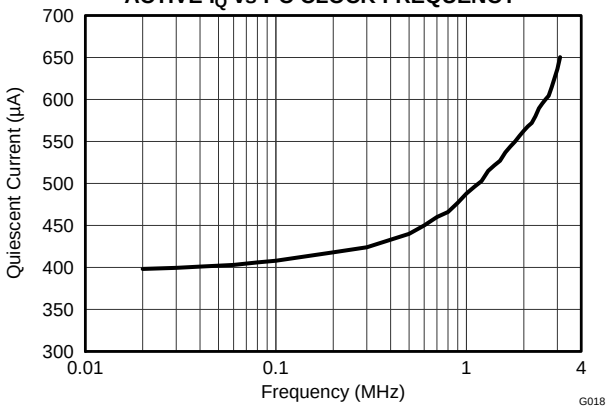

Figure 18.

SHUTDOWN I_Q vs I^2C CLOCK FREQUENCY

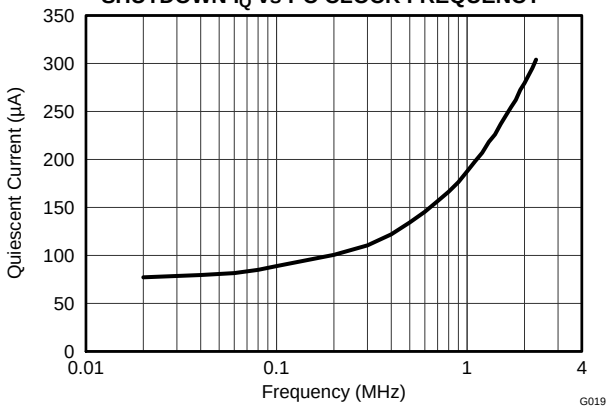

Figure 19.

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APPLICATION INFORMATION

The INA3221 is a current-shunt and bus voltage monitor that communicates over an I²C- and SMBus-compatible interface. The device provides digital shunt and bus voltage readings necessary for accurate decision making in precisely-controlled systems and also monitors multiple rails to ensure compliance voltages are maintained. Programmable registers offer flexible configuration for measurement precision and continuous versus single-shot operation. The *Register Information* section provides details of the INA3221 registers, beginning with Table 1. See Figure 1 for a register block diagram of the INA3221.

INA3221 TYPICAL APPLICATION

Figure 20 illustrates a typical INA3221 application circuit. Use a 0.1-µF ceramic capacitor for power-supply bypassing, placed as close as possible to the supply and ground pins.

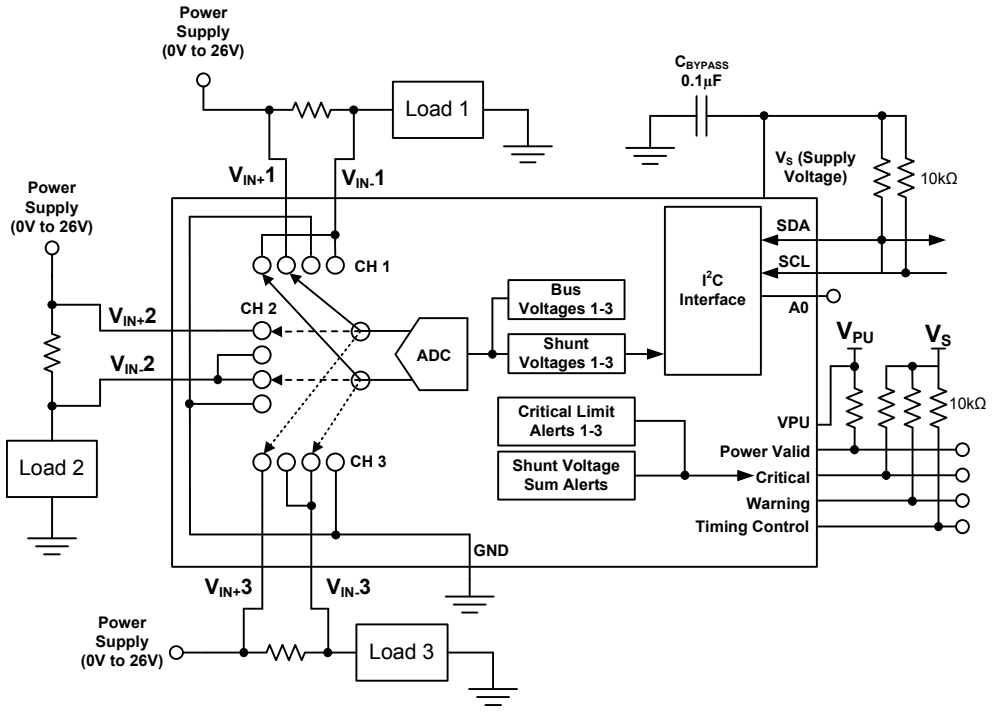

Figure 20. Typical Application Diagram

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BASIC ADC FUNCTIONS

The INA3221 performs two measurements on up to three power supplies of interest. The voltage developed from the load current passing through a shunt resistor creates a shunt voltage that is measured between the IN+ and IN– pins. The device also internally measures the power-supply bus voltage at the IN– pin for each channel. The differential shunt voltage is measured with respect to the VIN– pin while the bus voltage is measured, with respect to ground.

The INA3221 is typically powered by a separate power supply that ranges from 2.7 V to 5.5 V. The monitored supply buses range from 0 V to 26 V. **Note that, based on the fixed 8-mV bus voltage register LSB, a full-scale register value results in 32.76 V. However, the actual voltage applied to the INA3221 input pins should not exceed 26 V.** There are no special power-supply sequencing considerations between the common-mode input ranges and the device power-supply voltage because they are independent of each other; therefore, the bus voltages can be present with the supply voltage off and vice-versa.

As noted, the INA3221 takes two measurements for each channel. Each measurement can be independently or sequentially measured, based on the mode setting (bits[2:0] in the Configuration Register). When the INA3221 is in normal operating mode (that is, the MODE bits of the Configuration Register are set to '111'), the device continuously converts a shunt voltage reading followed by a bus voltage reading. This procedure converts one channel and then continues to the shunt voltage reading of the next enabled channel, followed by the channel bus voltage reading for that channel, and so on, until all enabled channels have been measured. The programmed Configuration Register mode setting applies to all channels. Any channels not enabled are bypassed in the measurement sequence, regardless of mode setting.

The INA3221 has two operating modes (continuous and single-shot) that determine the internal ADC operation after these conversions complete. When the INA3221 is set to continuous mode, based on the MODE bit settings, the device continues to cycle through all enabled channels until a new configuration setting is programmed.

The Configuration Register MODE control bits also enable modes to be selected that convert only the shunt or bus voltage. This feature further allows the monitoring function configuration to fit specific application requirements.

In single-shot modes, writing any single-shot convert modes to the Configuration Register (that is, the Configuration Register MODE bits set to ‘001’, ‘010’, or ‘011’) triggers a single-shot conversion. This action produces a single set of measurements for all enabled channels. To trigger another single-shot conversion, the Configuration Register must be written a second time, even if the mode does not change. When a single-shot conversion is initiated, all enabled channels are measured one time and then the device enters a power-down state. The INA3221 registers can be read at any time, even while in power-down. The data present in these registers are from the last completed conversion results for the corresponding register. The Conversion Ready Flag bit (Mask/Enable Register CVRF bit) can help coordinate single-shot conversions, which is especially helpful during longer conversion time settings. The CVRF bit is set after all conversions are complete. The CVRF bit clears under the following conditions:

1. Writing to the Configuration Register, except when configuring the MODE bits for power-down mode; or
2. Reading the Status Register.

In addition to the two operating modes (continuous and single-shot), the INA3221 also has a separate selectable power-down mode that reduces the quiescent current and turns off current into the INA3221 inputs, thus reducing the impact of supply drain when the device is not used. Full recovery from power-down mode requires 40 µs. The INA3221 registers can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active MODE settings are written to the Configuration Register.

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INA3221 AVERAGING FUNCTION

The INA3221 includes three channels to monitor up to three independent supply buses. Multichannel monitoring potentially results in poor shunt resistor placement. Ideally, the shunt resistors should be located as close as possible to the corresponding channel input pins. However, because of system layout and multiple power-supply rails, one or more shunt resistors may have to be located further away from the INA3221 than they otherwise ideally would be, thus presenting potentially larger measurement errors. These errors can result from additional trace inductance and other parasitic impedances between the shunt resistor and input pins. Longer traces also create an additional potential for coupling noise into the signal if they are routed near noise-generating sections of the board. The INA3221 averaging function mitigates this potential problem by limiting the impact any single measurement has on the averaged value of each measured signal. This limitation reduces the influence noise has on the averaged value, thereby effectively creating an input signal filter.

The averaging function is described in Figure 21. The INA3221 operation begins by first measuring the shunt input signal on channel 1. This value is then subtracted from the previous value that was present in the corresponding data output register. This difference is then divided by the value programmed by the Averaging Mode setting (Configuration Register bits[11:9]) and stored in an internal accumulation register. The computed result is then added to the previously-loaded data output register value and that resulting value is loaded to the corresponding data output register. After the update, the next signal to be measured follows the same process. The larger the value selected for the averaging mode setting, the less impact or influence any new conversion has on the average value, as shown in Figure 22. This averaging feature functions as a filter to reduce input noise from the averaged measurement value.

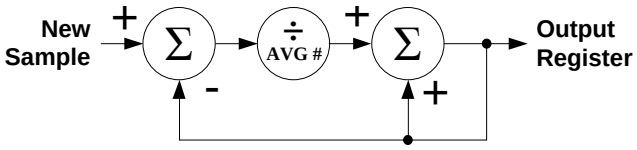

Figure 21. Averaging Function Block Diagram

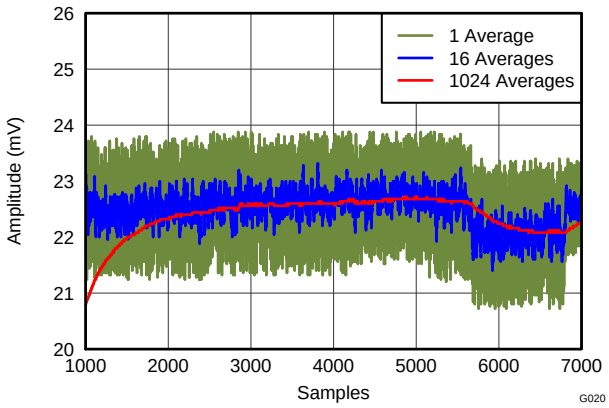

Figure 22. Average Setting Example

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MULTIPLE CHANNEL MONITORING

The INA3221 can be configured to monitor shunt and voltage measurements for up to three unique power-supply rails. This configuration allows for a total of six different signals to be measured. The INA3221 can be configured to adjust the number of channels and signals being measured through the Channel Enable and MODE bits in the Configuration Register. This adjustment allows the device to be optimized based on application requirements because the system is in use.

Channel Configuration

If an application requires that all three channels be monitored at power-up, but only one channel must be monitored after the system has stabilized, the other two channels can be disabled after power-up. This process allows the INA3221 to only monitor the power-supply rail of interest. Disabling unused channels helps improve system response time by more quickly returning to sampling the channel of interest. The INA3221 linearly monitors the enabled channels. This means that if all three channels are enabled for both shunt and bus voltage measurements, it takes five more completed conversions after a signal is measured before the device returns to that particular signal to begin another conversion. Changing the operating mode to monitor only the shunt voltage reduces this requirement to two conversions before the device begins a new conversion on a particular channel again.

There is also a timing aspect involved in reducing the signals being measured. The amount of time to complete an all-channel, shunt and bus voltage sequence is equal to the sum of the shunt voltage conversion time and the bus voltage conversion time (as programmed by the CT bits in the Configuration Register) multiplied by the three channels. The conversion times for the shunt and bus voltage measurements are programmed independently, however, the shunt and bus voltage conversion times selected apply to all channels.

Enabling a single channel with only one signal measured allows for that particular signal to be monitored solely. This setting enables the fastest response over time to changes in that specific input signal because there is no delay from the end of one conversion before the next conversion begins on that channel. Conversion time is not affected by enabling or disabling other channels. Selecting both the shunt and bus voltage settings as well as enabling additional channels extends the time from the end of one conversion on a signal before the beginning of the next conversion of that signal.

Averaging and Conversion Time Considerations

The INA3221 has programmable conversion times for both the shunt and bus voltage measurements. The conversion times for these measurements can be selected from 140 µs to 8.244 ms. The conversion time settings, along with the programmable averaging mode, enable the INA3221 to be configured to optimize available timing requirements in a given application. For example, if a system requires data to be read every 2 ms with all three channels monitored, the INA3221 can be configured with the conversion times for the shunt and bus voltage measurements set to 332 µs. The INA3221 can also be configured with a different conversion time setting for the shunt and bus voltage measurements. This approach is common in applications where the bus voltage tends to be relatively stable. This situation allows for the time focused on the bus voltage measurement to be reduced relative to the shunt voltage measurement. For example, the shunt voltage conversion time can be set to 4.156 ms with the bus voltage conversion time set to 588 µs for a 5-ms update time.

There are trade-offs associated with conversion time settings and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the INA3221 to reduce the amount of noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages allows the INA3221 to be more effective in reducing the measurement noise component. The trade-off to this noise reduction is that the averaged value has a longer response time to input signal changes. This aspect of the averaging feature is mitigated to some extent with the critical alert feature that compares each single conversion to determine if a measured signal (with its noise component) has exceeded the maximum acceptable level.

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The conversion times selected can also have an impact on measurement accuracy. This effect can seen in Figure 23. Multiple conversion times shown in Figure 23 illustrate the impact of noise on the measurement. These curves were taken without averaging used. In order to achieve the highest accuracy measurement possible, a combination of the longest allowable conversion times and highest number of averages should be used, based on system timing requirements.

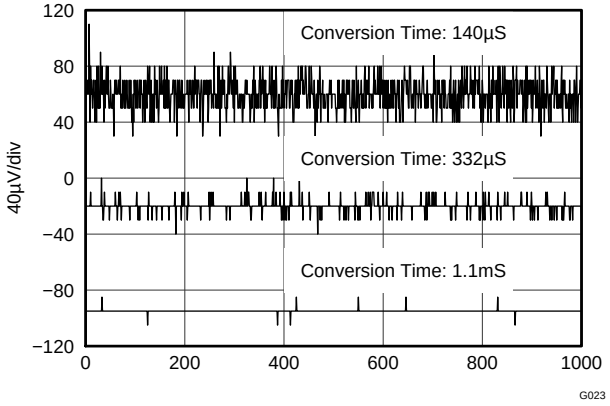

Figure 23. Noise versus Conversion Time

ALERT MONITORING

Because the INA3221 allows programmable thresholds that ensure the intended application operates within the desired operating conditions, multiple monitoring functions are available via four Alert pins: Critical Alert, Warning Alert, Power Valid Alert, and Timing Control Alert. These Alert pins are open-drain connections.

Critical Alert

The Critical Alert monitors functions based on individual conversions of each shunt voltage channel. The Critical Alert Limit feature compares the shunt voltage conversion for each channel to the corresponding value programmed into the corresponding limit register to determine if the measured value exceeds the intended limit. Exceeding the programmed limit indicates that the current through the shunt resistor is too high. The default Critical Alert Limit value for each channel is set to a positive full-scale value to effectively disable this alert at power-up. The corresponding limit registers can be programmed at any time to begin monitoring for out-of-range conditions. The Critical Alert pin is asserted and pulled low if any channel measurements exceed the limit present in the corresponding channel Critical Alert Limit. When the Critical Alert pin is asserted, the Mask/Enable Register can be read to determine which channel caused the Critical Flag Bit to assert.

The INA3221 also allows the Critical Alert pin to be controlled by the Summation Control function. The Summation Control function compares the sum of the single conversions of the desired channels based on the Summation Channel Control bits set in the Mask/Enable Register to determine if the combined sum has exceeded the programmed limit. In order for this summation limit to have a meaningful value, all included channels must use the same shunt resistor value. The individual conversion values cannot be added directly together in the Shunt Voltage Sum register to report the total current unless equal shunt resistor values are used for each channel. The Summation Channel Control bits either disable the Summation Control function or allow the Summation Control function to switch between including two or three channels in the Shunt Voltage Sum register. The Shunt Voltage Sum Limit register contains the programmed value used to compare the Shunt Voltage Sum register to determine if the total summed limit has been exceeded. If the Shunt Voltage Sum Limit value is exceeded, the Critical Alert pin is asserted low. Either the Summation Flag bit or the individual Critical Alert Limit bits in the Mask/Enable Register can determine the source of the alert when the Critical Alert pin asserts.

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Warning Alert

The Warning Alert monitors the averaged value of each shunt voltage channel. The averaged value of each shunt voltage channel is based on the number of averages set with the Average Mode bits in the Configuration Register. The average value is updated in the shunt voltage output register each time there is a conversion on the corresponding channel. The averaged value is compared to the value programmed in the corresponding channel Warning Alert Limit register to determine if the averaged value has been exceeded, which indicates if the average current is too high. The default Warning Alert Limit value for each channel is set to a positive full-scale value to effectively disable this alert at power-up. The corresponding limit registers can be programmed at any time to begin monitoring for out-of-range conditions. The Warning Alert pin is asserted and pulled low if any channel measurements exceed the limit present in the corresponding channel Warning Alert Limit. When the Warning Alert pin is asserted, the Mask/Enable Register can be read to determine which channel Warning Flag Bit is asserted.

Power Valid Alert

The Power Valid Alert verifies if all power rails are above the required levels. This feature allows the INA3221 to ensure power sequencing is properly managed and that the reported measurements are valid based on system configuration. The Power Valid mode starts at power-up to detect when all channels exceed a 10-V threshold. This 10-V level is the default value programmed into the Power Valid Upper Limit register. This value can be reprogrammed when the INA3221 is powered up to a valid supply voltage level of at least 2.7 V. When all three bus voltage measurements reach the programmed value loaded to the Power Valid Upper Limit register, the Power Valid Alert pin is pulled high. The Power Valid Alert powers up in a low state and is not pulled high until the Power Valid conditions are met, indicating all bus voltage rails are above the Power Valid Upper Limit value. This sequence is shown in Figure 24.

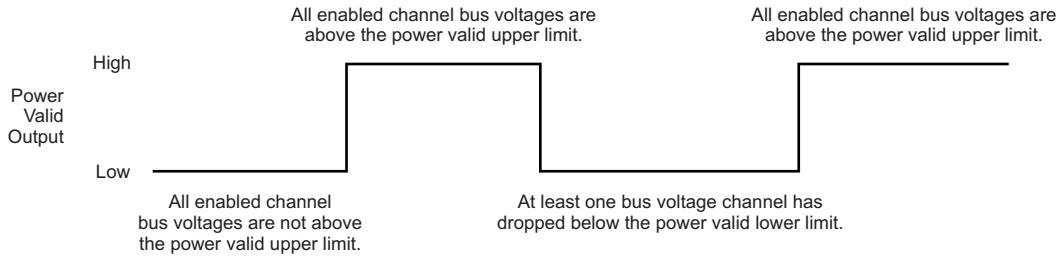

Figure 24. Power Valid State Diagram

When the Power Valid conditions are met and the Power Valid Alert pin is pulled high, the INA3221 switches to a mode that detects if any bus voltage measurements drop below 9 V. This 9-V level is the default value programmed into the Power Valid Lower Limit register. This value can also be reprogrammed when the INA3221 powers up to a supply voltage of at least 2.7 V. If any bus voltage measurement on the three channels drops below the Power Valid Lower Limit register, the Power Valid Alert pin goes low, indicating that the Power Valid condition is no longer met. At this point, the INA3221 switches back to a mode that identifies a Power Valid condition when all power rails again reach the Power Valid Upper Limit register values.

The Power Valid Alert function is based on the Power Valid conditions requirement that all three channels reach the intended Power Valid Upper Limit value. If all three channels are not used, the unused channel VIN– pin must be externally connected to one of the used channels in order to use the Power Valid Alert function. If the unused channel is not connected to a valid rail, the Power Valid Alert function cannot detect if all three channels reach the Power Valid level. The unused channel VIN+ pin should be left floating.

The Power Valid function also requires bus voltage measurements to be monitored. Bus voltage measurements must be enabled through one of the corresponding MODE settings set in the Configuration Register to be able to detect changes in the Power Valid state. The Single-Shot Bus Voltage mode can periodically cycle between the bus voltage measurements to ensure that the Power Valid conditions are met.

When all three bus voltage measurements are completed, the results are compared to the Power Valid threshold values to determine the Power Valid state. The bus voltage measurement values remain in the corresponding channel output registers until the bus voltage measurements are taken again, which updates the output registers. When the output registers are updated, the values are again compared to the Power Valid thresholds. Without taking periodic bus voltage measurements, the INA3221 is unable to determine if the Power Valid conditions are maintained.

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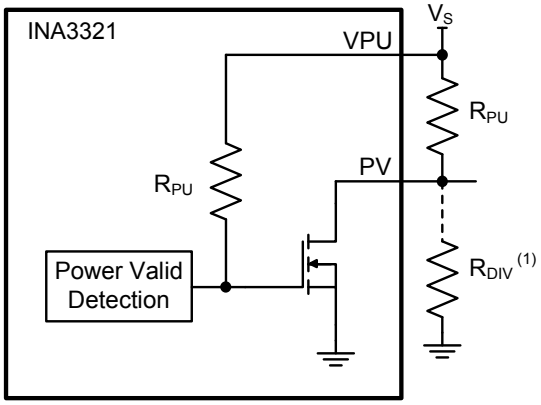
The Power Valid output pin allows for a 0-V output that indicates a power invalid condition. An output equal to the pull-up supply voltage connected to VPU indicates a power valid condition, as shown in Figure 25. It is also possible to divide down the High Power Valid pull-up voltage by adding a resistor to ground at the PV output, thus allowing this function to interface with lower-voltage circuitry if needed.



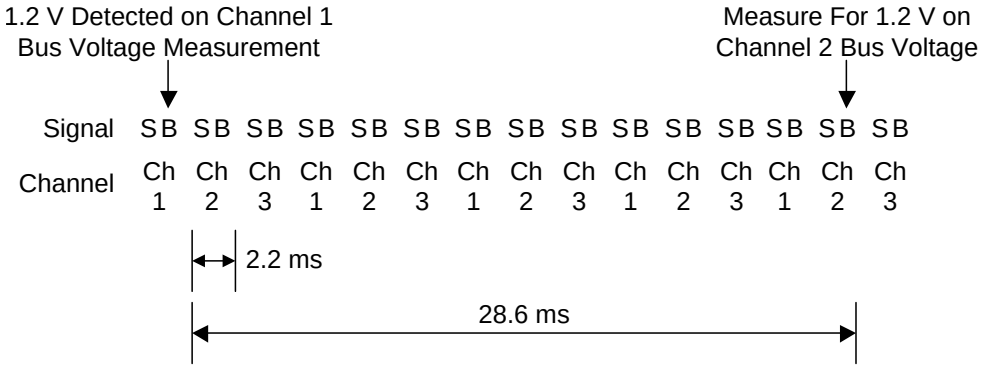
Note (1): R_{DIV} can be used to level shift High PV output.

(1) R_{DIV} can be used to level shift the PV output high.

Figure 25. Power Valid Output Structure

Timing Control Alert

The INA3221 has a Timing Control Alert function helps verify proper power-supply sequencing. On power-up, the default INA3221 setting is Continuous Shunt and Bus Voltage conversion mode. While in this mode at power-up, the INA3221 internally begins comparing the channel 1 bus voltage to determine when a 1.2-V level is reached. This comparison is made each time the sequence returns to the channel 1 bus voltage measurement. When a 1.2-V level is detected on the channel 1 bus voltage measurement, the INA3221 begins looking for a 1.2-V level present on the channel 2 bus voltage measurement. After a 1.2-V level is detected on channel 1, if the INA3221 does not detect a 1.2-V value or greater on the bus voltage measurement following four complete cycles of all three channels, the Timing Control Alert pin is asserted low to indicate that the INA3221 is has not detected a valid power rail on channel 2. This sequence allows for approximately 28.6 ms, as shown in Figure 26, from the time 1.2 V is detected on channel 1 for a valid voltage to be detected on channel 2. Figure 27 illustrates the state diagram for the Timing Control Alert pin.



NOTE: The signal refers to the corresponding shunt (S) and bus (B) voltage measurement for each channel.

Figure 26. Timing Control Timing Diagram

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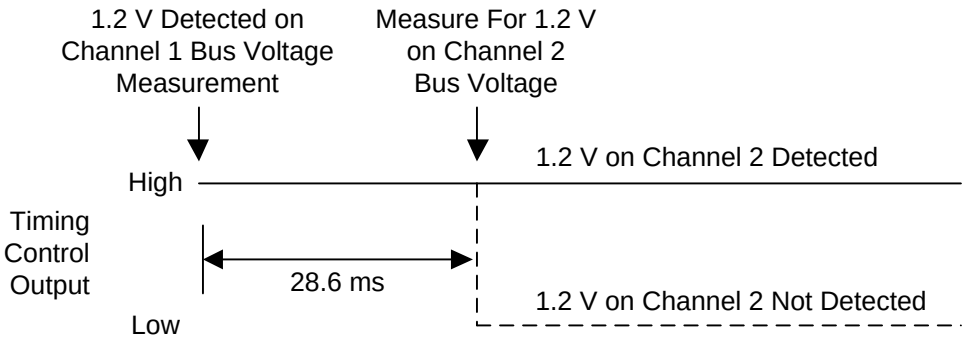

Figure 27. Timing Control State Diagram

The Timing Control Alert function is only monitored at power-up or when a software reset is issued by setting the RESET bit (bit 15) in the Configuration Register. The Timing Control Alert function timing is based on the default device settings at power-up. Writing to the Configuration Register before the Timing Control Alert function completes the full sequence results in disabling the Timing Control Alert until power is cycled or a software reset is issued.

FILTERING AND INPUT CONSIDERATIONS

Measuring current is often noisy, and such noise can be difficult to define. The INA3221 offers several filtering options by allowing conversion times and the number of averages to be selected independently in the Configuration Register. The conversion times can be set independently for the shunt and bus voltage measurements for added flexibility in configuring power-supply bus monitoring.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500-kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be managed by incorporating filtering at the INA3221 input. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. In general, filtering the INA3221 input is only necessary if there are transients at exact harmonics of the 500-kHz (±30%) sampling rate (greater than 1 MHz). Filter using the lowest possible series resistance (typically 10 Ω or less) and a ceramic capacitor. Recommended capacitor values are 0.1 µF to 1.0 µF. Figure 28 shows the INA3221 with an additional filter added at the input.

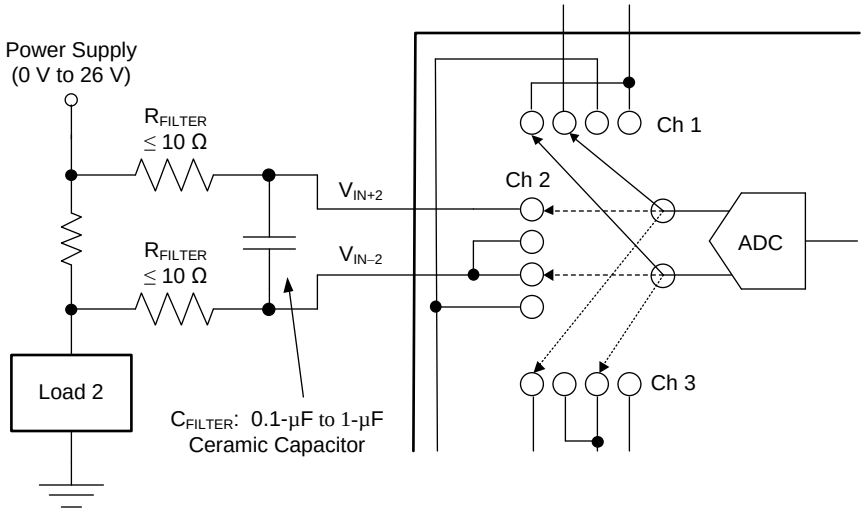

Figure 28. INA3221 with Input Filtering

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Overload conditions are another consideration for the INA3221 inputs. The INA3221 inputs are specified to tolerate 26 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long as the power supply or energy storage capacitors can support it). Keep in mind that removing a short to ground can result in inductive kickbacks that can exceed the 26-V differential and common-mode rating of the INA3221. Inductive kickback voltages are best controlled by zener-type transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy storage capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications without large electrolytics present. This problem occurs because an excessive dV/dt can activate the INA3221 ESD protection in systems where large currents are available. Testing has demonstrated that the addition of 10-Ω resistors in series with each INA3221 input sufficiently protects the inputs against this dV/dt failure up to the 26-V device rating. Selecting these resistors in the range noted has minimal effect on accuracy.

DEFAULT INA3221 SETTINGS

The default register power-up states are listed in the *Register Details* section. These registers are volatile, and if programmed to a value other than the default values shown in Table 1, they must be reprogrammed every time the device powers up.

Software Reset

The INA3321 features a software reset that can reinitialize the device and register settings to the default power-up values without having to cycle power to the device. Bit 15 (RESET) of the Configuration Register can be used to perform this software reset. Setting this bit reinitializes all registers and settings to the default power state with the exception of the Power Valid output state.

If a software reset is issued, the INA3221 holds the output of the Power Valid pin until the Power Valid detection sequence completes. The Power Valid Upper and Lower limit registers default to the default state when the software reset has been issued so any reprogrammed limit registers are reset, thus resulting in the original Power Valid thresholds validating the Power Valid conditions. This architecture ensures that circuitry connected to the Power Valid output is not interrupted during a software reset event.

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REGISTER INFORMATION

The INA3221 uses a bank of registers for holding configuration settings, measurement results, minimum and maximum limits, and status information. Table 1 summarizes the INA3221 registers; refer to Figure 1 for an illustration of the registers.

Table 1. Summary of Register Set

POINTER ADDRESS (Hex)	REGISTER NAME	DESCRIPTION	POWER-ON RESET		TYPE(1)
			BINARY	HEX	
0	Configuration Register	All-register reset, shunt and bus voltage ADC conversion times and averaging, operating mode.	01110001 00100111	7127	R/$\overline{W}$
1	Channel 1 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
2	Channel 1 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
3	Channel 2 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
4	Channel 2 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
5	Channel 3 Shunt Voltage	Averaged shunt voltage value.	00000000 00000000	0000	R
6	Channel 3 Bus Voltage	Averaged bus voltage value.	00000000 00000000	0000	R
7	Channel 1 Critical Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
8	Channel 1 Warning Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
9	Channel 2 Critical Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
A	Channel 2 Warning Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
B	Channel 3 Critical Limit	Contains limit value to compare each conversion value to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
C	Channel 3 Warning Limit	Contains limit value to compare to averaged measurement to determine if the corresponding limit has been exceeded.	01111111 11111000	7FF8	R/$\overline{W}$
D	Shunt Voltage Sum	Contains the summed value of the each of the selected shunt voltage conversions.	00000000 00000000	0000	R
E	Shunt Voltage Sum Limit	Contains limit value to compare to the Shunt Voltage Sum register to determine if the corresponding limit has been exceeded.	01111111 11111110	7FFE	R/$\overline{W}$
F	Mask/Enable	Alert configuration, alert status indication, summation control and status.	00000000 00000010	0002	R/$\overline{W}$
10	Power Valid Upper Limit	Contains limit value to compare all bus voltage conversions to determine if the Power Valid level has been reached.	00100111 00010000	2710	R/$\overline{W}$
11	Power Valid Lower Limit	Contains limit value to compare all bus voltage conversions to determine if the any voltage rail has dropped below the Power Valid range.	00100011 00101000	2328	R/$\overline{W}$
FE	Manufacturer ID	Contains unique manufacturer identification number.	01010100 01001001	5449	R
FF	Die ID	Contains unique die identification number.	00110010 00100000	3220	R

(1) Type: R = read-only, R/$\overline{W}$ = read/write.

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REGISTER DETAILS

All 16-bit INA3221 registers are two 8-bit bytes via the I^2C interface. Table 2 shows a register map for the INA3221.

Table 2. Register Map

REGISTER	ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	00	RST	$CH1_{en}$	$CH2_{en}$	$CH3_{en}$	AVG2	AVG1	AVG0	$V_{BUS}CT2$	$V_{BUS}CT1$	$V_{BUS}CT0$	$V_{SH}CT2$	$V_{SH}CT1$	$V_{SH}CT0$	MODE3	MODE2	MODE1
Channel 1 Shunt Voltage	01	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
Channel 1 Bus Voltage	02	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
Channel 2 Shunt Voltage	03	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
Channel 2 Bus Voltage	04	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
Channel 3 Shunt Voltage	05	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
Channel 3 Bus Voltage	06	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
Critical Alert Channel 1 Limit	07	C1L12	C1L11	C1L10	C1L9	C1L8	C1L7	C1L6	C1L5	C1L4	C1L3	C1L2	C1L1	C1L0	—	—	—
Warning Alert Channel 1 Limit	08	W1L12	W1L11	W1L10	W1L9	W1L8	W1L7	W1L6	W1L5	W1L4	W1L3	W1L2	W1L1	W1L0	—	—	—
Critical Alert Channel 2 Limit	09	C2L12	C2L11	C2L10	C2L9	C2L8	C2L7	C2L6	C2L5	C2L4	C2L3	C2L2	C2L1	C2L0	—	—	—
Warning Alert Channel 2 Limit	0A	W2L12	W2L11	W2L10	W2L9	W2L8	W2L7	W2L6	W2L5	W2L4	W2L3	W2L2	W2L1	W2L0	—	—	—
Critical Alert Channel 3 Limit	0B	C3L12	C3L11	C3L10	C3L9	C3L8	C3L7	C3L6	C3L5	C3L4	C3L3	C3L2	C3L1	C3L0	—	—	—
Warning Alert Channel 3 Limit	0C	W3L12	W3L11	W3L10	W3L9	W3L8	W3L7	W3L6	W3L5	W3L4	W3L3	W3L2	W3L1	W3L0	—	—	—
Shunt Voltage Sum	0D	SIGN	SV13	SV12	SV11	SV10	SV9	SV8	SV7	SV6	SV5	SV4	SV3	SV2	SV1	SV0	—
Shunt Voltage Sum Limit	0E	SIGN	SVL13	SVL12	SVL11	SVL10	SVL9	SVL8	SVL7	SVL6	SVL5	SVL4	SVL3	SVL2	SVL1	SVL0	—
Mask/Enable	0F	—	SCC1	SCC2	SCC3	WEN	CEN	CF1	CF2	CF3	SF	WF1	WF2	WF3	PVF	TCF	CVRF
Power Valid Upper Limit	10	PVU12	PVU11	PVU10	PVU9	PVU8	PVU7	PVU6	PVU5	PVU4	PVU3	PVU2	PVU1	PVU0	—	—	—
Power Valid Lower Limit	11	PVL12	PVL11	PVL10	PVL9	PVL8	PVL7	PVL6	PVL5	PVL4	PVL3	PVL2	PVL1	PVL0	—	—	—
Manufacturer ID	FE	0	1	0	1	0	1	0	0	0	1	0	0	1	0	0	1
Die ID Register	FF	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0

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Configuration Register (Address = 00h, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	RST	$CH1_{en}$	$CH2_{en}$	$CH3_{en}$	AVG2	AVG1	AVG0	$V_{BUS}CT2$	$V_{BUS}CT1$	$V_{BUS}CT0$	$V_{SH}CT2$	$V_{SH}CT1$	$V_{SH}CT0$	MODE3	MODE2	MODE1
POR VALUE	0	1	1	1	0	0	0	1	0	0	1	0	0	1	1	1

Bit 15 **RST: Reset bit**

Setting this bit to '1' generates a system reset that is the same as a power-on reset (POR). This bit resets all registers to default values and self-clears.

Bits[14:12] **CHEN: Channel enable mode**

The channel enable mode bits allow each channel to be independently enabled or disabled.
0 = Channel disable
1 = Channel enable (default)

Bits[11:9] **AVG: Averaging mode**

Sets the number of samples that are collected and averaged together.
Table 3 summarizes the AVG bit settings and related number of averages for each bit.

Table 3. AVG Bit Settings, Bits[11:9]

AVG2 D11	AVG1 D10	AVG0 D9	NUMBER OF AVERAGES
0 (default)	0 (default)	0 (default)	1 (default)
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

Bits[8:6] **V_{BUS} CT: Bus voltage conversion time**

Sets the conversion time for the bus voltage measurement.
Table 4 shows the V_{BUS} CT bit options and related conversion times for each bit.

Table 4. V_{BUS} CT Bit Settings, Bits[8:6]

V_{BUS} CT2 D8	V_{BUS} CT1 D7	V_{BUS} CT0 D6	CONVERSION TIME
0	0	0	140 µs
0	0	1	204 µs
0	1	0	332 µs
0	1	1	588 µs
1 (default)	0 (default)	0 (default)	1.1 ms (default)
1	0	1	2.116 ms
1	1	0	4.156 ms
1	1	1	8.244 ms

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Bits[5:3] **V_{SH} CT: Shunt voltage conversion time**

Sets the conversion time for the shunt voltage measurement.
Table 5 shows the V_{SH} CT bit options and related conversion times for each bit.

Table 5. V_{SH} CT Bit Settings, Bits[5:3]

V_{SH} CT2 D5	V_{SH} CT1 D4	V_{SH} CT0 D3	CONVERSION TIME
0	0	0	140 µs
0	0	1	204 µs
0	1	0	332 µs
0	1	1	588 µs
1 (default)	0 (default)	0 (default)	1.1 ms (default)
1	0	1	2.116 ms
1	1	0	4.156 ms
1	1	1	8.244 ms

Bits[2:0] **MODE: Operating mode**

Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode.
The mode settings are shown in Table 6.

Table 6. Mode Settings, Bits[2:0]

MODE3 D2	MODE2 D1	MODE1 D0	MODE
0	0	0	Power-down
0	0	1	Shunt voltage, triggered
0	1	0	Bus voltage, triggered
0	1	1	Shunt and bus, triggered
1	0	0	Power-down
1	0	1	Shunt voltage, continuous
1	1	0	Bus voltage, continuous
1 (default)	1 (default)	1 (default)	Shunt and bus, continuous (default)

The Configuration Register settings control the operating modes for the shunt and bus voltage measurements for the three input channels. This register controls the conversion time settings for both the shunt and bus voltage measurements and the averaging mode used. The Configuration Register can be used to independently enable or disable each channel as well as select the operating mode that controls which signals are selected to be measured.

This register can be read from at any time without impacting or affecting either device settings or conversions in progress. Writing to this register halts any conversion in progress until the write sequence is completed, resulting in a new conversion starting based on the new Configuration Register contents. This architecture prevents any uncertainty in the conditions used for the next completed conversion.

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Channel 1 Shunt Voltage Register (Address = 01h, Read-Only)

Full-scale range = 163.8 mV (decimal = 7FF8); LSB (SD0): 40 µV. This register contains the averaged shunt voltage measurement for channel 1.

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register stores the current shunt voltage reading, V_{SHUNT}, for channel 1. Negative numbers are represented in twos complement format. Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting MSB = 1.

Example: For a value of V_{SHUNT} = –80 mV:

1. Take the absolute value: 80 mV
2. Translate this number to a whole decimal number (80 mV / 40 µV) = 2000
3. Convert this number to binary = 011 1110 1000 0--- (non-used bits are '0')
4. Complement the binary result = 100 0001 0111 1111
5. Add '1' to the complement to create the twos complement result = 100 0001 1000 0000
6. Extend the sign and create the 16-bit word: 1100 0001 1000 0000 = C180h

Channel 1 Bus Voltage Register (Address = 02h, Read-Only)(1)

Full-scale range = 32.76 V(1) (decimal = 7FF8); LSB (BD0) = 8 mV.

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) While the input range is 26 V, the full-scale range of the ADC scaling is 32.76 V. Do not apply more than 26 V.

This register stores the bus voltage reading, V_{BUS}, for channel 1.

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Channel 2 Shunt Voltage Register (Address = 03h, Read-Only)

Full-scale range = 163.8 mV (decimal = 7FF8); LSB (SD0): 40 µV. This register contains the averaged shunt voltage measurement for channel 2.

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register stores the current shunt voltage reading, V_{SHUNT}, for channel 2.

Channel 2 Bus Voltage Register (Address = 04h, Read-Only)(1)

Full-scale range = 32.76 V (1) (decimal = 7FF8); LSB (BD0) = 8 mV.

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) While the input range is 26 V, the full-scale range of the ADC scaling is 32.76 V. Do not apply more than 26 V.

This register stores the bus voltage reading, V_{BUS}, for channel 2.

Channel 3 Shunt Voltage Register (Address = 05h, Read-Only)

Full-scale range = 163.8 mV (decimal = 7FF8); LSB (SD0): 40 µV. This register contains the averaged shunt voltage measurement for channel 3.

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register stores the current shunt voltage reading, V_{SHUNT}, for channel 3.

Channel 3 Bus Voltage Register (Address = 06h, Read-Only)(1)

Full-scale range = 32.76 V(1) (decimal = 7FF8); LSB (BD0) = 8 mV.

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	—	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) While the input range is 26 V, the full-scale range of the ADC scaling is 32.76 V. Do not apply more than 26 V.

This register stores the bus voltage reading, V_{BUS}, for channel 3.

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Critical Alert Channel 1 Limit Register (Address = 07h, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C1L12	C1L11	C1L10	C1L9	C1L8	C1L7	C1L6	C1L5	C1L4	C1L3	C1L2	C1L1	C1L0	—	—	—
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

This register contains the value used to compare to each shunt voltage conversion on channel 1 to detect fast overcurrent events.

Warning Alert Channel 1 Limit Register (Address = 08h, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	W1L12	W1L11	W1L10	W1L9	W1L8	W1L7	W1L6	W1L5	W1L4	W1L3	W1L2	W1L1	W1L0	—	—	—
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

This register contains the value used to compare to the averaged shunt voltage value of channel 1 to detect a longer duration overcurrent event.

Critical Alert Channel 2 Limit Register (Address = 09h, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C2L12	C2L11	C2L10	C2L9	C2L8	C2L7	C2L6	C2L5	C2L4	C2L3	C2L2	C2L1	C2L0	—	—	—
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

This register contains the value used to compare to each shunt voltage conversion on channel 2 to detect fast overcurrent events.

Warning Alert Channel 2 Limit Register (Address = 0Ah, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	W2L12	W2L11	W2L10	W2L9	W2L8	W2L7	W2L6	W2L5	W2L4	W2L3	W2L2	W2L1	W2L0	—	—	—
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

This register contains the value used to compare to the averaged shunt voltage value of channel 2 to detect a longer duration overcurrent event.

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Critical Alert Channel 3 Limit Register (Address = 0Bh, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	C3L12	C3L11	C3L10	C3L9	C3L8	C3L7	C3L6	C3L5	C3L4	C3L3	C3L2	C3L1	C3L0	—	—	—
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

This register contains the value used to compare to each shunt voltage conversion on channel 3 to detect fast overcurrent events.

Warning Alert Channel 3 Limit Register (Address = 0Ch, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	W3L12	W3L11	W3L10	W3L9	W3L8	W3L7	W3L6	W3L5	W3L4	W3L3	W3L2	W3L1	W3L0	—	—	—
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

This register contains the value used to compare to the averaged shunt voltage value of channel 3 to detect a longer duration overcurrent event.

Shunt Voltage Sum Register (Address = 0Dh, Read-Only)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	SV13	SV12	SV11	SV10	SV9	SV8	SV7	SV6	SV5	SV4	SV3	SV2	SV1	SV0	—
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register contains the sum of the single conversion shunt voltages of the selected channels based on the summation control bits 12, 13, and 14 in the Mask/Enable Register.

This register is updated with the most recent sum following each complete cycle of all selected channels. The Shunt Voltage Sum Register LSB value is 40 µV.

Shunt Voltage Sum Limit Register (Address = 0Eh, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	SVL13	SVL12	SVL11	SVL10	SVL9	SVL8	SVL7	SVL6	SVL5	SVL4	SVL3	SVL2	SVL1	SVL0	—
POR VALUE	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

This register contains the value used to compare the Shunt Voltage following each completed cycle of all selected channels to detect for system overcurrent events. The Shunt Voltage Sum Limit Register LSB value is 40 µV.

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Mask/Enable Register (Address = 0Fh, Read/Write)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	—	SCC1	SCC2	SCC3	WEN	CEN	CF1	CF2	CF3	SF	WF1	WF2	WF3	PVF	TCF	CVRF
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits[14:12] **SCC: Summation Channel Control**

These bits determine which shunt voltage measurement channels are enabled to fill the Shunt Voltage Sum register. The selection of these bits does not impact the individual channel enable or disable status or the corresponding channel measurements. The corresponding bit is used to select if the channel is used to fill the Shunt Voltage Sum Register.
0 = Disabled (default)
1 = Enabled

Bit 11 **WEN: Warning Alert Latch Enable configures the latching feature of the Warning Alert pin.**

0 = Transparent (default)
1 = Latch enabled

Bit 10 **CEN: Critical Alert Latch Enable configures the latching feature of the Critical Alert pin.**

0 = Transparent (default)
1 = Latch enabled

Bits[9:7] **CF: Critical Alert Flag Indicator**

These bits are asserted if the corresponding channel measurement has exceeded the Critical Alert limit resulting in the Critical Alert pin being asserted. These bits can be read back to determine which channel caused the Critical Alert. The Critical Alert Flag bits are cleared when the Mask/Enable Register is read back.

Bit 6 **SF: Summation Alert Flag Indicator**

This bit is asserted if the Shunt Voltage Sum register exceeds the Shunt Voltage Sum Limit register. If the Summation Alert Flag is asserted, the Critical Alert pin is also asserted. The Summation Alert Flag bit is cleared when the Mask/Enable Register is read back.

Bits[5:3] **WF: Warning Alert Flag Indicator**

These bits are asserted if the corresponding channel's averaged measurement has exceeded the Warning Alert limit resulting in the Warning Alert pin being asserted. These bits can be read back to determine which channel caused the Warning Alert. The Warning Alert Flag bits clear when the Mask/Enable Register is read back.

Bit 2 **PVF: Power Valid Alert Flag Indicator**

This bit can be used to be able to determine if the Power Valid Alert pin has been asserted through software rather than hardware. The bit setting corresponds to the status of the Power Valid Alert pin. This bit does not clear until the condition that caused the alert is removed and the Power Valid Alert pin has cleared.

Bit 1 **TCF: Timing Control Alert Flag Indicator**

This bit can be used to be able to determine if the Timing Control Alert pin has been asserted through software rather than hardware. The bit setting corresponds to the status of the Timing Control Alert pin. This bit does not clear once it has been asserted unless the power is recycled or a software reset is issued. The default state for the Timing Control Alert Flag is High.

Bit 0 **CVRF: Conversion Ready Flag**

Although the INA3221 can be read at any time, and the data from the last conversion is available, the Conversion Ready bit is provided to help coordinate single-shot conversions. The Conversion bit is set after all conversions are complete. Conversion Ready clears under the following conditions:

- Writing the Configuration Register (except for power-down or disable mode selections).
- Reading the Mask/Enable Register.

This register selects which function is enabled to control the Critical Alert and Warning Alert pins and how each Warning Alert responds to the corresponding channel. Reading the Mask/Enable Register clears any flag results present. Writing to this register does not clear the flag bit status. To ensure that there is no uncertainty in the warning function setting that resulted in a flag bit being set, the Mask/Enable Register should be read from to clear the flag bit status before changing the warning function setting.

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Power Valid Upper Limit Register (Address = 10h, Read/Write)(1)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	PVU11	PVU10	PVU9	PVU8	PVU7	PVU6	PVU5	PVU4	PVU3	PVU2	PVU1	PVU0	—	—	—
POR VALUE	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0

(1) Power-on reset value is 2710h (10.000 V)

This register contains the value used to determine if the Power Valid conditions are met. The Power Valid condition is reached when all bus voltage channels exceed the value set in this limit register. When the Power Valid condition is met, the Power Valid Alert pin asserts high to indicate that the INA3221 has confirmed all bus voltage channels are above the Power Valid Upper Limit value. In order for the Power Valid conditions to be monitored, the bus measurements must be enabled through one of the corresponding MODE settings set in the Configuration Register. The Power Valid Upper Limit LSB value is 8 mV.

Power Valid Lower Limit Register (Address = 11h, Read/Write)(1)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	SIGN	PVL11	PVL10	PVL9	PVL8	PVL7	PVL6	PVL5	PVL4	PVL3	PVL2	PVL1	PVL0	—	—	—
POR VALUE	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	0

(1) Power-on reset value is 2328h (9.000 V)

This register contains the value used to determine if any of the bus voltage channels drops below the Power Valid Lower Limit when the Power Valid conditions are met. This limit contains the value used to compare all bus channel readings to ensure that all channels remain above the Power Valid Lower Limit, thus ensuring the Power Valid condition is maintained. If any bus voltage channel drops below the Power Valid Lower Limit, the Power Valid Alert pin is pulled low to indicate that the INA3221 detects a bus voltage reading below the Power Valid Lower Limit. In order for the Power Valid condition to be monitored, the bus measurements must be enabled through one of the corresponding MODE settings set in the Configuration Register. The Power Valid Lower Limit LSB value is 8 mV.

Manufacturer ID Register (Address = FEh, Read)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	0	1	0	1	0	1	0	0	0	1	0	0	1	0	0	1

This register contains a factory-programmable identification value that identifies this device as being manufactured by Texas Instruments. This register distinguishes this device from other devices that are on the same I^2C bus. The contents of this register are 5449h, or TI in Ascii.

Die ID Register (Address = FFh, Read)

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0

This register contains a factory-programmable identification value that identifies this device as an INA3221. This register distinguishes this device from other devices that are on the same I^2C bus. The Die ID for the INA3221 is 3220h.

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BUS OVERVIEW

The INA3221 offers compatibility with both I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with one another.

The I^2C interface is used throughout this data sheet as the primary example, with the SMBus protocol specified only when a difference between the two systems is discussed. Two bidirectional lines, the serial clock (SCL) and data signal line (SDA), connect the INA3221 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by the master device that generates the SCL, controls the bus access, and generates start and stop conditions.

To address a specific device, the master initiates a start condition by pulling SDA from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an *Acknowledge* bit and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

Once all data are transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The INA3221 includes a 28-ms timeout on the interface to prevent locking up the bus.

Serial Bus Address

To communicate with the INA3221, the master must first address slave devices with a slave address byte. This byte consists of seven address bits and a direction bit to indicate whether the intended action is a read or write operation.

The INA3221 has one address pin, A0. Table 7 describes the pin logic levels for each of the four possible addresses. The state of the A0 pin is sampled on every bus communication and should be set before any activity on the interface occurs.

Table 7. INA3221 Address Pins and Slave Addresses

A0	SLAVE ADDRESS
GND	1000000
V_{S+}	1000001
SDA	1000010
SCL	1000011

Serial Interface

The INA3221 only operates as a slave device on the I^2C bus and SMBus. Bus connections are made via the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. While there is spike suppression integrated into the digital I/O lines, proper layout should be used to minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitively coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielding communication lines in general is recommended to reduce the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The INA3221 supports a transmission protocol for Fast (1 kHz to 400 kHz) and High-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted MSB first.

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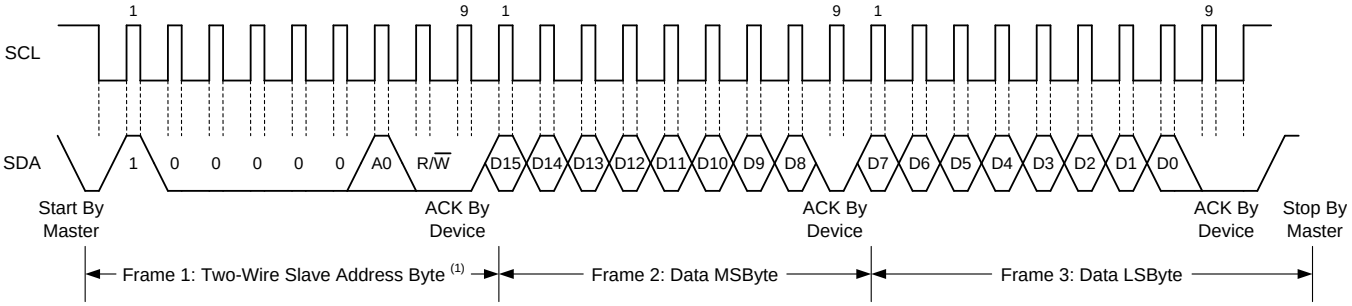
WRITING TO AND READING FROM THE INA3221

Accessing a specific INA3221 register is accomplished by writing the appropriate value to the register pointer. Refer to Table 1 for a complete list of registers and corresponding addresses. The value for the register pointer (refer to Figure 32) is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the INA3221 requires a register pointer value.

Register writes begin with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit low. The INA3221 then acknowledges receipt of a valid address. The next byte transmitted by the master is the register address that data are written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The INA3221 acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

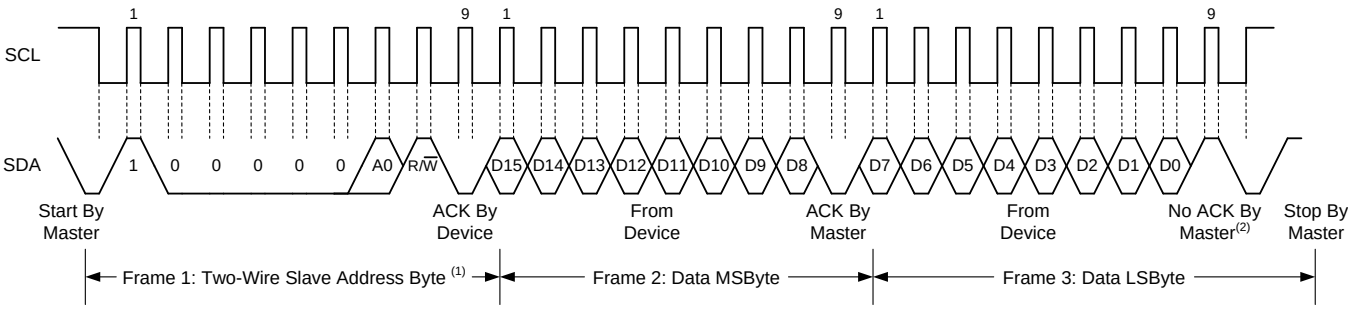
When reading from the INA3221, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the INA3221 retains the register pointer value until it is changed by the next write operation.

Figure 29 and Figure 30 show the write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the Slave Address byte is determined by the A0 pin setting. Refer to Table 7.

Figure 29. Timing Diagram for Write Word Format



(1) The value of the Slave Address byte is determined by the A0 pin setting. Refer to Table 7.

(2) Read data are from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 23.

(3) An ACK by the master can also be sent.

Figure 30. Timing Diagram for Read Word Format

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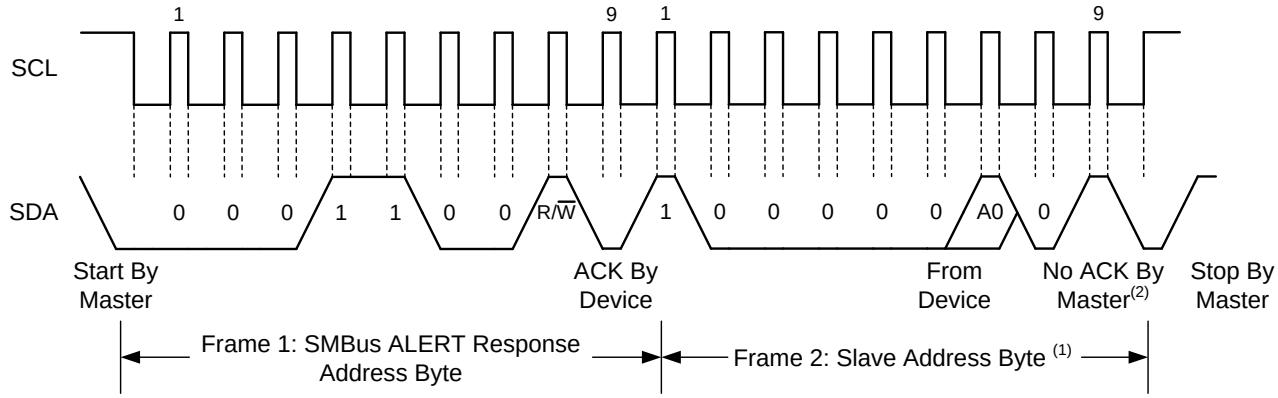
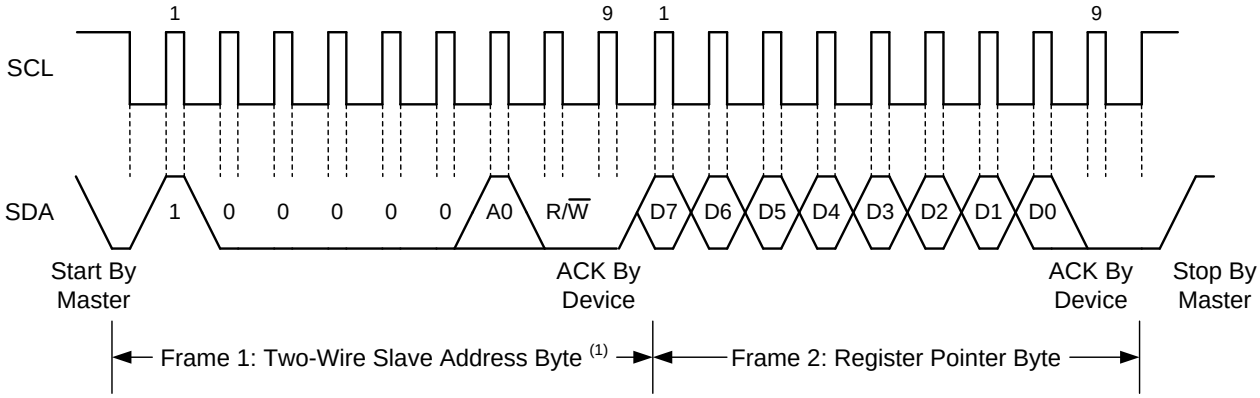
Figure 31 shows the timing diagram for the SMBus Alert response operation. Figure 32 illustrates a typical register pointer configuration.



(1) The value of the Slave Address Byte is determined by the A0 pin setting. Refer to Table 7.

Figure 31. Timing Diagram for SMBus ALERT



(1) The value of the Slave Address Byte is determined by the A0 pin setting. Refer to Table 7.

Figure 32. Typical Register Pointer Set

High-Speed I²C Mode

When the bus is idle, the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte with the High-Speed (HS) master code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The INA3221 does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4-MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 MHz are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all internal INA3221 filters to support F/S mode.

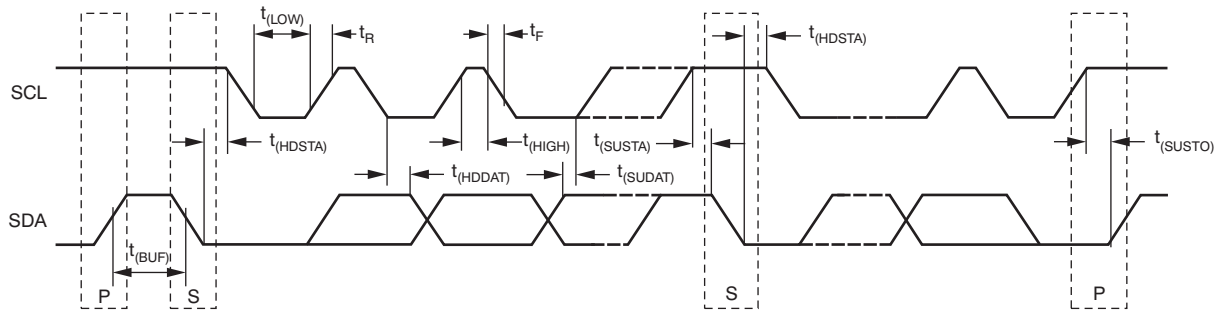


Figure 33. Bus Timing Diagram

Bus Timing Diagram Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	3.4	MHz
$t_{(BUF)}$	Bus free time between stop and start conditions	600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	100		100		ns
$t_{(SUSTA)}$	Repeated start condition setup time	100		100		ns
$t_{(SUSTO)}$	STOP condition setup time	100		100		ns
$t_{(HDDAT)}$	Data hold time	0		0		ns
$t_{(SUDAT)}$	Data setup time	100		10		ns
$t_{(LOW)}$	SCL clock low period	1300		160		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
t_F	Clock and data fall time		300		160	ns
t_R	Clock and data rise time		300		160	ns
	Clock and data rise time for SCLK ≤ 100 kHz		1000			ns

SMBus ALERT RESPONSE

The INA3221 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple slave devices. When an Alert occurs, the master can broadcast the Alert Response slave address (0001 100) with the R/$\overline{W}$ bit set high. Following this Alert Response, any slave devices that generated an alert identify themselves by acknowledging the Alert Response and sending their respective address on the bus.

The Alert Response can activate several different slave devices simultaneously, similar to the I²C General Call. If more than one slave attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until the interrupt is cleared.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2012) to Revision A **Page**

- Changed Input, *Voltage input range, Shunt* parameter specifications in +3.3 V Electrical Characteristics table 3
- Updated Figure 24 15
- Changed bit D15 in Power Valid Upper Limit Register 28
- Changed bit D15 in Power Valid Lower Limit Register 28
- Changed second paragraph of *Serial Bus Address* section 29
- Updated Figure 29 and Figure 30 30
- Changed footnote 1 in Figure 29 and Figure 30 30
- Updated Figure 31 and Figure 32 31
- Changed footnote 1 in Figure 31 and Figure 32 31

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA3221AIRGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 3221	Samples
INA3221AIRGVT	ACTIVE	VQFN	RGV	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 3221	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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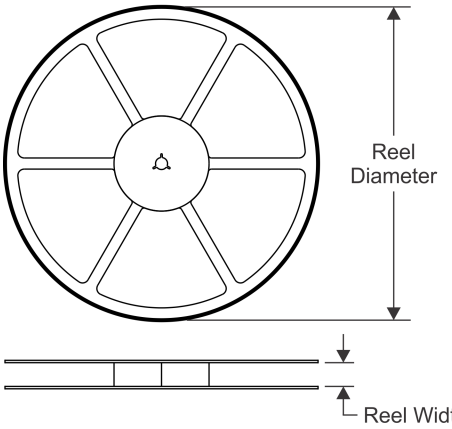
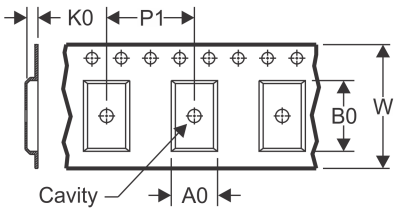
TAPE AND REEL INFORMATION

REEL DIMENSIONS

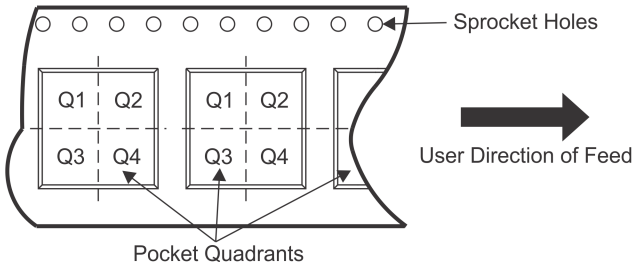


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

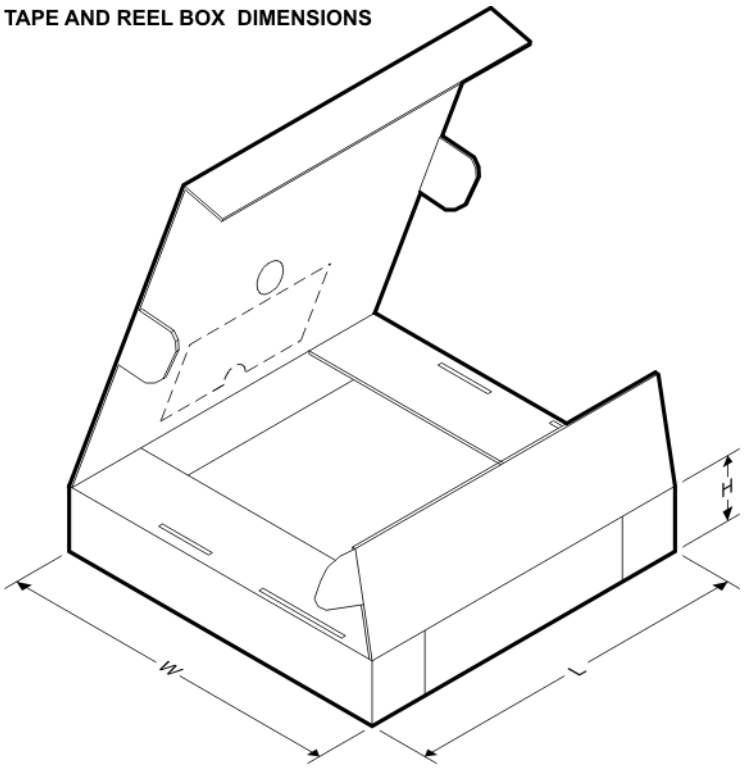
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA3221AIRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
INA3221AIRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

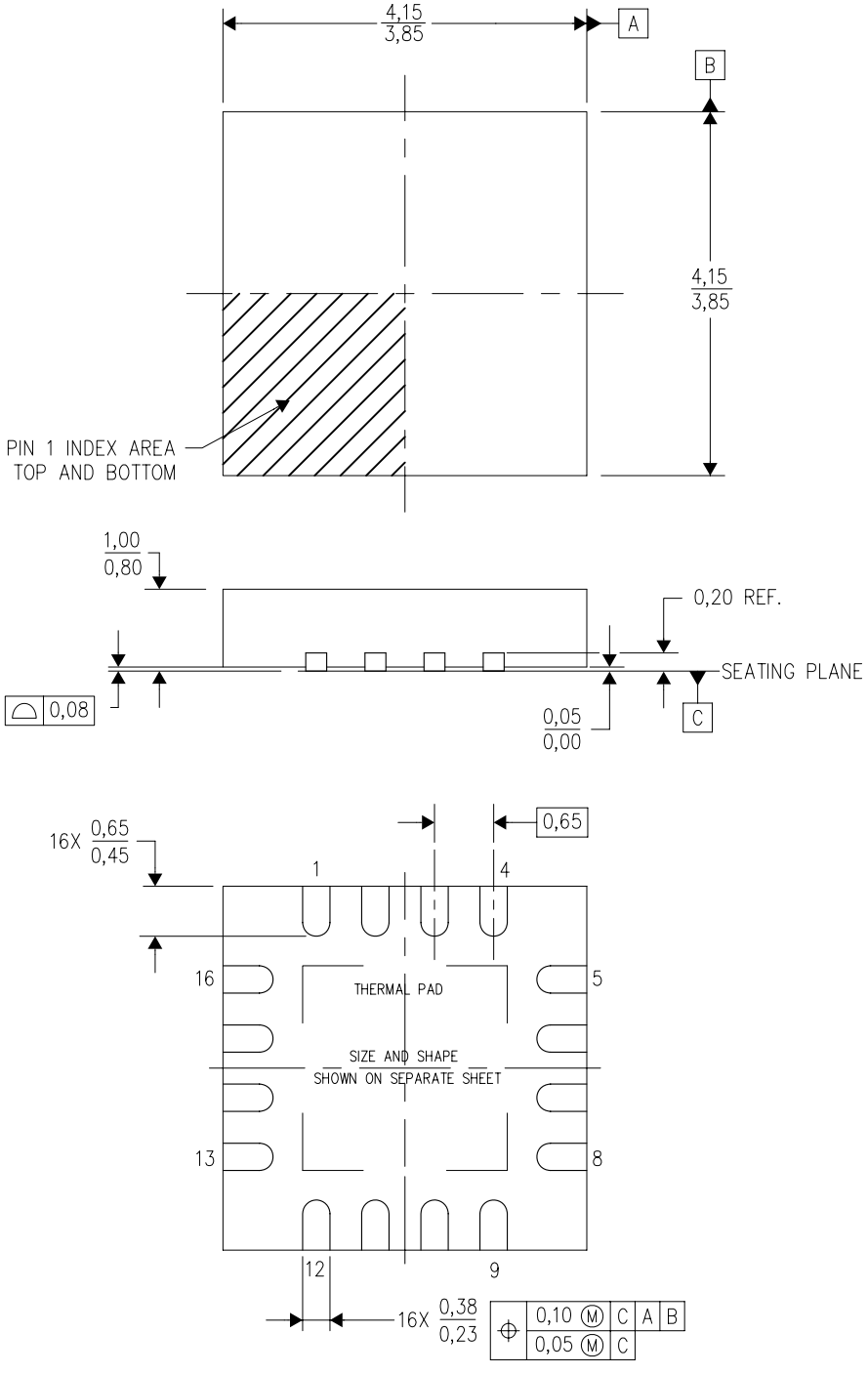
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA3221AIRGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
INA3221AIRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

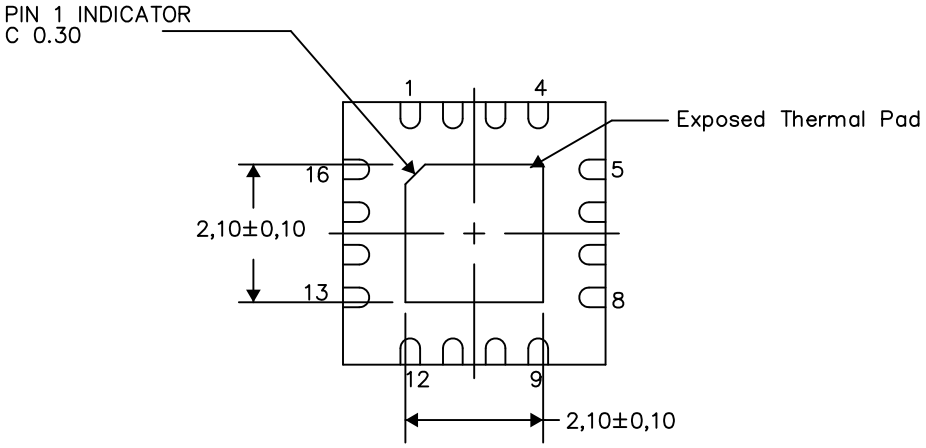
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206351–3/L 05/13

NOTE: All linear dimensions are in millimeters

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