Inductive Cell Balancer IC with Balancing Current Up to 2A

DESCRIPTION

FEATURES

ETA3000 is an inductive cell balancer based on ETA's patent pending proprietary technology. Unlike conventional passive balancing technique, ETA3000 utilizes a control scheme with an inductor to shuffle currents between two cells until the cells are balanced. Due to the switching nature, the heat and power dissipation generated in conventional linear balance technique are greatly reduced. The balance time is also significantly reduced due to higher balancing current not being limited by package thermal dissipation. ETA3000 consumes only &A ultra-low current from batteries in standby mode, extending the battery shelftime. The final balanced voltages ofboth cells are also highly accurate which enhances the performance and lifetime for the batteries connected in series. ETA3000 can also be used in multiple cells stacking with even number of cel Is. ETA3000 includes protection features similar to precondition in battery charging, that is when one cell's voltage is grossly lower than the other, the balancing current is reduced to a safe level until the lower voltage cell is charged up.

Inductive, Switching control Scheme Upto 92% Charger transfer efficiency Accurate Balanced voltages down to30mV Auto detect unbalance and auto balance Low sleeping supply current, 2^A Programmable balancing current up to 2A Precondition balancing current Status Indications

Battery Over voltage protection Support small size inductor

APPLICATIONS

ETA3000 is available in two type of package, SOT23-6, DFN2x2-8L

Two Cells System

E-Cigarette

Battery Pack

Portable Equipment and Instrumentation

Battery Backup Systems

TYPICAL APPLICATION

BATP

ENABLE

STAT BIAS

enETA3000sw

ISET BATC

10uF

1nF：

:Riset

ORDERING INFORMATION

BATN

22uF

2. 2uH

10uF

Li+

Batte

ry

Li+

Batte

ry

Figure 1: Typical Application Circuit

PART No.

ETA3000S2G

ETA3000D2I

PACKAGE

SOT23-6L

DFN2x2-8L

TOP MARK

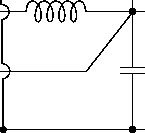
GIYW

GSYW

Pcs/Reel

3000

3000





PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS

BATC

ISET

BATP

BATN

SW

BIAS

SOT23-6

BATC

EN

BATP

ISET

SW

STAT

BATN

BIAS

DFN2x2-8

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for

long periods may affect device reliability.)

SWZ STAT Voltage to BATN

BIAS to SW Voltage

BATC to BATN Voltage

BATP to BATN Voltage

ISET to BATN Voltage

SWZ BATC, BATP to BATN current Operating Temperature Range..

. .…-0.3 V to 12V -0.3 V to 6V

. .…-0.3 V to 6V ……-0.3 V to 12V . .…-0.3 V to 6V Internally limited

. .…-40°Cto85°C

,-55°Cto150°C

260°C

,..2KV

..200V

Storage Temperature Range

Thermal Resistance

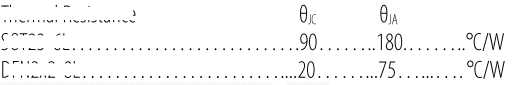
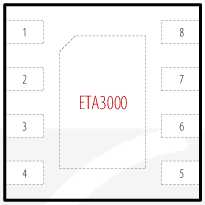
SOT23-6L

DFN2x2-8L

Lead Temperature (SolderingJOssec)

ESDHBM (Human Body Mode) .....

ESDMM (Machine Mode)



ELECTRICAL CHACRACTERISTICS

*(Ta=25°C, LX = 1卩川 Cbot=Gop= 1[jFifnotspecified)*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **PARAMETER** | | **TEST CONDITIONS** | **MIN TYP** | **MAX** | **UNIT** |
| **SUPPLY** | | | | | |
|  | Shutdown current | EN islow/VBATP=8V | 1 | | 卩A |
| IsUPPLY | Quiescent current | EN is high, Vbatp=8V, Vbatr-Vbatc=Vbatc-Vbatn | 2 | | 帕 |
| Operating supply current | EN is high/VBATP=8VJn balancing mode, No Switching | 700 | | 卩A |
| Vbatp | VBATP operating voltage |  | 10 | | V |
| Vbatc | VBATC operating voltage |  | 5 | | V |
| UVLO | Under lock-out voltage threshold | Vbatp Rising | 3.75 | | V |
| UVLO HYS | UVLD hysteresis |  | 200 | | mV |
| **DETECTION** | | | | | |
| Tsleep | Detection interval timer | Part sleeps during Tsleep | 2 | | S |
| Tallow | Unbalance detection acknowledgment timer | Unbalance status is accepted after Tallow when enter CHECK state. | 3.85 | | mS |
| Tcheck | Maximum unbalance checking timer | IC get back to sleeping mode if don't detect unbalance afterTCHECK | 7.68 | | mS |
| Tdone | FinishingTimer | Maximum switching skip before enter sleep mode | 62 | | mS |



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Vkick | Unbalance detection threshold | Balancing only workifOVP>VBATP>UVLO and Vkick Detected between 2 cells | 100 | | | mV |
| Verror | Balancing Accuracy | Error voltage between 2 cells after balancing finish | -30 |  | 30 | mV |
| **BALANCECONTROLLER** | | | | | | |
| FREQ | Switching Frequency | PWM Clock | 1 | | | MHz |
| VlSET | ISET pin voltage in Normal | V (BATP-BATC) >TOP\_PRECOND  And V(batc-batn)>BOT PRECOND | 1 | | | V |
| V|SET\_PRE | ISET Pin Voltage in Precondition | V(batp-batc)<TOP\_PRECOND  OrV(BATc-BATN)<BOT PRECOND | 0.1 | | | V |
| 1 AVERAGE | Average Inductor current Regulation | Riset = 50k0 | 1 | | | A |
| IpRECOND | Precondition current Regulation | Riset = 50k0 | 100 | | | mA |
| **BATTERY PROTECTION** | | | | | | |
| TOP OVP | Top Cell over voltage protection threshold | V(batp-batc)Rising | 5 | | | V |
| TOP OVP HYST | TOP OVP hysteresis | V(BATP-BATc)Falling | 350 | | | mV |
| BOT OVP | Bottom Cell overvoltage protection threshold | V(BATC-BATN)布网 | 5 | | | V |
| BOT OVP HYST | BATC OVP hysteresis | V(batc-batn)Falling | 350 | | | mV |
| TOP PRECOND | Top battery precondition threshold | V(batp-batc)Rising | 2.8 | | | V |
| TOP PREC HYST | TOP PRECOND hysteresis | V(batp-batc)Falling | 150 | | | mV |
| BOT PRECOND | Bottom battery precondition threshold | V(BATC-BATN)布网 | 2.8 | | | V |
| BOT PREC HYST | BOT PRECOND hysteresis | V(batc-batn)Falling | 150 | | | mV |
| **BALANCE PROTECTION** | | | | | | |
| TOPJLIM | Top cell drive current limit | DOWN direction: V(batp-batc)> V(batc-batn) |  | 4.5 |  | A |
| BOT ILIM | Lower cell drive current limit | U P direction: V(batp-batc)< V(batc-batn) |  | 4.5 |  | A |
| **LOGIC CHARATERISTICS** | | | | | | |
| VIL | EN low threshold |  |  |  | 0.4 | V |
| VIH | EN high threshold |  | 1.2 |  |  | V |
| VOL | STAT active low voltage | lsTAT=5mA |  |  | 0.4 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| TSD | Thermal shutdown |  | 160 | | | °C |
| TSD HYST | TSD Hysteresis |  | 30 | | | °C |

PIN DESCRIPTION

|  |  |  |  |
| --- | --- | --- | --- |
| **PIN NAME** | **DESCRIPTION** | | |
| **S0T23-6** | **DFN2x2-8L** |  |
| ISET | 1 | 7 | Balancing current setting pin. Connect a resistor from ISET to BATN to program the balancing current. Bypass the pin to BATN with 1nF capacitor. |
| BATN | 2 | 4 | Negative terminal Sense voltage input and common Ground pin. |
| BIAS | 3 | 5 | Bias pin. Connect a 10nF capacitor from BIAS to SW |
| SW | 4 | 3 | Switching node. Connected to inductor. |
| BATP | 5 | 2 | Sense voltage input for top cell. Connect 1 pF capacitor between BATP and BATC. |
| BATC | 6 | 1 | Sense voltage input for bottom cell. Connect 1 pF capacitor between BATC and BATN. |
| STAT | N/A | 6 | Open drain output to indicate balancing state. STAT active LOW during balancing |
| EN | N/A | 8 | IC Enable Input. EN is internally pulled to Logic High. Driver to a Logic Low to disable IC. EN pin is internally pulled up to Logic High. |
| EP | N/A | EP | Exposed Pad, connect it toGND |

Figure 2: Functional Block Diagram

|  |  |  |
| --- | --- | --- |
| Bandgap &VDD &BIAS &OVP &TSD |  | Battery  Sense |
| I |
| Balance |
|  |
| Balance  Current  Sense | — | Control |

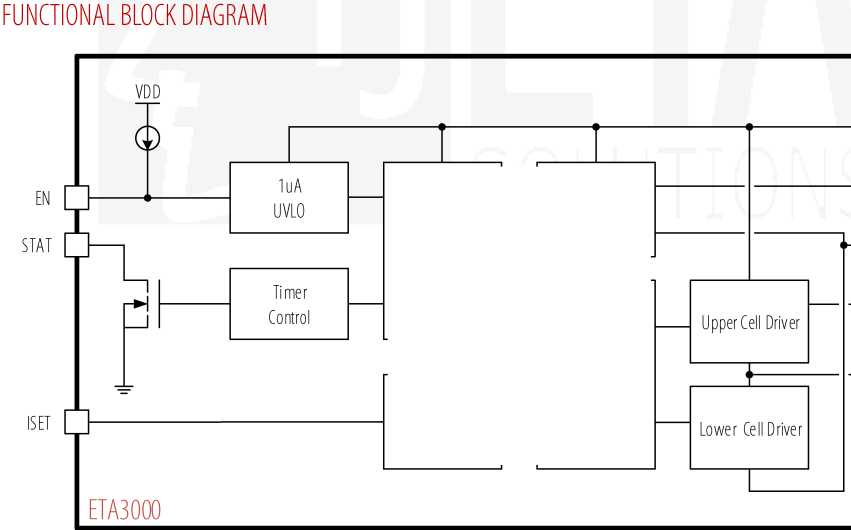
BATP

BATC

BATN

BIAS

sw

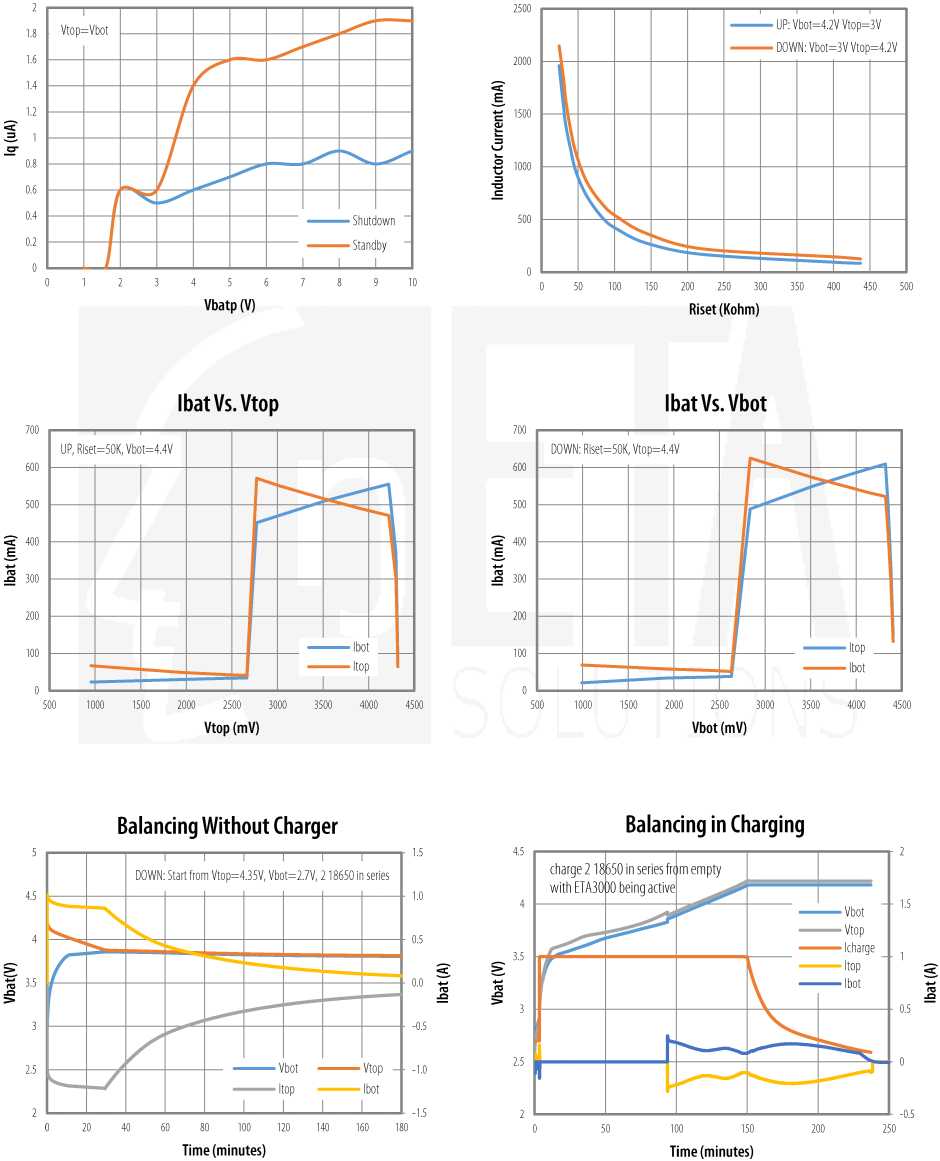


TYPICAL PERFORMANCE CHARACTERISTICS

(TA=25OC, unless otherwise specified)

**IqVs.Vbatp**

**Inductor Current Vs. Riset**





TYPICAL PERFORMANCE CHARACTERISTICS (cont')

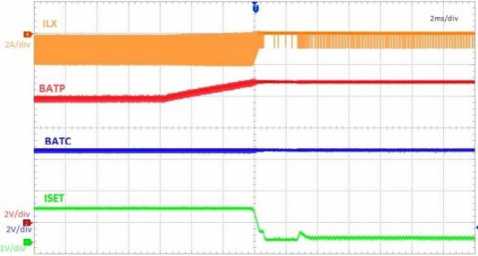
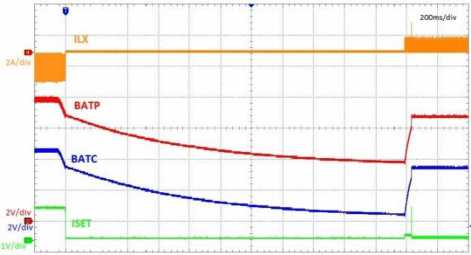
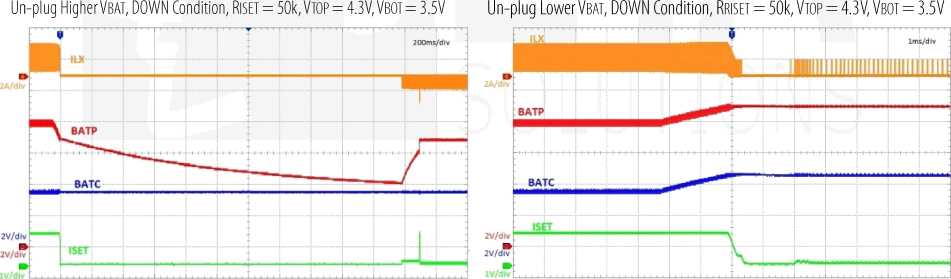
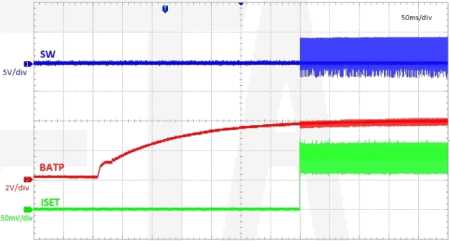
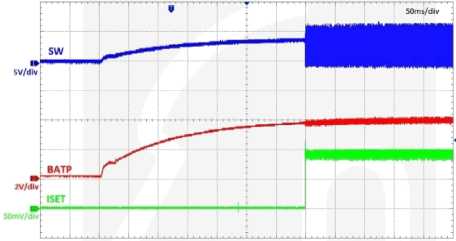
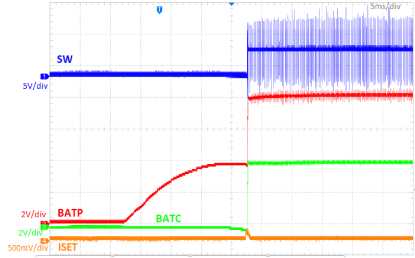
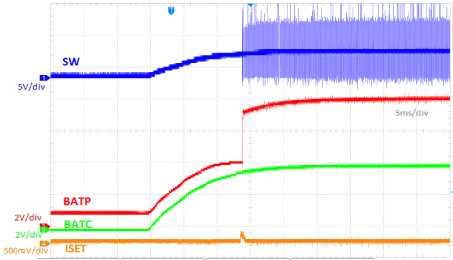
Vbot plug-in Start-Up, Vtop = Floating, Riset = 50kz Vbot = 4.3V

Vbotplug-in Start-Up,Vtop = Shorted, Riset = 50kzVbot = 4.3V

Vtop plug-in Start-Up, Vbot = Shorted, Riset = 50kz Vtop = 4.3V

Un-plug HigherVBAT, UP Condition, Riset = 50k,VTop = 4.3V, Vbot = 3.5V

Un-plug Lower Vbat, UP Condition, Riset = 50k, Vtop = 4.3V, Vbot = 3.5V





FEATURE DESCRIPTION

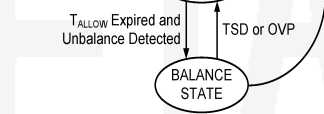
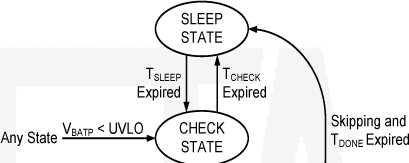
The ETA3000 is a battery cell balancerwith lossless inductive architecture based on ETA's proprietary technology. Thetechnology is developed by ETA Solutionsand any copy without ETA's agreement will be forbidden.

During operation, ETA3000 detects the difference between 2 cells then start balancing if the difference exceeds Vkick. Once detected Vkick, ETA3000 will discharge the higher voltage cell, store that discharging energy in the inductor then charge that energy to the lower voltage cell. ETA3000 keeps balancing until there is no difference between 2 cells.

ETA3000 technology allows balancing in either charge or discharge phases of the battery with minimized loss.

Without unbalanced condition, ETA3000 operates in sleep mode with low supply current. This is an advantage to extend battery pack life time.

STATE MACHINE

The ETA3000 provides a completed state machine that controls whole operation intelligently. With this state machine, ETA3000 is equipped with self-protection from any accident during balancing. It also keeps the part stay asleep as much as possible until unbalance detected.

Figures： State Machine Diagram

ETA3000 always starts from CHECK state when battery is plugged in.

Any fault always forces ETA3000 back to SLEEP State where ETA3000 burns only 2pA (typically) from BATR

The ETA3000 timing diagram for state machine is shown in following figure.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| nUVLO and |  | |  |  |  |  |  |  |  |  |  |  |  |  |
| EN |  | |  |  |  |  |  | BALANCING | | |  |  |  |  |
| 2s TIMER | — | Tcheck | **H**  **O LU**  **1— LU Q** | / TslEEP 、 | **I— o LU 1— LU Q** | | Constant |  | Current | | Skip  / Tdone \ | / Tsleep 、 | **H**  **O LU**  **1— LU Q** |  |
| — |  | — | — | Current |  | Dimming | |  | — |
|  |  | |  |  |  |  |  |  |  |  | DO | NE |  |  |
|  |  | |  |  |  |  |  |  |  |  | — |  | | |

Figure 4: Timing Profile

UNBALANCE DETECTION

When state is in CHECK State, ETA3000 detects Vkick difference between 2 cells to enter BALANCE State. If the top cell voltage is higher, balancing will be "DOWN： meaning discharge the top cell to charge to bottom cell. And if the bottom cell voltage is higher, balancing will be "UP： meaning discharge the bottom cell to charge to top cell.

BALANCING PROFILE

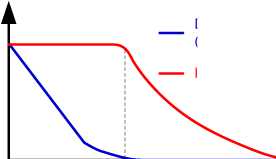
ETA3000 balancing always starts with ^Constant Current Regulation'7 phase since it is always with high voltage difference. Constant current is set by Riset.

Figure5: Balancing Profile

Inductor Current

fonstant Curren\* Current Dimming 又 JTDone

Delta Voltage

(At IC pin Measurement)

When the detected difference atICpin is almost zero, but due to battery equivalent series resistance, real difference is not zero, then current is not immediately zero but reduced slowly depend on battery capacitance. This condition is called "Current Dimming〃phase.

When two cell voltages are equal, balancing current becomes almost zero, when this persist fora time period oHdone, the balancing finishes one cycle, and ETA3000 goes back to SLEEP State.

PROTECTION

ETA3000 provides full protection to batteries that extend the life time ofthe batteries:

* Short and Low Voltage Protection: When either ofthe cell voltage below Vprecond, maximum balancing current will be re-defined to 10% ofthe level set by ISET pin resistor.
* Open and Over Voltage Protection: When either ofthe cell voltage is greater than Vovp, ETA3000 will stop balancing, and go back to SLEEPING. Part will wake up afterTsiB
* Thermal Shutdown: When part gets hotter than 160°Cz ETA3000 will stop balancing, and go back to SLEEPING. Part will wake up after Tsleep.
* Current Limit Protection: Maximum ofthe peak of inductor current is allowed to 5.5A.

APPLICATION INFORMATION

BALANCING CURRENT SETTING

Balancing current is defined as the half of average inductance current. Average inductance current is regulated following ISET resistor configuration.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CURRENT** | **ISETRESSITOR** | **ISET CAPACITOR** | **INDUCTOR** | **BATTERY CAPACITOR** |
| 100mA | 500k0 | 500pF-10nF | 0.33-0.6 卩 H | 0.47 卩 F-3.3” |
| 250mA | 200k0 | 500pF-10nF | 0.47-1 nH | 0.47 卩 F-3.3” |
| 400mA | 125k0 | 500pF-10nF | 0.47-1 nH | 0.47 卩 F-3.3” |
| 500mA | 100k0 | 500pF-10nF | 0.47-1 nH | 0.47 卩 F-3.3” |
| 625mA | 80k0 | 500pF-10nF | 0.68-1 | 0.47 卩 F-3.3” |
| 800mA | 62.5k0 | 500pF-10nF | 0.68-1 | 0.47 卩 F-3.3” |
| 1000mA | 50k0 | 500pF-10nF | 0.68-1 | 0.47 卩 F-3.3” |
| 1250mA | 40k0 | 500pF-10nF | 0.68-1 | 0.47 卩 F-3.3” |
| 1515mA | 33k0 | 500pF-10nF | 0.68-1 nH | 0.47 卩 F-3.3” |
| 1667mA | 30k0 | 500pF-10nF | ■ | 0.47 卩 F-3.3” |
| 2000mA | 25k0 | 500pF-10nF | 1-2nH | 0.47 卩 F-3.3” |

**RECOMMENDED COMPONENT**

**AVERAGE INDUCTION**

Balancing current isdefinec

as average of inductor current.

RESTRICTED CONDITIONS

ETA3OOO does not allow following restricted conditions:

* Reverse battery connection
* ShortSWtoanyofBATN, BATR BATC
* Not exceed the absolute maximum rating of each IC pin

MULTI-COUPLE CELL BALANCING SOLUTION

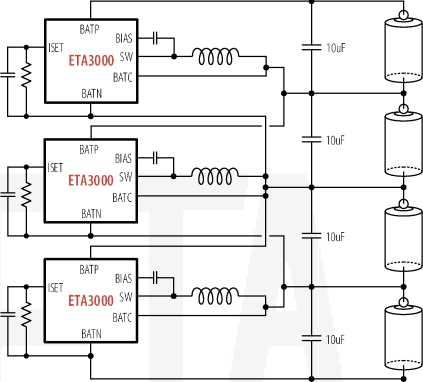
It is also possible to use several ETA3000 ICs in application to balance multi-cell series battery such as balancing for laptop battery pack.

Figure 7 shows a typical solution for 4-cell-battery in battery pack.

Each ETA3000 manages balancing of 2 neighbor cells. And without enable control, each ETA3000 operates independently.

Positive terminal of the pack is connected to BATP of Cell 4 and Negative terminal of the pack is connected to BATN of Cell 1.

Figure 6: Multi-Cell Balancing Solution



JE1A

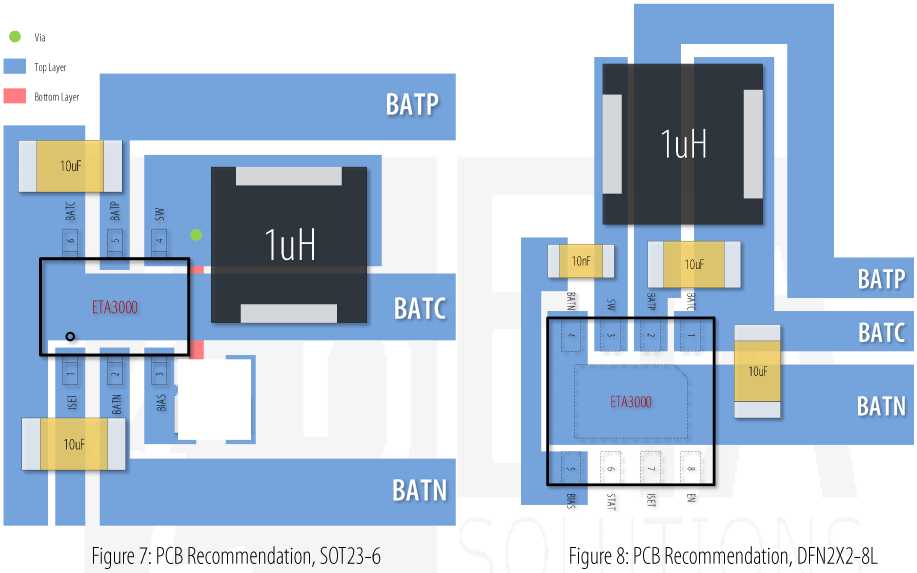
**ring Minds** □「腿 **Smarts**

PCB DESIGN GUIDELINE

In an UP case that bottom cell voltage is greater than top cell voltage, bottom cell becomes input and top cell becomes output of the switching regulation. In a DOWN case that top cell voltage is greater than bottom cell voltage, top cell becomes input and bottom cell becomes output. These mean parallel battery capacitors are always output capacitor or input capacitor for regulator. So please require to locate as close as possible to IC pins to minimize series resistance.

Please try to get the order of battery pins are BATP - BATC - BATN to make an easy battery connection.

|  |  |  |
| --- | --- | --- |
|  |  | |
| ■ | | |
|  | llOnFl |  |
|  | | |



JIA

**ring Minds** □「腿 **Smarts**

PACKAGE OUTLINE

**Dimensions In Inches**

0.000

0.100

0.000

0.004

1.050

1.150

0.041

0.045

0.300

0.500

0.012

0.020

0.100

0.004

0.008

2.820

0.111

0.119

1.500

0.059

0.067

0.116

1.800

0.071

0.079

0.300

0.024

**Dimensions In Inches**

0.002

0.082

2.076

0.076

0.082

1.300

0.043

0.051

0.700

0.020

0.028

0.200 MIN

0.008 MIN

0.426

**Dimensions In Millimeters**

■LTLrLru

1.050

1.250

0.041

0.049

2.650

0.200

1.700

2.950

0.104

0.012

**Dimensions In  
Millimeters**

0.700

0.000

1.924

1.924

0.500

0.200

0.800

0.050

2.076

0.300

0.028

0.000

0.076

0.008

0.031

0.012

