1. Description

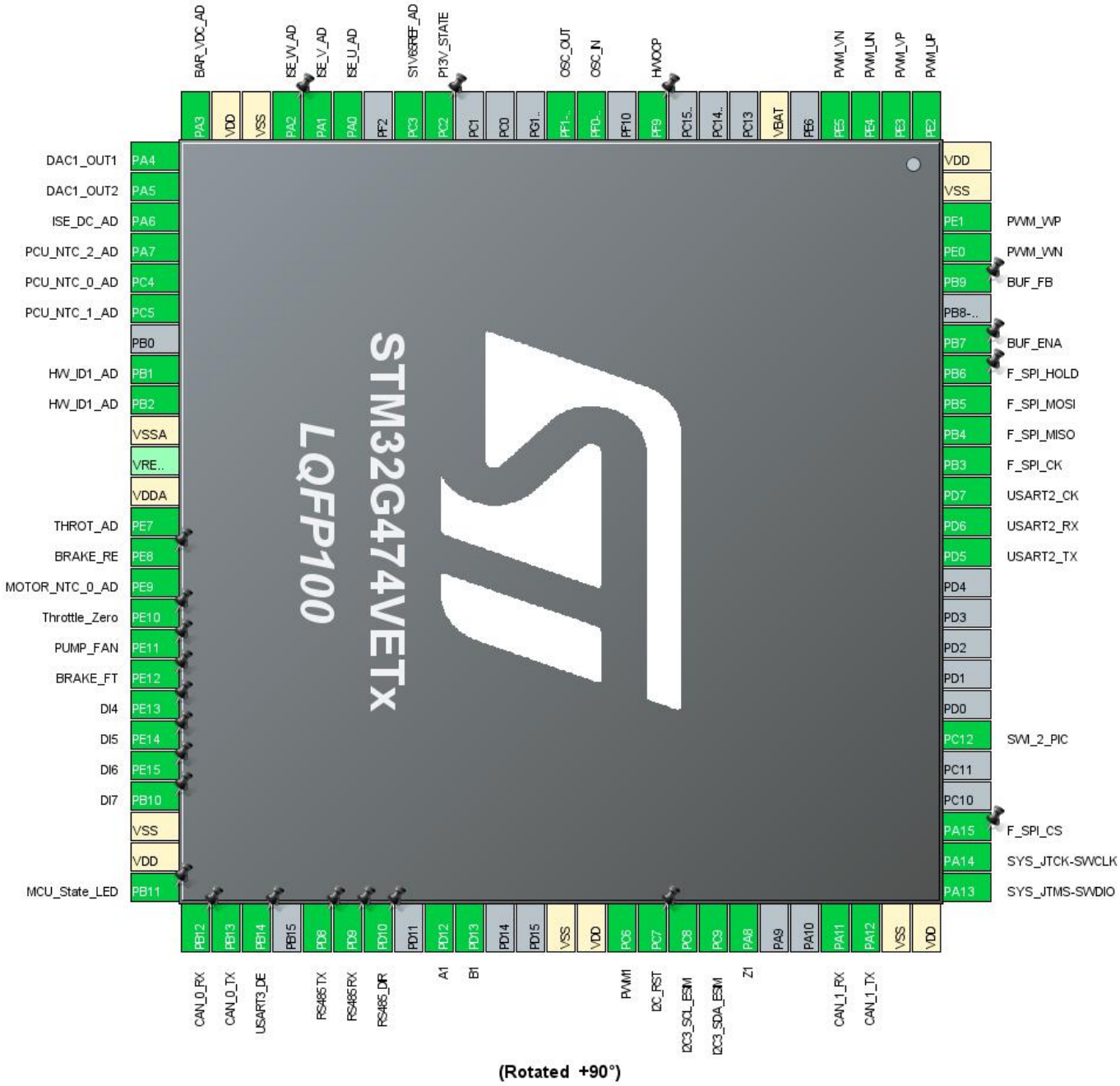
1.1. Project

Project Name	trunk
Board Name	custom
Generated with:	STM32CubeMX 5.4.0
Date	12/16/2020

1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



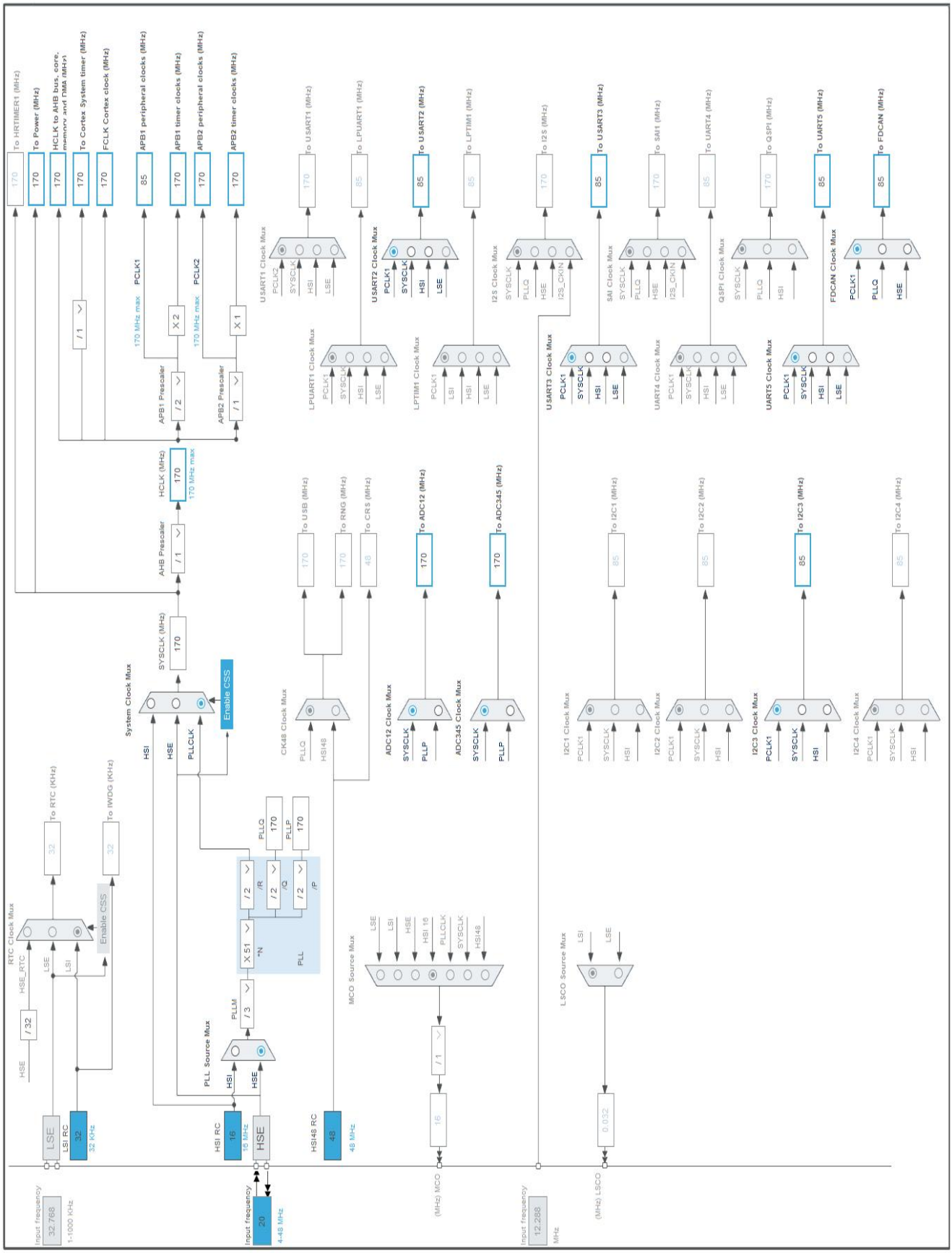
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	TIM20_CH1	PWM_UP
2	PE3	I/O	TIM20_CH2	PWM_VP
3	PE4	I/O	TIM20_CH1N	PWM_UN
4	PE5	I/O	TIM20_CH2N	PWM_VN
6	VBAT	Power		
10	PF9	I/O	TIM20_BKIN	HWOCP
12	PF0-OSC_IN	I/O	RCC_OSC_IN	OSC_IN
13	PF1-OSC_OUT	I/O	RCC_OSC_OUT	OSC_OUT
17	PC2 *	I/O	GPIO_Input	P13V_STATE
18	PC3	I/O	ADC1_IN9	S1V65REF_AD
20	PA0	I/O	ADC1_IN1	ISE_U_AD
21	PA1	I/O	ADC2_IN2	ISE_V_AD
22	PA2	I/O	ADC1_IN3	ISE_W_AD
23	VSS	Power		
24	VDD	Power		
25	PA3	I/O	ADC1_IN4	BAR_VDC_AD
26	PA4	I/O	DAC1_OUT1	
27	PA5	I/O	DAC1_OUT2	
28	PA6	I/O	ADC2_IN3	ISE_DC_AD
29	PA7	I/O	ADC2_IN4	PCU_NTC_2_AD
30	PC4	I/O	ADC2_IN5	PCU_NTC_0_AD
31	PC5	I/O	ADC2_IN11	PCU_NTC_1_AD
33	PB1	I/O	ADC3_IN1	HW_ID1_AD
34	PB2	I/O	ADC2_IN12	HW_ID1_AD
35	VSSA	Power		
37	VDDA	Power		
38	PE7	I/O	ADC3_IN4	THROT_AD
39	PE8 *	I/O	GPIO_Input	BRAKE_RE
40	PE9	I/O	ADC3_IN2	MOTOR_NTC_0_AD
41	PE10 *	I/O	GPIO_Input	Throttle_Zero
42	PE11 *	I/O	GPIO_Input	PUMP_FAN
43	PE12 *	I/O	GPIO_Input	BRAKE_FT
44	PE13 *	I/O	GPIO_Input	DI4
45	PE14 *	I/O	GPIO_Input	DI5
46	PE15 *	I/O	GPIO_Input	DI6
47	PB10 *	I/O	GPIO_Input	DI7

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
48	VSS	Power		
49	VDD	Power		
50	PB11 *	I/O	GPIO_Output	MCU_State_LED
51	PB12	I/O	FDCAN2_RX	CAN_0_RX
52	PB13	I/O	FDCAN2_TX	CAN_0_TX
53	PB14	I/O	USART3_DE	
55	PD8	I/O	USART3_TX	RS485 TX
56	PD9	I/O	USART3_RX	RS485 RX
57	PD10 *	I/O	GPIO_Output	RS485_DIR
59	PD12	I/O	TIM4_CH1	A1
60	PD13	I/O	TIM4_CH2	B1
63	VSS	Power		
64	VDD	Power		
65	PC6	I/O	TIM3_CH1	PWM1
66	PC7 *	I/O	GPIO_Output	I2C_RST
67	PC8	I/O	I2C3_SCL	I2C3_SCL_ESIM
68	PC9	I/O	I2C3_SDA	I2C3_SDA_ESIM
69	PA8	I/O	TIM4_ETR	Z1
72	PA11	I/O	FDCAN1_RX	CAN_1_RX
73	PA12	I/O	FDCAN1_TX	CAN_1_TX
74	VSS	Power		
75	VDD	Power		
76	PA13	I/O	SYS_JTMS-SWDIO	
77	PA14	I/O	SYS_JTCK-SWCLK	
78	PA15 *	I/O	GPIO_Output	F_SPI_CS
81	PC12	I/O	UART5_TX	SWI_2_PIC
87	PD5	I/O	USART2_TX	
88	PD6	I/O	USART2_RX	
89	PD7	I/O	USART2_CK	
90	PB3	I/O	SPI1_SCK	F_SPI_CK
91	PB4	I/O	SPI1_MISO	F_SPI_MISO
92	PB5	I/O	SPI1_MOSI	F_SPI_MOSI
93	PB6 *	I/O	GPIO_Output	F_SPI_HOLD
94	PB7 *	I/O	GPIO_Output	BUF_ENA
96	PB9 *	I/O	GPIO_Input	BUF_FB
97	PE0	I/O	TIM20_CH4N	PWM_WN
98	PE1	I/O	TIM20_CH4	PWM_WP
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	trunk
Project Folder	D:\CodeRepo\trunk
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.1.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
MCU	STM32G474VETx
Datasheet	DS12288_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN9: IN9 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Enabled
End Of Conversion Selection	**End of sequence of conversion ***
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	**Channel 9 ***
Sampling Time	**24.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	**Enable ***
Number Of Conversions	**3 ***
External Trigger Source	**Timer 20 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Enable Injected Oversampling	Disable

Injected Conversion Mode	None
Injected Queue	Injected Queue Disable
Rank	1
Channel	Channel 1
Sampling Time	**12.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 3 ***
Sampling Time	**12.5 Cycles ***
Offset Number	No offset
Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	**12.5 Cycles ***
Offset Number	No offset

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

IN11: IN11 Single-ended

IN12: IN12 Single-ended

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0

Scan Conversion Mode	Enabled
End Of Conversion Selection	**End of sequence of conversion ***
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**5 ***
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	**Channel 3 ***
Sampling Time	**24.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 4 ***
Sampling Time	**24.5 Cycles ***
Offset Number	No offset
Rank	**3 ***
Channel	**Channel 5 ***
Sampling Time	**24.5 Cycles ***
Offset Number	No offset
Rank	**4 ***
Channel	**Channel 11 ***
Sampling Time	**24.5 Cycles ***
Offset Number	No offset
Rank	**5 ***
Channel	**Channel 12 ***
Sampling Time	**24.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	**Enable ***
Number Of Conversions	**1 ***
External Trigger Source	**Timer 20 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge

Enable Injected Oversampling	Disable
Injected Conversion Mode	None
Injected Queue	Injected Queue Disable
Rank	1
Channel	Channel 2
Sampling Time	**12.5 Cycles ***
Offset Number	No offset

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC3

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN4: IN4 Single-ended

7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Enabled
End Of Conversion Selection	**End of sequence of conversion ***
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**3 ***

External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 1
Sampling Time	**12.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**12.5 Cycles ***
Offset Number	No offset
Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	**12.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. CORDIC

mode: Activated

7.5. DAC1

OUT1 mode: Connected to external pin only

OUT2 mode: Connected to external pin only

7.5.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
DAC High Frequency	Mode Automatic
DMA Double Data	Disable
Signed Format	Disable
Trigger	None

Trigger2	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Enable
DAC High Frequency	Mode Automatic
DMA Double Data	Disable
Signed Format	Disable
Trigger	None
Trigger2	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.6. FDCAN1

Mode: Classic Master

7.6.1. Parameter Settings:

Basic Parameters:

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	**Enable ***
Protocol Exception	Disable
Nominal Prescaler	**5 ***
Nominal Sync Jump Width	**6 ***
Nominal Time Seg1	**25 ***
Nominal Time Seg2	**8 ***
Data Prescaler	**5 ***
Data Sync Jump Width	**6 ***
Data Time Seg1	**25 ***
Data Time Seg2	**8 ***
Std Filters Nbr	**4 ***
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

7.7. FDCAN2

Mode: Classic Slave

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	**Enable ***
Protocol Exception	Disable
Nominal Prescaler	**5 ***
Nominal Sync Jump Width	**6 ***
Nominal Time Seg1	**25 ***
Nominal Time Seg2	**8 ***
Data Prescaler	**5 ***
Data Sync Jump Width	**6 ***
Data Time Seg1	**25 ***
Data Time Seg2	**8 ***
Std Filters Nbr	**3 ***
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

7.8. GPIO

7.9. I2C3

I2C: I2C

7.9.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	

	0x10A0A6FB *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.10.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	8WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.11. SPI1

Mode: Full-Duplex Master

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**5.3125 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	**Disabled ***
NSS Signal Type	Software

7.12. SYS

Debug: Serial Wire
Power Voltage Detector In: Power Voltage Detector In (Internal analog voltage)
Timebase Source: SysTick
mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.12.1. Parameter Settings:

Programmable_Voltage_Detector_Settings:

PVD detection Level	PWR PVD LEVEL 0 (2.0 V)
PWR PVD Mode	basic mode is used

7.13. TIM3

Slave Mode: Reset Mode
Trigger Source: TI1FP1
Clock Source : Internal Clock
Channel1: Input Capture direct mode
Channel2: Input Capture indirect mode

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1-1
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**16384-1 ***
Internal Clock Division (CKD)	**Division by 4 ***
auto-reload preload	Disable

Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	**Falling Edge ***
IC Selection	Indirect
Prescaler Division Ratio	No division

7.14. TIM4

Combined Channels: Encoder Mode + index

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

Encoder:

Index input polarity	Non Inverted
Index Prescaler	Capture performed each event
index filter	0
encoder first index	Disable

Index Position	Encoder index position is AB=00
Index Direction	Index resets the counter whatever the direction
Encoder Mode	Encoder Mode TI1
Slave Mode Preload Activation	Disable
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.15. TIM6

mode: Activated

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**(170 - 1) ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**(1000 - 1) ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

7.16. TIM7

mode: Activated

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**(170-1) ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**(10000-1) ***

auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

7.17. TIM20

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel4: PWM Generation CH4 CH4N

mode: Activate-Break-Input

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	(1 - 1)
Counter Mode	**Center Aligned mode1 ***
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**(8500 - 1) ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	**1 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Enable
BRK Polarity	**Low ***
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Enable
Break_IO mode selection	Break IO is an Input
Digital Input Polarity	Polarity High
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable

- COMP7	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
DeadTime Preload	Disable
Dead Time	**128 ***
Asymmetrical DeadTime	Disable
Falling Dead Time	0

Clear Input:

Clear Input Source	Disable

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable

CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 4 and 4N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

7.18. UART5

Mode: Single Wire (Half-Duplex)

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	**FIFO mode enable ***
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. USART2

Mode: Synchronous Master

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
ClockPrescaler	clock /1
Slave Mode	Disable
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Clock Parameters:

Clock Polarity	Low
Clock Phase	One Edge
Clock Last Bit	Disable

7.20. USART3

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1

Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	S1V65REF_AD
	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	ISE_U_AD
	PA2	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	ISE_W_AD
	PA3	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	BAR_VDC_AD
ADC2	PA1	ADC2_IN2	Analog mode	No pull-up and no pull-down	n/a	ISE_V_AD
	PA6	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	ISE_DC_AD
	PA7	ADC2_IN4	Analog mode	No pull-up and no pull-down	n/a	PCU_NTC_2_AD
	PC4	ADC2_IN5	Analog mode	No pull-up and no pull-down	n/a	PCU_NTC_0_AD
	PC5	ADC2_IN11	Analog mode	No pull-up and no pull-down	n/a	PCU_NTC_1_AD
	PB2	ADC2_IN12	Analog mode	No pull-up and no pull-down	n/a	HW_ID1_AD
ADC3	PB1	ADC3_IN1	Analog mode	No pull-up and no pull-down	n/a	HW_ID1_AD
	PE7	ADC3_IN4	Analog mode	No pull-up and no pull-down	n/a	THROT_AD
	PE9	ADC3_IN2	Analog mode	No pull-up and no pull-down	n/a	MOTOR_NTC_0_AD
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
FDCAN1	PA11	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	CAN_1_RX
	PA12	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	CAN_1_TX
FDCAN2	PB12	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	CAN_0_RX
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	CAN_0_TX
I2C3	PC8	I2C3_SCL	Alternate Function Open Drain	Pull-up	Low	I2C3_SCL_ESIM
	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	Low	I2C3_SDA_ESIM
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	OSC_IN
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	OSC_OUT
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	F_SPI_CK
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	F_SPI_MISO
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	F_SPI_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM1
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	A1
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	B1
	PA8	TIM4_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	Z1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM20	PE2	TIM20_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_UP
	PE3	TIM20_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_VP
	PE4	TIM20_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_UN
	PE5	TIM20_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_VN
	PF9	TIM20_BKIN	Alternate Function Open Drain	No pull-up and no pull-down	Low	HWOCP
	PE0	TIM20_CH4N	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_WN
	PE1	TIM20_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_WP
UART5	PC12	UART5_TX	Alternate Function Open Drain	No pull-up and no pull-down	Low	SWI_2_PIC
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD7	USART2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB14	USART3_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	RS485 TX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	RS485 RX
GPIO	PC2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	P13V_STATE
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRAKE_RE
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Throttle_Zero
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PUMP_FAN
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BRAKE_FT
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI4
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI5
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI6
	PB10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DI7
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MCU_State_LED
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RS485_DIR
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	I2C_RST
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	F_SPI_CS
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	F_SPI_HOLD
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUF_ENA
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUF_FB

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC3	DMA1_Channel3	Peripheral To Memory	**Medium ***
ADC1	DMA1_Channel1	Peripheral To Memory	**Medium ***
ADC2	DMA1_Channel2	Peripheral To Memory	**Medium ***

ADC3: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA1_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	7	0
DMA1 channel2 global interrupt	true	7	0
DMA1 channel3 global interrupt	true	7	0
ADC1 and ADC2 global interrupt	true	3	0
FDCAN1 interrupt 0	true	7	0
FDCAN1 interrupt 1	true	7	0
TIM3 global interrupt	true	4	0
TIM4 global interrupt	true	4	0
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	true	6	0
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	true	4	0
TIM7 global interrupt, DAC2 and DAC4 channel underrun error interrupts	true	5	0
TIM20 update interrupt	true	1	0
FDCAN2 interrupt 0	true	7	0
FDCAN2 interrupt 1	true	7	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		
ADC3 global interrupt	unused		
UART5 global interrupt / UART5 wake-up interrupt through EXTI line 35	unused		
TIM20 break interrupt	unused		
TIM20 trigger and commutation interrupts	unused		
TIM20 capture compare interrupt	unused		
FPU global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
I2C3 event interrupt / I2C3 wake-up interrupt through EXTI line 27	unused		
I2C3 error interrupt	unused		
CORDIC interrupt	unused		

*** User modified value**

9. Software Pack Report