5G NR Link Level Simulation Using Simulink HDL Coder

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Abstract

With the rapid advancement of 5G technology, remote robotic surgery has become a reality.This paper discusses and completes the design of the 5G NR communication system using 2022a Matlab/Simulink software, and uses HDL Coder toolbox on the simulink platform for physical layer design of FPGA. The design contains CRC16, LDPC, beamforming, MRC, soft demodulation, scheduling. It also includes LDPC rate matching and control signal recovery and synchronization, and simulates a complete timing diagram and plots BER graph under AWGN and Rayleigh channel with various SNR at the end. This approach is useful to provide validation before hardware implementation.
Keywords: 5G NR, link level simulation, HDL Coder

Topics: information and communication model, information systems

1 Introduction

In the medical sector, 5G holds vast application prospects. Remote surgery applications require ultra-reliable low-latency communication (uRLLC), while remote monitoring of video streams demands enhanced mobile broadband (eMBB) capabilities [1]. In order to analyze the unique advantages of 5G communication and understand the functionalities of its various components, link-level simulation is essential [2]. In [3], authors developed a Matlab-based 5G link-level simulation tool to evaluate the average performance of large-scale networks. The NS-3 5G LENA simulator [4] is an NS-3 module that allows for end-to-end simulation of 3GPP-based cellular networks. Furthermore, authors in [12] developed a transceiver using Matlab/Simulink.

HDL Coder is a code generation software developed by MathWork based on Matlab platform. The software can translate Matlab code or simulink models into Verilog standard HDL language. In [5], the authors utilized HDL Coder to construct a PUCCH (Physical Uplink Control Channel) demodulation unit and deployed it on an FPGA (Field-Programmable Gate Array) device. In this paper, we developed a link-level simulation for the 5G downlink using HDL Coder and conducted simulations. The contribution of this paper lies in the establishment of a visual interface utilizing the Simulink tool to bridge the gap between Matlab and actual hardware design.

2 Overview of system architecture

In this paper, HDL Coder toolbox in simulink platform will be used to realize communication transceiver based on 5G NR standard, and simulation result diagram and complete design process will be given for reference when using FPGA design. The current system parameters are as follows:

Parameter	Settings
Bandwidth	100MHz
Subcarrier spacing	120KHz
Number of RB	66
Subcarriers per RB	12
OFDM symbols per slot	14
Slots per sub-frame	8
Slots per frame	80
FFT points of OFDM	1024
Sampling rate	1024×120K
Long CP	136
Short CP	72

Table 1: System link simulation parameters

In order to better monitor and process data, the system architecture adopted in this paper is to first generate random user bit data from Matlab, formulate transmission protocols according to transmitter transmission requirements, and modify the user data format to transmit to the transmitter model. After the transmitter

completes the simulation in simulink, the simulation data and control information are returned to Matlab, and then transmitted to the receiver model after the channel model is built in Matlab. After the receiver is processed, the received information is returned to Matlab for data verification and statistics. The simulation architecture process is shown in the figure below.

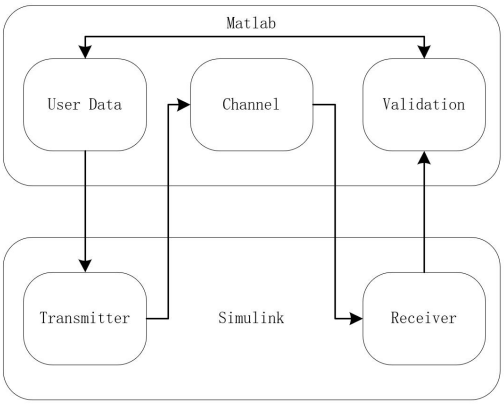

Fig.1: Architecture of simulation

3 Design of transmitter module

The generation of the transmission block is determined based on the predefined parameter set (Table 1). According to the parameters mentioned earlier, the transmission block length used here is 512 bits, controlled by an enable signal. Besides requiring block processing, the transmission block module must also possess hierarchical and multi-process functionalities. The multi-process feature allows for data segmentation, creating certain time gaps for serialized data in subsequent processing, thereby providing effective processing space for the data.

According to the 5G NR standard, each wireless frame consists of 10 slots, and each slot contains 14 OFDM symbols. Among these symbols, the first one is a reference signal (pilot symbol), while the rest are data symbols. This implies that 13 processing steps are required to complete the necessary functions. The transmitter's received user data goes through a series of modules: multiplexer, CRC encoding module, LDPC rate matching module, LDPC encoding module, symbol mapping module, beamforming module, OFDM modulation module, and another multiplexer.As per TS38.211[6], under redundancy mode 0, the rate matching process involves discarding data from the 385th to the 576th position after LDPC encoding and then selecting the first 1584 data items. In this paper, the adopted strategy is to store the initial 384 data items into RAM first and then store the data from the 577th to the 985th position into RAM. When the 986th data item arrives, the data in RAM is sequentially output together, completing the interleaving encoding process while maintaining an overall data rate unchanged.

Since QPSK modulation is used, and the upper-layer output data is in parallel, QPSK symbol generation can be directly implemented using combinational logic circuits. In the beamforming module, the strategy used is to share one column vector of an 8×8 DFT matrix (stored in ROM) among every 8 RBs, leaving 2 RBs to be multiplied with the first two column vectors of the DFT matrix, resulting in a total of 66 RBs. The DFT matrix used for multiplication should have the same type as the input data. However, due to the nature of multiplication, the result is typically 64 bits, requiring some sacrifice of precision.

Since it is divided into 13 processes, with each process having 8 serial OFDM symbols, the first serial symbol of each process is extracted to form the waveform plot shown below. It can be seen that the OFDM symbols exhibit a stepped pattern without any gaps in between. The transmitter model is depicted in Figure 2.

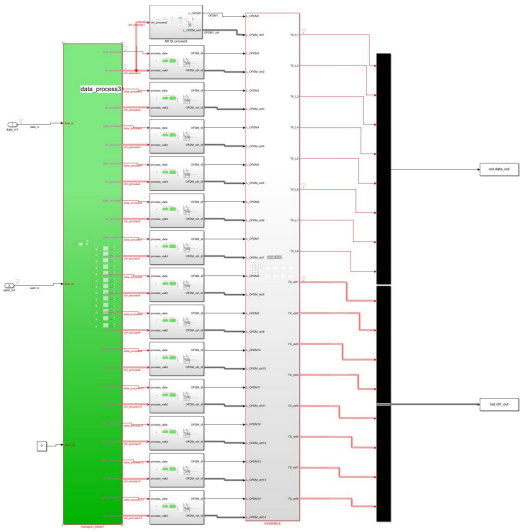

Fig.2: transmitter based on 5G NR module

4 Design of channel estimation module

Simulink saves the transmitter data to the Matlab work area. After the channel model is established in Matlab, the transmitted data is transmitted through the channel, and the received data is transmitted to the receiver model. This is convenient to facilitate Simulink simulation, as well as data validation and data processing. In Matlab, the modeling channel is Rayleigh channel[7]. The basic parameters are shown in the following table:

Parameter	Settings
Sample Rate	1024×120K
Path Delay	[0, 1.1e-8, 3.2e-8]
Average Path Gain	[1, 0.8, 2]
Max Doppler Shift	10Hz

Table 2: Parameter of Rayleigh channel

The objective of channel estimation is to estimate the effects of the channel and obtain information about its characteristics. Channel estimation is typically achieved by inserting known pilot symbols into the OFDM symbol sequence. In this system, the pilot positions are only present in the first OFDM symbol. The pilots are inserted starting from the first subcarrier and are spaced at intervals of one subcarrier. Using this pilot pattern, we have achieved parallel computation of channel estimation and noise variance estimation. The channel estimation process involves LS (Least Squares) estimation[8], TA (Time Alignment) compensation, and average interpolation. As for noise variance estimation, we employ an iterative algorithm for online calculation. The overall implementation is illustrated in Fig 3.

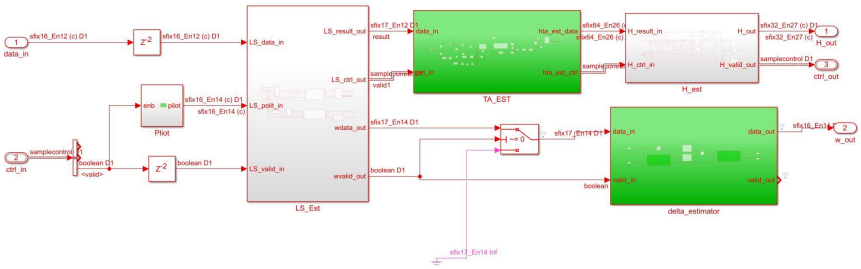

Fig.3: channel estimation module and noise variance estimation module

5 Design of receiver module

In the receiver, the pilot information is processed at first, the channel gain and noise variance are estimated, and the information is transmitted synchronously to the other 13 processes and cached in the process register. When each process needs channel information for channel balancing, the channel information is read out and synchronized with the data in the process[9]. This design also makes a synchronization protection mechanism, whether the process requests the channel information first, or the channel information arrives at the process first, will be cached in the synchronization area, so as to ensure the synchronization between data. The design is shown in Fig.4.

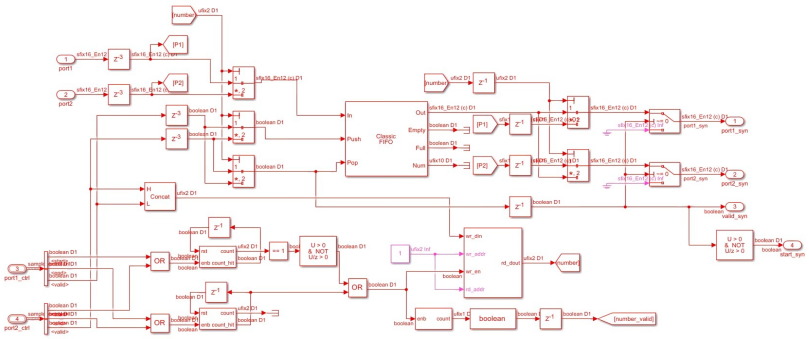

Fig.4: Process synchronous cache module

The receiver data successively passes through the following basic modules: process synchronous cache module, MRC module, soft demodulation data channel equalization module, de-interleaver module, LDPC rate matching module, frame format conversion module, LDPC decoder, transmission block format conversion module, CRC decoder.

The above module is packaged well, and the interface is configured, and the receiver is completed. The following figure shows the overall structure of the receiver. It can be seen that the receiver will be divided into processes after receiving data, and the pilot processing module will be connected to other process modules. After the other data modules are processed, they will be uniformly transmitted to Matlab for processing.

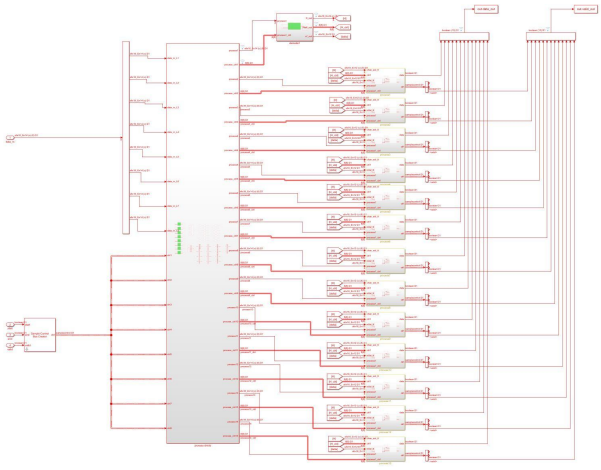

Fig.5: Receiver based on 5G NR module

6 Simulation result

In order to reduce simulink compilation time[10], complexity and data cache conflicts[11], this paper simulates 10 time slots each time, the process is repeated 10,000 times, and each re-simulation will change the channel, so as to simulate the real scene. The following figure shows the simulation results with 10 slots.

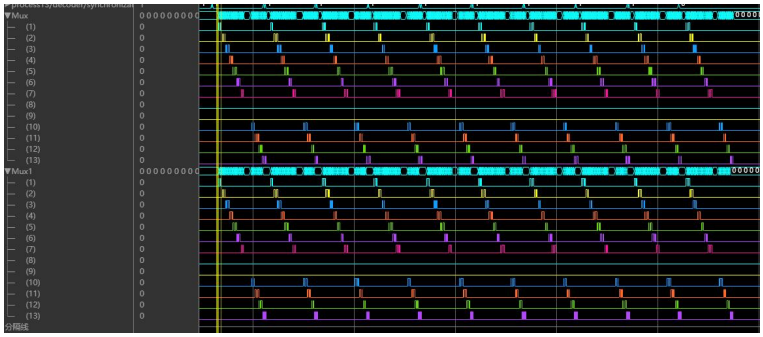

Fig.6: process decoder design

According to the established Rayleigh channel model, the BER curves under multi-path channels and AWGN channels under different paths and different SNRS are simulated in this paper. The result is shown in Figure 7. Table 3 is the parameter table of the multi-path channel, where type V parameter is the analog AWGN channel, and Figure 8 is the channel estimation of the receiver under the multi-path channel. It can be seen that the tracking performance of the receiver is very good, and the channel gain can be accurately estimated.

Type	Parameter	Settings
I	SNR	-5~10 dB
	Path Delay	[0, 1.1e-8]
	Average Path Gain	[1, 0.8]
	Max Doppler Shift	0Hz
II	SNR	-5~10 dB
	Path Delay	[0, 1.1e-8]
	Average Path Gain	[1, -1.8]
	Max Doppler Shift	10Hz
III	SNR	-5~10 dB
	Path Delay	[0, 1.1e-8, 3.2e-8]
	Average Path Gain	[1, 0.8, 2]
	Max Doppler Shift	0Hz
IV	SNR	-5~10 dB
	Path Delay	[0, 1.1e-8, 3.2e-8]
	Average Path Gain	[1, -1.8, 2]
	Max Doppler Shift	10Hz
V	SNR	-5~10 dB
	Path Delay	[0]
	Average Path Gain	[1]
	Max Doppler Shift	0Hz

Table 3: Parameter of multi-path channel

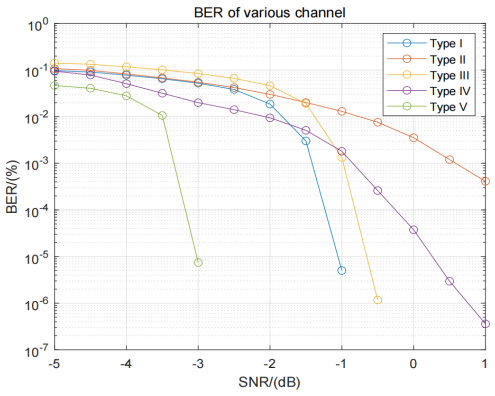

Fig.7: BER over multi-path channel

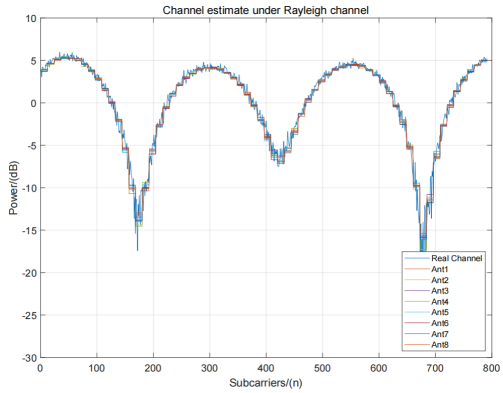

Fig.8: channel estimation over multi-path channel

Conclusion

In this paper, we mainly designed a communication transceiver based on HDL Coder under 5G NR standard, which is used as a reference for subsequent FPGA design. We propose a simulation workflow structure based on Matlab and simulink, which can monitor and process data more conveniently. The simulation results show that the communication transceiver designed by us can realize high reliability and low delay communication in multi-antenna system under AWGN channel and Rayleigh channel.

Although Simulink offers visual representation and automated code generation, we've encountered difficulties in crafting simulation files. Compiling a Simulink model, especially for a simplex communication system, proves time-intensive. To mitigate this, we've substituted some receiver components with MATLAB code, speeding up compilation and improving reproducibility. However, the primary aim of our paper is to visually bridge theory and practical hardware design, fostering seamless integration in both educational and real-world contexts.

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