Efficient Responsivity Enhancement of Surface-Illuminated InGaAs Avalanche Photodiode by Photon Trapping on the SOI Substrate

Rui Shao, Jishen Zhang, Kian Hua Tan, Satrio Wicaksono, Haiwen Xu, Yue Chen, *Graduate Student Member, IEEE*, Xuanqi Chen, *Graduate Student Member, IEEE*, Yuxuan Wang, *Graduate Student Member, IEEE*, Chen Sun, Qiwen Kong, *Graduate Student Member, IEEE*, Xuanyao Fong, *Member, IEEE*, and Xiao Gong

***Abstract*— The short-wave infrared avalanche photodiodes (SWIR-APDs) with high signal-to-noise ratio (SNR) and high bandwidth are essential components for optical interconnections and large-scale photonic integrated circuits (PICs). However, most surface-illuminated APDs rely on the use of a relatively thick absorber for high absorption efficiency, sacrificing the bandwidth and dark current. To address the challenge, we reported InGaAs APDs with a photon-trapping (PT) structure on the silicon-on-insulator (SOI) substrate using a ∼250-nm absorber, featuring a record-high responsivity of 0.75 A/W at unit gain with a wavelength of 1626 nm, equivalent to an external quantum efficiency (EQE) of 57.2%, and a low dark current of 51.3 nA at 90% of the breakdown voltage. A broad operation window from −4 to −24.1 V is achieved, with high detectivities of 9.34×10^{10} Jones at −4 V and 3.43×10^{12} Jones at −24.1 V. The work exhibits the dramatic advantage of the PT structure in photon responsivity enhancement with 2.5 times and the feasibility of InGaAs-based APD to integrate with silicon PICs, paving the way for high-efficiency and high-speed detectors targeting a broad range of emerging applications.**

***Index Terms*— Avalanche photodiode (APD), heterogeneous integration, photon-trapping (PT) structures, silicon photonic integrated circuits (PICs).**

Received 14 December 2024; revised 3 February 2025; accepted 19 February 2025. Date of publication 4 March 2025; date of current version 7 May 2025. This work was supported in part by the National University of Singapore (NUS) Semiconductor Trailblazer under Grant A-8002620-02-00, in part by Singapore Ministry of Education (MOE) Tier 2 under Grant MOE-T2EP50221-0008, and in part by MOE Tier 1 under Grant A 8001168-00-00 and Grant A-8002027-00-00. This article is an extended version of a paper presented at IEDM 2024. The review of this article was arranged by Editor M. Waltl. *(Corresponding authors: Jishen Zhang; Xiao Gong.)*

The authors are with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117582 (e-mail: jishen@u.nus.edu; elegong@nus.edu.sg).

Digital Object Identifier 10.1109/TED.2025.3544972

I. Introduction

THE significant expanding of short-wave infrared (SWIR) photonics in high-level automotive self-driving and high-performance computing (HPC) raises the urgent demand for high signal-to-noise ratio (SNR), large bandwidth, and energy-efficient receivers integrated into silicon platforms. The capability of the receivers to detect weak signals, sometimes down to a few photons, becomes vital in both free space and fiber links to meet the requirements for longer detection distance in ranging (LiDAR) applications [1] and to compensate for the increased insertion loss and propagation loss in a very large-scale integrated silicon photonic circuit [2]. Much effort and research have been made into avalanche photodiodes (APDs) attributed to their fast response and ultrahigh sensitivity down to single-photon levels due to their internal multiplication [3]. Various material platforms have been developed to improve the APD performance at SWIR wavelength, including germanium (Ge) [4], [5] and InGaAs [6], [7]. Ge-based APDs are dominantly adopted in on-chip silicon photonics because of their compatibility with CMOS fabrication to enable monolithic integration. However, the small energy bandgap of Ge and the large amount of dislocations at the Si/Ge interface make them usually possess a high dark current, dissatisfying the requirements of high SNR [8]. InAlAs has attracted much attention as the multiplication layer, which exhibits excellent advantages in suppressing dark current and extending gain-bandwidth-product owing to its higher avalanche triggering probability and relatively small excess noise [9].

InGaAs APDs with thin InAlAs multiplication layer thickness have been demonstrated to reduce the carrier transit time and dark current, achieving >40-GHz bandwidth [10]. However, conventional surface-illuminated APDs rely on thick absorption layers to achieve high photon responsivity [11]. This would inevitably bring in long carrier transit time and

severe dark current, leading to worse bandwidth and SNR. Despite the ease of reducing the thickness of the InAlAs multiplication layer, long carrier drift time from photocurrent in the thick absorption layer hinders further improvement of bandwidth and sensitivity. The laterally coupled APD could alleviate the dilemma of thinning down the absorption layer; however, such structure is limited by many applications [8]. The key challenge for the surface-illuminated APD is that photon absorption is proportional to the thickness of the absorber, meaning that a thinner absorber would cause a lower photon absorption length, which in turn weakens the SNR.

Various designs of resonant-cavity-enhanced (RCE) APDs have been reported to ease the tradeoff between bandwidth and absorption, such as using distributed Bragg reflectors (DBRs) [6], [12], [13]. In addition, the light-trapping structure has been introduced in the emerging detectors [14], [15], [16], [17]. Light manipulation in the lateral directions of the absorber can dramatically elongate the effective optical path, within a broad wavelength spectrum and incident angle insensitivity [18]. The recent investigation of the photon-trapping (PT) structure has been mostly exhibited on Si/Ge-based APDs [15], [19] using micro air holes, as well as AlInAsSb midwave infrared APDs using metal gratings [16]. To date, there are rare explorations about the PT design on InGaAs APDs for SWIR detection that can simultaneously meet the requirements of high photon responsivity and high bandwidth, as well as its integration on the silicon photonics, toward next-generation large-scale silicon photonic integrated circuits (PICs).

In this work, we proposed a novel design of thin InGaAs APDs with PT structures (PTAPDs) to enable high responsivity within a wide detection spectrum, with a theoretical projection for high-speed applications. The co-design of the heterogeneous integration on the silicon-on-insulator (SOI) platform was also carried out. To overcome the challenge of low photon absorption in thin absorbers and the difficulty in the integration of III–V compound materials on the SOI platform, we innovatively designed reverse-placed PT structures using 2-D photonic crystals (2-D PCs) and adopted a manufacturable bonding technology. The 2-D PCs were carefully tuned by optical and electrical simulations with optimized dimensions. Due to the comprehensive simulations and process optimization, our PTAPDs on the SOI substrate function with excellent performance. Initial results were reported in [9]. This article presents more comprehensive simulations and characterizations as well as more in-depth analysis of device physics in the optical and electrical domains.

II. Device Design, Simulation, and Realization

A. Design PTAPD on SOI Substrate

A 3-D schematic illustration of the InGaAs/InAlAs PTAPD on the SOI substrate and a cross section schematic of the separate-absorption-grading-charge-multiplication (SAGCM) layers in a unit cell are shown in Fig. 1(a) and (b), respectively. With the InAlAs-up–InGaAs-down structure, the high electric field in the InAlAs layer under reverse bias can be effectively confined far away from the edge surface of the PT structures, by forming reverse-placed, truncated-cone-shaped holes and

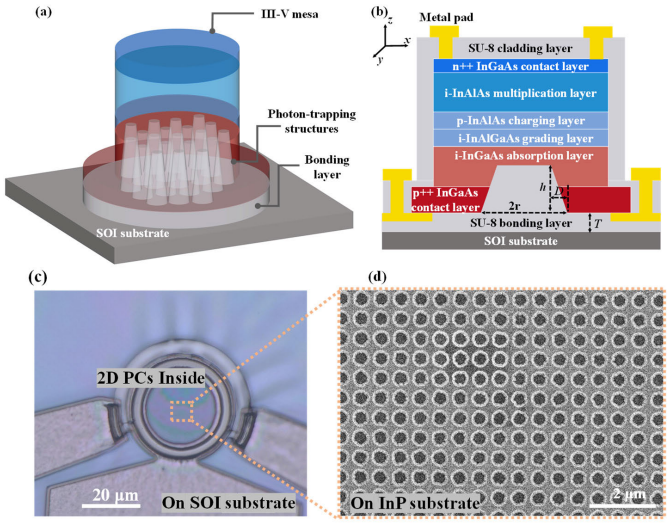

Fig. 1. (a) 3-D schematic illustration of the heterogeneously integrated InGaAs/InAlAs PTAPD on the SOI substrate. (b) Cross-sectional view of the unit cell of the device with III–V epilayer structures. (c) Microscopy image of the PTAPD on the SOI substrate. (d) SEM image of the inside 2-D PCs on the InP substrate. The SEM image was captured before bonding.

slanted sidewalls. Two-dimensional PCs with a rectangular lattice were designed at the bottom of the InGaAs absorber, where the PT effect can be achieved due to the existence of the lateral propagation mode in the thin InGaAs absorber once the light is incident from the top side of the device. A ~200-nm InAlAs multiplication layer and a ~250-nm InGaAs absorber were used in the work. Due to the periodic property of the PT structures, the unit cell of the device is defined by the period a (the distance between each cone), the radius r of the bottom circular base of the truncated cone, the etch depth h or the height of the truncated cone, the lateral etching distance D, and the SU-8 intermedia layer thickness T. The period a is the same in both the x- and y-directions for independent polarization. The microscope image of the mesa after bonding on the SOI substrate and scanning electron microscope (SEM) image of the PT structures before bonding on the InP substrate are shown in Fig. 1(c) and (d).

Regarding the incident light from the top surface of the device, the wave mainly propagates in the z-direction with wavevectors k_z. The photon absorption is mainly proportional to the thickness of the InGaAs absorber. Thus, the photon reflection from the bottom could enhance photon absorption. However, resonance in the z-direction would have a sharp spectral response and have no contribution to the wave propagation in the xy plane with wavevectors $k_{//}$, limiting the enhancement of absorption [17], [20]. The crucial issue is to couple incident light into the lateral propagation mode due to the much longer optical path in the xy plane of the absorber in comparison to the small thickness in the z-direction. In our design, diffraction gratings can be obtained by periodic refractive indices in the form of 2-D PCs. Once the incident light reaches the 2-D PCs in the InGaAs absorber, part of the diffracted light would be coupled to the lateral propagation mode. The light can be trapped in the z-direction

by complete internal reflection since the InGaAs absorber has a higher refractive index compared to the surrounding InAlAs and SU-8 layers [21]. In the *xy* plane, the transverse waves start to form and are determined by the 2-D PCs. The light inside the 2-D PCs is excited as Bloch waves and propagates laterally with much lower group velocity near the photonic bandgap edge [22]. Therefore, the light can be trapped in the InGaAs absorber in our design, significantly improving the absorption efficiency as compared to no PT structures. By engineering nanostructures in the InGaAs absorber, a sufficient long optical path can be generated in the lateral direction of the InGaAs absorber, independent of the thickness of the InGaAs absorber. Meanwhile, the electrical path within the device would not be affected, enabling a high-speed operation. Together with the reduced junction area by these nanostructures, the bandwidth of the APD can be effectively enhanced without any compromise of absorption efficiency. The III–V epilayers will be located on top of the SOI substrate through an SU-8 adhesive intermedia layer, which possesses the properties of low refractive index at SWIR, low dielectric constant, and chemical inertness.

B. Optical and Electrical Simulations

The finite-difference time-domain (FDTD) method was used to explore the optical field and the absorption at the InGaAs absorber. Because of the periodic 2-D PCs, only the unit cell of the PTAPD was included in the 3-D FDTD simulation region, incorporating periodic boundary conditions set in the *x*- and *y*-directions and perfectly matched layer (PML) set in the *z*-direction, as seen in Fig. 1(b). The normally incident plane wave illuminates the device in the conditions of TEM polarization and the electric field parallel to the *y*-axis. Optical absorption α in the InGaAs absorber in the unit cell is calculated by integrating the loss function over the volume, which is expressed by

$$\alpha = \frac{1}{2}\iiint_{V_{\mathrm{InGaAs}}} \mathrm{Re}(\nabla \cdot \mathbf{P}) dV \tag{1}$$

where $\mathbf{P}$ is the Poynting vector, and V_{InGaAs} is the volume of the InGaAs absorber. Accordingly, we can get the responsivity R of the PTAPD by

$$R = \frac{I_{\mathrm{ph}}}{P_{\mathrm{in}}} = \alpha\eta\frac{e}{hf} \tag{2}$$

in which I_{ph} is the photocurrent, P_{in} is the input optical power, η is the internal quantum efficiency (here, we define it as 1 in the simulation), e is the elementary charge, h is the Planck constant, and f is the frequency of the light.

The optimized parameters of the nanostructures are a = 625 nm, r = 250 nm, h = 220 nm, D = 80 nm, and T = 300 nm. These parameters were carefully determined through a combination of simulations and practical fabrication constraints. The lateral etching distance and SU-8 thickness were determined by fabrication considerations, such as ensuring compatibility with dry etching processes for III–V compounds and achieving stable heterogeneous integration. The etch depth was optimized first due to its significant influence on both optical and electrical performance. Following this, a simultaneous sweep of the period and radius was conducted at the optimized etch depth to reach the maximum absorption. The simulated responsivity versus wavelength calculated by (1) and (2) is shown in Fig. 2(a). The PTAPD shows a large enhancement of responsivity in a wide spectrum from 1520 to 1630 nm compared to the APD without PT structures. A maximum peak responsivity reaches 0.87 A/W at a wavelength of 1615 nm. The normalized electric field intensity distribution in the *xz* plane at 1615 nm is plotted in Fig. 2(b). Multiple lateral resonance peaks were observed around the PT structure at the i-InAlAs and i-InGaAs layers. A relatively strong resonance mode is located at the center of the InGaAs absorber. Weaker resonance modes are also formed close to the bottom of the InGaAs absorber. To ensure high photon absorption, the coupling efficiency from normal incident light to lateral propagation mode light should be as high as possible, which is determined by the geometry of the PT structure. Simultaneously, large fractional mode intensity inside the InGaAs absorber should be ensured, which is controlled by the etch depth h. If h is too small, only part of the mode intensity stays inside the InGaAs absorber, leading to much lower photon absorption. On the other hand, if h is too high, part of the multiplication layer would be etched. This would bring in a high electric field at the nanostructure edge, causing field-related dark current and premature breakdown. To further investigate the mechanism of the light propagation in the complex III–V epilayers with 2-D PCs, the transient time evolution from time t = 24.8, 26.8, 29.8, and 31.8 fs is simulated. The field intensity distributions from the bottom 220-nm silicon layer to the top III–V epilayers in the *xz* plane are illustrated in Fig. 3(a)–(d). Lateral waves appear around the bottom edge of the 2-D PC, and subsequently, lateral resonance modes start to form from the bottom side to the top side over time.

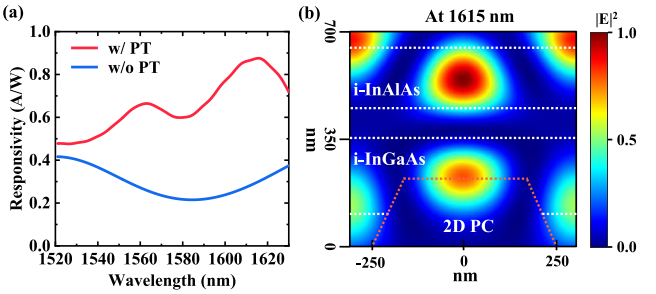

Fig. 2. (a) Simulated responsivity as a function of wavelength, with the red line for the PTAPD and blue line for the control device without PT structures. (b) Optical mode profile in the III–V epilayers at the *xz* plane. The red dashed lines indicate the position of the 2-D PC. The white dashed lines indicate the InAlAs multiplication layer and InGaAs absorption layer.

Except for the photon absorption in the optical domain, 2-D PCs also influence the E-field distribution under reverse bias in the electrical domain. TCAD electrical simulations were conducted to comprehensively understand the electrical performance. To ensure rapid convergence around the holes, three cylindrical holes were included in the 2-D simulation region. The optimized geometry parameters from the optical

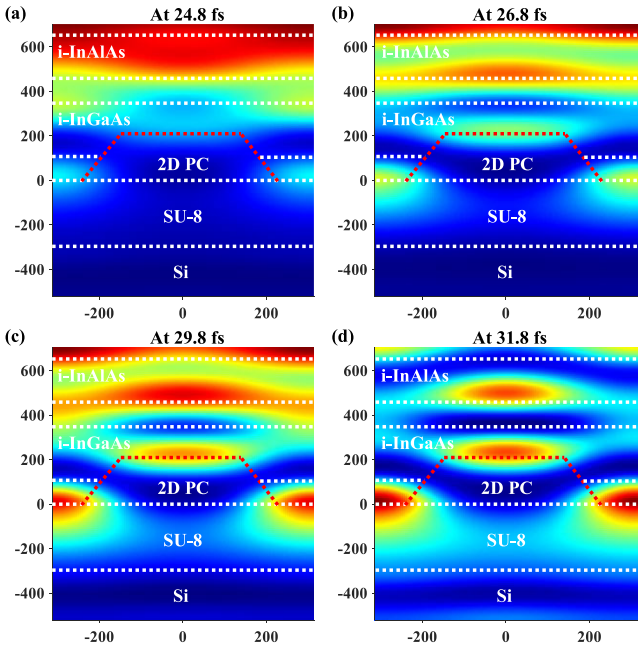

Fig. 3. Transient time evolution of the optical mode profile in the *xz* plane at (a) 24.8, (b) 26.8, (c) 29.8, and (d) 31.8 fs. The input light source was positioned 550 nm above the device in the simulation. The simulation time was recorded starting from the moment the input source was activated. The unit of *x*- and *z*-axes is nanometer. The field intensity is normalized and squared, mapping to the color ranging from blue to red. The layer structures from the bottom SOI substrate to the top III–V epilayers are indicated by the white dash lines. The inside 2-D PC is represented by the red dashed lines.

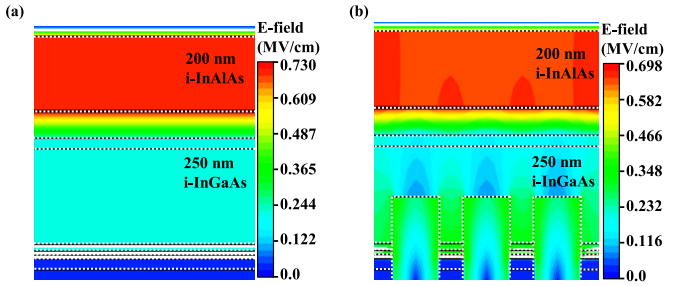

Fig. 4. *E*-field distribution of the devices for (a) control APD without PT structures and (b) PTAPD, both under a reverse bias of 23.8 V without illumination. Each III–V layer and PT structures are indicated by the white dashed lines. Only cylindrical 2-D PCs are modeled in the simulation to enable rapid convergence. The maximum *E*-fields at the i-InAlAs layer are 0.730 MV/cm for the control APD and 0.682 MV/cm for the PTAPD.

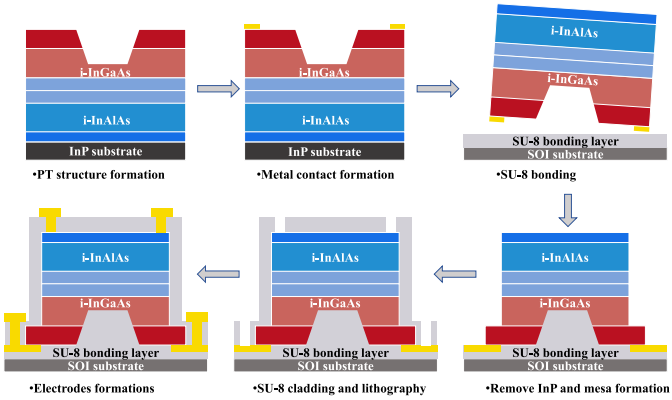

Fig. 5. Schematic illustrations of key fabrication processes, consisting of 2-D PC and metal formations, bonding of III–V on the SOI substrate, InP substrate removal, PTAPD mesa formation, SU-8 cladding, and electrode formations. Details of III–V epilayers are not stated here.

simulations ($a = 625$ nm, $r = 250$ nm, and $h = 220$ nm) are applied. Fig. 4(a) and (b) presents the 2-D *E*-field distributions of the APDs with and without PT structures in the *xz* plane under a breakdown voltage. Moderate *E*-fields in the InAlAs multiplication layer and the InGaAs absorption layer were initially achieved in Fig. 4(a) by optimizing the charging layer thickness and doping concentration when considering no PT structures. Concentrated high *E*-field primarily within the InAlAs layer enhances impact ionization rate for avalanche breakdown. Introducing PT structures generates enhanced *E*-field peaks confined around the edges of 2-D PCs, while the *E*-fields at the top base of the 2-D PCs are significantly reduced in Fig. 4(b). The *E*-field in the InAlAs multiplication layer is generally uniform with a slight reduction of the *E*-field above the top base of the 2-D PCs. By proper engineering of the PT structure geometry, especially the etch depth, the *E*-field peaks can be efficiently flattened to reduce the field-related tunneling leakage current and avoid premature breakdown. Additionally forming slanted sidewalls in the etched III–V epilayers can be adopted to suppress leakage current induced by 2-D PCs.

C. Device Fabrication

The key fabrication steps are illustrated in Fig. 5. Initially, the SAGCM III–V epitaxial layers were grown on an InP substrate by using a molecular-beam epitaxy (MBE) system. Low-temperature plasma-enhanced chemical vapor deposition (PECVD) SiO_2 was used as the hard mask to pattern PT structures. A desired depth and slanted sidewalls were achieved by using electron beam lithography (EBL) and the subsequent depth-controlled Ar/Cl_2-based reactive ion etching (RIE). Then, the W electrode was formed as the bottom electrode by sputtering and lithography. After that, the III–V die was then bonded in a flip-chip manner on the SOI substrate through an SU-8 adhesive intermedia layer in the condition of 80 N/cm^2 at a temperature of 150 °C for 30 min. It is worth mentioning that the SU-8 layer thickness was optimized by diluting the concentration of SU-8 and controlling the bonding force and time to be consistent with the optical simulation. The InP handle substrate was then removed using the concentrated HCl. The InGaAs etch-stop layer was partially etched to reduce the undesired absorption during the measurement. Subsequently, the top contact electrode was deposited followed by the mesa etching using $H_3PO_4/H_2O_2/H_2O$ solution to minimize the surface defects. The device was finally passivated by the SU-8 cladding layer.

Fig. 6(a) displays the SEM image of the cross-sectional PTAPD with the SU-8 cladding layer on the SOI substrate. Periodic reverse-placed and truncated-cone-shaped holes are clearly shown. The zoom-in SEM image in Fig. 6(b) demonstrates the whole layer structures, which from bottom to top are SOI substrate, SU-8 adhesive layer, III–V epilayers, and SU-8

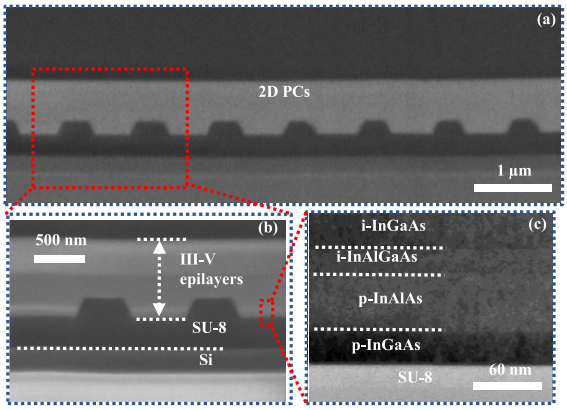

Fig. 6. (a) SEM image of the cross-sectional PTAPD on the SOI substrate along the diagonal direction of the 2-D PCs with a rectangle lattice. (b) Zoom-in SEM image of the 2-D PCs, with white dashed lines indicating each layer. (c) Zoom-in SEM image at the SU-8 and III–V epilayer interface. Smooth and flat interface at the SU-8 and p-InGaAs layers are observed.

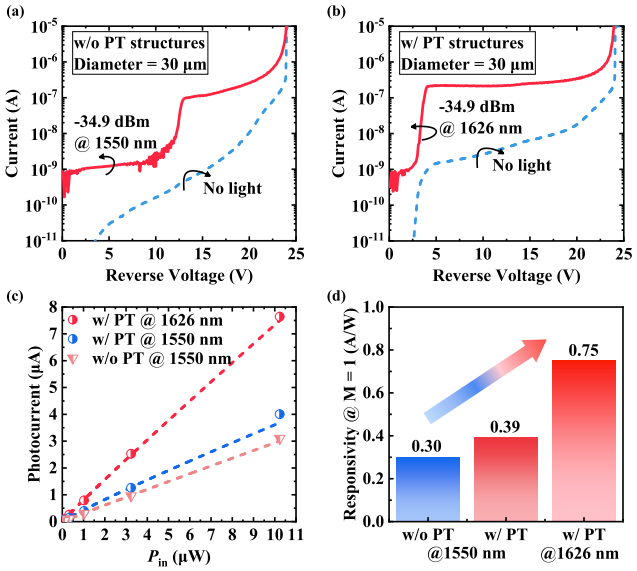

Fig. 7. *I–V* characteristics of (a) control APD without PT structures and (b) PTAPD under no light and light illuminance. The blue dashed line indicates the dark current under reverse bias. The red solid line indicates the current under a light intensity of −34.9 dBm. (c) Photocurrent as a function of input light power at wavelengths of 1550 and 1626 nm. (d) Extracted responsivity at unit gain for the control APD and PTAPD. 2.5 times enhancement of responsivity is achieved for the PTAPD at 1626 nm.

cladding layer. Smooth slanted sidewalls with a lateral distance of about 77 nm are observed. Fig. 6(c) gives the zoom-in SEM image at the interface between SU-8 and p-InGaAs, confirming well-controlled layer thicknesses and elemental compositions using MBE. A smooth III–V surface and flat SU-8 bonding layer are exhibited as well.

III. Device Characterization and Discussion

A. Electrical and Optical Characterization

The current–voltage (I–V) characteristics of the control APD without PT structures and the PTAPD with a mesa diameter of 30 μm were measured under no light and light illumination, as depicted in Fig. 7(a) and (b). Normal-incident light with a 10° angle illuminates the active region of the devices through a single-mode lensed fiber with a 10.4 μm diameter. The fiber was close and aligned to the center of the PT structures when measuring the PTAPD. The area of the 2-D PCs with a 20 × 20 hole array is 12.5 × 12.5 μm^2. To enable the fiber to fully focus on the 2-D PC active region, an autoalignment step was conducted by the ultrahigh-precise alignment station until the photocurrent reached the maximum. The avalanche breakdown voltages V_{br} and punchthrough voltages $V_{punch\text{-}through}$ of the control APD and PTAPD are −24.0 and −12.8 V and −24.2 and −4 V, respectively. A largely reduced $V_{punch\text{-}through}$ of the PTAPD is attributed to a partially high E-field at the edge surface of 2-D PCs, driving photogenerated carriers in the InGaAs absorber injected into the multiplication layer, which is consistent with the electric field simulation in Fig. 4(b). The dark currents of the control APD and PTAPD at 90% V_{br} are 16.9 and 51.3 nA. The effective suppression of field-related tunneling dark current induced by 2-D PCs was achieved through proper design of the geometry and fabrication optimization.

The optical response current characteristics of the control APD and PTAPD were measured by varying the input power from 0.1023 to 10.23 μW at the wavelengths of 1550 and 1626 nm, as seen in Fig. 7(c). The steady-state responsivity at a unit gain ($M = 1$) was extracted by (2) and is plotted in Fig. 7(d). Our PTAPD reaches 0.75 A/W at a unit gain, 2.5× at 1626-nm and 1.3× at 1550-nm enhancement of the responsivity in comparison to the control APD at 1550 nm. Fig. 8(a) plots the relationship between the photocurrent and input optical power at different voltages near V_{br}. Over 100 multiplication gain is achieved when the input power is below 0.1 μW at a reverse voltage of 24 V. Besides, high detectivities of 9.34 × 10^{10} Jones at −4 V and 3.43 × 10^{12} Jones at −24.1 V were achieved with a broad voltage operation window from −4 to −24.1 V.

To further understand the light propagation inside the PT structures, the responsivities at different wavelengths for the control and PTAPD were extracted and illustrated in Fig. 8(b). The curve of the PTAPD exhibits a rapid increase from 1520 to 1630 nm, reaching a maximum peak responsivity at 1626 nm. However, the control APD shows a relatively flat curve, where the responsivity is slightly influenced by the wavelength, similar to the simulated spectrum response in Fig. 2(a). The possible reasons for the difference between the measured and simulated spectrum response in the PTAPD are imperfect 2-D PCs due to variations from exposure dose in EBL and etching inconsistencies in RIE and a finite number of 2-D PCs. At smaller wavelengths, the coupling efficiency from the top-illuminated light to lateral propagated light is reduced. Additionally, unintended light absorption at the high doping concertation region occurs in the active region. Fig. 8(c) and (d) shows the responsivity spectrum when sweeping the period a and etch depth h, highlighting the tunable responsivity spectrum capability of PTAPDs. Besides, the absorption enhancement is governed by the PT effect,

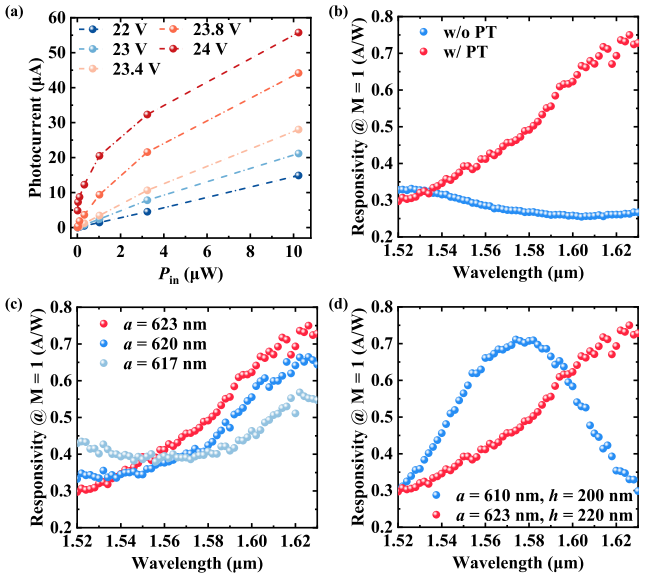

Fig. 8. (a) Photocurrent versus input light power under different reverse biases. Over 100 multiplication gain is achieved at a reverse bias of 24 V. (b) Responsivity spectra for the control APD and PTAPD from 1520 to 1630 nm. A maximum peak of 0.75 A/W at 1626 nm for the PTAPD is obtained. (c) Responsivity spectra of the PTAPDs at different periods. (d) Responsivity spectra of the PTAPDs at different periods and etch depths.

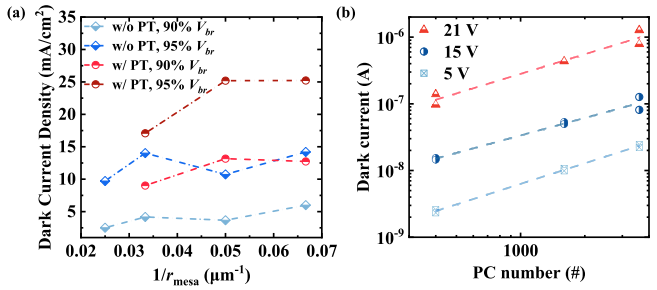

Fig. 9. (a) Relationship between the dark current density and one of the mesa radii for the control APD and PTAPD under reverse biases of 90% V_{br} and 95% V_{br}. (b) Dark current as a function of the number of PC in the log scale under reverse biases of 5, 15, and 21 V.

as evidenced by the tunability of the absorption peak with the changes in PC geometry [Fig. 8(c) and (d)] and the broad peak spectral response, both of which are the hallmarks of the PT effect.

B. Dark Current Analysis

To further investigate the leakage mechanism in PTAPDs, we extracted the dark current density J_{dark} versus one of the mesa radius $1/r_{mesa}$ under 90% V_{br} and 95% V_{br} and analyzed the effect of 2-D PC area on the dark current, as depicted in Fig. 9(a) and (b). For conventional APDs, the dark current mainly comes from the bulk and surface leakage currents due to material defects at the bulk and mesa surface. The total dark current density J_{dark} in a circular APD can be expressed by

$$J_{dark} = J_{bulk} + \frac{2J_{surface}}{r_{mesa}} \tag{3}$$

where J_{bulk} and $J_{surface}$ mean the bulk and surface leakage current density, respectively [23]. When PT structures are formed inside the bulk region, J_{bulk} changes accordingly. To simplify the calculation, we assume that the distribution of the electric field is abruptly changed at the border of the PT structures. Considering PT structures, the modified bulk dark current density J'_{bulk} can be represented by

$$\begin{aligned} J'_{bulk} &= \left(1 - \frac{A_{PT}}{\pi \cdot r_{mesa}^2}\right) \cdot J_{bulk} + \frac{A_{PT}}{\pi \cdot r_{mesa}^2} \cdot J_{PT} \\ &= J_{bulk} + \frac{A_{PT}}{\pi \cdot r_{mesa}^2}(J_{PT} - J_{bulk}) \end{aligned} \tag{4}$$

where A_{PT} means the area of PT structures and J_{PT} is the dark current density in the 2-D PC area. In this equation, the term J_{PT} is defined as the average increased dark current density induced by the photonic crystal structures. Due to the relatively minor influence of geometrical parameters, such as period and radius on dark current—compared to other dominant contributors, such as bulk dark current density and mesa surface dark current density—we treated J_{PT} as an averaged value across the photonic crystal region. This simplification is reasonable because variations in geometrical parameters (e.g., period and radius) are on the few nanometer scale, which is negligible compared to the overall device dimensions in the tens of micrometer range. Thus, the dark current contribution from these small geometrical variations is significantly smaller than the variations arising from other sources of dark current. PTAPDs show a large intercept and strong 2-D PC area dependence on dark current, indicating perimeter leakage current at the 2-D PC area is the dominant leakage source at high reverse bias. This is related to the partially E-field peaks around the 2-D PC edges, as explained in the electrical simulations in Fig. 4(b). It is worth noting that when the 2-D PC area ($12.5 \times 12.5\ \mu m^2$) is comparable to the mesa area ($r_{mesa} = 15\ \mu m$), there is a slight drop in dark current density in Fig. 9(a). A possible reason is that E-field peaks at the mesa edge are reduced by the center 2-D PCs, leading to a reduced surface leakage current, especially at a high reverse bias. Therefore, by reducing the 2-D PC area to the size of the illumination spot from the fiber, the dark current density can be efficiently suppressed without sacrificing the photon responsivity.

In addition, the temperature dependence of reverse current was investigated from 240 to 320 K in Fig. 10(a) and (b). The dark current increases slightly with the increase in temperature due to more severe thermal generation in both PTAPD and the control APD. To understand the leakage generation mechanism in the PTAPD, the $\ln(I_{dark}/T^{3/2})$ versus 1/kT was extracted and plotted in Fig. 10(c) and (d) at biases of 10 and 20 V, respectively, for both APDs [7]. The activation energy E_A at a bias of 10 V for the PTAPD and the control APD is comparable (0.32 and 0.30 eV, respectively), while a slightly smaller E_A (0.11 eV) is obtained in the PTAPD at a bias of 20 V. This suggests that, generally, the leakage current remains stable with the introduction of 2-D PCs, while the tunneling-related generation of dark current becomes more prevailing in PTAPDs at higher reverse biases.

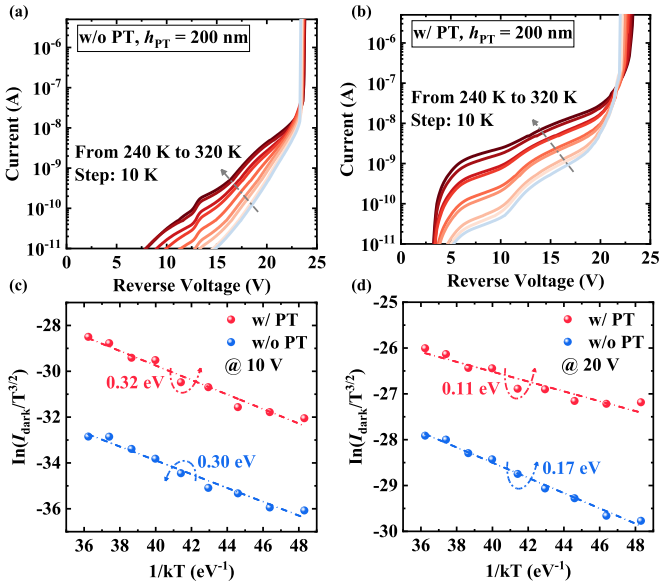

Fig. 10. Temperature dependence of *I*–*V* characteristics from 240 to 320 K with a step of 10 K for (a) control APD and (b) PTAPD with a etch depth of 200 nm. (c) Arrhenius plot of the control APD and PTAPD at a reverse bias of (c) 10 and (d) 20 V. The slope indicates the activation function E_A. The control and PTAPD show 0.30 and 0.32 eV at 10 V and 0.17 and 0.11 eV at 20 V, respectively.

TABLE I
BENCHMARK OF DEVICE MATERIAL, STRUCTURE, DARK CURRENT, DARK CURRENT DENSITY, GAIN, AND RESPONSIVITY AMONG REPORTED SURFACE-ILLUMINATED APDS

Ref.	Material	Substrate	Structure	Dark current (nA)	Dark current density (mA/cm^2)	Multiplication Gain	Responsivity (A/W)
[19]	Ge/Si	Si	700 nm absorber with PT	1E6 @ 97% V_{br}	3.53E4	21	0.32 @ 1550 nm
[24]	Ge/Si	SOI	1.03 μm absorber	~2E3 @ 95% V_{br}	2.83E2	40	0.3 @ 1550 nm
[25]	Ge/Si	SOI	-	900 nA @ 90% V_{br}	2.86E2	10	0.55 @ 1310 nm
[26]	InGaAs /InAlAs	Si	1.1 μm absorber	261 nA @ 95% V_{br}	83.1	21	0.54 @ 1550 nm
[27]	InGaAs /InAlAs	InP	570 nm absorber	110 nA @ 90% V_{br}	35.0	>100	0.51 @ 1310 nm
[16]	AlInAsSb	GaSb	200 nm absorber with PT	230 nA @ 95% V_{br}	46.8	>100	0.35 @ 2000 nm
This work	InGaAs /InAlAs	SOI	250 nm absorber with PT	51.3 nA @ 90% V_{br}	7.3	>100	0.39 @ 1550 nm 0.75 @ 1626 nm

C. Benchmark

Fig. 11 presents the simulated external quantum efficiency (EQE) as a function of the InGaAs absorber thickness. Our device without PT structures matches well with the simulation data. The PTAPD shows a significant enhancement of EQE (2.86×), comparable to a conventional APD with a 1.1-μm InGaAs absorber. Table I benchmarks the key metrics of reported surface-illuminated APDs at telecommunication wavelengths, including conventional Ge-on-Si APDs [19], [24], [25], InGaAs-based APDs on various substrates [26], [27], and AlInAsSb APDs with PT structures [16]. Our PTAPD shows outstanding performance in terms of responsivity, multiplication gain, and dark current despite utilizing thin InGaAs/InAlAs layers on the SOI substrate.

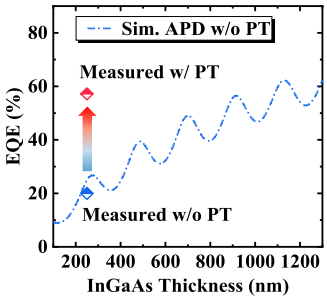

Fig. 11. EQE as a function of the InGaAs absorber thickness at 1626 nm for the simulated APD without PT structures marked in the blue dashed-dotted line and measured PTAPD and the control APD marked in dots.

IV. CONCLUSION

In summary, InGaAs PTAPDs on the SOI substrate have been presented with the effectiveness of PT structures. The large-scale manufacturable integration method, together with optical and electrical simulations, enables high-performance InGaAs PTAPDs, including 2.5 times enhancement of responsivity, low dark current, high multiplication gain, and excellent detectivity. The potential to engineer the punchthrough voltage and capability to tune the wavelength of peak absorption has also been demonstrated by changing the PT structures. The comprehensive analysis and characterization of the devices were conducted to have an in-depth understanding of the device physics in both electrical and optical domains. We believe this presents a significant milestone in the development of InGaAs APDs for future optoelectronic integrated circuits.

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