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Document Version
Publisher's PDF, also known as Version of record

Publication date:
1996

[Link to publication in University of Groningen/UMCG research database](#)

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A ferroelectric transparent thin-film transistor

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Operation is demonstrated of a field-effect transistor made of transparant oxidic thin films, showing an intrinsic memory function due to the usage of a ferroelectric insulator. The device consists of a high mobility Sb-doped n-type SnO_2 semiconductor layer, $PbZr_{0.2}Ti_{0.8}O_3$ as a ferroelectric insulator, and $SrRuO_3$ as a gate electrode, each layer prepared by pulsed laser deposition. The hysteresis behavior of the channel conductance is studied. Using gate voltage pulses of 100 μs duration and a pulse height of ± 3 V, a change of a factor of two in the remnant conductance is achieved. The dependence of the conductance on the polarity of the gate pulse proves that the memory effect is driven by the ferroelectric polarization. The influence of charge trapping is also observed and discussed. © *1996 American Institute of Physics.* [S0003-6951(96)01025-X]

Field-effect transistors with a ferroelectric insulator have been the subject of numerous studies because of their memory function and non-destructive readout properties. Early works used a thin film of semiconductor material deposited on a bulk ferroelectic substrate.[1] Since the seventies the research has been focused on integration with IC technology,[2,3] where a ferroelectric thin film is deposited on a semiconductor substrate. Only very recently the fabrication of a ferroelectric thin-film transistor has become feasible, where the ferroelectric as well as the semiconductor material are deposited as thin films.[4–7] Although this approach is technologically more demanding, it offers the advantage of flexibility with respect to the choice of substrate. In particular, the usage of an optically transparent substrate in combination with wide bandgap materials for the thin-film transistor gives interesting opportunities for optical applications, e.g. as on-screen electronic devices in displays, projectors and cameras.

In this letter, we report on the operation of a ferroelectric transparent field-effect transistor realized completely in oxidic thin films. The gate insulator is composed of a ferroelectric Pb(Zr,Ti)O$_3$ thin film, while the semiconductor channel consists of an antimony doped n-type SnO_2 film. Measurements are performed at ambient temperature and pressure. The device construction is illustrated in Fig. 1. The layers were deposited on a SrTiO$_3$ (100) substrate by pulsed laser deposition with the off-axis technique.[6,8] First, a 140-nm SrRuO$_3$ layer was grown and subsequently patterned by reactive ion etching in order to form the gate structures. Thereafter, in a single run 160 nm PbZr$_{0.2}$Ti$_{0.8}$O$_3$ and 110 nm SnO$_2$:Sb were deposited. By reactive ion etching, the semiconductor channels were defined and contact holes were made to the buried gates. Ferroelectric Pb(Zr,Ti)O$_3$ finds wide application (e.g. Refs. 9 and 10) due to its large remnant polarization (of the order of 10 μC cm^{-2}) and low

coercive field strength (between 10 and 10^2 kV/cm). The semiconductor material is doped with 220 μg antimony per gram of SnO$_2$ (equivalent to a dopant concentration of 8 $\times 10^{18}$ cm^{-3}) and shows a textured (111) structure with a grain size of 30–60 nm. SnO$_2$ is a transparent semiconductor with an electron mobility as high as 240 cm^2 V^{-1}s^{-1} for bulk material.[11,12] However, in thin films the reported mobilities are about an order of magnitude lower,[11,13] a phenomenon associated with the presence of grain boundaries. The semiconductor material used for the transistor channel has a resistivity of the order of 1 Ω cm. We verified that the resistivity of undoped SnO$_2$ films is more than three orders of magnitude higher; hence, the free carrier density in our films is entirely supplied by the antimony dopant atoms. The negative temperature dependence of the resistivity confirmed the semiconductive character of the SnO$_2$. Hall measurements showed n-type conductivity, a carrier concentration of

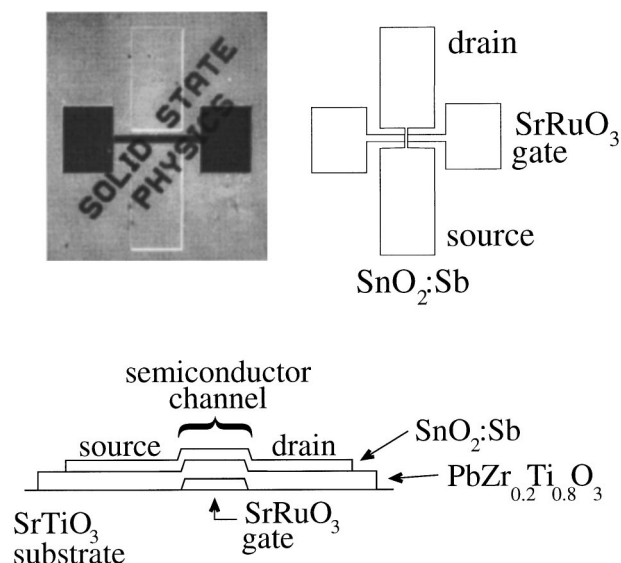FIG. 1. Picture and sketch of the transistor (top view and cross sectional view). The picture shows the text 'solid state physics' that is read *through* the device, so seen through the thin-film device and the SrTiO$_3$ substrate with a thickness of 1 mm. The picture was taken with interference contrast, in order to visualize the edges of the thin films. The picture size is 1.4 mm $\times$ 1.8 mm.
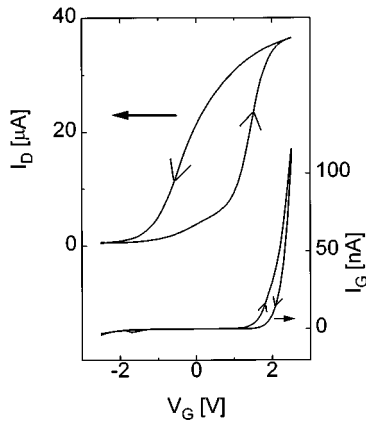
FIG. 2. Drain current (I_D) and gate current (I_G) vs gate voltage (V_G). The gate voltage was swept at a rate of 2 V/s. Note the difference in the scales. The drain was at 100 mV with respect to the source. In this device, the distance between the source and drain contacts (L) is 5 μm and the channel width (W) is 300 μm.

FIG. 3. Switching levels of the drain current, upon the application of gate voltage pulses with a pulse height of ± 3V and a duration of 100 μs. V_D =100 mV. For a device with L=10 μm and W=300 μm.

about 10^{18} cm^{-3}, and a mobility of 5 cm^2 V^{-1}s^{-1}. The latter value is still fairly high for a thin-film transistor. In another paper[14] we will present a detailed study on the electronic properties of SnO$_2$ as a function of doping concentration. Figure 1 shows a sketch of the device construction, while the picture illustrates the optical transparency of the transistor. In the channel area of the present structure, the optical absorption (tens of percents) is due to the gate electrode layer of SrRuO$_3$. By fabricating an all-oxide thin-film transistor with heavily doped SnO$_2$ for the gate electrode, we verified that the realization of a fully transparent thin-film transistor is possible.

Figure 2 shows the measured drain current (I_D) and the gate current (I_G) as a function of the gate voltage. Note that the current leaking through the ferroelectric insulator is more than two orders of magnitude smaller than the drain current, demonstrative of a proper transistor operation. By changing the band bending in the semiconductor, the gate voltage causes the drain-source channel conductance to be larger at a positive gate voltage (forward bias, channel enrichment) than at a negative gate voltage (reverse bias, channel depletion). As Fig. 2 shows, a change of the channel conductance is achieved of a factor of $I_{max}/I_{min}=36$ μ A/0.6 μA=60. This can be understood as follows. For a constant density of space charge eN_d, the width of the depletion region in the semiconductor is given by $[2\epsilon_0\epsilon_r V_{bb}/eN_d]^{1/2}$,[15] where V_{bb} is the band bending potential. If we assume that the full gate voltage sweep induces a change of the band bending $V_{bb}\simeq 4$ V and using a carrier concentration $N_d=10^{18\pm0.5}$ cm^{-3}, we find a change of the depletion width of 80 ± 40 nm ($\epsilon_r\simeq10$). In other words, the large change of channel conductance is due to the fact that the change of the depletion width is comparable to the thickness of the semiconductor channel.

The memory function of this thin-film transistor is demonstrated by the hysteresis behavior of the drain current.[16] The remnant channel conductance, i.e. the conductance at zero gate voltage, depends on the history of the gate voltage: the remnant conductance is large when a positive gate voltage has been applied (on-state) and small after a negative voltage (off-state). This proves that the memory effect is
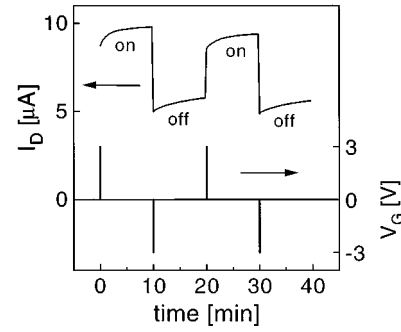
driven by the ferroelectric polarization, and is not a result of the injection of charge into the insulator layer (this issue is discussed in detail in Refs. 2 and 4). The voltage shift between the up-sweep and down-sweep is 1.6 V. This should be compared with $2d_f E_c$, where d_f is the thickness of the ferroelectric layer and E_c its coercive field. Using d_f=160 nm, we find a coercive field of 50 kV/cm. In order to verify that the hysteresis is due to the field effect, we measured the charge collected on the gate electrode as a function of the gate voltage (not shown) in a Sawyer-Tower measurement[17]; this revealed a hysteresis behavior with a remnant charge density of 10 μC cm^{-2}.

The switching characteristics of the transistor are depicted in Fig. 3, showing the time evolution of the remnant conductance of the source-drain channel. Gate voltage pulses with a duration of 100 μs and a pulse height of ± 3 V were used. A switching is observed with an on/off ratio close to a factor of 2.[18] This can be compared with previous achievements in ferroelectric thin-film transistors: Seager et al.[4] observed a memory effect that was dominated by charge injection and opposite to the ferroelectric polarization, while Watanabe[5] showed a polarization-type memory effect of 5%, with gate voltage pulses of 7-V amplitude and 10-ms duration. We observed a substantial decrease of the on/off ratio with pulses shorter than 10 μs. This is not due to the ferroelectric material, because in Pb(Zr,Ti)O$_3$ the switching of polarization takes place on a nanosecond time scale.[19] A speed limitation is given by the RC switching time constant, that is the product of the source-drain channel resistance ($\sim$ 10 kΩ) and the gate capacitance ($\sim$ 0.3 nF). The theoretical limit to the device speed is given by $L^2/V\mu$,[15] where L is the channel length, V is the applied voltage, and μ is the carrier mobility. As an example, using one volt, a mobility of 10 cm^2 V^{-1}s^{-1}, and a channel length of 1 μm, a switching speed of 1 ns should be possible.

In addition to the switching behavior, a relaxation of the on-state and the off-state is observed in Fig. 3. The relaxation is of equal direction for the two states (toward a higher conductance) and the relaxation is of similar magnitude. It is well-known that the polarization of ferroelectric materials is partially volatile.[10] However, a ferroelectric relaxation would lead to a reduction of the on-state conductance and an increase of the off-state conductance with time, in contrast to what is recorded in Fig. 3; in addition, we also observed the

Appl. Phys. Lett., Vol. 68, No. 25, 17 June 1996

Prins et al.   3651

relaxation for low voltages, when the ferroelectric material is hardly switched (low on/off ratio). Our observations point to the presence of electron trap states, that are filled by the gate current pulse. During the relaxation process, the liberation of trapped electrons leads to an increase of the free carrier density in the n-type channel. We verified experimentally that gate pulses of longer duration give stronger relaxation effects, as is expected for an increased amount of trapped charge. Also, the relaxation time decreased upon illuminating the sample with photons of sub-bandgap energy, which is another indication that gap states are involved. The trap states may be related to the inactive fraction of dopant atoms, or to structural defects at the grain boundaries in the semiconductor thin film.[20] Summarizing, we have demonstrated the operation of an all-oxide transistor with the following features: (i) an all-thin-film design, (ii) the incorporation of a high mobility semiconductor like SnO_2, (iii) an inherent memory function due to a ferroelectric insulator, (iv) a low switching voltage, and (v) optical transparency.

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