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We present a study of electrical characteristics of ferroelectric field-effect transistors made of $PbZr_{0.2}Ti_{0.8}O_3$ and SnO_2:Sb thin films. Due to properly chosen semiconductor parameters, the transistor channel can be totally depleted by the ferroelectric charge displacement. The observed remnant on/off ratio of the channel current amounts to 7×10^3. Pulse response measurements give information on data retention, device speed, and the occurrence of charge injection. The results lead to important design considerations for ferroelectric transistors. © *1997 American Institute of Physics.* [S0003-6951(97)04204-6]

Recent years have shown an increasing effort in the development of electronic devices utilizing complex oxidic thin films.[1] From the point of view of physics and materials technology, one of the most challenging devices is the thin-film field-effect transistor with a ferroelectric insulator. Its nonvolatile ferroelectric polarization, low programming voltage, and nondestructive readout make the ferroelectric transistor interesting for memory applications. Recently, considerable progress has been made with thin-film depletion-type transistors.[2,3] However, total depletion of the semiconductor channel has not been achieved so far, resulting in a memory effect with a remnant on/off ratio close to unity. In this letter we report complete channel depletion in thin-film ferroelectric transistors made of $PbZr_{0.2}Ti_{0.8}O_3$ and SnO_2:Sb thin films, leading to an on/off ratio well in excess of 10^3. In addition, we clarify important electronic constraints that apply to the design of ferroelectric transistors (semiconductor parameters, device speed, and maximum on/off ratio).

First we discuss the optimization of a transistor based on channel depletion, considering the semiconductor doping density and layer thickness. In the linear regime of operation the drain current in a field-effect transistor is given by[4] $I_D=\mu\widetilde{Q}V_D\,W/L$,where W and L are the width and length of the semiconductor channel, respectively, μ is the charge mobility, and $\widetilde{Q}$ (units C/m^2) is the areal charge density in the channel (the influence of interface states or contact resistance is neglected). When the transistor is operated, the modulation of the charge density in the channel results from the variation of the electrostatic potential at the semiconductor surface (band bending). Due to the memory effect in a ferroelectric transistor, the drain current can attain different values at zero gate voltage. At zero gate voltage we define two remnant states, namely the on-state of high drain current ($I_D^{\rm on}$), and the off-state of low current ($I_D^{\rm off}$). We would like to maximize the on-state current as well as the on/off ratio ($I_D^{\rm on}/I_D^{\rm off}$). For a given transistor geometry (W/L), carrier mobility, and drain voltage, the on-state current can be maximized by increasing the areal charge density in the channel. However, in order to be able to achieve total depletion of the channel in the off state, two constraints apply. First, $\widetilde{Q}$ should be smaller than or equal to the available remnant charge displacement of the ferroelectric material. Second, the band bending involved in totally depleting the semiconductor channel ($V_{\rm bb}$) should not be so large as to cause depolarization of the ferroelectric layer. When the carrier concentration is determined by the dopant density N_d, $\widetilde{Q}$ and $V_{\rm bb}$ are given by[4]

$$\widetilde{Q}=eN_d t_s, \quad V_{\rm bb}=\frac{eN_d}{2\epsilon_0\epsilon_r}t_s^2, \tag{1}$$

where e is the electronic charge, N_d is the dopant density, t_s is the semiconductor layer thickness, and ϵ_r is the relative dielectric constant of the semiconductor. Fig. 1 serves to illustrate the implications for the range of values allowed for N_d and t_s. As a realistic example, assume a transistor with a ferroelectric insulator having a remnant polarization of the order of 20 $\mu C/cm^2$ and a coercive potential of 2 V. Lines of constant charge density and constant band bending are shown in Fig. 1. Complete semiconductor depletion can only be reached if the point with coordinates t_s and N_d is located on the left-bottom side of the indicated lines. Using practical layer thicknesses (larger than 5 nm) and dopant concentrations (larger than $\sim10^{18}$ cm^{-3}), we are left with a semiconductor parameter window that is roughly indicated by the shaded area. Note that our parameter window is limited by the coercive potential of the ferroelectric layer and *not* by the

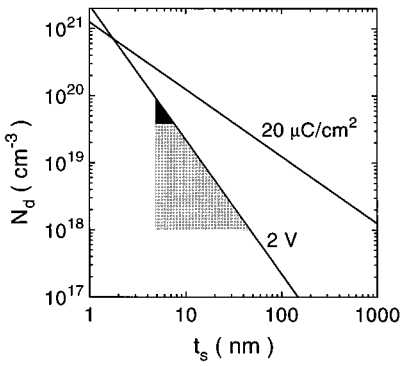

FIG. 1. Curves for a constant areal charge density of 20 $\mu C/cm^2$ and a constant band bending of 2 V [cf. Eq. (1), $\epsilon_r=10$], for a semiconductor thin film with carrier density N_d and thickness t_s. The shaded area indicates the parameter window of practical interest for a transistor based on complete channel depletion; the dark triangle gives the maximum on-state channel conductance.

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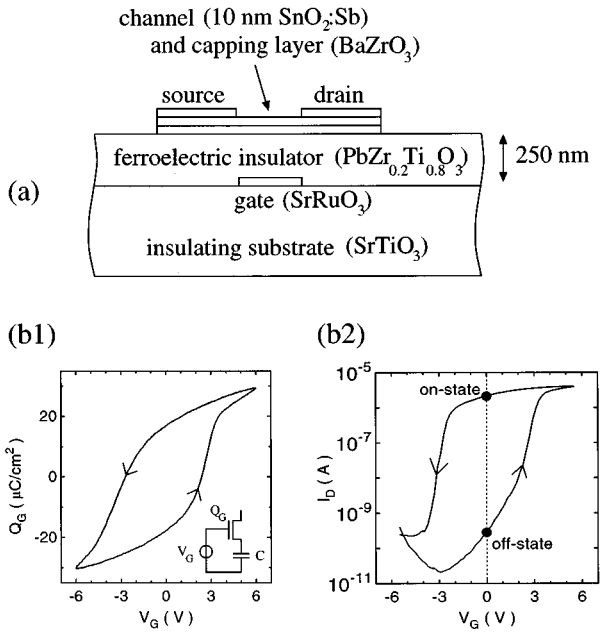

FIG. 2. (a) Schematic cross section of the oxidic thin-film transistor. (b1) The electrical charge per unit gate area displaced in the ferroelectric insulator (Q_G), as a function of the gate voltage (V_G). The displaced charge is measured with an external capacitor C (see inset). (b2) Transfer characteristic (drain current I_D versus V_G). The source is at zero potential and $V_D = 0.1$ V.

available polarization. A maximum on-state current is achieved when the product $N_d t_s$ is maximized; this preferred region is indicated by the dark triangle.

The staggered thin-film transistor with bottom-gate design is depicted in Fig. 2(a). The device consists of an *n*-type Sb-doped SnO_2 semiconductor layer, $PbZr_{0.2}Ti_{0.8}O_3$ as a ferroelectric insulator, and a $SrRuO_3$ gate electrode, each layer prepared by pulsed laser deposition (for more details we refer to Ref. 3). For protection purposes the semiconductor channel has been capped with 10 nm of insulating $BaZrO_3$. The 2-cm-diameter wafers contain resistance test structures, Hall bars, diodes, and transistors. We show data measured under ambient conditions, for transistors with a source-drain distance (L) between 5 and 100 μm and a channel width (W) of 300 μm. The source and drain contact pads consist of either Mo or degenerately doped In_2O_3:Sn. The contact resistance is 5–20 kΩ, caused by the presence of the $BaZrO_3$ capping layer. Following the analysis of Fig. 1,

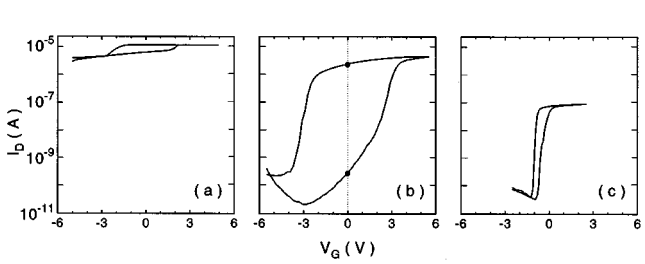

FIG. 3. Different types of transfer characteristics observed for wafers with different semiconductor films: (a) for thick films with a low sheet resistance, (b) showing the optimized on/off ratio, and (c) for thin films with a high sheet resistance. Note that the panels have equal voltage and current scales. The source is at zero potential and $V_D = 0.1$ V. The gate leakage current ($I_G \leqslant 0.5$ nA) disturbs the transfer characteristics at negative voltages.

SnO_2:Sb films were grown with a thickness of 10 nm and a dopant density of 4×10^{19} cm^{-3}. These films have a sheet resistance of 2×10^4 $\Omega/\square$. Using $R_{\square}^{-1} = \tilde{Q}\mu$ and Eq. (1), we deduce a charge mobility of 8 cm^2/V s. Hall measurements yield similar values for the carrier mobility,[5] while the measured field-effect mobility is of the order of 1 cm^2/V s.

Panel (b1) of Fig. 2 shows the measured displaced areal charge density. The charge displacement shows a hysteresis behavior with a remnant charge density of 17 μC/cm^2 and a coercive voltage of 2.5 V. Hysteresis is observed in the transfer characteristic (panel b2) with the same sense of rotation; this proves that the memory effect is driven by the ferroelectric charge displacement.[6] The gate leakage current ($I_G \leqslant 0.5$ nA) disturbs the transfer characteristic below -3 V. At zero gate voltage, the high-current on state and low-current off state are indicated in the figure. The on-state current is limited by the resistance of the source and drain contacts. The nonzero off-state current we attribute to carrier transport through interface or gap states in the semiconductor. For transistors with a channel length of 20 μm or less, we observe on/off ratios of the order of 10^3, with a maximum of 7×10^3. To our knowledge, an on/off ratio of this size has not been previously reported for oxidic thin-film transistors.[9]

When varying the semiconductor parameters, different types of transfer characteristics are observed. Extreme cases (low and high sheet resistance) are shown in Fig. 3. Curve type (a) is observed for semiconductor films with a thickness above 10 nm. The transistors show a proper hysteresis, however with a low on/off ratio. This is due to the fact that the semiconductor film contains too much charge, so that total depletion cannot be reached. Curve (b) shows the maximum on/off ratio achieved at present. Curves of type (c) are observed for thin semiconductor films with a high sheet resistance (of the order of a M$\Omega/\square$ or larger). For these transistors, the hysteresis behavior is strongly reduced in the transfer characteristic as well as in the charge displacement curve. We attribute this behavior to an insufficient field sweep in the ferroelectric material. For negative gate voltages (channel depletion) the applied voltage essentially drops across the semiconductor channel instead of across the ferroelectric insulator; as a result, the ferroelectric material does not pass through a saturated loop, but effectuates a minor hysteresis loop with low coercivity. Instead of comparing the characteristics of different wafers under the same measurement conditions (cf. Fig. 3), one can also compare the characteristics of one sample for different conditions of data acquisition. Interestingly, we could weakly observe the same trends as shown in Fig. 3 by cooling down a sample to cryogenic temperatures [shift towards type (c) due to a loss of free carriers] or by exciting with radiation of sufficient energy [shift towards type (a) due to an increase of the free carrier density].

Fig. 4 demonstrates the memory retention of our transistors. We observe an increase of the off-state current and a decrease of the on-state current with time, i.e., converging time evolution curves. The off-state drain current increases by a factor of 1.6 every time decade; after a relaxation time of 3 h, the off-state drain current is still more than two orders of magnitude smaller than the on-state current. We attribute

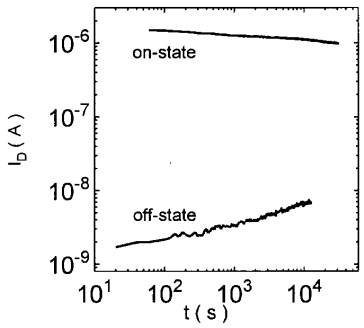

FIG. 4. Time evolution of the drain current, recorded with $V_D=0.1$ V and $V_G=0$ V. At $t=0$ a gate voltage pulse was applied, with an amplitude of $+6$ V for the on state and -6 V for the off state.

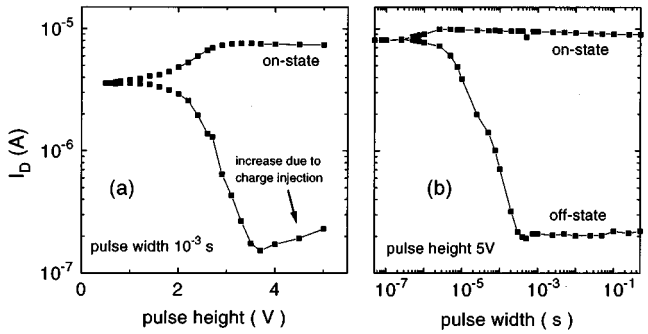

FIG. 5. On-state and off-state current (a) as a function of pulse height for fixed pulse width, and (b) as a function of pulse width for constant pulse height; recorded with $V_D=0.1$ V and $V_G=0$ V. Note that the current scales are equal.

these observations to a slow relaxation of the ferroelectric polarization, possibly caused by the depolarizing potential (band bending) of the semiconductor layer.

The switching voltage and switching speed can be studied by applying pulses of varying pulse height and width. The transistor of Fig. 5 shows a maximum on/off ratio for pulses of ± 3.5 V. At higher voltages the off current increases due to charge injection; the on current is limited by the contact resistance of the source and drain pads. The switching time can be estimated from the switched charge and the current drive:

$$\tau \simeq \Delta\tilde{Q} W L R_{\max}/V, \tag{2}$$

where $\Delta\tilde{Q}$ is the switched charge per unit gate area, V is the applied gate voltage, and $R_{\max}$ is the maximum channel resistance encountered during the switching procedure. In transistors with a transfer characteristic of rectangular shape, the maximum channel resistance equals the off-state resistance. In our devices the switched charge density is about 50 μC/cm^2 [see Fig. 2(a)]; hence, for the transistor of Fig. 5 ($W=300$ μm, $L=20$ μm, $V=5$ V, $R_{\max}\simeq 0.5$ MΩ) we calculate a required switching time of 300 μs. This value agrees with the data of Fig. 5(b). The experimentally determined speed of our devices is well described by Eq. (2).

For applications, it is important to consider operational limitations of ferroelectric transistors. The maximum on-state channel conductance is given by $\mu\tilde{Q}W/L$. On the other hand, the minimum off-state conductance is directly related to the required switching speed, described by Eq. (2). As a result, the on/off ratio is subject to the following upper limit:

$$\frac{I^{\text{on}}}{I^{\text{off}}} \lesssim \frac{\mu\tilde{Q}W/L}{\Delta\tilde{Q}WL/V\tau} = \frac{\mu V \tau}{L^2}. \tag{3}$$

Here we assumed that $\tilde{Q}$ equals $\Delta\tilde{Q}$, which applies for a transistor based on total depletion. As an example, using a carrier mobility of 20 cm^2/V s, and a switchable areal charge density of 50 μC/cm^2, we find a maximum channel conductance of 1 mS per square; using $L=1$ μm and $V=2$ V, we find a maximum on/off ratio of 4×10^3 for $\tau=1$ μs, and a maximum on/off ratio of 40 for $\tau=10$ ns. Clearly, the optimum design should be determined by the application envisaged.

In summary, we have fabricated ferroelectric transistors with different values of channel conductance, leading to strongly different transfer characteristics. The maximum remnant on/off ratio observed amounts to 7×10^3. The low off-state current is caused by total depletion of the semiconductor channel; the required band-bending potential is delivered by the coercivity of the ferroelectric charge displacement. Finally, the present study has clarified important design rules for depletion-type ferroelectric transistors.

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