A back-end, CMOS compatible ferroelectric Field Effect Transistor for synaptic weights

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Abstract

Neuromorphic computing architectures enable the dense co-location of memory and processing elements within a single circuit. This co-location removes the communication bottleneck of transferring data between separate memory and computing units as in standard von Neuman architectures for data-critical applications including machine learning. The essential building blocks of neuromorphic systems are non-volatile synaptic elements such as memristors. Key memristor properties include a suitable non-volatile resistance range, continuous linear resistance modulation and symmetric switching. In this work, we demonstrate voltage-controlled, symmetric and analog potentiation and depression of a ferroelectric $Hf_{0.57}Zr_{0.43}O_2$ (HZO) field effect transistor (FeFET) with good linearity. Our FeFET operates with a low writing energy (fJ) and fast programming time (40 ns). Retention measurements have been done over 4-bits depth with low noise (1 %) in the tungsten oxide (WO_x) read out channel. By adjusting the channel thickness from 15nm to 8nm, the on/off ratio of the FeFET can be engineered from 1 % to 200 % with an on-resistance ideally >100 kΩ, depending on the channel geometry. The device concept is using earth-abundant materials, and is

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compatible with a back end of line (BEOL) integration into complementary metal-oxide-semiconductor (CMOS) processes. It has therefore a great potential for the fabrication of high density, large-scale integrated arrays of artificial analog synapses.

Keywords

ferroelectric switching, hafnium zirconium oxide, tungsten oxide, BEOL, ferroelectric field-effect transistor, memristor

1   Introduction

The development of new computing architectures has seen a substantial push since the scaling of conventional CMOS technology has come to its limits and cannot keep up with the always increasing demand for computational power. A large part of today's computing resources is dedicated to processing large amounts of data, such as images, videos, or sensor outputs. For all these workloads, conventional von Neuman architectures are limited by a fundamental, time and power consuming task of transferring data between the processor and the memory.[1] Brain-inspired neuromorphic architectures with co-located computation and memory units appear as promising candidates to overcome this issue.[2] Such architectures consist of neurons that are interconnected by plastic synapses, which can be arranged in a crossbar topology to efficiently perform matrix-vector multiplications[3] âĂŞ a key computing task when executing neural networks.[4,5] In recent years, much progress has been made in neuromorphic hardware, in particular in creating crossbar arrays of artificial synapses connected to CMOS neurons.[6–12] Multiple device concepts have been proposed in order to realize the required artificial synapse, such as phase change memory (PCM),[13–15] filamentary and non-filamentary resistive switching memory (RRAM),[16–18] electro-chemical memory (ECRAM),[19–21] and ferroelectric (FE)[7,22–25] based memory cells. Unlike classical memory elements, such devices are characterized by the stronger need for multilevel or analog pro-

gramming capabilities to define the synaptic weight. While PCM and RRAM devices are essentially current controlled, the different states in ferroelectric memory elements are controlled by applying an electric field. The states are linked to the partial switching of the ferroelectric polarization, which allows to fine tune the synaptic weights in analog computing approaches, with fast and low-power writing.[26]

For circuits solving real world applications, the number of required synapses rapidly explodes with the complexity of the task at hand. Solving even a simple task such as the MNIST database of handwritten digits requires $\approx 10^5$ synapses,[27] while the training of a deep neural network (DNN) relies on up to millions of synapses. Such numbers of hardware synapses can only be obtained in densely integrated circuits such as fabricated using modern CMOS technology. Part of the functions in neural networks can also be implemented using CMOS circuits (e.g. activation). Therefore, it is important that materials and processes are CMOS compatible. The recent discovery of ferroelectricity in hafnia composites,[28] a material already present in CMOS lines, has revived research activity in the field of integrated ferroelectrics. Artificial ferroelectric synapses have been realized based on two device concepts, namely two-terminal ferroelectric tunneling junctions (FTJ)[29–33] and three-terminal ferroelectric field-effect transistors (FeFET).[7,22,24,34–37] Hafnia-based FTJs remain a challenge as the stabilization of the ferroelectric phase in sub-5 nm thick structures becomes difficult and polarization drops at film thicknesses relevant for tunneling.[33,38,39] Using a transistor instead has the advantage of separating the write process (low power write through high impedance gate[26]) and the read process (through source-drain resistance). It also permits to tune synaptic resistance by changing the channel geometry. Hafnia-based FeFETs were demonstrated mainly as non-volatile memory cells,[34] steep-slope field-effect transistors,[35,36] and artificial neurons.[8] These concepts usually are implemented on the front end of line (FEOL) and use Si as a channel. Because of the constraints imposed by the FEOL on the thermal budget and on the device geometry, an integration in the back end of line (BEOL) can be advantageous. E.g., an integration in the BEOL enable a larger device area with

respect to the size of the ferroelectric domains, which can translate into a larger number of states. Recently, analog synaptic behavior has been shown in a hafnia-based FeFET with indium gallium zinc oxide (IGZO) and poly-Si channels fabricated in the BEOL.[22,24,37] The combination of a hafnia-based ferroelectric with an oxide channel is expected to alleviate the known issues associated with Si-based FeFETs such as unintended low-k interfacial layers formed at the Si interface. On Si based channels, buffer layers have been used as a solution, but they have the disadvantage of reducing the effective field over the ferroelectric layer.[40–43] For neuromorphic applications the absolute resistance should be in the $M\Omega$ range[3] and the relative change in resistance ideally within a window of 8[3] up to 20-50.[44] Those values are a compromise between being large enough for performing learning tasks, and low enough to avoid one synaptic element to dominate the respone of a whole column/row of the overall crossbar array.[3,44] Here, we report on a $Hf_{0.57}Zr_{0.43}O_2$ (HZO) based FeFET utilizing a tungsten oxide (WO_x) channel. We demonstrate the impact of the ferroelectric polarization on the channel resistance, the influence of the channel thickness on the on/off ratio, ferroelectric HZO with a long endurance, the stabilization of multiple differentiable states, a good retention as well as a continuous potentiation and depression. By using a BEOL compatible process and by using only abundant and CMOS friendly materials, the proposed HZO/WO_x stack is very promising for large-scale integrated neuromorphic hardware based on ferroelectrics.

2 Results and discussion

For our study, we designed FeFET devices similar to back gated PseudoMOS[45] with an HZO ($10\,nm$)/TiN ($10\,nm$)/n^+ Si gate stack and an $8\,nm$ thick WO_x channel[20,21] (Figure 1a). The channel is formed by oxidizing $2.5\,nm$ of W after the formation of the ferroelectric HZO.[46] The source and drain contacts are deposited on the WO_x channel through lift-off. The device is encapsulated by a $5\,nm$ Al_2O_3 and a $100\,nm$ SiO_2 passivation layer. Contact

pads are formed on top of the passivation layers and routed through openings to source and drain. The gate is accessible through the highly n^+ doped Si substrate and is shared between all devices on our chip. As visible in the bright field scanning transmission electron microscopy (BF-STEM), our fabrication process results in sharp interfaces between the layers and crystalline WO_x grains (Figure 1b). The energy-dispersive X-ray spectroscopy (EDS) line profile confirms the targeted elemental distributions and reveals regions of intermixing between the various layers. After the low temperature crystallization of HZO by a millisecond flash lamp technique described elsewhere,[46] grazing incidence X-ray diffraction (GIXRD) analysis shows the characteristic peak at 30.6Å of the orthorhombic/tetragonal phase in HZO (Figure 1c). The diffractogram is consistent with data from metal-ferroelectric-metal (MFM) structures with the same HZO published in Ref. (46). No monoclinic phase (peaks at 28.2Å and 31.8Å)[47] is present in our samples, which is a consequence of the low temperature crystallization technique. Following the oxidation and crystallization of W to WO_x, GIXRD still shows no monoclinic HZO phase, but displays two additional peaks at 28.8Å and 33.6Å that can be attributed to the monoclinic P121/c1 phase of WO_x (ICSD-647640).[48]

For the electrical characterization of HZO in our FeFET devices, additional metal-semiconductor-ferroelectric-metal (MSFM) capacitor structures have been processed on the same sample. "Capacitance versus voltage" $(C - V)$ measurements on a $60\,\mu m \times 60\,\mu m$ capacitor reveal a ferroelectric typical butterfly-shaped hysteresis curve typical of ferroelectrics, with a capacitance per unit area of $C_{OX} = 2.7\,\mu F/cm^2$ (Figure 2a). The asymmetric behavior originates from the asymmetric electrodes (WO_x, TiN). "Polarization versus voltage" $(P - V)$ measurements were performed on the same capacitor (Figure 2b) and show typical characteristics. In the pristine state, the $P - V$ curve is anti-ferroelectric (AFE)-like with hysteresis, especially on the negative voltage side.[49] We applied 10^5 switching cycles with an amplitude of $\pm 3.8\,V$ at a frequency of $100\,kHz$, resulting in a pinched $P - V$ curve with a positive (negative) remanent polarization $+P_r = 12.4\,\mu C/cm^2$ ($-P_r = 11.8\,\mu C/cm^2$). Furthermore, a slight imprint with a positive coercive voltage of $+V_C = 0.91\,V$ and a negative
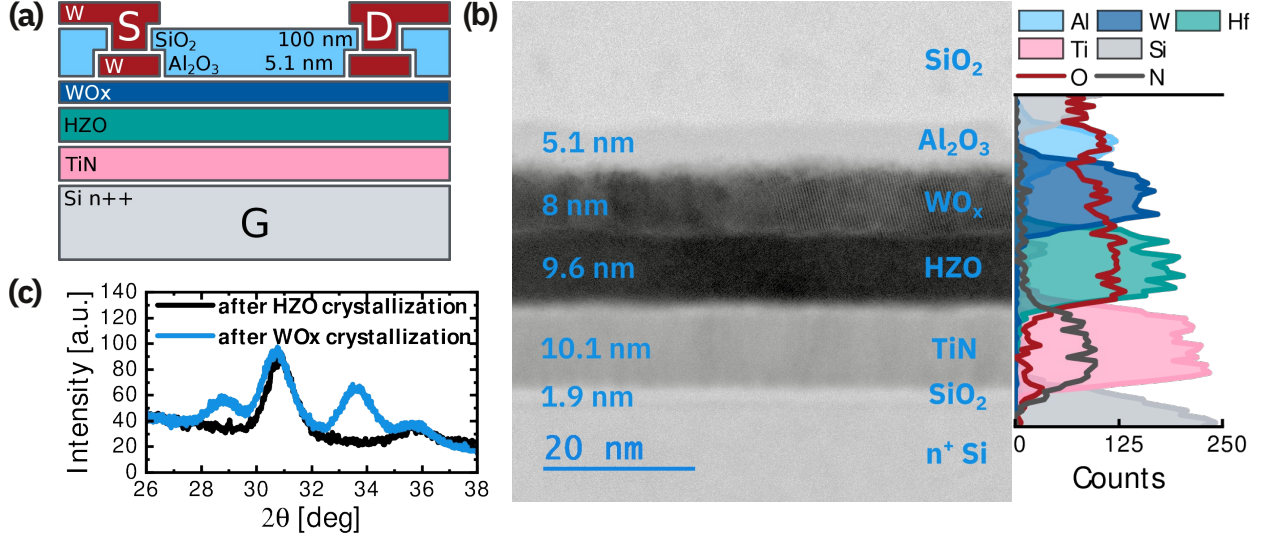
Figure 1: Structural data of the FeFET. **(a)** Schematic illustration of a FeFET, indicating source (S), drain (D), gate (G), a WO_x channel and a ferroelectric HZO gate dielectric. **(b)** Cross-sectional BF-STEM image with energy-dispersive X-ray spectroscopy (EDS) line profile of the $SiO_2/Al_2O_3/WO_x/HZO/TiN/n^+$ Si gate region. **(c)** GIXRD for a diffraction angle (2θ) from 26Âř to 38Âř showing the presence of the orthorhombic/tetragonal crystalline phase in HZO after crystallization and after the W layer was oxidized to WO_x.

one of $-V_C = -1.27\,\text{V}$ are observed due to the asymmetric electrodes. The cycling endurance of our HZO is 10^8 for an MFM structure and 8×10^6 in the case of the MSFM configuration present in our FeFET (Figure S1).

Having confirmed the ferroelectric nature of our HZO gate dielectric, the electrical characterization of the WO_x channel in a FeFET device was performed next, by investigating the influence of P_r, channel thickness (d_{WOx}), and the channel carrier concentration (N_D) on the channel resistance (R_{DS}). For that, three samples with different d_{WOx} and one with a non-ferroelectric HfO_2 gate dielectric were realized. R_{DS} was measured between source and drain after each $2\,\mu s$ long write pulse (V_{write}) applied to the gate (measurement scheme can be seen in Figure S4). For ease of comparison, R_{DS} is normalized by R_{ON} (Figure 2c, d, e, f). A clear hysteresis in R_{DS} is observed for devices with a ferroelectric HZO gate dielectric. To confirm that the modulation of the channel resistance originates from P_r and not from another effect, an identical device with a non-ferroelectric HfO_2 gate dielectric was measured. Both have an 8 nm thick WO_x channel. R_{DS} shows no hysteresis in the non-ferroelectric

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HfO$_2$ sample (Figure 2c) and further proves that the hysteresis originates from the ferroelectricity in HZO. In addition to the polarization in the HZO, the type and concentration of the free charge carriers[50,51] as well as d_{WOx} influence the on/off ratio. For a maximum reduction in the channel off-current, the polarization-field induced depletion width (x_{d}) should be larger than d_{WOx}. Using Poisson’s equation, the relationship between x_{d} and N_D can be expressed as follows:[51–53]

$$x_{\text{d}} = \frac{\epsilon_0 \epsilon_{\text{WOx}}}{C_{\text{HZO}}} \left[\left(1 + \frac{2C_{\text{HZO}}^2 V_{\text{GS}}}{q N_{\text{D}} \epsilon_0 \epsilon_{\text{WOx}}} \right)^{1/2} - 1 \right], \tag{1}$$

where ϵ_0 is the vacuum permittivity, ϵ_{WOx} the permittivity of WO$_x$ ($\epsilon_{\text{WOx}} = 189$, see supplementary information), C_{HZO} is the HZO capacitance per unit area ($C_{HZO} = 3.14\,\mu\text{F/cm}^2$, Figure S5b), and V_{GS} is the polarization charge-induced potential across HZO. The carrier concentration ($N_{\text{D}} = 1.01 \times 10^{20}\,\text{cm}^{-3}$), the channel resistivity ($\rho_{\text{H}} = 3.27 \times 10^{-1}\,\Omega\,\text{cm}$) and its mobility ($\mu_{\text{H}} = 0.19\,\text{cm}^2\,\text{V}^{-1}\,\text{s}$) were determined by Hall measurements carried out on a similar sample. Using Eq. (1), a depletion width $x_{\text{d}} = 1.7\,\text{nm}$, $3.3\,\text{nm}$, $4.8\,\text{nm}$ and $6.4\,\text{nm}$ for $V_{\text{GS}} = 1\,\text{V}$, $2\,\text{V}$, $3\,\text{V}$ and $4\,\text{V}$, respectively was calculated (Figure S6b). For a constant polarization, the largest effect is obtained if $d_{\text{WOx}} < x_{\text{d}} = 6.4\,\text{nm}$ or $N_{\text{D}} < 1 \times 10^{20}\,\text{cm}^{-3}$. Three samples with different d_{WOx} were realized to benchmark this estimation with experimental data. BF-STEM measurements reveal $d_{\text{WOx}} = 8\,\text{nm}$, $11.3\,\text{nm}$ and $15\,\text{nm}$, as reported in Figures 1b and S2a,b, respectively. The polarization does not change between the three structures (Figures 2a and S3a,b). By decreasing d_{WOx} from $15\,\text{nm}$ to $11.3\,\text{nm}$ and $8\,\text{nm}$ the on/off ratio increases from $\approx 1\,\%$ to $\approx 5\,\%$ and $\approx 90\,\%$, respectively. Those results agree well with the x_{d} calculated by Eq. (1).

For neuromorphic applications multiple (analog) levels of the channel resistance, good retention properties, low device-to-device and cycle-to-cycle variations, fast updates, and low power consumption are important characteristics of ideal devices.[3,4,44,54] The exact requirements vary depending on the details of operation and from one implementation to the other. As an example, inference workloads would use off-line trained weights transferred to the chip
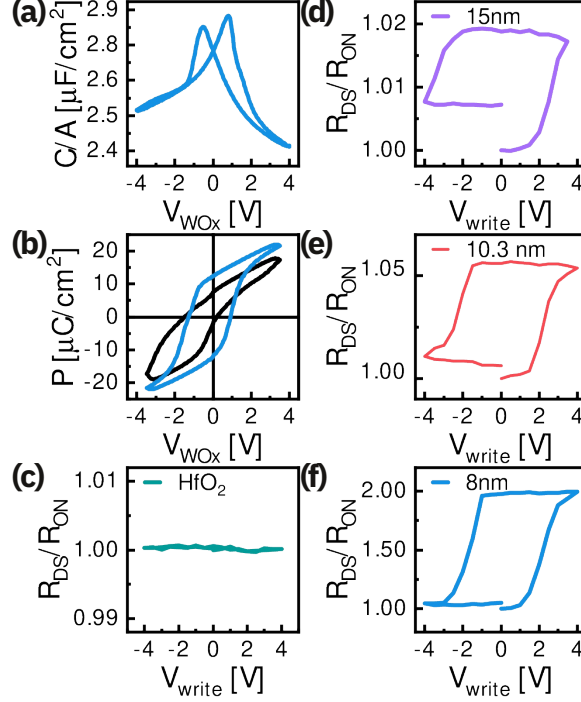
Figure 2: Capacitance and polarization behavior of a $60\,\mu\text{m} \times 60\,\mu\text{m}$ $\text{W}/\text{WO}_\text{x}/\text{HZO}/\text{TiN}/\text{n}^+Si$ MSFM structure and WO_x channel resistance hysteresis: **(a)** Capacitance versus voltage $(C - V)$ measurements after the HZO was woken up by 20 $C - V$ cycles. **(b)** Polarization versus voltage $(P - V)$ characteristics in the pristine state and after 10^5 cycles. **(c, f)** Comparison of simultaneously processed samples with HZO and HfO_2 gate dielectric. The non ferroelectric HfO_2 sample does not show any channel resistance hysteresis. **(d, e, f)** Influence of the channel thickness (d_{WOx}) on the on/off ratio.

to operate the network, and the precision of the weights ($\geq$3bit) is more relaxed as in the case of a chip designed to perform on-line learning.[55] In our device structure, weights are defined through the intermediate states of the channel resistance, enabled via the multi-domain nature of the ferroelectric HZO layer.[25,29,56] By switching only a subset of the domains, a state between R_{ON} and R_{OFF} can be set.[29] The fraction of the switched ferroelectric domains
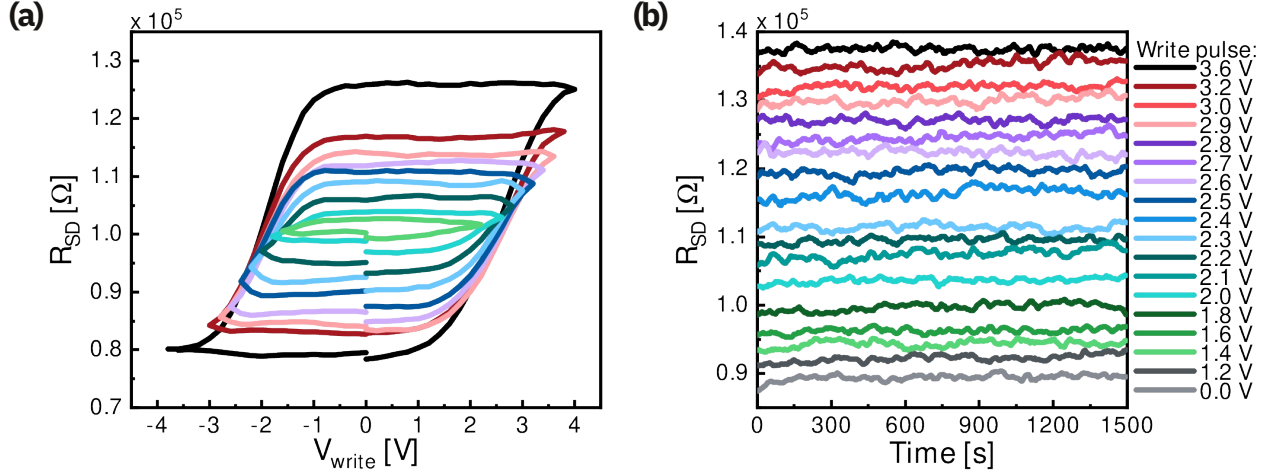
Figure 3: Analog multi-level behavior of a FeFET of 20 µm width and 5 µm length. **(a)** The channel resistance (R_{DS}) after the application of 5 µs write pulses (V_{write}) of varying amplitudes. The different curves correspond to different consecutive measurements with reducing V_{write} range. **(b)** Retention measurement for 1500 s. $V_{read,D} = 200$ mV was uninterruptedly applied while R_{DS} was measured every 5 s.

depends on the amplitude, width, and number of the applied write pulses. Different pulsing schemes on HZO have been investigated in the past.[22] For on-line learning algorithms running on crossbar arrays integrated on CMOS, potentiation and depression pulse schemes with a constant pulse amplitude and width are preferred to those with varying amplitude. Nevertheless, for the proof of concept the multi-state nature of a 20 µm wide and 5 µm long FeFET was investigated by applying voltage pulses of varying amplitudes, while keeping a fixed pulse duration of 5 µs (Figure 3a). This pulse scheme results in the best linearity in potentiation and depression.[22] By sweeping V_{write} from -4 V to 4 V, R_{DS} shows a hysteretic cycle from 80 kΩ to 125 kΩ with various intermediate states (on/off ≈ 1.55). By reducing the range of V_{write} numerous R_{DS} sub-loops can be accessed, as shown in Figure 3a. The asymmetry in the hysteresis loop is due to the imprint in the ferroelectric layer. Furthermore, the retention properties have been studied, as demonstrated in Figure 3b. First, an intermediate state was written by a 5 µs pulse. Then, a source-to-drain voltage $V_{DS} = 200$ mV was applied for 1500 s, while R_{DS} was measured every 5 s. Between each measured intermediate state the FeFET was reset to its low resistive state (R_{ON}) by setting $V_{write} = -4$ V during 1 ms. The
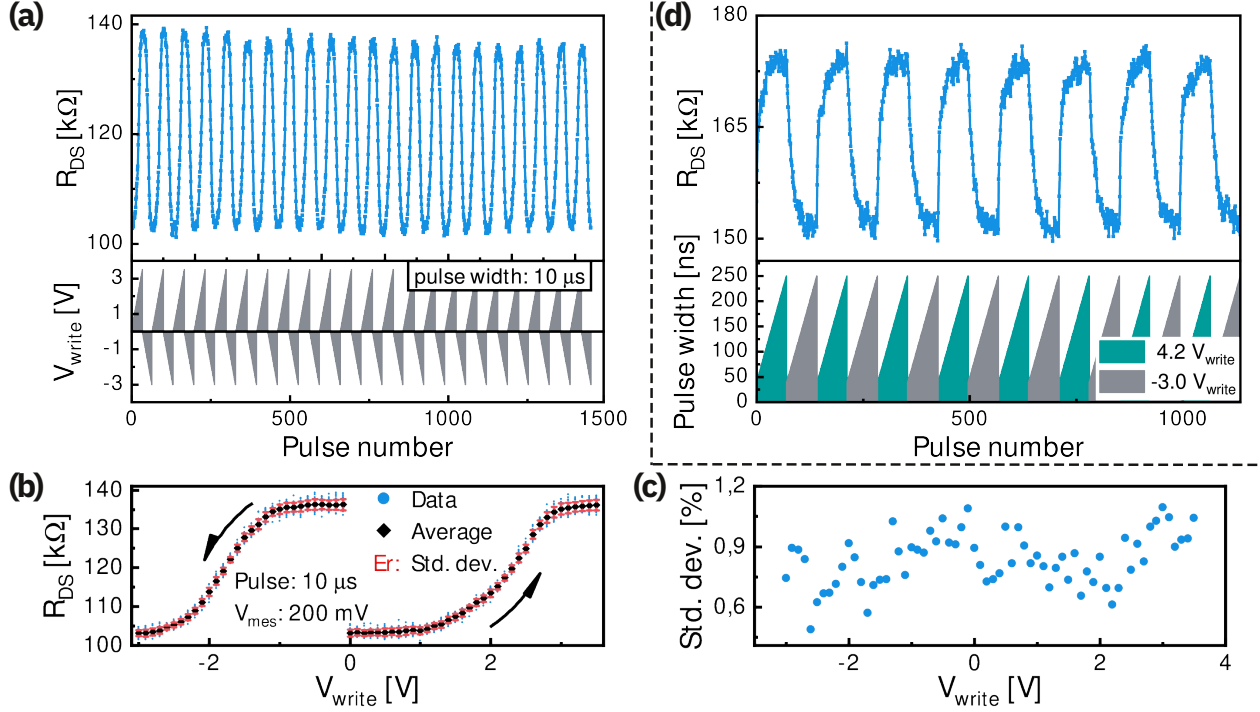
Figure 4: Potentiation and depression of a $20\,\mu m$ wide and $5\,\mu m$ long FeFET. **(a)** The top panel shows multiple potentiation and depression cycles of the channel resistance (R_{DS}) with varying pulse amplitude (V_{write}) and constant pulse width (t_{write}). The bottom panel shows the corresponding write pulse sequence . After each pulse R_{DS} was measured. **(b)** Absolute cycle-to-cycle variation of R_{DS} showing the data, average and standard deviation error bars. **(c)** Standard deviation of the R_{DS} cycle-to-cycle variation in percent. **(d)** Multiple potentiation and depression cycles of R_{DS} with increasing t_{write} from $40\,ns$ to $250\,ns$ and constant V_{write}.

FeFET showed stable retention properties for 18 differentiable channel resistances (>4bit) for the full $1500\,s$. The good retention measurement hints to an absence of depolarization or other screening mechanisms. The obtained multistate storage capability, the long retention and rather fast programming speed makes this FeFET suited for inference applications.

For on-chip learning, artificial synapses require a finer mesh of intermediate levels. In addition, symmetric and linear potentiation and depression are desirable. With respect to symmetry the field-driven ferroelectric switching is advantageous to other technologies that often show abrupt or unidirectional switching.[22,44] The requirement of low variability is relaxed as the training occurs on a specific hardware and thus incorporates the variability in its solution.[55] To investigate the linearity and symmetry of the potentiation and depression,

multiple write pulses of increasing and decreasing amplitude were applied. For the potentiation V_{write} was increased from 0 V to 3.5 V and for the depression decreased from 0 V to −3 V with 100 mV steps (Figure 4a). The duration of the write pulses was kept constant at 10 µs. When averaging over several cycles (Figure 4b), multiple states with small standard deviation are observed. Normalizing the cycle-to-cycle standard deviation by R_{ON} reveals a constant value of about 1 % (Figure 4c). The number and overlap of states are defined by the potentiation and depression step size. The latter could be reduced further to increase the resolution. When fitting the potentiation range from 1 V to 3.1 V and depression range from −0.9 V to −3.0 V by linear regression (Figure 5a), an adjusted residual-square value of 0.952 is obtained. The residuals normalized by the R_{DS} window as a function of pulse number is depicted in Figure 5b. For a more detailed analysis of the symmetry, Gaussian process regression (GPR) was used to predict a noise free signal (Figure 5c).[57] Plotting ΔR (Figure 5e) and the signal to noise ratio (SNR, Figure 5d) as a function of pulse number reveals diminishing ΔR and noisier signals towards the extremes. The symmetry factor (SF) was then calculated using the following equation:[57]

$$SF = |\frac{\Delta R_+ - \Delta R_-}{\Delta R_+ + \Delta R_-}|, \tag{2}$$

where ΔR_+ is the potentiation and ΔR_- is the depression change in resistance at a certain resistance level. By this definition, SF can take values between 0 and 1 where 0 is the perfect symmetry. The less linear the range of the data becomes, the larger is SF (Figure 5d). The average across the full resistance range is $SF = 0.20$ while the most linear part in the center reaches a very good symmetry factor of $SF = 0.08$.

Short programming pulses are advantageous as fast writing and low-power consumption are important for neuromorphic applications. By varying the pulse width from 40 ns to 250 ns with a fixed amplitude (Figure 4d), already the shortest applied pulse of 40 ns (equipment limit) changes the resistance and demonstrates very fast writing capabilities of the FeFET. It is expected that even shorter pulses could successfully program the device.[29] In our device,
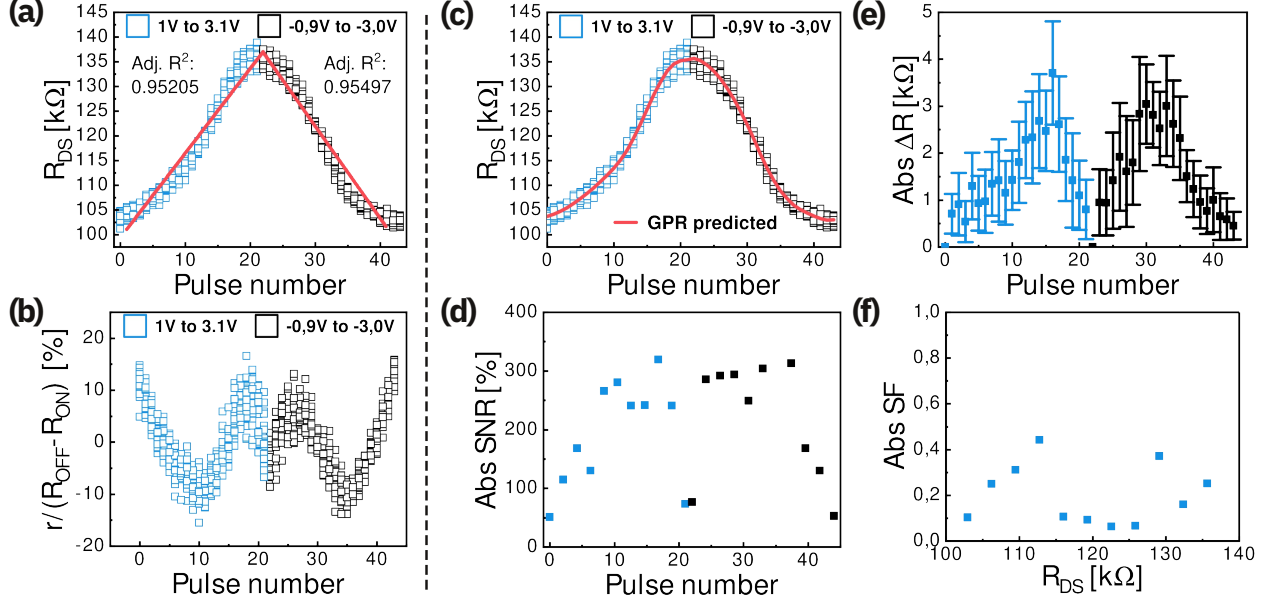
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Figure 5: Extraction of linearity and symmetry metric. Linear regression and the GPR methodology[57] is applied to our FeFET data from multiple cycles with: 22 potentiation pulses (blue) with increasing amplitude (1 V to 3.1 V) and 22 depression pulses (black) with decreasing negative amplitude (-0.9 V to -3 V). **(a)** R_{DS} as a function of pulse number and the linear regression fit (red). **(b)** Absolute residuals r normalized by the channel resistance window.**(c)** Channel resistance (R_{DS}) as a function of pulse number and the GPR predicted noise free signal (red). **(d)** Absolute SNR for each potentiation and depression pulse. **(e)** Absolute change of R_{DS} after each potentiation and depression pulse. **(f)** Symmetry factor (SF) as a function of R_{DS}.

little energy is consumed while writing a state. When applying $V_{write} = 3.5$ V a gate current of $I_{gate} = 3.02 \times 10^{-8}$ A is measured. Applying a write pulse duration of $t_{write} = 200$ ns results in $E = \frac{V_{write} \cdot I_{gate} \cdot t_{write}}{w \cdot l} = 2.1 \times 10^{-17}$ J µm^{-2}, where l is the length and w the width of the gate.

3   Conclusion

We propose a device concept based on the ferroelectric field effect into a thin WO$_x$ channel using HZO gate dielectric, that can be used as a synaptic element in hardware-supported neural networks. The fabrication process is compatible with the integration in the Back End Of Line of CMOS technology and is using earth-abundant materials, which is making

it attractive for large-scale integration. By comparing HZO and HfO$_2$ based devices, and carefully analyzing capacitor and transistor data, we unambiguously show that the channel resistance is directly coupled to the polarization of the HZO layer and can be programmed in a non-volatile manner. Multilevel states programmed over more than 4-bits depth with a good retention and an almost symmetric potentiation and depression is obtained, together with a low programming energy. The property of the WO$_x$ layer and the geometry of the device can be arranged so that a well-suited resistance range is obtained, favorable to build large scale arrays. The proposed device exhibit therefore promising metrics when considered as a synaptic element for processing cores supporting artificial neural networks. Future work will concentrate on controlling the channel thickness and the carrier concentration of WO$_x$ to increase the on/off ratio, so that the device can be operated strictly in the linear region, without ever fully switching all the domains to the same polarization. This is expected to improve symmetry and to allow a constant pulse scheme for potentiation and depression, which is more friendly to learning algorithms.

4   Experimental

Sample preparation. Our FeFET is a bottom/gate device with shared gate. The gate contact is accessed through the Si n^+ substrate. First, 10 nm TiN was deposited using a tetrakis(dimethylamino)titanium (TDMAT) precursor and N$_2$/H$_2$ plasma in an Oxford Instruments plasma enhanced atomic layer deposition (PEALD) system. An approximately 10 nm thick layer of HZO was grown in a process using alternating cycles of tetrakis(ethylmethylamino)hafnium (TEMAH), and ZrCMMM ((MeCp)2Zr(OMe)(Me)) at 300 °C. Rutherford Back Scattering (RBS) analysis of the film (not shown) indicated an actual film composition of Hf$_{0.57}$Zr$_{0.43}$O$_2$. The sample was then immediately transferred to a sputter chamber for the deposition of 4 nm W. For the crystallization of HZO a millisecond flash lamp anneal (ms-FLA)[46] with a background temperature of 375 °C was performed.

After crystallization the $4\,\mathrm{nm}$ W was reduced to $\approx 2.5\,\mathrm{nm}$ by Ar sputtering. The W was then crystallized and oxidized to $10\,\mathrm{nm}$ WO_3 in a rapid thermal annealer (RTA) at $350\,°\mathrm{C}$ for $6\,\mathrm{min}$ with $50\,\mathrm{sccm}$ O_2. Afterwards a reduction of the WO_3 to WO_x was performed in a RTA by H_2 annealing at $150\,°\mathrm{C}$ and vacuum annealing at $350\,°\mathrm{C}$. WO_x was further thinned by Ar sputtering to $8\,\mathrm{nm}$. Source and drain were deposited by sputtering and liftoff. The passivation consists of $5\,\mathrm{nm}$ Al_2O_3 by thermal ALD (precursor) and $100\,\mathrm{nm}$ SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). Vias were etched using a reactive ion etcher (RIE) with a CHF_3/O_2 plasma. Finally, the contacts were realized by depositing $100\,\mathrm{nm}$ W by sputtering and defined in an RIE with a SF_6/O_2 plasma.

Structural Characterization. Grazing incidence X-ray diffraction (GIXRD) measurements were performed in a Bruker D8 Discover diffractometer equipped with a rotating anode generator. TEM lamellas have been prepared by Focused Ion Beam using a FEI FIB Helios FEI Helios NanoLab 450S and investigated with a double spherical aberration-corrected JEOL JEM-ARM200F microscope. Bright field STEM (BF-STEM) images have been acquired at 200 kV and Energy Dispersive x-ray Spectroscopy (EDS) line profiles have been performed using a liquid-nitrogen-free silicon drift detector.

Electrical Characterization. $R_{DS} - V_{write}$ and retention were measured using an Agilent B1500. V_{write} pulses were generated by a WGFMU and RSU module for the Agilent B1500 and applied to source and drain simultaneously while grounding the gate (Figure S4a). R_{DS} was measured by applying an IV-sweep from $-200\,\mathrm{mV}$ to $200\,\mathrm{mV}$ to the drain while having the source connected to ground (Figure S4b). R_{DS} was then determined by averaging the resistance at $\pm 200\,\mathrm{mV}$. $P - V$ loops on HZO were recorded using a TF Analyzer 2000 from AixAct. The signal of $5\,\mathrm{kHz}$ was applied to the top W/WOx contact while the bottom TiN/n^+ Si contact (substrate) was grounded. For the wake-up of HZO, 10^5 cycles of $\pm 3.8\,\mathrm{V}$ and $100\,\mathrm{kHz}$ were applied.

Supporting Information Available

The following files are available free of charge.

The Supporting Information is available free of charge on the ACS Publications website at DOI:

- Additional data concerning the endurance of MFM and MSFM structures, BF-STEM and $P-V$ measurements on additional samples, electrical measuring schemes, capacitance measurements and permittivity and depletion width calculations. (PDF)

Acknowledgement

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Supporting information for:

A back-end, CMOS compatible ferroelectric

Field Effect Transistor for synaptic weights

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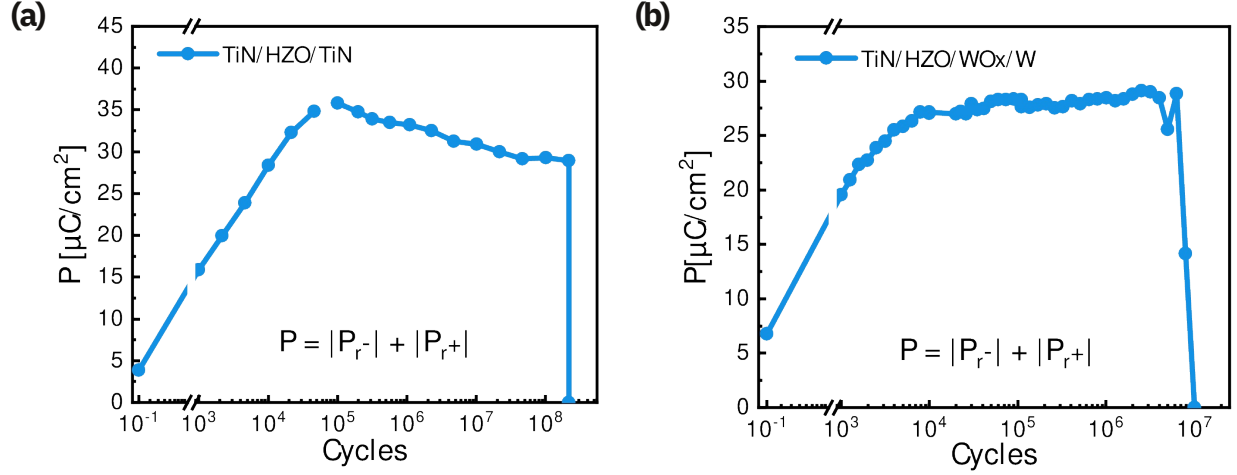‡*Integrated Systems Laboratory, ETH Zurich, CH-8092 Zurich, Switzerland*

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Figure S1: Endurance measurements of 10 nm HZO. The total remanent polarization $(P = |P_{r-}| + |P_{r+}|)$ was determined by positive up negative down (PUND) measurements with 1 kHz and ± 3.5 V. The cycling frequency was set to 1 kHz up to 10^4 cycles, 10 kHz up to 10^5 cycles and 100 kHz for cycles above 10^5: **(a)** The TiN/HZO/TiN MFM configuration was cycled at ± 3.5 V. **(b)** The W/WO$_x$/HZO/TiN MSFM configuration was cycled at ± 3.0 V with a -0.5 V offset.
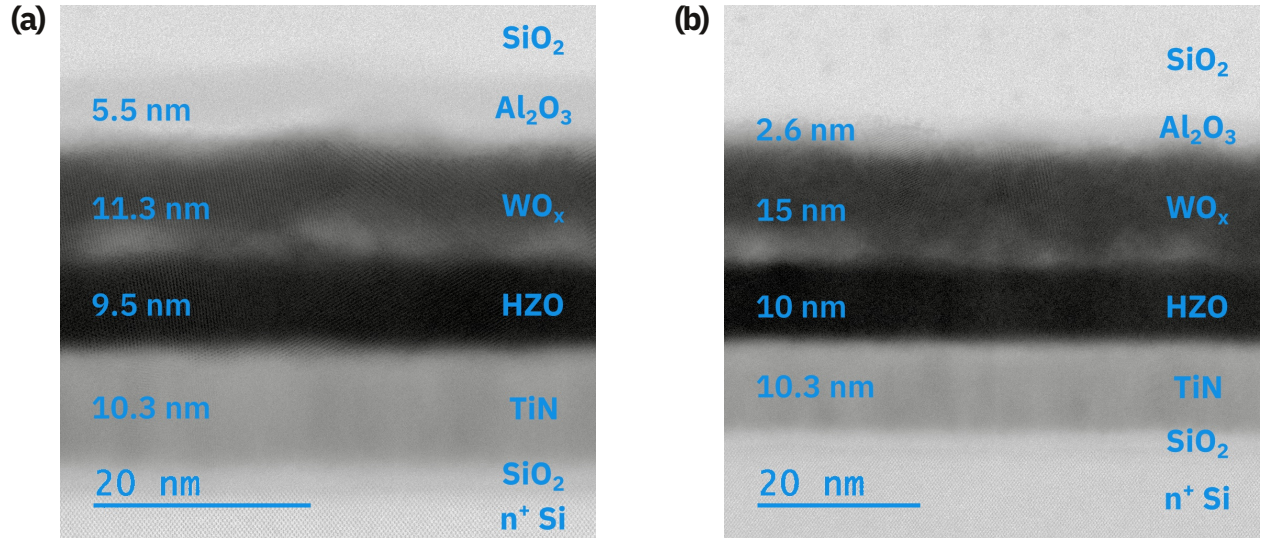

Figure S2: Cross-sectional BF-STEM images of the samples from the WO$_x$ thickness series: **(a)** $d_{WOx} = 11.3$ nm, **(b)** $d_{WOx} = 15$ nm
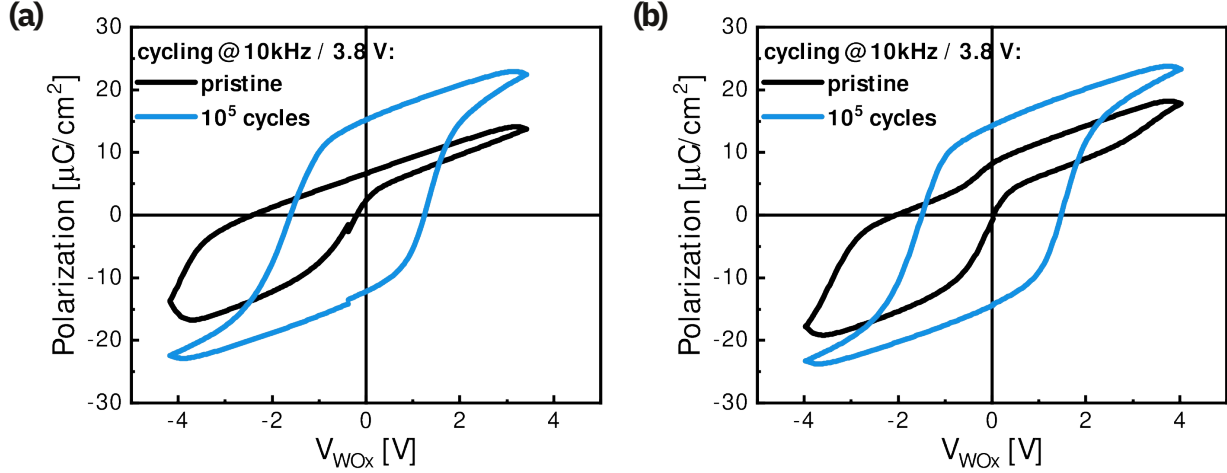
Figure S3: P-V measurements on the samples from the WO_x thickness series. Polarization versus voltage $(P-V)$ characteristics measured on $60\,\mu m \times 60\,\mu m$ $W/WO_x/HZO/TiN/n^+Si$ MFM structures at $5\,kHz$ in the pristine state and after 10^5 cycles: **(a)** $d_{WOx} = 11.3\,nm$, **(b)** $d_{WOx} = 15\,nm$.
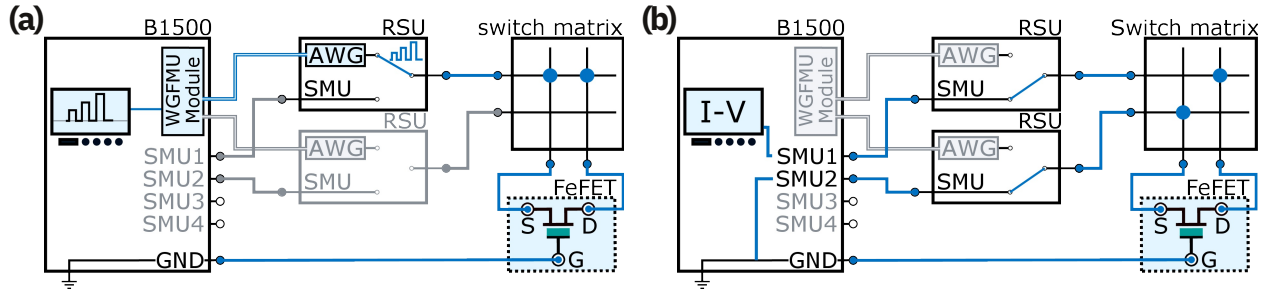

Figure S4: Write and read schematic showing a semiconductor parameter analizer (B1500) with the waveform generator/fast measurement unit (WGFMU) and its two remote-sense and switch units (RSU): A state is written by applying a pulse to source (S) and drain (D) while the gate (G) is grounded. The channel resistance is read by applying an IV-sweep from $-200\,mV$ to $200\,mV$ to D while having S connected to the common ground through SMU2.
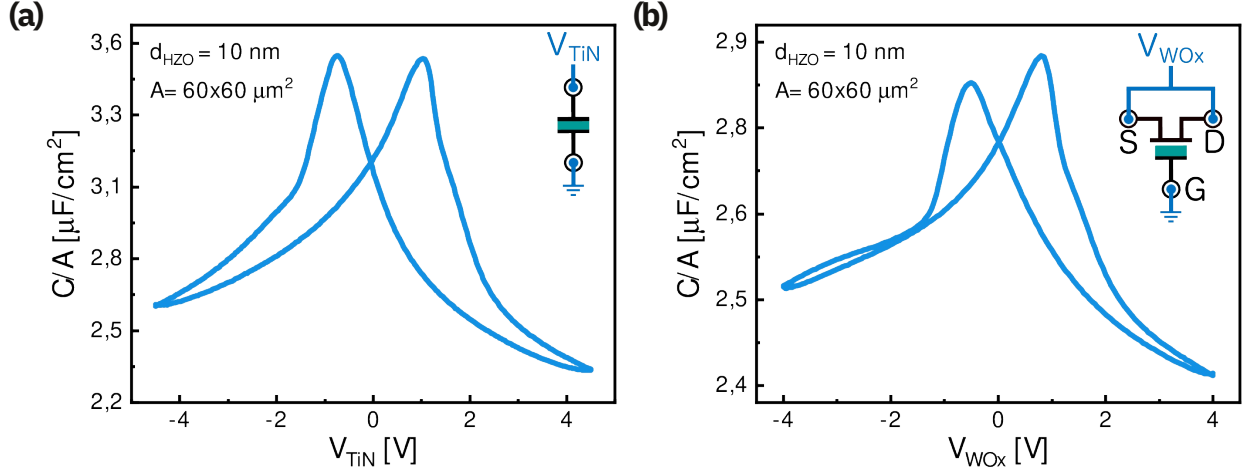
Figure S5: Capacitance measurements on a $60\,\mu\text{m} \times 60\,\mu\text{m}$ **(a)** $\text{TiN/WO}_x/\text{TiN}$ MFM and **(b)** $\text{W/WO}_x/\text{HZO/TiN/n}^+\text{Si}$ MSFM structure

WO$_x$ permitivity

The permittivity of WO_x ($\epsilon_{\text{WOx}} = 189$) was calculated using the following equation of two capacitances in series:

$$\frac{1}{C_{\text{WOxHZO}}} = \frac{1}{C_{\text{HZO}}} + \frac{d_{\text{WOx}}}{\epsilon_0 * \epsilon_{\text{WOx}} * A},\tag{1}$$

where C_{WOxHZO} is the capacitance of the $\text{W/WO}_x/\text{HZO/TiN}$ stack, C_{HZO} the capacitance of TiN/HZO/TiN stack, $d_{\text{WOx}} = 8\,\text{nm}$ the thickness of the WO_x channel, ϵ_0 the vacuum permittivity and $A = 3600\,\mu\text{m}^2$ the area of the capacitor. From Figure S5a we get $C_{\text{HZO}} = 1.13 \times 10^{-10}\,\text{F}$ and from Figure S5b we get $C_{\text{WOxHZO}} = 9.9 \times 10^{-11}\,\text{F}$.

$$x_d = \frac{\epsilon_0 \epsilon_{WOx}}{C_{HZO}} \left[\left(1 + \frac{2C_{HZO}^2 V_{GS}}{qN_D \epsilon_0 \epsilon_{WOx}} \right)^{1/2} - 1 \right]$$
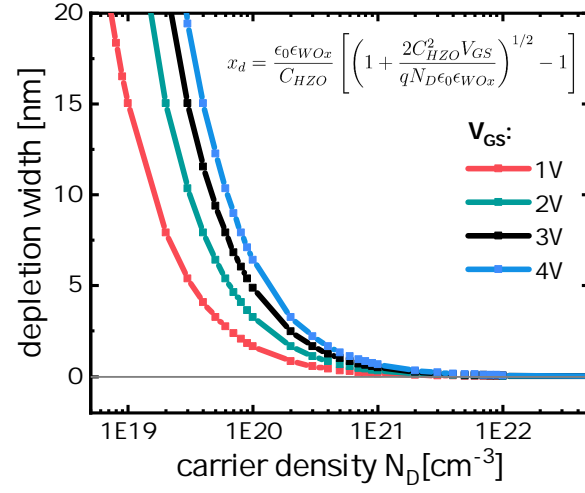
Figure S6: Depletion width as a function of carrier concentration N_D calculated for different V_{GS}