Discussion :

The system works according to provided specifications .
We had difficulties to navigate in the software.
To improve the system, we can do a decimal rather than hexadecimal display using 2 digit
We could also extend the system to display more digit

Conclusion :

Today we have learned to design a decoder. It is an example of a system using combinatorial logic. We have done a module that we can now use in any of our project. Every time we may have 4 inputs, we will be able to visualize them through a7 segment display.

Questions :

1. Can there be a difference in logical behavior between the intended logic entered and simulated and, the logic actually synthesized for FPGA? Why?

Yes , there can be a difference. Our system is a simulation, witch use several gates to simulate one.
Moreover, component are not perfect. This causes delay that can interfere with the logic

2. Why do we need a configuration file?

For the verilog module, input and output are just variables. We need a configuration file to link them with real port of the FPGA.

3. Is there a functional difference in circuitry between Lab 1, Part 3andBasys board for this particular application?
There is no functional difference. Both system have the same input and output.

4.What must be done in order to use switches SW3 and SW7 instead of SW0 and SW1? How about using LED5 instead of LED0?
We just have to replace the port names in the .ucf file :
For the switches, we can change P11 and L3 to B4 and N3.
For the LEDwe can change M5 to N4.