

Imperial College London

Department of Electrical and Electronic Engineering

Final Year Project Report 2023

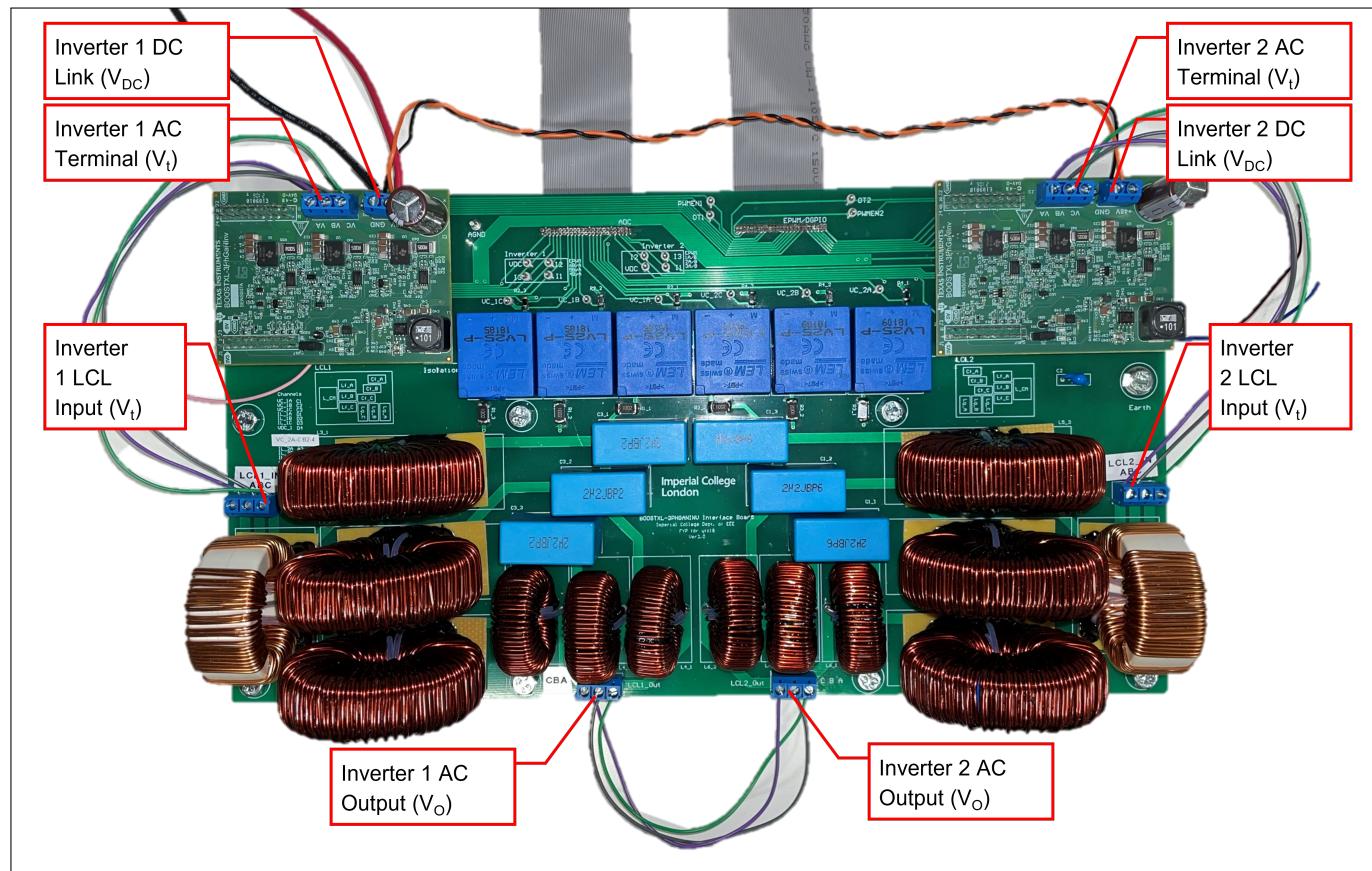


Figure 1: Image of board, completed with all soldered components: a 3-phase grid-forming (GFM) inverter connected with a 3-phase grid-following (GFL) inverter

Project Title: **Deployment of Rapid Control Prototyping Technique for 3-phase Inverters**

Student: **Yan To Chau**

CID: **01705211**

Course: **EEE4**

Project Supervisor: **Professor Tim Green**

Second Marker: **Dr Balarko Chaudhuri**

1 Cover Notes

1.1 Plagiarism Statement

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1.2 Symbols

In most sections, the converter side inductor currents are denoted i or i_L instead of i_{Lf} for clarity. Similarly, the capacitor voltages are denoted V instead of V_c . This is because these are the only two measurements taken for feedback control on the dual-inverter prototype.

1.3 Acronyms

This section lists all acronyms used in this report, in alphabetical order. Page numbers to instances of these acronyms are also included.

AC Alternating Current. 7–9, 13, 14, 24, 25, 35

ADC Analogue-Digital Converter. 39

CMC Common Mode Choke. 8, 11, 12, 38

DC Direct Current. 7–9, 11, 13, 24–26, 39, 47

EMI Electromagnetic Interference. 9, 11, 25

ESR Equivalent Series Resistance. 40

ESS Energy Storage System. 13

EVM Inverter Evaluation Module BOOSTXL-3PhGaNInv. 22, 25, 27–29, 31, 38, 43, 46, 47

GFL Grid Following. 4, 7, 8, 12–18, 21–23, 34, 35, 39–42, 44, 45, 47, 52–54

GFM Grid Forming. 4, 7, 8, 12–16, 18–24, 41–45, 47, 52–54

HVDC High Voltage DC. 7

IBR Inverter-Based Resource. 4, 7, 13, 14, 44, 47

- IGBT** Insulated-Gate Bipolar Transistor. 9, 24, 25
- LPF** Low-Pass filter. 16, 17, 35, 44
- PCB** Printed Circuit Board. 4, 8, 26, 28, 30–32, 38, 46, 57
- PCC** Point of Common Coupling. 13, 14, 23, 44
- PI Controller** Proportional-Integral Controller. 7, 15, 16, 18, 20, 47
- PLL** Phase-lock loop. 7, 13, 14, 16, 17, 19, 34, 35, 42–44, 47, 52
- PV** Photovoltaic. 13
- PWM** Pulse-width Modulation. 9, 11, 12, 18, 25, 28, 47
- RCP** Rapid Control Prototyping. 4, 7, 25, 28, 44, 46
- RES** Renewable Energy Source. 7
- RMS** Root Mean Square. 24, 38
- RTT** Real-time Targets. 4, 7, 8, 47, 52, 55
- SRF** Synchronous Reference Frame. 7, 14, 16, 35
- TIM** Thermal Interface Material. 26
- UPS** Uninterruptible Power Supply. 13
- VCO** Voltage-Controlled Oscillator. 17, 19, 44
- VSC** Voltage Source Converter. 9, 13

2 Abstract

The motive of the project is to develop a small-scale inverter prototype combined with **Rapid Control Prototyping (RCP)** technology, which has been shown an effective experimental tool for the design and validation of control algorithms for **Inverter-Based Resources (IBRs)** in power systems. Throughout the project, a three-phase dual-inverter prototype has been designed, extensively tested in simulation, built with hardware, and deployed with careful tuning of controllers. The result is a hardware prototype capable of operating the two inverters in closed-loop and connected to each other, where one operates in **Grid Following (GFL)** mode controlling its output power, and the other in **Grid Forming (GFM)** mode fixing its terminal voltage. In combination, the dual-inverter prototype and Simplus **RCP** system offers a robust and versatile platform for the the teaching and research of grid-connected **IBR**.

3 Acknowledgements

I would like to express my greatest gratitude to Dr Yue Zhu, for his constructive guidance offered throughout the way. I not only developed a much deeper understanding on power converters and their control strategies, but also the freedom to experiment with building (and failing) electronics designs, something which would not have been possible without his supervision. He has also brought a suitcase of inductors from home for this project, which is admirable. In addition, I would like to wholeheartedly thank Professor Tim Green and Dr Yunjie Gu for offering invaluable advice when the project was at critical crossroads.

Moreover, the project is part of the Maurice Hancock Laboratory Team's collaborative effort to upgrade the lab's network of **IBRs**. The team has developed Simplus, the Simulink-based **RCP** system for controlling **Real-Time Targets (RTTs)** in this project. My work lies upon the solid foundation of the team's research efforts, and for this I would like to extend my gratitude to the team for making this a learning opportunity for me.

The technical support I have received over the course of my FYP is also instrumental to the hardware I have managed to build. Firstly I would like to thank Mr Victor Boddy for supervising and guiding me through milling screw-holes in the aluminium heat-sink, with a pillar drill. Otherwise, I would have had to wait 3 weeks to get it milled professionally at the Mechanical Workshop! In addition, I would like to thank Dr Adria Junyent-Ferre for teaching me to use the Banham **Printed Circuit Board (PCB)** miller in the Laboratory. This has allowed me to make quick prototypes at early stages of the project, which has been a great convenience and time-saver.

And as the project marks the final piece of submitted work for my degree, I realise I am greatly indebted to my parents Chris and Pamela, who have been supportive of my aspirations all my life. Their unwavering support is important to who I am. Last but not least, I would like to praise my almighty God, who has been faithful, loving and merciful. While He has been present my whole life, it is in my most challenging moments that His grace prevails.

Contents

1 Cover Notes	2
1.1 Plagiarism Statement	2
1.2 Symbols	2
1.3 Acronyms	2
2 Abstract	4
3 Acknowledgements	4
4 Introduction	7
4.1 Project Objective	8
4.2 Report Layout	8
5 Background and Analysis	8
5.1 3-Phase Inverter Hardware	8
5.1.1 3-Phase Half-Bridge Inverter Topology	9
5.1.2 LCL Filter Design	9
5.1.3 Common Mode Choke Design	11
5.2 Inverter dynamics	12
5.2.1 Inverter plant equations	12
5.2.2 Inverters in GFL and GFM Modes	13
5.3 Control of inverters	14
5.3.1 Reference Frames	15
5.3.2 Current-mode vs Voltage-mode Control	15
5.3.3 GFL Phase Lock Loop (PLL)	16
5.3.4 GFL Power to Current Reference Conversion	17
5.3.5 GFL Current Control and GFM Inner-Loop Current Control	18
5.3.6 GFM Voltage-Controlled Oscillator (VCO)	19
5.3.7 GFM Outer-loop voltage control	19
5.3.8 Summary for GLF and GFM Operation	21
6 Implementation	21
6.1 System Overview	22
6.2 Hardware Specification	24
6.3 Component Selection and Measurement Circuits	25
6.3.1 Inverter Selection	25
6.3.2 Load Resistor Considerations	25
6.3.3 Capacitor Voltage Measurement	26
6.3.4 Amplification for Inductor Current and DC Bus Voltage Measurement	27
6.4 Circuit Designs	28
6.4.1 Design 1: Initial tests for the LCL filter	28
6.4.2 Design 2: Dual-inverter System	29
7 Results for RCP deployment on simulations and hardware	34
7.1 Controller Parameter Initialisation	34

7.2 Inverter in open-loop	34
7.2.1 Simulation of open-loop inverter with a passive load	34
7.2.2 Hardware test for open-loop inverter with passive load	38
7.3 GFL inverter in closed-loop	39
7.3.1 Simulations of GFL inverter with stiff grid	39
7.3.2 Hardware test of GFL inverter with open-loop voltage generator	41
7.4 GFM inverter in closed-loop	42
7.4.1 Simulations of GFM inverter in closed-loop with passive load	42
7.4.2 Hardware test of GFM inverter connected to passive load	43
7.5 Both inverters in closed-loop	43
8 Conclusion	44
8.1 Evaluation	46
8.2 Works Performed	46
8.3 Further Works	47
9 Appendices	48
9.1 User Guide: Accessing Simulink Model Files and Design Scripts	52
9.1.1 Simulations	52
9.1.2 Running Simplus Models	52
9.1.3 Results	53
9.2 Dual-Inverter System (Design 2) Files	57

4 Introduction

With the construction of power transmission and public lighting systems in the late 19th century, a war of currents grew between Thomas Edison's Edison Electric Light Company and George Westinghouse's Westinghouse Electric Corporation, in which Edison was a proponent of **Direct Current (DC)** and Westinghouse of **Alternating Current (AC)** power transmission[1]. Over time, AC power has proven itself a more efficient solution for power over long distances, which has enabled the construction of centralised generation stations that support the livelihoods of the population and support economic centres across the nation. Despite Edison's initial efforts in promoting that AC power systems were hazardous, electrical systems across the globe have since then been developed on AC power, with the exception of recently emerging **High Voltage DC (HVDC)** transmission links for ultra-long distance power transmission [2].

As established in the 2015 Paris Agreement, the United Nations has set a goal to reduce emissions by 45% by 2030, and to achieve reach net zero by 2050 [3]. Since then, efforts have been made to reduce polluting sources of generation, by replacing coal, gas and other forms of fossil fuel generation with **Renewable Energy Sources (RES)**, such as wind and solar energy farms. While the operation of fossil-fuel-fired plants are often characterised by synchronous generation where the frequency of the **AC** current injection is determined by the rotation of the machines, **RES** are characterised by **IBRs** where the source does not physically couple with the generated frequency [4]. Instead, the source is of an **IBR** is interfaced to mains **AC** power grids via a power electronic inverter.

As a result of higher demand for the **RES**, there has been a rapid increase in **IBRs** deployment. Challenges of **IBRs** have been raised, such as the large variations of **RES** generation over time, and compliance with strict grid code requirements [5]. Therein lies numerous opportunities to study the behaviour of **IBRs** to improve the efficiency, stability and longevity of inverters, in both stiff AC grid systems or islanded conditions.

The Maurice Hancock Energy Laboratory offers an extensive and versatile system of lab-scaled inverters which form a 100% **IBR** system. With careful deployment of suitable control strategies, the inverters on the system can behave either in **GFL** or **GFM** mode, as detailed in subsection 5.2.2. This enables experiments for various applications to be performed, allowing the observation of characteristics such as power exchange efficiency and fault protection capabilities. An important tool of the system is **RCP**, which enables engineers to quickly modify the control algorithms on an intuitive block-based MATLAB Simulink Interface without programming error-prone low level code [6]. **RCP** transforms it into an embedded implementation to be deployed, and **RTTs** can be modified during run-time. Among the algorithms commonly deployed on a power converter control systems are **Proportional-Integral (PI) Controllers** for current or voltage reference tracking, **Phase-lock loop (PLL)** for obtaining the phase of a signal, and frame transformation for control in the **Synchronous Reference Frame (SRF)**.

The retirement of support for the Triphase inverter's built-in controller in the lab effectively renders the system obsolete in the near future, which necessitates the development of a new system. Simplus, a new Simulink **RCP** system designed by the Maurice Hancock Laboratory Team, enables convenient modification of **RTTs** during run-time for tuning optimal performance.

Therefore, the ultimate objective of the project is to fully develop, test and verify the Simplus **RCP** on a multi-inverter system prototype, so as to facilitate future deployment in the lab's new 15 kVA inverter system.

4.1 Project Objective

The project will start from a simulation on MATLAB Simulink, which would entail verifying open-loop, **GFL** and **GFM** inverter operation, as well as designing suitable control algorithms for the new system. The majority of efforts would then be spent on hardware development, which includes designing, building and testing the **PCB**. The final and most significant step is to extensively tune and test the controllers, to fully demonstrate the entire system with **RTT** control in place.

4.2 Report Layout

Following the introduction and project specifications above, the report begins with a background and analysis section, section 5, that discusses three core areas of theoretical concepts related to inverters, namely their hardware design, dynamics and control. The implementation of the hardware is subsequently explained in section 6, where detailed justification is offered for various design decisions made. This is proceeded with section 7, a discussion of results for operation in various configurations, both in simulation and on hardware. Finally, section 8 closes the report with a conclusion of the work undergone in the project, an evaluation of the dual-inverter system in terms of its ability to validate the lab's new 15 kVA system, and potential future work for the system.

5 Background and Analysis

5.1 3-Phase Inverter Hardware

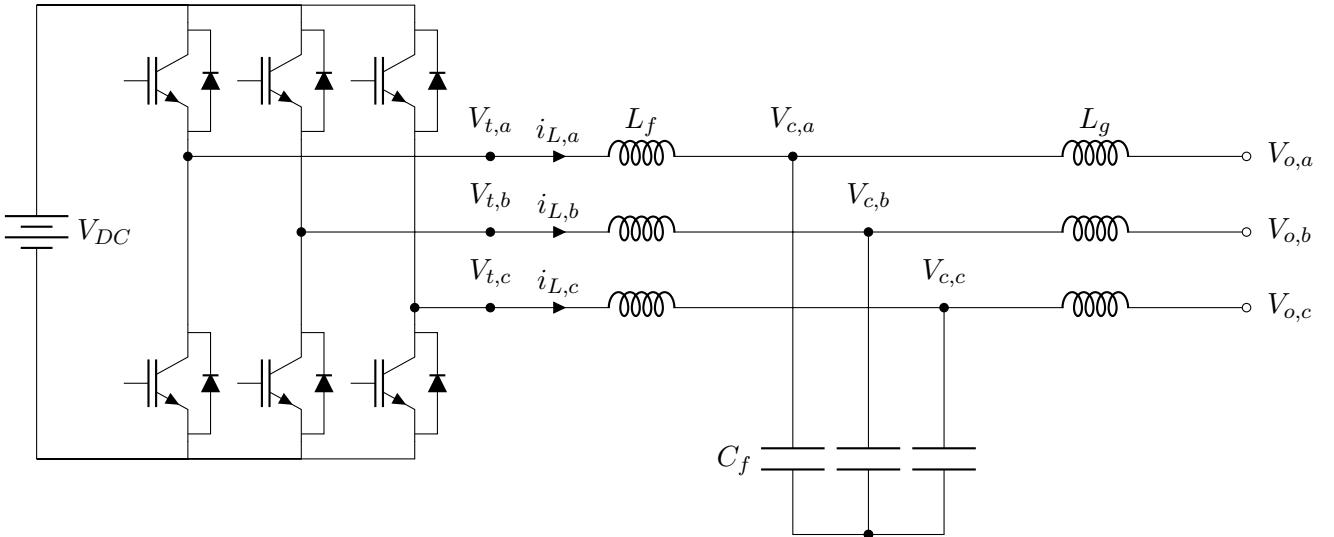


Figure 2: Lossless inverter omitting measurement and control path signals for switch modulation. The output terminals are intentionally left disconnected in the diagram, as it could be connected to a load or a stiff grid.

As an overview, the studied inverter system is shown in figure 2. This subsection explores the role of various components in this system, including the 3-phase half-bridge inverter for **DC-AC** conversion, the LCL filter which serves to suppress ripples and harmonics at the required operating conditions, and a **Common Mode Choke (CMC)** for disturbance rejection.

5.1.1 3-Phase Half-Bridge Inverter Topology

A DC-AC single-phase half-bridge converter consists of 2 switches operating in complementarity with a sinusoidal Pulse-width Modulation (PWM) strategy as discussed in [7]. Its AC grid voltage V_{AC} is capable of swinging between $\pm V_{DC}/2$, whose amplitude is defined by the duty cycle δ of the upper switch. For instance, a sinusoidal duty cycle of $\delta = 0.3\sin(\omega_0 t) + 0.5$ leads to the AC voltage $V_{AC} = 0.3V_{DC}\sin(\omega_0 t)$ relative to its neutral point. A dead-time between the on-time of both switches is typically incorporated to ensure that the current in each switch has fully commutated, to prevent of shoot-through current between the two-switches and leading to a DC bus voltage short circuit. Finally, three single-phase half-bridge converters form a 3-phase half-bridge inverter or two-level Voltage Source Converter (VSC) as shown in figure 2, where the duty cycle of each phase is delayed by 120° to achieve a balanced 3-phase grid voltage [8].

5.1.2 LCL Filter Design

As outlined in [9], filters are an extensively researched topic in power electronics, as a poor filter design can result in distortion or lower attenuation as a result of resonances. The ultimate goal is to design a filter that can suppress the ripple at a reasonable cost, and with total harmonic distortion (THD) across all frequencies. While the L or LC filter is sufficient for most low-pass filter purposes, the component size must be reduced by increasing operation frequency, an option not typically suited for Insulated-Gate Bipolar Transistor (IGBT) DC-AC power-electronics converters, which are limited to operation at lower switching frequencies due to switching stresses and Electromagnetic Interference (EMI) considerations.

An LCL filter is one of the most selected topologies, for its more favourable attenuation characteristics at lower switching frequencies [10], and its ability to achieve this with reduced inductor size, volume, and cost. The ripple magnitude of high-frequency harmonics can be reduced up to 50% [9], due to the existence of the grid-side inductor L_g and capacitor C_f which further attenuates current harmonics and significantly reduces the stress on the converter-side inductor L_f [11]. Besides the design flexibility advantage, L_g also provides better decoupling between the filter and grid impedance [12]. However, one notable disadvantage of an LCL filter is the resonance at certain frequencies associated with the third order loop gain transfer function, which leads to closed-loop instability [13].

To mitigate this resonance, there are various topologies for passive damping, including the addition of a passive damping resistor R_{damp} in series with the filter capacitor C_f , a LLCL filter topology as proposed in [11], and a parallel RC branch or series L||R branch as proposed in [10]. However, these should be considered with caution, as damping can be influenced by grid impedance deviation and uncertainty in grid frequency. In addition, the resistance will incur additional losses below the resonant frequency.

For an effective design, an appropriate starting point is to take into consideration the desired current ripple, reactive power absorption and resonant frequency.

Firstly, L_f serves the same purpose as the inductor in an LC filter, and is designed with respect to the desired current ripple $\Delta i_{L_f,\max}$, in this case $y = 10\%$ of the rated current i_{rated} . Note the converter-side inductor currents is denoted i_{Lf} in this section as opposed to the i_L in the rest of the report, to differentiate it from the grid-side inductor current i_{Lg} . $i_{Lf,\max}$ is derived as follows [14]:

$$\Delta i_{Lf,\max} = \frac{1}{8} \cdot \frac{V_{dc}}{L_f \cdot f_{sw}} = y \cdot i_{rated}$$

This can be rearranged to give L_f :

$$L_f = \frac{1}{8} \cdot \frac{V_{DC}}{\Delta i_{Lf,max} \cdot f_{sw}} \quad (1)$$

Secondly, a capacitor C_f offers a low impedance path for high frequency switching current harmonics generated by the inverters. Following a per-unit based approach, the base impedance Z_b and base capacitance C_b with respect to the rated grid-side power P_{rated} and rated grid-side voltage V_{rated} are:

$$Z_b = \frac{V_{rated}^2}{P_{rated}}$$

$$C_b = \frac{1}{2\pi f_{AC} Z_b}$$

An overly large C_f would draw more reactive power and current from the switching, which lowers the efficiency. In contrast, a small or absent C_f would make V_o heavily dependent on the grid or load impedance. To meet the same attenuation requirements, a large inductor would be required, leading to a larger voltage drop between the terminals and the output.

As C_b is a quantity directly proportional to power, an arbitrary design factor can be applied to adjust reactive power absorption. With respect to the considerations aforementioned, a balance between current efficiency and voltage drop can be achieved by designing C_f to $x = 5\%$ of reactive power absorption or 'power factor variation'. The capacitance is then designed as:

$$C_f = x \cdot C_b = x \cdot \frac{1}{2\pi f_{AC} Z_b} \quad (2)$$

Finally, given the desired attenuation ratio $y = i_{Lg}/i_{Lf}$ and the transfer function from the converter terminal voltage to the ripple $\Delta i_{Lg}/\Delta V_t$ [15],

$$\frac{\Delta i_{Lg}}{\Delta V_t} = \frac{1}{L_f L_g C_f s^3 + R_g C_f L_f s^2 + (L_f + L_g)s + R_g}$$

This equation can then be simplified and rearranged such that L_g is selected as follows [16]:

$$L_g = \frac{1/y + 1}{C_f \omega_{sw}^2} \quad (3)$$

The resonance frequency ω_{res} is an important quantity that must be verified, either a priori or a posteriori. It should not coincide with the grid or switching frequencies, to avoid resonance with either the grid impedance or switch output impedance. Otherwise, harmonics in the voltage and currents can potentially jeopardise system stability. As a rule of thumb, the resonance frequency should lie in the range [16]

$$10\omega_{AC} < \omega_{res} < 0.5\omega_{sw} \quad (4)$$

As an optional addition, a passive damping resistor R_{damp} can be connected in series with C_f . This atten-

uates the magnitude of ripple on the switching frequency and reduces resonance. An effective design for the damping resistor would be [12]:

$$R_{damp} = \frac{1}{3 \cdot w_{res} \cdot C_f} \quad (5)$$

5.1.3 CMC design

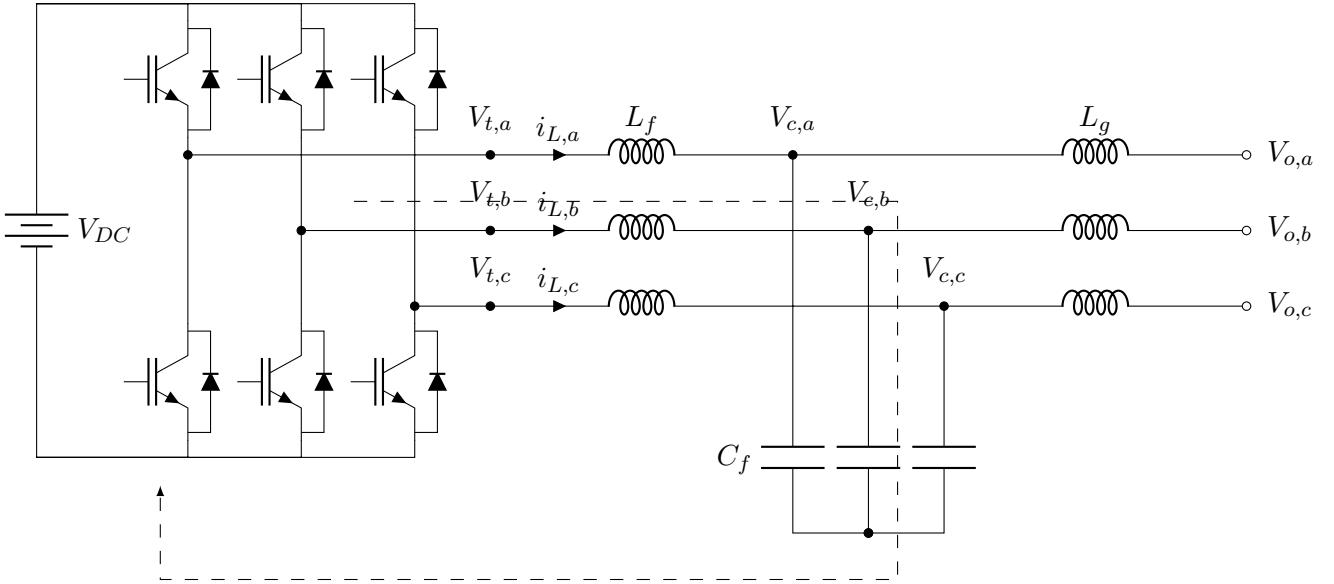


Figure 3: Common mode noise flow, indicated by dashed arrow.

The common mode voltage \$V_{CM}\$ at the terminals of the inverter is defined as:

$$V_{CM} = \frac{V_{t,a} + V_{t,b} + V_{t,c}}{3} \quad (6)$$

It is the voltage difference between the capacitor neutral point and the **DC** ground, where the change between switching states \$\Delta V_{CM}\$ can reach \$\pm V_{DC}/2\$ if a space-vector **PWM** strategy is adopted, or \$\pm V_{DC}/3\$ if a sinusoidal **PWM** strategy is adopted[17]¹. Rapid changes in common mode voltage \$\Delta V_{CM}\$ can lead to high pulsed common-mode currents circulating through stray capacitances formed between the capacitor and **DC** ground, as shown in figure 3. Besides common mode currents that arise from the transition between these switching stages, there is also some common mode noise as a result of power supply noise propagating through all 3-phases simultaneously. This leads to worsened distortion and **EMI**.

Though not a strictly necessary part of an inverter output filter, a **CMC** attenuates common mode noise effectively. The magnetic flux created by the common-mode currents accumulate, thereby producing an inductive impedance that opposes the common-mode currents [18]. This noise consequently returns to the source via \$C_f\$ and stray capacitances that connect the capacitor neutral to the **DC** ground. Similar to the design of an inductor, several factors are considered, including:

¹The maximum \$\Delta V_{CM}\$ for SPWM modulation is \$\pm V_{DC}/3\$, not to be confused with the fact that the maximum \$V_{CM}\$ remains \$\pm V_{DC}/2\$ in states \$(m_a, m_b, m_c) = (0, 0, 0)\$ or \$(m_a, m_b, m_c) = (1, 1, 1)\$

1. Amount of common mode current ripple attenuation, which determines the inductance and the number of turns required,
2. Frequency of the noise, which impacts the effective impedance of the windings,
3. Wire size, which determines the resistive losses and temperature rise; and,
4. Number of turns and core cross-section, which ensures the required common mode current can flow without saturating the core.

Extensive research has been performed for CMC [19], but for the purposes of this project an off-the-shelf CMC was used. In addition, the use of the sinusoidal PWM (SPWM) instead of space-vector PWM (SVPWM) has relaxed the common mode noise, so the CMC was later found ineffective. A decision was then made to short-circuit the CMC.

5.2 Inverter dynamics

With respect to the inverter topology introduced in subsection 5.1, this subsection first defines a plant model of an inverter's dynamics, providing the justification for a filter which ensures reliable operation, and controllers which compensate for errors at the desired operating power. This is followed by a discussion of inverters in GFL and GFM modes, and their overall control scheme.

5.2.1 Inverter plant equations

While the chosen filter topology is LCL, as the feedback voltage is often the capacitor voltage V_c instead of the output voltage V_o , the output dynamics are described by an LC filter.

Firstly, the voltage across the inductor is defined by the difference between the capacitor voltage $V_c(t)$ and the terminal voltage $V_t(t)$, with the voltage drop across the inductor resistance R (not to be confused with the load resistance R_{load}) and switch on-state resistances R_{on} subtracted. Hence, the relationship between $V_t - V_c$ and i_L can then be expressed as the following vector equation.

$$L_f \frac{d\vec{i}_L}{dt} = -(R + r_{on})\vec{i}_L + \vec{V}_c - \vec{V}_t = -(R + r_{on})\vec{i}_L + \vec{V}_t - \hat{V}_c e^{j\omega t + \theta_0} \quad (7)$$

where ω is the instantaneous AC-side (source) voltage frequency, and θ_0 is the source initial phase angle. In the Laplace domain, this can be expressed as follows.

$$G_L(s) = \frac{\vec{i}_L}{\vec{V}_t - \vec{V}_c} = \frac{1}{Ls + (R + r_{on})} \quad (8)$$

As a result of the transformations to the synchronous frame as described in subsection 5.3.1, the inductor dynamics couple the d and q-axis currents in the synchronous dq -frame, which will need to be decoupled to control the system [20], [21]:

$$L \frac{di_{L,d}}{dt} = (L \frac{d\rho}{dt}) i_{L,q} - (R + r_{on}) i_{L,d} + V_{t,d} - \vec{V}_c \quad (9)$$

$$L \frac{di_{L,q}}{dt} = -(L \frac{d\rho}{dt}) i_{L,d} - (R + r_{on}) i_{L,q} + V_{t,q} - \vec{V}_c \quad (10)$$

ρ represents the phase associated with the rotational speed of the dq -frame relative to the stationary abc -frame. A **PLL** ensures $\rho = \omega_0 t + \theta_0$, or that the rotational speed of the dq -frame is synchronous with that of the grid, as further described in subsection 5.3.3.

These equations describe the relationship between the current and terminal voltage error of a current-controlled **VSC**, and as such they represent the plant model when controlling the current in closed-loop. Similarly, the load voltage dynamics across the capacitor can be expressed with the following vector equation.

$$C_f \frac{d\vec{V}_c}{dt} = \vec{i}_{Lf} - \vec{i}_{Lg} \quad (11)$$

In the Laplace domain, this can be expressed as follows.

$$G_C(s) = \frac{\vec{V}_c}{\vec{i}_{Lf} - \vec{i}_{Lg}} = \frac{1}{C_f s} \quad (12)$$

Analogous to the inductor dynamics, the real and imaginary voltage are coupled in the synchronous dq -frame as a result of the transformation:

$$C_f \frac{dV_{c,d}}{dt} = C_f \left(\frac{d\rho}{dt} V_{c,q} \right) + i_{Lf,d} - i_{Lg,d} \quad (13)$$

$$C_f \frac{dV_{c,q}}{dt} = -C_f \left(\frac{d\rho}{dt} V_{c,d} \right) + i_{Lf,q} - i_{Lg,q} \quad (14)$$

These equations describe the dynamics of the load voltage with respect to the current error. Therefore, they represent the plant model when controlling terminal voltage in the outer loop.

5.2.2 Inverters in **GFL** and **GFM** modes

An inverter can operate in 2 modes, depending on the need to 'follow' or 'form' a grid.

The first is a controlled-frequency **VSC** system, or inverter in **GFM** mode, which behaves such that the inverter control tracks references for the voltage output and operating frequency at $V_{c,abc}$ [8]. This is the configuration when the inverter is solely dedicated to supplying **AC** loads in a dedicated isolated network, and an example for this is an **Uninterruptible Power Supply (UPS)** providing backup power to a load in the event of a mains power failure.

In contrast, a grid-imposed **VSC**, or inverter in **GFL** mode, is such that the inverter output at V_{oabc} is connected to an **AC** system, via a switched connection called **Point of Common Coupling (PCC)**. The aim of this inverter is to control the power and reactive power exchange between the **DC** source and the **AC** grid, while ensuring that the output voltage is synchronous with the operating frequency of the **AC** system. This is a common topology for power networks, where **IBRs** are required to be interfaced to an **AC** grid with strong system strength. An example of this is connecting a farm of **Photovoltaic (PV)** panels or **Energy**

Storage System (ESS) to a grid [22], where the controller serves to correct the frequency as it deviates beyond the desired bandwidth.

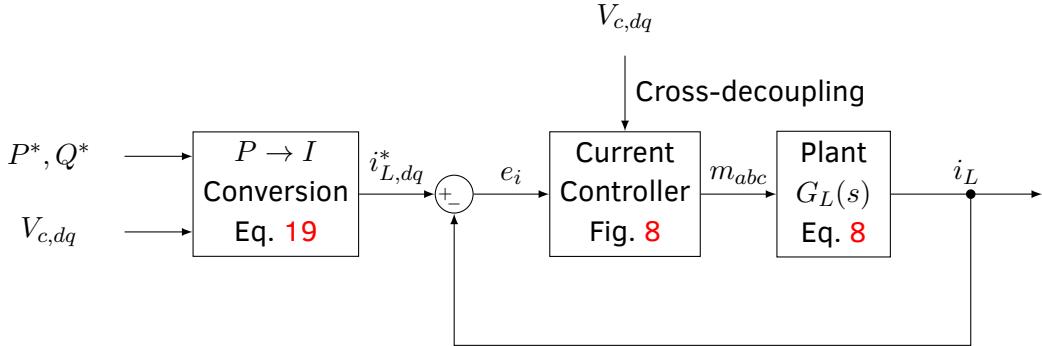


Figure 4: **GFL** control diagram.

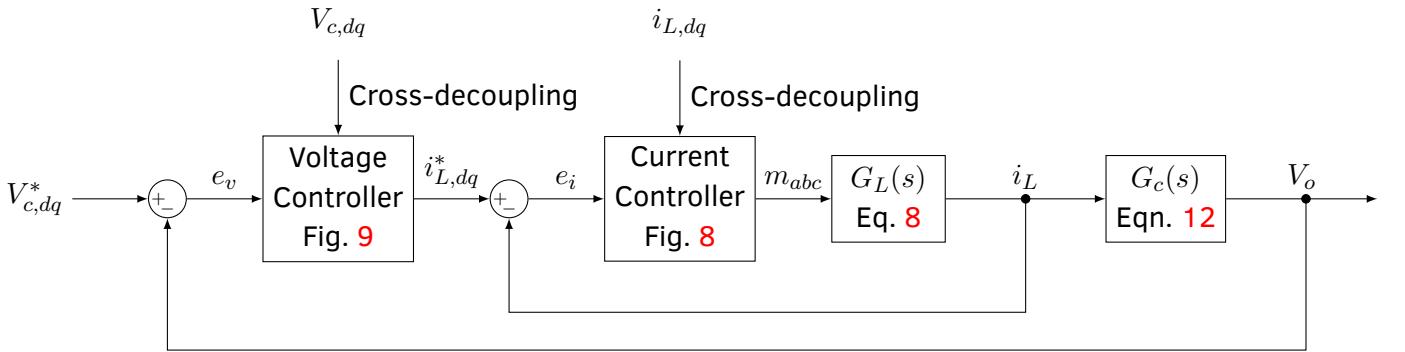


Figure 5: **GFM** control diagram.

High level control diagrams inverter in **GFL** and **GFM** modes are shown in figures 4 and 5 respectively[23], [24], omitting reference-frame transformations for simplicity. The control theory of both systems and each block are elaborately described in section 5.3.

As a note, it is important to recognise that an inverter can switch between these 2 modes of operation by opening the **PCC** switch, provided that the disturbance can be rapidly detected [25], [26]. For example, when the **AC** system strength is weak, or when an **IBR** is starting up from an **AC** grid blackout, the inverter needs to behave in **GFM** mode to regulate the **AC**-side voltage and frequency initially [22] [27]. Only when the **AC** system resumes nominal operating conditions and system strength can **GFL** operation be recovered; this is when the **PCC** switch can be closed.

5.3 Control of inverters

As was seen in subsection 5.2, the currents and voltages of an inverter are time-varying, normally sinusoidally in steady state, which presents challenges for control. This difficulty can be overcome by transformation to a **dq SRF** in which steady sinusoidal signals become DC; one way to form this reference is with a **PLL**. The transformed currents and voltages can subsequently be controlled with conventional PI controllers. Beginning with a brief discussion on reference frames and current-mode control for inverters, this subsection explores the control methodology for inverters operating in **GFL** and **GFM** mode.

5.3.1 Reference Frames

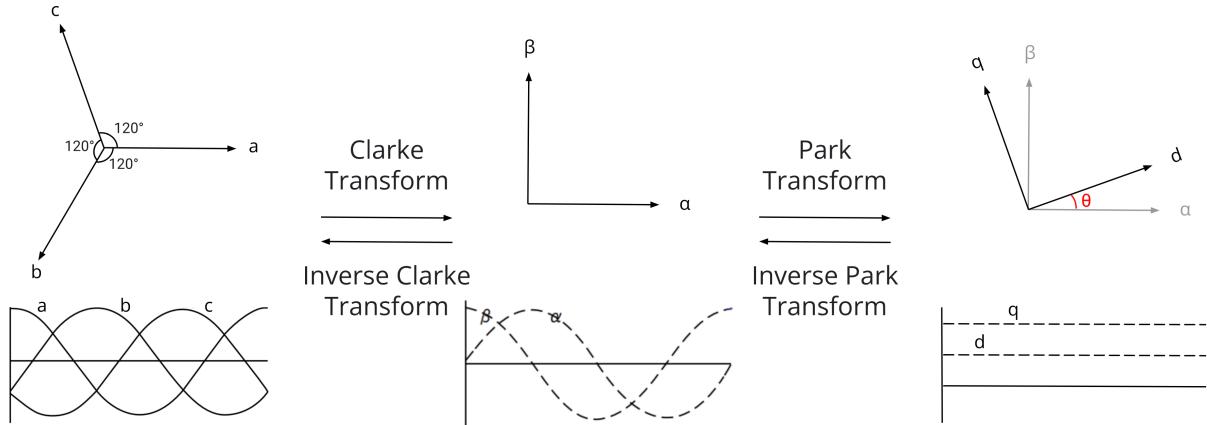


Figure 6: Frame transformations [28]

Time-domain voltage and current signals of an inverter can be expressed using a combination of quantities in different reference frames. Explaining in detail the transformations between each of these reference frames is beyond the scope of the report, but an intuitive description for each of them is offered below [29], alongside figure 6 which shows the relationship between these frames.

1. Stationary abc : 3 quantities of a balanced 3-phase system in a stationary co-planar reference frame,
2. Natural $\alpha\beta$: two time-varying orthogonal quantities in a stationary orthogonal frame; and,
3. Synchronous dq : two DC orthogonal quantities in a rotating orthogonal frame.

The synchronous dq frame is used for analysis of the small-signal dynamics of a power system, and is a suitable domain for control strategies to be implemented effectively for both **GFL** and **GFM** inverters [30], as it encapsulates the information of a time-varying AC signal in 2 signals which are DC or time-invariant in steady state. This enables the control signal to be DC, such that the integral term in a **PI Controller** can therefore achieve zero steady-state error for tracking [31].

Furthermore, in contrast to the coupling between phases in a stationary 3-phase frame, using cross-coupling terms in the dq domain decouples the real and imaginary component of a signal, which allows injection or consumption of real and reactive power to be separately controlled.

Note that a power-invariant transform is used throughout this project, where dq voltage and current values represent the amplitude of their abc counterparts. This is to conform to the implementation of the $abc-dq0$ and $dq0-abc$ block in Simscape Electrical's Specialised Power System Library.

5.3.2 Current-mode vs Voltage-mode Control

While voltage-mode control is utilised for high voltage and power applications [32], current-mode control for an inverter allows protection of over-currents in the switches and in the output line currents. Other cited advantages are robustness against variations in operating conditions, dynamic performance and control precision [33]. This enables the current harmonics of the system to be controlled, so as to meet the regulations on total harmonic distortion (THD) imposed by National Grid [5].

For that reason, current-mode control has been chosen for both **GFL** and **GFM** modes. However, the current reference is generated differently depending on the mode. Whereas the former generates a current reference with respect to an output voltage reference (section 5.3.7), the latter is generated with real and reactive power references (section 5.3.4). The dynamics of a current-controlled inverter and current tracking method is discussed in depth in subsection 5.3.5.

5.3.3 **GFL** Phase Lock Loop (PLL)

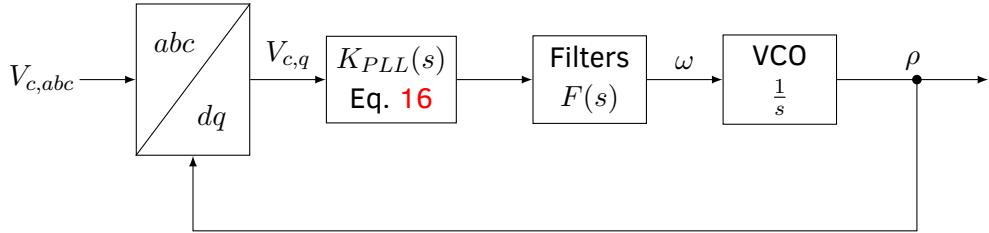


Figure 7: PLL control diagram.

To explore the role of a **PLL** for a **GFL** inverter, the dynamics of the inverter are briefly revisited. Firstly, the inverter's AC-side voltage $V_{c,abc}$, when expressed in space vector form is

$$\vec{V}_c(t) = \hat{V}_c e^{j\omega t + \theta_0} \quad (15)$$

where \hat{V}_c is the peak value of the capacitor voltage, ω is the AC-side (source) voltage frequency, and θ_0 is the source initial phase angle.

In order to convert *abc*-signals to stable DC signals for control in the *dq*-frame, the frame must be synchronised with the grid voltage, i.e., rotate at an angular velocity ω_0 identical to the grid frequency and at the same phase ρ relative to the terminal voltage. Similarly, when converting *dq* signals to *abc* domain, the transform must rotate at the same speed to ensure that the reference is frequency and phase synchronous to the grid [34], [35]. Hence, the **PLL** serves to track the grid phase and frequency $\omega t + \theta_0$ [36].

There are various methods of implementing a **PLL** as summarised in [37]. The first of which is to use three single-phase **PLL** as described in [38], which eliminates the need for an *abc* – *dq* transformation at the cost of its inability to detect unbalanced conditions. The second, more commonly-adopted approach, is to translate the control variables to the *dq SRF*, such that is capable of following the positive sequence grid voltage under fault conditions. An example of a **SRF PLL** is proposed in [39], which also incorporates a notch-filter and lead-lag compensator to achieve both high bandwidth with selective cancellation. Similar non-conventional high-order filters is proposed in [40], which is tuned to precisely detect phase angle in the presence of 5th and 7th order harmonics. A method utilising symmetrical optimum is presented in [41], for operation under common utility distortions.

A **SRF PLL** consisting of a generic **PI Controller** and **Low-Pass filter (LPF)** without damping compensation shall be chosen for an initial implementation. This begins with a generic **PI Controller** $K_{PLL}(s)$ with equations defined as follows [42]:

$$K_{PLL}(s) = \frac{k_p s + k_i}{s} \quad (16)$$

where k_p and k_i are the proportional and integral gains respectively. With respect to figure 7, the loop gain is therefore:

$$L_{PLL}(s) = K_{PLL}(s) \frac{1}{s} = \frac{k_p s + k_i}{s^2} \quad (17)$$

A generic loop shaping method is then adopted to select the gains k_p and k_i with respect to the crossover and cutoff frequency[24]. The crossover frequency or bandwidth is typically chosen at a lower value to maintain stability in the event of distortion or imbalance. To achieve zero steady-state error, loop gain should be established as unity at crossover frequency ω_c , or $|L_{PLL}(j\omega_c)| = 1$. Moreover, the zero at $s = k_i/k_p$ defines the cut-off frequency $\omega_1 = \omega_c/x$ of $L(s)$, such that $k_i = k_p \omega_c / x$. In combination, the gains are justified as follows:

$$k_p = \sqrt{\frac{\omega_c^4}{\omega_c^2 + \omega_1^2}} \quad k_i = k_p \frac{\omega_c}{x} \quad (18)$$

Suppose the **PLL** is suitably designed with a rapid and stable response, whose output ρ adjusts the rotational speed of the $abc - dq$ and $dq - abc$ blocks. Consequently, the error between ρ and $\omega t + \theta_0$, and hence the reactive voltage $V_{c,q}$, shall be compensated to zero such that the phase of the reference and grid are synchronous, or $\hat{V}_c = V_{c,d}$. Otherwise, the output of the $K_{PLL}(s)$ compensator $\delta\omega_0$ is the error relative to the grid frequency of 50 Hz, which the **PLL** is centred at. ω is then passed into a **Voltage-Controlled Oscillator (VCO)** or mod- 2π integrator to generate ρ .

Finally, a **LPF** shall be added to attenuate the response to high frequency components, so as to minimise fluctuations associated with sinusoidal components of $V_{c,q}$. The filter complexity will be experimented with depending on the discretisation constraints. In addition, the post-compensation saturation block imposes limits on ρ , which prevents the system from swinging out of stability and ensures a correct initial state.

In summary, a diagram describing the **PLL** controller is shown in figure 7 [36], [43]–[45].

5.3.4 **GFL** Power to Current Reference Conversion

As introduced in section 5.2.2, the aim of a current-controlled **GFL** inverter is to control power exchange. This necessitates the need for a transformation from power references P^* and Q^* to current references $i_{L,d}^*$ and $i_{L,q}^*$, as the chosen inverter is a current-controlled device as discussed in subsection 5.3.2. In combination with the instantaneous real and quadrature voltage $V_{c,d}$ and $V_{c,q}$, this transformation can be achieved as shown by the following equations:

$$i_{L,d}^* = \frac{P^* V_{c,d} + Q^* V_{c,q}}{V_{c,d}^2 + V_{c,q}^2} \quad i_{L,q}^* = \frac{-P^* V_{c,q} + Q^* V_{c,d}}{V_{c,d}^2 + V_{c,q}^2} \quad (19)$$

These equations are form the $P \rightarrow I$ conversion block shown in the **GFL** control diagram on figure 4.

Conversely, the instantaneous currents $i_{L,d}$ and $i_{L,q}$ be utilised to compute the instantaneous power P and Q for comparison against the references P^* and Q^* :

$$P = V_{c,d}i_{L,d} + V_{c,q}i_{L,q} \quad Q = -V_{c,d}i_{L,q} + V_{c,q}i_{L,d} \quad (20)$$

5.3.5 GFL Current Control and GFM Inner-Loop Current Control

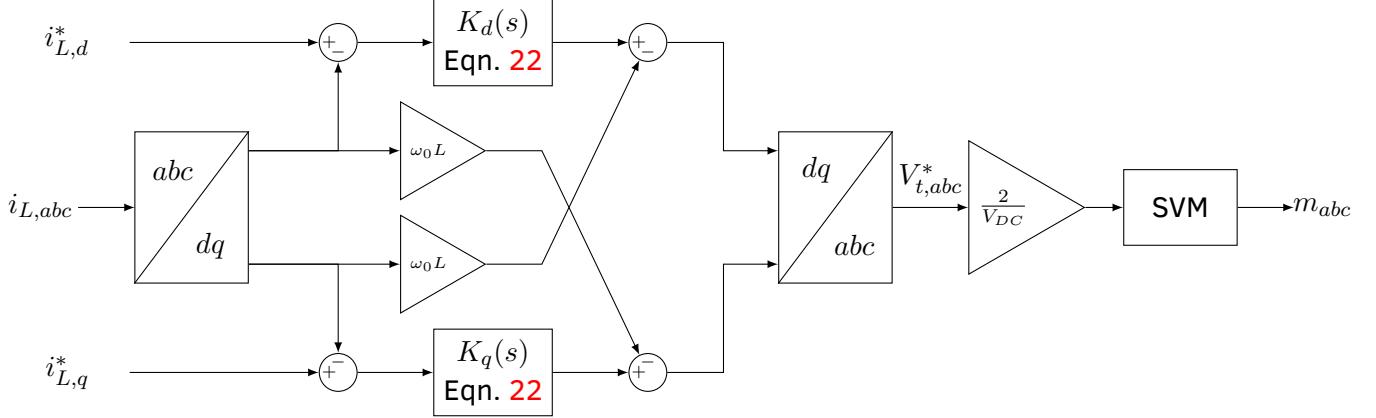


Figure 8: Current control scheme for GFL inverters, and for inner-loop control of GFM inverters.

This subsection presents the current controller of a GFL converter as shown in figure 4 and the inner-loop current controller of a GFM converter as shown in figure 5. Both utilise the same topology, with different gains chosen depending on the desired bandwidth.

The current controller takes in the converter-side inductor current i_L as a feedback signal and transforms it into the dq -frame. After compensating for the feedback error and decoupling the real and imaginary components cross-decoupling gains, the control signal is conversely transformed into a voltage reference signal in the abc domain [46]. This is scaled to return the duty cycle of the 6 switches, and modulated into PWM switch signals using sinusoidal or space-vector PWM as described in [7], [47]. The goal of regulating P , Q and i_L is ultimately achieved through adjusting the effective AC-side terminal voltage V_t .

To effectively track the current reference i_L^* , the compensators must be designed correctly. A good controller is designed in conjunction with considerations for the topology of a filter [9], [48], as a system's stability is very sensitive to filter parameters which impact resonance and damping effects. Various elaborate methods have been proposed to control the current of an inverter, such as including resonance control for a shunt active power filter (SAPF) [49], or using a conventional PI Controller accompanied with various damping techniques. Furthermore, active damping control is an area that is widely explored, allowing the system's desired control bandwidth and damping factor to be realised instantaneously [9], [50]. Nevertheless, the diminishing returns on stability benefits, as well as complicated discretisation implications of implementing a high-order controller makes a conventional PI Controller accompanied with passive damping the most appropriate solution.

Suppose the compensators $K_d(s)$ and $K_q(s)$ are generic PI Controllers as defined in equation 16, such that $K(s) = K_d(s) = K_q(s)$. Considering the inverter dynamics described in equation 8, the loop transfer function $L(s)$ of the current controller is:

$$L(s) = G_L(s)K(s) = \frac{1}{Ls + (R + r_{on})} \frac{k_p s + k_i}{s} = \frac{k_p}{Ls} \times \frac{s + k_i/k_p}{s + (R + r_{on})/L} \quad (21)$$

Following the cut-off and crossover frequency loop shaping methodology outlined in section 5.3.3, the gains are approximately justified as follows:

$$k_p = \omega_c L \quad k_i = k_p \frac{\omega_c}{x} \quad (22)$$

However, the selection of τ_i presents a trade-off. For fast response, a small τ_i is required. In contrast, for the corresponding bandwidth of $1/\tau_i$ to be smaller (typically 10 times smaller) than the switching frequency, τ_i must be sufficiently large. A typical selection of a τ_i for this application is 0.5-5ms, which is more than 10 times smaller than the switching frequency of 10kHz.

A further simplification is described in [8], where the time constant of the system is selected to control the response speed of the system. If the k_p and k_i gains are chosen as:

$$k_p = L/\tau_i \quad k_i = (R + r_{on})/\tau_i \quad (23)$$

the current-tracking closed loop transfer function $T_i(s) = I(s)/I^*(s)$ then becomes

$$T_i(s) = \frac{I(s)}{I^*(s)} = \frac{L(s)}{1 + L(s)} = \frac{1}{\tau_i s + 1} \quad (24)$$

Nevertheless, the method returns a set of gains which are similar to that derived for equation 21. The difference in integral gains obtained from the 2 methods largely influence the phase margin of the system, which can be further tuned during implementation.

5.3.6 GFM Voltage-Controlled Oscillator (VCO)

A PLL is not required for closed-loop GFM operation as the grid phase is determined, and hence automatically synchronised with the voltage reference. However, as dq references are required for closed-loop current and voltage control, a VCO with input ω^* is required to generate ρ_{GFM} for GFM $abc - dq$ and $dq - abc$ blocks.

5.3.7 GFM Outer-loop voltage control

As previously introduced in section 5.2.2, a GFM inverter consists of an outer-loop voltage controller and an inner-loop current controller described in section 5.3.5. This subsection explores the design of the voltage controller, which is illustrated by the diagram in figure 9. It consists of a feedback controller and cross-decoupling terms for decoupling capacitor dynamics, such that $V_{c,d}$ and $V_{c,q}$ can be controlled separately to track references $V_{c,d}^*$ and $V_{c,q}^*$ respectively[23].

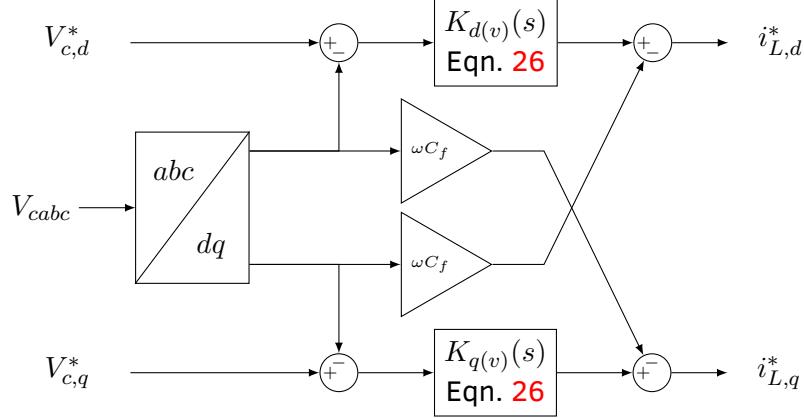


Figure 9: Outer loop voltage control scheme for GFM inverters.

To design the voltage controller, two poles have to be considered, namely:

1. Pole at origin due to the load voltage dynamic, as shown in equation 12; and,
2. Real pole at $s = -1/\tau_i$, associated with the closed inner-loop transfer function derived in equation 21. This simplification assumes that the inner loop operates at a higher bandwidth.

With respect to figure 5, using a generic **PI Controller** as described in equation 16 results in the loop transfer function $L_v(s)$:

$$L_v(s) = \frac{k_{pv}s + k_{iv}}{s} \frac{1}{sC_f} \frac{1}{\tau_i s + 1} \quad (25)$$

Following the crossover frequency and cut-off frequency loop shaping methodology outlined in section 5.3.3, the gains of $K_v(s)$ are approximately:

$$k_{pv} = \omega_c^2 \tau_i C_f \quad k_{iv} = k_p \frac{\omega_c}{x} \quad (26)$$

Nevertheless, designing two cascaded controllers is always a challenge. A design methodology with respect to the phase margin would be more suited for a outer-loop controller, allowing it to achieve fast regulation and zero steady-state error. As proposed in [51], "symmetrical optimum" is a design methodology that considers these constraints, utilising a **PI Controller** described as follows:

$$K'_v(s) = k \frac{s + z}{s} \quad (27)$$

This results in the open-loop gain:

$$L'_v(s) = \frac{k}{\tau_i C_f} \frac{s + z}{s + \tau_i^{-1}} \frac{1}{s^2} \quad (28)$$

Using frequency response analysis, the crossover frequency ω_m and phase margin δ_m for $L_v(s)$ are:

$$\delta_m = \sin^{-1} \frac{1 - \tau_i z}{1 + \tau_i z} \quad (29)$$

$$\omega_m = \sqrt{z\tau_i^{-1}} \quad (30)$$

The phase margin δ_m is typically selected between 30° and 75° , depending on how close the poles are. For example, a phase margin of $\delta_m = 45^\circ$ gives a critical damping ratio of $\zeta = 0.707$, whereas $\delta_m = 53^\circ$ makes the two poles coincide with the controller crossover frequency of $s = \omega_c$ [8]. Having selected the desired phase margin, equation 29 can be rearranged to give z :

$$z = \frac{1 + \sin\delta_m}{1 - \sin\delta_m} \frac{1}{\tau_i} \quad (31)$$

Finally, to satisfy unity loop gain such that $|L_v^*(\omega_m)| = 1$, k can be selected as:

$$k = C_f \omega_m \quad (32)$$

As a comparison, the k value from the symmetrical optimum method is identical to the k_p value obtained with the loop shaping method. This shows that both methods parallel each other, but the integral gain depends upon the constraint specified, whether it be the phase margin or cutoff frequency. Nonetheless, both methods provide a solid and justified foundation for initial values which would be tuned to obtain the optimal response.

5.3.8 Summary for **GFL** and **GFM** operation

Having explored the details of the current controller, voltage controller and power-current reference conversion equations, the overall block diagrams of a **GFL** and **GFM** inverter from subsection 5.2.2 can again be put into context. Note that reference transformations between dq and abc frames as well as PLL and ω_t signals have been omitted from the diagrams for simplicity.

The overall control diagram of a **GFL** inverter has previously been shown in figure 4. Since the aim is to control power exchange for a current-controlled inverter, the real and reactive power references P^* and Q^* are first transformed into current references $i_{L,d}^*$ and $i_{L,q}^*$ with respect to the feedback voltage V_c , using equation 19. This reference is then passed into the current controller detailed in section 5.3.5 to control the plant.

Figure 5 shows a diagram for a **GFM** inverter in a similar manner. The inner loop is identical to that of an inverter in **GFL** operation, whereby the current controller $K(s)$ and plant model $G(s)$ form the inner loop transfer function $l(s)$ shown in equation 21. The outer-loop voltage controller detailed in subsection 5.3.7 then returns the control inputs to the inner-loop current reference tracking described in section 5.3.5. Assuming that the outer loop speed is slower than that of the inner loop, both the current and voltage dynamics of the inverter can be effectively controlled.

6 Implementation

The key objective of this project is to develop a prototype system that allows testing of inverters in various operating modes. Hence, this section begins with a high-level overview of the envisioned final design and how it can be used for testing various inverter configurations. The power exchange requirements

in section 5 are transformed into hardware specifications for the inverter and LCL filter. Implementation details for the auxiliary circuits, including the capacitor voltage V_c measurement and amplification of Inverter Evaluation Module BOOSTXL-3PhGaNInv (EVM) measurements are then discussed.

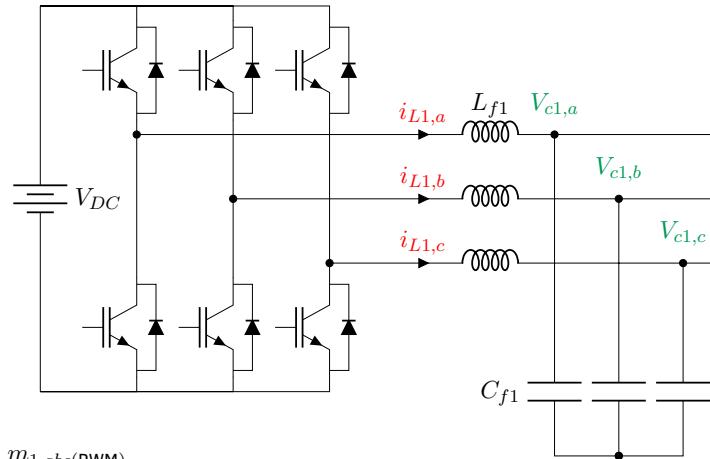
6.1 System Overview

To test the inverters in open-loop, **GFL**, **GFM**, or a combination of these operating modes, a dual inverter design is proposed for the system, as shown in figure 10. Testing of various operation modes can then be achieved by configuring the inverters as shown in table 1.

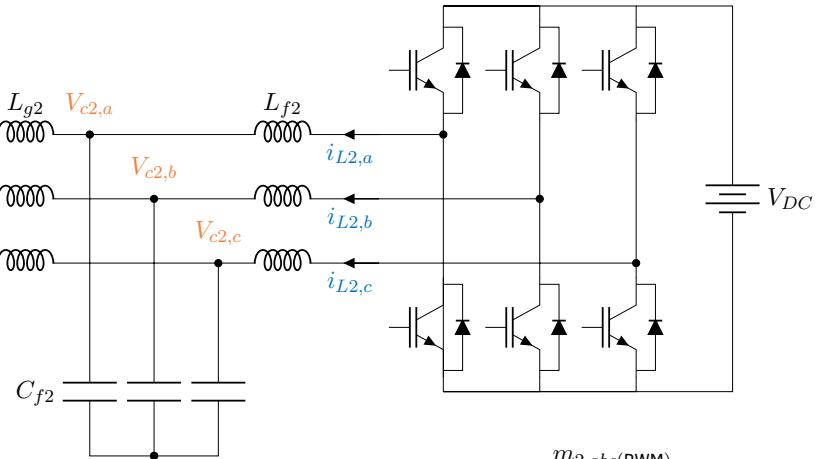
Test	Inverter 1	Inverter 2
GFL	Open-Loop	GFL control using current controller described in figure 8
GFM	GFM control using voltage and current controllers described in figures 9 and 8 respectively.	Off
GFL + GFM	Controller from previous GFM test, with further tuning.	Controller from previous GFL test, with further tuning.

Table 1: Configurations for testing various operation-modes.

Inverter 1 (GFM)



Inverter 2 (GFL)



23

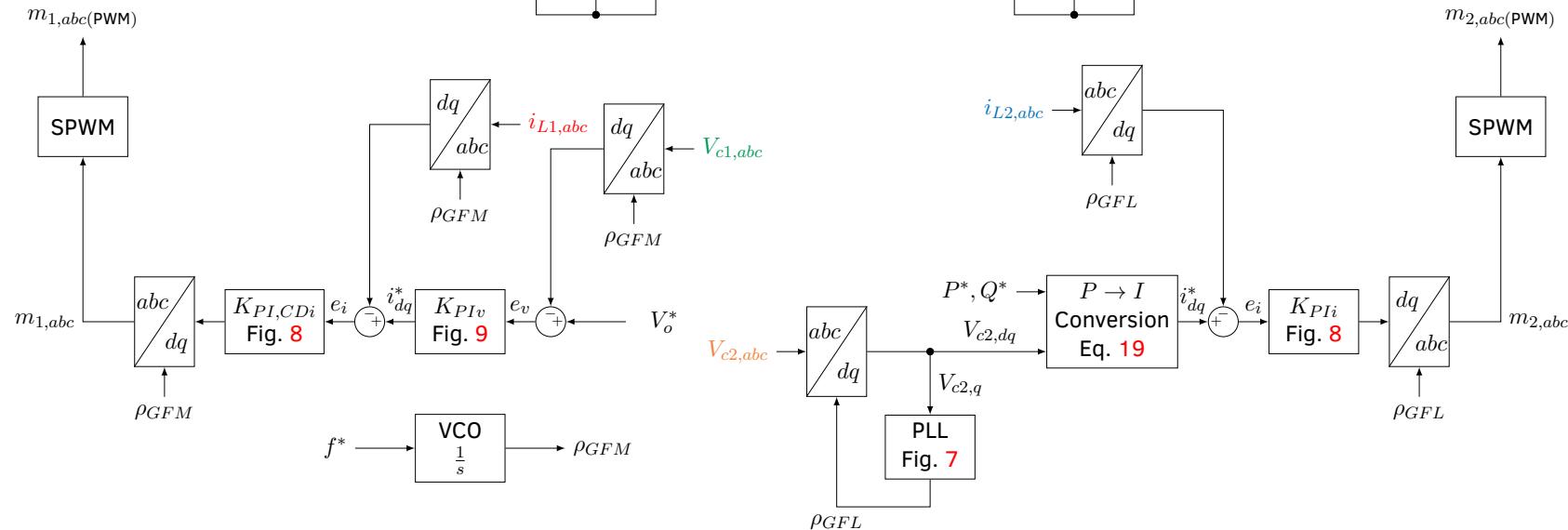


Figure 10: System overview.

6.2 Hardware Specification

The nominal power requirements and justifications are specified in table 2.

Quantity	Value	Justification
DC bus voltage V_{DC}	50 V	Set below 50 V, as an insulated cabinet would be required for operating devices above 50 V in the laboratory.
Nominal AC grid voltage $V_{AC,rms} = V_{rated}$	30 V	Magnitude chosen based on the maximum Root Mean Square (RMS) AC voltage, that is $48/\sqrt{2} \approx 30V$.
Nominal AC grid frequency f_{AC}	50 Hz	Consistent with power supply mains frequency in the United Kingdom.
Nominal AC phase current $I_{AC,rms} = I_{rated}$	1.5 A	To ensure that average and peak 3-phase power draw $P_{3\phi,nom}$ is below that of a 100 W power supply.
Switching frequency f_{sw}	10 kHz	Matches that of a high-power IGBT AC-DC converter, instead of the frequency offered by MOSFETs in low power inverter modules which could typically reach 100 kHz.

Table 2: Nominal requirements for dual-inverter prototype.

Therefore, the nominal phase power P_{rated} and 3-phase power are as follows:

$$P_{rated} = V_{rated} \cdot I_{rated} = 30 \cdot 1.5 = 45W$$

$$P_{3\phi,nom} = \sqrt{3}P_{rated} = \sqrt{3} \cdot 45 = 78W$$

With respect to the nominal power requirements in table 2 (I_{rated} , V_{rated} , f_{AC} , f_{sw}) and guidelines in section 5.1.2, the LCL filter can be designed as follows:

- $L_f = 4mH$ (eqn. 1, ripple magnitude $y = 10\%$ of rated current I_{rated})
- $C_f = 8.8\mu F$ (eqn. 2, reactive power absorption $x = 5\%$)
- $L_g = 350\mu H$ (eqn. 3, $y = 10\%$)

The resonance frequency is verified a posteriori as $\omega_{res} = 848.3Hz$, so with respect to equation 4 the resonance frequency will not interfere with system stability. Finally, following equation 5, the optional damping resistor value is $R_{damp} = 7.8\Omega$.

In addition, a load resistor is used for absorbing real power during open-loop and GFM tests, which is chosen based on the desired load voltage and current:

$$R_{load} = \frac{V_{AC,rms}}{I_{AC,rms}} = \frac{30}{1.5} = 20\Omega$$

These specific components are then selected with respect to their voltage or current ratings. Special attention has been given to the inductors to ensure that they have a high maximum current rating beyond

$I_{AC,rms}$. Otherwise, an insufficient rating would cause the magnetic flux density in the core to saturate, which would lead to a reduction in effective inductance and hence an increase in current ripple Δi_L .

To meet the requirements, the custom-wound toroidal core inductor design is chosen for L_f . Its inherent closed-loop design offers high magnetic flux density, low EMI and high efficiency in a relatively compact size. The biggest compromises are cost and longer lead-times, as these inductors are made-to-order. A smaller core could also have possibly been chosen, though the reduced window area would have further increased winding difficulty and cost.

6.3 Component Selection and Measurement Circuits

With respect to the requirements mentioned, the subsection details the justifications for two important components of the circuit, namely the inverter prototype and load resistor, as well as the measurement circuitry for V_c and i_L .

6.3.1 Inverter Selection

After consulting the datasheet [52], the Texas Instruments EVM inverter was chosen for this project based on the following criteria:

1. DC Bus Voltage: As the board can operate with a DC bus voltage below 50V, it is a suitable candidate for testing without the need of an insulated cabinet,
2. Measurement signals: The board features fully-differential measurements for phase voltages of all 3 phases, which are scaled to 0 to 3.3V, making it compatible with both the new controller and the build-in controller connections. Phase current measurements are obtained via INA240 differential amplifier chips in series with each phase output. This enables current measurements to be obtained over the full period of the switching cycle, which compares favourably to emitter current measurement on some other boards that only measure currents during on-times.
3. Fault Protection: Measurements for temperature and DC bus voltage are available, which can enable fault protection measures to be implemented. Over-temperature protection is also built-in as a hardware feature, which shuts the board in the event of high temperature, likely driven by over-current.
4. Control: The board takes PWM signals for gate driving of half bridges, which allows custom control models to be developed via the lab's RCP system.
5. Operating frequency: The switching frequency of most high-power IGBT AC-DC converters are under 13.5 kHz. Hence the prototype will be configured to operate at this lower frequency.

6.3.2 Load Resistor Considerations

The load resistor is chosen based on the desired value of $R_{Load} = 20\Omega$, as well as the nominal power rating per phase $P_{rated} = 45W$. To ensure that its temperature is kept in a suitable range, it should also be fitted with a heat-sink, which ensures that electrical power dissipated as heat is readily transferred to its surroundings.

Hence, an ABL132AB1500B heatsink is purchased, which has a thermal resistance $J_{sa} = 0.17^\circ C/W$ [53]. While the thermal resistance of the 20Ω resistor is not available, it is known that the resistor can dissipate 30W at $25^\circ C$ without a heatsink [54]. Assuming the thermal resistance at the resistor-Termal Interface Material (TIM) and TIM-sink junctions are zero, the temperature rise is only due to the sink-ambient junction. When operating at the $P_{rated} = 45W$, the resistor is 15W above the resistor ambient rating of 30W, which leads to a temperature increase of:

$$\Delta T = J_{sa} \times \Delta P = 0.17 \times 15 = 2.55^\circ C$$

The resulting device temperature is below $50^\circ C$, the temperature at which a warning sign is recommended. This selection yields a safe tradeoff between power dissipation and area required.

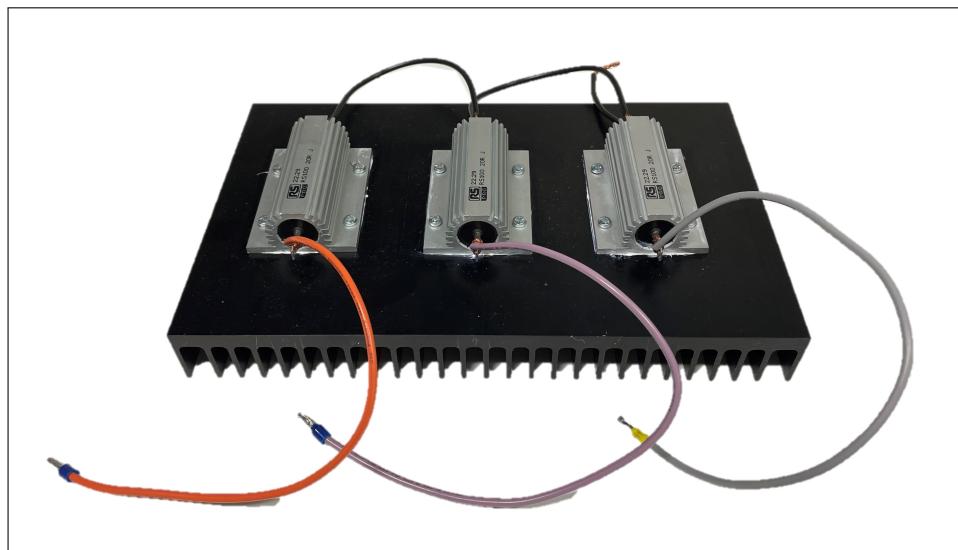


Figure 11: Three load resistors $R_{Load} = 20\Omega$ fitted with ABL132AB1500B heatsink.

Figure 11 shows the wye-connected resistors fitted on the heatsink.

6.3.3 Capacitor Voltage V_c Measurement

The capacitor voltage V_c is selected for feedback as this offers separation between the output voltage V_o at the grid and the system. In addition, as a result of ignoring L_g , this corresponds to the plant model defined in equation 8 which assumes an LC-filter.

Two options for V_c measurement, were considered, including:

1. Resistor string to ground, with a LC low-pass filter; or,
2. Using a hall effect voltage sensor.

For the purposes of research, it was decided that an analogue hall effect voltage sensor would be more suitable, which generates an output signal proportional to the flux density produced by the current flowing through the primary coil. While it occupies significantly more PCB space, the isolated topology enables the output signal to be coupled to the DC ground, which is more robust than taking differential measurements against a floating neutral point. The topology of the hall effect voltage measurement is shown in

figure 12.

A suitable candidate is the Hall-Effect Voltage Transducer LV 25-P readily available at the laboratory. With respect to the guidelines in its datasheet [55], the parameters are chosen as follows:

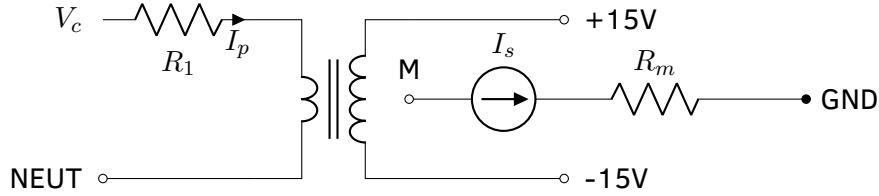


Figure 12: Hall effect voltage sensor topology for capacitor voltage V_c measurement.

- Given a maximum primary voltage of $V_c = 50V$ at a primary coil current of $I_p = 10mA$, the primary resistance is $R_1 = 5k\Omega$. It shall be rated for a power dissipation of 800mW.
- As a result of a turns ratio of $N_s/N_p = 2.5$, the nominal secondary current induced is $I_s = 25mA$. The measuring resistance is at the maximum recommended value of $R_M = 350\Omega$ which returns a range of $\pm 8.75V$, which is below the limitation imposed by the $\pm 15V$ voltage rails. At the maximum secondary voltage, the resistor must be rated for 219mW.

6.3.4 Amplification for Inductor Current i_L and DC Voltage V_{DC} Measurements

The Simplus controller range is $\pm 15V$ or ± 2048 in digital terms. As the output range of the inductor current i_L and DC voltage V_{DC} signals from the EVM is 0 to 3.3V, the digital range when directly connected to Simplus is 0 to +450. As verified with Design 1, this poor resolution is detrimental to the performance as it causes instability and bandwidth restrictions. Hence, to take full advantage of the Simplus ± 2048 range, the current and voltage signals from the EVM shall be amplified to the full $\pm 15V$ range, with a non-inverting differential amplifier referenced to the EVM zero measurement point of 1.65 V, as shown in figure 13b. The equation of this differential amplifier is defined as follows:

$$V_{out} = \frac{R_2}{R_1}(V_{in} - 1.65)$$

Note the generation of the 1.65V reference is achieved with the voltage follower shown in figure 13a, which is physically close to the non-inverting amplifier to maximise common mode noise rejection. This is possible as a result of the 4-channel configuration of the TL074CDR Operational Amplifier, which fits 4 high bandwidth and high slew rate differential amplifiers within a compact footprint.

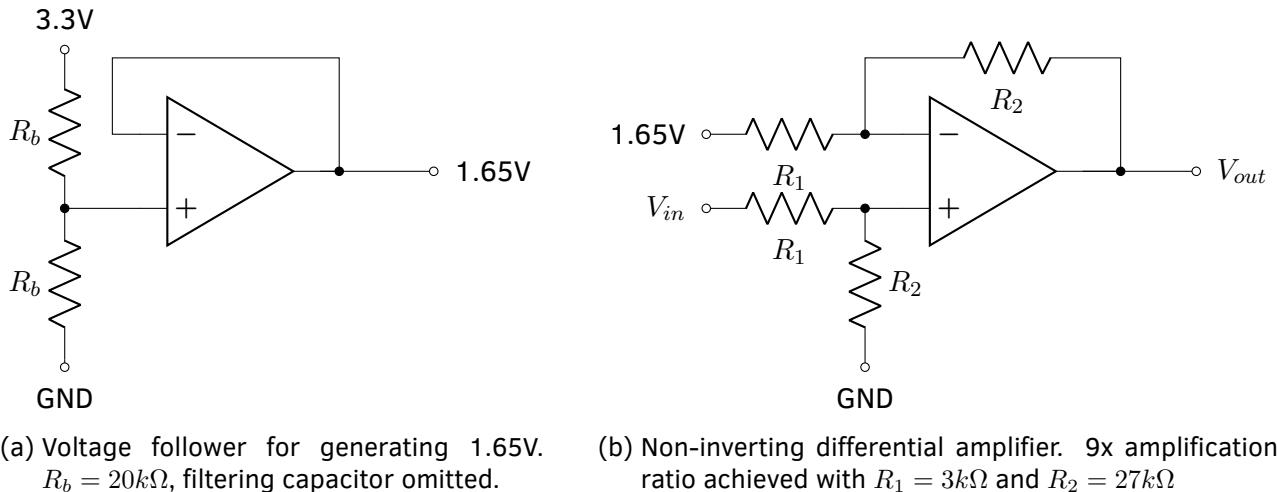


Figure 13: Amplifier circuitry for signals from EVM.

6.4 Circuit Designs

To perform tests on the **EVM** with the **RCP** system in the lab, 2 iterations of intermediate **PCBs** were developed on Altium Designer. The first design consists of an intermediate board between the host and the inverter with no measurements, which is only intended for verifying the effectiveness of the LCL filter using open-loop operation. The second is a hugely elaborate design for the dual inverter system that houses both inverters and their filtering components, as well as feedback measurement circuitry for deploying **RCP**.

This signals to and from each **EVM** are interfaced through two 20-pin connectors, which are well documented on the datasheet from TI[52]; J1 is exclusively used for analogue signals such as phase voltage and current measurements, while J2 is used for digital signals which consists of **PWM** and fault protection signals. The input/output interface to the host is the Simplus controller, which has two 50-pin connectors and can simultaneously monitor up to 16 channels of measurements for a variety of applications. The controller is engineered by the Maurice Hancock Laboratory Team, and is primarily intended as a replacement interface card for the Danfoss FC302 Inverter at the Maurice Hancock Laboratory. An image of the controller is shown in figure 14.

This subsection describes the mappings between the host and the **EVM** of each design, and the modifications made to the second design.

6.4.1 Design 1: Initial tests for the LCL filter

J1 at the **EVM** offers fault protection and enable signals, which can be connected to the digital GPIO pins on Simplus. Similarly, V_t and i_L measurements at J2 can be connected to Simplus' ADC pins. By mapping signals at J1 and J2 of the **EVM** to the Simplus interface, this results in the schematic of this intermediate **PCB** as defined by tables 3 and 4. The 2D layout and 3D isometric view of the PCB are shown in figures 15b and 15a respectively.

For initial tests, the **EVM** is connected to the filter board shown in figure 16, and the limitations observed are as follows. Firstly, V_o cannot be replaced by V_t , which is the unfiltered voltage at the half-bridge terminals; as such, the current design has no measurement circuitry present for V_o . Secondly, in contrast

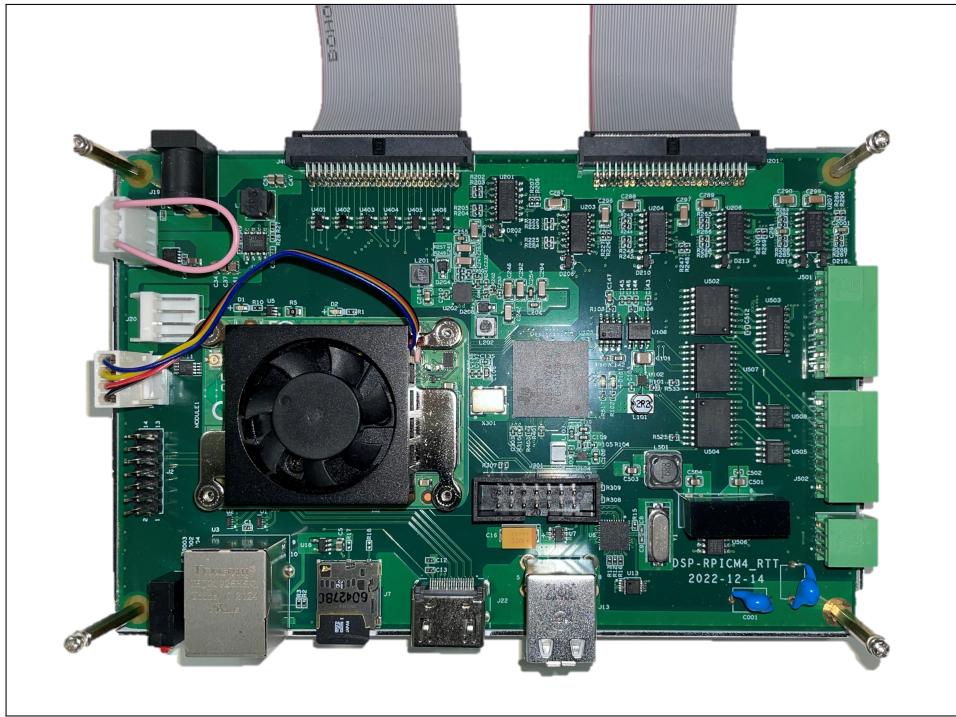


Figure 14: Simplus Controller Board, developed by Maurice Hancock Laboratory members.

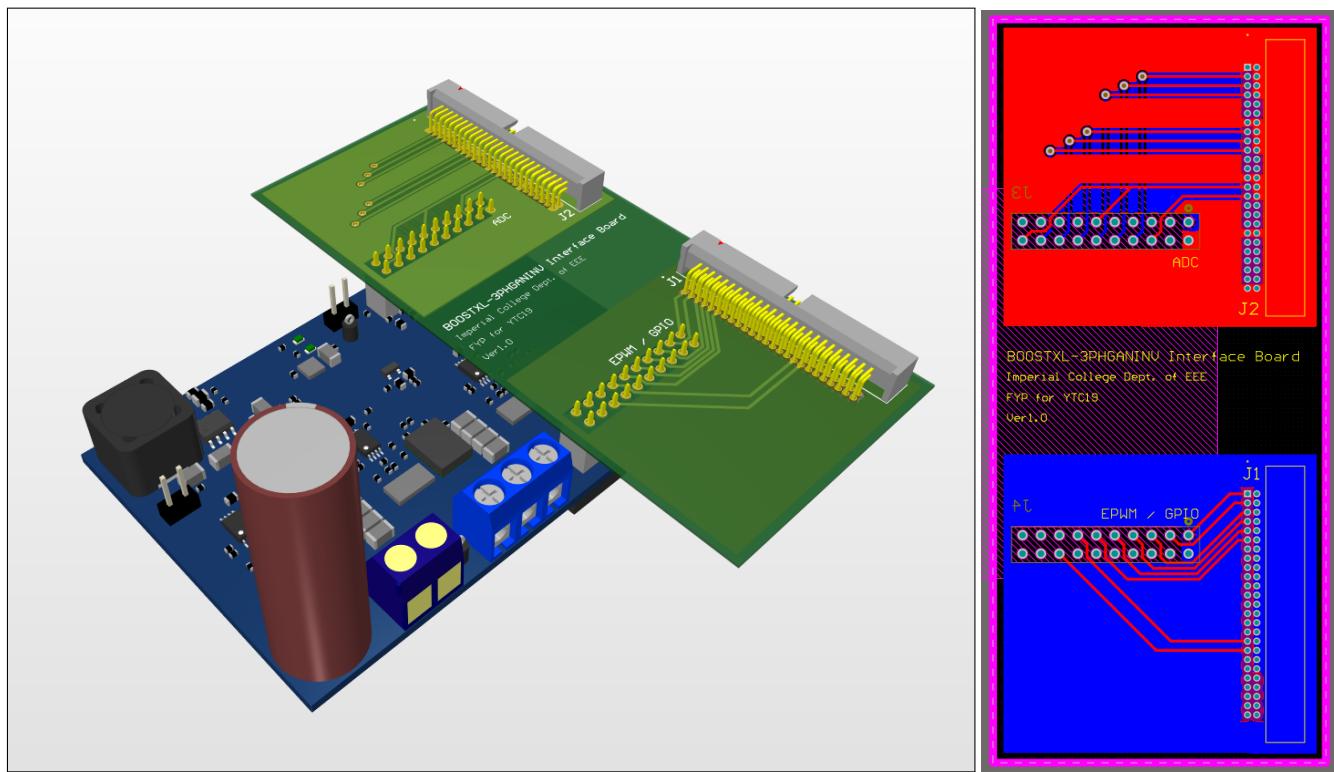
to the Danfoss FC302 double-ended signals ($\pm 15V$), analogue measurements on the EVM are single-ended signals (0 to 3.3V), so all negative signals on the interface end are wired to common analogue ground on the EVM; this results in lower data resolution as the digital output range is restricted to 0-450 rather than ± 2048 .

6.4.2 Design 2: Dual-inverter System

Having tested design 1, several observations were made that contributed towards design 2:

1. The LCL filter is effective for the required power exchange requirements, but the filter capacitance will be reduced to $C_f = 2.2\mu F$ to reduce the reactive power consumption.²
2. The current and voltage signals from the EVM shall be amplified to -15 to 15V to improve output resolution. This is crucial as poor resolution will cause instability and bandwidth problems if the system were to be operated in closed-loop. The implementation of this auxiliary circuit is described in subsection 6.3.4.
3. Similarly, as described in section 6.3.3, hall effect voltage sensors will be used to obtain the capacitor voltage V_c measurement, rather than terminal voltage V_t . This makes the system suitable for closed-loop operation.
4. The damping resistor R_{damp} in series with the filter capacitor C_f can be removed, as there is no appreciable difference between a setup with and without R_{damp} , as evidenced by the response com-

²I would like to acknowledge this as a design mistake made in initial simulations which hindered correct control of reactive power. This increases the resonance frequency to $\omega_{res} = 1.7Hz$, though it does not violate the resonance frequency constraint in equation 4. As this mistake does not affect steady state performance and the hardware has already been soldered, the value was kept at $C_f = 2.2\mu F$ rather than $C_f = 8.8\mu F$.



(a) 3D View

(b) 2D Layout View

Figure 15: Design 1 Intermediate PCB

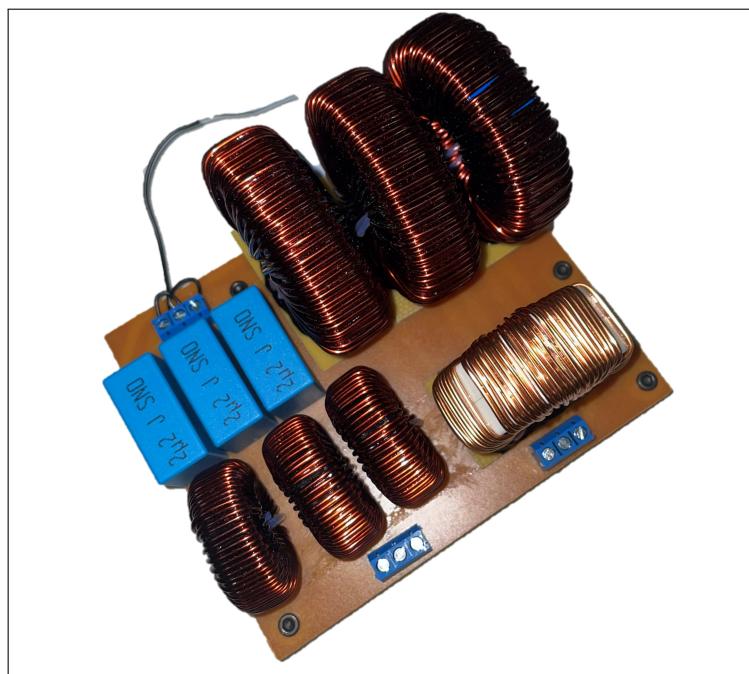


Figure 16: LCL filter with no feedback circuitry

Simplus		EVM	
Signal	Signal	Pin at J1	
A1	VA	8	
A2	VB	10	
A3	VC	12	
B1	IA	14	
B2	IB	16	
B3	IC	18	
C1	VREF	20	
C2	VREF	11	
C3	VDC	6	
A1-	C2-	GND	4

Table 3: ADC signals (0 to 3.3V) at Simplus, connects to EVM J1.

Simplus		EVM	
Signal	Signal	Pin at J2	
EPWM1A	PWM A (high-side)	1	
EPWM1B	PWM A (low-side)	3	
EPWM2A	PWM B (high-side)	5	
EPWM2B	PWM B (low-side)	7	
EPWM3A	PWM C (high-side)	9	
EPWM3B	PWM C (low-side)	11	
dGPIO17	/PCB OT enable	13	
dGPIO18	/PCB OT alert	16	
GND	GND	2	

Table 4: Digital signals at Simplus, connects to EVM J2.

pared as shown in figure 18.³

5. No tests could be done with the common-mode choke at the time of design 1 as there was only one inverter and intermediate board. As such it was not possible to exchange reactive power between 2 inverters, common mode current measurements were not taken.

Furthermore, for the new dual inverter system, the signals had to be re-routed as the Simplus controller will be controlling and monitoring measurements for 2 inverters simultaneously. Omitting pin numbers for simplicity, the Simplus ADC and dGPIO connector mappings are defined in tables 5 and 6 respectively.

As shown in figures 17 and 32, or the 2D and 3D views of the PCB respectively, the bottom two-thirds of the board is dedicated to housing the LCL filters, whereas the top portion is for the hall effect voltage sensors, auxiliary amplification circuits for the EVM signals, as well as the EVM and Simplus connections. Alternatively, an image of the completed board is also shown in figure 1.

³Although there is no visible difference, as acknowledged in the conclusion, there was a lack of foresight in removing the terminal for R_{damp} , which would have made it possible to test damping required under different conditions.

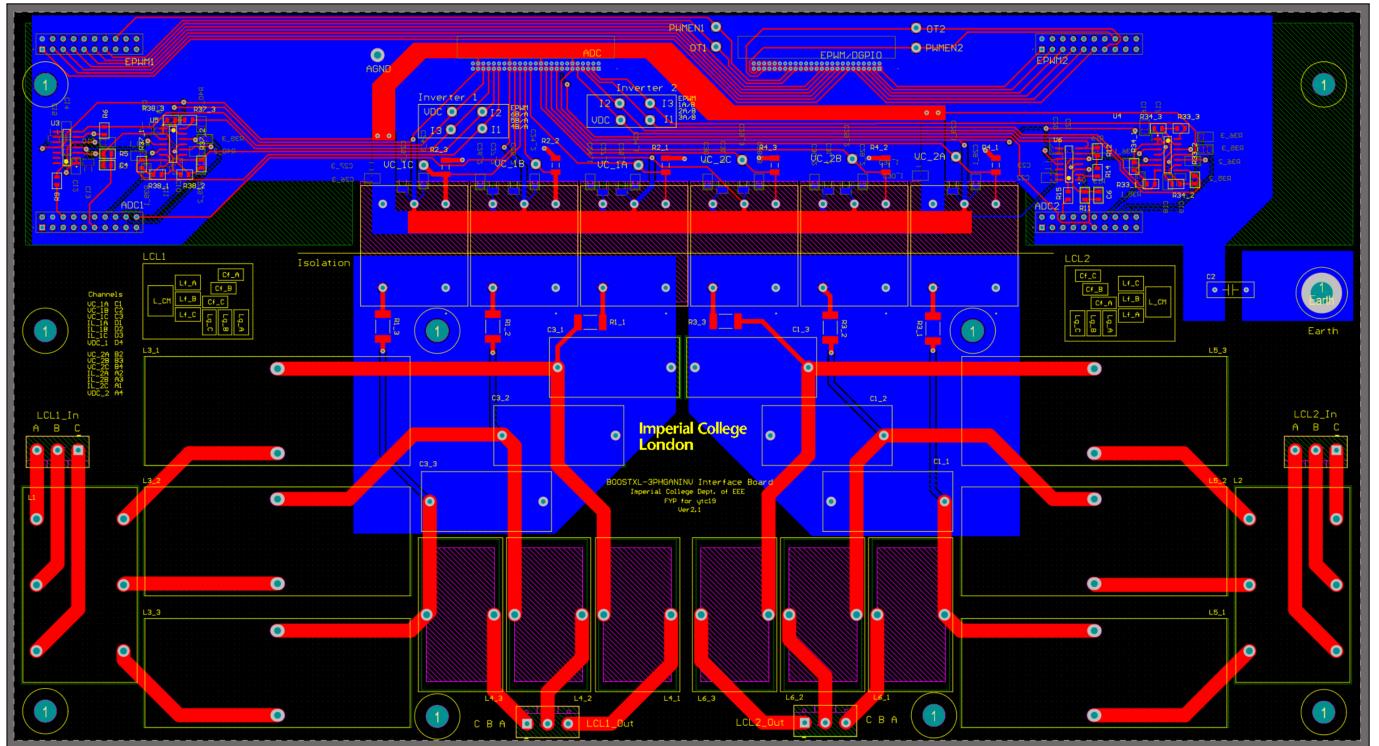


Figure 17: Design 2 PCB 2D layout view.

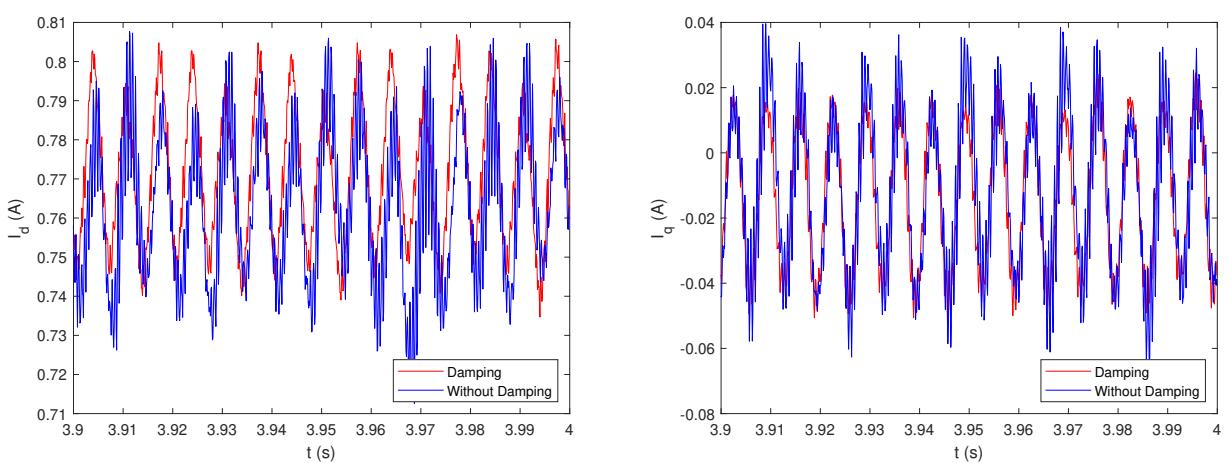


Figure 18: i_d and i_q oscillations, with or without R_{damp} .

Simplus	Inverter		
Signal	Trace Name	Signal	EVM
A1	IL_2C	IC	2
A2	IL_2A	IA	2
A3	IL_2B	IB	2
A4	VDC_2	VDC	2
B1	VREF_2	VREF	2
B2	VC_2A	VA	2
B3	VC_2B	VB	2
B4	VC_2C	VC	2
C1	VC_1A	VA	1
C2	VC_1B	VB	1
C3	VC_1C	VC	1
C4	VREF_1	VREF	1
D1	IL_1A	IA	1
D2	IL_1B	IB	1
D3	IL_1C	IC	1
D4	VDC_1	VDC	1

Table 5: Simplus ADC Signals

Simplus	Inverter		
Signal	Trace Name	Signal	EVM
EPWM1A	EPWM1A	PWM A (high-side)	2
EPWM1B	EPWM1B	PWM A (low-side)	2
EPWM2A	EPWM2A	PWM B (high-side)	2
EPWM2B	EPWM2B	PWM B (low-side)	2
EPWM3A	EPWM3A	PWM C (high-side)	2
EPWM3B	EPWM3B	PWM C (low-side)	2
EPWM4A	EPWM4A	PWM A (high-side)	1
EPWM4B	EPWM4B	PWM A (low-side)	1
EPWM5A	EPWM5A	PWM B (high-side)	1
EPWM5B	EPWM5B	PWM B (low-side)	1
EPWM6A	EPWM6A	PWM C (high-side)	1
EPWM6B	EPWM6B	PWM C (low-side)	1
dGPIO17	PCB_OT_1	/PCB OT enable	1
dGPIO18	PWM_EN_1	/PCB OT alert	1
dGPIO23	PCB_OT_2	/PCB OT enable	2
dGPIO24	PWM_EN_2	/PCB OT alert	2

Table 6: Simplus Digital Signals

7 Results for RCP deployment on simulations and hardware

The following section embodies the essential aim of this project - to deploy simulated setups on hardware. For each configuration, a model is first developed on Simulink with respect to the control schemes outlined in section 5 (diagrams attached in the Appendix 9.1), and tested on simulation and hardware using the gains initially calculated. A comparison justifies the validity of the model before further step responses are studied. An extensive study is then performed for each configuration on hardware, to tune the most suitable current, voltage and PLL gains for optimal performance, based on results from reference power, voltage, frequency or other perturbations. A user guide for running the setup is included in appendix 9.1.

7.1 Controller Parameter Initialisation

Following the loop shaping method described in section 5.3.5, the controller parameters are initialised assuming bandwidths determined by the crossover frequencies $f_{ci} = 500Hz$, $f_{cv} = 200Hz$ and $f_{cpll} = 0.5Hz$. These bandwidths are chosen with respect to the following considerations:

1. The closed loop bandwidth of both the voltage and current controllers must be higher than the grid and filter resonance frequencies to achieve zero steady-state error in the rotating reference frame.
2. The inner current loop bandwidth must be higher for rapid response to perturbations, and there must be sufficient separation between the outer voltage and inner current loop for good stability and disturbance rejection.
3. As a PLL is crucial for system stability, a low bandwidth and over-damped response is selected.

The resulting gains are shown in table 7, alongside tuned values obtained during hardware experiments. Note the large adjustment in the voltage controller gains, which are optimised during testing as later outlined in subsection 7.4. This is done in an attempt to increase the voltage controller speed.

Controller	Gains	Calculated	Tuned
Current	k_p	1.22	1.22
	k_i	957.49	957
Voltage	k_{pv}	0.0028	0.028
	k_{iv}	0.8685	8.685
PLL	$k_{p,pll}$	3.05	3.05
	$k_{i,pll}$	2.39	2.39

Table 7: Controller Parameters.

The top-level Simulink implementation of the power inverter for all simulations is shown in figure 29, and the implementation of the PLL for GFL configuration is shown in figure 19 (both in appendix 9.1).

7.2 Inverter in open-loop

7.2.1 Simulation of open-loop inverter with a passive load

While implementing closed-loop control is the ultimate goal of this project, testing the model with a 3-phase passive load in open-loop allows the circuit plant model to be verified, and confirms the effective-

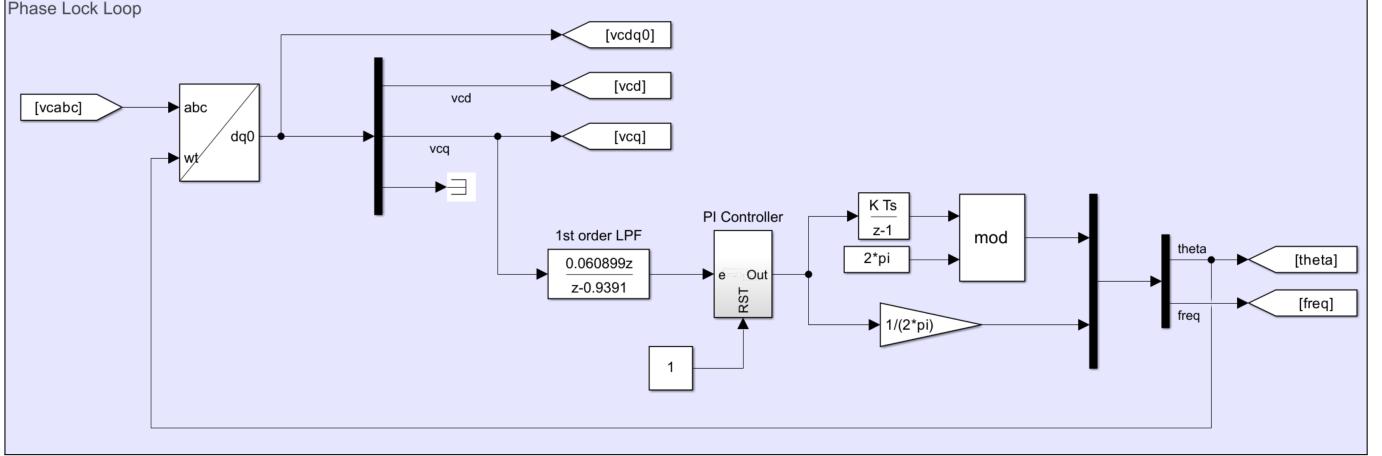


Figure 19: Simulink implementation of **PLL** circuitry, used for all open-loop and closed-loop **GFL** simulations and hardware implementations. Note the first-order **LPF** discretised with a zero-order hold, which consists of a pole at $p = e^{2\pi f_{\text{cutoff}} T_s}$

ness of the LCL filter in allowing the plant to produce AC waveforms with minimal oscillations. Open-loop generation is achieved by setting the duty cycle to a 50 Hz sine wave of amplitude 0.3.

Before proceeding towards results, the following list outlines the initial rule-of-thumb checks performed in all future tests to ease debugging in any configuration:

1. Always calibrate with zero currents and voltages,
2. Check power and current definitions, which should be in generator convention,
3. Observe order of phases in *abc*-frame, which should be in positive sequence convention; and,
4. Check controller values, especially initial states, output saturation, and integrator saturation which may be limited by default.

As shown in figure 21, all of the *abc* waveforms are sinusoidal as anticipated, with v_o and i_o being the filtered versions of v_c and i_L respectively, as a result of additional filtering from the grid-side inductance L_g . The 50 Hz component is visually discernible as the dominant frequency component, which is a desirable characteristic.

The *abc*-frame the oscillatory nature of voltages and currents conceal aspects of system stability, which must be analysed in *dq*. Note that the **PLL** of this open-loop setup only exists to generate *dq* waveforms for diagnosis rather than to control the system in closed-loop, so the tracking of *dq* results are unimportant. However, the stability of the **PLL** and *dq* plots remains an integral aspect to be observed, as it is a prerequisite for **GFL** operation.

As shown in figure 22, the *dq* quantities are steady and the v_d and i_d are equal to the amplitude of $v_{o,abc}$ and $i_{L,abc}$, which indicates that *dq SRF* is correctly driven by the **PLL** by the frequency of the **AC** grid. The high frequency harmonic oscillations present in these results are approximately 300 Hz and 10 kHz, which are anticipated imperfections associated with third harmonic injection and switching. The low frequency settling oscillation is reflected in the open-loop frequency response in figure 20, which shows a time delay at low frequencies, and the slow response attributed to the low bandwidth of the system. This stable performance is also evidenced by the relatively large phase margin at crossover frequency.

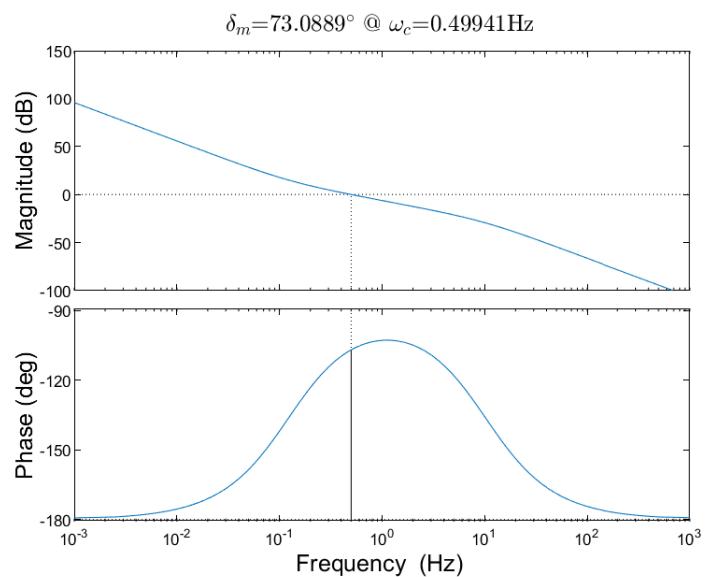


Figure 20: Open-loop frequency response of PLL.

Simulink simulation results of a 3-phase inverter with open-loop control.

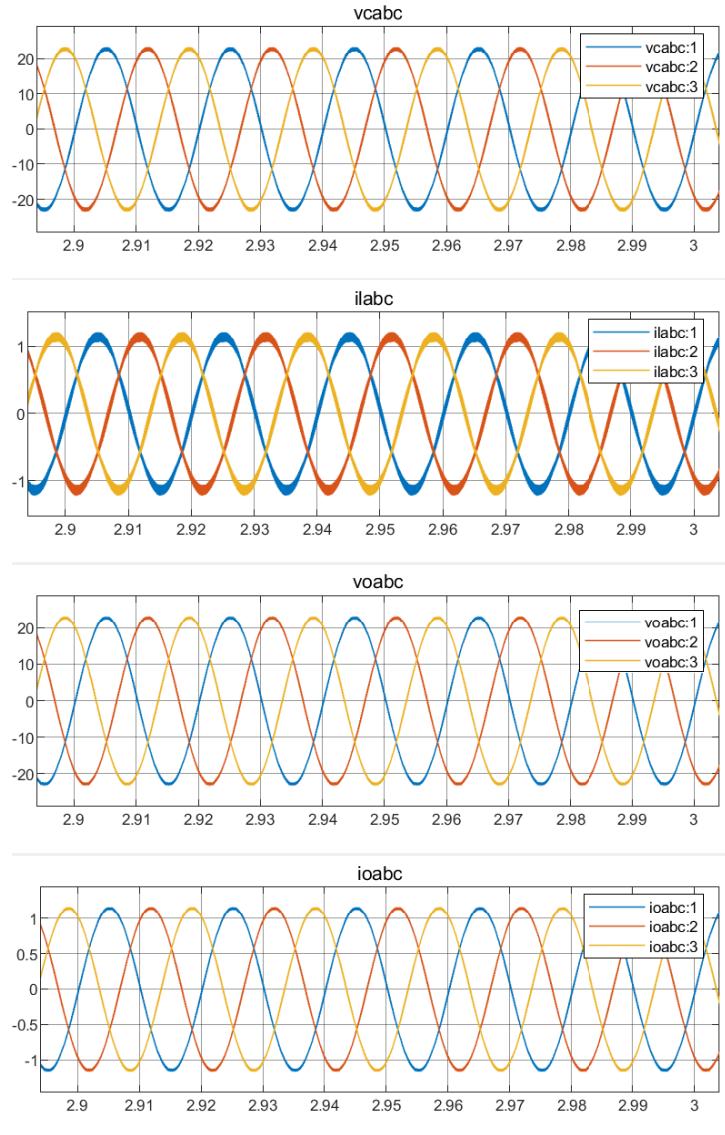


Figure 21: A detail look at sinusoidal waveforms: voltage V_c across the filter capacitor C_f , current flow i_L through the first LCL inductor L_f , output voltage V_o , and output current i_o .

37

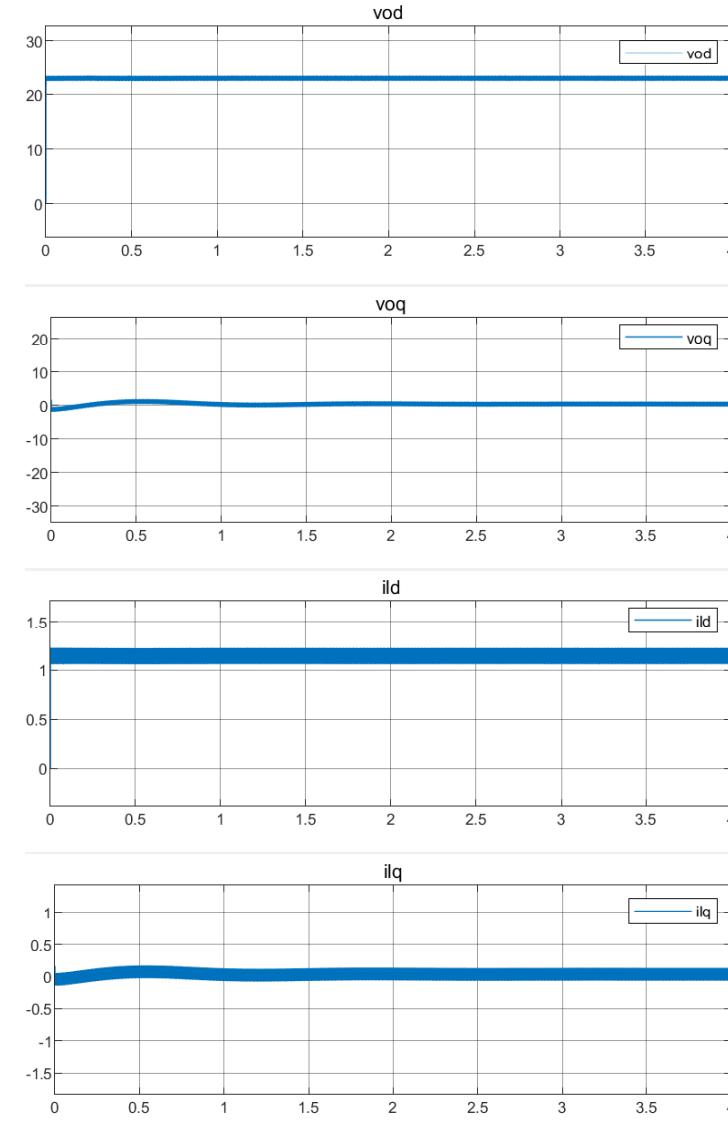


Figure 22: Voltage V_c across filter capacitor C_f and current flow i_L through the first LCL inductor L_f in both d and q axes.

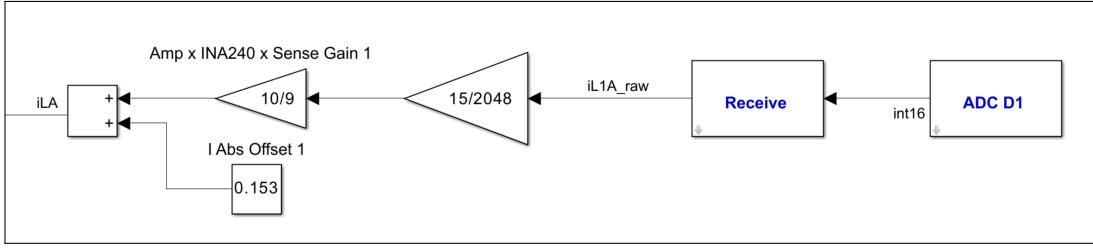


Figure 23: Calibration of i_{LA} .

7.2.2 Hardware test for open-loop inverter with passive load

The principal aim of the hardware open-loop test is to ensure the robust performance of the hardware in preparation for feedback operation. This enabled a comprehensive check on the functionality of circuit components, and a calibration of voltage and current measurements.

Prior to calibration, the errors detected and rectified were as follows:

1. Phases were incorrectly labelling, which was noticeable upon connecting the 2 inverters operating in zero phase offset. The label maker was used to correct labels on the 3 terminals.
2. The digital current polarity was reversed, due to the load convention current output measurement on the **EVM**. This was fixed on the model.
3. Incorrect bias voltage was identified for several outputs, as a result of incorrect resistors installed for the 1.65V voltage follower. Replacing the resistors resolved the issues.
4. Non-intuitive value of V_{DC} : A mistake was made to bias all measurements from the **EVM** at 1.65V, which results in negative digital values for $V_{DC} \subseteq [0, 40]$. This was fixed with a software tweak.
5. The **CMC** was immediately identified a useless addition to the **PCB**, as the common mode current ripple exceeded 0.15A when no phase offset was applied. Consequently, a decision was made to short the **CMCs** altogether.
6. Check the inverses of the $abc - dq$ and $dq - abc$ transforms: In literature, there are 2 options for scaling the transforms depending on whether an amplitude or **RMS** value is desired in the dq frame.

The absolute errors of the measurements dominate. Several possible reasons for these errors are the errors in bias created by the voltage followers, poor layout optimisation on the dual-inverter prototype **PCB**, and non-idealities on the Simplus Controller Board. Hence, to calibrate measurements, a constant compensation offset is added after the conversion from digital to the $\pm 15V$ range and multiplication with the theoretical gains. An example is shown in figure 23. These values are noted in table 8, and as observed the largest absolute error is 1.13V in actual terms. Precise calibration is crucial, as the mismatch between the zero-points of phases will lead to 50 Hz oscillations in the dq frame.

Channel	Inverter	Voltage/ Current Injection (V or A)	± 2048 Digi- tal Value	High Thresh- old	Triggered	Trigger Value (V or A)	
VDC	D4	L	40	-296.82	-296	Yes	39.95
VDC	A4	R	Not tested - faulty soldering				
V1A	C1	L	10	238.93	240	Yes	10.81
V1B	C2	L	10	238.93	240	Yes	11.13
V1C	C3	L	10	238.93	240	Yes	10.68
V2A	B2	R	10	238.93	240	Yes	11.07
V2B	B3	R	10	238.93	240	Yes	11.26
V2C	B4	R	10	238.93	240	Yes	11.02
IL1A	D1	L	1	122.88	123	Yes	1.19
IL1B	D2	L	1	122.88	123	Yes	1.14
IL1C	D3	L	1	122.88	123	Yes	1.18
IL2A	A2	R	1	122.88	123	Yes	1.31
IL2B	A3	R	1	122.88	123	Yes	1.21
IL2C	A1	R	1	122.88	123	Yes	1.42

Table 9: ADC trigger values.

Signal	Inv_Left (1)	Inv_Right (2)
IL_A (A)	0.1153	0.254
IL_B (A)	0.116	0.188
IL_C (A)	0.162	0.338
VC_A (V)	0.84	0.753
VC_B (V)	0.927	1.13
VC_C (V)	0.58	0.795

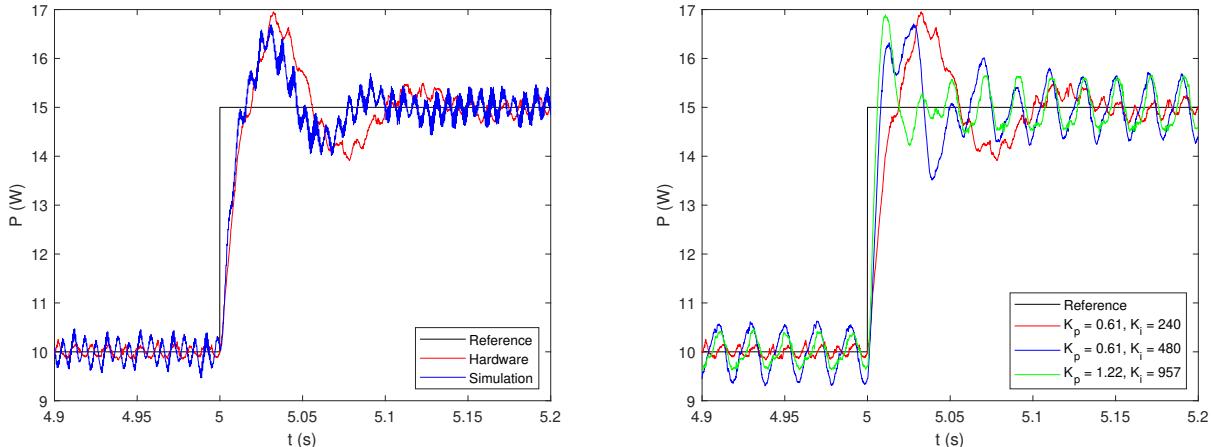
Table 8: Calibration Parameters.

The **Analogue-Digital Converter (ADC)** protection blocks for each channel are then tested, by setting the high threshold for the test channel to a low and safe value, while keeping other channels at a relatively higher threshold. The voltage or current is then increased, either by increasing the **DC** bus voltage or the phase offset between the inverters. Finally, the corresponding trigger value is compared against the desired threshold. As shown in table 9, all channels are triggered successfully at the limit, with the exception of VDC_2 which was excluded from the test due to faulty circuitry. The fault was not fixed because of time constraints, but it is not critical as the **DC** bus is connected for all tests, such that the **DC** measurement from VDC_1 serves the same purpose.

7.3 **GFL** inverter in closed-loop configuration

7.3.1 Simulations of **GFL** inverter with stiff grid

For a **GFL** inverter, the goal is to control the real and reactive power exchange between the inverter and the grid, as discussed in section 5.2.2. With respect to the controller topology and design principles outlined in section 5.3, an implementation of this current control scheme on Simulink is shown in figure 30a in appendix 9.1.



(a) Comparison between simulation and inverter hardware deployment, at $K_p = 0.61$ and $K_i = 240$. (b) Inverter hardware deployment with different controller gains.

Figure 24: Real Power P perturbation step responses.

To examine the validity of the model, a step change in real power reference from 10W to 15W at $t = 1$ s is performed both in simulation and on Simplus hardware, with other control variables constant during the time of simulation. This test is performed as the purpose of a current-controlled **GFL** inverter is to track power exchange.

In simulation, the circuit is completed by connecting the setup shown in figure 29 to an ideal-voltage source. For Simplus deployment, the model sets inverter 1 to open-loop operation with an adjustable sine generator at the duty-cycle input and **GFL** control on inverter 2, as detailed in the overview in subsection 6.1.

Since the converter controls power exchange via current control as described in subsection 5.3.4, the key variables of interest for this configuration are the reference and actual trajectories of i_d , i_q , and P , which are shown in figure 24a.

As observed in both the simulated and hardware experiments, the feedback currents effectively track the reference, and reach the required steady-state value within a satisfactory time period. However, there are oscillations at various frequencies, which can be briefly explained as follows:

1. 10 kHz: small ripples from the switching of the half bridges,
2. 1 kHz: a result of resonance in the LCL-filter,
3. 300 Hz: associated with third harmonic injection; and,
4. Lower frequencies associated with the response of the controller. The main difference between the simulated and hardware result is the low frequency oscillations, which is a result of the under-estimated **Equivalent Series Resistance (ESR)** in both inductors, which has reduced the damping of the performance

In conclusion, this experiment verifies the equivalence between simulation and hardware results. Having proven that this nominal controller is steady-state stable, the **GFL** inverter's performance can be improved by comparing the deployment of various controller gains on hardware.

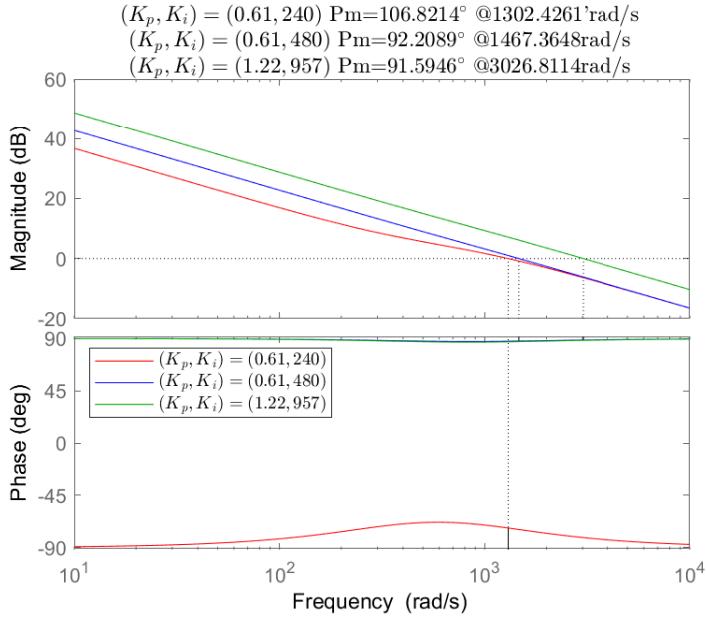


Figure 25: Bode plot for loop transfer function of current control loop $L = GK$ (eqn. 21) with different controller gains.

7.3.2 Hardware test of **GFL** inverter with open-loop voltage generator

As a continuation of the previous subsection 7.3.1, the hardware experiment is repeated for 6 sets of controller gains, namely in the ranges $k_p \subseteq [0.31, 2.44]$ and $k_i \subseteq [240, 957]$. For illustration purposes, only 3 sets of results (corresponding to 3 set of gains) are rendered in the plots on figure 24b, which shows that $(k_p, k_i) = (0.61, 240)$ yields the best balance between settling time and oscillation magnitude.

However, the comparison also reveals several implications that will be useful for tuning the current controller when it will later be operating in the inner loop of a dual-loop **GFM** controller:

1. Increasing k_p largely corrects the static error and increases the rise magnitude of the first oscillation after the perturbation, which accelerates the response. However, it reduces the time to accumulate error, which result in increased magnitude of oscillations.
2. Increasing k_i enables the steady-state to be reached quicker. However, this decreases the phase margin, leading to increased oscillations and reduced steady-state stability.

This is evidenced by the bode plot in figure 25.

However, while a current controller at $(k_p, k_i) = (0.61, 240)$ gives the best response in terms of achieving the balance aforementioned, when a **GFM** inverter is connected to a **GFL** inverter, a faster but less stable response such as that offered by $(k_p, k_i) = (1.22, 957)$ will be required for the **GFL** inverter. This is because a faster response is required for the **GFL** inverter's current controller, as it needs to regulate the output current within the limits. Therefore, while $(k_p, k_i) = (1.22, 957)$ makes a suitable candidate for a **GFL** current-controller due to its fast response, Hence, these current controller gains shall be further refined when both inverters on the board are operating in closed-loop.

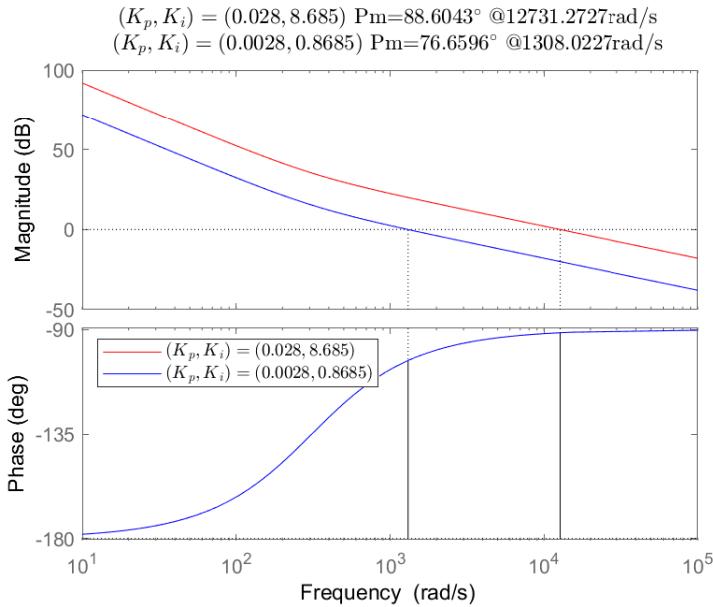


Figure 26: Bode plot for loop function $L_v(s)$ of voltage control loop with different controller gains. Note that the current loop is omitted, and that the current gain is assumed unity in the operating bandwidth of the voltage controller loop, that is $T_i = 1/(\tau_i s + 1) = 1$.

7.4 GFM inverter in closed-loop

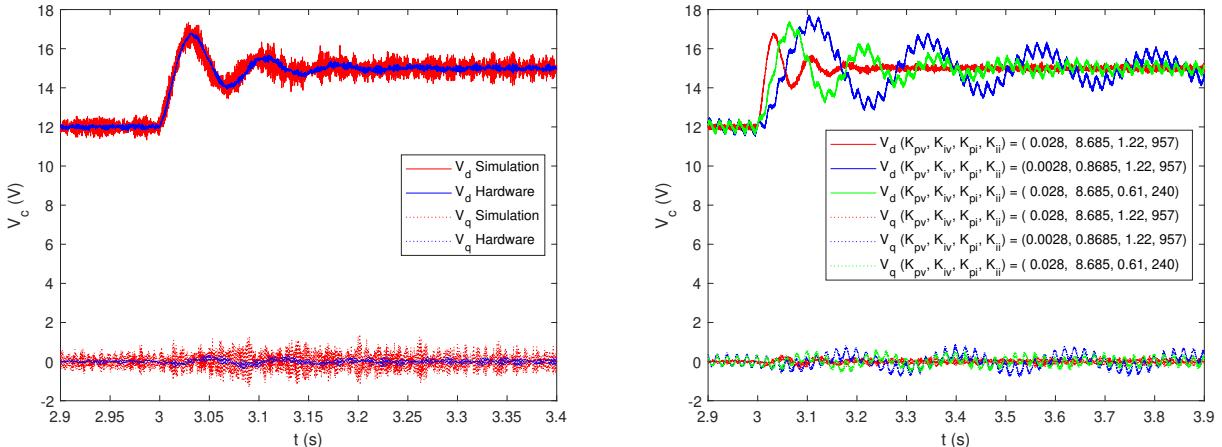
7.4.1 Simulations of GFM in closed-loop with passive load

Following the controller topology and design principles outlined in section 5.3, a block model for GFM control is constructed on Simulink as shown in figure 30b (attached in appendix 9.1).

Similar to subsection 7.3.1, a step response test is performed on the GFM inverter to verify the equivalence between the simulation and hardware deployment. The real voltage V_d step response serves as an appropriate indicator of its performance, as the goal of the GFM inverter is to control the desired voltage and frequency of the grid is utilised as a reference for the system. The results are shown in figure 27a, which reveals several conclusions:

1. Contrary to the GFL results in subsection 7.3.1, the simulation results in figure 27a shows more oscillations in the simulation compared to the hardware deployment. A close examination reveals that the noise frequency is beyond 10 kHz, suggesting that this noise is caused by the $1\mu s$ simulation time step discretisation, which is smaller than the sampling frequency of $100\mu s$.
2. The slow voltage controller has caused a delay between V^* and duty cycle, and consequently the grid voltage which is used for controller feedback. This leads to a non-minimum phase as characterised by the frequency response as shown in figure 26, and explains the low frequency oscillations.
3. Reducing the integral gain and controller output limit while maintaining the integrator saturation limit could reduce the magnitude of the oscillations. A first order low-pass filter can also be implemented on the PLL. However, the hardware also has additional parasitics which would increase the effective integral gain.
4. The rise time could be reduced by increasing the proportional gain.

Ultimately, adjusting the gains of the outer-loop voltage controller is a balancing act, as increasing these



(a) Comparison between simulation and inverter hardware deployment.
(b) Inverter hardware deployment with different controller gains.

Figure 27: Real voltage V_d perturbation step responses

gains will increase the effective bandwidth and contradict the requirement of the inner and outer loop bandwidth separation for adequate disturbance rejection[56]. Having verified the equivalence between the **GFM** simulation and hardware models, the bandwidth can now be tuned more precisely by testing various gains on the **EVM**.

7.4.2 Hardware test of **GFM** inverter connected to passive load

Having validated the simulation and hardware model of a **GFM** inverter, the V_d^* perturbation tests is performed using 7 different sets of gains on hardware, in the ranges $k_{pi} \subseteq [0.31, 2.44]$, $k_{ii} \subseteq [240, 957]$, $k_{pv} \subseteq [0.0028, 0.028]$ and $k_{iv} \subseteq [0.8685, 8.685]$. The results for 3 sets of gains are displayed in figure 27b, where several observations can be made.

1. The smallest set of gains, $(K_{pv}, K_{iv}, K_{pi}, K_{ii}) = (0.0028, 0.8685, 1.22, 957)$, initialised with the loop shaping methodology, results in the largest overshoot and settling time. It can also take up to 1 s to achieve the required steady state value, which is a time-scale beyond that of the **PLL**.
2. The highest set of k_p and k_i , $(K_{pv}, K_{iv}, K_{pi}, K_{ii}) = (0.028, 8.685, 1.22, 957)$, results in the smallest overshoot and settling time. At this operating point, there is sufficient bandwidth separation between the inner and outer loops, which ensures disturbance rejection and reduces steady state oscillations.

Consequently, it can be concluded that $(K_{pv}, K_{iv}, K_{pi}, K_{ii}) = (0.0028, 0.8685, 1.22, 957)$ offers the best performance in terms of oscillations and response speed.

7.5 Both inverters in closed-loop

Following the tuning process described in subsections 7.3 and 7.4, the control parameters for this dual closed-loop test are initialised using the tuned values obtained from those experiments, and further modified as shown in table 10. The justification for the modifications are as follows:

1. Reducing the integral gains K_{ii} of the current controllers increases the inner control loop phase margin and stability. This compensates for the decreased bandwidth separation between the inner current loop and outer voltage loop, as K_{pv} was increased to accelerate the voltage step response.
2. Increasing the integral gain K_{iv} of the **GFM** voltage controller significantly reduces the voltage steady state error.
3. The bandwidth of the **PLL**(*) has been increased to $f_{PLL} = 1Hz$, with the **LPF** cut-off frequency increased to $f_{cutoff} = 100Hz$. Both of these changes accelerate the response of the **PLL**.

Controller	Gains	From	sections	Tuned
		7.3, 7.4		
GFM Current	k_p	0.61		0.61
	k_i	240		15
GFM Voltage	k_{pv}	0.028		0.028
	k_{iv}	8.685		8.685
GFL Current	k_p	1.22		1.22
	k_i	957		60
GFL PLL(*)	$k_{p,pll}$	6.09		6.09
	$k_{i,pll}$	9.57		9.57

Table 10: Controller Parameters.

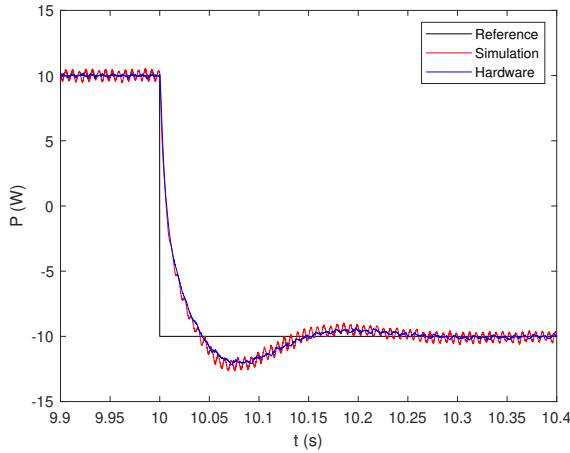
Further tuning for inverters in a network of resources and loads is a justified and commonly adopted practice. Albeit the existence of generator with large synchronous rotating masses, power network grids are never fully stiff. This is especially true with the increased penetration of **IBRs** which further reduces the stiffness. Therefore, the dynamics at the output of an inverter system is reliant on grid or load impedance, which varies depending on the location of the **PCC**.

The step responses due to **GFL** real power P , **GFM VCO** frequency f_{ref} and **GFM** real voltage V_d perturbations are then obtained both in simulation and hardware. These perturbation tests are a combination of tests performed in the previous subsections, and reflect the performance of both inverters in closed-loop. The notable addition is the the **VCO** frequency perturbation test, which reflects the stability of the **PLL** in perturbing grid conditions.

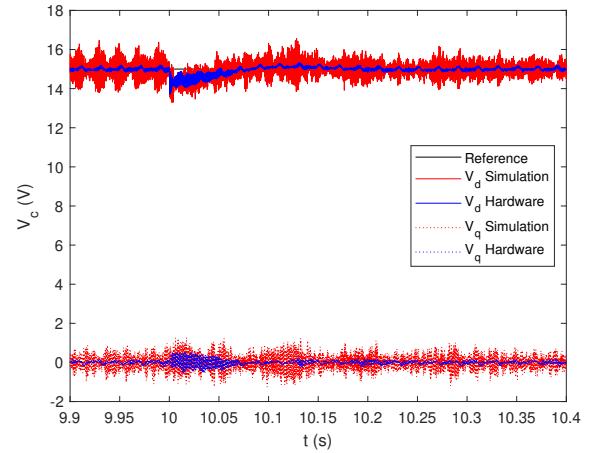
The results, as shown in figure 28, proves that the system is resilient to perturbations in grid voltage and frequency, and that the **GFL** inverter can reliably behave as a power importer or exporter.

8 Conclusion

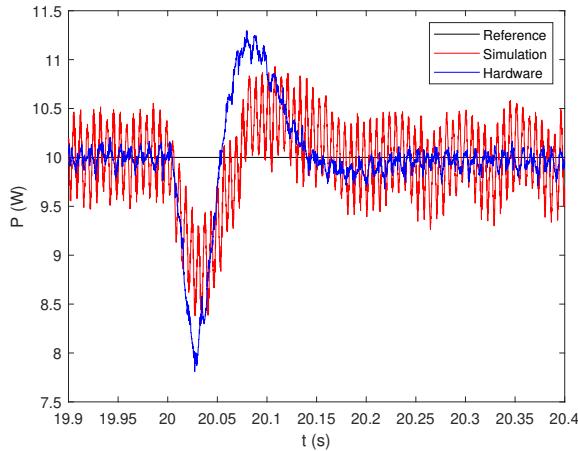
This project proposes a dual-inverter **RCP** system concept, which is a versatile test-bench capable of testing systems in numerous configurations. It is tested on simulation, implemented on hardware, and verified with numerous tests. The key feature of this **RCP** system is the correspondence between simulation and hardware results, which affirms the role of the dual-inverter **RCP** system in validating simulation designs. This is reflected in the step response results across all 3 configurations, **GFL**, **GFM** and both in closed loop, as shown in figures 24a, 27a and 28 respectively.



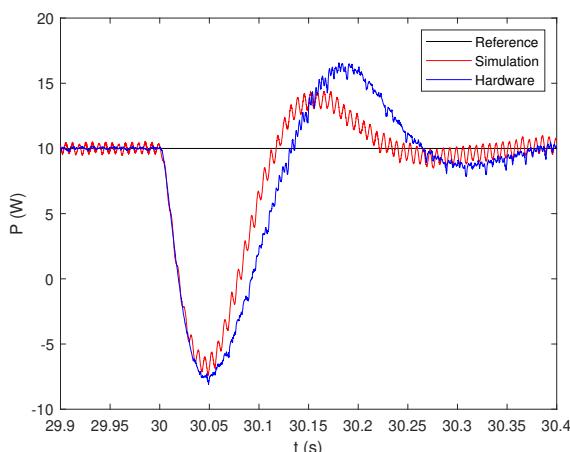
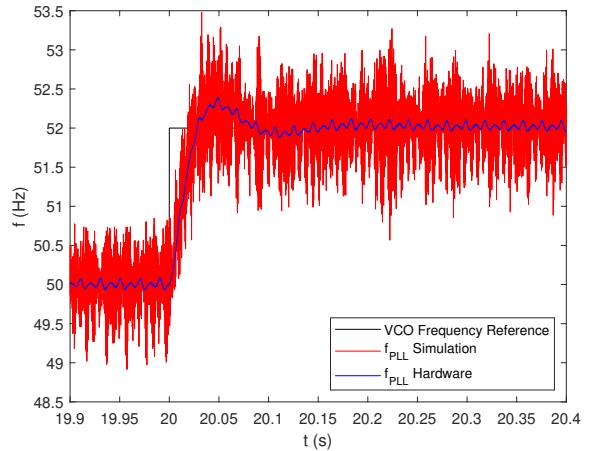
(a) P response due to P perturbation.



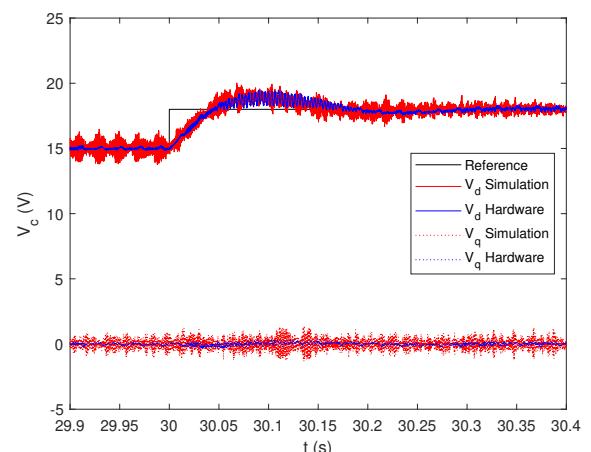
(b) V_d response due to P perturbation.



(c) P response due to VCO frequency perturbation. (d) f_{PLL} response due to VCO frequency perturbation.



(e) P response due to V_d perturbation.



(f) V_d response due to V_d perturbation.

Figure 28: Simulation vs Hardware step responses for both inverters in closed-loop, 1 and 2 operating in GFM and GFL respectively.

An awareness of hardware discretisation and simulation model simplifications is important when using an RCP for testing, as they explain the following two differences between simulation and experiments. Firstly, in simulation there is noise exceeding the sampling frequency of 10 kHz, which is especially apparent on figure 27a and 28d. This is due to the fact that the present simulation setup uses a time step of $1\mu s$, and the noise could have been resolved had a smaller simulation time-step been used. Secondly, there are modest differences in the settling time or low frequency oscillations in the current control. This is to be expected as the parasitic resistance of the converter and grid side inductors are not captured in the simulation model, as these are difficult quantities to measure. Knowledge of the parasitics would have otherwise damped the simulation response.

With these limitations in mind, a relatively over-damped simulation can be safely deployed on hardware, with the guarantee that the hardware setup will be stable and substantially equivalent. Further tuning can then be performed on hardware to optimise response.

8.1 Evaluation

In contrast to studies that are performed purely on simulation, such as the solar-photovoltaic system modeled in [57], experiments performed on the dual-inverter system accurately reflect real hardware behaviour due to constraints such as sampling, discretisation and complex dynamics which would have otherwise been unattainable via a simulation. Nevertheless, the system in [57] also demands a boost converter and control of variables such as solar irradiance, which would have required numerous additions to this dual-inverter system. Compared to experiments performed on extensive laboratory setups, such as the inverter system with Semikron SKM50GB063D IGBT switches in [13], the dual-inverter system is a compact, low-power solution that enables the proposed control schemes to be deployed safely and quickly. Hence, it is a suitable candidate for engineering education and research purposes. However, the experiment in [13] operates at a significantly higher power level, which would have been unattainable with the dual-inverter system.

Considering these strengths and weaknesses, the dual-inverter system represents an attempt to serve as an intermediate prototyping tool between simulations and high-power laboratory setups.

8.2 Works Performed

The following work conducted throughout the project has contributed towards the final achieved results:

1. Numerous preliminary simulations comparing performance results across various filter topologies and damping solutions,
2. Initial tests on the EVM with the Texas Instruments C2000 controller when Simplus was under production,
3. The development of Design 1 PCB which interfaced the EVM to a filter with no feedback,
4. Manufacturing two filter PCBs with the lab's Banham PCB miller, for initial tests with different filter capacitor and inductor values,
5. The design and debugging of the dual-inverter PCB, which consists of 162 components and 540 solder pads. This was achieved within tight time constraints and used electronic components that

can be obtained relatively effortlessly,

6. Identification of bugs on Simplus, such as incorrect pin allocations, **PWM** phase offsets and data read-in limitations; and,
7. Tuning **RTTs** of voltage, current and **PLL** controllers gains for optimal performance, such that **GFL** and **GFM** operation modes are able to control power exchange and grid voltage with stable performance.

8.3 Further Works

While this deviates from the nominal operating requirements stipulated for the project, a notable limitation of the dual-inverter system is its inability to track a low or zero current reference in **GFL** mode. The ripples indicate a low signal-to-noise ratio at low current which is caused by insufficient gain bandwidth of amplification or low resolution, a result of amplifying the current signal through the INA240 differential amplifier on the **EVM** and the TL074CDR operational amplifier on the system board. Furthermore, as detailed in subsection 7.2.2, the hardware debugging of the system revealed numerous design flaws.

As the dual-inverter system has proven a versatile platform for testing systems, the following non-exhaustive list of proposed modifications and experiments provides a direction for facilitating future research of high-power inverters at the Maurice Hancock Energy Laboratory:

1. To enable low current tracking, an op-amp with higher gain-bandwidth product (GBWP) can be used, such that the current signal can remain sinusoidal and free from noise at low current levels. To take further advantage of the full $\pm 15V$ range of the Simplus controller, the in-line resistor for the INA240 can be further increased, at the cost of a slightly reduced efficiency. Low-current tracking is important for **IBR** research, as sources like solar photovoltaic systems often operate at low-current.
2. The inability to track low currents is also likely a result of unstable modes which only manifest at low currents when the impact of parasitics are exemplified. As proposed in [58], the current and voltage **PI Controller** can be modelled as circuit elements in series with L_f and C_f respectively. Given the impedance of the **GFM** inverter and admittance of the **GFL** inverter with controllers, the Nyquist Stability Criterion as described in [59] can then be used for small signal stability analysis.
3. In terms of board layout optimisation, the amplification of the **DC** measurement shall also be referenced to ground, such that the signal is positive for all positive **DC** voltages.
4. The inclusion of a neutral connection terminal at the C_f capacitors would enable damping resistors to be connected. While this was omitted at the early stages of the project as the feature was seen unnecessary, this omission lacked foresight and has hindered numerous potential tests. Damping circuits would relax requirements for bandwidth conflicts between the control system and filter resonance as discussed in [13].
5. For high power applications, multiple inverters can be deployed in parallel to relax the **DC** link voltage requirement, or in series to reduce the risk of shoot-through [60]. These topologies can be further explored by connecting multiple dual-inverter systems together.
6. Testing for **DC** voltage perturbation would further reinforce the role of this system for sustainability studies, as **IBRs** are often driven from renewable sources that vary drastically depending on weather conditions.

9 Appendices

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9.1 User Guide: Accessing Simulink Model Files and Design Scripts

The following 2 links can be used to access my project files:

1. [OneDrive](#): Datasets
2. [GitHub](#): Altium design files, Simplus and Simulation Model Files (.slx) for all three configurations ([GFM](#), [GFL](#), dual), scripts for generating plots

To start, download the 3-Phase-Inverter-RCP-FYP repository from GitHub.

Optionally, to plot various step responses of datasets previously obtained, download the folders SimData and SimplusData from OneDrive and place them in the Results folder. The instructions are for visualising these results are in subsection [9.1.3](#). The files concat_legend.m, plotcurrentwithstyle.m, plotwithstyle.m and trim_results.m are functions used within the plotting scripts, and shall not be deleted.

9.1.1 Simulations

The [GFL](#), [GFM](#) and dual-inverter simulations can be accessible within the Simulations folder. In each file, an inverter and filter is setup as shown in figure [29](#). The nominal values are shown in subsection [6.2](#), but the topology can be easily modified. For example, damping resistors can be added.

The following controllers can be modified double clicking the down arrow ↓ on the corner of mask blocks:

- Current controller gains ([GFL](#), [GFM](#), dual),
- Voltage controller gains ([GFM](#), dual); and,
- [PLL](#) f_{cutoff} and gains ([GFL](#), dual).

An example of modifying the gains are shown in figures [30a](#) and [30b](#).

Finally, before running the simulations, modify the step inputs, for example as shown in figure [30c](#). Modify the stop time accordingly and log the scope output to the workspace for future comparisons.

9.1.2 Running Simplus Models

At the time of project completion, the Simplus controller and software toolbox for Simulink can be obtained from Yue Zhu yue.zhu18@imperial.ac.uk or Yunjie Gu yunjie.gu@imperial.ac.uk.

The Simplus models for all 3 configurations for this project are available in the Simplus folder. For [GFL](#) and [GFM](#), the controllers can be modified in dialogue boxes similar to those shown in figure [30](#). For the dual setup with both inverters in closed loop, a higher level interface is offered as shown in figure [31](#).

To run a manual setup with easy modification of [RTTs](#) during run-time:

1. Set stop time to inf,
2. Set scope trigger time in Simplus > Control Panel > Signal & Triggering is set to the 1 second or 10000 samples; and,
3. Disable data logging to workspace.

To run an automated setup:

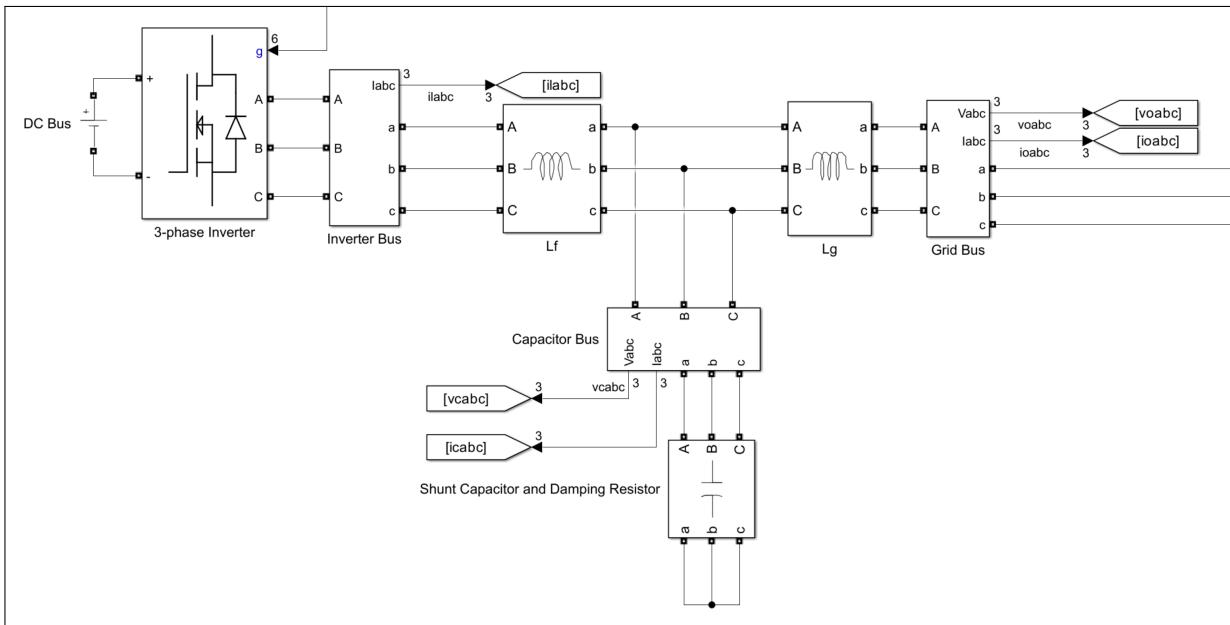


Figure 29: Simulink model of inverter filter and output connections. Used for simulations only

1. Set up the step inputs in advance:
2. Set stop time to a desired length,
3. Set scope trigger time in Simplus > Control Panel > Signal & Triggering is set to the stop time; and,
4. Ensure scope results are logged to the workspace for future comparisons.

To run the model, head to the Simplus tab to click 'Build for Monitoring', 'Connect' and finally 'Run'. During run-time, inverter 1 can be switched OFF and ON, and between **GFM** and open-loop; inverter 2 can be switched between OFF and **GFL** ON.

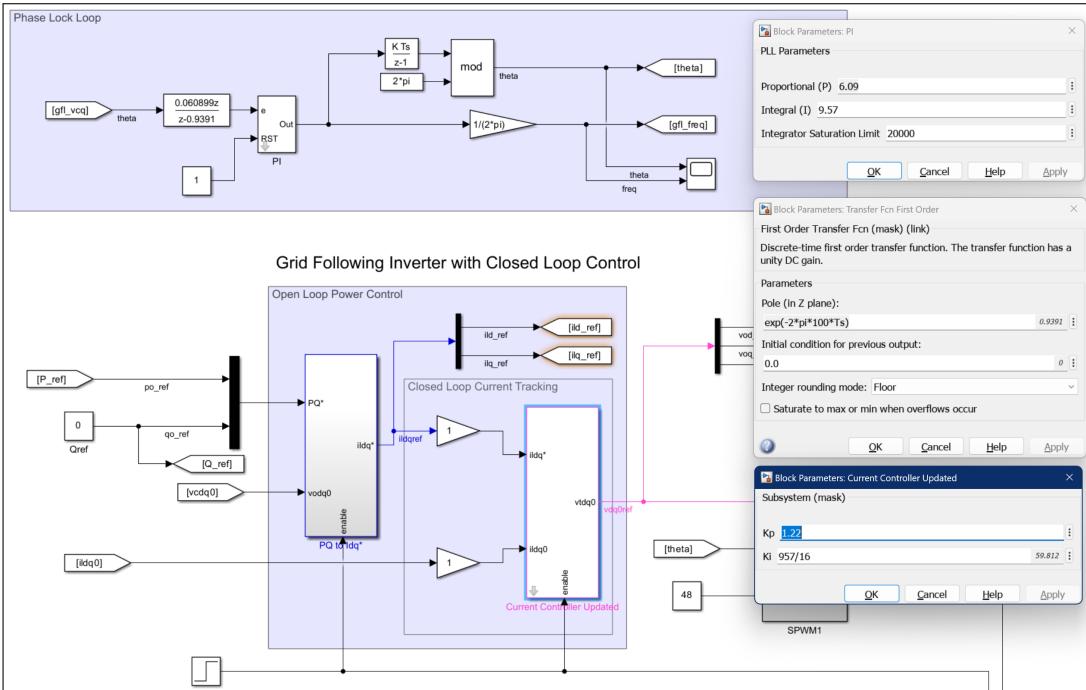
9.1.3 Results

Assuming the step responses between various tests of the same configuration are aligned, the results can be compared using the scripts in the Results folder.

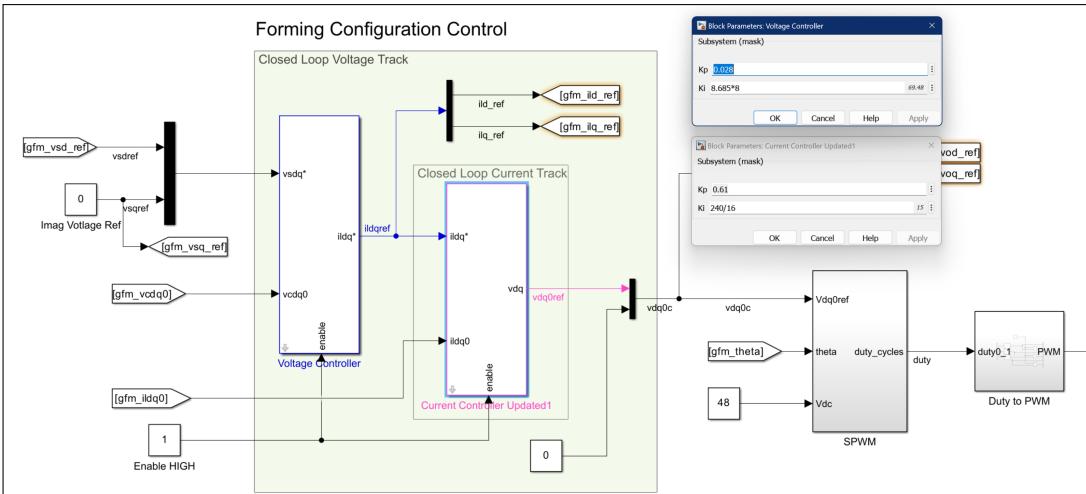
`Dual_Plot_Many_Results.m` is meant for comparing the power, frequency or real voltage perturbations one at a time. To do so, change the `perturb` variable in the first section. More tests can be added, where each string array variable (e.g. `sim_new`), consists of the file name and legend.

The `GFM_Plot_Many_Results.m` and `GFL_Plot_Many_Results.m` scripts are more full-featured, and are designed to compare up to 5 sets of tests simultaneously as follows:

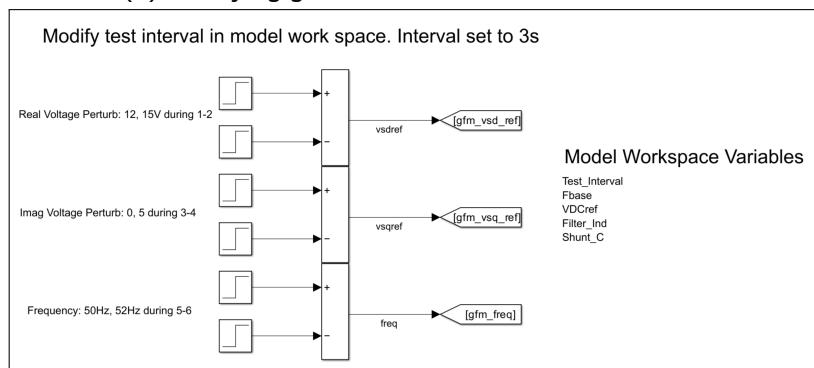
1. In the first section of the script, EDIT: File names and legend names, add a string array variable (e.g. `sim_new`), that consists of the file name and legend. The legend typically shows the gains used for the test.
2. Change the selected variable to include the tests to be compared. It is a `nx1` column array.



(a) Modifying gains for GFI inverter in simulation



(b) Modifying gains of GFM inverter in simulation.



(c) Modify simulation step inputs.

Figure 30: Quick guide to simulation models.

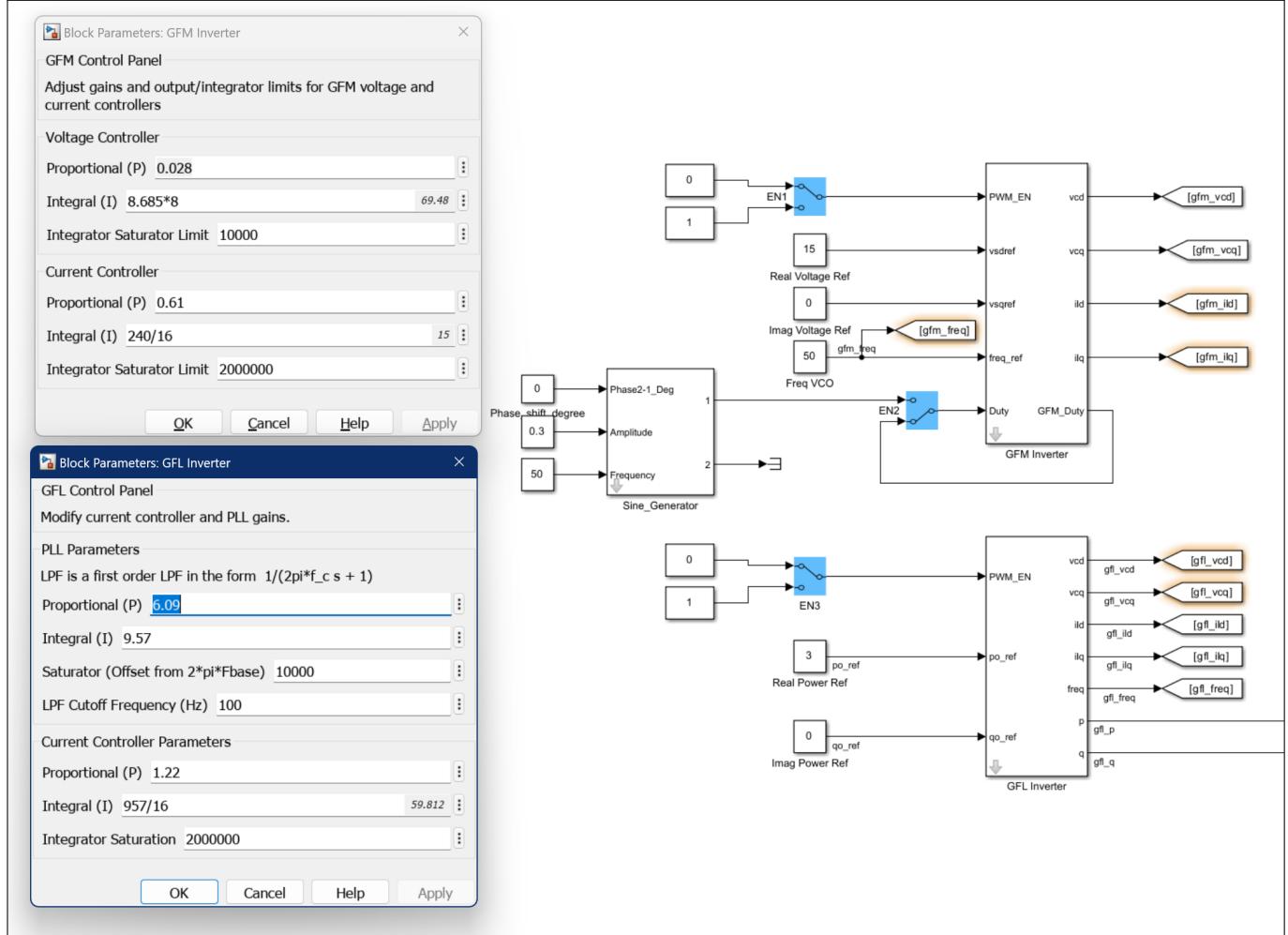


Figure 31: Modify RTTs for the dual-inverter prototype system.

3. Change the perturbation times in the second section. This restricts the x-axis of the plots to the time span specified.
4. If a simulation dataset is used, include its variable name in the first if statement of the file. For example, it should be

```
if (selected(i,:) == sim_single) | (selected(i,:) == sim_new)
```

Uncomment unnecessary plots and run the script to generate the plots.

9.2 Dual-Inverter System (Design 2) Files

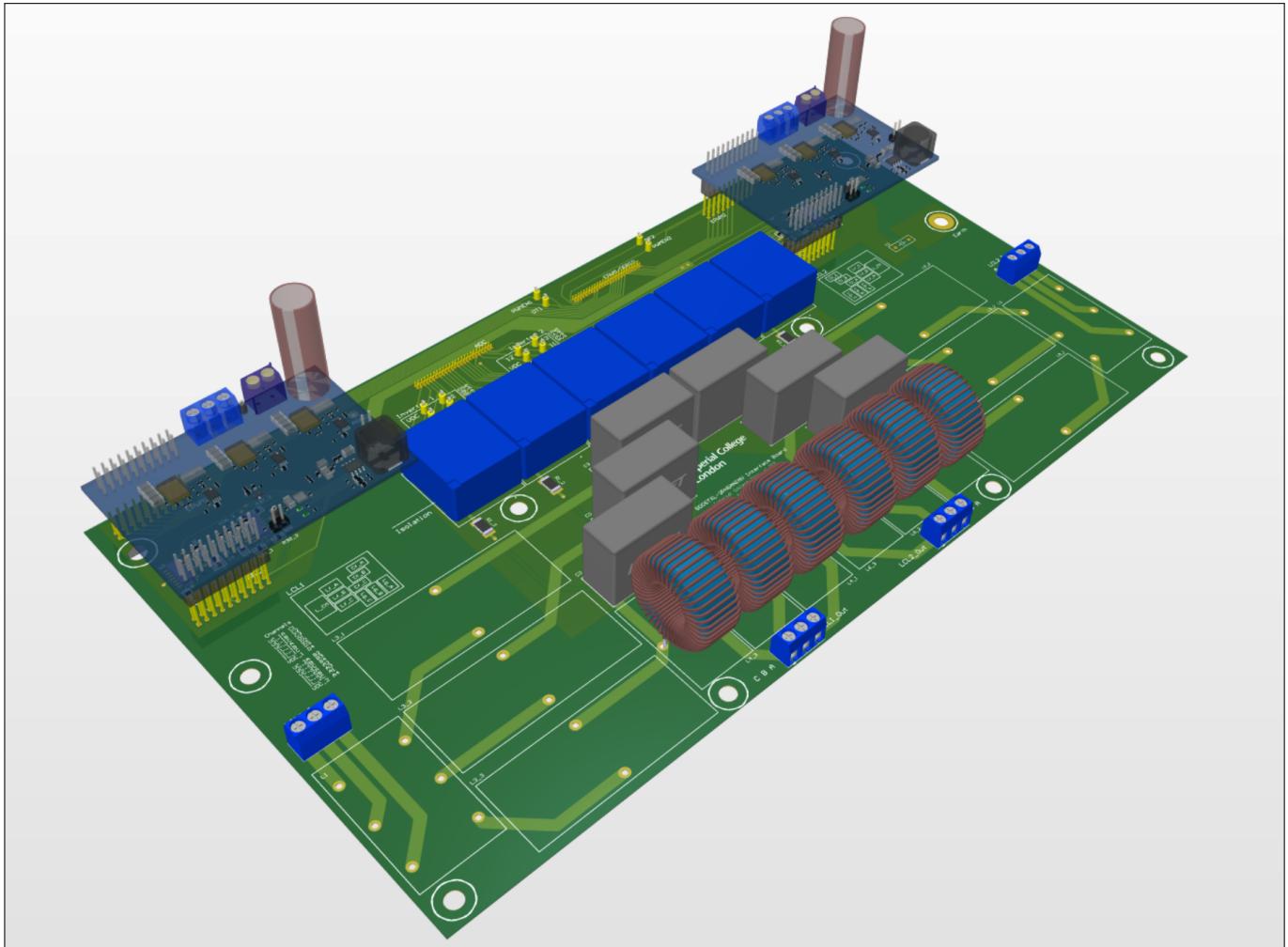


Figure 32: Design 2 PCB 3D render.

For the convenience of the assessor, the bill of materials, schematic and assembly drawings of the dual-inverter system PCB are enclosed in the following pages. The files for the other PCBs are attached in the GitHub repository.

Note the following:

1. The feedback resistors of the non-inverting amplifiers has been updated from $(R1, R2) = (10k, 200k)$ to $(R1, R2) = (3k, 27k)$ following a new design gain and slew rate considerations. However, these changes do not impact the footprints on the **PCB**.
 2. Rooms have been used to compartmentalise repetitive features such as feedback and bias resistors for amplifiers, and 3-phase LCL filters. By denoting components types with numbers and rooms by subscript numbers (isolated by an `_` underscore), this enables components to be easily identified during soldering.

Comment	Description	Designator	Footprint	LibRef	Quantity	Received	Notes
2.2uF_180V	KEMET PHE450 Metallised Polypropylene Film Capacitor, 180 V ac, 250 V dc, ±5%, 2.2µF, Through Hole	C1_1, C1_2, C1_3, C3_1, C3_2, C3_3	Film Capacitor PHE450H	PHE450HF7220JR06L2	6	TRUE	
Earth Capacitor	Y Earth Capacitor	C2	RAD-0.3	102_Y	1	TRUE	CS45-B2GA101K-VKA Ceramic Suppression Capacitor, 100 pF, ± 10%, X1 / Y2, 440 V, 300 V, Radial Leaded, £0.15
2.2uF_0805	SMD Multilayer Ceramic Capacitor, 2.2 µF, 50 V, 0805 [2012 Metric], ± 10%, X5R, C	C4, C5, C6, C7	0805 Capacitor	C2012X5R1H225K125	4	TRUE	Suggest changing to 1nF for better high freq performance
100nF_0805	SMD Multilayer Ceramic Capacitor, 0.1 µF, 50 V, 0805 [2012 Metric], ± 5%, X7R, C Series KEMET	C8, C10, C12, C14, C16, C18, C20, C22, C24_1, C24_2, C24_3, C26_1, C26_2, C26_3, C28_1, C28_2, C28_3	0805 Capacitor	C0805C104J5RACTU	20	TRUE	
4.7uF_1206	SMD Multilayer Ceramic Capacitor, 4.7 µF, 50 V, 1206 [3216 Metric], ± 10%, X7R, C	C9, C11, C13, C15, C17, C19, C21, C23, C25_1, C25_2, C25_3, C27_1, C27_2, C27_3, C29_1, C29_2, C29_3	1206 Capacitor	C3216X7R1H475K160	20	TRUE	
ADC	50-Pin Simplus Connector	J1	SHF-125-01-L-D-RA	SHF-125-01-L-D-RA	1	TRUE	
EPWM	50-Pin Simplus Connector	J2	SHF-125-01-L-D-RA	SHF-125-01-L-D-RA	1	TRUE	
ADC1	SSQ - Samtec 2.54mm Square Tail Dual Row Socket Strip 8.5mm Profile - Fast Stock	J3	SSQ-110-03-T-D	SSQ-110-03-T-D	1	TRUE	
EPWM1	SSQ - Samtec 2.54mm Square Tail Dual Row Socket Strip 8.5mm Profile - Fast Stock	J4	SSQ-110-03-T-D	SSQ-110-03-T-D	1	TRUE	
M5 Mounting Hole		J5, J10, J13, J14, J15, J16, J17, J19, J20	M5 Mounting Hole	M5 Mounting Hole	9	TRUE	
LCL1_Out	3 Position Terminal Block 5.08mm	J6	3 Pin Terminal	3PinTerminal	1	TRUE	
LCL1_In	3 Position Terminal Block 5.08mm	J7	3 Pin Terminal	3PinTerminal	1	TRUE	
LCL2_Out	3 Position Terminal Block 5.08mm	J8	3 Pin Terminal	3PinTerminal	1	TRUE	
LCL2_In	3 Position Terminal Block 5.08mm	J9	3 Pin Terminal	3PinTerminal	1	TRUE	
ADC2	SSQ - Samtec 2.54mm Square Tail Dual Row Socket Strip 8.5mm Profile - Fast Stock	J11	SSQ-110-03-T-D	SSQ-110-03-T-D	1	TRUE	
EPWM2	SSQ - Samtec 2.54mm Square Tail Dual Row Socket Strip 8.5mm Profile - Fast Stock	J12	SSQ-110-03-T-D	SSQ-110-03-T-D	1	TRUE	
M5 Earthing Hole		J18	M5 Earthing Hole	M5 Earthing Hole	1	TRUE	
30mH CM	30mH Custom CM Choke	L1, L2	CM Choke Custom	30mH Custom CM Chc	2	TRUE	Custom
4mH		L3_1, L3_2, L3_3, L5_1, L5_2, L5_3	4mH Custom	4mH Custom Inductor	6	TRUE	Custom
380uH		L4_1, L4_2, L4_3, L6_1, L6_2, L6_3	380uH Custom	380uH Custom Inducto	6	TRUE	Custom
10k_2512	SMD Chip Resistor, 10 kohm, ± 1%, 2 W, 2512 [6432 Metric], Thick Film, High Power	R1_1, R1_2, R1_3, R3_1, R3_2, R3_3	2512 Resistor	MCHP122WF1002T4E	6	TRUE	
							Updated to CRCW1206348RFKEA. SMD Chip Resistor, 348 ohm, ± 1%, 250 mW, 1206 [3216 Metric], Thick Film, General Purpose, £0.05
130_1206	SMD Chip Resistor, 130 ohm, ± 1%, 250 mW, 1206 [3216 Metric], Thick Film, General Purpose	R2_1, R2_2, R2_3, R4_1, R4_2, R4_3	1206 Resistor	CRCW1206130RFKEA	6	TRUE	
20k_0805	SMD Chip Resistor, 20 kohm, ± 1%, 125 mW, 0805 [2012 Metric], Thick Film, General Purpose	R5, R7, R11, R13	0805 Resistor	CRCW080520K0FKEA	4	TRUE	Bias Resistor
200k_0805	SMD Chip Resistor, 200 kohm, ± 1%, 125 mW, 0805 [2012 Metric], Thick Film, General Purpose	R6, R10, R12, R16, R33_1, R33_2, R33_3, R36_1, R36_2, R36_3, R37_1, R37_2, R37_3, R40_1, R40_2, R40_3	0805 Resistor	CRCW0805200KFKEA	16		Suggest 27 kOhm. Gain 9. Big resistors have high freq leakage inductance.
10k_0805	SMD Chip Resistor, 10 kohm, ± 1%, 125 mW, 0805 [2012 Metric], Thick Film, General Purpose	R8, R9, R14, R15, R34_1, R34_2, R34_3, R35_1	0805 Resistor	CRCW080510K0FKEA	16		Suggest 3k Ohm
I3	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP1, TP15	PCB 1.32mm TestPoint	PCBTestpoint	2	TRUE	
I1	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP2, TP13	PCB 1.32mm TestPoint	PCBTestpoint	2	TRUE	
I2	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP3, TP14	PCB 1.32mm TestPoint	PCBTestpoint	2	TRUE	
VDC	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP4, TP16	PCB 1.32mm TestPoint	PCBTestpoint	2	TRUE	
VC_2A	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP6	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
VC_2B	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP7	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
VC_2C	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP8	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
VC_1A	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP9	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
VC_1B	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP10	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
VC_1C	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP11	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
OT1	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP17	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
PWMEN1	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP18	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
OT2	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP19	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
PWMEN2	20-313143 PCB Test Point, White, Through Hole Mount, 1.32 mm, Phosphor Bronze, Tin Plated Contacts	TP20	PCB 1.32mm TestPoint	PCBTestpoint	1	TRUE	
AGND	H2182-01 PCB Test Point, PCB Mount, 1.9 mm, Brass, Tin Plated Contacts	TP35	1.9mm Hole	GroundTestPoint	1	TRUE	
LV25P	Undefined or Miscellaneous	U1_1, U1_2, U1_3, U2_1, U2_2, U2_3	LV-25-P	LV25P	6		In Lab
4ch Op Amp	Quad, 30-V, 3-MHz, high slew rate (13-V/µs), In to V+, JFET-input op amp	U3, U4, U5, U6	SOIC-14	TL074D	4	TRUE	

