ELEC70012 Full Custom IC Design: Lab Logbook

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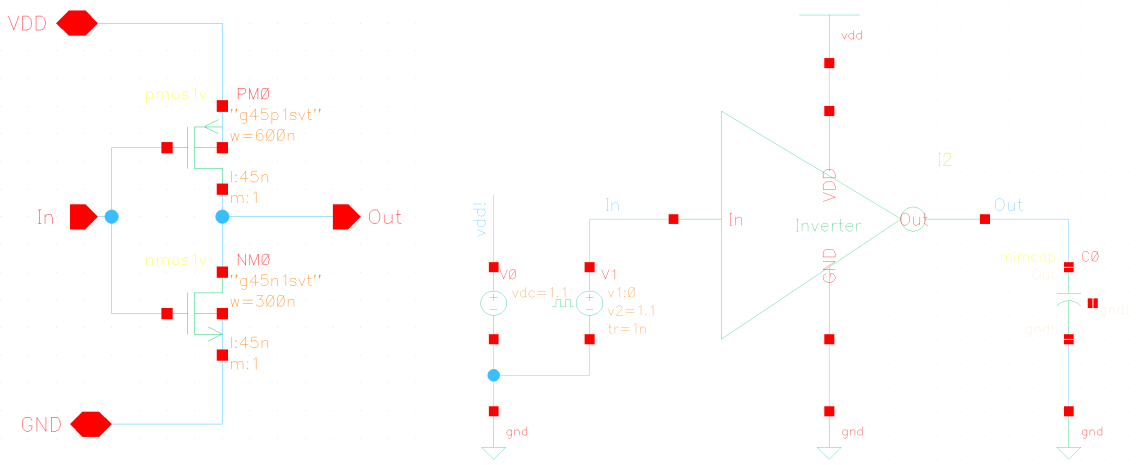
While simulation waveforms are inserted in the main logbook content, for the interests of space-saving and readability, all the schematics, layouts, and proofs for clean DRC and LVS are attached in the front. When necessary, references are made to these diagrams. In addition, note that the section numbers are not in chronological order, rather they correspond to the sections in the lab manual.

Many transistor dimensions are explored during simulations to achieve specific oscillation frequencies or other characteristics, and these are documented in the main body. However, for implementation on the edge-triggered D Flip-flop (DFF), the transistor sizes might have been adjusted to satisfy compromises based on transistor area and time constraints; in terms of layout, the heights of the NAND, Inverter and DFF cells have all been all standardised to $3\mu m$. After numerous revisions, the schematics and layouts below reflect the final implementation for the DFF cell.

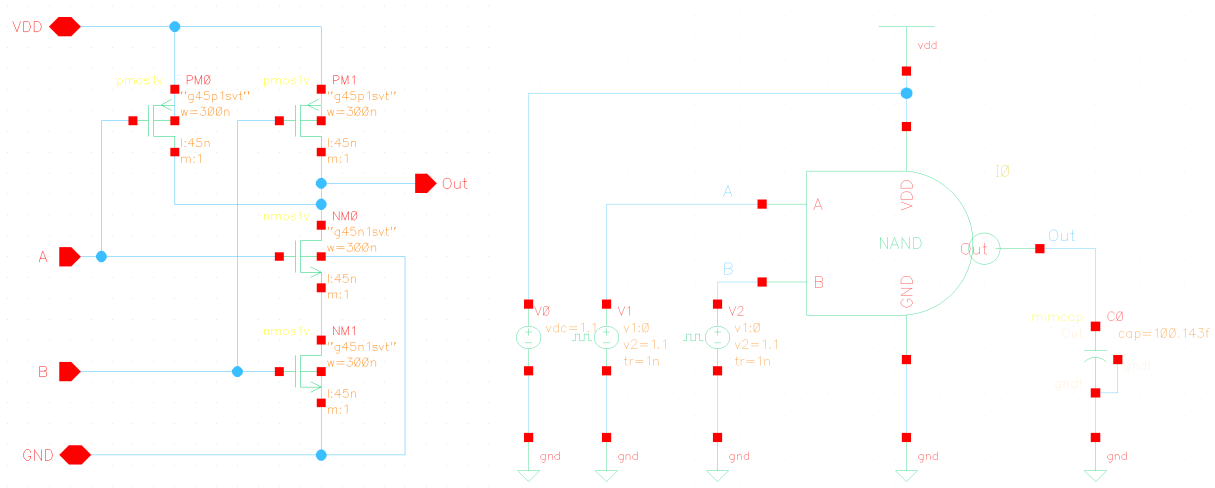
0.1 Schematics



(a) Inverter schematic.

(b) Inverter test-bench schematic.

Figure 1



(a) NAND schematic.

(b) NAND test-bench schematic.

Figure 2

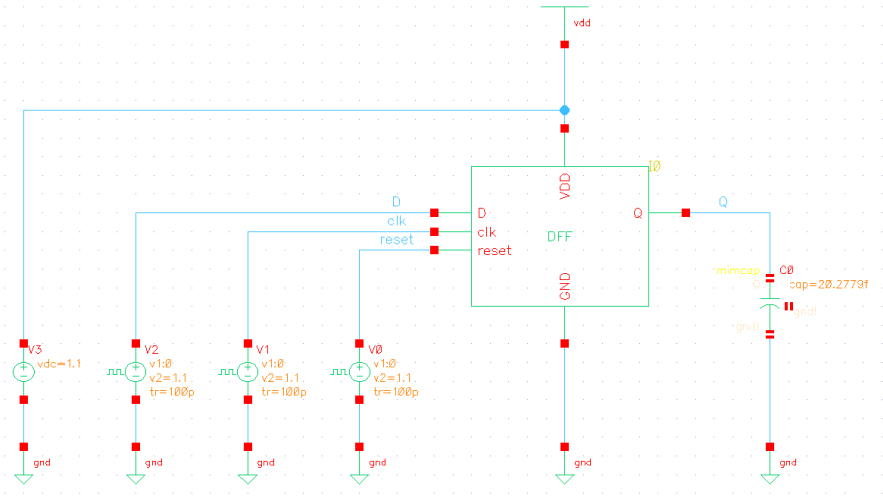


Figure 3: DFF Testbench schematic.

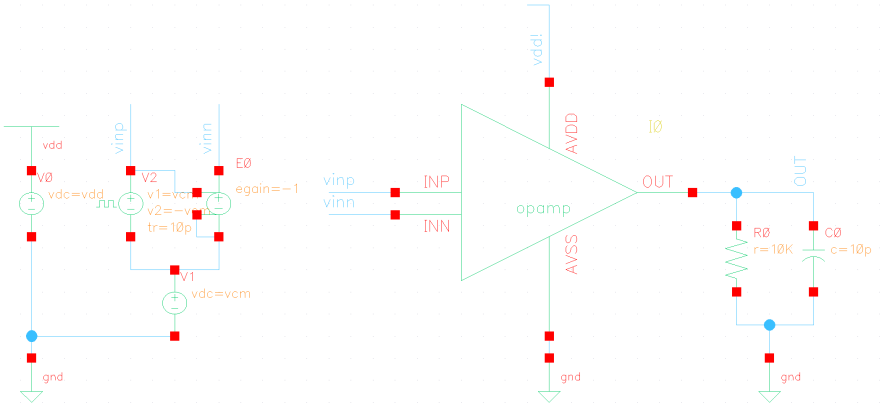
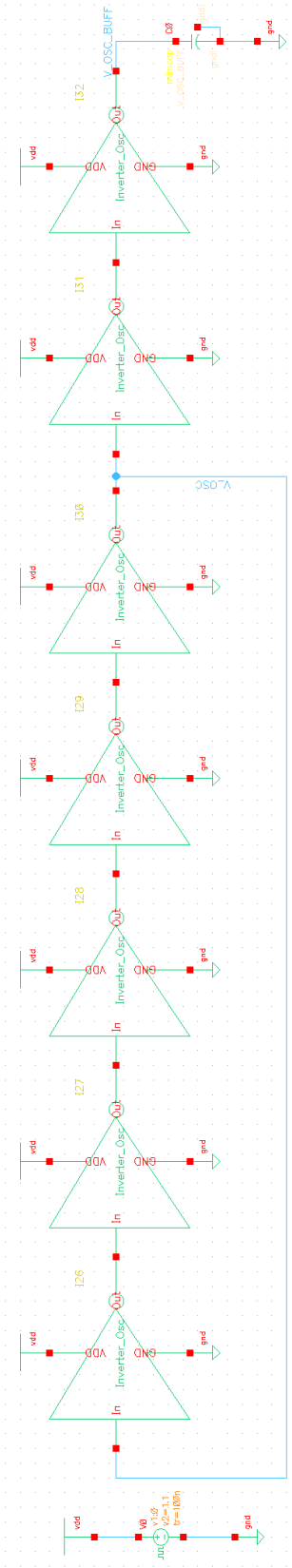
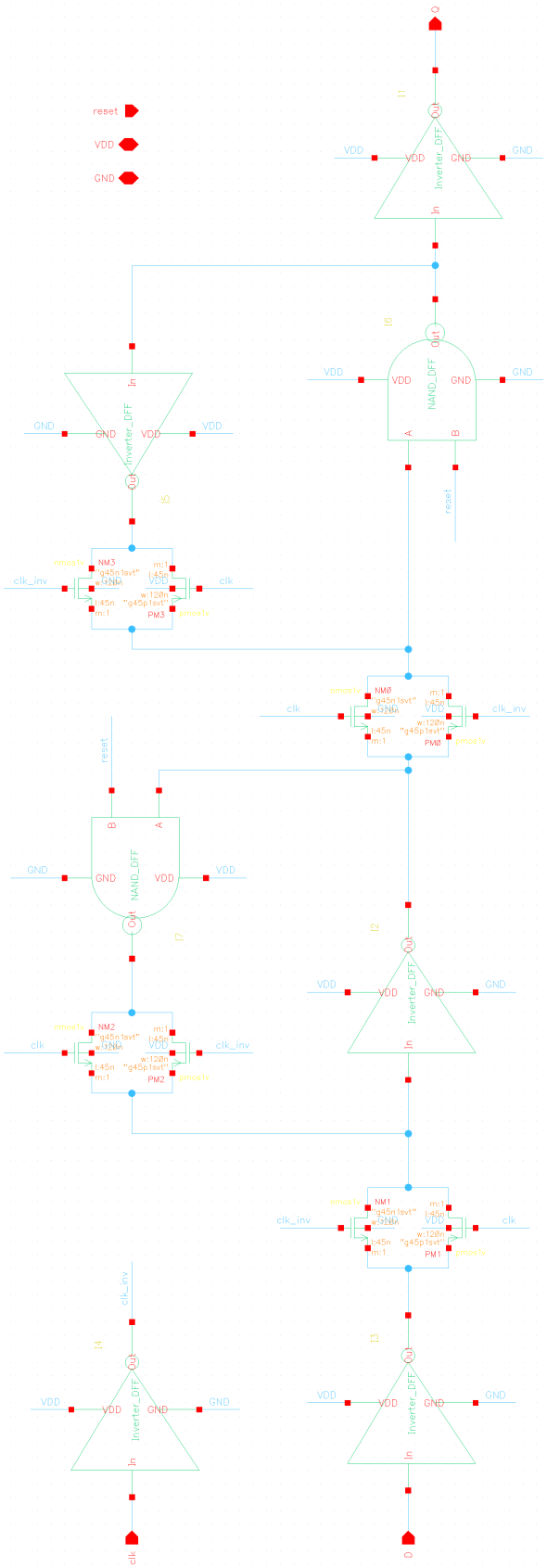


Figure 4: Op-amp testbench schematic.



(a) 5-stage ring oscillator test-bench schematic.



(b) DFF schematic.

Figure 5

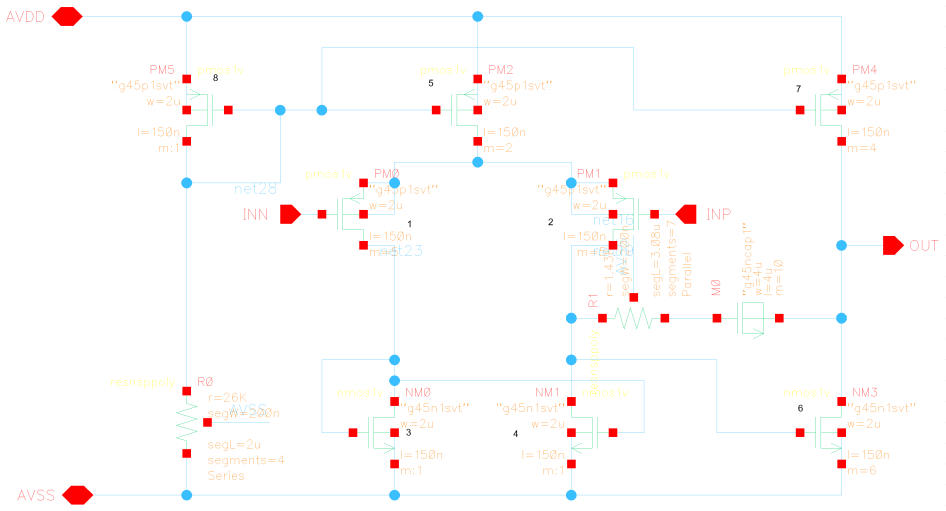
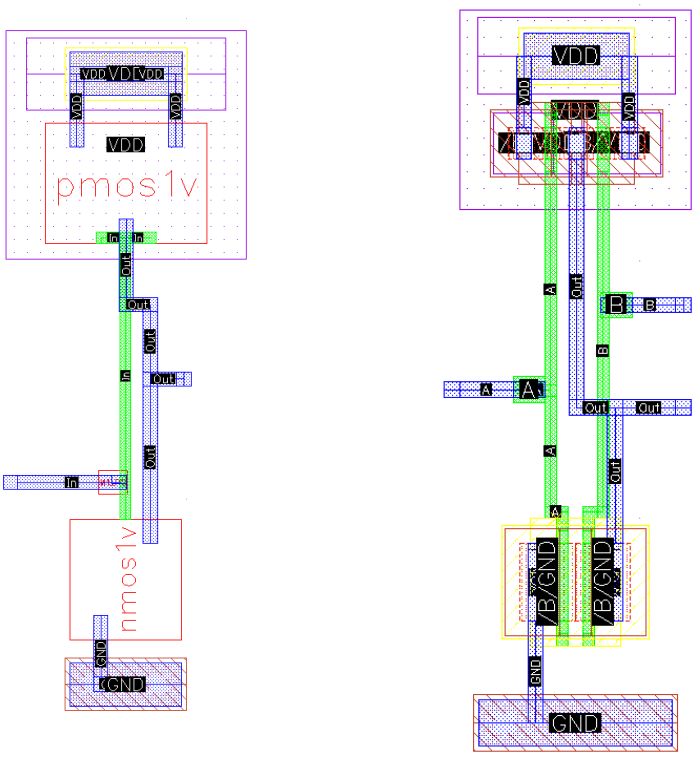


Figure 6: Op-amp schematic.

0.2 Layouts



(a) Inverter layout.

(b) NAND layout.

Figure 7

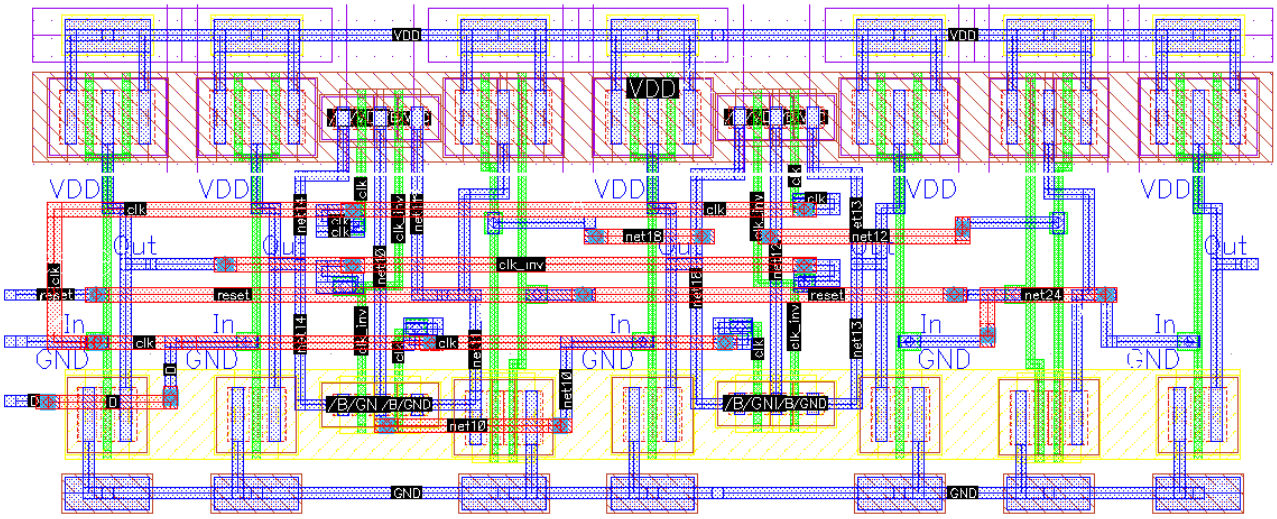


Figure 8: DFF Layout.

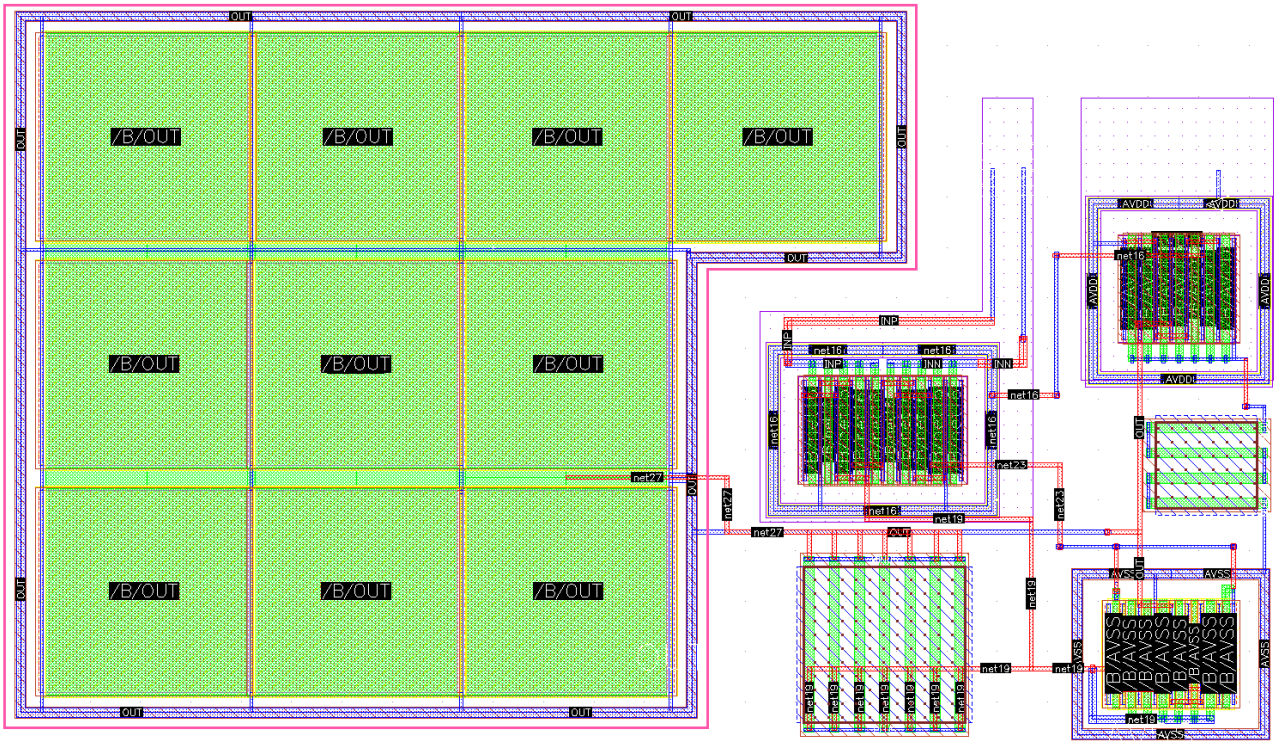


Figure 9: Op-amp Layout

0.3 Screenshots for clean DRC and LVS

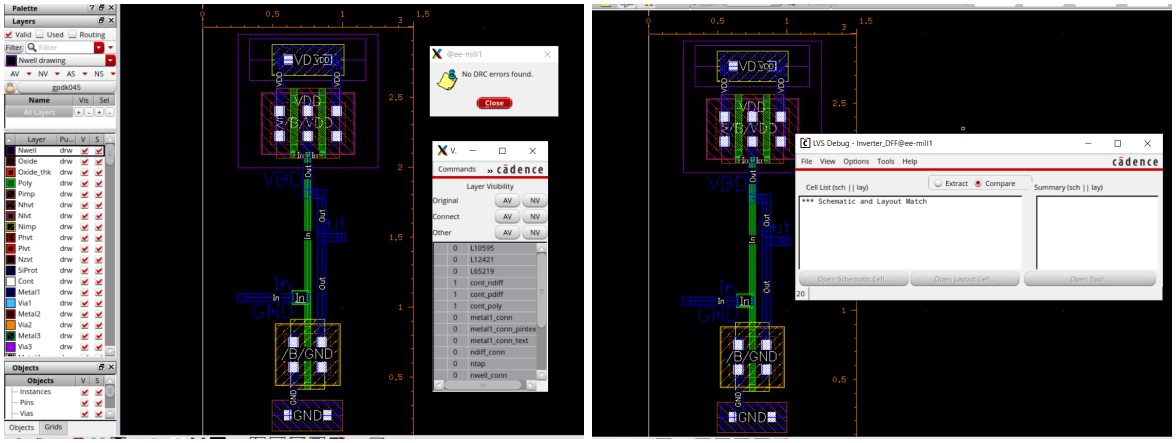


Figure 10: Inverter layout DRC and LVS passed.

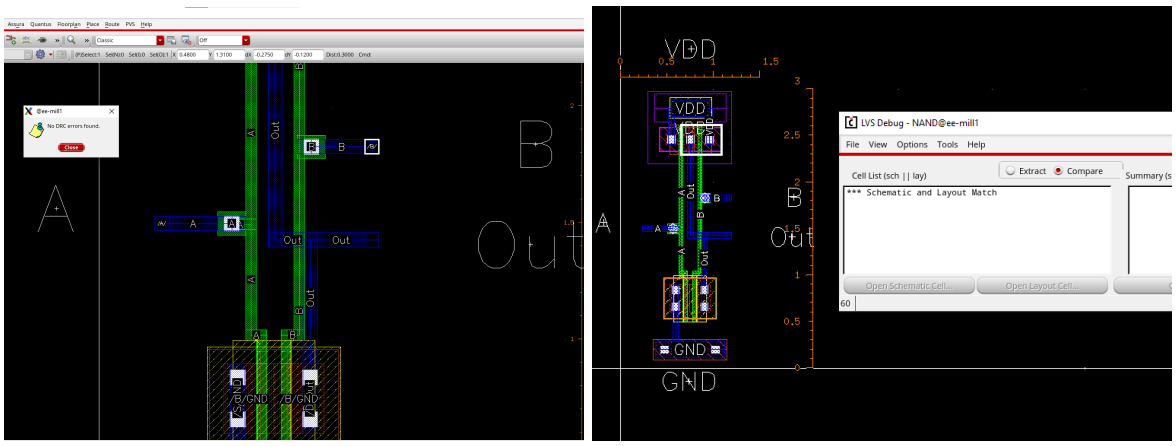


Figure 11: NAND layout DRC and LVS passed.

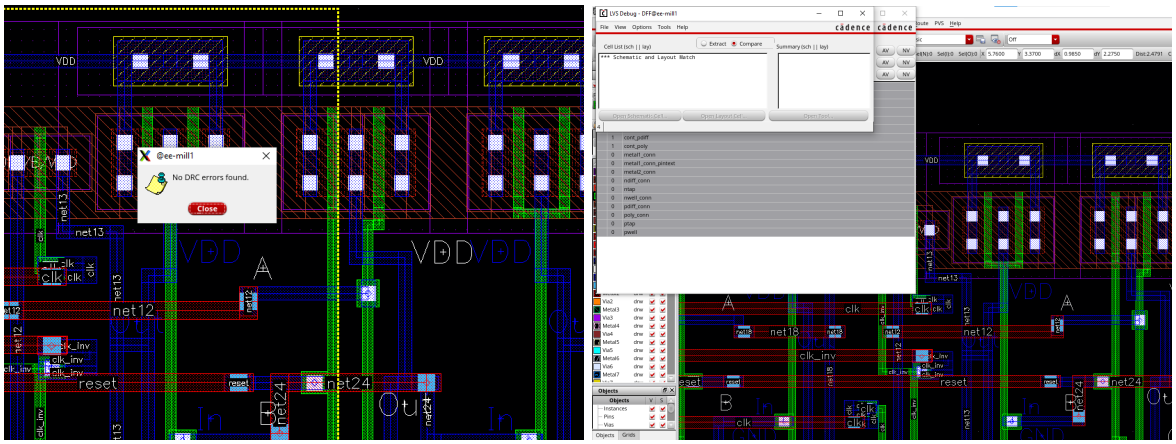


Figure 12: DFF layout DRC and LVS passed.

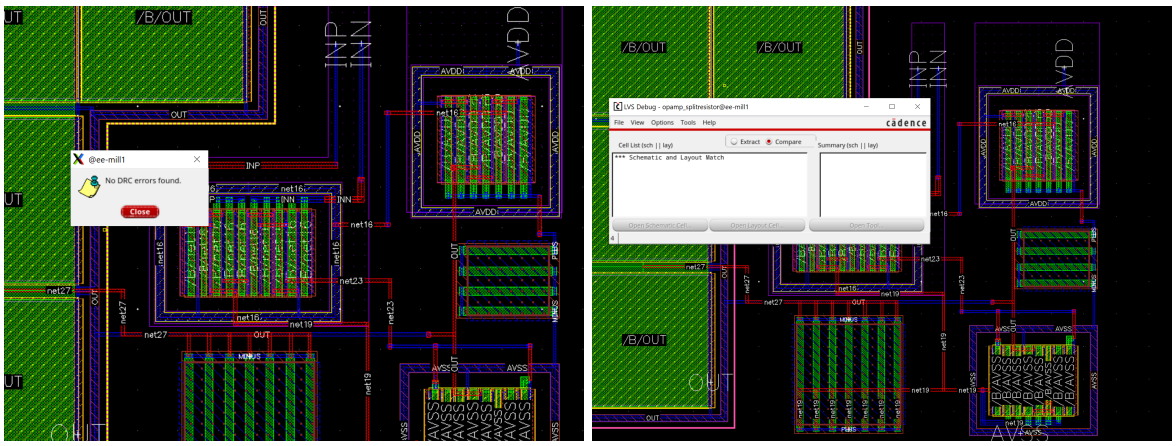


Figure 13: Two stage Miller Op-Amp layout DRC and LVS passed.

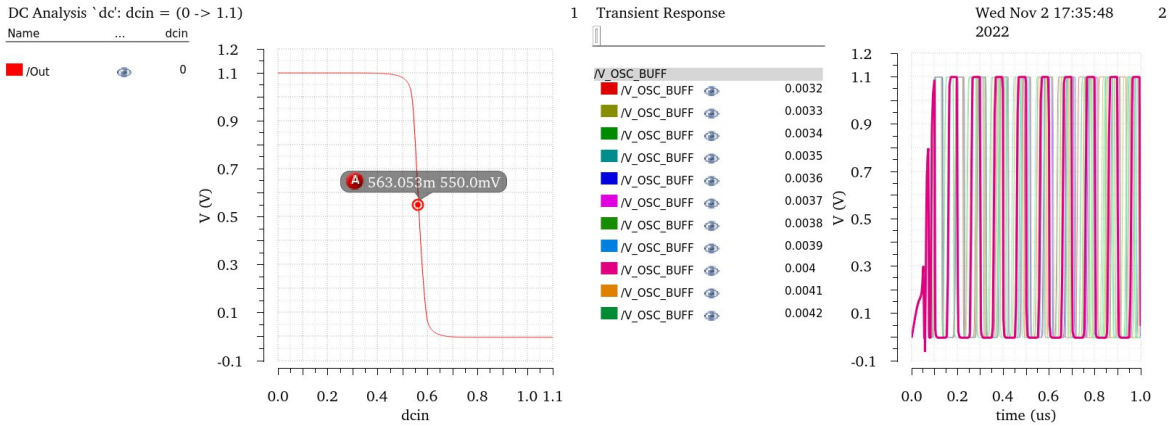
1.4 Inverter schematic entry and tests

For the inverter, the lengths of both the PMOS and NMOS are 45nm, and the lengths are 600nm and 300nm respectively. as shown in the schematic in figure 1a. Using the testbench circuitry shown in figure 1b, the inverter output switches from 1.1V (HIGH) to 0V (LOW) at an input threshold voltage of 563mV, which is approximately $V_{DD}/2$, as shown in figure 14a; this indicates that it equally rejects noise in both states.

1.5 Ring Oscillator

The deliverable of this task is a 5-stage ring oscillator which drives a 500fF load at an oscillation frequency of 10MHz at $27°C$, as shown in figure 5. The startup of the oscillator is triggered when the supply ramps up from 0 to 1.1V in 100ns.

After performing parametric analysis on a range of PMOS widths, the final design incorporates a PMOS width of 4mm and an NMOS width of 2.79mm, with the oscillation frequency achieved being **10.03MHz**; the waveform and schematic are in figure 14b and 5a respectively.



(a) Transient simulation of inverter for determining signal-crossing threshold.

(b) Bold waveform (PMOS width = 4mm) reflects parameters chosen for final design.

Figure 14: Inverter and ring oscillator waveforms.

Input Transition	Propagation delay(ns)	
AB/A'B'	Forward transition	Backward transition
01/11	1.050	1.613
10/11	1.041	1.615
00/11	1.090	0.941

Table 1: Propagation delays for NAND gate: input toggle to output toggle (ns)

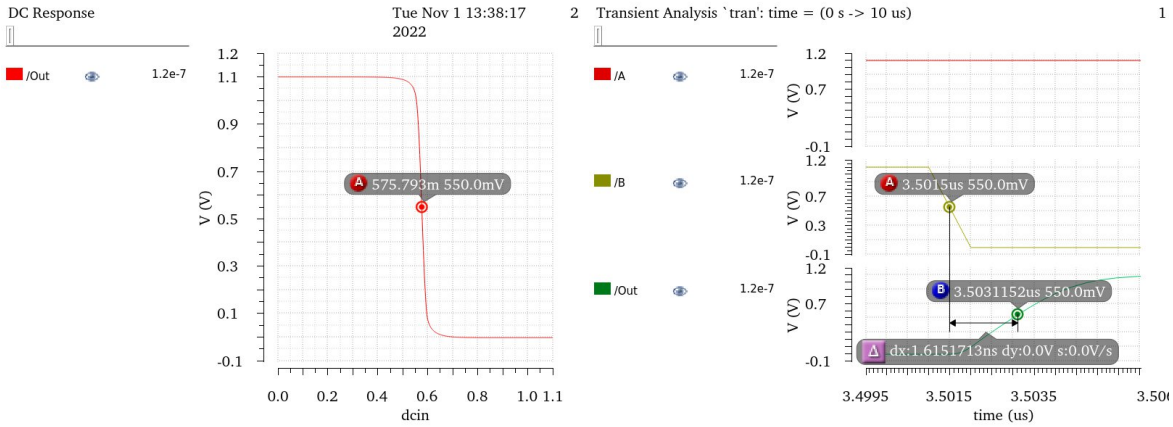


Figure 15: NAND crossover point and maximum delay time waveform (input B fall to output toggle).

2.4 Inverter Layout

While the design has been repetitively iterated throughout the lab to accommodate for requirements in later sections (NAND gate or DFF), the layout in figure 7a reflects the final design used for the DFF.

2.5 NAND Gate

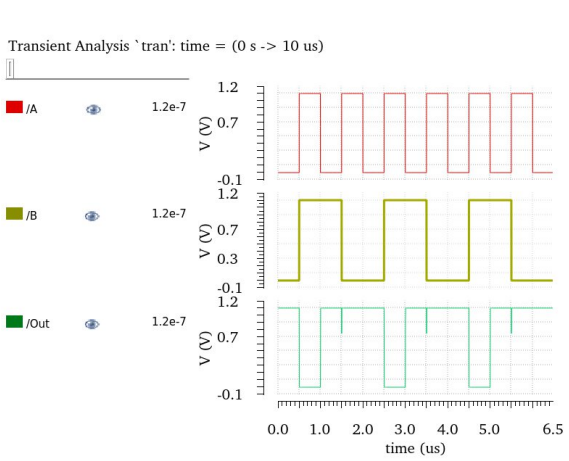
The overall aim is to design a NAND gate which drives a 100fF mimcap capacitor. The schematic and layout are in figures 2a, and 7b respectively. Tests were then performed using the test-bench circuit shown in figure 2b.

Overall, as shown in 16a, the operation of the gate is valid, though there is an undesired (but expected) glitch condition upon toggling both inputs A and B simultaneously. In addition, as shown in figure 15, the switching point is at approximately $V_{DD}/2$, which indicates that it is equally resistive to noise when the input is high or low.

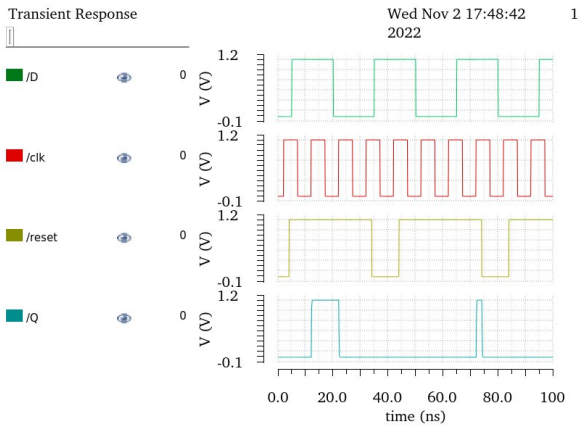
To investigate propagation delays, all 3 (or 6) possible input transitions that cause the output to toggle are observed; all the results are recorded in table 1, and the worst delay is shown in figure **??**. It was initially predicted that the propagation delay associated with A is higher, as there is a delay associated with the bottom NMOS bringing the source capacitance of the top NMOS fully to ground. Regardless, none of the delays exceeds 10ns as required, indicating that the design is suitable for operation in the DFF in the following section, provided that the clock is 100MHz or below.

2.6 Edge triggered D Flip-Flop

The aim of this task is to create an edge triggeed D Flip-flop (DFF), as shown in the schematic in figure 5b. This is tested with a $4\mu m$ by $4\mu m$ gpdk045 mimcap load at 100MHz, using the test-bench schematic in figure 3. After experiments with various transistor sizing, a transient simulation has then



(a) NAND testbench waveforms.



(b) DFF testbench waveforms. Note that the reset signal is active low.

Figure 16

been run to show that the DFF is working with the conditions mentioned, as shown in figure 16b. Indeed, the output is updated at the rising edge of the clock signal, and set to zero upon an active-low reset signal, Having confirmed that the operation is correct, a compact layout was then created, as shown in figure 8.

3.6 Two stage Miller Op-smp

This 2-stage operational amplifier, as shown in figure 6, is tested with a resistive capacitive load with a signal frequency of 200kHz, using the test-bench schematic in figure 4. With the recommended transistor sizing, a transient simulation has then been run to verify that all transistors are operating in saturation, as shown in figure 18. Finally, the layout is created, as shown in figure 9.

At a first glance, with the exception of PM0 and PM1 operating in region 3 (sub-threshold), all other transistors are operating in region 2 (saturation), which suggests an issue with the biasing of the input differential pair. While drift current dominates in saturation operation and diffusion in sub-threshold, a closer study of the sub-threshold region reveals that it is an operating region between cutoff and triode where the drain current exhibits a log exponential behaviour with respect to the gate voltage; therefore, the current does "saturate" towards a fixed value independent of the drain voltage, making it a suitable region for low power operation in CMOS designs.

The following subsections detail more rigorous circuit analysis of the op-amp's characteristics.

DC analysis

With respect to the DC analysis on figure 19b, it can be observed that V_{out} varies with respect to the DC voltage. This indicates that there is an offset in the differential pair, which leads to a common mode voltage at the output. Furthermore, there might be an input-referred offset voltage due to the unbalanced V_{DS} at the output transistors, which explains why $V_{out} \neq 0$ despite a zero differential input.

Gain

With respect to the labels in figure 6, the first stage A_{V1} in the signal path is a long tail differential pair 1 and 2 that provides the high current gain, and it determines the CMRR and PSRR. The second stage

A_{V2} is an inverting common-source amplifier 6 that provides high voltage gain.The transconductance gains G_{m1} and G_{m2}, and output impedances R_{o1} and R_{o2} of the two stages are by observation:

$$G_{m1} = g_{m2} \qquad G_{m2} = g_{m6}$$
$$R_{o1} = \frac{1}{g_{o2} + g_{o4}} \qquad R_{o2} = \frac{1}{g_{o6} + g_{o7}(+g_{load})}$$

For the purposes of simplifying the analysis, the output load g_{load} is omitted, which yields the open-loop differential gain under no-load condition:

$$A_V = A_{V1} \times A_{V2} = -G_{m1}R_{o1} \times -G_{m2}R_{o2} = \frac{g_{m2}}{g_{o2} + g_{o4}} \frac{g_{m6}}{g_{o6} + g_{o7}}$$

Using the small signal parameters in the "DC-operating points" results obtained post-simulation (figure 18), the gain is:

$$A_V = \frac{g_{m2}}{g_{o2} + g_{o4}} \frac{g_{m6}}{g_{o6} + g_{o7}} = \frac{350.4\mu}{1/86.50k + 1/112.0k} \frac{1.114m}{1/12.73k + 1/26.77k} = 164 \approx 44.3dB$$

If the 10k output load resistance in parallel with $g_{o6} + g_{o7}$ is included, then the gain is effectively reduced to 88.24 or 38.91dB, closer to the figure shown in the AC simulation. To express the gain in terms of the circuit's operational parameters, more rigorous analysis can be performed, though it should be noted that these relationships are often too simple for modern transistor geometries.

In general, the drain current of a transistor in saturation is $I_D = \frac{\mu C_{OX}}{2} \frac{W}{L}(V_{GS} - V_{Th})^2(1 + \lambda V_{DS})$. Therefore, performing small signal analysis of the drain current with respect to V_{GS} and V_{DS} gives the transconductance g_m and output conductance g_o:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{OX} \frac{W}{L}(V_{GS} - V_{Th}) \qquad g_o = \frac{\partial I_D}{\partial V_{DS}} = \lambda \frac{\mu C_{OX}}{2} \frac{W}{L}(V_{GS} - V_{Th})^2$$

For a coarse approximation, it is assumed that μ, C_{OX}, λ and $V_{OD} = V_{GS} - V_{Th}$ across all devices are matched. Using a unit width of $2\mu m$, the W/L of transistors 2,4,6,7 are 5,1,6,4 respectively, which yields an approximation in terms of the early voltage and overdrive voltage V_{OD} of the transistors:

$$A_V = \frac{5}{\frac{\lambda}{2}(5+1)(V_{GS} - V_{Th})} \times \frac{6}{\frac{\lambda}{2}(6+4)(V_{GS} - V_{Th})} = \frac{2}{\lambda^2(V_{GS} - V_{Th})} = \frac{2}{\lambda^2 V_{OD}}$$

3dB Cutoff-frequency

With respect to the AC analysis of the op-amp in figure 19a, the 3dB cutoff frequency is 399kHz. This indicates that at this frequency the signal power falls to half the power at full-pass.

For an analytic solution of the 3-dB cutoff bandwidth, the frequency response is obtained by analysing the high frequency small signal equivalent circuit. If the load capacitance C_L and resistance (or conductance g_{load}) is accounted for, after rigorous analysis, the frequency response is then:

$$\frac{v_{out}}{v_{in}} = A_{V1}A_{V2} \times \frac{1 - j\frac{f}{f_z}}{(1 + j\frac{f}{f_{p1}})(1 + j\frac{f}{f_{p2}})}$$

where f_z is associated with the miller capacitor C_C and nulling resistance R_Z, f_{p1} is associated with the impedance on the output node of stage 1 (including impedance referred from stage 2 on stage 1), and f_{p2} is associated with the impedance on the output node of stage 2 (including impedance of the output load).

$$f_z = \frac{1}{2\pi C(\frac{1}{G_{m2}} - R_Z)} \qquad f_{p1} = \frac{1}{2\pi G_{m2} R_{o2} R_{o1} C_C} \qquad f_{p2} = \frac{G_{m2}}{2\pi C_L}$$

Note that the expression for f_{p2} is a simplification, assuming that C_L is significantly larger than the miller capacitance and parasitic capacitances, such that it dominates.

Nevertheless, f_{p2} is s non-dominant pole, and the location of the zero f_z is close to f_{p2}. Therefore, the turning point or the 3dB cutoff frequency of the magnitude bode plot is defined by f_{p1}.

Slew rate

The slew rate is the fastest rate at which the output voltage can swing, so it determines the maximum frequency of the op-amp input. For this 2-stage op-amp circuit, the startup circuit consisting of PMOS 8 and R0 determines the bias current, and this is mirrored to the tail current in PMOS 5 of the differential pair. In the event of a large positive or negative input signal, all the current in PMOS 5 is drawn into or out of the miller capacitor (directly or through the current mirror 3 and 4), such that the slew rate is:

$$SR = \frac{I_{D5}}{C_C} = \frac{30.20\mu}{241.3f} = 1.252 \times 10^8 V/s$$

Improving gain

To improve gain, the input stage can be cascoded, by cascoding the current mirror and differential pair. Similarly, the output stage can be cascoded, by cascoding the common source amplifier and the current drain PMOS. In both cases, the advantage of the cascode is a significantly increased gain and PSRR (power supply rejection ratio). However, the disadvantages are as follows:

1. Increased area for transistors, and additional circuitry to bias cascode transistors,
2. Reduced stability due to increased impedance at the the output node of each stage, which leads to a larger time constant or smaller bandwidth; and,
3. Reduced common-mode voltage range or output swing capability, due to the need to keep more transistors in saturation.

Linear input range

For a multi-stage op-amp, the transconductance defines the rate of change of output current I_{out} against input voltage V_{in} or V_{GS} of stage 1, in other words $\frac{\partial I_{out}}{\partial V_{in}}$. Since the relationship is non-linear, an expression of the linear input range cannot be obtained trivially, though it can be empirically determined by the voltage change when the transconductance drops by 1% from its maximum value, which is:

$$0.01 \times G_m = 0.01 G_{m1} G_{m2} = 0.01 \times 350.4\mu \times 1.114m = 3.90 \times 10^{-7} A/V$$

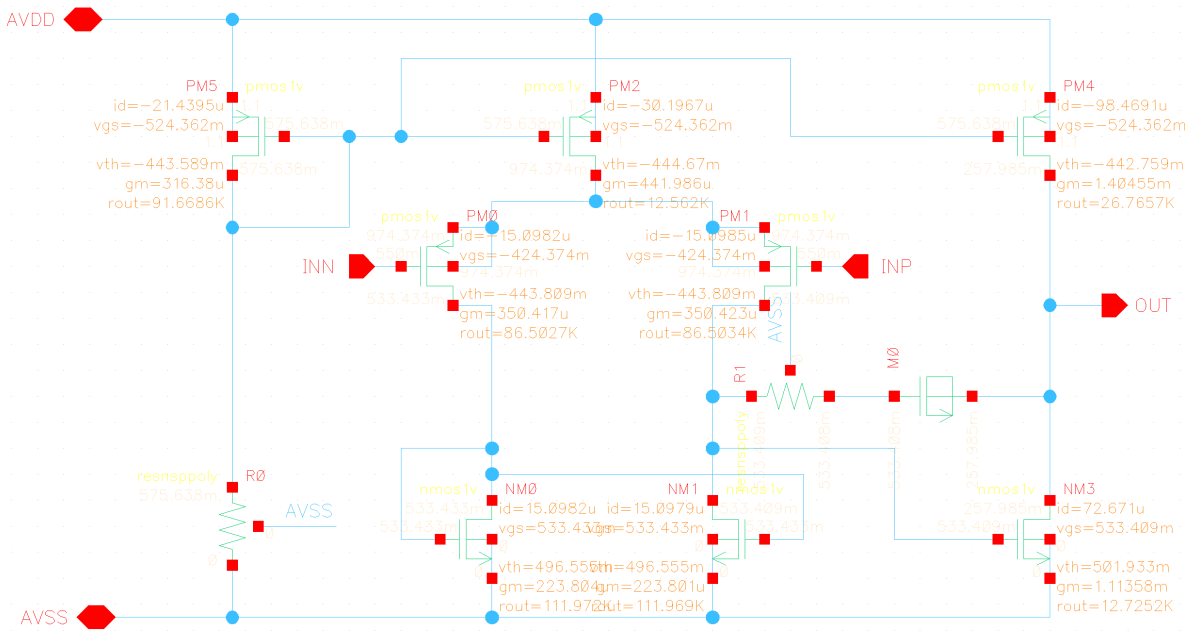


Figure 17: Op-amp operating points. All transistors in region 2 (saturation), except PM0 and PM1 in region 3 (subthreshold).

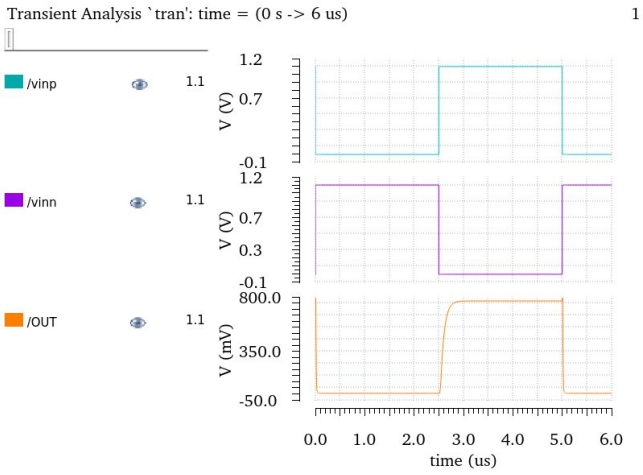
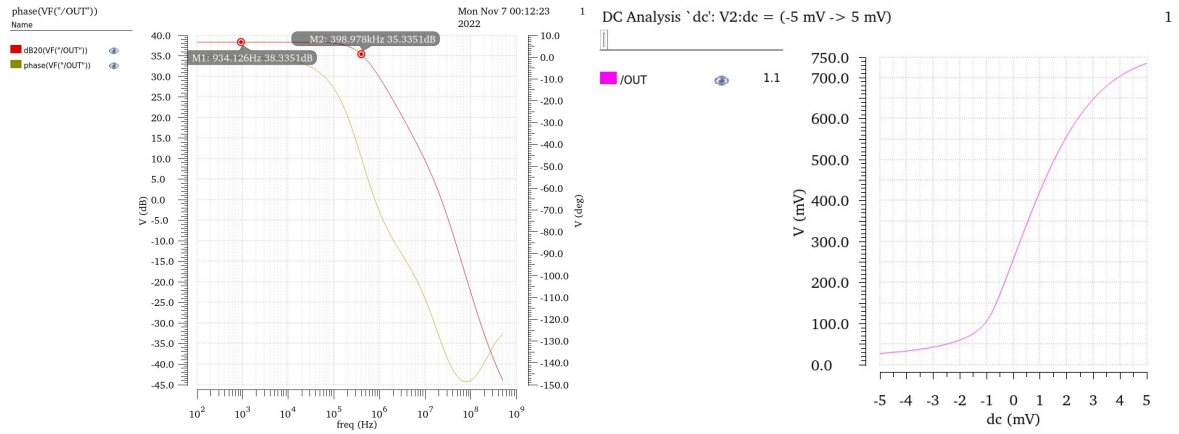


Figure 18: Op-amp transient simulation.



(a) AC analysis (frequency response) of op-amp.

(b) DC analysis for op-amp.

Figure 19