

5mA, Linear Performance, Fast Response LDO Regulator

1 Features

- 5mA output current capability: Tested up to 40mA
- Input Voltage Range: 1.8 to 2.0V
- Reference Voltage: 0.8V
- Selectable output voltages: 1.0V, 1.2V, 1.4V, 1.6V
- Shutdown mode for low current operation at 1.231 μ A typ.
- Low Dropout Voltage: mV typ. At 5mA
- Stable without external output capacitor
- Fast response and low overshoot during load transients
- Precise load and line regulation
- Low quiescent current: 113 μ A typ.
- High Power Supply Rejection Ratio

2 Description

The LDOC1S2YTC is a 5mA Low Dropout (LDO) linear regulator that provides good line and load regulation. Its linear performance and fast response, combined with its highly compact form factor, makes it a suitable candidate for low-noise and speed-critical applications such as wireless and wired communications.

Its operational amplifier not only provides high gain and stability, but also high noise rejection as the cascode-compensation eliminates the feedforward path from the supply to its output. Additionally, its relatively small compensation capacitor retains good bandwidth for rapid monitoring of changes at the output.

The output voltage is by default 1.6V, and can be digitally selected by means of 3 active low selection pins. The active-low shutdown pin also enables the device to enter a current idle mode, making it attractive for portable computing applications.

3 Electrical Characteristics

Unless otherwise noted, all tests are performed with operating conditions $T = 27^\circ\text{C}$, $V_I = 1.9\text{V}$, $I_O = 5\text{mA}$ ($R_{\text{load}} = V_O / I_O$), $V_{\text{Ref}} = 800\text{mV}$ and $V_{\text{Shutdown}} = V_I$. All results are obtained from the testbench *LDO_Testbench_Old*, with the exception of load transient related results (settling time and overshoot), which are obtained from *LDO_Testbench*.

Parameters	Symbol	Value at selected output voltage V_O (typ, min, max) ⁱ				Units	Conditions
		1.0	1.2	1.4	1.6		
Efficiency							
Dropout voltage	V_{DO}	73.14 61.46, 133.9	60.12 50.73, 106.9	51.05 43.19, 89.13	44.36 37.60, 76.47	mV	$V_I = 800\text{mV}$
Quiescent Current	I_Q	113.1 71.75, 167.1	113.0 71.71, 167.0	112.9 71.64, 166.9	112.8 71.53, 166.7	μA	
Shutdown mode Input Current	$I_{I,\text{SD}}$	1.231 0.1858, 5.05				μA	$V_{\text{Shutdown}} = 0$
Noise Regulation							
Power Supply Rejection Ratio ⁱⁱ	$\text{PSRR}_{10\text{kHz}}$	-59.47 -56.81, -61.73	-58.19 -55.56, -60.56	-57.44 -54.93, -59.98	-58.28 -56.73, -62.32	dB	$V_{I,\text{AC}} = 200\text{mV}_{\text{pk-pk}}$
	$\text{PSRR}_{25\text{kHz}}$	-57.12 -56.12, -58.61	-55.77 -54.87, -57.41	-54.81 -56.76, -53.93	-54.54 -53.34, -57.51		
Transient Response and Linearity							
Line Regulation ⁱⁱⁱ	$\Delta V_O / \Delta V_I$	1.067 0.6894, 1.533	1.231 0.7664, 1.765	1.301 0.7306, 1.843	0.3662 0.3662, 1.612	mV/V	$V_I = 1.7 - 2.1\text{V}$
Load Regulation ^{iv}	$\Delta V_O / \Delta I_O$	89.67 89.67, 127.7	109.7 109.7, 155.8	131.8 131.7, 186.7	161.2 161.2, 228.9	mV/A	$I_O = 4.95 - 5.05\text{mA}$
Temperature Regulation ^v	$\Delta V_O / \Delta T$	45.16 41.26, 65.74	38.02 36.73, 55.62	33.95 33.52, 48.81	13.65 13.65, 17.51	$\mu\text{V}/^\circ\text{C}$	$T = 20 - 30^\circ\text{C}$
Settling Time ^{vi}	t_s	2.844 2.067, 3.334	2.933 2.182, 4.012	2.986 2.368, 4.208	3.124 2.761, 7.542	μs	$I_{O_1} = 5\text{mA}$ $I_{O_2} \approx 0\text{mA}$ $t_{\text{Load1} \Rightarrow \text{Load2}} = 1\mu\text{s}$ $FoM = t_r \frac{I_Q}{I_{O,\text{Max}}}$
Overshoot ^{vi}	$V_{\text{Max}} - V_O$	4.215 4.168, 11.04	6.205 5.646, 13.22	7.454 6.789, 15.22	8.524 7.690, 17.03	mV	
Figure of Merit	FoM	64.33	66.29	67.42	70.48	ns	

4 Performance Curves¹

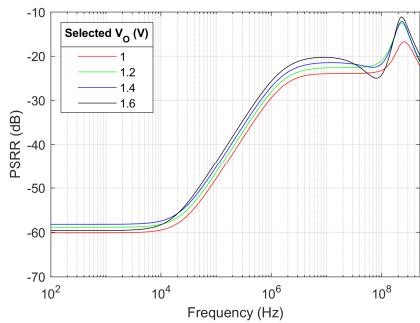
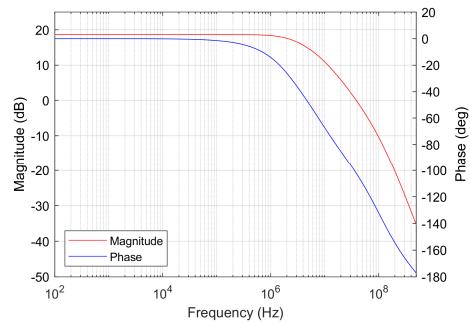
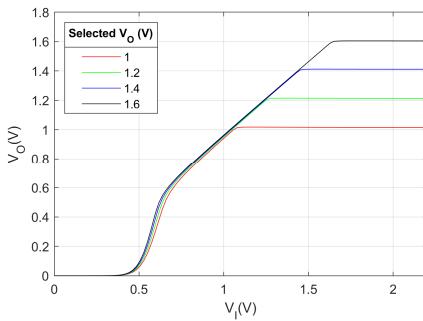
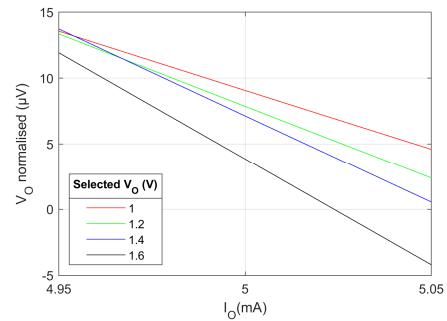
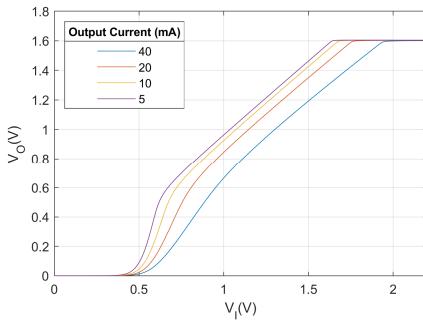
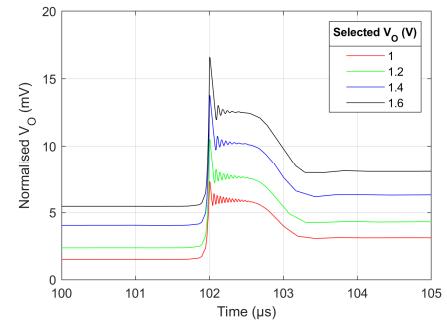
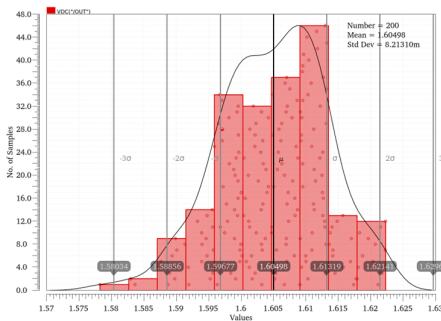
Figure 1 Power Supply Rejection RatioⁱⁱFigure 2 Operational Amplifier Frequency Response^{vii}Figure 3 Line Regulationⁱⁱⁱ at selected output voltagesFigure 4 Load Regulation: Output current sweep^{iv}Figure 5 Line Regulationⁱⁱⁱ at various output currentsFigure 6 Transient at load change: typical responses^{vi}

Figure 7 Monte Carlo analysis: Variation of nominal V_o (1.6V), sample size 200.

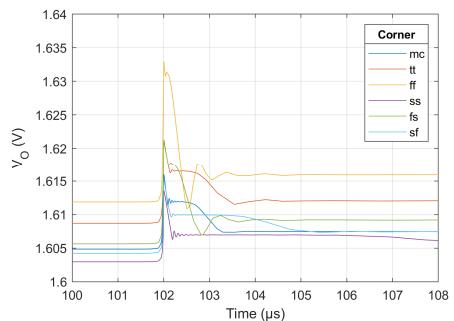
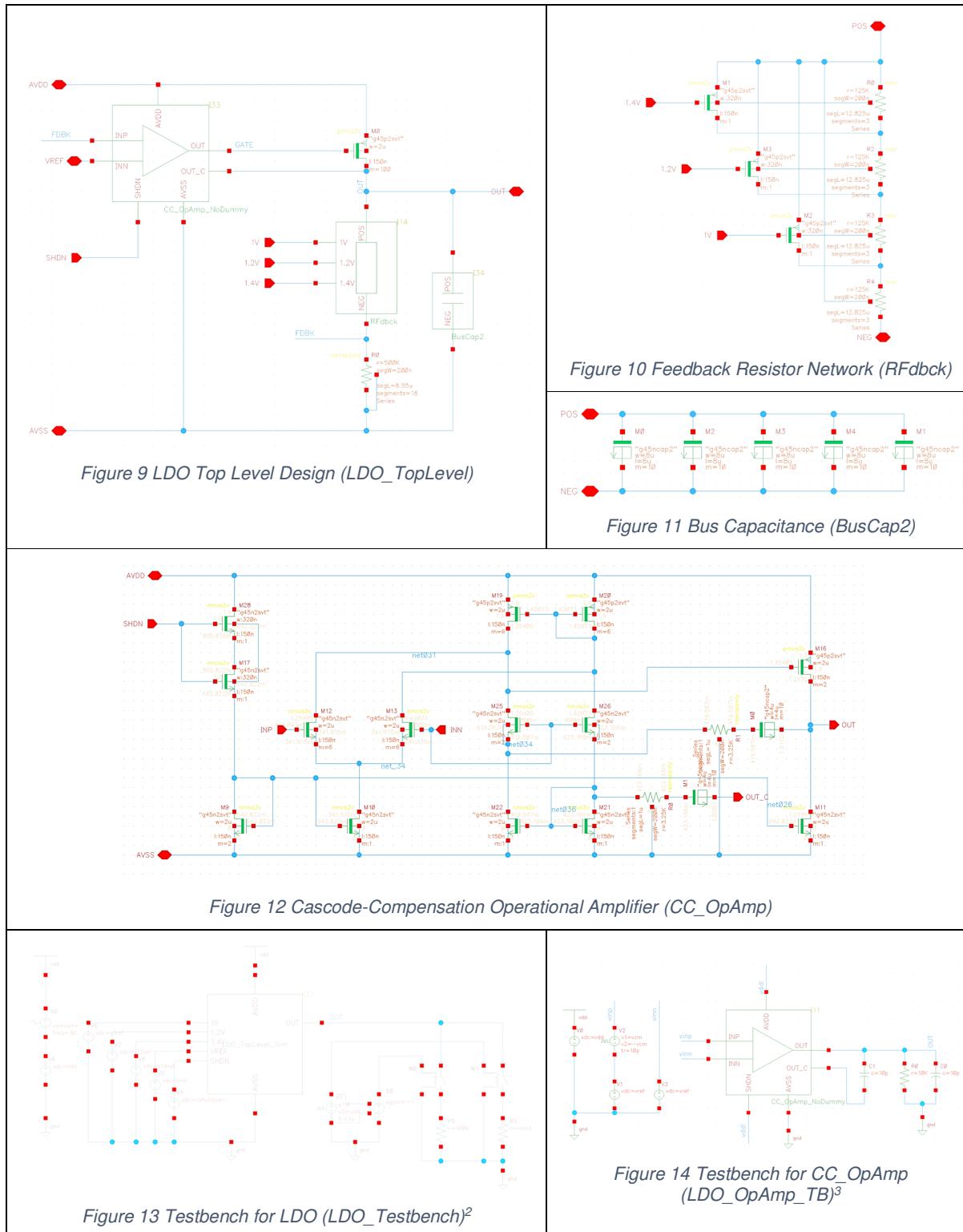


Figure 8 Transient at load change: response at mc, tt, ff, ss, fs and sf corners (V_o = 1.6V)

¹ V_o is normalised for load, temperature and transient graphs (figures 4, 5 and 6) to compare the response at various V_o . Nominal V_o is V_o minus mean of V_o . While Figures 1 to 4 show variations at typical performance, Figures 6 and 7 show variations due to process variations and device mismatch.

5 Circuit Schematics

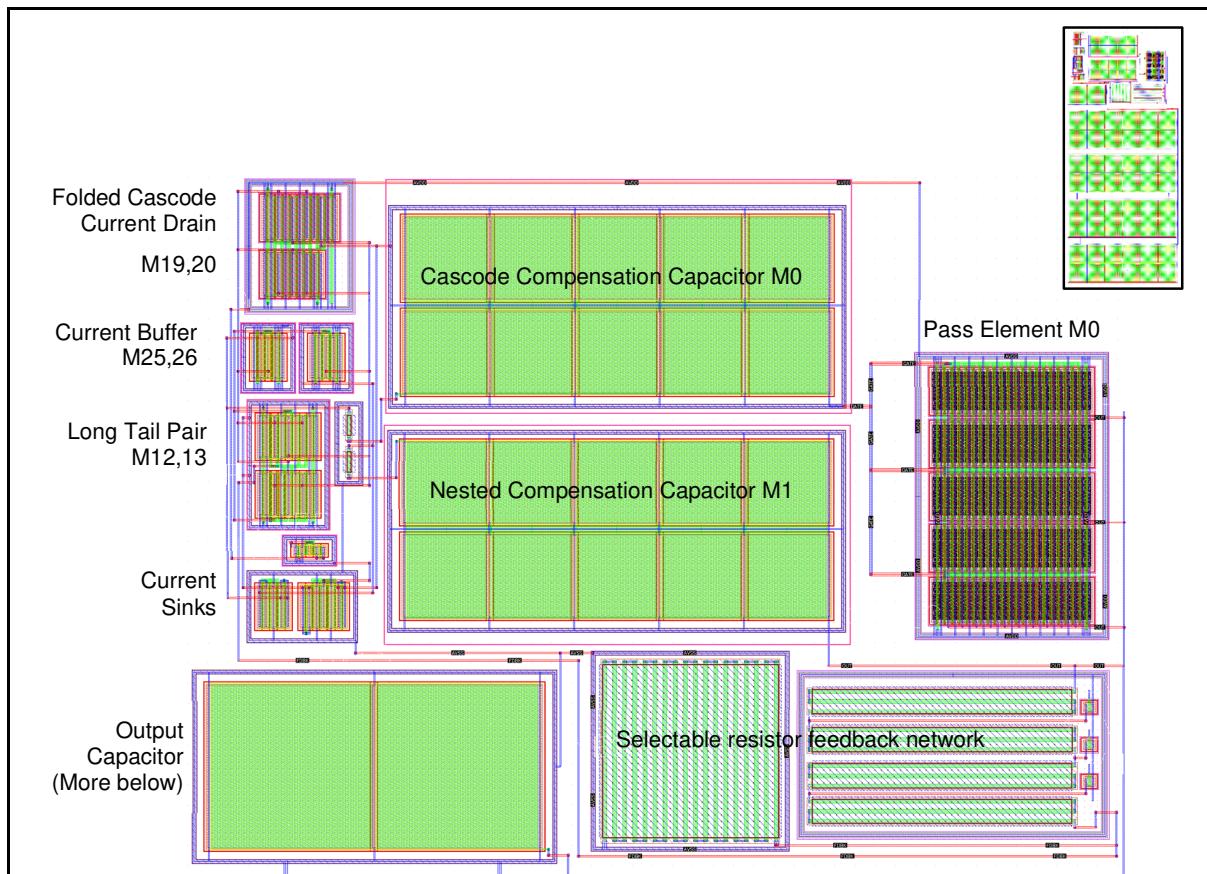


² Switched output load only used only for load transient test. In other tests, an older variant of the testbench (*LDO_Testbench_Old*) is used, where the load is only one resistor R_{load} , such that $I_o = 5\text{mA}$ ($R_{load} = V_o / I_o$).

³ Negative input terminal (INN) of the Op-Amp fixed to 0.8V to align with operation conditions of Op-Amp in the LDO. Additionally note that the terminal is used to bias the voltage of the current buffer transistor gates.

6 Circuit Layout

The full layout of this circuit is $50.86\mu\text{m} \times 116.88\mu\text{m}$ which yields a total area of $5945 \mu\text{m}^2$ or 0.005945 mm^2 . For clarity, the main diagram below only shows the top portion of the circuit; the breadcrumb in the upper right hand corner shows the entire circuit, including the bank of output capacitors.



The following figures shows the proofs for clean DRC and LVS for the top-level design.

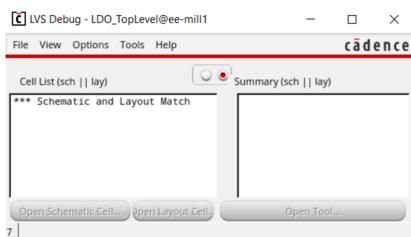


Figure 16 Clean DRC

Figure 15 Clean LVS

ⁱ Default Output voltage is 1.6V. Active-low Vo pins (`vxref`), $x=\{1,1.2,1.4\}$, automatically programmed to the selected Vo (`vout`) with the directive `vdd*ceiling(abs(vout-x))`. Min and max values obtained from corner analysis tests.

ⁱⁱ AC Test: 100-500MHz, 50 points per decade. $V_{I,AC} = 200\text{mV}_{\text{pk-pk}}$

ⁱⁱⁱ Voltage Sweep: $V_I = 0 - 2.2\text{V}$, 100 Linear Steps. Line Regulation ($\Delta V_O / \Delta V_I$) computed for regulation region, 1.7 - 2.1V.

^{iv} Resistance Sweep: Centre = $R_{load} = V_O / I_O$, Span = 50, 100 Linear Steps. Load Regulation ($\Delta V_O / \Delta I_O$) computed at nominal output current, 4.95 - 5.05mA.

^v Temperature Sweep: $T = 20 - 30^\circ\text{C}$, 100 Linear Steps. Temperature regulation ($\Delta V_O / \Delta T$) computed across entire sweep region.

^{vi} Load Transient Test for switching between large and small load: $I_{O1} = 5\text{mA}$ ($R_{load1} = V_O / I_{O1}$), $I_{O2} \approx 0\text{mA}$ ($R_{load2} = 100\text{k}\Omega$). $t_{sim}=200\mu\text{s}$, $t_{Load1}=0-100\mu\text{s}$, $t_{Load2}=100-200\mu\text{s}$, $t_{Load1 \Rightarrow Load2} = 1\mu\text{s}$.

^{vii} LDO_OpAmp_TB used for testing. $V_{DD} = 1.9\text{V}$, $V_{I,DC} = V_{DD}/2$, $V_{I,AC} = 1.6\text{V}_{\text{pk-pk}}$.