Overview

Purpose of a Linear Dropout Regulator (LDO)

To provide a steady, isolated voltage supply under all conditions, regardless of fluctuations in supply and load.

Specifications and targets for the proposed LDO

Device specifications, desirable characteristics, and important parameters to be optimised for good linearity and transient response:

1. Specifications
    1. Input Voltage $V_I = 1.8 - 2V$
    2. Output Voltage $V_O = 1, 1.2, 1.4, 1.6$
    3. Output Current $I_O > 5mA$
    4. Global design constraints outlined in the manual
2. Efficiency
    1. Dropout voltage $V_{DO} = V_O - V_I$
    2. Quiescent Current $I_Q = I_O - I_I < 200\mu A$
    3. Efficiency $\eta = (V_O I_O)/\{V_I(I_I + I_Q)\}$
3. Noise Rejection and Isolation: Power Supply Rejection

$$PSRR_{DB} = 20\log\frac{\Delta V_O}{\Delta V_I}\begin{cases} < -55dB\ @10kHz \\ < -25dB\ @25kHz \end{cases}$$

4. Transient Response and Linearity
    1. Line regulation $\Delta V_O/\Delta V_I < 1mV/V$
    2. Load regulation $\Delta V_O/\Delta I_O < 1mV/mA$
    3. Temperature regulation $\Delta V_O/\Delta T < 1mV/℃$
    4. Recovery/ Settling Time $t_{s,90\%} < 1\mu s$
    5. Overshoot/Undershoot $V_{max} - V_o < 25mV, V_o - V_{min} < 25mV$

Literature Review: Previously published LDOs

To facilitate a comparison of regulators with different specifications, a figure of merit (FoM) has been used below. The smaller the FoM, the better the regulator.

$$FoM = t_r\frac{I_Q}{I_{O,Max}}$$

	LDO with Ultra-Fast Load Regulation	**Capacitor Free LDO with DFC**	**High PSRR LDO for RF SoC**	**Low Quiescent Current LDO**	**Cascoded OTA LDO**
PSRR (dB)	-16dB @ High Freq	< -30 @1MHz	<-65 @20kHz	-	-34.31 @10kHz
$I_{O,Max}$ (mA)	100	100	150	50	450
No-load I_Q (µA)	6000	38	160	23	50
Worst Load Regulation (mV/mA)	0.65	0.007	17.4	0.380	0.012
Line regulation (mV/V)	-	<3.75 @1.5V	1.5 @2.8V	1.05 @3.8V	3.2 @4.5V
Response time t_s (µs)	0.00054	2	2.5*	5	6
Area (mm²)	0.008	0.0003	0.166	0.0014	-
FoM (ns)	0.03	0.76	2.67	2.30	0.67
Summary	Fast load regulation. Poor quiescent performance	Good quiescent performance and PSRR.	Excellent PSRR. Poor load regulation.	Good quiescent performance. Poor load regulation.	Good PSRR. Poor load regulation.

*Extrapolated from measured load slew rate

Initial Design Considerations

Feedback Loop Compensation Techniques

Compensation must be considered to stabilise response due to high impedance poles at the input of the EA differential pair and PE output.

1) R_{ESR}: Introduces zero to compensate high output impedance pole.

2) Miller Compensation between V_G and V_O: Pushes apart dominant of the 2 nodes and increases phase margin. However, a large capacitor is needed, and at high frequencies, it couples the output with V_I (V_{DD}) and reduces the PSRR. The reduced slew rate is also reduced which slows load regulation

3) Cascode Feedback Compensation: By adding a current buffer to the miller capacitor, this eliminates the feedforward path. The compensation capacitance to be reduced, which increases the maximum slew rate and the bandwidth.

4) DFC Compensation: Similarly, a smaller compensation capacitance and PE is required, which increases slew rate. However it only controls the imaginary part of the pole to prevent overdamping, which has little impact on settling time.

Pass Element (PE) Pros and Cons

PE	Pros	Cons
Common-Drain (CD) NMOS	Low output impedance at high current and high frequency	A charge-pump is required to charge V_G beyond V_I, to operate it in saturation.
Common-source (CS) PMOS	Given $V_G < V_I$, device is in saturation, so gain is higher and voltage drop is lower.	Low-frequency, dominant poles associated with the gate and output of the PE, which requires compensation for stability.
Native NMOS	Weaker p-doped bulk means threshold voltage is zero, which avoids the need for a charge-pump.	Small transconductance, so a larger area required to achieve same conductivity.

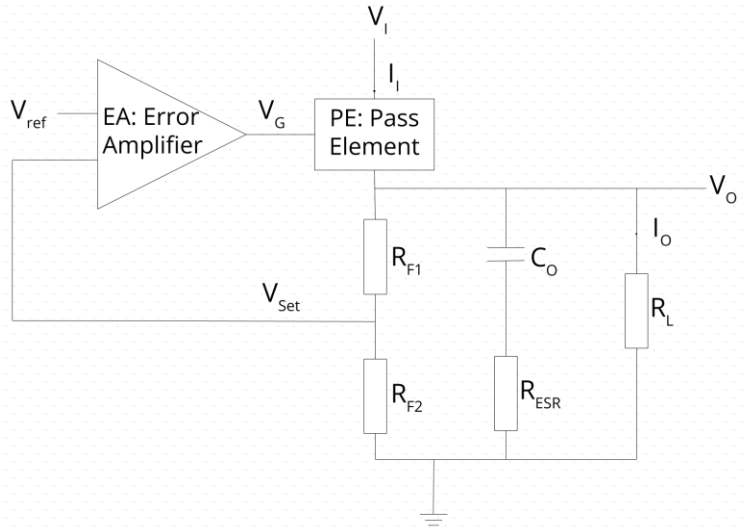
Error Amplifier (EA)/ OTA Considerations

1) Input: for V_O to track V_{ref}, wide bandwidth is not necessary, but high gain improves rejection of noise from V_{Set}

2) Output: requires a wide bandwidth for fast load regulation. High output swing is also desired for PE to operate in saturation.

EA + Pass Element Combinations

EA	PE	Gate of PE coupled to V_I?	$\Delta v_O/\Delta v_I$	PSRR
NMOS	PMOS	Yes. Gate behaves as resistive divider.	$R_L/(r_{ds}+R_L)$	High
NMOS	NMOS	No. Gate behaves as common gate stage.	$g_m(r_{ds}\|\|R_L)$	Low
PMOS	PMOS	No. Gate behaves as cascode.	$1/(g_m v_{ds})$	Low
PMOS	NMOS	Yes. Gate behaves as source follower.	≈ 1	High



Design Details

OTA and feedback loop design

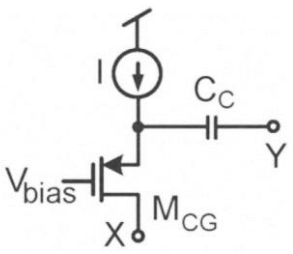
1) Differential pair and CS Amplifier
    1) Biased with PTAT: to source or sink current
    2) Option: Cascode to increase transconductance and bandwidth, at the cost of increased quiescent current, and reduced input and output swing (which will not affect performance as feedback ratio is fixed during operation)
2) Cascode (Ahuja) Compensation:
    1) Acts as a current buffer to the miller capacitor and eliminates the feedforward path.
    2) Reduces capacitance to be reduced, which increases the maximum slew rate and the bandwidth.
    3) Bandwidth determined by dominate outputpole $GBW = \frac{g_m}{C_C}$

Pass Element (PE): Common Source PMOS

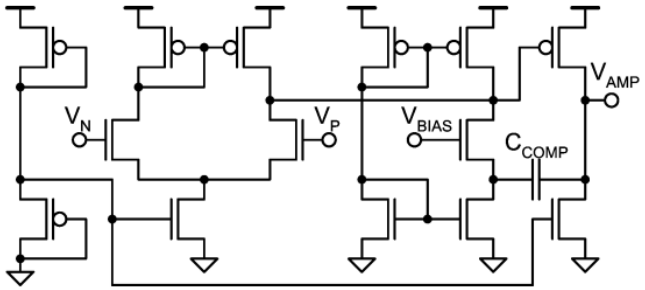
Despite the dominant pole associated with the large output impedance of a CS PMOS, this avoids a charge pump and its quiescent current.

Digital power-down and programmable V_O

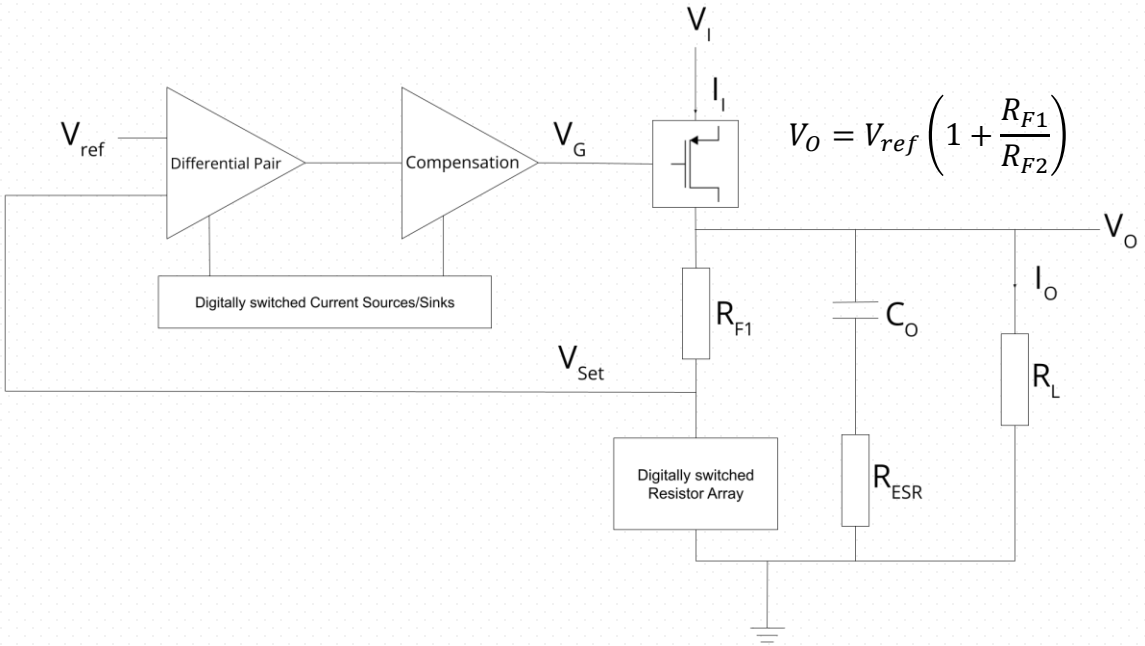
1) Digitally controlled PTAT/ Current Sinks: This halts the quiescent current in the event of a power-down signal.
2) NMOS for feedback resistors to program V_O



Cascode compensation Illustration



Implementation of 2-stage op-amp with cascode compensation



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