

**Birkbeck
(University of London)**

MSc Examination

Department of Computer Science and Information Systems

COMPUTER SYSTEMS (COIY060H7)

CREDIT VALUE: 15 credits

Date of examination: Thursday, 7th June 2012

Duration of paper: 14:30–16:30

There are five questions in this paper; each of them is compulsory and worth 20 marks.
The paper is not prior-disclosed.
The use of electronic calculators is not permitted.

1. (a) List the most important registers on the CPU and briefly explain their functions. (7 marks)
 - (b) Explain how the CPU is connected to main memory. (3 marks)
 - (c) Describe in detail the data flow between the CPU and main memory during the fetch, indirect and interrupt cycles. (10 marks)

 2. (a) Briefly describe the compiler-based register optimization technique (typically used for RISC machines). (4 marks)
 - (b) Describe the delayed branch technique and explain why it is more common in RISC machines than in superscalar processors. (4 marks)
 - (c) Show the pipeline activity for the following code fragment with and without applying the delayed branch technique. Assume that there are three pipeline stages (fetch-decode, address calculation, data movement) for load and store instructions and two stages (fetch-decode, execute) for ALU instructions.

Address	Instruction	Comment
100	LOAD RA,X	X -> RA
101	LOAD RB,Y	
102	ADD RA,RB	RA + RB -> RA
103	JUMP 106	
104	ADD RB,1	
105	STORE Y,RB	RB -> Y
106	STORE X,RA	
- (10 marks)
- (d) Assume that, before the execution of the code, memory locations X and Y contain 1 and 2, respectively. What are their respective values after the execution of the code with and without applying the delayed branch technique? (2 marks)
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3. (a) Explain the benefits of the virtual memory technique. (5 marks)
 - (b) What addressing modes are suitable for a computer system that uses paging? (5 marks)
 - (c) Consider a (RISC) machine that uses 4KB pages and 4-byte instructions, and assume that a process switch just occurred. If the referenced instruction is on the hard disk, it takes 100 ms to load into main memory. The initial probability (after a process switch) that a referenced instruction is in main memory is 0.4. How many milliseconds does it take to load the first referenced instruction into the IR on average? How many milliseconds does it take to load the second instruction on average? You can assume that the first instruction referenced is not a jump and that the time accessing main memory is negligible compared to accessing the hard disk. (10 marks)

4. (a) Explain the benefits of multithreaded processes. (5 marks)
- (b) Describe two ways in which multithreaded processes can be implemented and compare their benefits. (5 marks)
- (c) Consider the following file server. It takes 20 ms to fetch the requested file if it is in the (disk) cache. If a disk operation is needed, as is the case for one-third of the requests, an additional 80 ms is needed. Compute how many requests/sec the server can handle if it is single threaded. How does this change when the server is multithreaded? (10 marks)
5. (a) Compare the benefits of Peterson's solution to the mutual exclusion problem as against solutions using semaphores. (5 marks)
- (b) Explain what the priority inversion problem is. Suggest a way in which modern operating systems can handle it. (5 marks)
- (c) The *exchange* machine instruction is defined as follows:

```
void exchange (int register, int memory)
{
    int temp;
    temp = memory;
    memory = register;
    register = temp;
}
```

It is assumed that it is implemented as an atomic instruction. Describe how exchange can be used to achieve mutual exclusion for n processes (e.g. by writing a mutual exclusion procedure using pseudo-code). Explain whether your solution avoids busy waiting. (10 marks)