Example — Immediate Addressing

Consider the computation $(((10 * 8) + 4) - 7)^2$.

1. Write an assembly program for the above computation by using a minimal number of registers.

2. Draw a diagram showing the in-order execution of the code on a five-stage pipeline and identify the delay slots. Assume that when an instruction cannot be further processed (e.g., because of some dependency or resource conflict), then it stalls the pipeline.

3. Now assume that there is an *instruction window* IW, where fetched and decoded instructions can be stored before further processing (so that the pipeline does not have to stall). In addition, allow an instructions to "jump the queue" (out-of-order execution), provided that this does not alter the outcome of the computation. Draw a diagram showing the execution of the code and identify the delay slots.

Solution to Example — Immediate Addressing

1. Here is the code:

```
I1  LOAD r1, #10
I2  LOAD r2, #8
I3  MUL  r1, r2
I4  LOAD r2, #4
I5  ADD r1, r2
I6  LOAD r2, #7
I7  SUB r1, r2
I8  MUL r1, r1
```

2. Here is the diagram showing delay slots (empty pipeline stages):

	IF	ID	RR	EX	WB	Comments
1	I1					
2	I2	I1				
3	I3	I2			I1	I1 skips RR,EX
4	I4	I3			I2	I2 skips RR,EX
5	I5	I4	I3			
6	I5	I4		I3		I4 skips RR,EX
7	I5	I4			I3	
8	I6	I5			I4	
9	I7	I6	I5			
10	I7	I6		I5		I6 skips RR,EX
11	I7	I6			I5	
12	I8	I7			I6	r2 not ready
13		I8	I7			
14		I8		I7		r1 not ready
15		I8			I7	
16			I8			
17				I8		
18					I8	

3. We insert a new column IW showing the decoded instructions waiting for further processing. Instructions which "jump the queue" are in boldface.

	IF	ID	IW	RR	EX	WB	Comments
1	I1						
2	I2	I1					
3	I3	I2				I1	I1 skips RR,EX
4	I4	I3				I2	I2 skips RR,EX
5	I5	I4		I3			
6	I6	I5			I3	**I4**	I4 skips RR,EX
7	I7	I6	I5			I3	r1 not ready
8	I8	I7	I6	I5			r2 in use
9		I8	I7		I5	**I6**	I6 skips RR,EX, r1,r2 not ready
10			I8,I7			I5	r1 not ready
11			I8	I7			
12			I8		I7		
13			I8			I7	
14				I8			
15					I8		
16						I8	

In cycle 6, I4 can go to WB, since I3 already read r2 in cycle 5. In cycle 9, I6 can go to WB, since I5 already read r2 in cycle 8.