

# 電子電路設計模擬與實習

實驗名稱：數位電路

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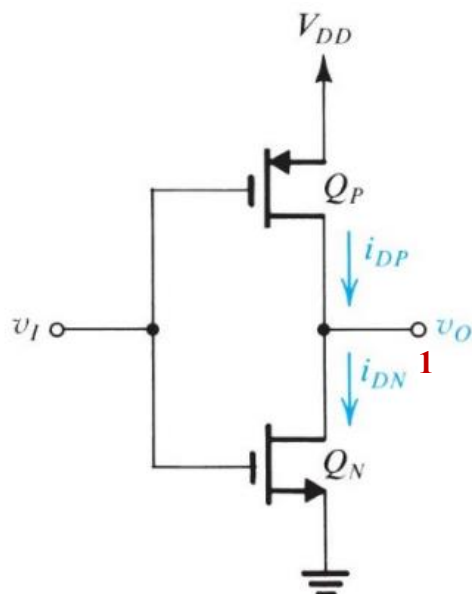
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## 10. CMOS 主動負載差動放大器設計

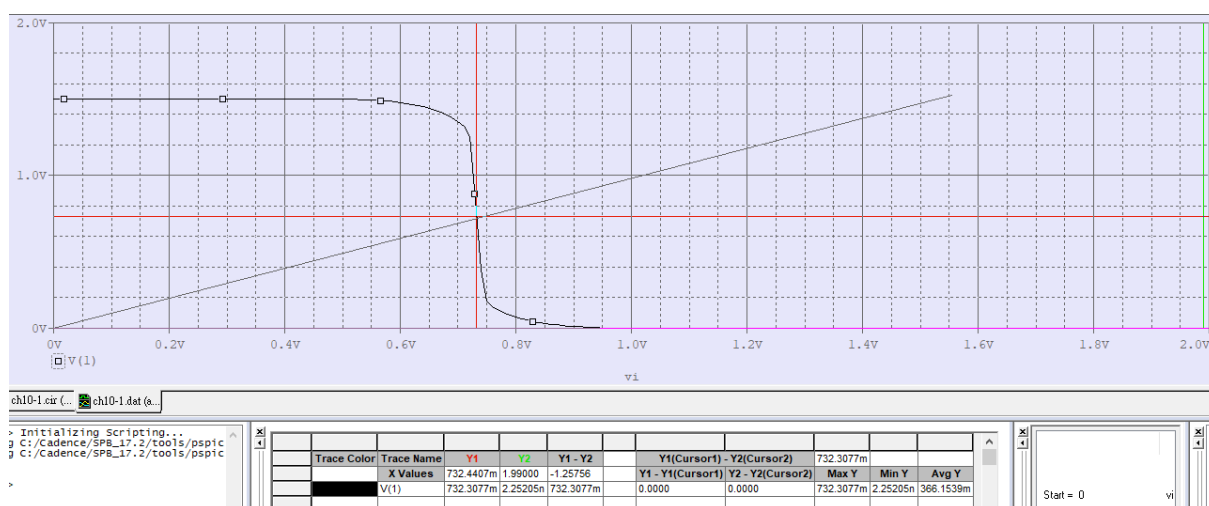
### Lab 10-1. CMOS 反向器 VTC 曲線模擬及靜態參數萃取

實驗電路圖：

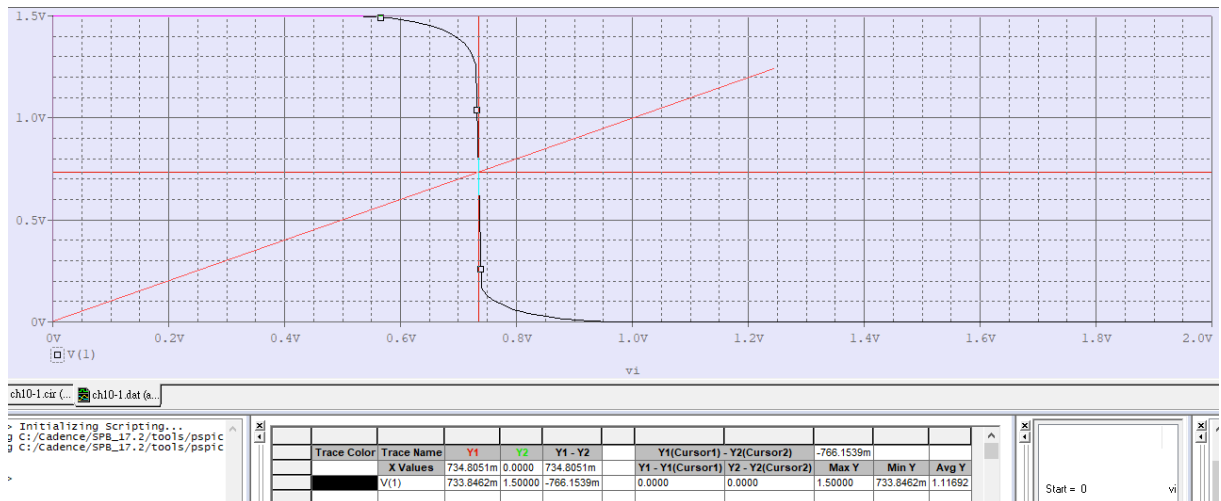


1. 模擬不同  $\lambda$  (0.2、0.02、0.002) 下之 VTC 曲線。

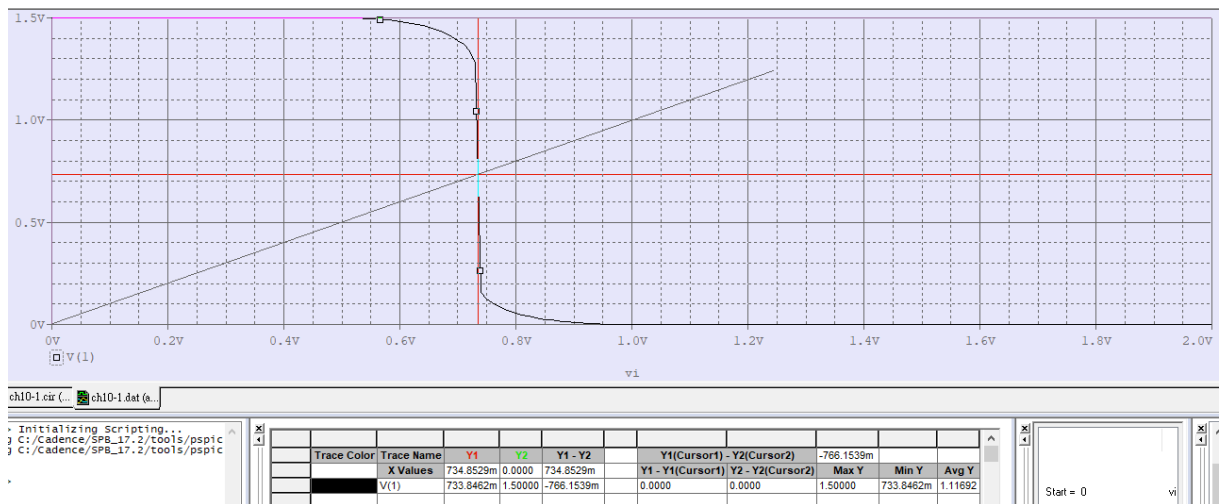
	$\lambda$		
	0.2	0.02	0.002
$V_M$	732.4407m	734.8051m	734.8529m
$g$	-46.1856	-11.1404	-8.00048



$\lambda = 0.2$



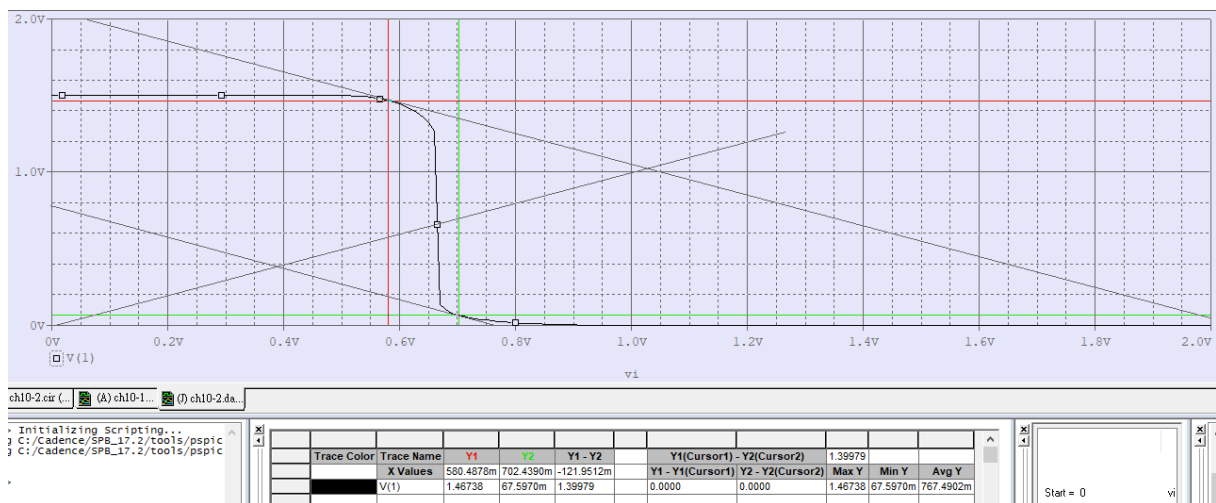
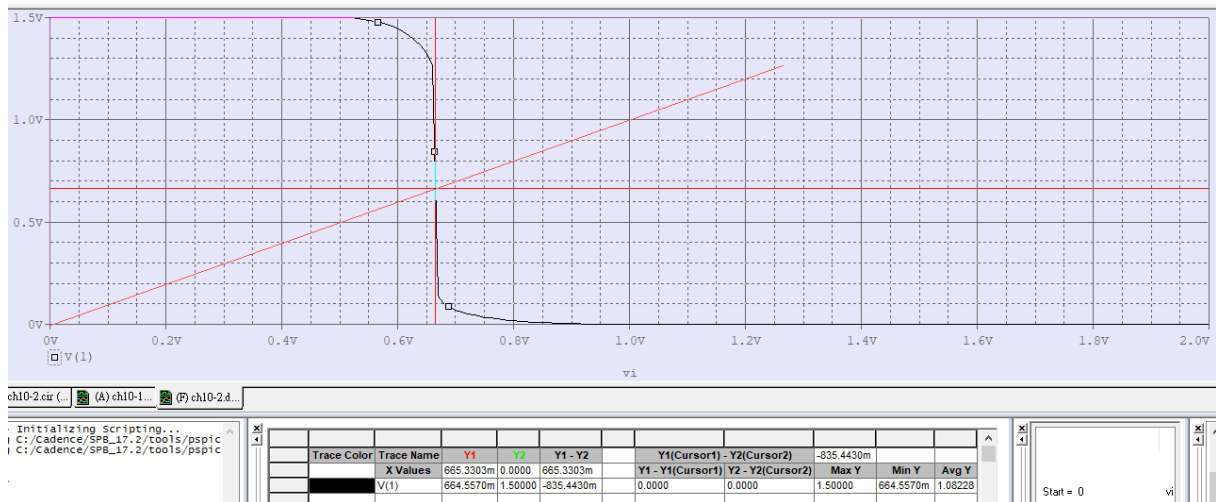
$\lambda = 0.02$



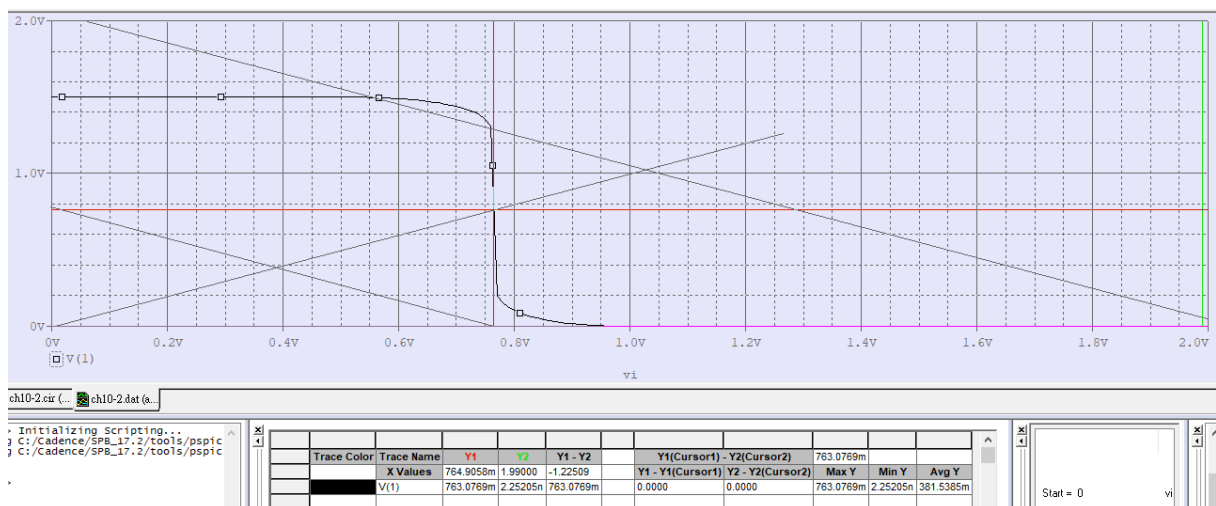
$\lambda = 0.002$

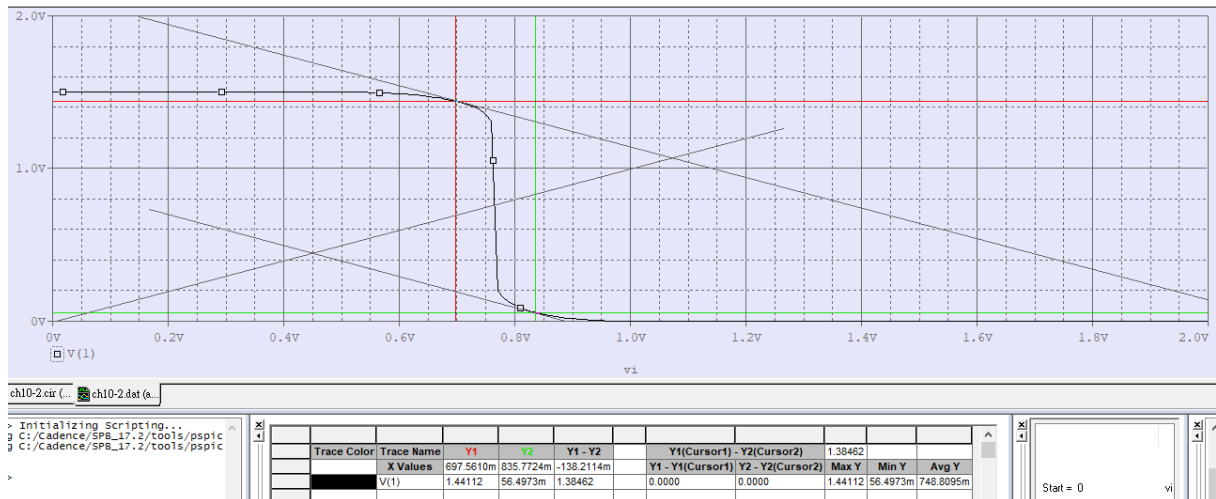
2. 模擬 PMOS、NMOS W/L 的尺寸比變動對反向器 VTC 曲線的影響。

靜態變數	PMOS-to-NMOS ration		
	1	5	11
$V_M$	665.3303m	764.9058m	814.6295m
$g$	-33.3033	-406.699	-14.613
$V_{IL}$	580.4878m	697.561m	773.9837m
$V_{IH}$	702.439m	835.7724m	881.3008m
$V_{OL}$	0	0	0
$V_{OH}$	1.5	1.5	1.5
$NM_L$	797.561m	664.2276m	618.6992m
$NM_H$	580.4878m	697.561m	773.9837m

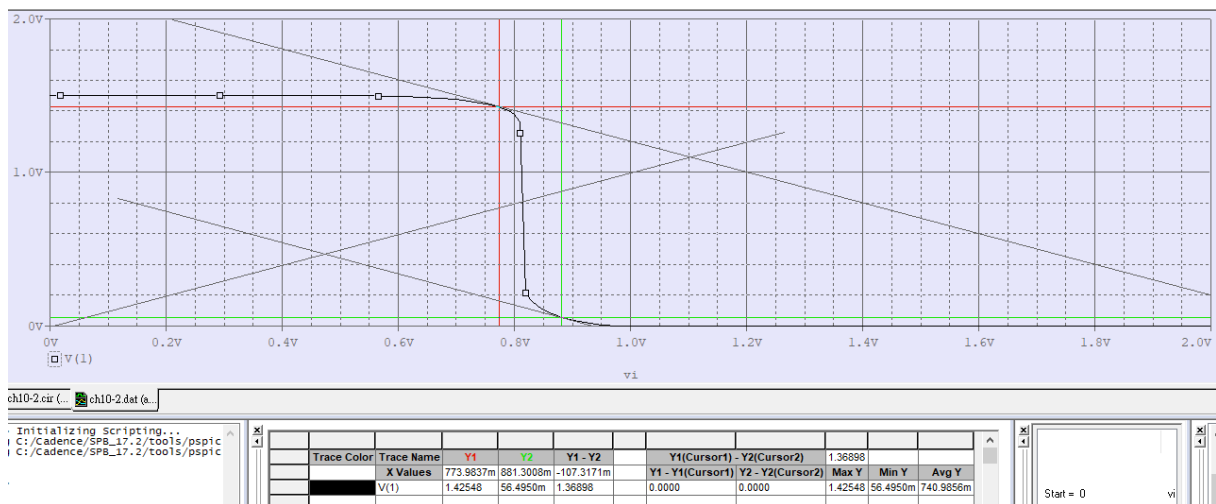
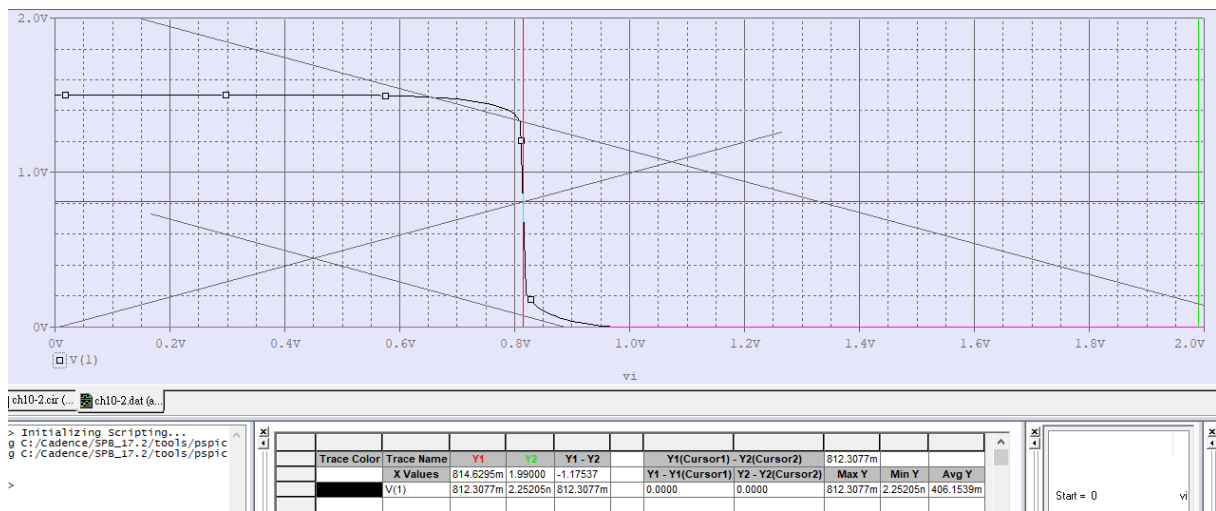


**PMOS-to-NMOS ratio = 1**





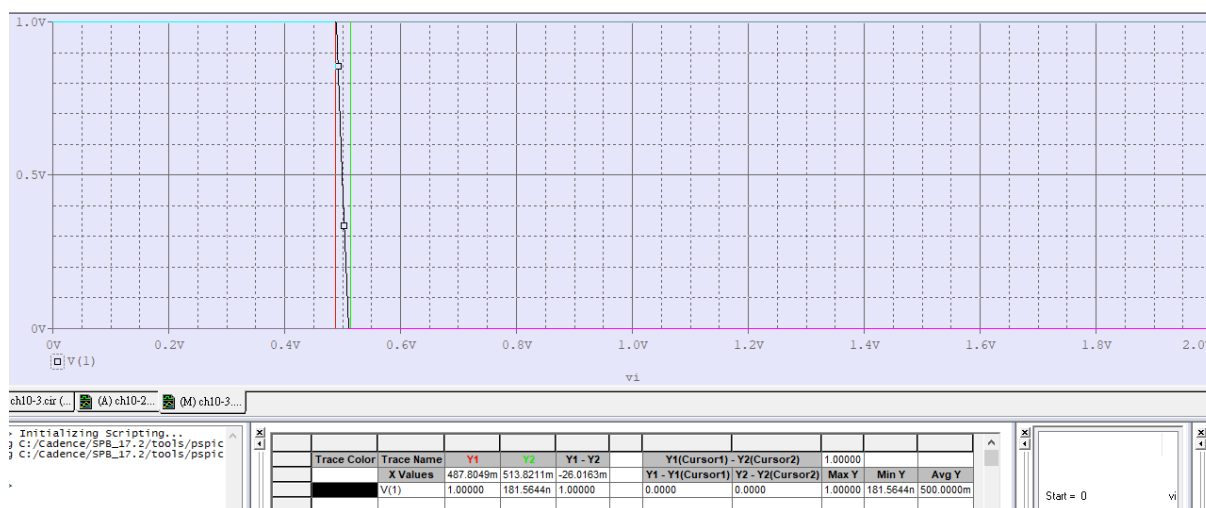
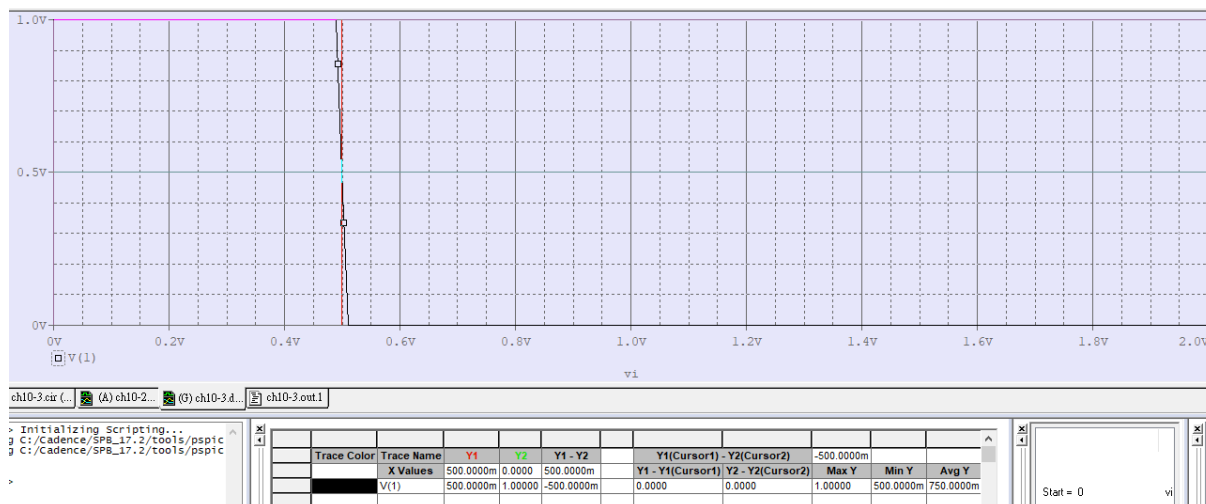
**PMOS-to-NMOS ratio = 5**



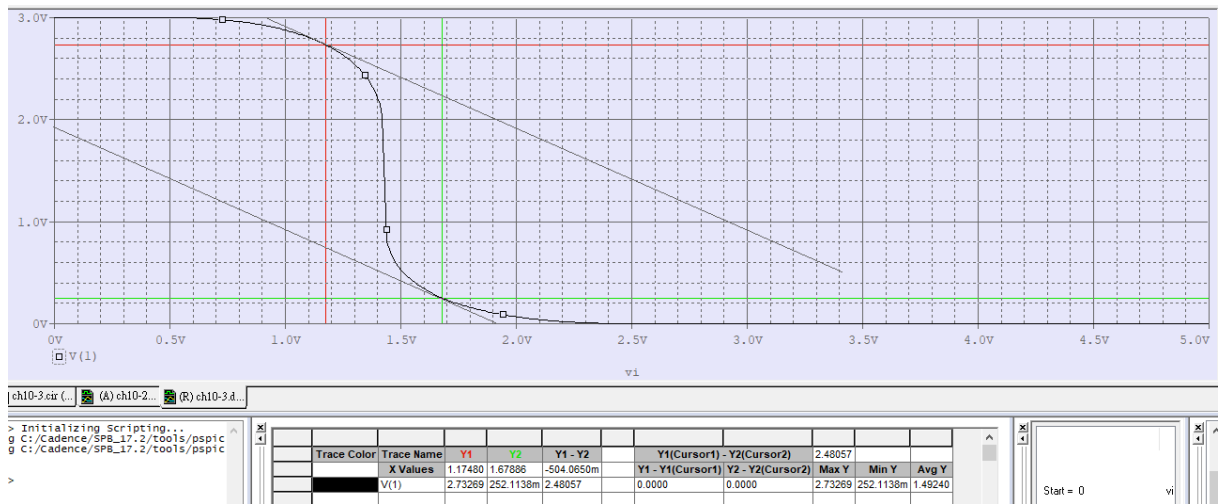
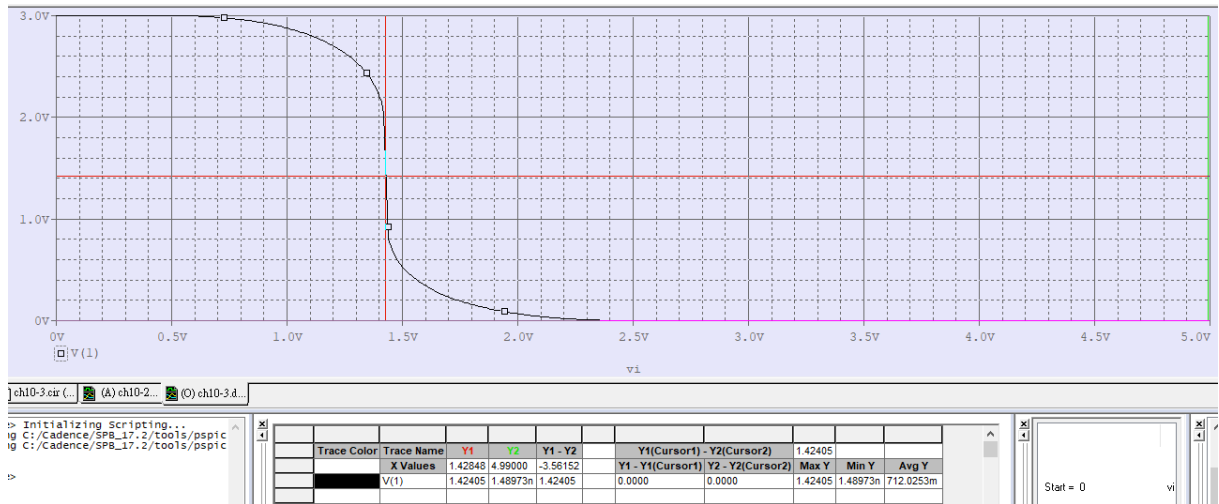
**PMOS-to-NMOS ratio = 11**

3. 模擬電源電壓  $V_{DD}$  變動對反向器 VTC 曲線的影響。

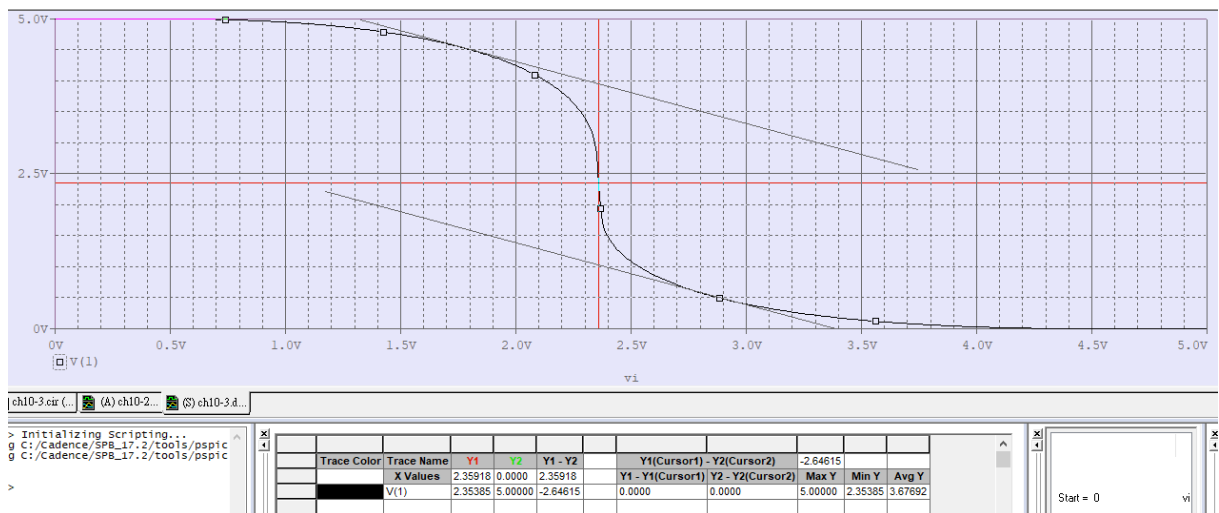
靜態變數	$V_{DD}$		
	1	3	5
$V_M$	0.5	1.42848	2.35918
$g$	0	-103.479	-52.6367
$V_{IL}$	487.8049m	1.17480	1.83058
$V_{IH}$	513.8211m	1.67886	2.85950
$V_{OL}$	0	0	0
$V_{OH}$	1	3	5
$NM_L$	486.1789m	1.32114	2.14050
$NM_H$	487.8049m	1.17480	1.83058

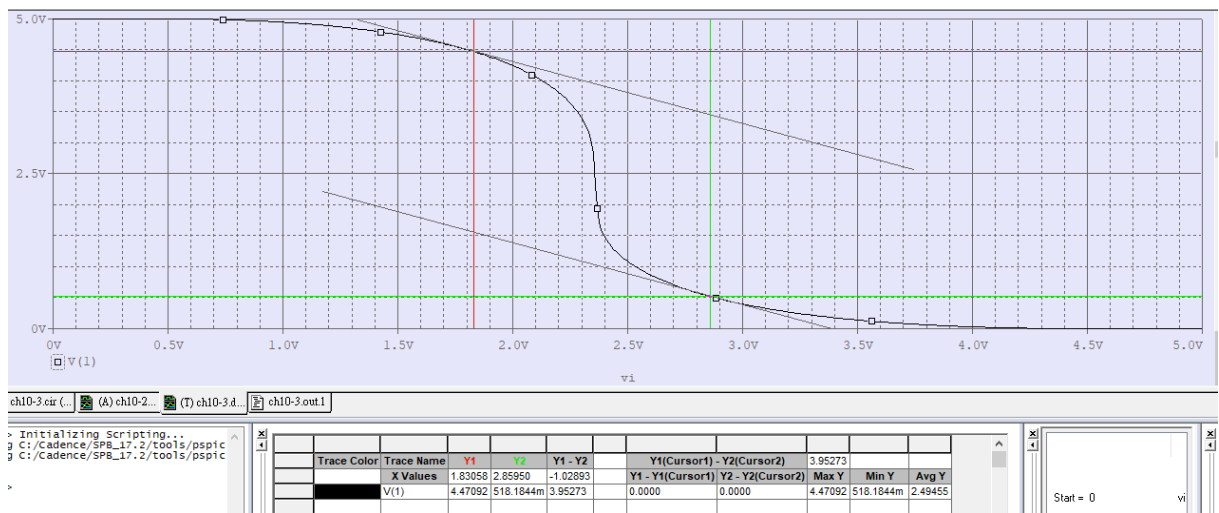


$V_{DD} = 1$



$V_{DD} = 3$





$$V_{DD} = 5$$