

電子電路設計模擬與實習

實驗名稱：CMOS 反向器延遲時間分析

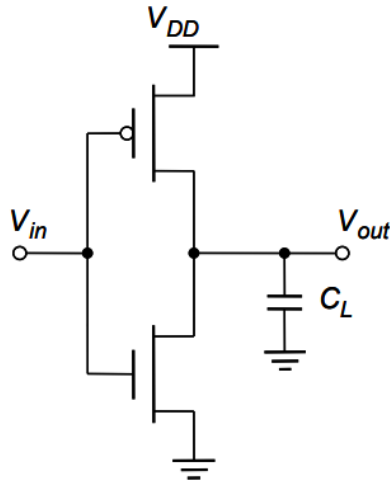
班級：電子二乙

組員：U0922113 郭晏寧

U0922107 張志斌

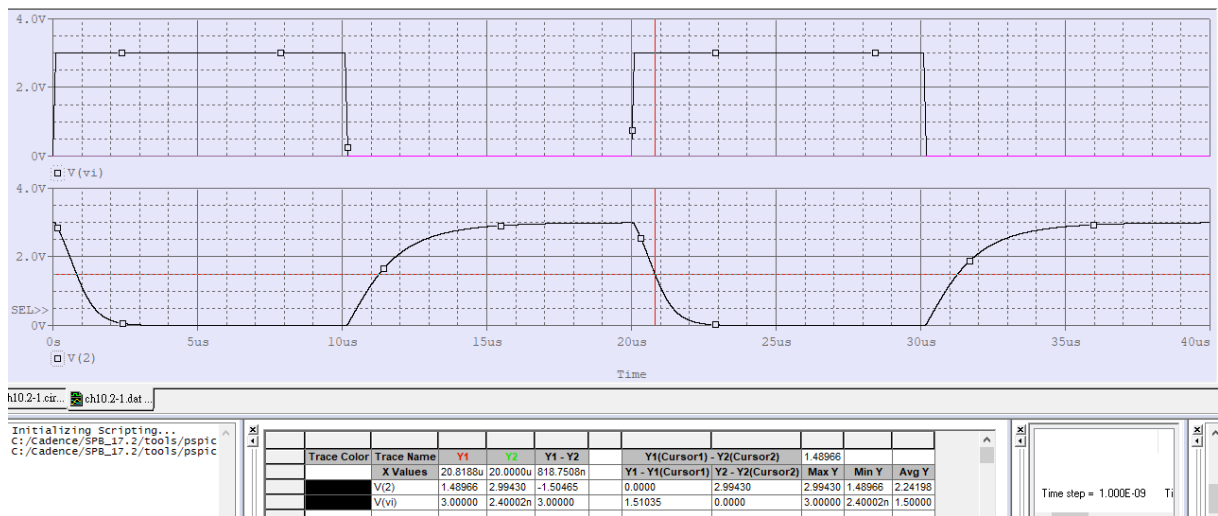
Lab 10-2. CMOS 反向器延遲時間分析

實驗電路圖：

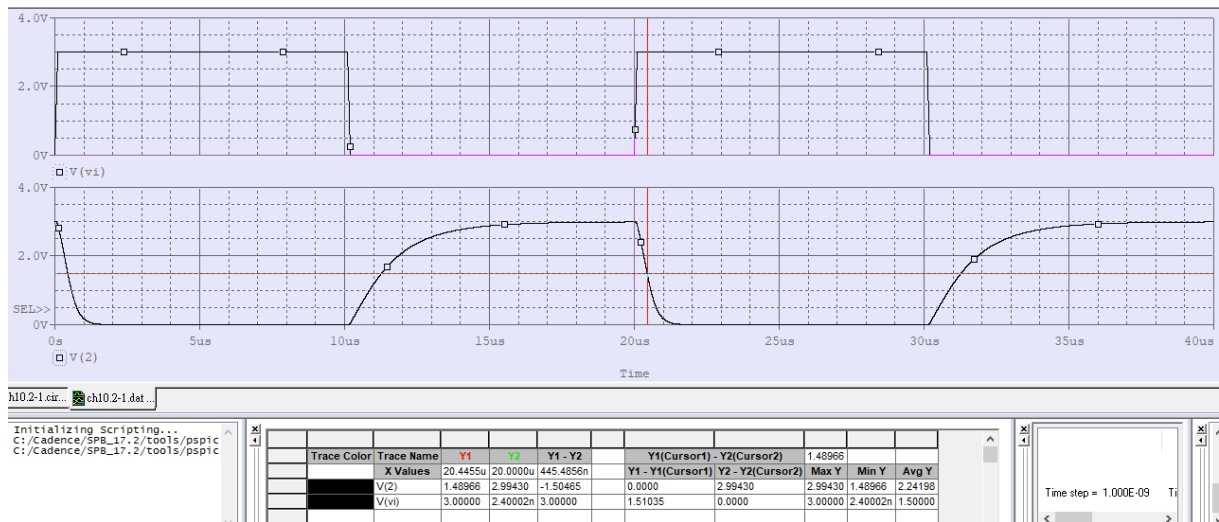


1. NMOS W/L 尺寸與 t_{pHL} 之關係

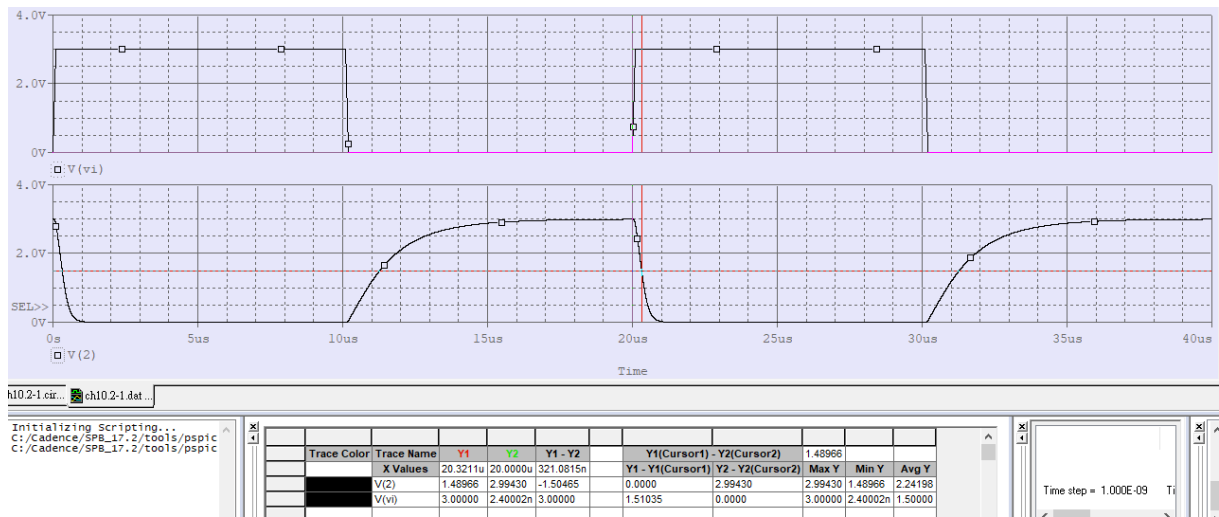
t_{pHL}	NMOS W/L ($L=0.18\mu\text{m}$)		
	1.5	3	4.5
PMOS W/L=3	0.8188μ	0.4455μ	0.3211μ



NMOS W/L = 1.5



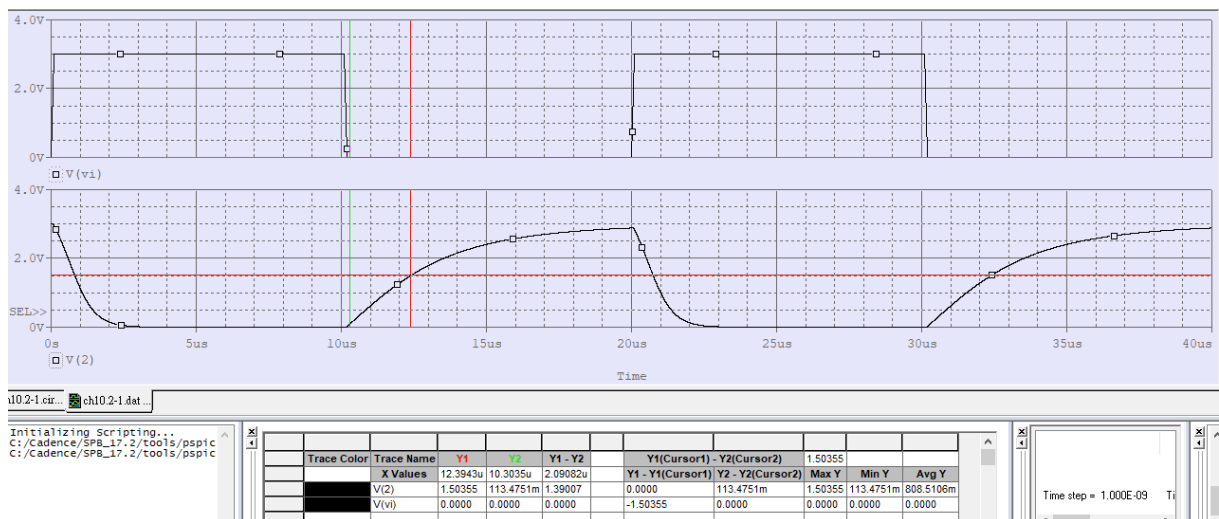
NMOS W/L = 3



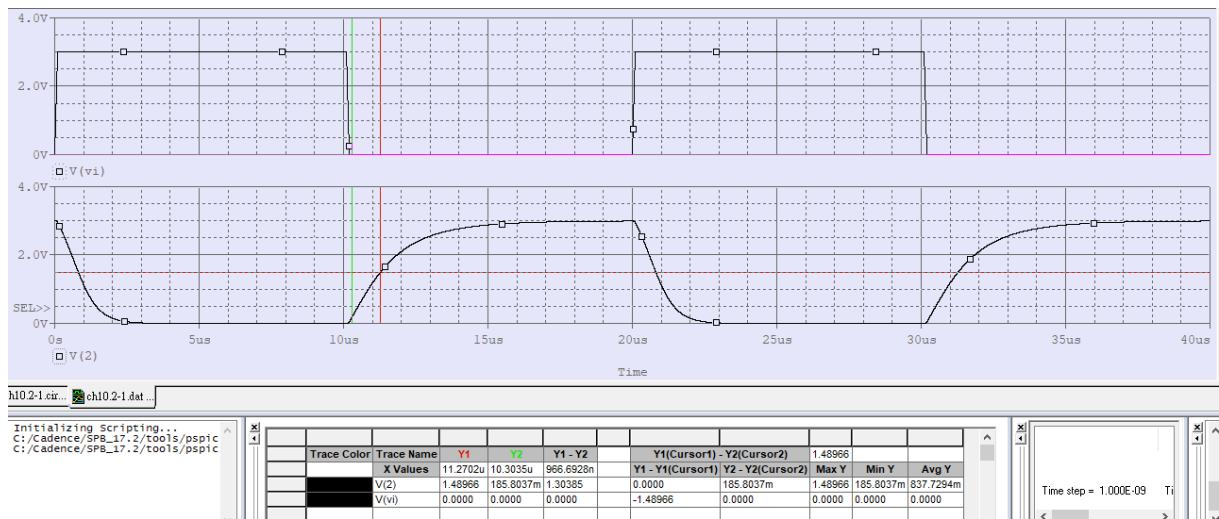
NMOS W/L = 4.5

2. PMOS W/L 尺寸與 t_{pLH} 之關係

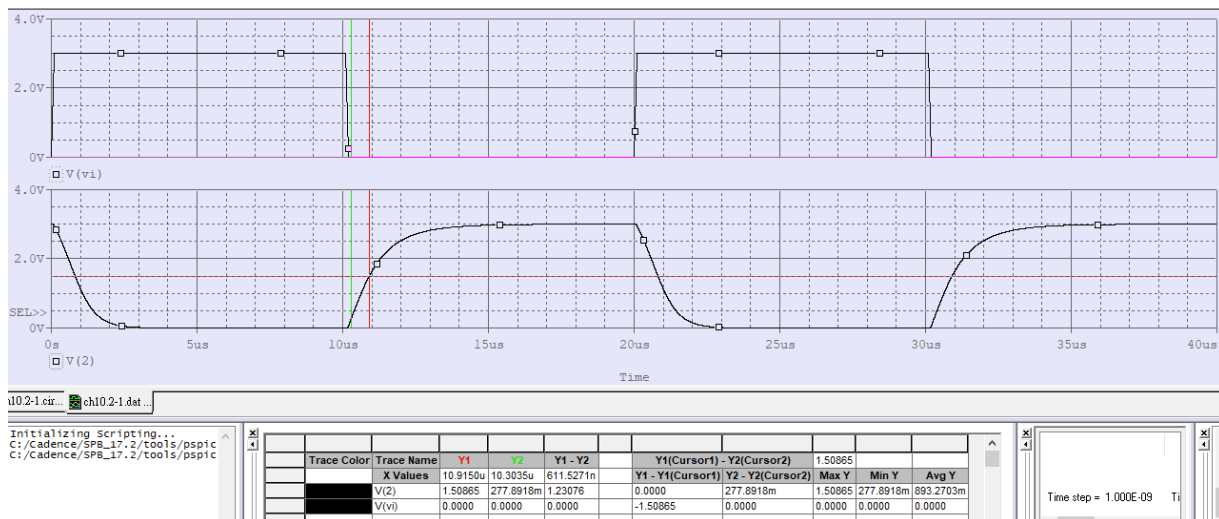
t_{pLH}	PMOS W/L (L=0.18um)		
	1.5	3	4.5
PMOS W/L=3	2.0908μ	0.9667μ	0.6115μ



PMOS W/L = 1.5



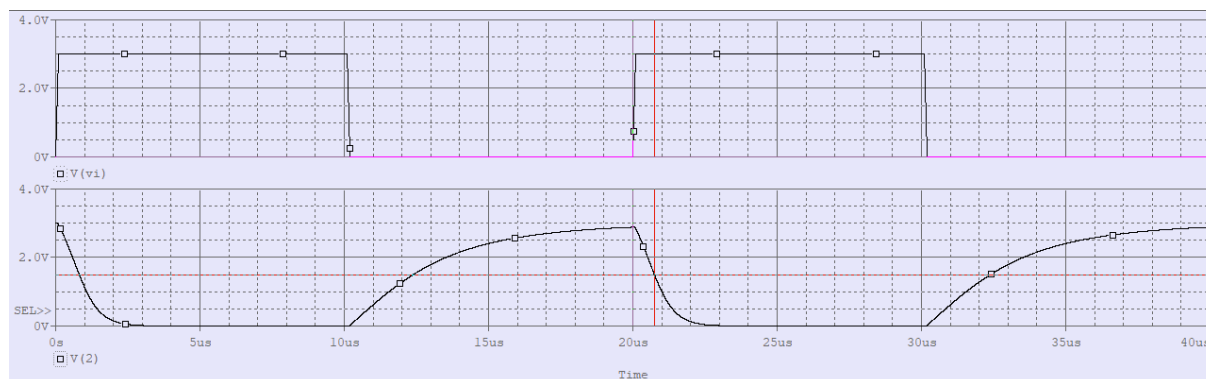
PMOS W/L = 3



PMOS W/L = 4.5

3. PMOS、NMOS W/L 的尺寸比(PMOS-to-NMOS ratio)與 t_{pHL} 、 t_{pLH} 之關係

	PMOS-to-NMOS ratio (L=0.18um)				
	1	2	3	4	5
t_{pHL}	0.7535 μ	0.8188 μ	0.8221 μ	0.8223 μ	0.8223 μ
t_{pLH}	2.1067 μ	1.0457 μ	0.6862 μ	0.4925 μ	0.35 μ

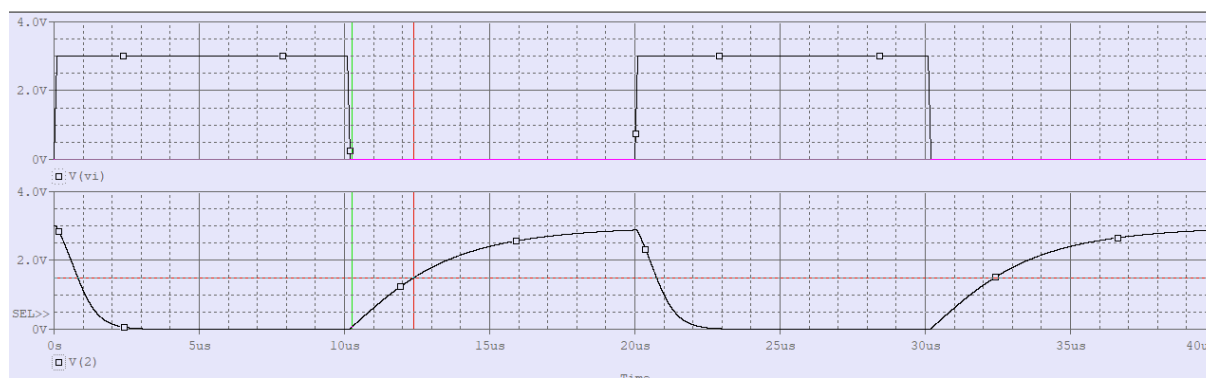


h102-1.cir... ch102-1.dat...

Initializing Scripting...
C:/Cadence/SPB_17.2/tools/pspic
C:/Cadence/SPB_17.2/tools/pspic

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	Max Y	Min Y	Avg Y
	X Values	20.7535u	20.0000u	753.5278n				
	V(2)	1.48966	2.88551	-1.39586	0.0000	2.88551	1.48966	2.18758
	V(v1)	3.00000	2.40002n	3.00000	1.51035	3.00000	2.40002n	1.50000

Time step = 1.000E-09



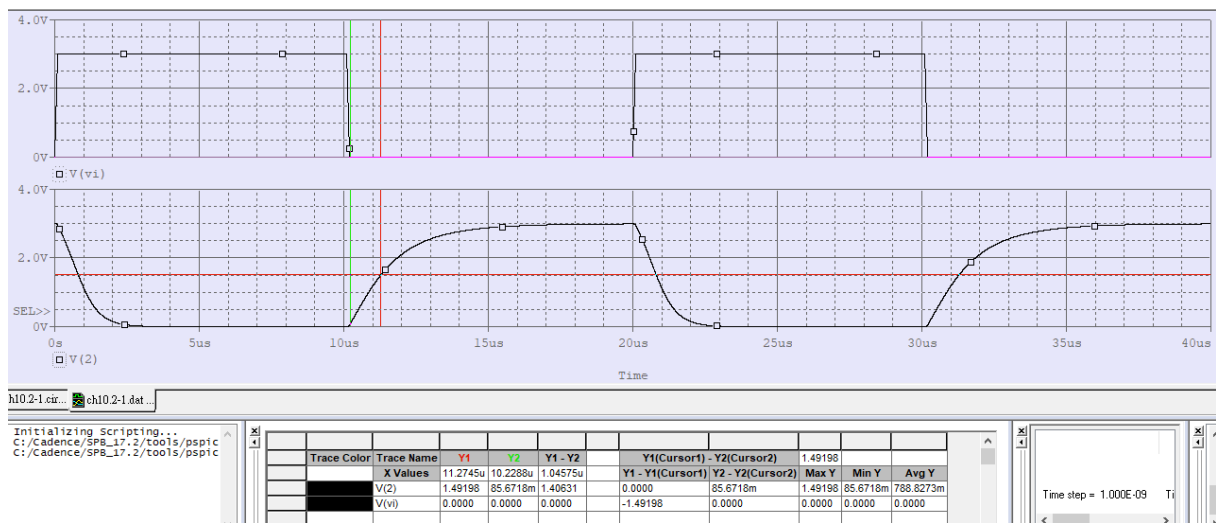
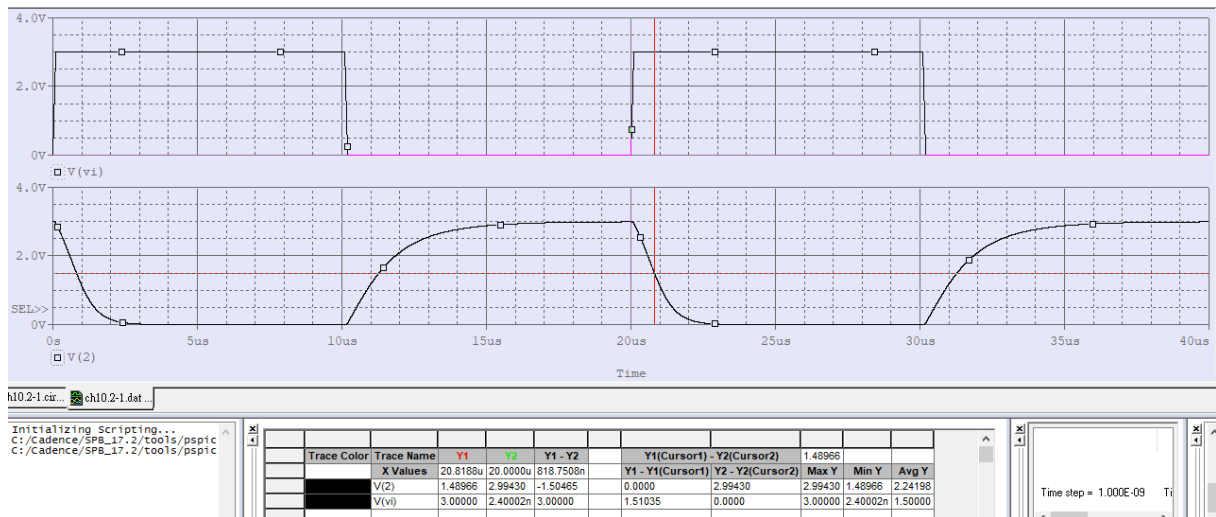
h102-1.cir... ch102-1.dat...

Initializing Scripting...
C:/Cadence/SPB_17.2/tools/pspic
C:/Cadence/SPB_17.2/tools/pspic

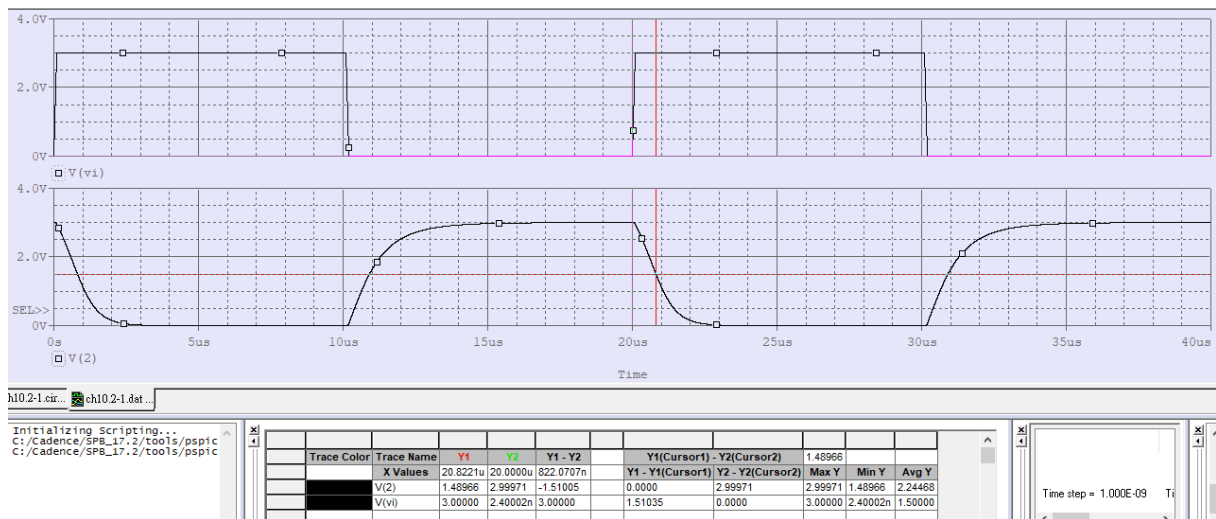
Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	Max Y	Min Y	Avg Y
	X Values	12.3681u	10.2614u	2.1067u				
	V(2)	1.48966	68.0182m	1.42164	0.0000	68.0182m	1.48966	68.0182m
	V(v1)	0.0000	0.0000	0.0000	-1.48966	0.0000	0.0000	0.0000

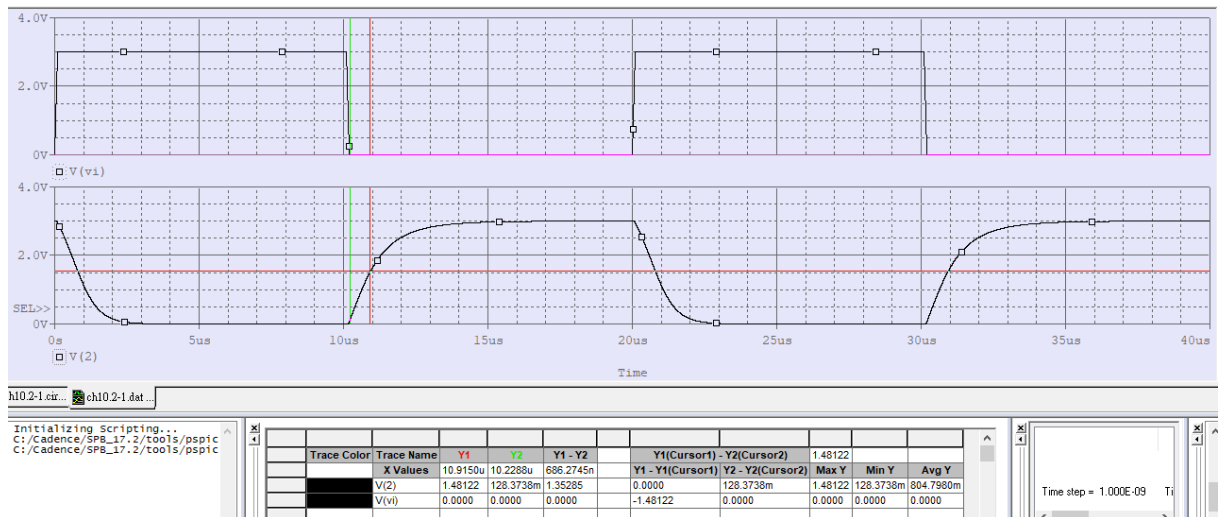
Time step = 1.000E-09

PMOS-to-NMOS ratio = 1

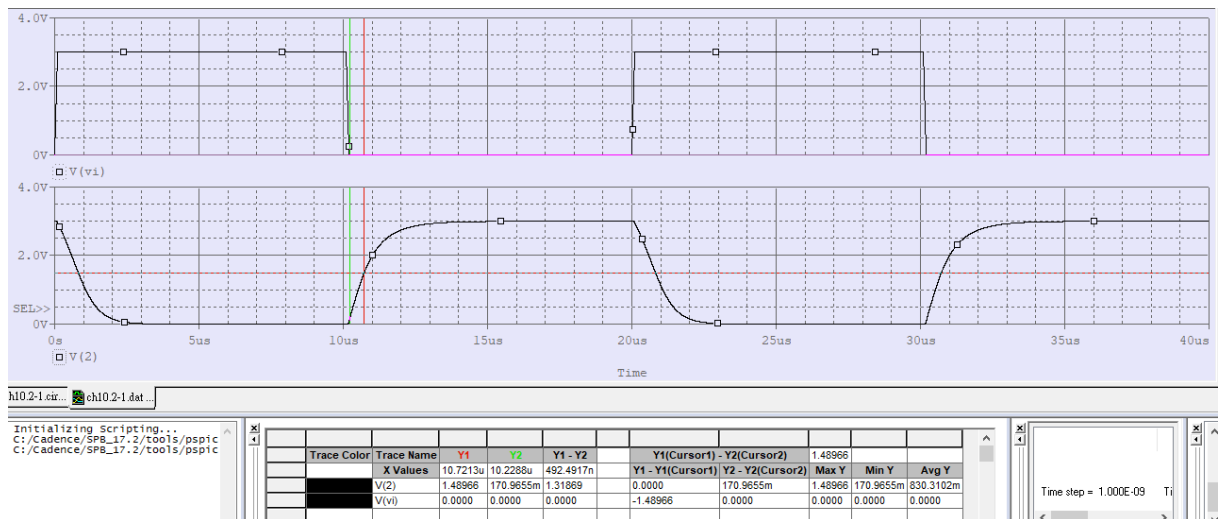
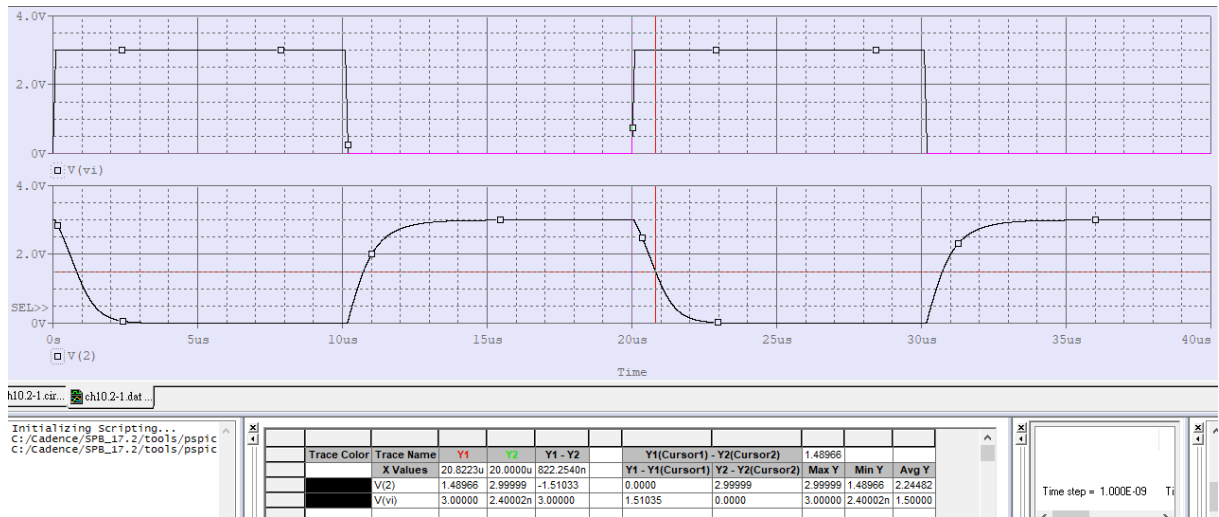


PMOS-to-NMOS ration = 2

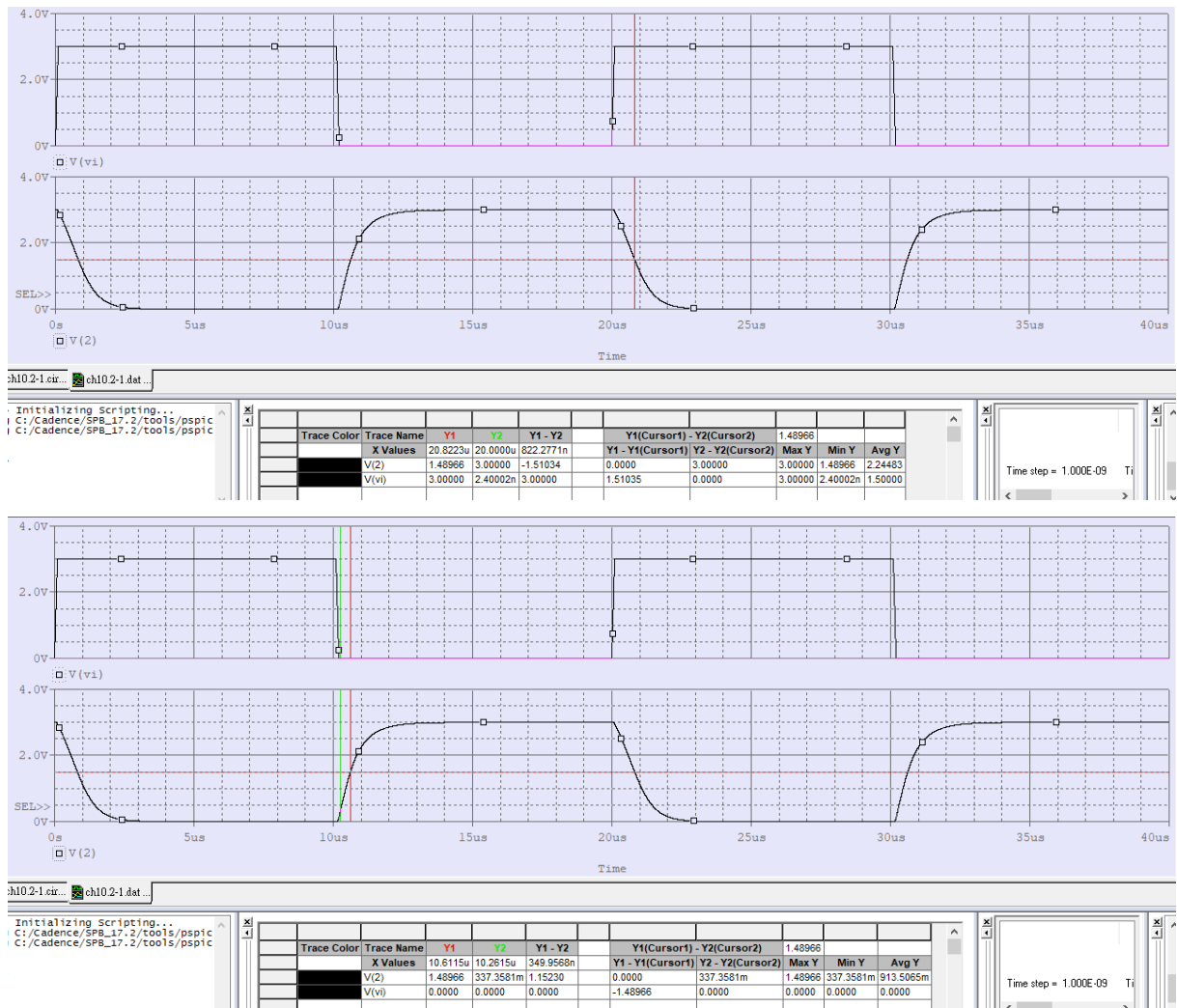




PMOS-to-NMOS ratio = 3



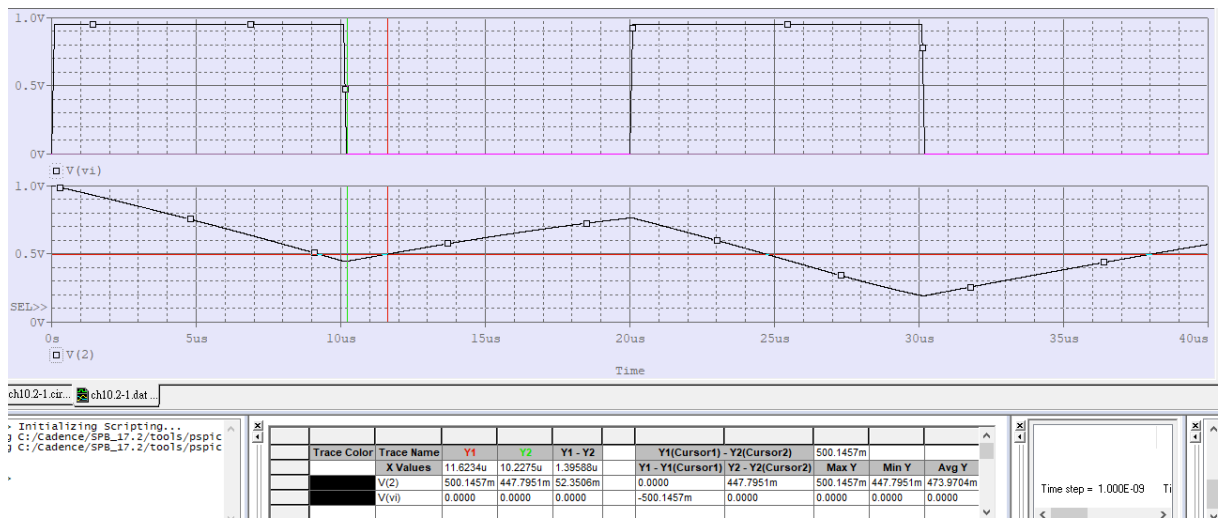
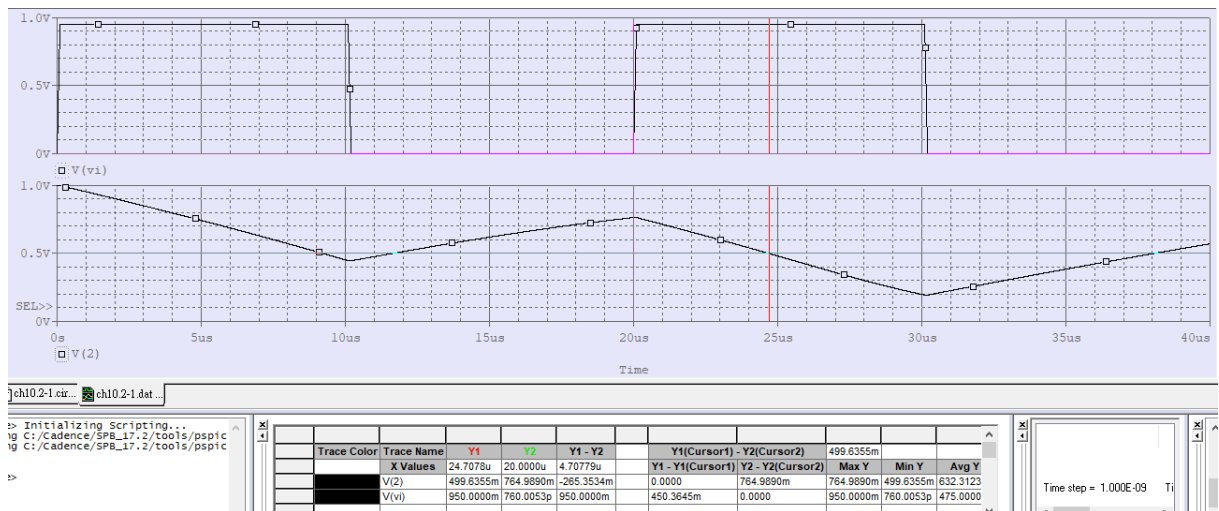
PMOS-to-NMOS ratio = 4



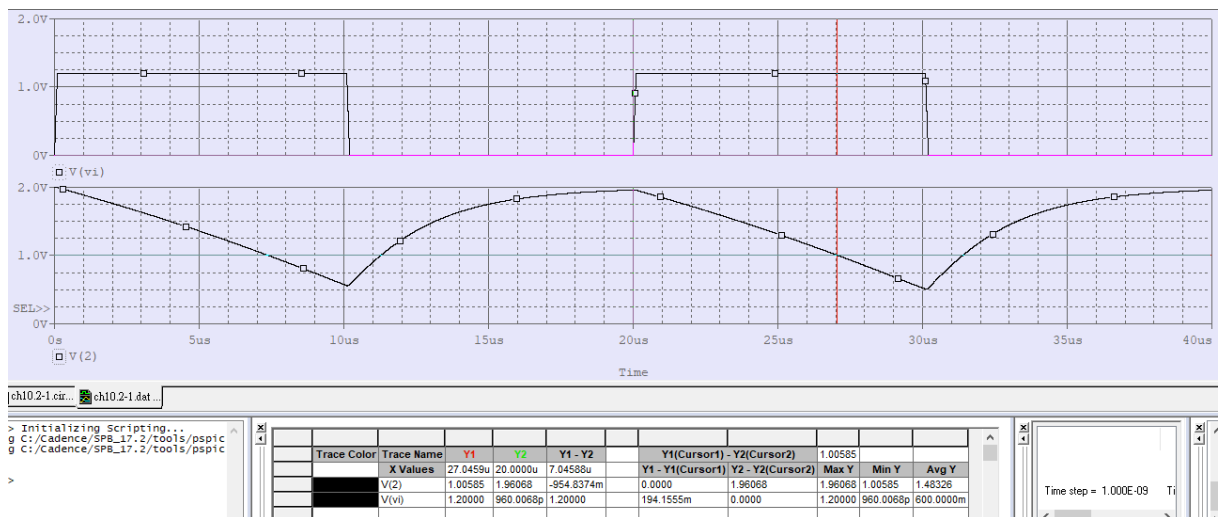
PMOS-to-NMOS ratio = 5

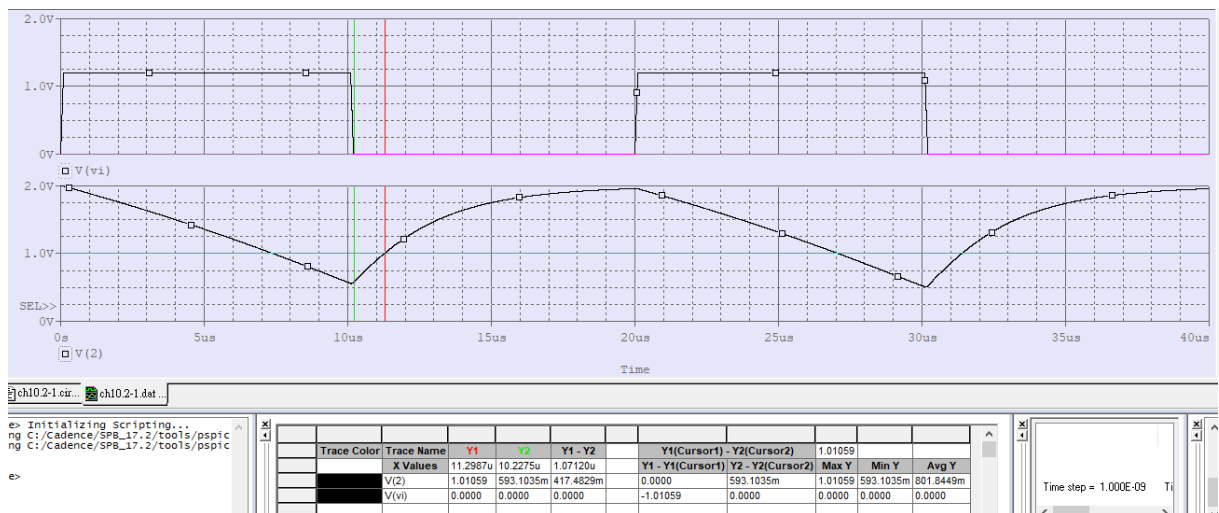
4. 電源電壓 V_{DD} 與 t_{pHL} 、 t_{pLH} 之關係。(NMOS W/L=1.5 及 PMOS W/L=3 (L=0.18um))

	V_{DD}				
	1	2	3	4	5
t_{pHL}	4.7078μ	7.0459μ	5.0974μ	3.0844μ	2.1429μ
t_{pLH}	1.3959μ	1.0712μ	0.8441μ	0.487μ	0.3119μ

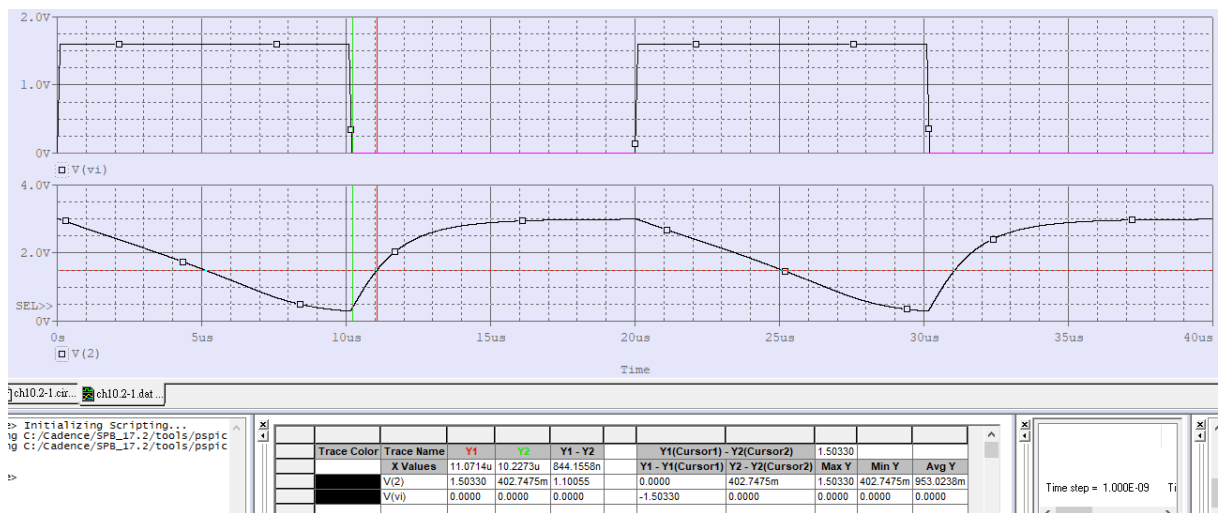
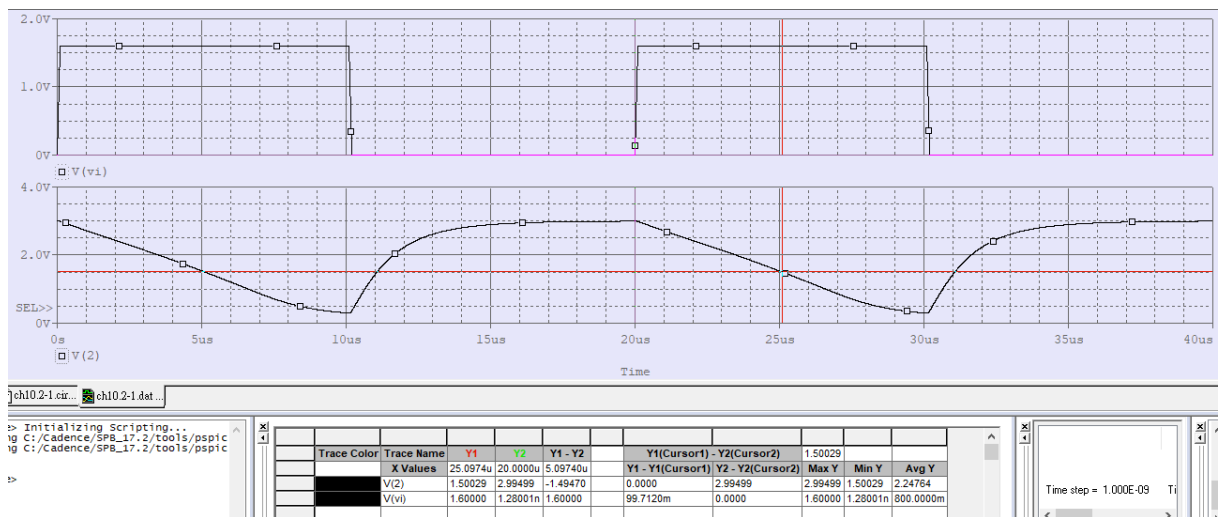


$V_{DD} = 1$

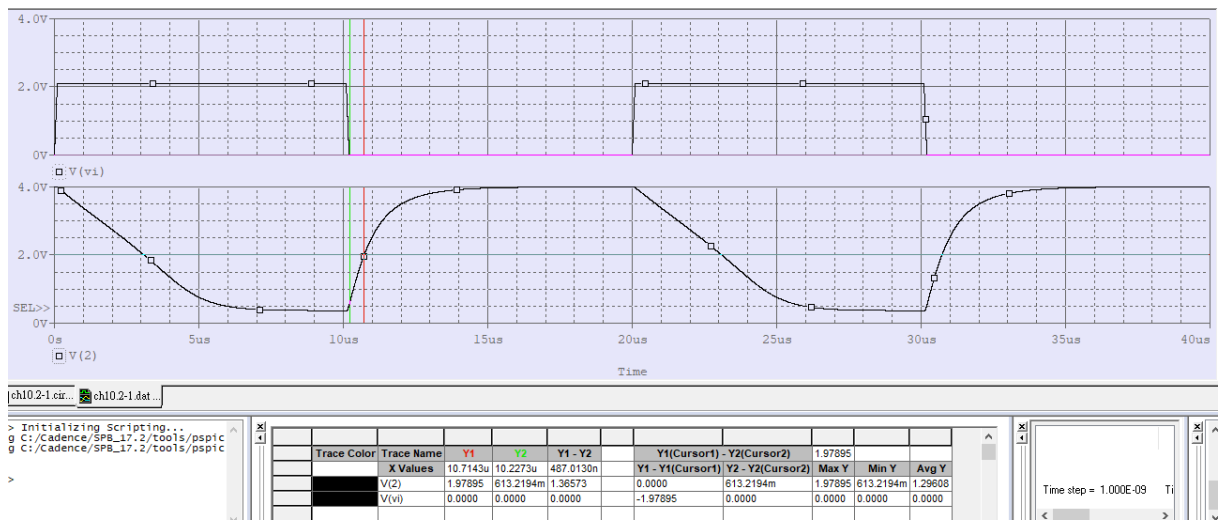
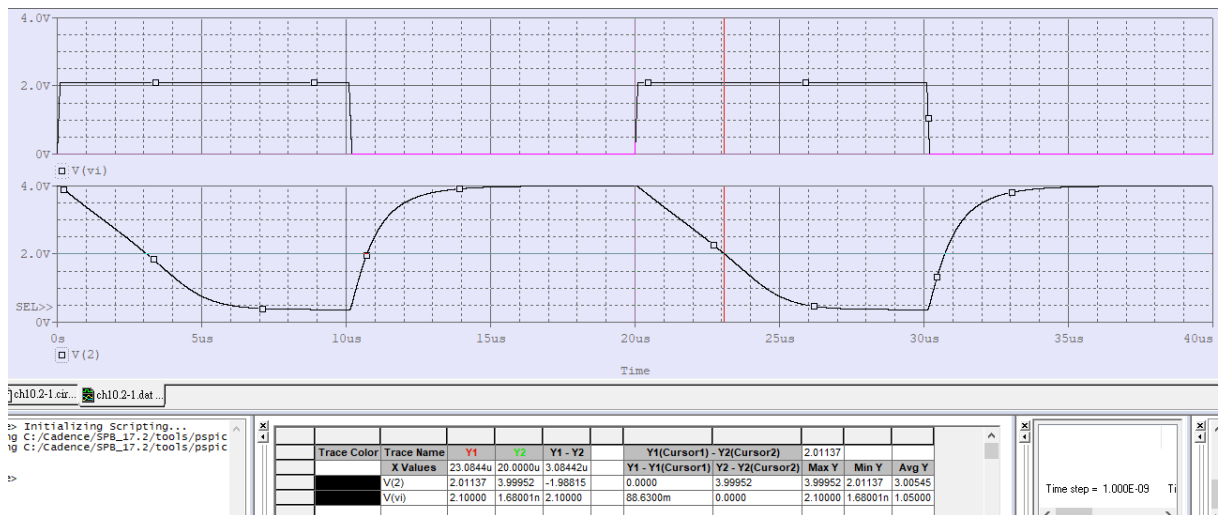




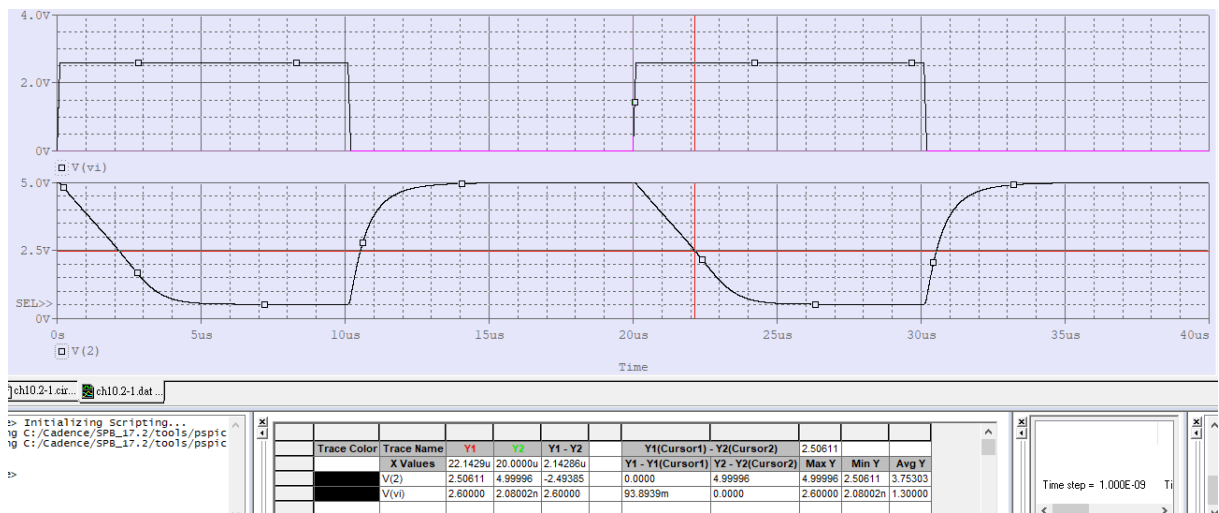
$V_{DD} = 2$

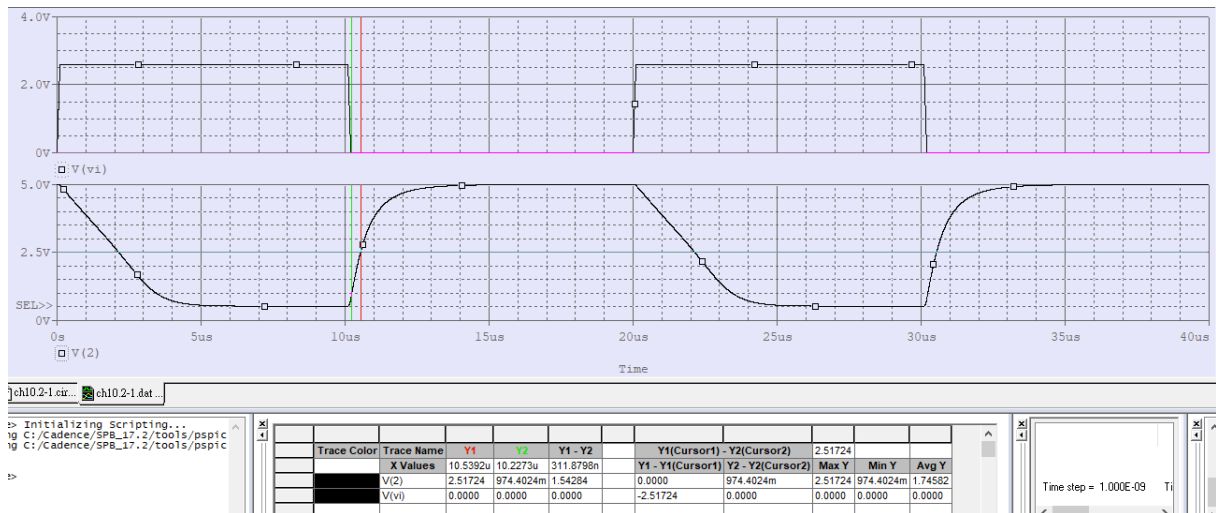


$V_{DD} = 3$



$V_{DD} = 4$

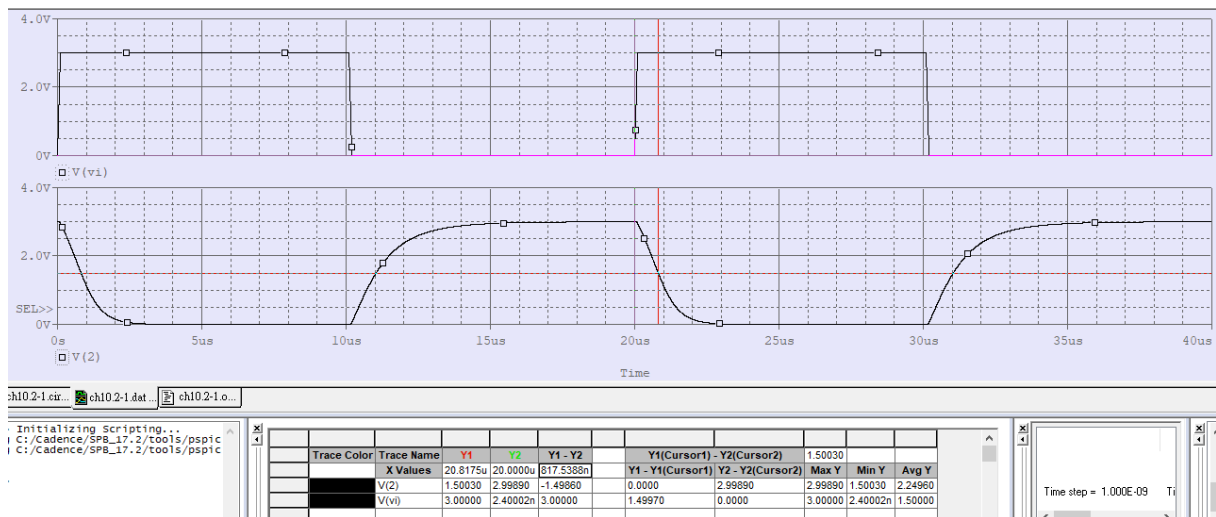




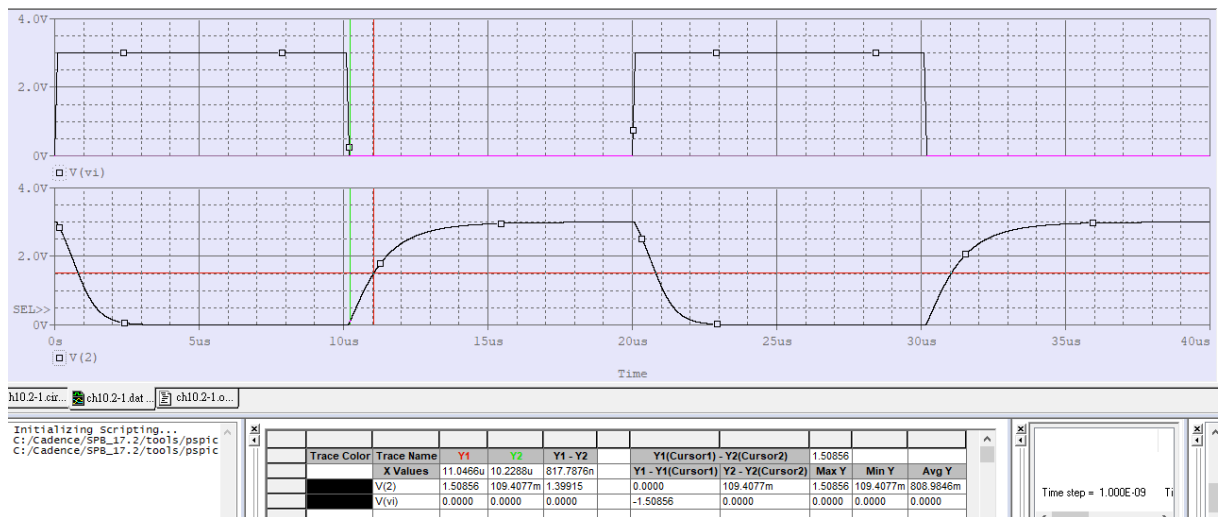
$$V_{DD} = 5$$

5. 設計 (決定 PMOS、NMOS W/L 的尺寸比) — t_{pHL} 、 t_{pLH} 相同之 CMOS 反向器 (假設 $L = 0.18\mu\text{m}$ ， $V_{DD} = 3\text{V}$)

NMOS : $L = 0.18\mu\text{m}$ ， $W = 0.27\mu\text{m}$ 。PMOS : $L = 0.18\mu\text{m}$ ， $W = 0.69\mu\text{m}$ 。



$$t_{pHL} = 817.5388\text{ns}$$



$$t_{pLH} = 817.7876\text{ns}$$