**電子電路設計模擬與實習**

實驗名稱：CMOS 反向器延遲時間分析

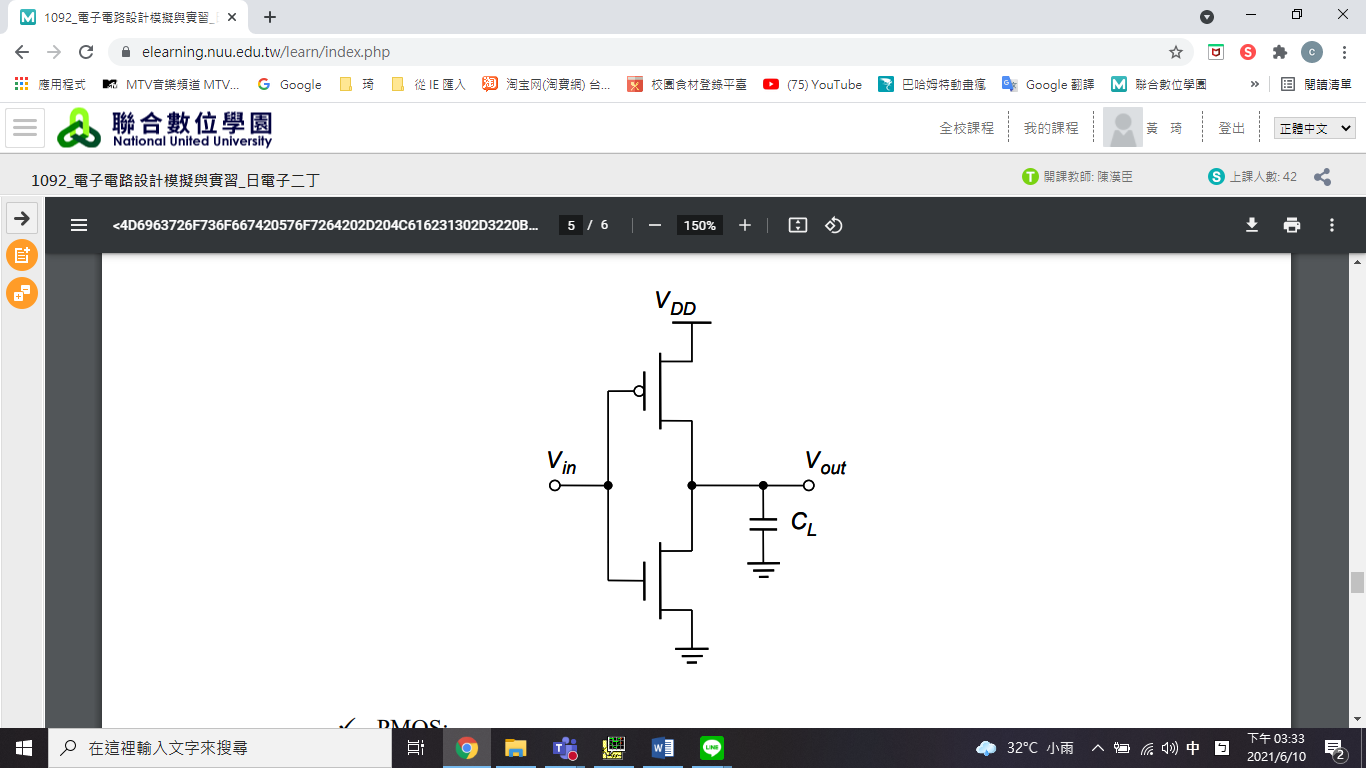
班級：電子二乙

組員：U0922113 郭晏寧

U0922107 張志斌

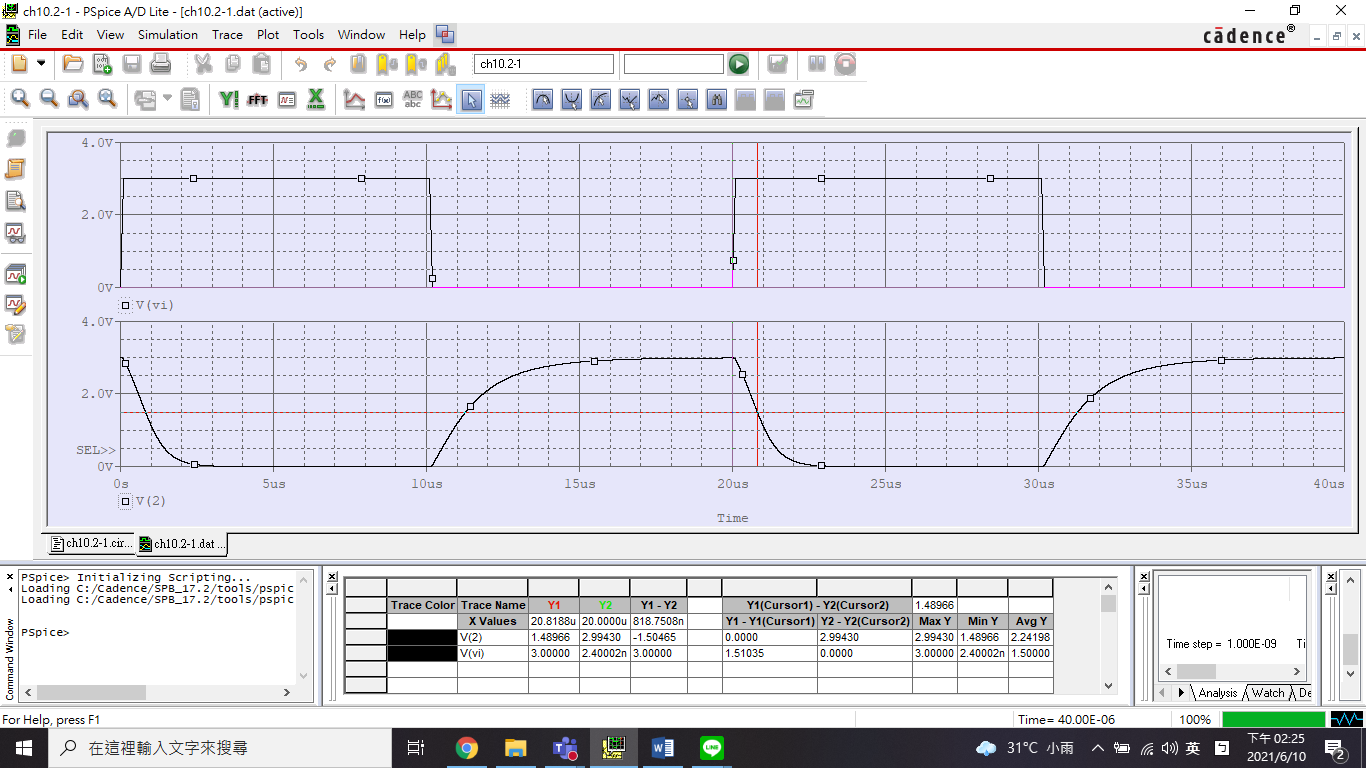
**Lab 10-2.** CMOS 反向器延遲時間分析

實驗電路圖：

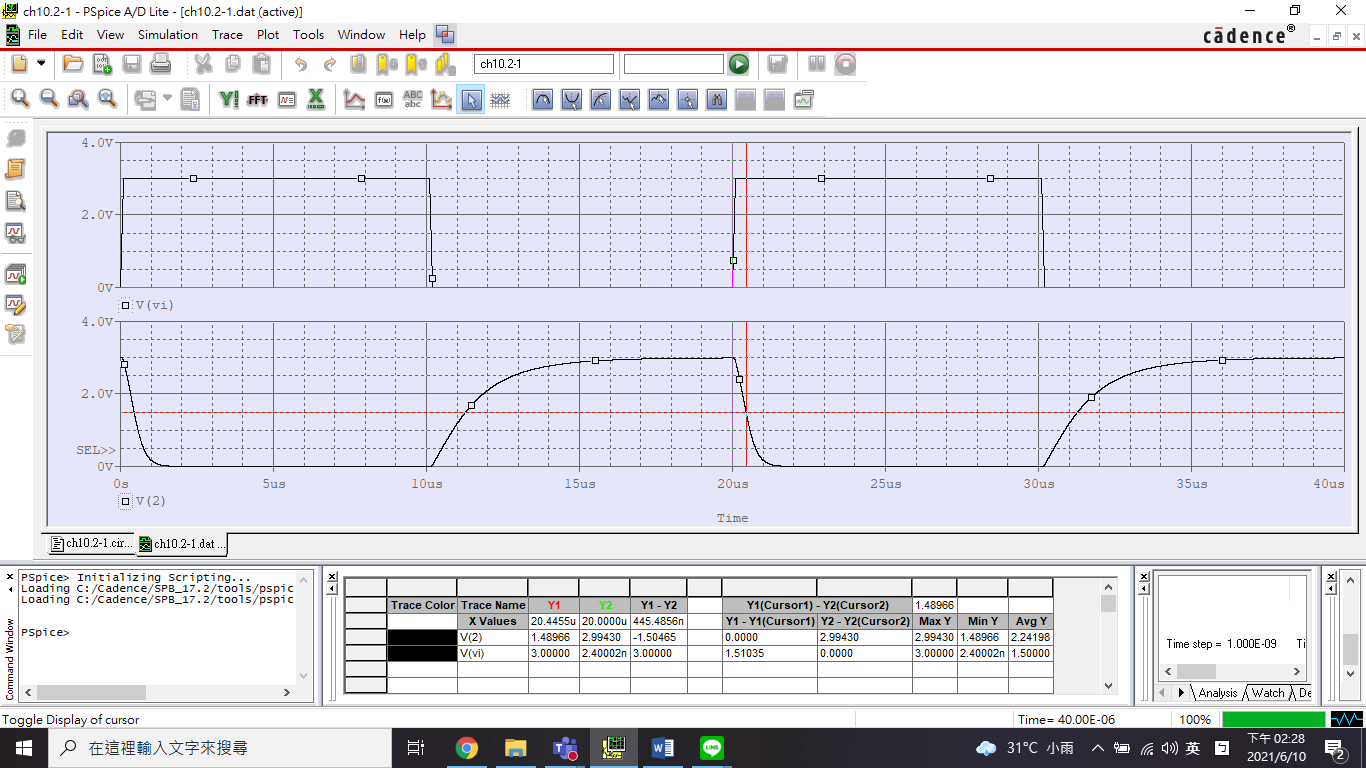


1. NMOS W/L尺寸與 之關係

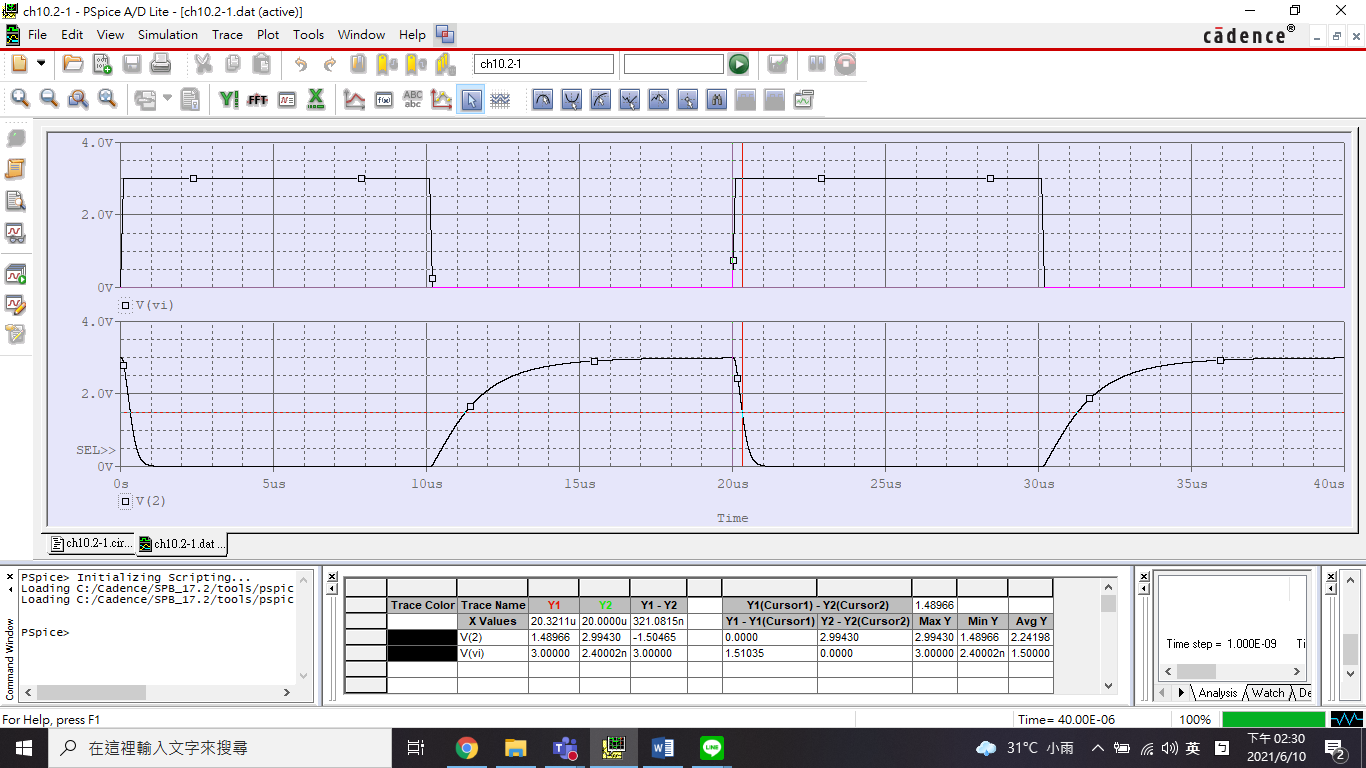
|  |  |  |  |
| --- | --- | --- | --- |
|  | **NMOS W/L** (L=0.18μm) | | |
| 1.5 | 3 | 4.5 |
| **PMOS W/L=3** | 0.8188μ | 0.4455μ | 0.3211μ |



NMOS W/L = 1.5



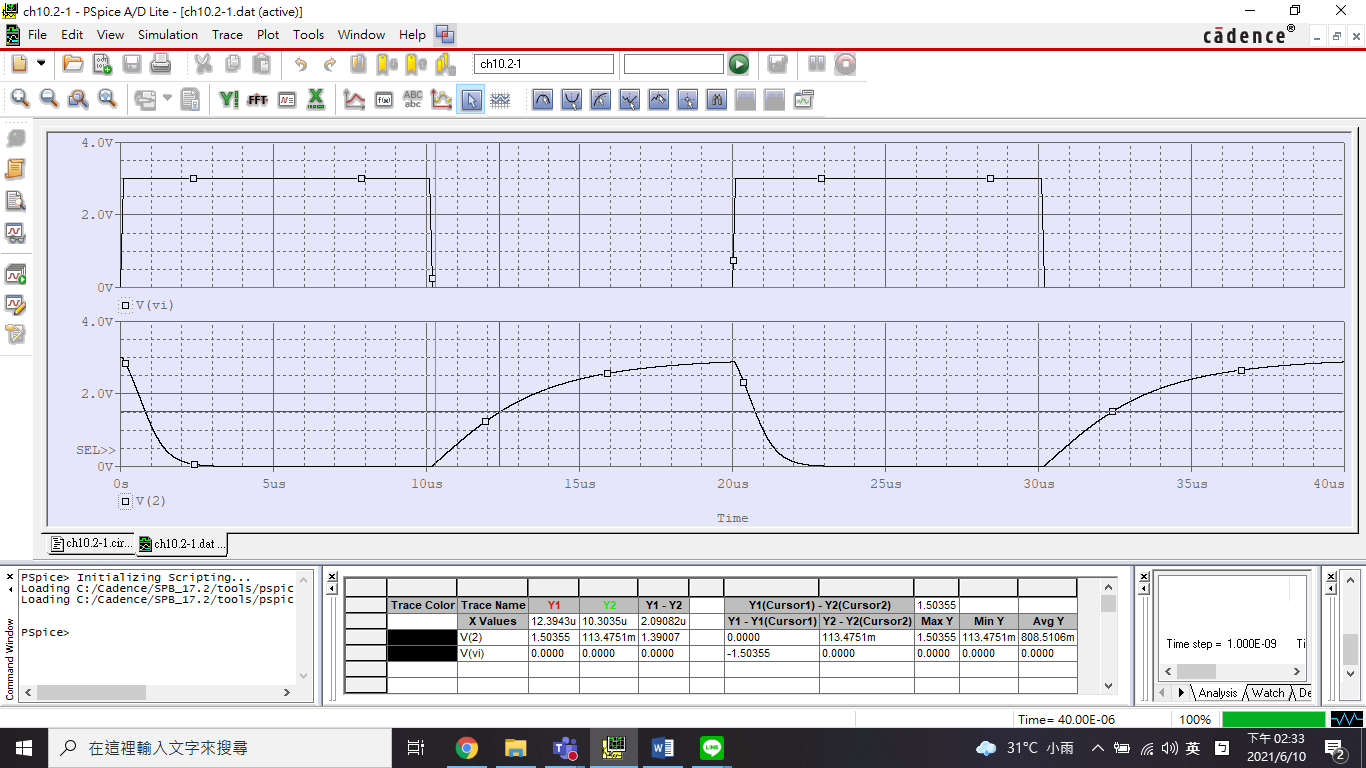
NMOS W/L = 3



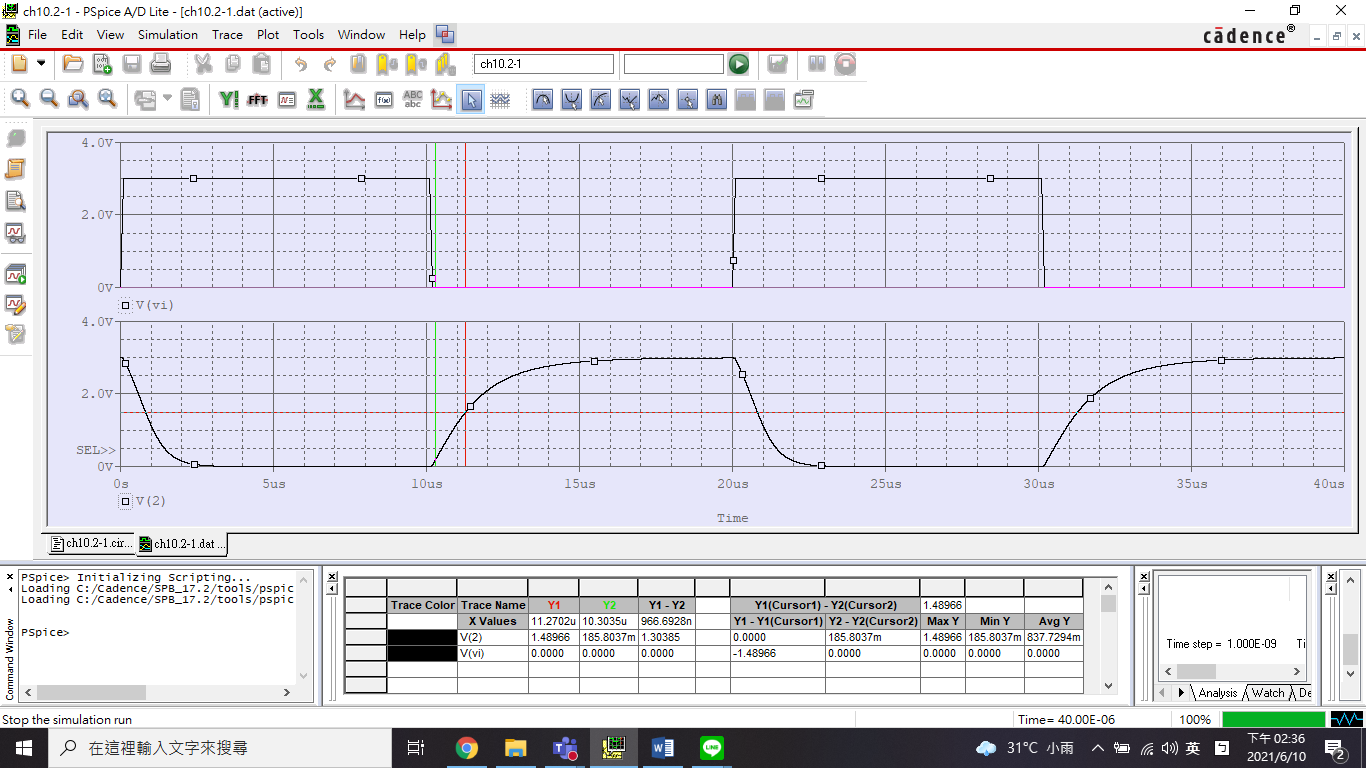
NMOS W/L = 4.5

1. PMOS W/L尺寸與 之關係

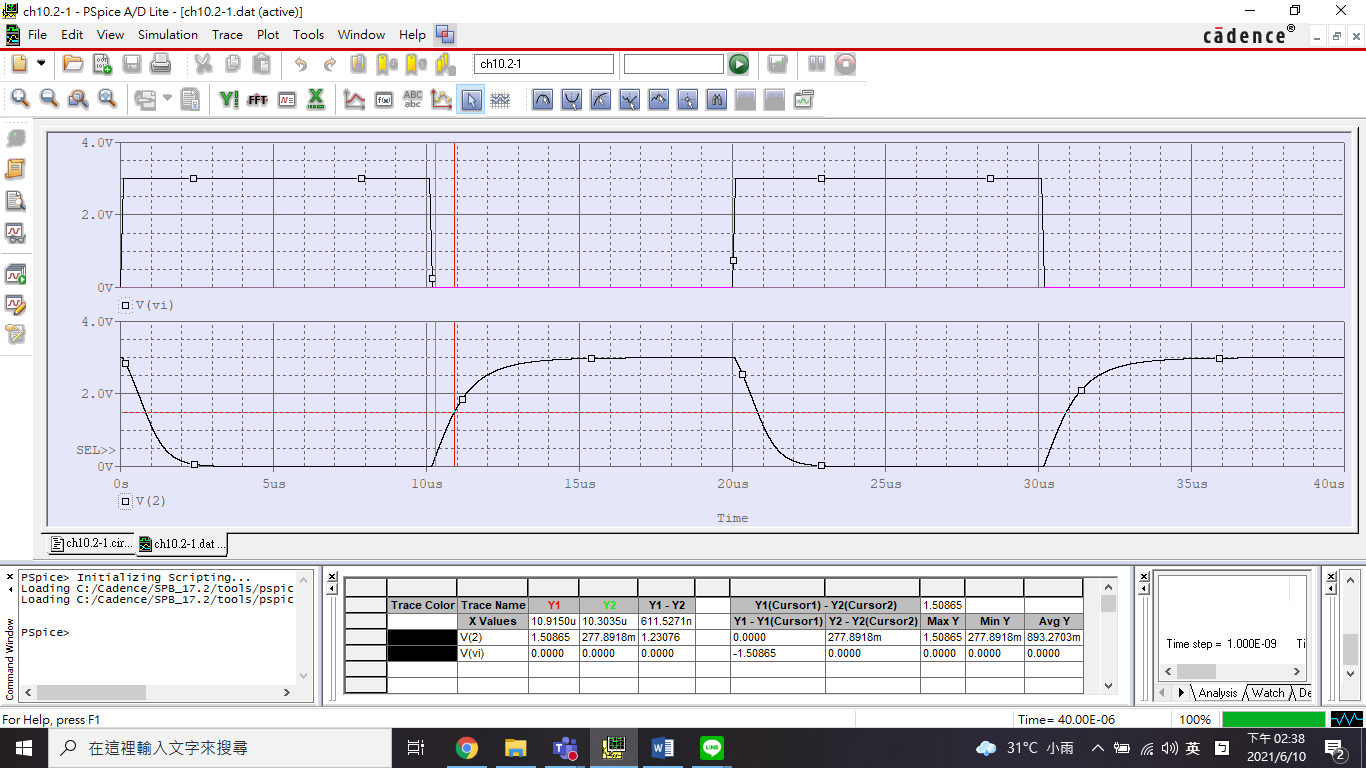
|  |  |  |  |
| --- | --- | --- | --- |
|  | **PMOS W/L** (L=0.18um) | | |
| 1.5 | 3 | 4.5 |
| **PMOS W/L=3** | 2.0908μ | 0.9667μ | 0.6115μ |



PMOS W/L = 1.5



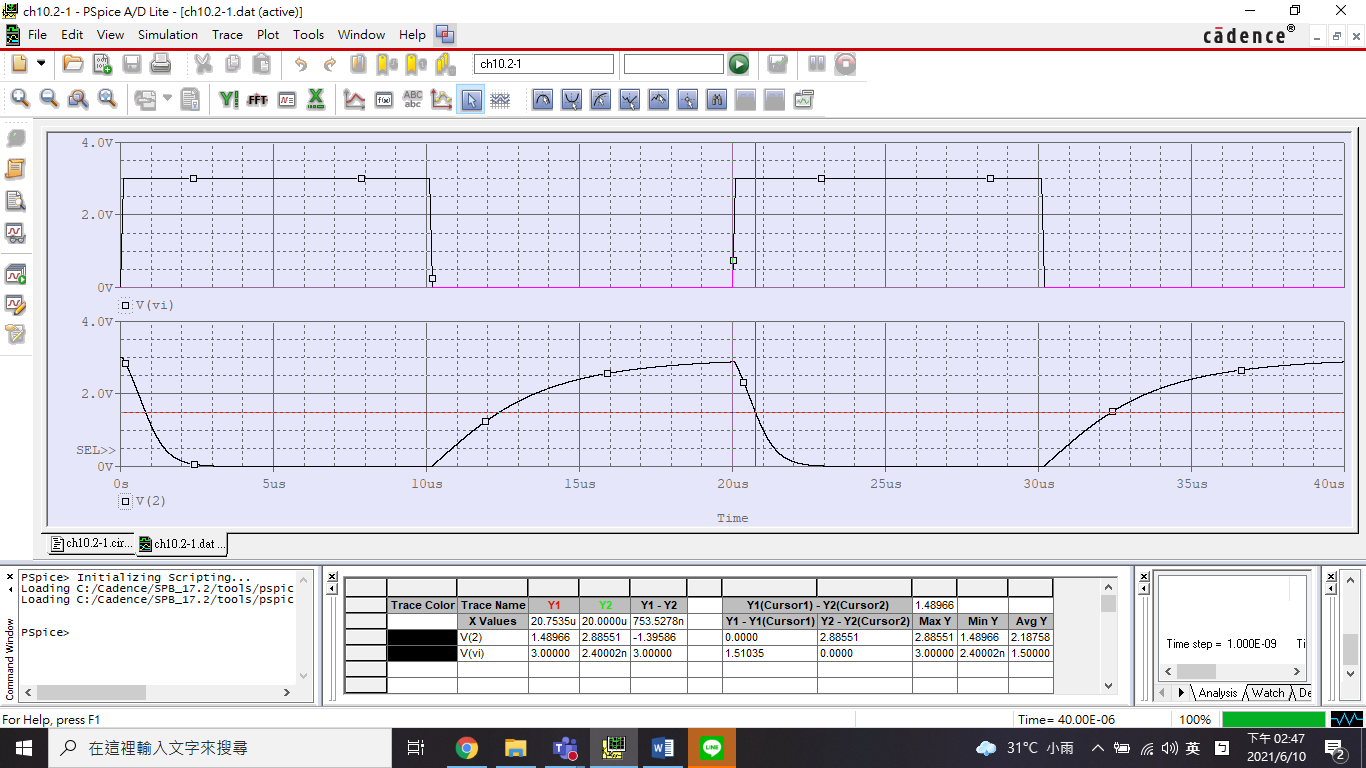
PMOS W/L = 3

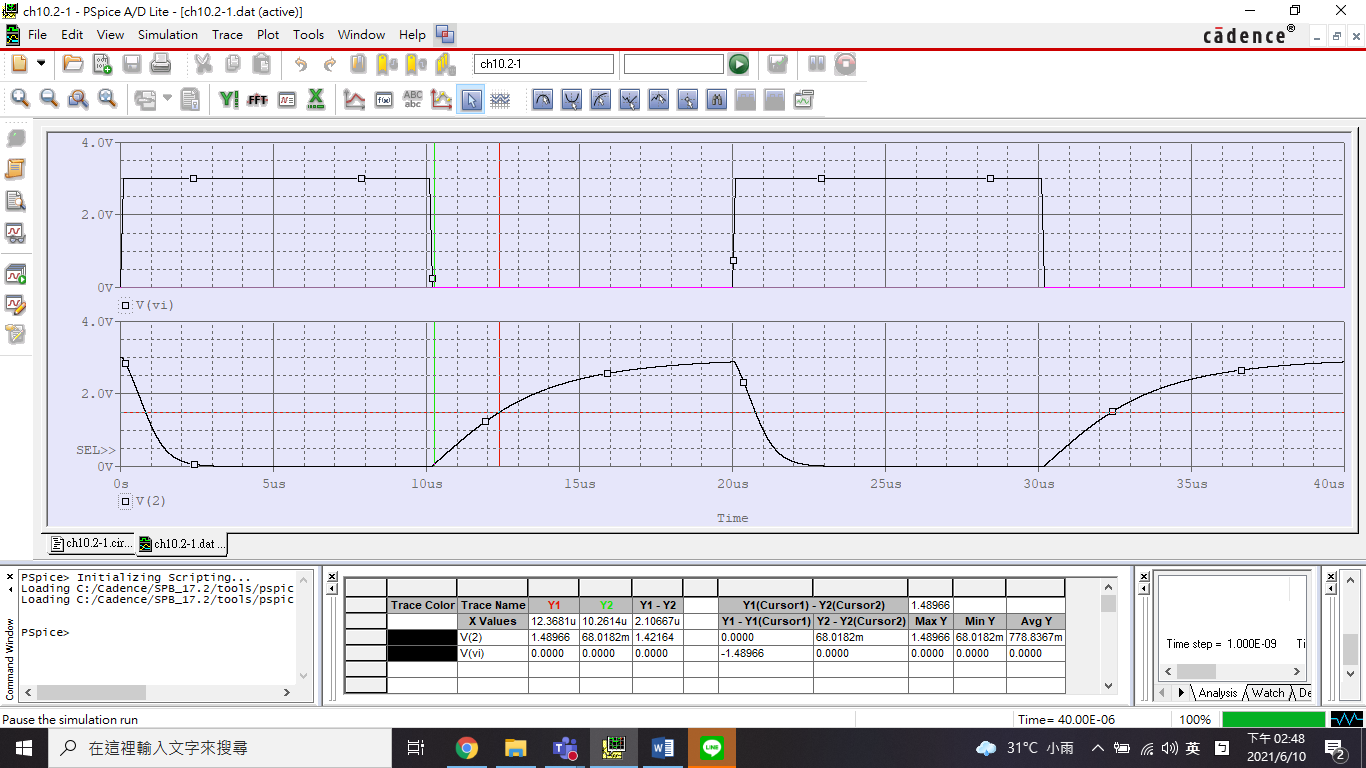


PMOS W/L = 4.5

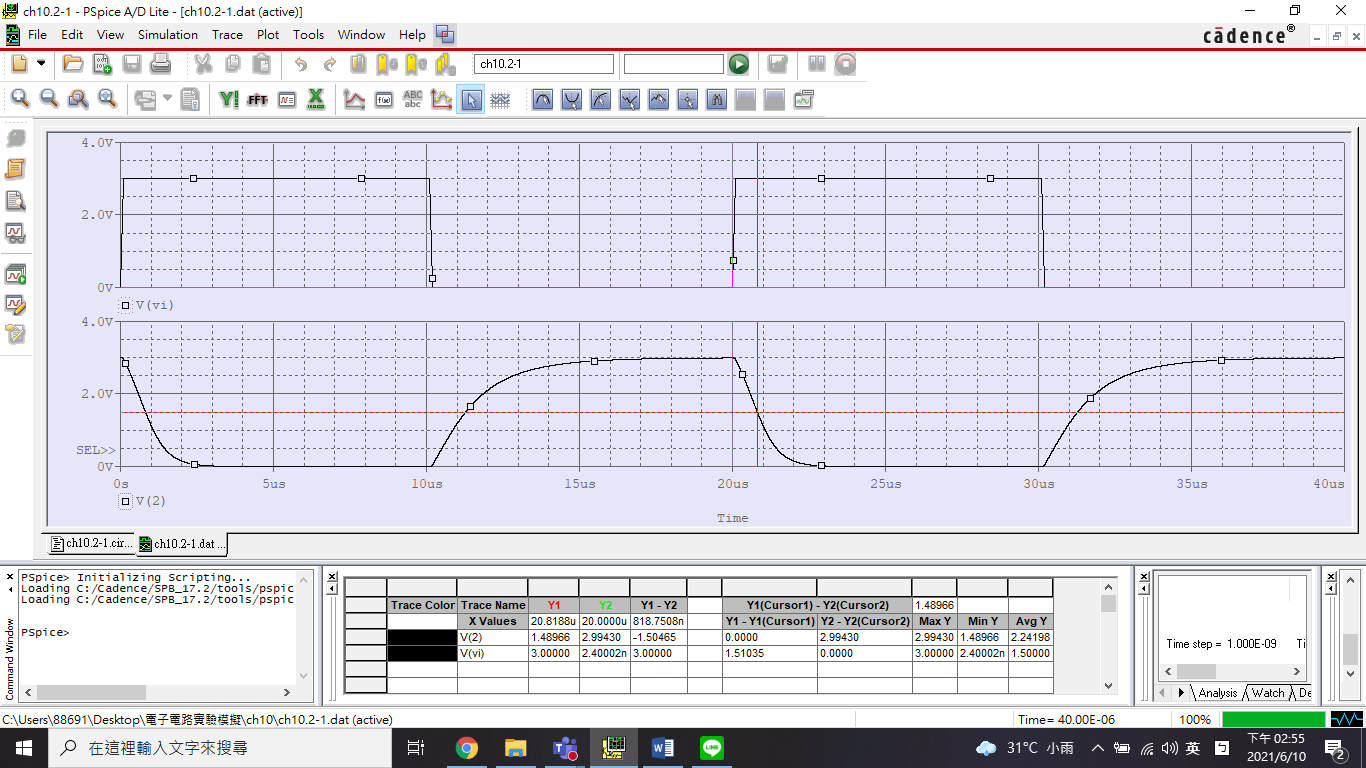
1. PMOS、NMOS W/L的尺寸比(PMOS-to-NMOS ration)與 、之關係

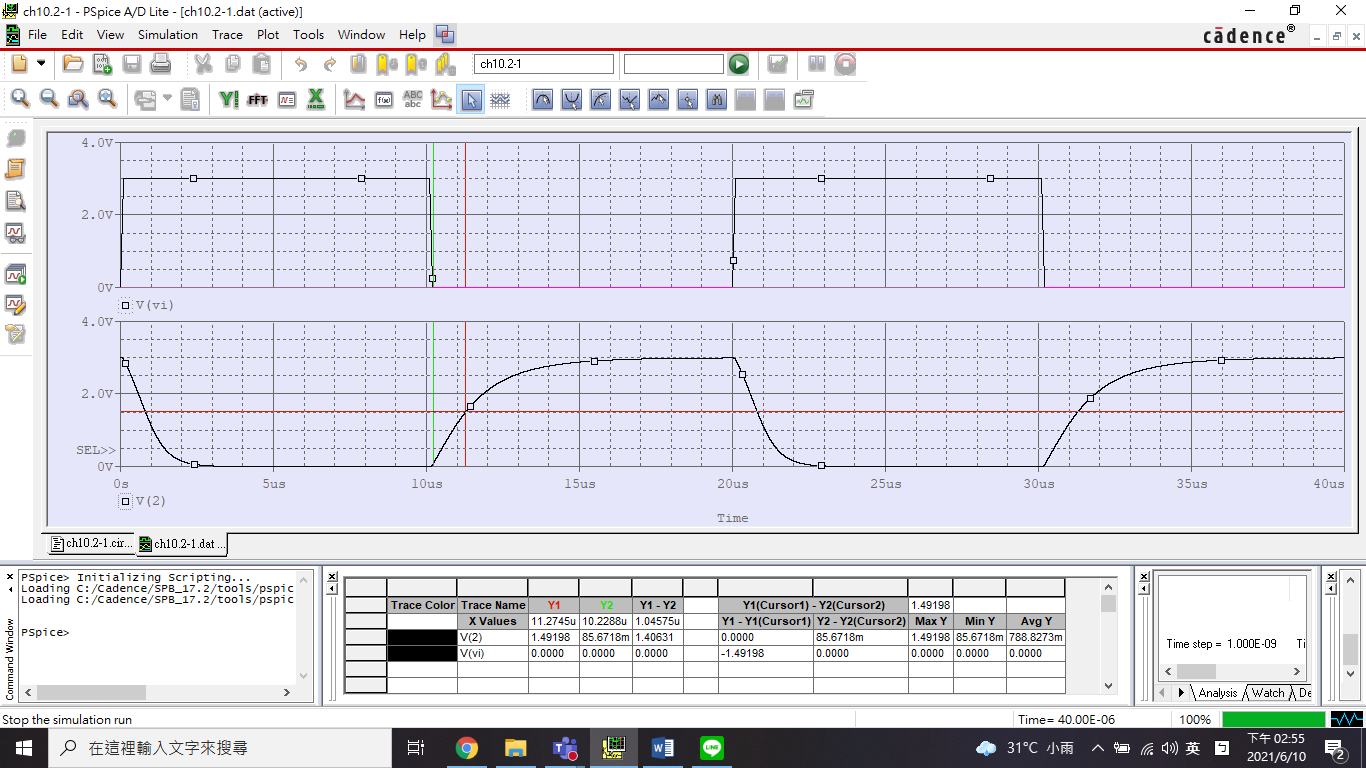
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **PMOS-to-NMOS ration** (L=0.18um) | | | | |
| 1 | 2 | 3 | 4 | 5 |
|  | 0.7535μ | 0.8188μ | 0.8221μ | 0.8223μ | 0.8223μ |
|  | 2.1067μ | 1.0457μ | 0.6862μ | 0.4925μ | 0.35μ |



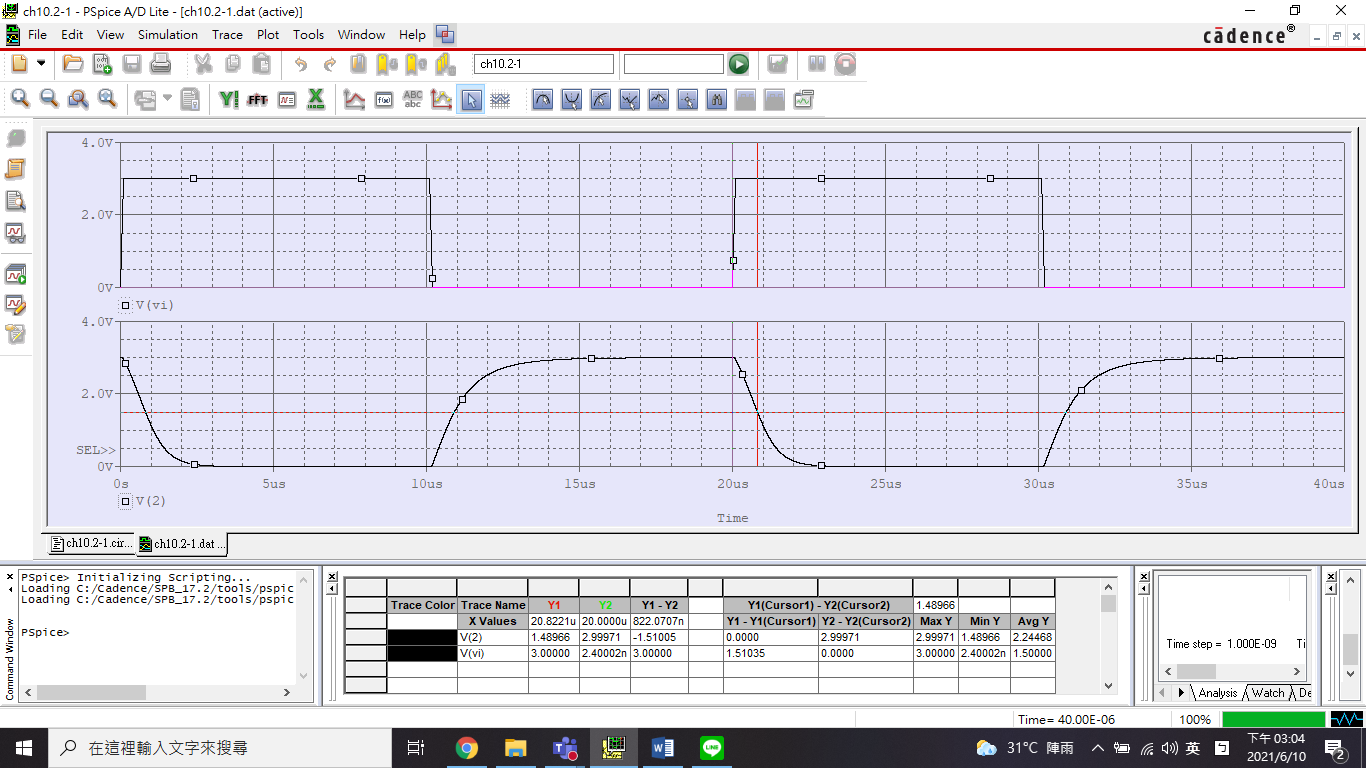


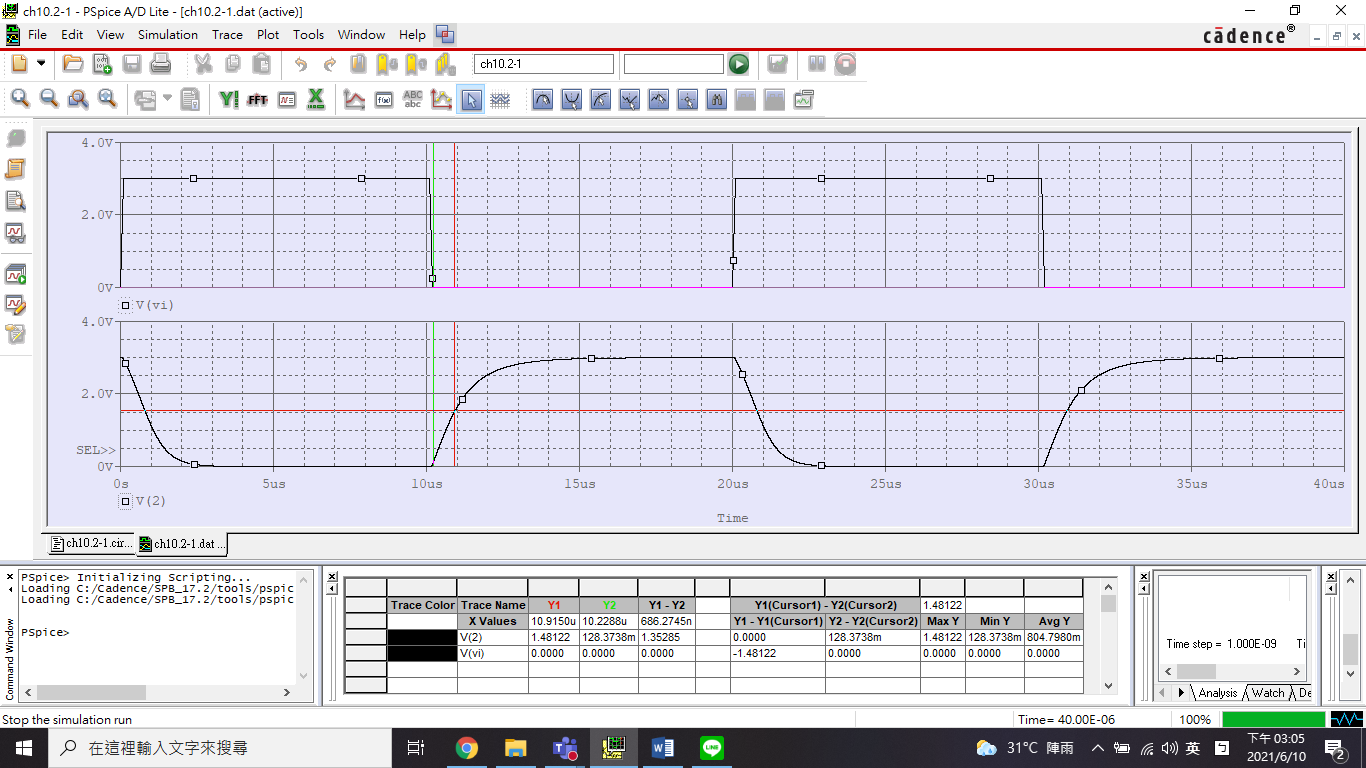
PMOS-to-NMOS ration = 1



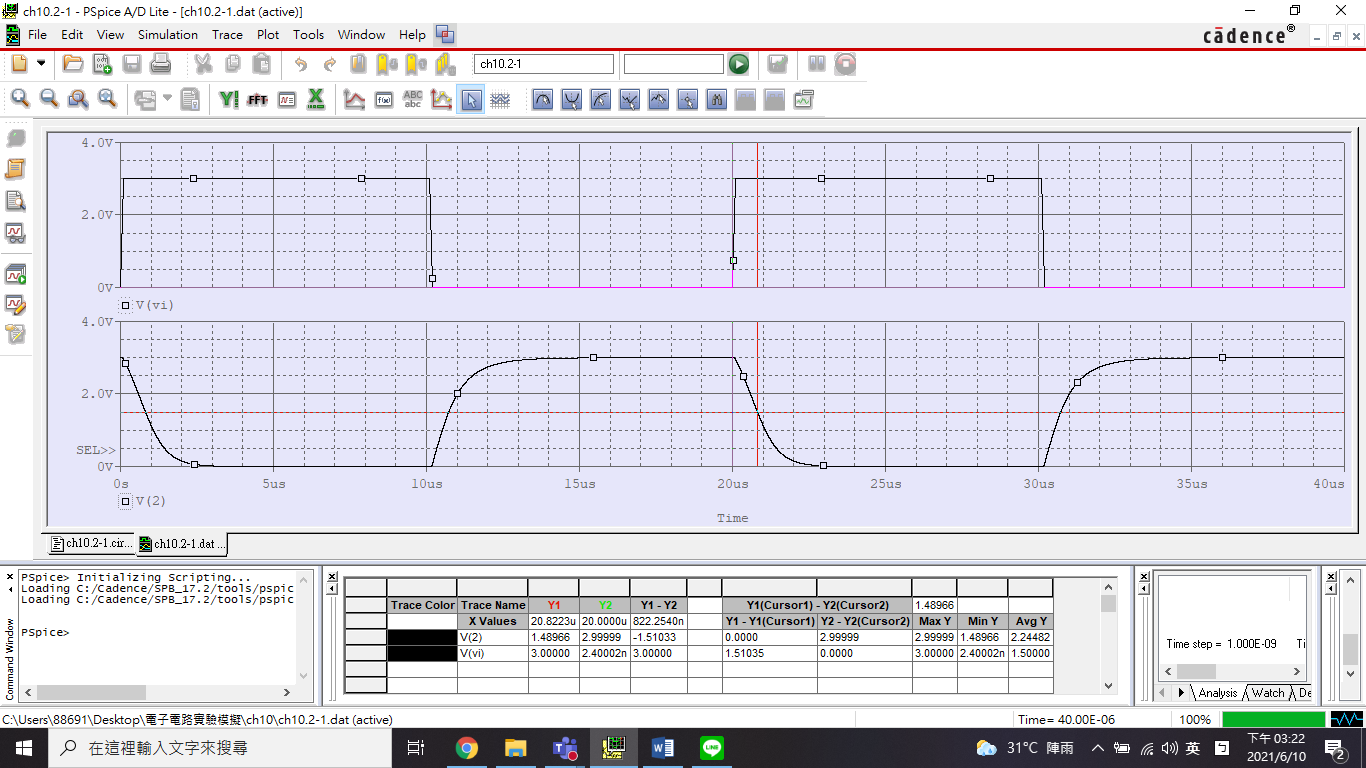


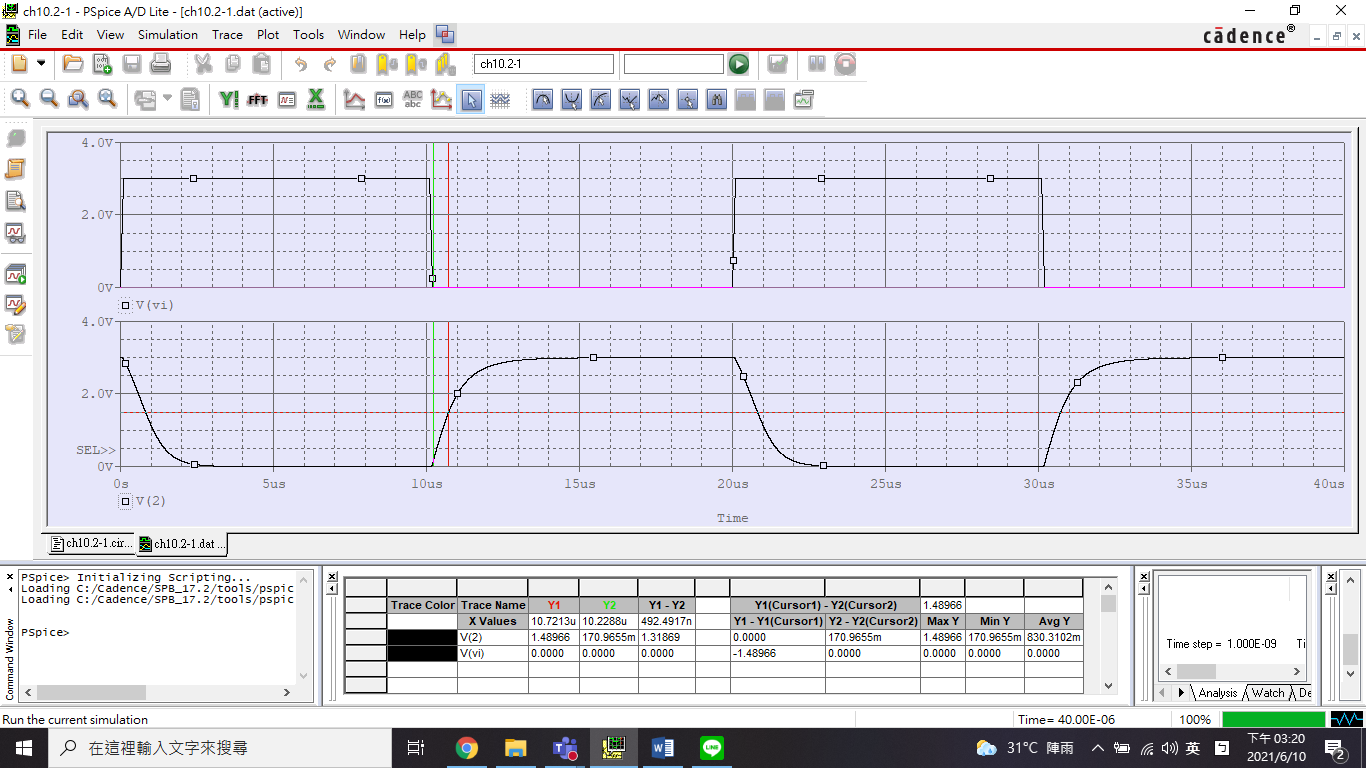
PMOS-to-NMOS ration = 2



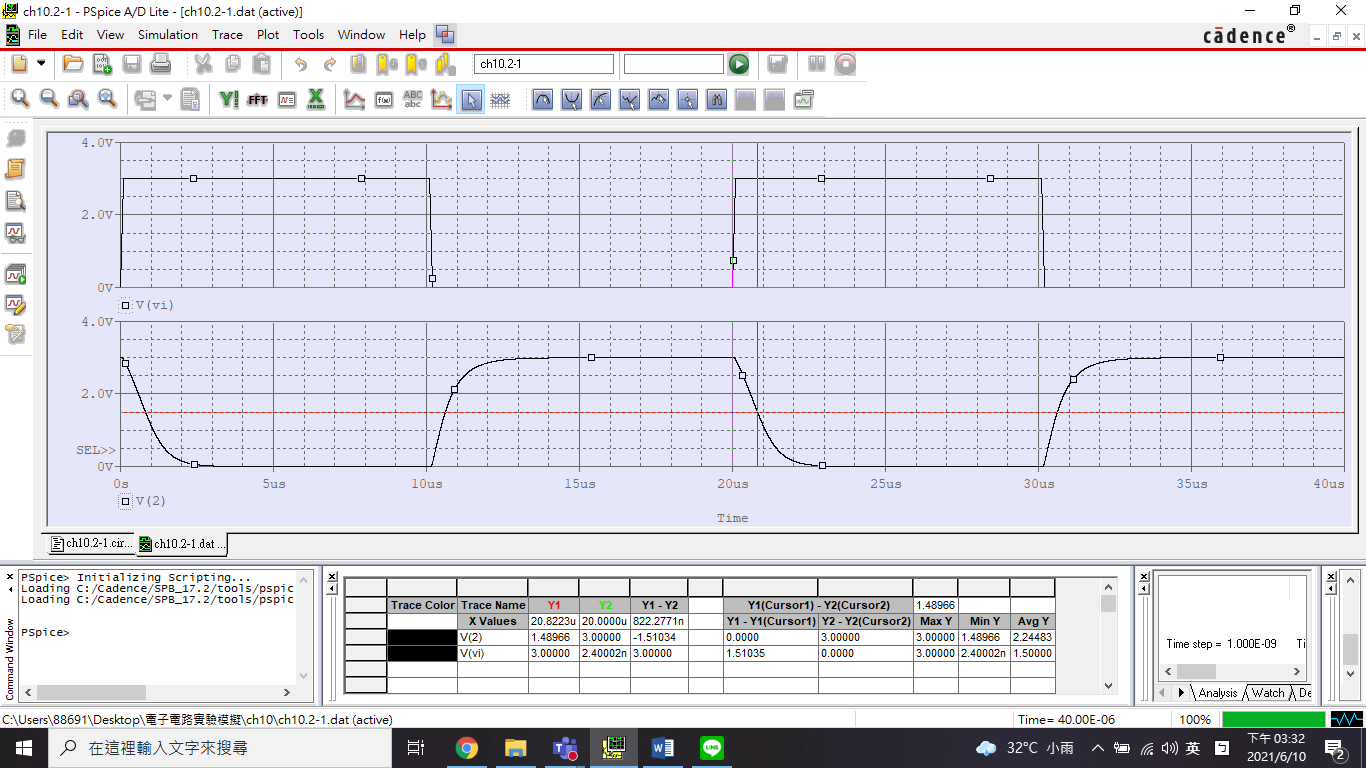


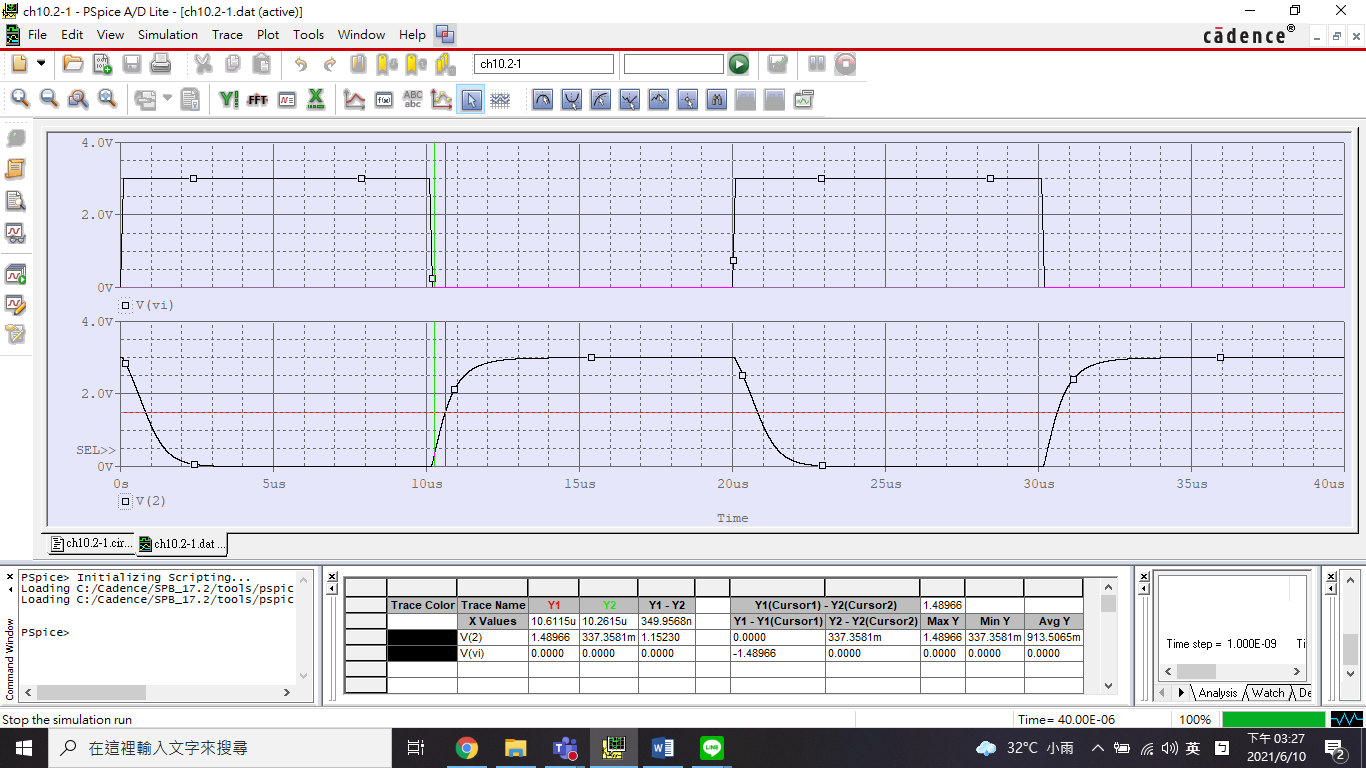
PMOS-to-NMOS ration = 3





PMOS-to-NMOS ration = 4

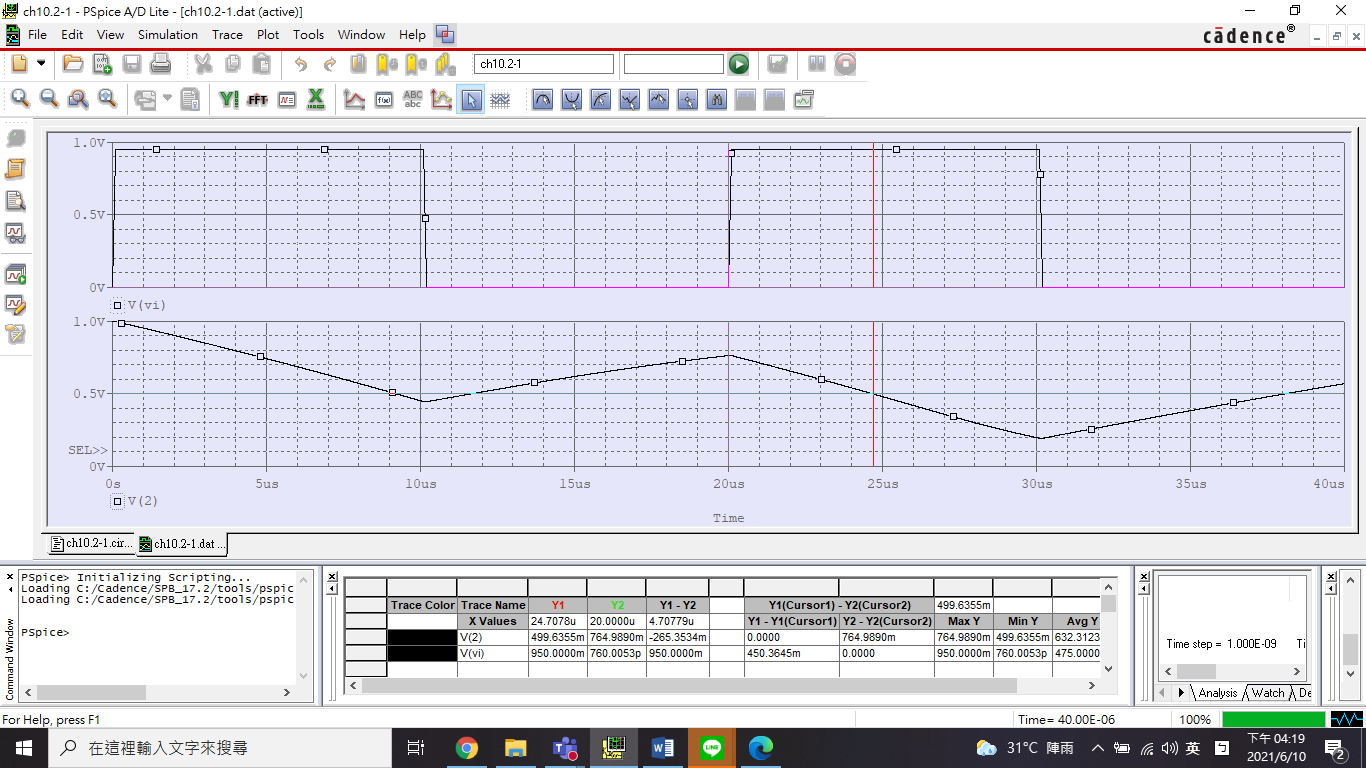


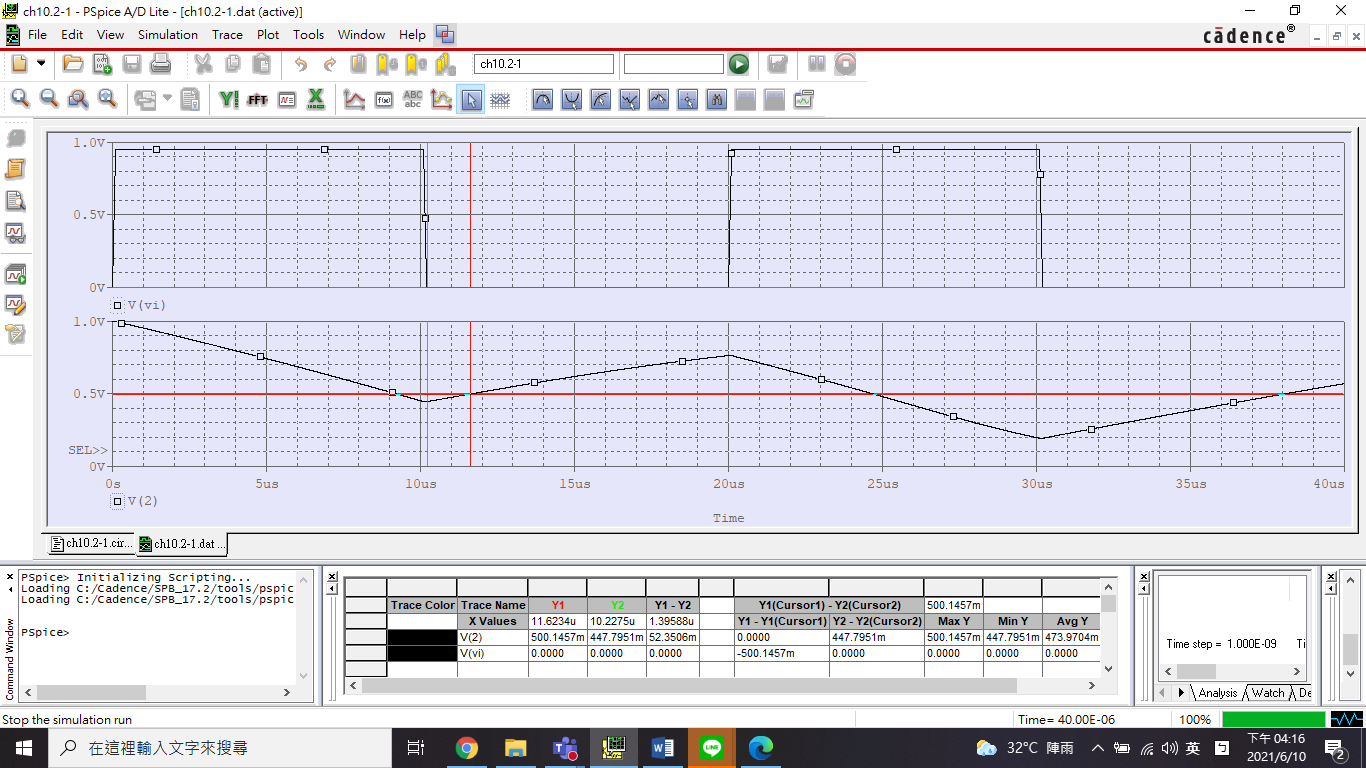


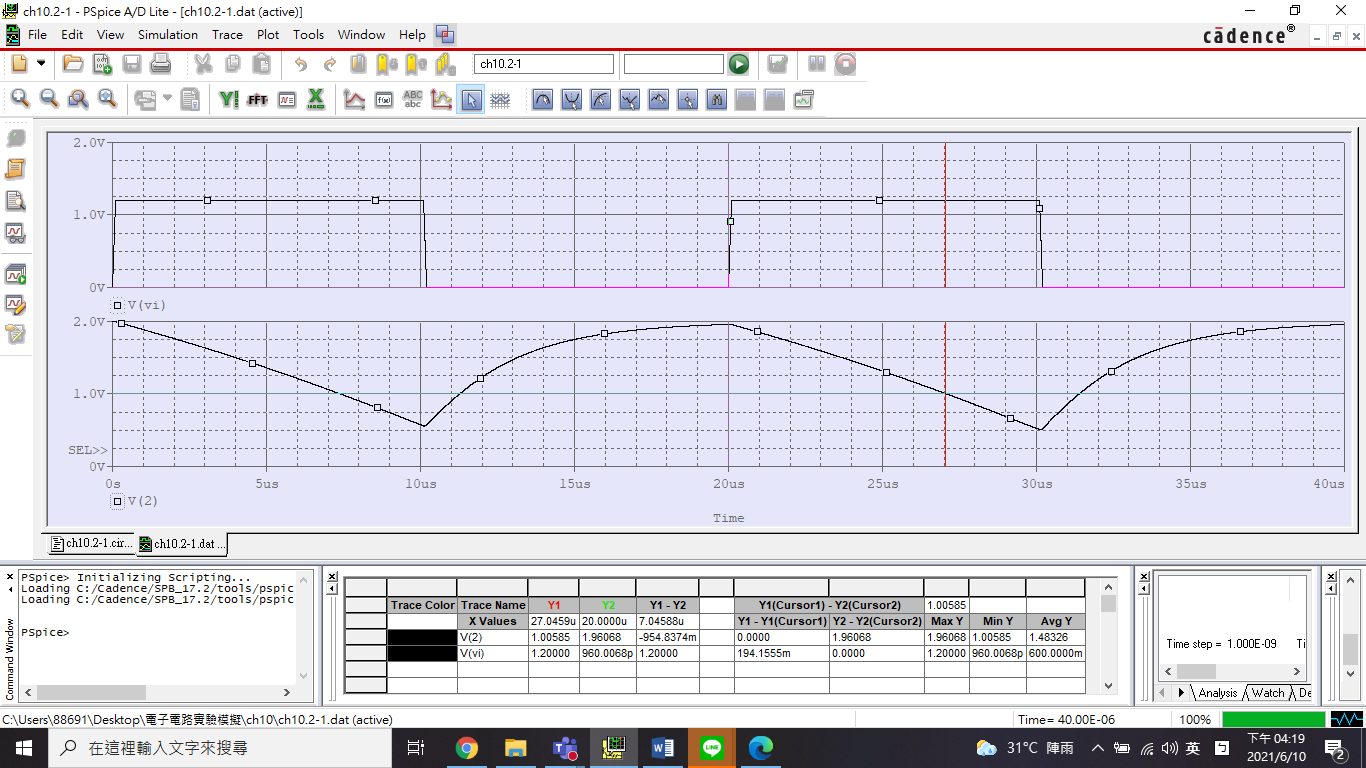
PMOS-to-NMOS ration = 5

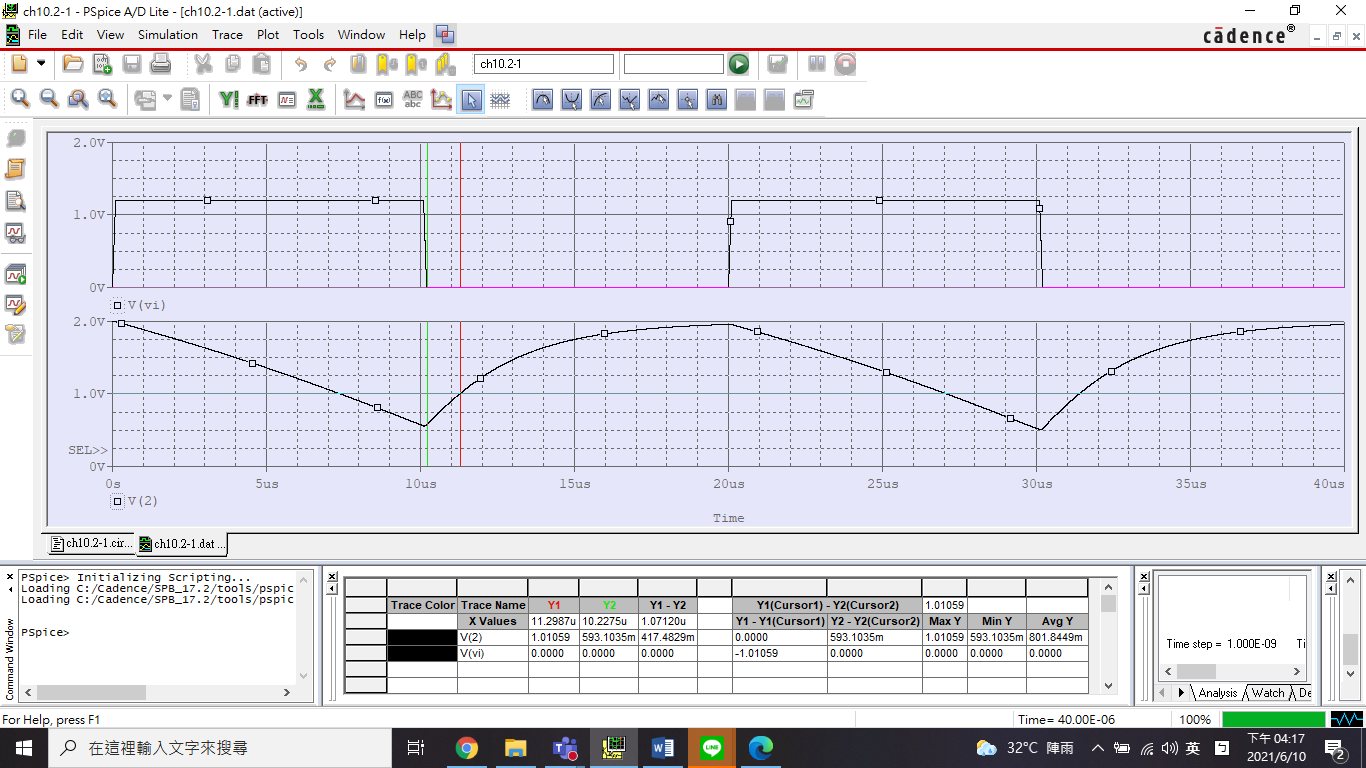
1. 電源電壓 與 、之關係。(NMOS W/L=1.5 及 PMOS W/L=3 (L=0. 18um))

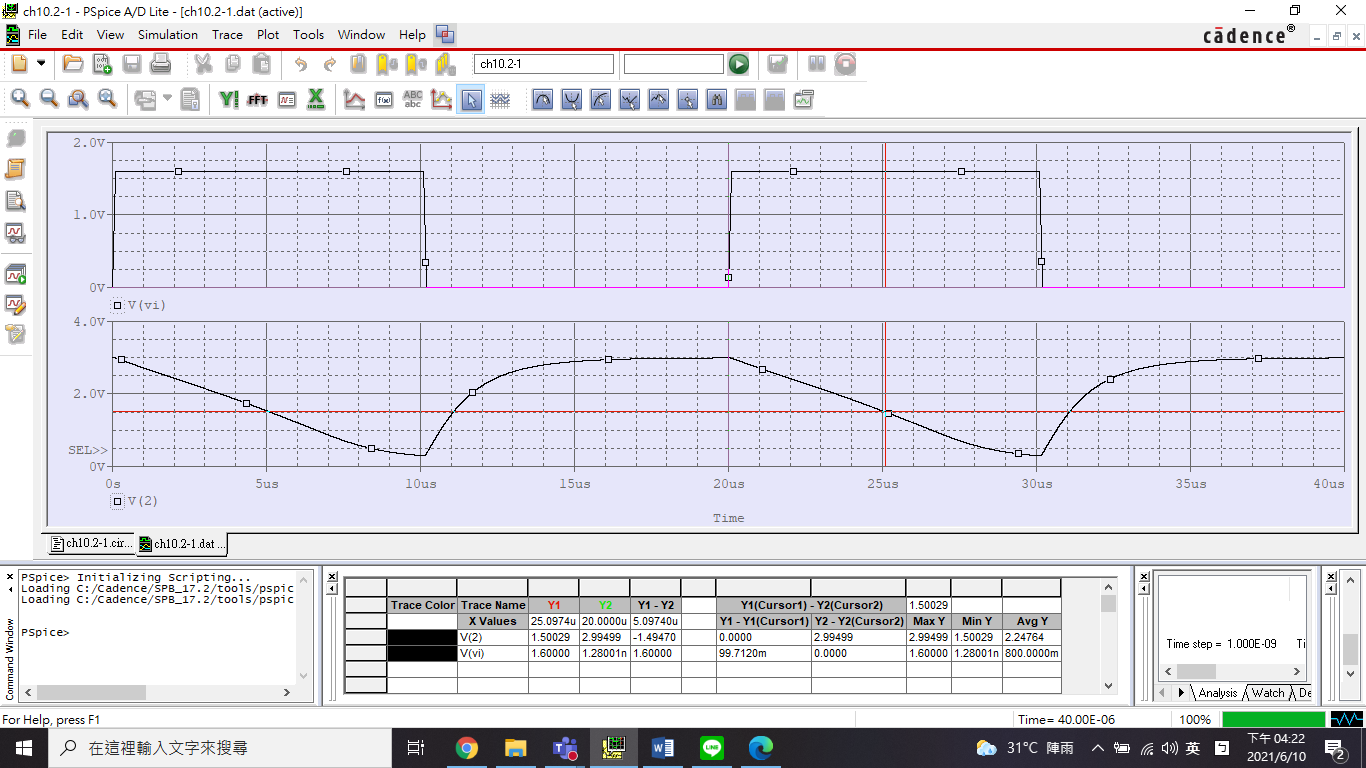
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | | | | |
| 1 | 2 | 3 | 4 | 5 |
|  | 4.7078μ | 7.0459μ | 5.0974μ | 3.0844μ | 2.1429μ |
|  | 1.3959μ | 1.0712μ | 0.8441μ | 0.487μ | 0.3119μ |

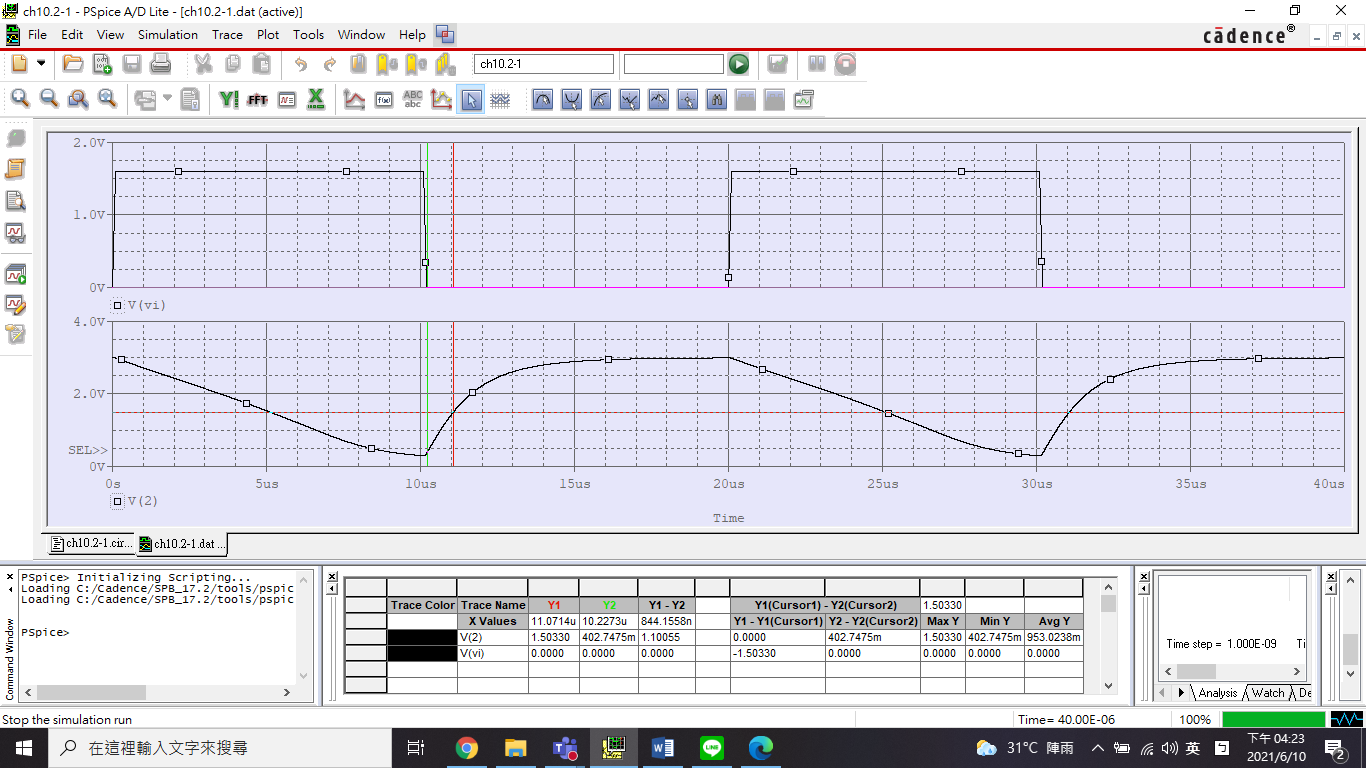


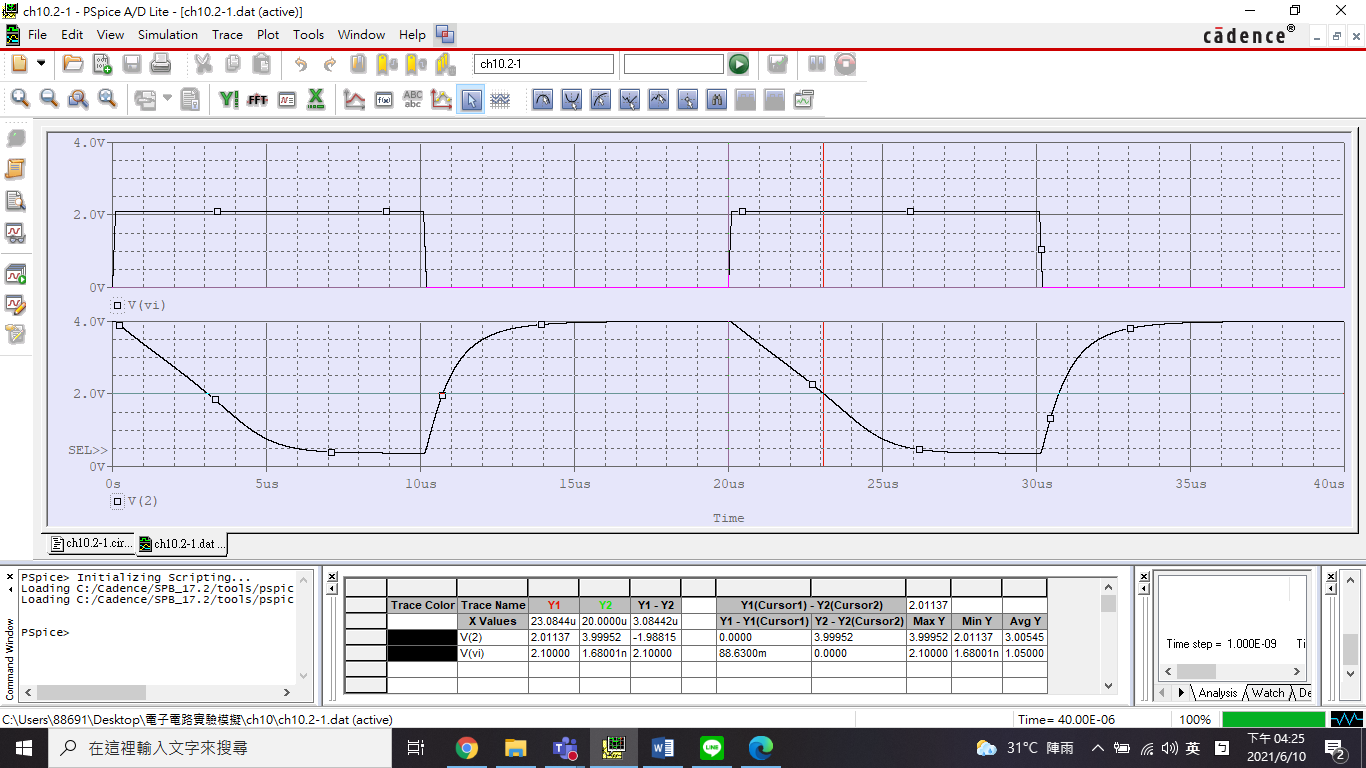


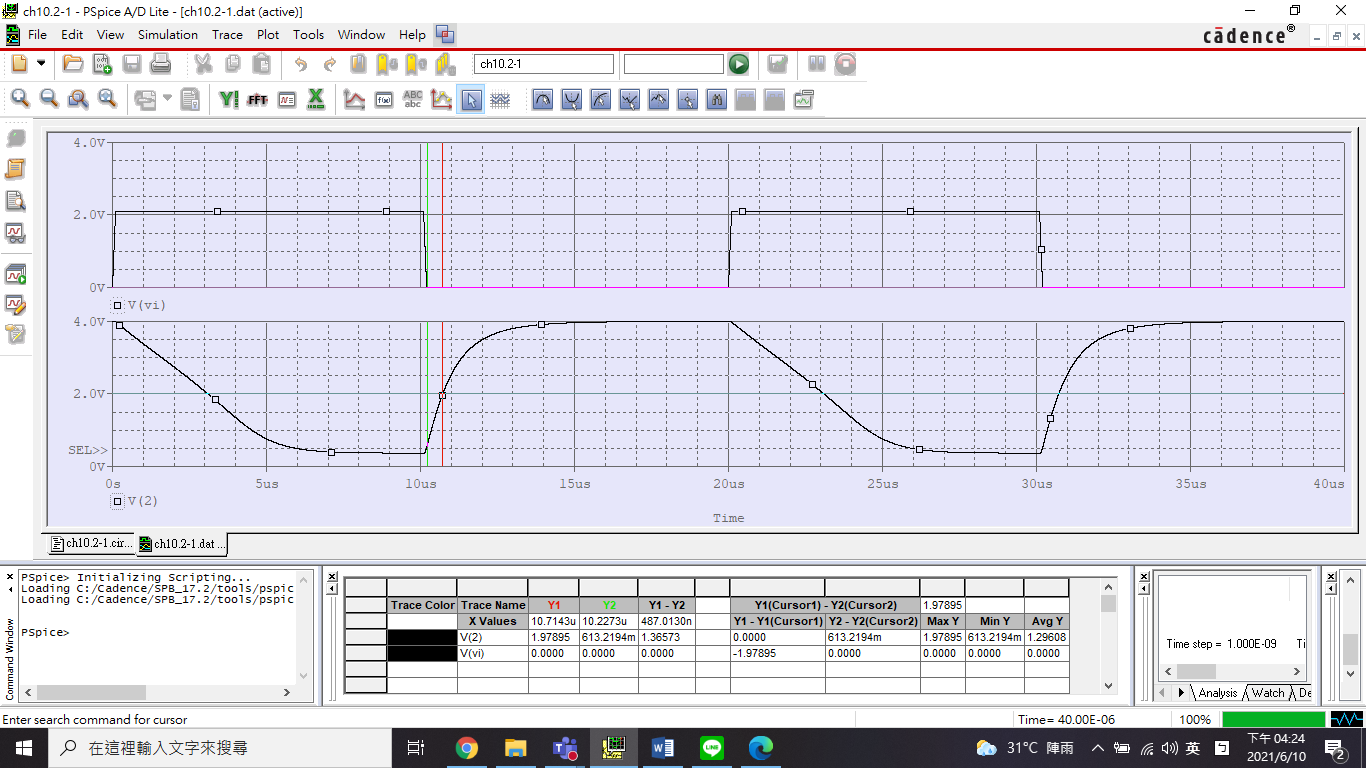


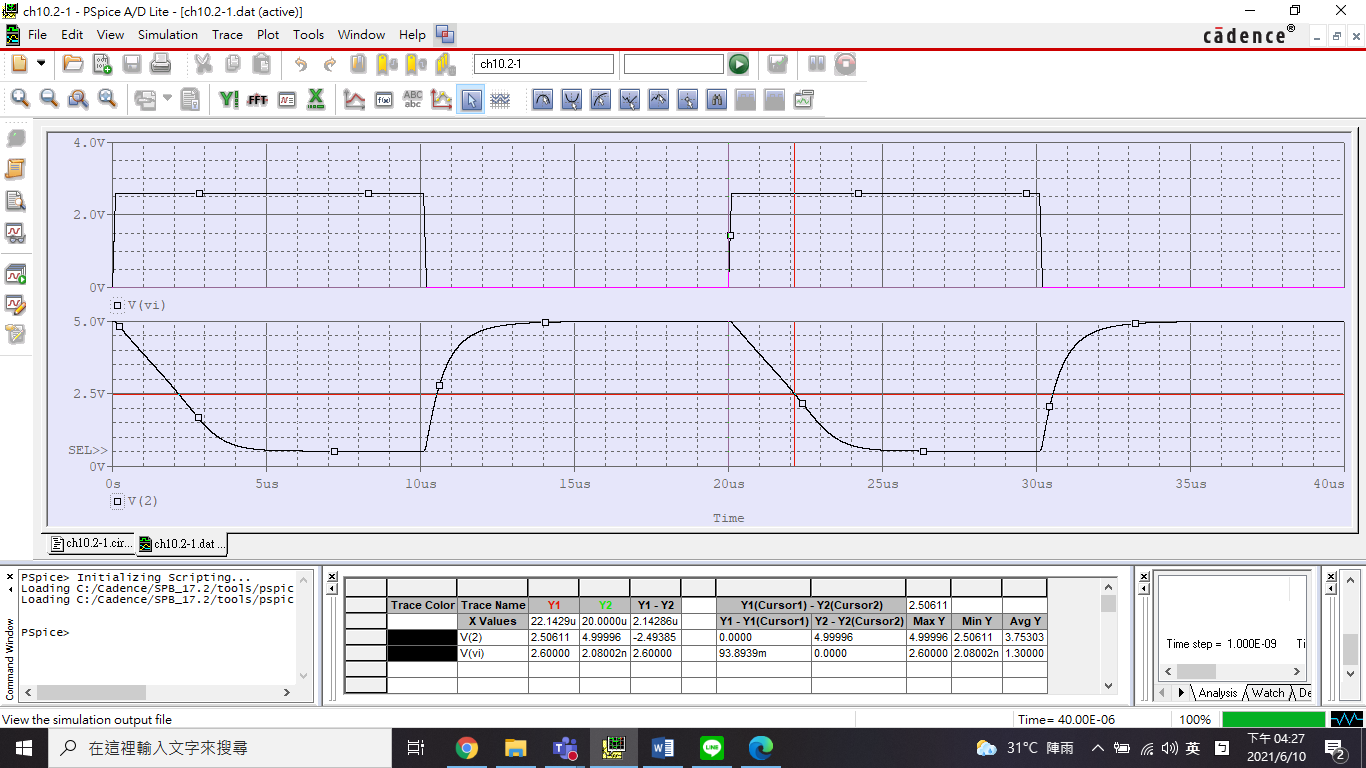


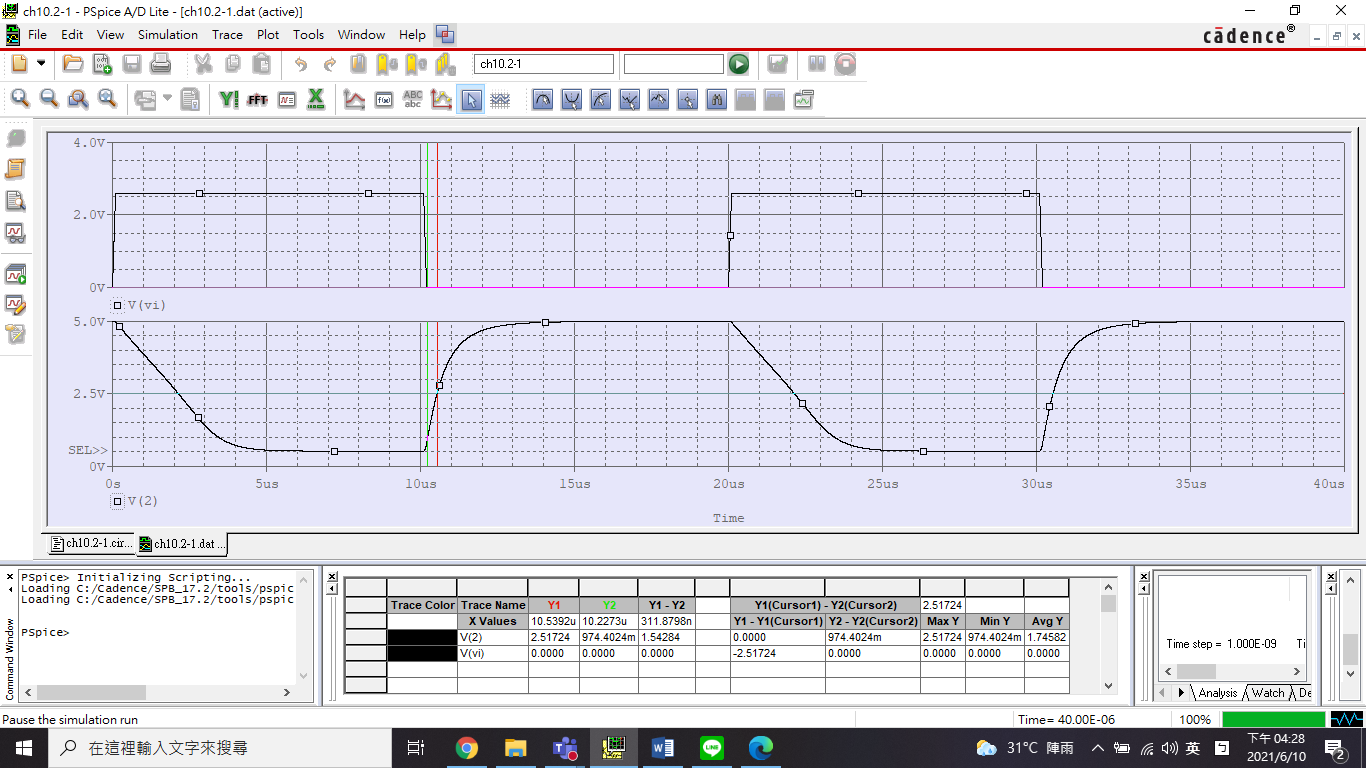












1. 設計 (決定 PMOS、NMOS W/L 的尺寸比) 一、相同之 CMOS 反向器 (假設 L = 0.18um，= 3V)

NMOS：L = 0.18um，W = 0.27um。PMOS：L = 0.18um，W = 0.69um。

