**電子電路設計模擬與實習**

實驗名稱：差動放大器

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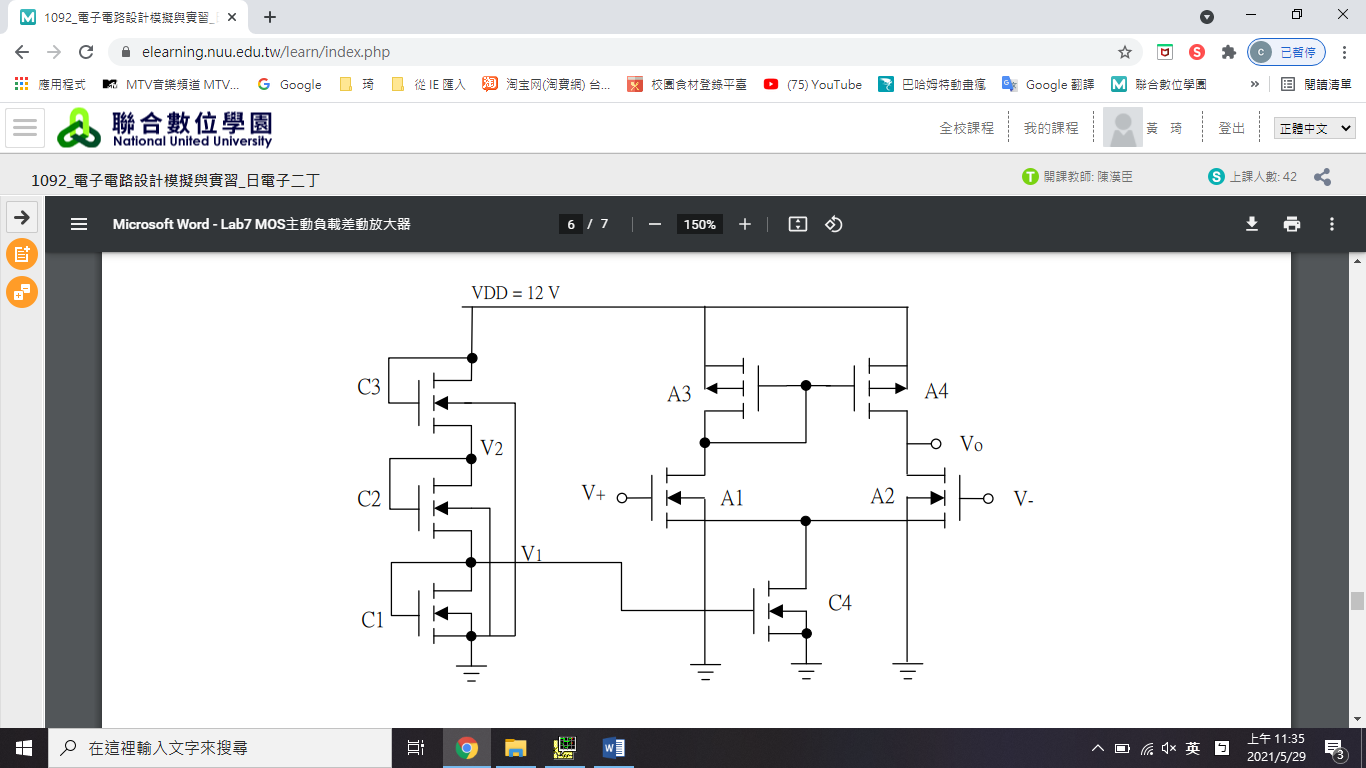
林雅晴 U0722045

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1. **CMOS主動負載差動放大器設計**

**Lab 7-1.** 試設計一主動負載 CMOS 差動放大器

實驗電路圖：



**5**

**4**

**3**

**2**

**1**

1. 電晶體參數值

|  |  |
| --- | --- |
|  |  |
| 1.073μ | 10.43μ |

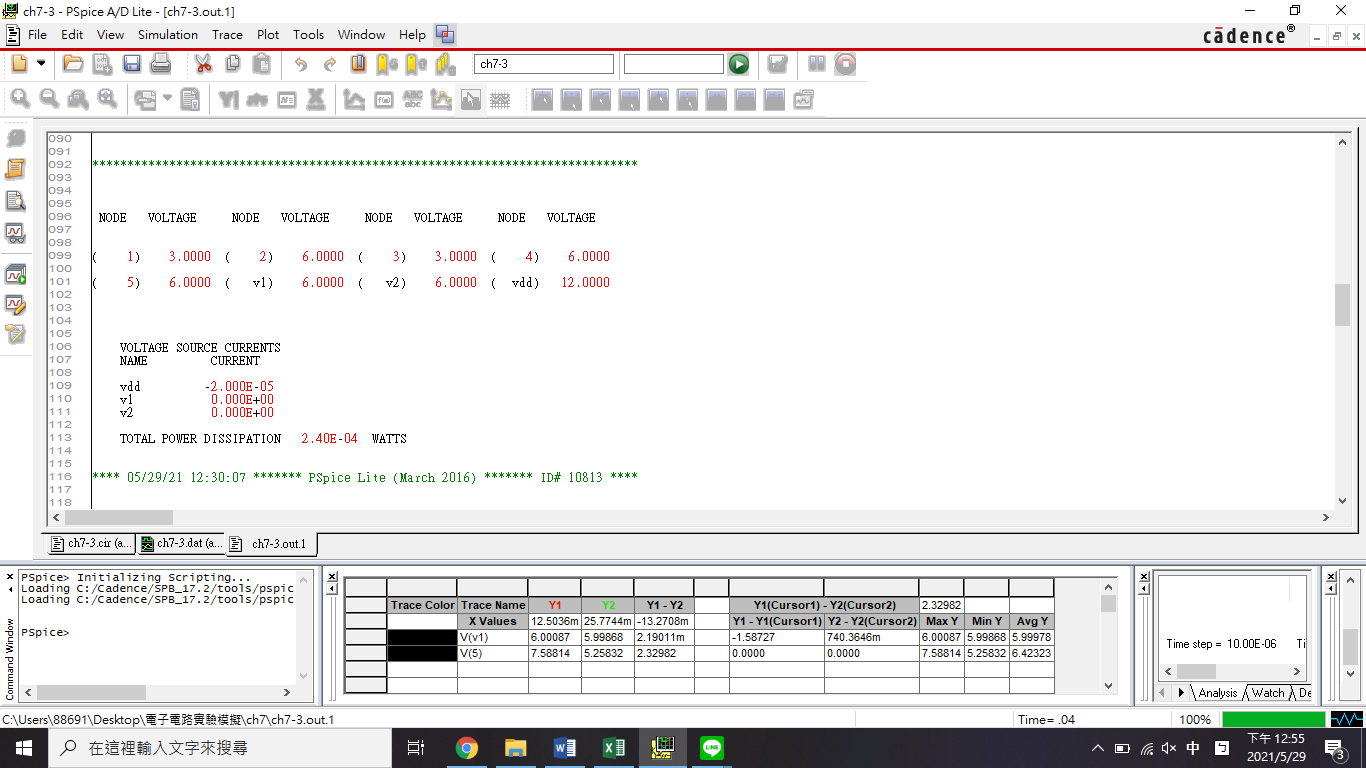
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |
| 1.73 | 1.73 | 1.73 | 1.73 | 1.73 | 1.73 | -3.533 | -3.533 |

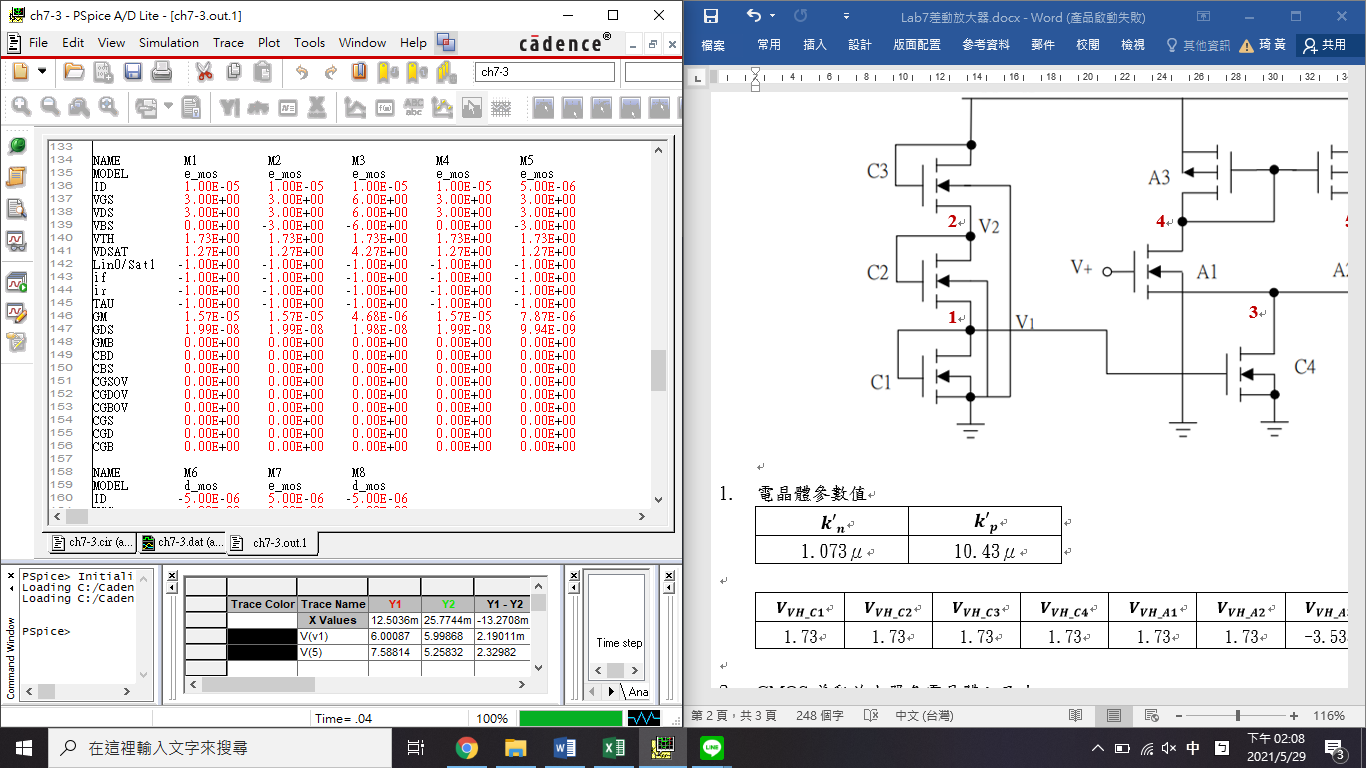
1. CMOS差動放大器各電晶體之尺寸

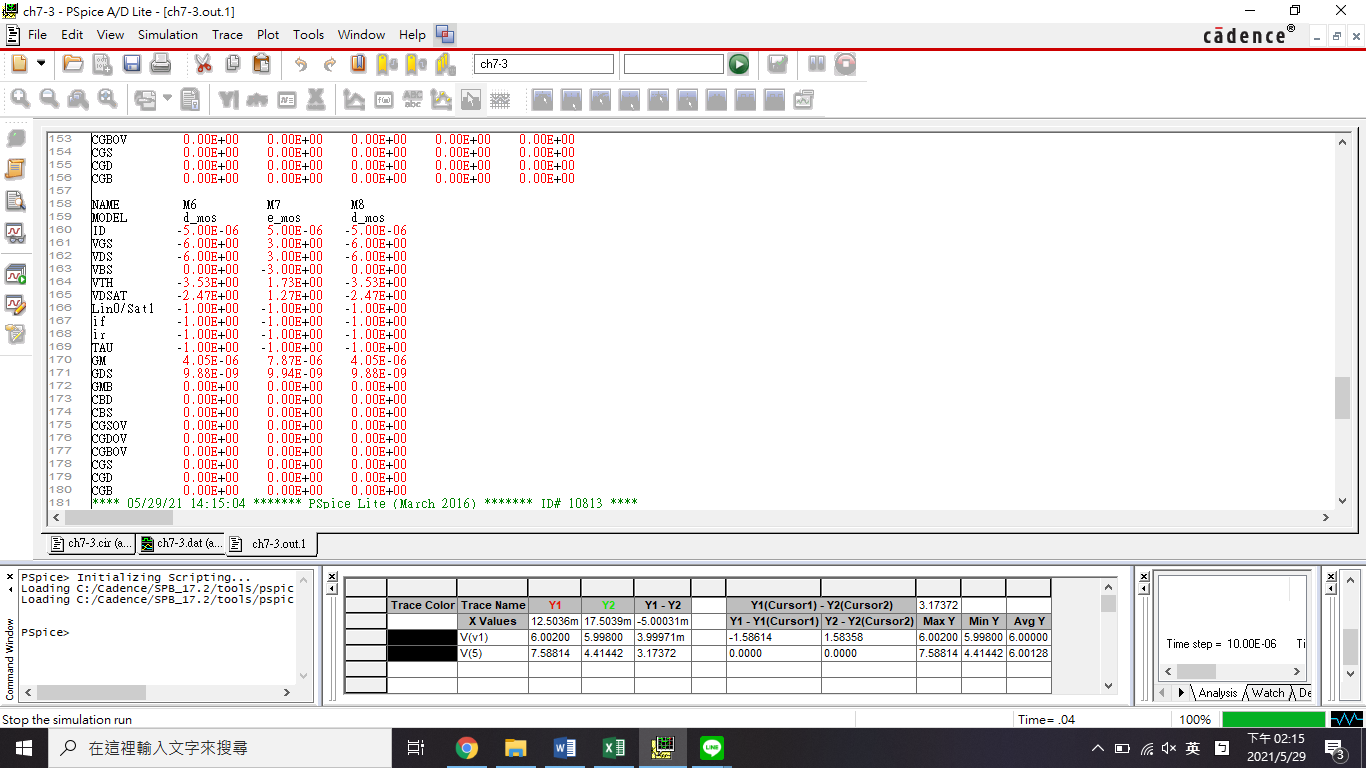
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |
| 11.48748 | 11.48748 | 1.01017 | 11.48748 | 5.74374 | 5.74374 | 0.15567 | 0.15567 |

1. CMOS差動放大器之直流工作點模擬值

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| **理論值**  **(設計規格)** | **3** | **6** | **3** | **6** | **6** | **10μ** |
| **模擬值** | 3 | 6 | 3 | 6 | 6 | 10μ |







1. CMOS差動放大器各參數之模擬值

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | **CMRR(1)** |  |  | **最大輸出電壓擺幅(swing)** |  |
| **理論值** | -393.7 | 2.4508m | 104.117 | 7.73 | 4.27 | 5.263 | 50.45M |
| **模擬值** | -397.1 | 2.3844m | 104.43 | 7.73 | 4.27 | 5.31358 | 50.47M |

