

# Effect of Capped Cu Layer on Protrusion Behaviors of Through Silicon via Copper (TSV-Cu) Under Double Annealing Conditions: Comparative Study

Min Zhang, Fei Qin<sup>✉</sup>, Si Chen<sup>✉</sup>, Yanwei Dai<sup>✉</sup>, Yifan Jin, Pei Chen<sup>✉</sup>, Tong An<sup>✉</sup>, and Yanpeng Gong

**Abstract**—Annealing process is generally adopted to reduce the residual stress and stabilize the microstructure of TSV-Cu in IC manufacturing. In this paper, the effects of capped Cu layer on the protrusion behaviors of TSV-Cu are investigated considering various double annealing processes. Higher protrusions of TSV-Cu with capped Cu layer are observed compared with that of TSV-Cu without capped Cu layer. The reason is that capped Cu layer impedes the elimination of grain boundaries and local misorientation during the first annealing, resulting in the remaining of larger amounts of atoms and higher energy in the grain boundaries. Thus, it is easier to induce protrusion by grain boundary migration during the second annealing. In addition, the capped Cu layer effects on mechanical properties of TSV-Cu under various double annealing conditions are investigated by nanoindentation test. The values of elastic modulus and hardness are generally higher in the presence of capped Cu layer. The reason is also discussed and clarified.

**Index Terms**—Through silicon via copper (TSV-Cu), capped Cu layer, protrusion, double annealing, microstructure, mechanical properties.

## I. INTRODUCTION

THREE-DIMENSIONAL (3D) packaging has been regarded as a promising approach to extend Moore's law, which is the basis of multifunctional integration technologies [1]. Copper (Cu) filled through silicon via (TSV-Cu) technology is very crucial to 3D integrated circuit (IC) as it provides shortest electrical path, lowest signal loss, smaller form factor and less weight [2], [3], [4]. However, due to unstable microstructure of Cu grain and accumulation of residual stress during various manufacturing and thermal interconnection processes, protrusion of TSV-Cu is still

Manuscript received 30 August 2022; revised 20 December 2022; accepted 22 December 2022. Date of publication 26 December 2022; date of current version 8 March 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 11672009 and Grant 61804032, and in part by the Innovation and Entrepreneurship Leading Team Zengcheng under Grant 202102001. (Corresponding authors: Fei Qin; Yanwei Dai.)

Min Zhang, Fei Qin, Yanwei Dai, Pei Chen, Tong An, and Yanpeng Gong are with the Institute of Electronics Packaging Technology and Reliability, Faculty of Materials and Manufacturing, Beijing University of Technology, Beijing 100124, China (e-mail: qfei@bjut.edu.cn; ywdai@bjut.edu.cn).

Si Chen is with the Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, China Electronic Product Reliability and Environmental Testing Research Institute, Guangzhou 510610, China.

Yifan Jin is with the Aerospace Internet of Things Technology Company Ltd, Beijing 100124, China.

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TDMR.2022.3232128>.

Digital Object Identifier 10.1109/TDMR.2022.3232128

one of the biggest issues, which can lead to failures of the back-end-of-line (BEOL) interconnected layers [5], [6], [7], [8], [9], [10], [11], [12], [13]. Recently, the relative investigations of TSV protrusion are focused on two aspects. One is how to control the protrusions by developing electroplating solution, the another is to reveal the protrusion mechanisms at microscopic or even atomic scale by simulations [7], [14], [15], [16], [17], [18]. It is noted that capped Cu layer is formed by excessively electroplating Cu on the surface of TSV-Cu and silicon (Si) substrate during TSV-Cu electroplating process, during which initial residual stresses could be accumulated in the TSV-Cu [19], [20]. To relieve the residual stress and stabilize the microstructure of TSV-Cu, annealing treatment is always adopted. Some announced studies have shown that the microstructure of TSV-Cu and the stress relief behaviors can be influenced by the capped Cu layer during the thermal annealing treatment process [20], [21]. However, influences of capped Cu layer on protrusion behaviors and microstructure evolution of TSV-Cu during thermal annealing processes are still not investigated thoroughly.

It was clarified by experimental studies that annealing of TSV wafer with capped Cu layer generated stronger warpages and stresses, while the reduction of total grain boundary lengths for TSV-Cu with capped layer was lower than that of uncapped TSV-Cu after annealing treatment [22]. It was also found that annealing of TSV samples with capped Cu layer at 400 °C can mitigate TSV-Cu protrusion behaviors during BEOL processes, however, Cu voids were inevitably induced [19], [23]. Finite element analysis indicated that protrusions of TSV-Cu with capped Cu layer during annealing was reduced compared with that of without capped Cu layer [24]. Other metallic capped layers deposited on the surface of TSV-Cu such like Co, W and Ta layers were also found to suppress protrusions of TSV-Cu under annealing process [25]. The reason was that those capped layers restrained the mass transport at top surface of the vias and along grain boundaries. However, the relation between TSV-Cu protrusion behavior and capped Cu layer is not thoroughly elaborated. Moreover, the first protrusion of TSV-Cu including the capped layer will be generally removed by chemical mechanical polishing (CMP) to conduct subsequent manufacturing process of interconnection layers. The thermal loading caused by subsequent manufacturing processes of interconnection and metallization layers could introduce continuous TSV-Cu protrusions, leading to delamination failure or cracking of interconnection layers [26], [27].

Hence, it is vital to evaluate whether the second protrusion will occur under additional thermal loading before subsequent manufacturing processes.

Investigations showed that plastic deformation, sliding and fracture of Cu/Si interface all can lead to TSV-Cu protrusion [28], which can be as well influenced by the etched shape of Si via, dielectric material, TSV geometrical dimension, electroplating solution and annealing process etc. Rough side wall of Si via generated higher stress, resulting in more TSV-Cu protrusions and failures of Cu/Si interface [29]. The materials of dielectric layers such as insulators and barriers can be optimized to minimize the thermal stress and eliminate the TSV-Cu protrusion [30], [31]. The effect of geometrical dimension of TSV-Cu on protrusions indicated that smaller pitch distance and larger diameter induced more protrusion height [32], [33]. In addition, electroplating current density and electrolyte composition also affected the microstructure of TSV-Cu, while the protrusion height was considered as a function of grain size of TSV-Cu according to [34], [35], [36]. Those investigations have confirmed that microstructure and residual stress are the two main indicators influencing the protrusions of TSV-Cu. Although tremendous efforts have been made to study the protrusion mechanisms of TSV-Cu from different aspects, the effect of capped Cu layer on TSV-Cu protrusion is always ignored and additional thermal test is still lacked to validate subsequent protrusion behavior in those investigations.

In addition, due to involving multiple thermal processes during the TSV integration, it is meaningful to connect the variations of mechanical properties for TSV-Cu with numbers of annealing processes. Although the microstructure and mechanical properties of TSV-Cu under once annealing temperature have been studied [37], [38], [39], [40], it is insufficient to assess the thermal mechanical reliabilities during entire TSV integration processes. With this consideration, the effect of capped Cu layer on microstructure and mechanical performance of TSV-Cu under different double annealing conditions will be analyzed.

The target of this paper is to study whether capped Cu layer can alleviate the protrusion behaviors of TSV-Cu under subsequent multistep annealing treatments by comparing various annealing conditions. Toward this target, TSV-Cu samples with or without capped Cu layer are annealed under the first annealing conditions. Then, the second annealing treatments are performed to validate their subsequent protrusion behaviors. Herein, the protrusions, microstructure and mechanical properties of TSV-Cu samples with capped Cu layer are characterized and compared with the results of uncapped TSV-Cu samples. Furthermore, the influencing mechanism of capped Cu layer is presented, and some guidelines are provided to understand capped layer effect on TSV protrusions under double annealing.

## II. EXPERIMENTAL PROCEDURE

### A. Sample Fabrication

Fig. 1(a) shows the schematic diagrams of capped TSV samples. The pitch distances along  $x$ -axis and  $y$ -axis are 115  $\mu\text{m}$  and 165  $\mu\text{m}$ , respectively. The depth and diameter

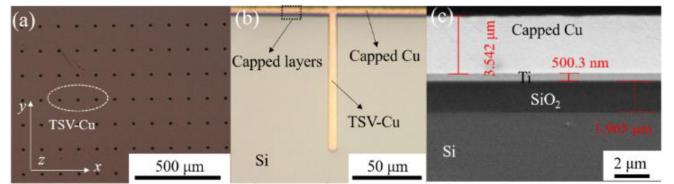


Fig. 1. Schematic diagrams of capped TSV sample: (a) TSV arrays, (b) Cross-section of capped TSV-Cu, (c) Thicknesses of capped layers over the silicon substrate.

of TSVs are 100  $\mu\text{m}$  and 10  $\mu\text{m}$ , respectively. During the manufacturing of the capped TSV-Cu, bind vias were firstly etched by deep reactive ion etching (DRIE) on a 12-inch Si wafer with the thickness of 800  $\mu\text{m}$ . Then,  $\text{SiO}_2$  insulator was deposited on these etched vias by chemical vapor deposition (CVD). After that, Ti based diffusion barrier and Cu seed layer were deposited on the sidewall of the vias by physical vapor deposition (PVD). Lastly, the vias were filled by Cu electroplating. As shown in Fig. 1(b), large amounts of capped Cu layer and tiny amounts of  $\text{SiO}_2$  insulator and Ti diffusion barrier unavoidably remained on the Si surface during the manufacturing processes. As shown from Fig. 1(c), the thicknesses of capped Cu, Ti barrier layer, and  $\text{SiO}_2$  insulator layer, are approximately 3.5  $\mu\text{m}$ , 500 nm and 2  $\mu\text{m}$ , respectively.

### B. Method of Protrusion Measurement Under Double Annealing Conditions

Fig. 2(a) shows the double annealing process of capped TSV-Cu and uncapped TSV-Cu. Herein, the capped Cu layers were removed by CMP to prepare the uncapped TSV-Cu samples. The manufacturing processes, geometric dimensions, and annealing conditions are the same between the capped TSV-Cu and uncapped TSV-Cu. The difference between capped TSV-Cu and uncapped TSV-Cu is the existence of the capped Cu or not. Three temperatures (i.e., 200 °C, 300 °C and 400 °C) were firstly adopted to anneal the capped TSV-Cu samples in a vacuum furnace (TL 1200). As a reference, the annealing of uncapped TSV-Cu samples was performed at the same conditions. Then, the first protrusions including capped Cu layer of the two kinds of samples were removed by CMP. To examine the annealing effect of the capped and uncapped TSV-Cu, a second annealing was further conducted on these two kinds of annealed TSV-Cu, and the second protrusions were measured. The second annealing temperatures were also set as 200 °C, 300 °C and 400 °C, respectively. The double annealing temperatures are given in TABLE I. The temperatures of the twice annealing processes raised from room temperature to the final target temperature at 10 °C/min and maintained for 30 mins, then cooled down naturally. The descriptions of double annealing conditions are denoted by the symbols ( $A_i$ ,  $B_i$ ,  $C_i$ ,  $i=1, 2, 3$ ). Characters  $A$ ,  $B$  and  $C$  represent the first annealing temperatures, i.e., 200 °C, 300 °C and 400 °C, while subscripts  $i=1, 2, 3$  represent the second annealing temperature, i.e., 200 °C, 300 °C and 400 °C. For example, double annealing condition  $A_1$  represents that the sample is annealed firstly at 200 °C, then annealed secondly at 200 °C.

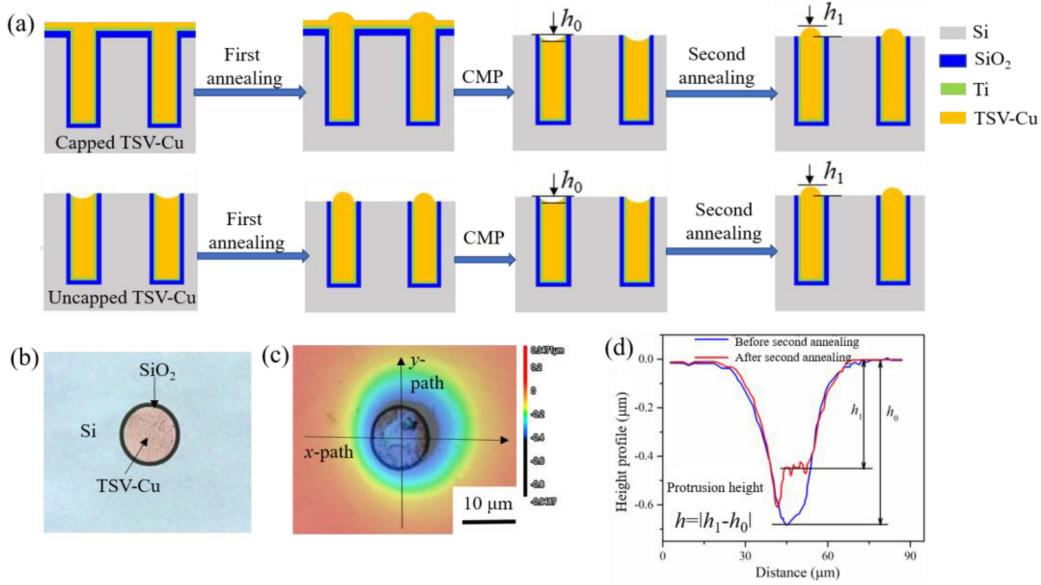


Fig. 2. Double annealing processes and protrusion measurement of capped and uncapped TSV-Cu samples: (a) Double annealing processes of capped TSV-Cu and uncapped TSV-Cu, (b) The polished surface, (c) 3D profile of TSV-Cu surface after CMP, (d) Height profile along  $x$ -path of TSV-Cu before and after second annealing.

TABLE I  
DOUBLE ANNEALING TEMPERATURES

Sample	First annealing temperature	Second annealing temperature	Symbols of conditions
Capped or uncapped TSV-Cu	200°C	200°C	$A_1$
	200°C	300°C	$A_2$
	200°C	400°C	$A_3$
	300°C	200°C	$B_1$
	300°C	300°C	$B_2$
	300°C	400°C	$B_3$
	400°C	200°C	$C_1$
	400°C	300°C	$C_2$
	400°C	400°C	$C_3$

As shown in Fig. 2(a), initial dents formed on the top surface of TSV-Cu after CMP due to higher removal rate of Cu than Si material. The polished surface of TSV-Cu is shown in Fig. 2(b). As shown from Fig. 2(c), the initial depths of the dents on the surface were measured by 3D laser scanning microscope (KEYENCE X200 series, measuring precision 12 nm).  $h_0$  is the average value of the depths along  $x$ -path and  $y$ -path. After second annealing, the second protrusion height  $h_1$  was also measured. As shown in Fig. 2(d), the absolute value,  $h = |h_1 - h_0|$ , is the actual protrusion height value of TSV-Cu. In order to obtain precise protrusion value,  $h_0$  and  $h_1$  were measured from a same Cu via, and at least five TSV-Cu vias of each sample were measured for each annealing condition. The final protrusion height value was calculated by averaging  $h$  of total Cu vias.

### C. Methodology of Microstructural and Mechanical Property Characterization

Focused ion beam scanning electron microscopy system (FIB-SEM) with an EBSD detector (Oxford “symmetry”) was

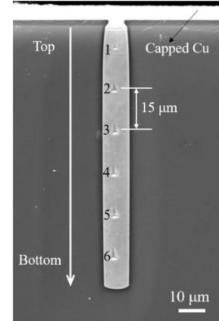


Fig. 3. SEM images of six indentation testing points on the cross-section of capped TSV-Cu.

used to analyze the microstructure of the capped TSV-Cu under various double annealing conditions. In order to acquire high-quality cross-section of TSV-Cu, ion milling method (Leica EM TIC 3X) was performed to remove the residual stress in the cross-section of TSV-Cu. The ion milling was operated for 25 min at 6 kV, then kept 15 min at 4 kV. After that, EBSD scanning was performed on the cross-section of capped TSV-Cu. The scanning voltage, incident beam current, and the scanning step were 20 kV, 5.5 nA, and 0.15 μm, respectively. The sample stage was inclined 70° from the horizontal direction to increase the resolution of EBSD pattern. Channel 5 software was utilized to analyze the EBSD data, including grain size, grain boundaries and local misorientation.

The elastic modulus ( $E$ ) and hardness ( $H$ ) in cross-sections of capped TSV-Cu under various double annealing conditions were measured by nanoindentation test (Agilent G200). Standard three-sided pyramid diamond indenter tip (Berkovitch) and continuous stiffness measurement (CSM) method were used during the tests.

As shown in Fig. 3, due to different constraints and inhomogeneous microstructure from the top to the bottom of the

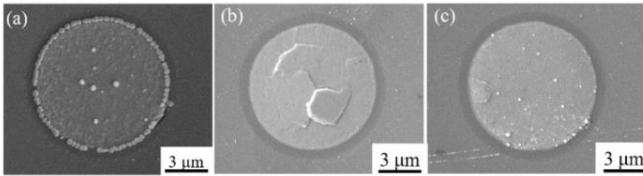


Fig. 4. SEM images of protrusion morphology of capped TSV-Cu after double annealing: (a) Edge protrusion, (b) Center protrusion, (c) Global protrusion.

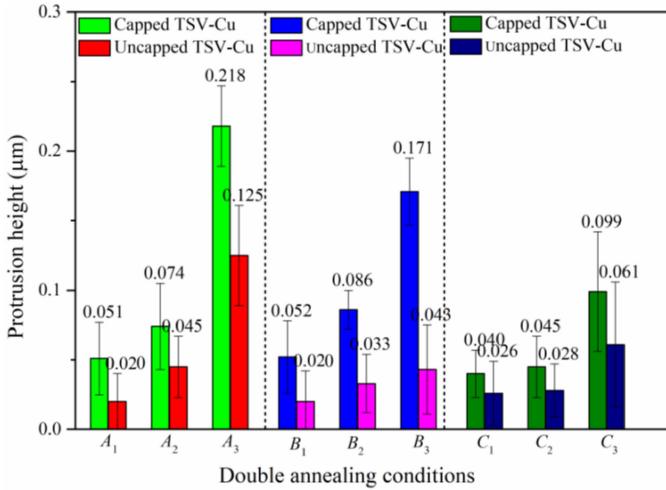


Fig. 5. The protrusion heights of capped and uncapped TSV-Cu after double annealing.

capped TSV-Cu, the mechanical properties could vary with nanoindentation testing positions in TSV-Cu cross-section. In order to study the effects of testing positions on mechanical properties, six indentation testing points with a spacing size of 15 μm were carried out on the cross-section of capped TSV-Cu. The constant strain rate was set as 0.05 s<sup>-1</sup>, and the maximum indentation depth was set as 500 nm. From the obtained load-displacement curves, the *E* and *H* can be calculated based on the Oliver-Pharr method.

### III. RESULTS

#### A. Protrusion Statistics of Capped TSV-Cu Under Double Annealing

Fig. 4 shows three kinds of main protrusion morphologies of capped TSV-Cu after double annealing treatments, i.e., edge protrusion, center protrusion and global protrusion, respectively. Formation mechanisms of different protrusion morphologies are related to its microstructures [34].

It is worth noting that the protrusion heights of uncapped TSV-Cu under various double annealing conditions have been given in our recent investigations [41]. Herein, the comparisons of protrusion heights between the capped and uncapped TSV-Cu are shown in Fig. 5. It can be found that the protrusion tendencies of the two kinds of samples are consistent, i.e., the protrusion height improves with the increasing of the second annealing temperature. However, the protrusion height of capped TSV-Cu is higher than that of uncapped TSV-Cu under

TABLE II  
FRACTIONS OF GRAINS WITH DIFFERENT DIAMETERS

Annealing conditions	Average grain size <i>d</i> (μm)	Fraction of grain size distribution		
		Small ( <i>d</i> <1 μm)	Median (1 μm< <i>d</i> <4 μm)	Large ( <i>d</i> >4 μm)
200 °C	1.67	0.608	0.266	0.126
300 °C	2.07	0.559	0.243	0.198
400 °C	2.30	0.508	0.310	0.182
200 °C+200 °C	1.79	0.549	0.351	0.100
200 °C+300 °C	2.05	0.377	0.377	0.246
200 °C+400 °C	2.35	0.217	0.520	0.263
300 °C+200 °C	2.20	0.436	0.325	0.239
300 °C+300 °C	2.37	0.250	0.400	0.350
300 °C+400 °C	2.49	0.150	0.514	0.336
400 °C+200 °C	2.94	0.428	0.287	0.285
400 °C+300 °C	3.12	0.246	0.329	0.425
400 °C+400 °C	3.30	0.176	0.587	0.237

the same double annealing conditions. In addition, the difference of protrusion height is limited within 40 nm if the first annealing temperature is as high as 400 °C. It illustrates that the annealing treatment of TSV-Cu with capped Cu layer promotes protrusion behaviors compared with those of uncapped samples for the second annealing treatment. However, the promoting effect weakens if the first annealing temperature is relative higher.

#### B. Microstructure Statistics of Capped TSV-Cu Under Double Annealing

Figs. 6 (a)-(b) show the EBSD maps along Y direction for capped TSV-Cu after first and second annealing processes. It can be seen that orientations of <111> and <110> are the dominant orientations, which are related to the types of electroplating additive, orientations of Cu seed layer and electroplating current [16], [35], [42]. In addition, the irregular shaped grains in the side wall coalesce with large grains in the center region to be larger equiaxed grains. The cross-section of TSV-Cu is mainly filled by these larger grains with <111> and <110> orientations.

The grains are categorized as small, median and large grains according to diameters of grain (*d*), i.e., *d*<1 μm, 1 μm<*d*<4 μm, and *d*>4 μm, respectively. The average grain size and fractions of various grain sizes are listed in TABLE II. During the first annealing process, the average grain size increases from 1.67 μm to 2.30 μm with annealing temperature raising. The main reason is due to that the fraction of small grains decreases and the fraction of large or median grains increases. With increasing the temperature of the second annealing process, the average grain size increases from 1.79 μm to 2.35 μm under the condition that the first annealing treatment temperature is 200 °C. The average grain size increases from 2.20 μm to 2.49 μm under the condition that the first annealing treatment temperature is 300 °C. The average grain size increases from 2.94 μm to 3.30 μm if the first annealing temperature is 400 °C. The increasing of average grain sizes under second annealing can be also explained by the variations of grain fractions of grain sizes.

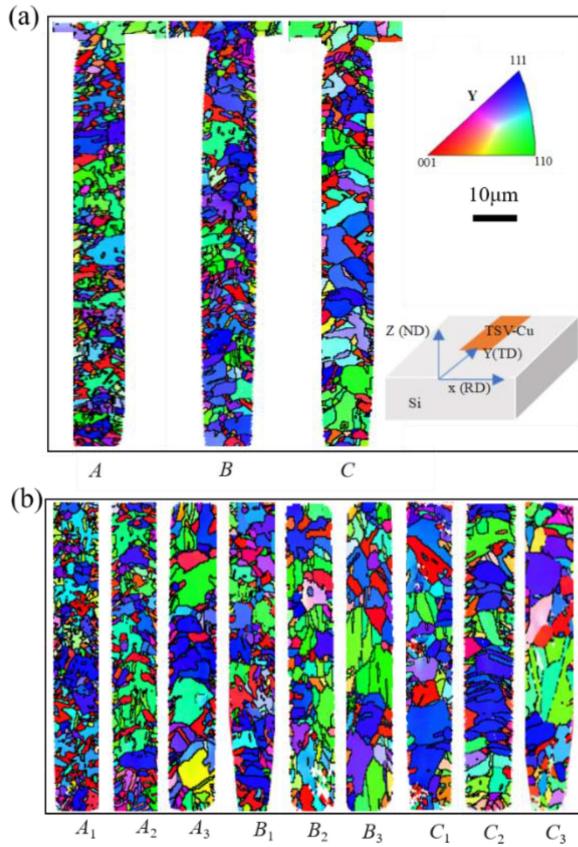


Fig. 6. EBSD maps of capped TSV-Cu under different annealing conditions: (a) After first annealing, (b) After second annealing.

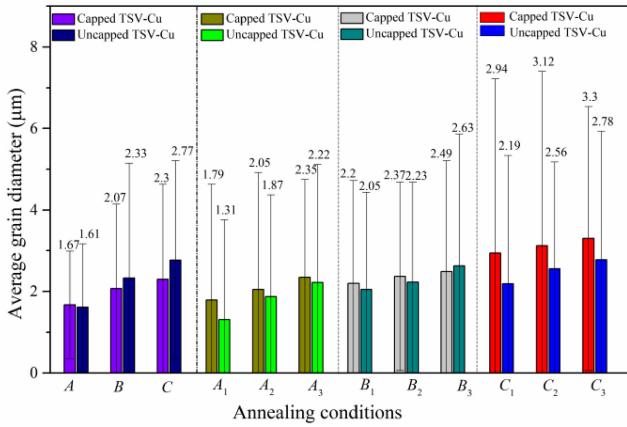


Fig. 7. Comparison of average grain size between capped and uncapped TSV-Cu under different annealing conditions.

In order to investigate the capped Cu layer effect on the average grain size considering various annealing conditions, the comparison of average grain sizes for capped and uncapped TSV-Cu is given in Fig. 7. It can be seen that the average grain sizes of capped TSV-Cu and uncapped TSV-Cu enlarge with the improvement of the annealing temperature regardless of annealing temperature sequences. In addition, the grain sizes are nearly similar under the conditions that the first annealing temperature is 200 °C, however the grain size of capped TSV-Cu is slightly smaller than that of uncapped TSV-Cu along

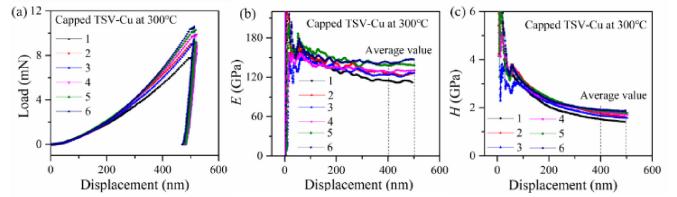


Fig. 8. Nanoindentation responses of six indentation testing points in cross-section for capped TSV-Cu annealing at 300 °C: (a) Load-displacement curves, (b)  $E$ -displacement curves, (c)  $H$ -displacement curves.

with that the first annealing temperature increases to 300 °C or 400 °C. On the contrary, the grain size of capped TSV-Cu is generally larger than that of uncapped samples even under the same double annealing conditions.

### C. Mechanical Properties of Capped TSV-Cu Under Double Annealing

Nanoindentation responses of the six testing points under each annealing condition are closely related with the testing positions in cross-section of capped TSV-Cu. For example, the representative nanoindentation responses at 300 °C are shown in Fig. 8. From Fig. 8(a), the maximum load at the deepest displacement varies accordingly with different testing indentation points. Therefore, Young's modulus  $E$  versus displacement curves and hardness  $H$  versus displacement curves display significantly discrepancies at different testing points, which are shown in Fig. 8(b)-(c). The results indicate that the mechanical properties of TSV-Cu are influenced by the indentation positions in cross-section of capped TSV-Cu. In addition, the values of Young's modulus  $E$  and hardness  $H$  are stable within 400 nm - 500 nm. Hence, the average values of Young's modulus  $E$  and hardness  $H$  for each indentation testing points are calculated by averaging their values within 400 - 500 nm.

Fig. 9(a) shows the average  $E$  of each indentation point in cross-section for capped TSV-Cu under various annealing conditions, the values of  $E$  exhibit an increasing tendency from the top region of TSV-Cu to its bottom region. Fig. 9(b) shows the average  $H$  in cross-section, the values of  $H$  generally improve from the top region of TSV-Cu to its bottom region. The distribution laws of mechanical properties could be related to the inhomogeneous residual stress in cross-section [5].

The average  $E$  and  $H$  of the total six indentation points for capped and uncapped TSV-Cu are compared in Fig. 10. Fig. 10(a) shows that average Young's modulus of capped TSV-Cu is generally larger than that of uncapped TSV-Cu under various annealing conditions. While Fig. 10(b) presents that the average hardness of capped TSV-Cu is also generally larger than that of uncapped TSV-Cu.

## IV. DISCUSSIONS

### A. Grain Boundary Effect on TSV-Cu Protrusions

Grain boundaries are the sources of defects, which are the main factors influencing the protrusions of TSV-Cu by the migration of grain boundary under thermal annealing. Coincident site lattice (CSL) grain boundaries, i.e.,  $\Sigma 3$ ,  $\Sigma 9$ ,  $\Sigma 27a$  and  $\Sigma 27b$ , are desirable twin boundary types with

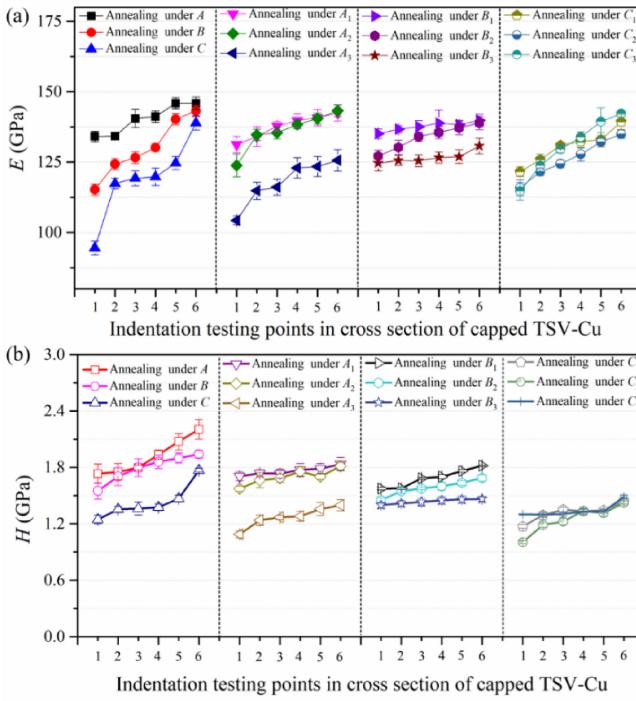


Fig. 9.  $E$  and  $H$  of six testing points in cross-section for capped TSV-Cu under different annealing conditions: (a)  $E$  under various annealing conditions, (b)  $H$  under various annealing conditions.

specific misorientation angle. These twin boundaries are more difficult to induce intergranular cracking, corrosion and plastic deformation, since they possess lower energy and lower mobility than other random lager angle grain boundaries [43]. Herein, grain boundary characteristics of the top region for TSV-Cu are investigated since the protrusion of TSV-Cu is mainly influenced by its top crystal structure. Figs. 11(a-c) show the CSL grain boundaries of capped and uncapped TSV-Cu after first annealing, the  $\Sigma 3$  (denoted by red line) is the most frequent. The specific fractions of different CSL grain boundaries are presented in Fig. 11(d). The fractions of  $\Sigma 3$  are approximately 60%, and the fractions of  $\Sigma 9$  (denoted by blue line) are about 10%. The fractions of  $\Sigma 27a$  (denoted by yellow line) and  $\Sigma 27b$  (denoted by green line) are within 5%. Moreover, the capped Cu layer and annealing temperatures have a trivial influence on the fractions of CSL grain boundaries.

As shown from Fig. 12(a), The HAGBs with misorientation angle larger than  $15^\circ$  are the dominant grain boundary type, and the fractions of HAGBs are above 95%. Moreover, the fractions of misorientation angle vary slightly regardless of the annealing temperatures and the presence of capped Cu layer. The similar phenomenon was also observed that grain orientations had a slight change under different annealing temperatures [6], [37], [39]. The reason is that the misorientation angle of TSV-Cu grain is mainly dependent on the electroplating processes, such as electroplating current, electrolyte composition, and the orientation of copper seed layer [16], [20], [38]. As a consequence, the fractions of  $\Sigma 3$  ( $60^\circ <111>$ ),  $\Sigma 9$  ( $38.94^\circ <110>$ ),  $\Sigma 27a$  ( $31.58^\circ <110>$ ) and  $\Sigma 27b$  ( $35.42^\circ <210>$ ) vary slightly. In addition, the total

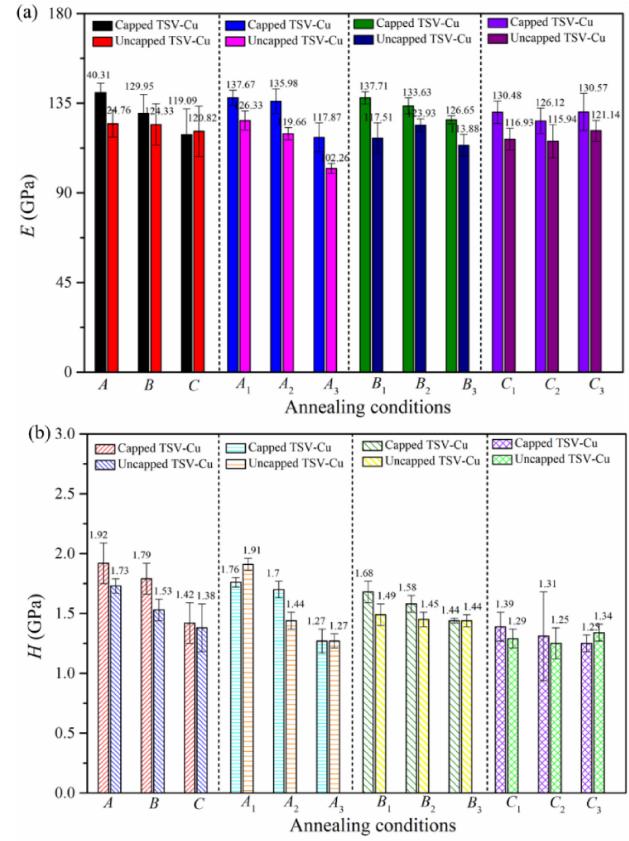


Fig. 10. Comparison of average  $E$  and  $H$  of total testing points between capped and uncapped TSV-Cu under different annealing conditions: (a) Comparison of average  $E$ , (b) Comparison of average  $H$ .

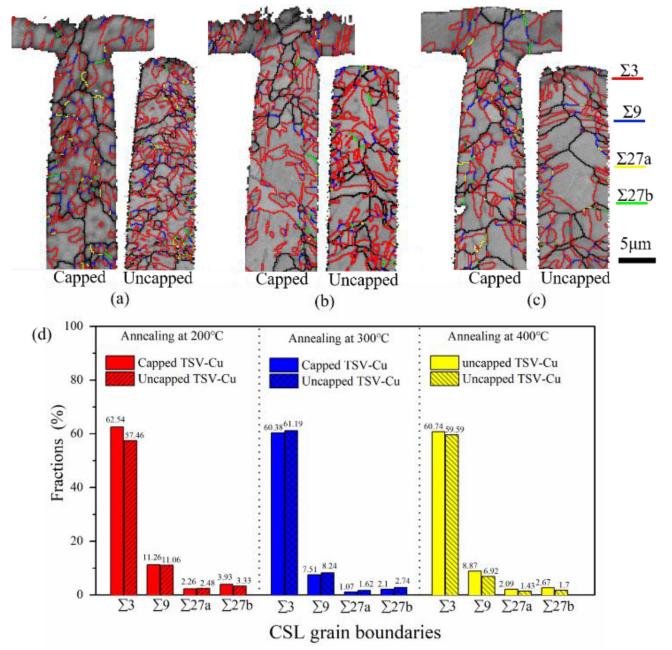


Fig. 11. Grain boundary maps of capped and uncapped TSV-Cu after first annealing, (a) Annealing at 200°C, (b) Annealing at 300°C, (c) Annealing at 400°C, (d) Fractions of different CSL grain boundaries.

lengths of grain boundaries are further analyzed, which are recorded by Image Pro software. As shown in Fig. 12 (b), the total lengths of grain boundaries for both capped and uncapped

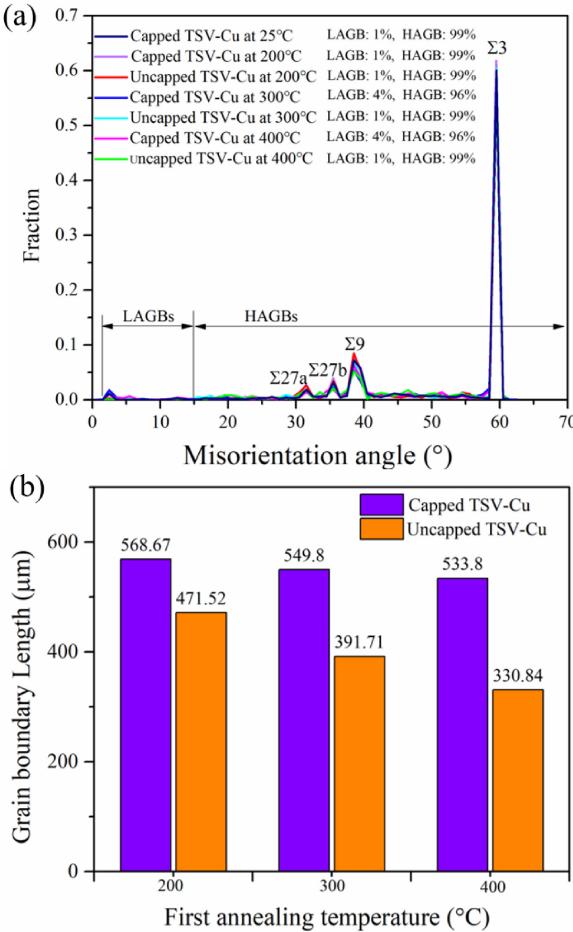


Fig. 12. Grain boundary information of capped and uncapped TSV-Cu after first annealing: (a) Fraction of misorientation angle distributions, (b) Grain boundary length.

TSV-Cu decrease with the increasing of annealing temperature due to grain growth. However, the reduction of grain boundary lengths for uncapped TSV-Cu is more remarkably than capped TSV-Cu. Besides, the grain boundary lengths of capped TSV-Cu are larger than that of uncapped TSV-Cu, indicating the remaining of larger amounts of defect sources in capped TSV-Cu after the first annealing treatment. Hence, capped TSV-Cu possesses more atoms in grain boundaries to migrate, therefore easier to protrude again compared with uncapped TSV-Cu during the second annealing.

#### B. Local Misorientation Effect on Protrusions

The local misorientation reflects the distribution of micro strain or dislocation density inside grains. Generally, the high level of micro strain or dislocation density make grains in a nonequilibrium thermodynamics state, therefore the grains can deform easily under additional thermal loading. Fig. 13(a) shows that high density of local misorientation exists in capped TSV-Cu fabricated at 25 °C. It indicates that large amounts initial micro strain or dislocation defects generate in the TSV-Cu electroplating. The local misorientation maps of capped and uncapped TSV-Cu are shown in Fig. 13(b-d). It can be

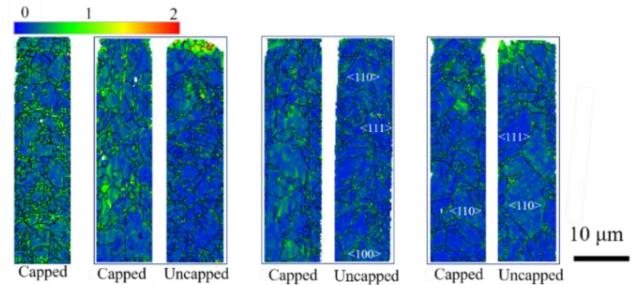


Fig. 13. Local misorientation maps of capped and uncapped TSV-Cu after first annealing: (a) As fabricated at 25 °C, (b) Annealing at 200 °C, (c) Annealing at 300 °C, (d) Annealing at 400 °C.

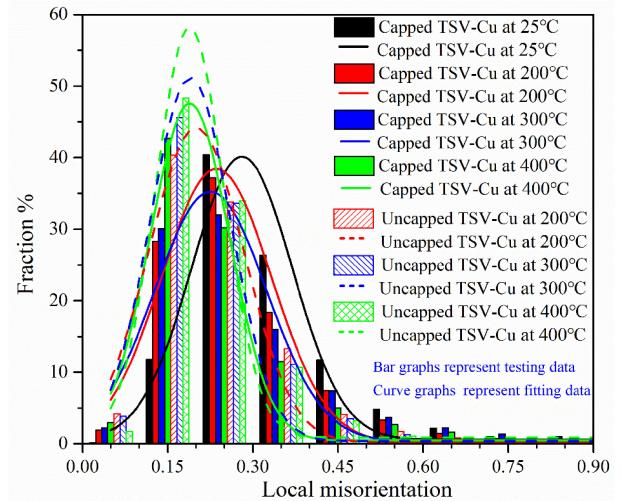


Fig. 14. Local misorientation distribution of capped and uncapped TSV-Cu after first annealing.

TABLE III  
VALUES OF KAM AFTER FIRST ANNEALING

Annealing temperature	Capped TSV-Cu	Uncapped TSV-Cu
25°C	0.281	
200°C	0.231	0.203
300°C	0.221	1.191
400°C	0.189	0.188

seen that initial micro strain are reduced significantly after annealing at 200 °C, 300 °C and 400 °C.

In order to qualitatively compare the difference of the local misorientation for capped and uncapped TSV-Cu after first annealing, Fig. 14 presents local misorientation distribution with Gauss fitting. The fraction of local misorientation value (larger than 0.25°) is the highest in capped sample at 25°C. Kernel average misorientation (KAM) after first annealing is listed in TABLE III. The KAM values for the two kinds of samples decrease with the increasing of annealing temperature. However, the KAM value of uncapped TSV-Cu is smaller than that of the capped TSV-Cu under each same annealing temperature. Furthermore, the difference of KAM values between capped samples and uncapped samples shrinks as the first annealing temperature increases. Hence, it can be inferred that the presence of capped Cu layer hinders the

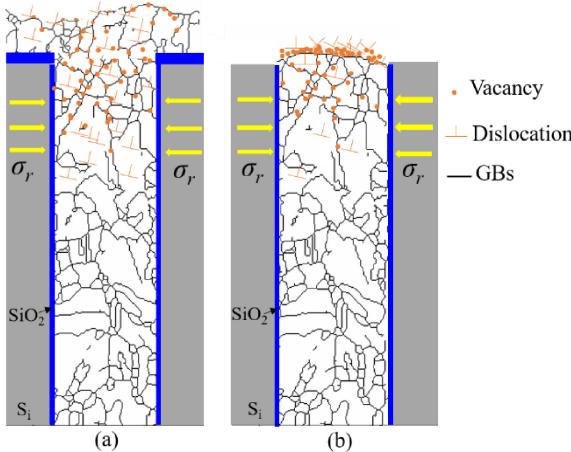


Fig. 15. Schematic illustration of diffusional mass transport in TSV-Cu during first annealing, (a) Capped TSV-Cu, (b) Uncapped TSV-Cu.

elimination of micro strain of capped TSV-Cu during first annealing. As a result, micro strain in the grains of uncapped TSV-Cu is relieved more fully than capped TSV-Cu, enabling the uncapped TSV-Cu more stable and difficult to protrude under the same double annealing conditions.

### C. Influencing Mechanisms of Capped Cu Layer

The barrier mechanisms of the capped Cu layer on the elimination of grain boundary and local misorientation during first annealing can be illustrated by diffusional mass transport in TSV-Cu shown in Fig. 15. The diffusions of defects including vacancies, dislocations and GBs are partially suppressed for capped TSV-Cu due to the longer transport route of capped Cu layer in Fig. 15 (a). Diffusion creep is one of the main mechanisms of inducing TSV-Cu protrusion [34]. The hindering effect of capped layer results in less protrusion compared with uncapped sample during first annealing. This phenomenon has been confirmed both by experiments and finite element analysis [24], [25]. In engineering, however, the first protrusion, including the capped layer, will be removed by CMP for subsequent fabrication processes of interconnected layers. If the thermal loading involved in these processes leads to continuous protrusions of TSV-Cu, the reliabilities of these interconnect layers could be at a great risk. Experiments in this study indicate that second protrusion heights of capped samples still reach about 100 nm, even the capped samples went through twice annealing at 400 °C. Similar experimental observation was also reported [44]. The reason is that the unrelieved micro strain and plentiful of atoms in GBs still remain in the capped TSV-Cu after first annealing. It also provides the kinetic energy for the diffusional migration of GBs under the second annealing.

However, as for those uncapped samples, the vacancies and dislocations are fully released during first annealing, while the grain growth is more sufficient. Thus, the grains are in more stable state, leading to less protrusions under second annealing. Therefore, it is suggested that after removing the excessively electroplated Cu layer by CMP, high temperature annealing is carried out to make the TSV-Cu fully protruded and grains stabilized. Then, the protrusions are polished by CMP to finish

the subsequent processes of interconnected layers fabrication. Due to stable microstructure of TSV-Cu and the constraint of interconnect layers, the problem of continuous protrusions can be effectively controlled.

In addition, compressive stresses were generally accumulated in the initially electroplated samples, which led to the sample warpage [45], [46]. Annealing of samples with capped layer could lead to larger compressive stress and aggravate the original curvature of the warpage [47]. However, the curvature and stress decreased for uncapped samples after annealing [25]. Furthermore, it was confirmed that compressive stress resulted in the overestimation of elastic modulus and hardness. Instead, tensile stress could cause the underestimation of elastic modulus and hardness values based on nanoindentation test [10], [48]. In this study, the internal compressive stress of uncapped samples could be fully relieved and greatly decreased comparing with capped samples, which is the main reason resulting in the differences of mechanical properties between the two kinds of samples. Annealing temperature, grain size, grain orientation and voids also affect the measured values of elastic modulus [49], [50], [51]. However, these factors are generally the same for the two kinds of samples, which is not the main reason for the discrepancy.

### V. SUMMARY

In this paper, the effects of capped Cu layer on the protrusion behaviors, microstructure evolution and mechanical properties of TSV-Cu are investigated by experiments considering various double annealing processes. The influencing mechanisms of capped Cu on the experimental findings are analyzed and discussed. On the one hand, the presence of capped Cu partially suppresses the diffusional mass transport in TSV-Cu. Thus, the elimination of grain boundary and local misorientation inner TSV-Cu during first annealing is not sufficient for capped samples. Instead, the unrelieved micro strain and plentiful of atoms in GBs provide more kinetic energy than uncapped samples for the diffusional migration of GBs under the second annealing. This is the reason that protrusion height of capped TSV-Cu is higher than that of uncapped TSV-Cu even under same double annealing conditions. On the other hand, the confinement of capped Cu layer restrains the relief of residual compressive stress of capped TSV-Cu, which finally improves the elastic modulus and hardness based on nanoindentation test.

This paper can provide some guidance on treatments of excessively capped Cu layer during annealing of TSV interconnected structure for IC manufacturing. It is recommended that after removing the capped Cu layer by CMP, high temperature annealing is carried out to make the TSV-Cu to be fully protruded and the grains to be stabilized. Due to microstructure stabilization of TSV-Cu and the interconnect layer constraint, the problem of continuous protrusions could be effectively controlled.

### REFERENCES

- [1] J. P. Gambino, S. A. Adderly, and J. U. Knickerbocker, "An overview of through-silicon-via technology and manufacturing challenges," *Microelec. Eng.*, vol. 135, pp. 73–106, Mar. 2015.

- [2] Y. Hu, L. Xiong, M. Li, and T. Hang, "Covalently formation of insulation and barrier layers in high aspect ratio TSVs," *Appl. Surf. Sci.*, vol. 573, Jan. 2022, Art. no. 151588.
- [3] H.-C. Chuang, Y.-C. Teng, and J. Sanchez, "Study on the effects of pressure and material characterization in thin film and TSV fabricated by supercritical carbon dioxide electrolyte," *Mater. Sci. Semicond. Process.*, vol. 56, pp. 5–13, Dec. 2016.
- [4] Z. Fan, X. Chen, Y. Jiang, X. Li, S. Zhang, and Y. Wang, "Effects of multi-cracks and thermal-mechanical coupled load on the TSV reliability," *Microelectron. Rel.*, vol. 131, Apr. 2022, Art. no. 114499.
- [5] C. Okoro, L. E. Levine, R. Xu, and Y. Obeng, "Experimental measurement of the effect of copper through-silicon via diameter on stress buildup using synchrotron-based X-ray source," *J. Mater. Sci.*, vol. 50, no. 18, pp. 6236–6244, Jun. 2015.
- [6] M. Song, Z. Wei, B. Wang, L. Chen, L. Chen, and J. A. Szpunar, "Study on copper protrusion of through-silicon via in a 3-D integrated circuit," *Mater. Sci. Eng. A*, vol. 755, pp. 66–74, May 2019.
- [7] S. B. Liang, C. B. Ke, C. Wei, M. B. Zhou, and X. P. Zhang, "Investigation of the interaction effect between the microstructure evolution and the thermo-mechanical behavior of Cu-filled through silicon via," *IEEE Trans. Device Mater. Rel.*, vol. 22, no. 2, pp. 267–275, Jun. 2022.
- [8] Z. Wang, G. Ye, X. Li, S. Xue, and L. Gong, "Thermal-mechanical performance analysis and structure optimization of the TSV in 3-D IC," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 11, no. 5, pp. 822–831, May 2021.
- [9] C. Rao et al., "Residual stress and pop-out simulation for TSVs and contacts in via-middle process," *IEEE Trans. Semicond. Manuf.*, vol. 30, no. 2, pp. 143–154, May 2017.
- [10] H. Kim, H. Jeon, D.-J. Lee, and J.-Y. Kim, "Surface residual stress in amorphous SiO<sub>2</sub> insulating layer on Si substrate near a Cu through-silicon via (TSV) investigated by nanoindentation," *Mater. Sci. Semicond. Process.*, vol. 135, Nov. 2021, Art. no. 106153.
- [11] T. Jiang, J. Im, R. Huang, and P. S. Ho, "Through-silicon via stress characteristics and reliability impact on 3D integrated circuits," *MRS Bull.*, vol. 40, no. 3, pp. 248–256, Mar. 2015.
- [12] A. P. Karmarkar et al., "Modeling copper plastic deformation and liner viscoelastic flow effects on performance and reliability in through silicon via (TSV) fabrication processes," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 4, pp. 642–653, Dec. 2019.
- [13] L. Spinella, T. Jiang, N. Tamura, J.-H. Im, and P. S. Ho, "Synchrotron X-ray microdiffraction investigation of scaling effects on reliability for through-silicon vias for 3-D integration," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 3, pp. 568–571, Sep. 2019.
- [14] M. Sung, A. Lee, T. Kim, Y. Yoon, T. Lim, and J. J. Kim, "Sulfur-containing additives for mitigating Cu protrusion in through silicon via (TSV)," *J. Electrochem. Soc.*, vol. 166, no. 12, pp. D514–D520, Jul. 2019.
- [15] J. Wang, L. Ma, and Y. Wang, "Investigation on filling method and thermal reliability of Sn58Bi-TSV," *Mater. Lett.*, vol. 288, Apr. 2021, Art. no. 129306.
- [16] T.-C. Lin et al., "Inhibiting the detrimental Cu protrusion in Cu through-silicon-via by highly (111)-oriented nanotwinned Cu," *Scripta Materialia*, vol. 197, May 2021, Art. no. 113782.
- [17] X. Luo et al., "Simulation of TSV protrusion in 3DIC integration by directly loading on coarse-grained phase-field crystal model," *Electronics*, vol. 11, no. 2, p. 221, Jan. 2022.
- [18] J. Liu, Z. Huang, P. P. Conway, and Y. Liu, "Processing-structure-protrusion relationship of 3-D Cu TSVs: Control at the atomic scale," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1270–1276, 2019.
- [19] E. Beyne, "Reliable via-middle copper through-silicon via technology for 3-D integration," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 6, no. 7, pp. 983–992, Jul. 2016.
- [20] Y. Zhang, G. Ding, H. Wang, and P. Cheng, "Microstructure of electrodeposited Cu micro-cylinders in high-aspect-ratio blind holes and crystallographic texture of the Cu overburden film," *J. Mater. Sci. Technol.*, vol. 32, no. 4, pp. 355–361, Sep. 2016.
- [21] L. Hu et al., "Optimization and characterization of the metal cap layout above through-silicon via to improve copper dishing and protrusion effect for the application of 3-D integrated circuits," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 8, no. 12, pp. 2222–2226, Dec. 2018.
- [22] P. Saettler, M. Boettcher, C. Rudolph, and K.-J. Wolter, "Bath chemistry and copper overburden as influencing factors of the TSV annealing," presented at the IEEE 63rd ECTC, 2013.
- [23] T. C. Tsai et al., "CMP process development for the via-middle 3D TSV applications at 28 nm technology node," *Microelecon. Eng.*, vol. 92, pp. 29–33, Apr. 2012.
- [24] X. Jing et al., "Effect of pre-CMP annealing on TSV pumping in thermal budget and reliability test," presented at the IEEE 22nd IPFA, 2015.
- [25] G. Jalilvand, O. Ahmed, L. Spinella, L. Zhou, and T. Jiang, "The effective control of Cu through-silicon via extrusion for three-dimensional integrated circuits by a metallic cap layer," *Scripta Materialia*, vol. 164, pp. 101–104, Apr. 2019.
- [26] Y. Chen, W. Su, H.-Z. Huang, P. Lai, X.-L. Lin, and S. Chen, "Stress evolution mechanism and thermo-mechanical reliability analysis of copper-filled TSV interposer," *Eksplotacjja i Niezawodnosć Maintenance Rel.*, vol. 22, no. 4, pp. 705–714, Apr. 2020.
- [27] C. Okoro, J. W. Lau, F. Golshany, K. Hummler, and Y. S. Obeng, "A detailed failure analysis examination of the effect of thermal cycling on Cu TSV reliability," *IEEE Trans. Electron. Devices*, vol. 61, no. 1, pp. 15–22, Jan. 2014.
- [28] C. Wu, R. Huang, and K. M. Liechti, "Characterizing interfacial sliding of through-silicon-via by nano-indentation," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 2, pp. 355–363, Jun. 2017.
- [29] S. Chen, Z. Wang, Y. En, Y. Huang, F. Qin, and T. An, "The experimental analysis and the mechanical model for the debonding failure of TSV-Cu/Si interface," *Microelectron. Rel.*, vol. 91, pp. 52–66, Dec. 2018.
- [30] C. Xue, Z. Cheng, Z. Chen, Y. Yan, Z. Cai, and Y. Ding, "Elimination of scallop-induced stress fluctuation on through-silicon-vias (TSVs) by employing polyimide liner," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 266–272, Jun. 2018.
- [31] Y. Zare, Y. Sasajima, and J. Onuki, "A novel lining method for eliminating plastic deformation and protrusion of copper in Cu-TSV using FEM analysis," *J. Electron. Mater.*, vol. 49, no. 6, pp. 3692–3700, Aug. 2020.
- [32] A. E. Majd, I. H. Jeong, J. P. Jung, and N. N. Ekere, "Cu protrusion of different through-silicon via shapes under annealing process," *J. Mater. Eng. Perform.*, vol. 30, no. 6, pp. 4712–4720, Apr. 2021.
- [33] G. Jalilvand, O. Ahmed, N. Dube, and T. Jiang, "The effect of pitch distance on the statistics and morphology of through-silicon via extrusion," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 11, no. 6, pp. 883–891, Jun. 2021.
- [34] T. An, F. Qin, S. Chen, and P. Chen, "The effect of the diffusion creep behavior on the TSV-Cu protrusion morphology during annealing," *J. Mater. Sci. Mater. Electron.*, vol. 29, no. 19, pp. 16305–16316, Jul. 2018.
- [35] S.-H. Kim, H.-J. Lee, D. Josell, and T. P. Moffat, "Bottom-up Cu filling of annular through silicon vias: Microstructure and texture," *Electrochimica Acta*, vol. 335, Mar. 2020, Art. no. 135612.
- [36] S. Chen, F. Qin, T. An, P. Chen, B. Xie, and X. Shi, "Protrusion of electroplated copper filled in through silicon vias during annealing process," *Microelectron. Rel.*, vol. 63, pp. 183–193, Aug. 2016.
- [37] Y. Li et al., "Constitutive modelling of annealing behavior in through silicon vias-copper," *Mater. Charact.*, vol. 179, Sep. 2021, Art. no. 111359.
- [38] H. Wang et al., "Effect of current density on microstructure and mechanical property of Cu micro-cylinders electrodeposited in through silicon vias," *Mater. Charact.*, vol. 109, pp. 164–172, Nov. 2015.
- [39] H. Wang et al., "Effect of thermal treatment on the mechanical properties of Cu specimen fabricated using electrodeposition bath for through-silicon-via filling," *Microelectron. Eng.*, vol. 114, pp. 85–90, Sep. 2014.
- [40] C. Okoro et al., "Influence of annealing conditions on the mechanical and microstructural behavior of electroplated Cu-TSV," *J. Micromech. Microeng.*, vol. 20, no. 4, Mar. 2010, Art. no. 45032.
- [41] M. Zhang, F. Qin, S. Chen, Y. Dai, P. Chen, and T. An, "Protrusion of through-silicon-via (TSV) copper with double annealing processes," *J. Electron. Mater.*, vol. 51, no. 5, pp. 2433–2449, Mar. 2022.
- [42] L. Xu et al., "Through-wafer electroplated copper interconnect with ultrafine grains and high density of nanotwins," *Appl. Phys. Lett.*, vol. 90, no. 3, Jan. 2007, Art. no. 33111.
- [43] L. Lu, Y. Shen, X. Chen, L. Qian, and K. Lu, "Ultrahigh strength and high electrical conductivity in copper," *Science*, vol. 304, no. 5669, pp. 422–426, Mar. 2004.
- [44] J. De Messemaeker et al., "Statistical distribution of through-silicon via Cu pumping," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 3, pp. 549–559, Sep. 2017.
- [45] A. S. Budiman et al., "Measurement of stresses in Cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits," *Microelectro. Rel.*, vol. 52, no. 3, pp. 530–533, Sep. 2012.
- [46] M. Faheem, R. R. Giridharan, Y. Liang, and P. van Der Heide, "Micro-XRD characterization of a single copper filled through-silicon via," *Mater. Lett.*, vol. 161, pp. 391–394, Dec. 2015.
- [47] D. Gan, "Thermal stress and stress relaxation in copper metallization for ULSI interconnects," Dept. Mater. Sci. Eng., Ph.D. dissertation, Univ. Texas Austin, Austin, TX, USA, 2005.

- [48] Y.-H. Lee and D. Kwon, "Measurement of residual-stress effect by nanoindentation on elastically strained (100) W," *Scripta Materialia*, vol. 49, no. 5, pp. 459–465, Sep. 2003.
- [49] K. Zhou, B. Liu, Y. Yao, and K. Zhong, "Effects of grain size and shape on mechanical properties of nanocrystalline copper investigated by molecular dynamics," *Mater. Sci. Eng. A*, vol. 615, pp. 92–97, Oct. 2014.
- [50] A. Basavalingappa and J. R. Lloyd, "Effect of microstructure and anisotropy of copper on reliability in nanoscale interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 69–79, Mar. 2017.
- [51] S. F. Wang et al., "Effect of deformation induced microstructure faults on the elastic mechanical parameters of micro-scale copper," *Exp. Technol.*, vol. 43, no. 1, pp. 1–6, May 2018.



**Min Zhang** received the B.E. degree in engineering mechanics from Wuhan University of Science and Technology, Wuhan, China, in 2017. She is currently pursuing the Ph.D. degree with the Institute of Electronics Packaging Technology and Reliability, Beijing University of Technology, Beijing, China.

Her current research interests include reliability analysis of electronics packaging structure and thermomechanical modeling.



**Fei Qin** received the B.E. degree in applied mechanics from Xi'an Jiaotong University, Xi'an, China, in 1985, and the M.E. and Ph.D. degrees in solid mechanics from Tsinghua University, Beijing, China, in 1987 and 1997, respectively.

He was a Postdoctoral Fellow and a Research Fellow with the School of Civil and Structures, Nanyang Technological University, Singapore, from 1997 to 2000. Since 2001, he has been with the Beijing University of Technology, Beijing, where he is currently a Full Professor and the Director of Institute of Electronics Packaging Technology and Reliability. He has authored more than 150 journal and conference papers, holds two U.S. patents and more than 50 Chinese patents. His current research interests include the areas of computer methods in materials science and engineering, design for reliability of electronic packaging, simulations, and characterization of the mechanical behavior of the materials, and structures and manufacturing processes in electronic packages.



**Si Chen** received the B.E. degree in materials science from Hohai University, Nanjing, China, in 2011, and the Ph.D. degree from the Beijing University of Technology, Beijing, China, in 2017.

Since 2019, she has been a Senior Engineer with the Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, China Electronic Product Reliability and Environmental Testing Research Institute. She has published well over 26 papers to journals and international conferences, and hold four patents. Her current research interests are focused on reliability issues of TSV stacking integration.



**Yanwei Dai** received the B.E. degree in engineering mechanics from the Wuhan University of Technology, Wuhan, China, in 2011, the M.E. degree in solid mechanics from China Agricultural University, Beijing, China, in 2013, and the Ph.D. degree in mechanics from Tsinghua University, Beijing, in 2018.

In 2018, he joined Beijing University of Technology, where he is currently an Associate Professor. He has authored and coauthored more than 50 peer-reviewed journal articles in the fields of mechanics and electronics packaging. His current research interests include fracture and fatigue mechanics of structures and materials in electronics packaging, reliability analyses and evaluations of 3D packaging, and design and characterization of power devices and related materials.



**Yifan Jin** received the B.E. degree in mechanical design, manufacturing, and automation from North China University of Science and Technology, Tangshan, China, in 2017, and the M.E. degree in mechanical engineering from the Institute of Electronics Packaging Technology and Reliability, Beijing University of Technology, Beijing, China, in 2022.

She currently works as a Structural Designer with Aerospace Internet of Things Technology Co., Ltd.



**Pei Chen** received the B.E. degree in mechanical engineering from Xiamen University, Fujian, China, in 2008, and the M.S. and Ph.D. degrees in mechanical engineering from the University of Akron, Akron, OH, USA, in 2010 and 2013, respectively.

Since 2014, he has been with the Institute of Electronics Packaging Technology and Reliability, Beijing University of Technology, Beijing, China. Before that, he was a Type Engineer with Linglong Tyre and Rubber Company from 2013 to 2014. He has authored and coauthored more than 20 peer-reviewed technical publications. His current research interests include precision process of semiconductor materials, chip-package interaction, and low-dimensional electronic materials.



**Tong An** received the B.E. degree in safety engineering, the M.E. degree in solids mechanics, and the Ph.D. degree in engineering mechanics from the Beijing University of Technology, Beijing, China, in 2006, 2009, and 2014, respectively.

She is currently an Associate Professor with the Institute of Electronics Packaging Technology and Reliability, Beijing University of Technology. Her current research interests include reliability of power semiconductor device, thermomechanical modeling, failure mechanism of electronic packaging, and micro- and macro-mechanical behaviors of packaging materials.



**Yanpeng Gong** received the B.S. degree in applied mathematics from Linyi University, Shandong, China, in 2012, the M.S. degree in computational mathematics from the Shandong University of Technology, Shandong, China, in 2015, and the Ph.D. degree in computational mechanics from the Beijing Institute of Technology, Beijing, China, in 2019.

He is currently an Associate Researcher with the Institute of Electronics Packaging Technology and Reliability, Beijing University of Technology. He has authored more than 30 journal and conference papers. His current research interests include computational mechanics, high performance computing, multiscale simulation, and model reduction techniques with special attention to semiconductor and electronic packaging structures.