DDR device internal clk is a ratio 16:1 of the IO clk

For controller clk 2133MHz, bandwidth because of the double edge is 4266Mbps, device internal clk is 266MHz.

How frequent of DDR refresh is independent of the IO clk, but a factor of RAM cell capacitator discharge

Latency:

L3: ~20ns

LLC: ~40 t0 50 ns

DRAM hit: ~100ns

DRAM miss: > 100ns

Machine generated alternative text:
Memory Timing Parameters 
Critical parameters for memory 
CL-tRCO-tRP 
CAS Latency (Read/Write command to Data) 
How quickly can we get data from sense amps, or from sense amps 
into memory array 
Row to Column Address Dely (Activate to Burst 
Command) 
How quickly we can move data from memory/rowto sense amplifiers 
Precharge/Closing a bank to Activate on same bank 
How quickly we can open another row 

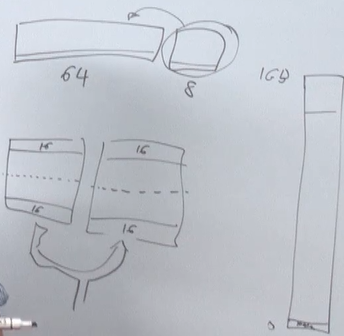
Machine generated alternative text:
Timing parameters 
Clock period — Interface clock cycle time 
CAS Latency —Time from read address application to when data is available 
TDQSS— Time from write command to first edge of DQS 
Trcd - 
Activate command to READ/VVRITE delay 
Trc 
— Activate to activate delay on same bank 
Trrd — Activate to activate delay different banks 
Tras — Activate to precharge delay 
— Refresh interval 

Machine generated alternative text:
Critical parameters (DDR2) 
Trc —Activate to activate delay (same bank) 
55 ns/l I cl< 
Affects how back to back accesses to same bank, different rows 
— 10 ns/2ck 
Trrd - Activate to activate delay (different bank) 
Trcd -Activate to READ/WRITE delay 13.125 ns/3ck 
ACT- 
RD-2 
rrd 
NOP 
NOP 
ACT- 
RD-3 
rcd 
RD-O 
NOP 
NOP 
ACT- 
RD-I 
3 
NOP 

Machine generated alternative text:
VDP 
20). 

Machine generated alternative text:
3 2_DO 
L-p raq_ 
32.90 42K' 

Inline ECC:



Machine generated alternative text:
Drives replacement cycle 
1% 
LPDDR4 
3200Mbps 
HD Video, 
Shiny games 
9% 
200-1600Mbps (LPDDR3 range) 
Text, Phone, Browse, Read, 
Photograph, 
Puzzles and simple games 
Off or low speed, one channel active 
Phone dark and in pocket or at bedside 
Maintain cell contact, receive texts, receive and 
display push notifications, sync mail, show clock 
Performance 
Focus 
Best 
Performance 
under low- 
speed power 
limits 
Power Focus 

Machine generated alternative text:
What's New in LPDDR4? 
• Operation up to 3200-4266Mb/s 
• Specifications for devices up to 16Gb 
• 6-bit SDR Command/Address bus 
• 4-phase addressing 
• Mandatory minimum burst of 16 
• New masked write method 
• Changed initialization, training and 
command sequences 
• Targeted Row Refresh (TRR) 
• Frequency set points 

Machine generated alternative text:
LPDDR4 is Different From Earlier DRAM 
• DDR2,3,4 are all one die per 
package with one 
command/address bus input and 
one data bus 
• LPDDR2,3 offer one or two dies 
per package, each die with its 
own command/address input and 
data bus 
• LPDDR4 have two 
command/address inputs 
(channels) and two data busses 
per die 
— Some LPDDR4 packages have two 
dies 4 channels 
2 independent channels 
2K8 Page 
8 banks 

Machine generated alternative text:
LPDDR4 Target: BW Performance 
Key features for BW Performance 
2-Channel x 8-bank architecture 
• More responders for higher scheduling efficiency 
• Lower average latency 
32B pre-fetch per channel 
• Optimized MAL for fragmented data traffic 
High speed I/O, up to 4.267 Mbps 
• Targeting support for up to 2DQ or 4CA loads (system 
dependent) 
6.4 GB/s to 8.5 GB/s bandwidth from each channel 
Up to 17GB/s per die, 34GB/s for x64 system 

Machine generated alternative text:
• Two DRAM devices: 
— Parallel (lockstep) 
— Series (multi-rank) 
— Multi-channel 
4 ways to connect 
— Multi-channel with Shared-CA 
Parallel connection: 
soc 
DRAM* 
Chip select 
DRAM* 
• 
• 
• one DRAM die Of LPDDR2J3 or one channel of LPDDR4 
Both DRAM devices receive 
the same command & 
address but transmit data 
over different byte lanes. 
Both devices are accessed 
simultaneously 

Machine generated alternative text:
— Series (multi-rank) 
— Multi-channel 
— Multi-channel with Shared-CA 
DRAM* 
Chi selects 
soc 
DRAM* 
• one DRAM die Of LPDDR2J3 or one channel Of LPDDR4 
Series (Multi-rank) Connection: 
• Both DRAM devices receive 
the same command & 
address and transmit their 
data over the same byte 
lanes. 
Chip select signals 
determine which device is 
being accessed, one at a 
time. 

Machine generated alternative text:
— Multi-channel 
— Multi-channel with Shared-CA 
Chip select 
DRAM* 
soc 
DRAM* 
Chip select 
Multi-Channel Connection: 
• Each DRAM device operates 
independently of the other, receives a 
different command & address, transmits 
over different byte lanes 
• One DRAM die Of LPDDR2/3 or one channel of LPDDR4 

Machine generated alternative text:
— Multi-channel with Shared-CA 
soc 
Multi-channel with Shared-CA (aka Shared-AC): 
Chip select 
• Both DRAM devices receive the same 
DRAM 
command & address but only one device is 
accessed with an active chip select at a time, 
so each DRAM device operates independently. 
DRAM devices transmit data over different byte 
DRAM 
lanes. 
Chip select 
Shared CA is more common with DDR 
consumer designs than LPDDR. 

Machine generated alternative text:
Parallel 
CA pins: 6 
DQ pins: 32 
CS pins: 1 
Banks: 8 
Fetch: 64 
Series 
CA pins: 6 
DQ pins: 16 
CS pins: 1 
Banks: 8 
Fetch: 32 
= 1 channel of LPDDR4 CA Bus 
Multi-channel 
CA pins: 12 
DQ pins: 32 
CS pins: 2 
Banks: 16 
Fetch: 32 
DQ (Data) Bus 
Shared-CA 
CA pins: 6 
DQ pins: 32 
CS pins: 2 
Banks: 16 
Fetch: 32/64 
CS(Chip Select) 

Machine generated alternative text:
- tRC (RAS cycle time) 
— The minimum time between activate commands to the same bank 

Machine generated alternative text:
Minimum Fetch Size 
soc 
4 Channel 
CA pins: 24 
DQ pins: 64 
CS pins: 4 
Banks: 32 
Fetch: 32 
Parallel 
CA pins: 6 
DQ pins: 64 
CS pins: 1 
Banks: 8 
Fetch: 128 
• Many CPUs have a cache line size of 
32 or 64 bytes 
• Video and networking traffic may also 
require 32 or 64 byte transfers 
• Choose a multichannel architecture 
that matches the system fetch size 
• LPDDR4 minimum burst length is 16 
• 64 DQ pins in parallel produces a 128 
byte fetch 
• Only suitable for long data transfers to 
contiguous addresses 

**Internal clock 200MHZ**

1. **Every time a reference is made to a new DRAM page, the full 8 KiB is transferred from the DRAM array to the DRAM sense amps. This uses a fair amount of power, and it makes sense to try to read the entire 8 KiB while it is in the sense amps. Although it is beyond the scope of today’s discussion, reading data from “open pages” uses only about 1/4 to 1/5 of the power required to read the same amount of data in “closed page” mode, where only one cache line is retrieved from each DRAM page.**
2. **Data in the sense amps can be accessed at significantly lower latency — this is called “open page” access (or a “page hit”), and the latency is referred to as the “CAS latency”. On most systems the CAS latency is between 12.5 ns and 15 ns, independent of the frequency of the DRAM bus. If the data is not in the sense amps (a “page miss”), loading data from the array to the sense amps takes an additional latency of 12.5 to 15 ns. If the sense amps were holding other valid data, it would be necessary to write that data back to the array, taking an additional 12.5 to 15 ns. If the DRAM latency is not completely overlapped with the cache coherence latency, these increases will reduce the sustainable bandwidth according to Little’s Law: *Bandwidth = Concurrency / Latency***

***From <***[***https://sites.utexas.edu/jdm4372/tag/dram/***](https://sites.utexas.edu/jdm4372/tag/dram/)***>***