1- Communication between the HPS using Linux to the FPGA on the terasic DE10 development board

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Introduction

This document will guide you through the creation of a SoC system on the DE10 Standard board from terasic. The communication between the ARM Core and the FPGA will be established via the HPS2FPGA Lightweight bridge, that offers low latency with a slower but sufficient datarate compared to the Highspeed bridge. A Linux system image from terasic will be used, as the focus lies on the communication between the ARM Core and the FPGA ant this point.

Required Software & Hardware

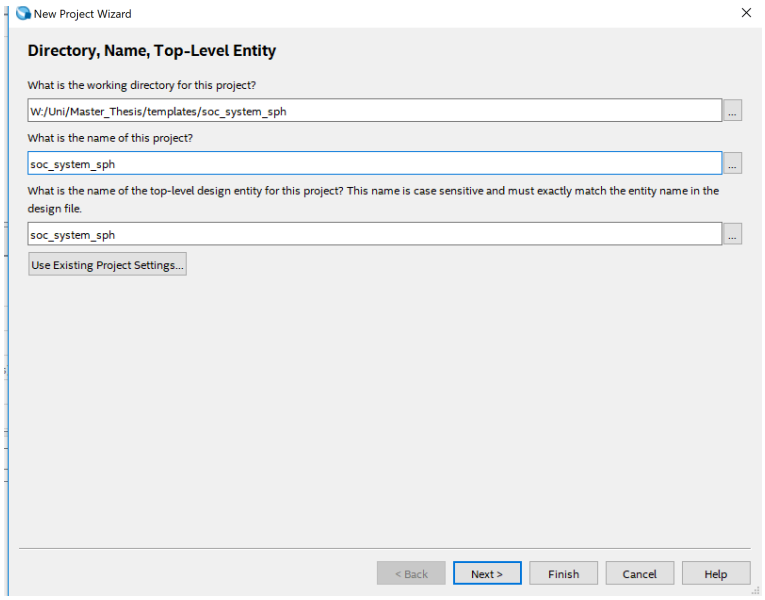
Linux System image: terasic linux image
DE10 Board
Micro SD Card with 8GB+
Windisk Imager 32 (or alternative tool to flash image to sd card)
Intel SoC EDS Version 16.0 (others might work, 16.0 was verified working)
Quartus 17.1 (others might work, 17.1 was verified working)
ARM DS-5 v5.23.1 Pro Version (using 30 day trial)

Installing Linux

- Flash image to SDCard with Windisk Imager 32 or alternative Tool.
- Insert the SD Card in the board.
- Set the MSEL Pins of the DE10 board to 01010 to boot from the SD Card.

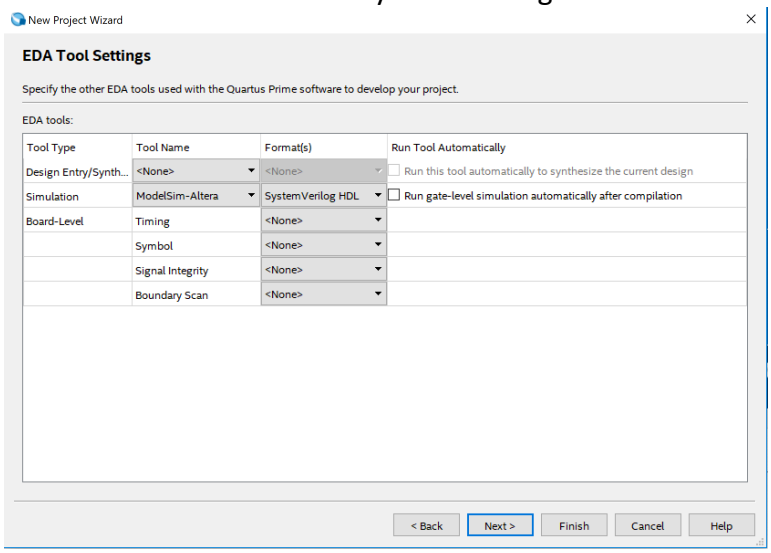
Create Quartus Project

Open Quartus Prime and select File->New->Project
Set project name and location

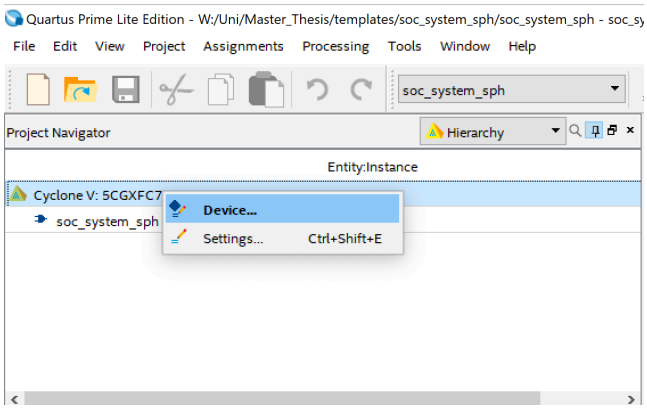


Choose empty project

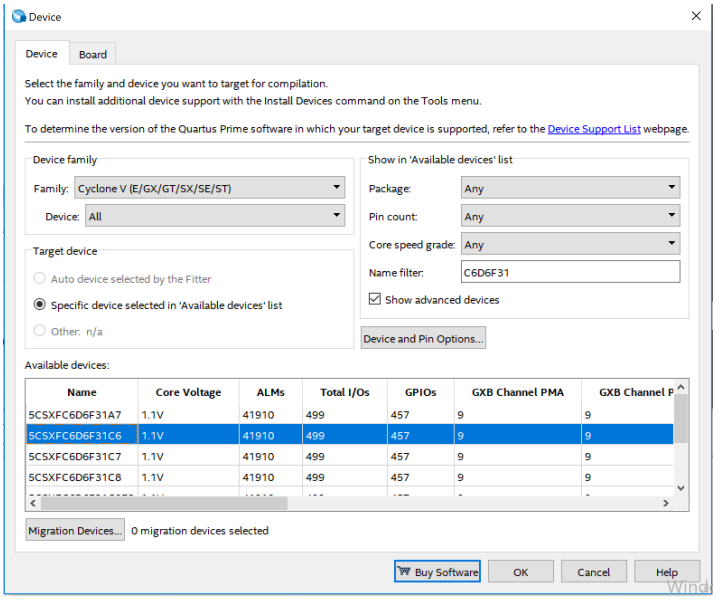
Choose ModelSim-Altera for Simulation and System Verilog HDL for Format



Click next -> finish



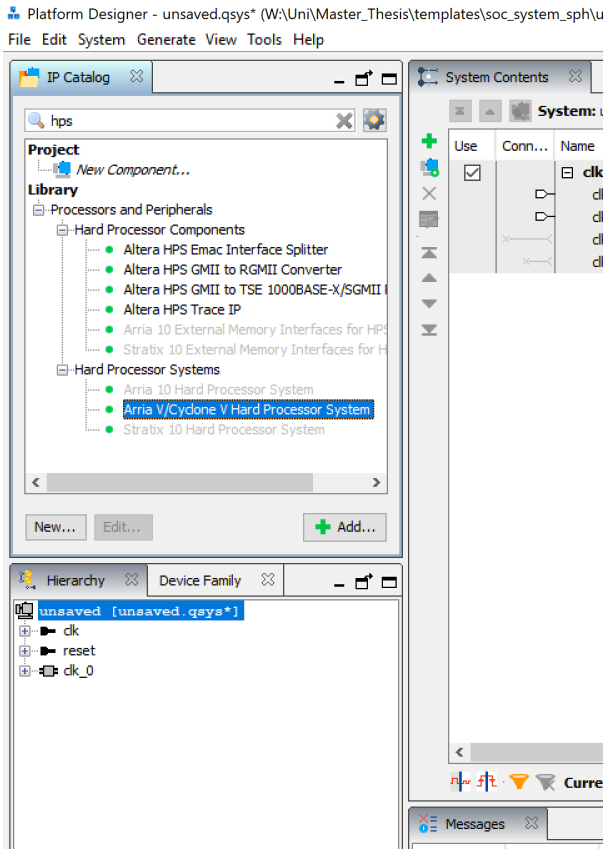
If the device selection menu was not previously shown, the device can be changed (if required) by right clicking on the device in the project navigator and selecting Device...



Select appropriate device and confirm with OK

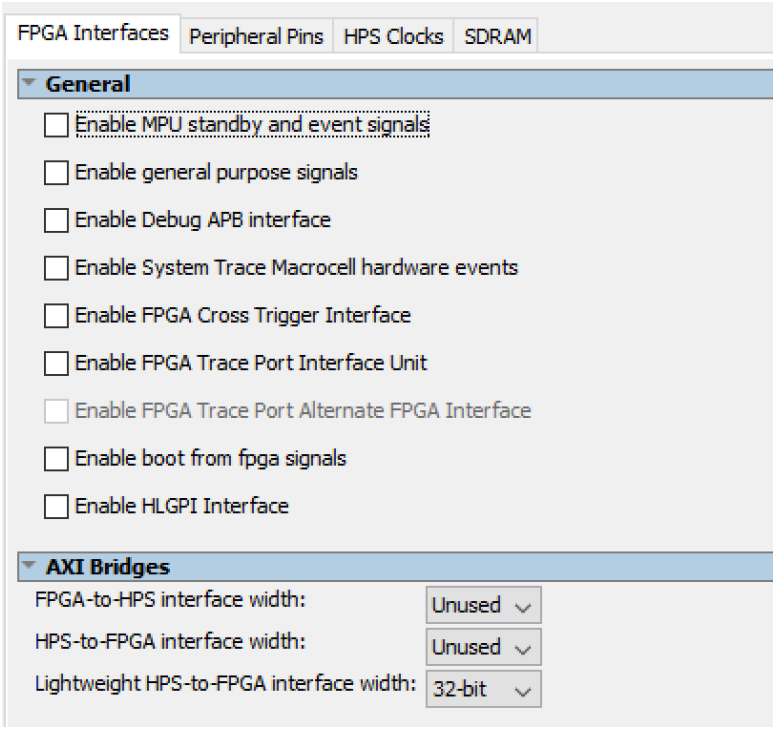
Create HPS System

To create the HPS System Select Tools->Platform Designer.

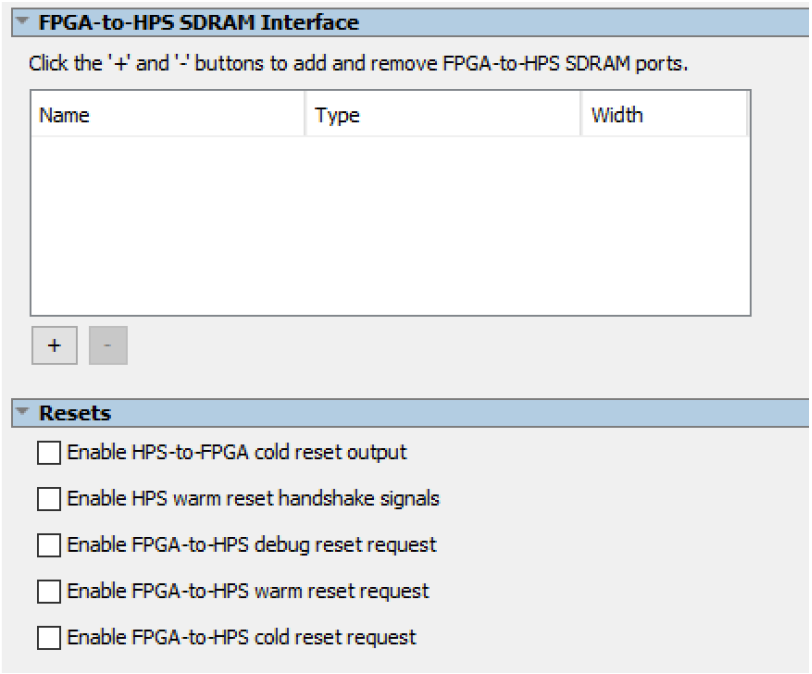


Search for hps in the IP Catalog and add it to the system by double clicking it.

Use the following settings:

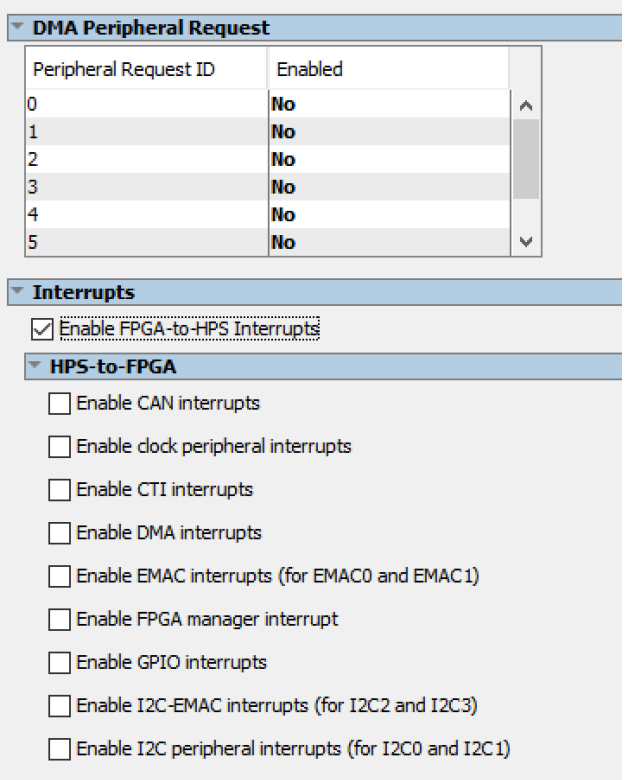


We will only use the lightweigt hps-fpga interface now.

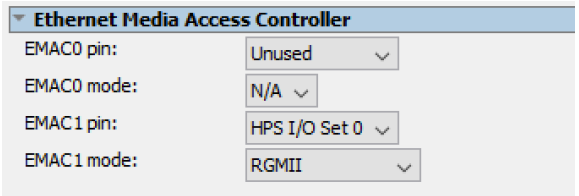


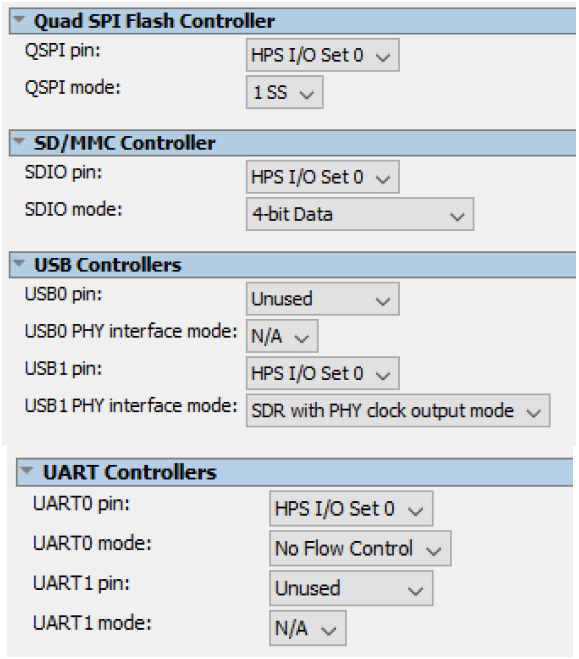
Disable all reset requests.

Enable FPGA to HPS Interrupts (all hps to fpga interrupts are disabled for now)

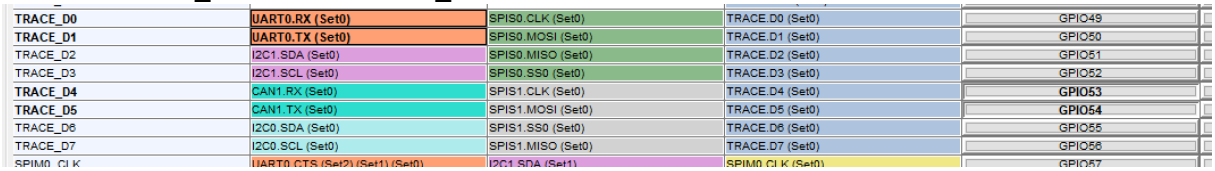


We want to enable the following peripherals for the HPS:
EMAC
QSPI
SD/MMC Controller
USB Controller
UART Controller

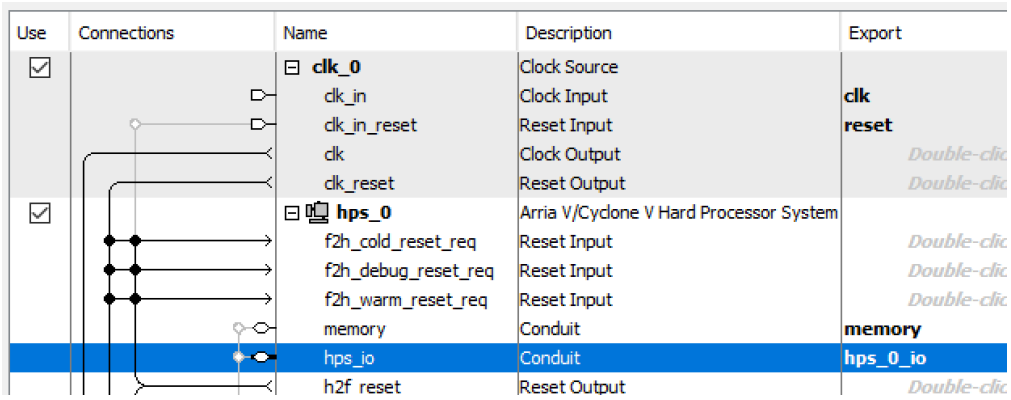




At the very bottom we activate GPIO 53 and 54 by clicking on the buttons. These are used to access the HPS_BUTTON and HPS_LED.

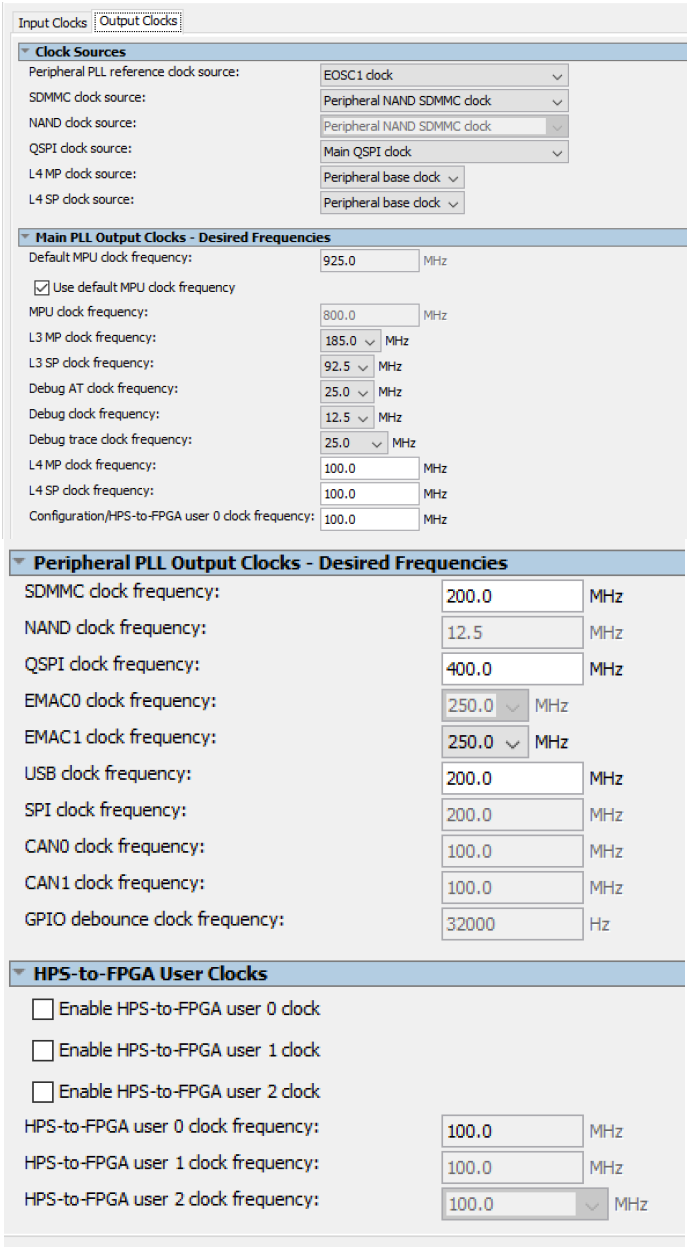


We export the hps_io conduit as hps_0_io :

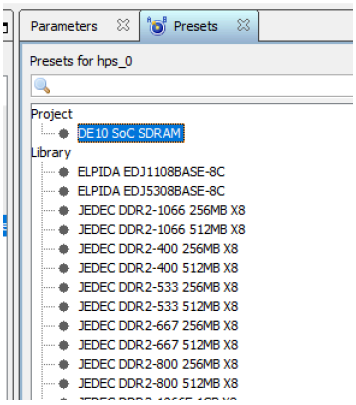


Now switch over to the HPS Clocks tab / Input clocks
Set both clocks to 25 MHz

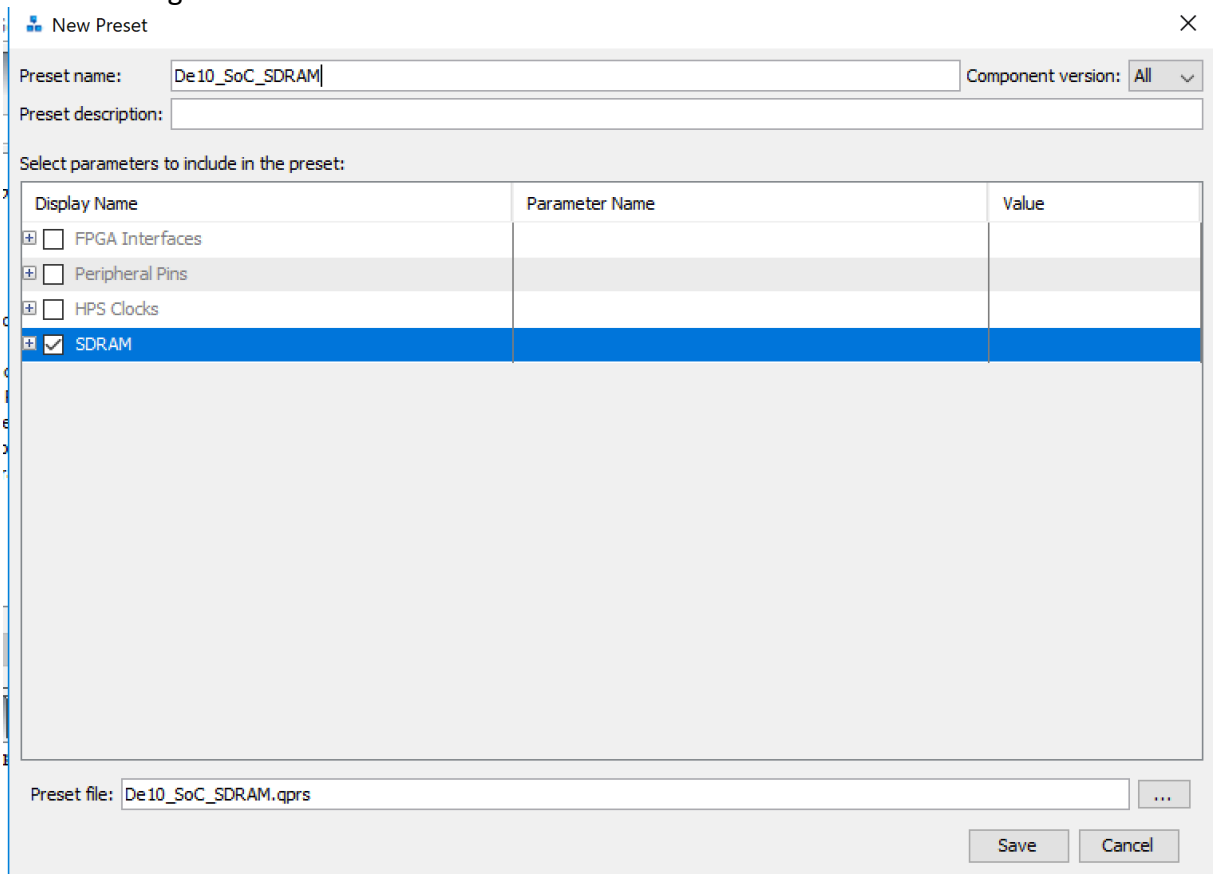
Switch to the output clocks. The default values should be correct, but it's better to check:



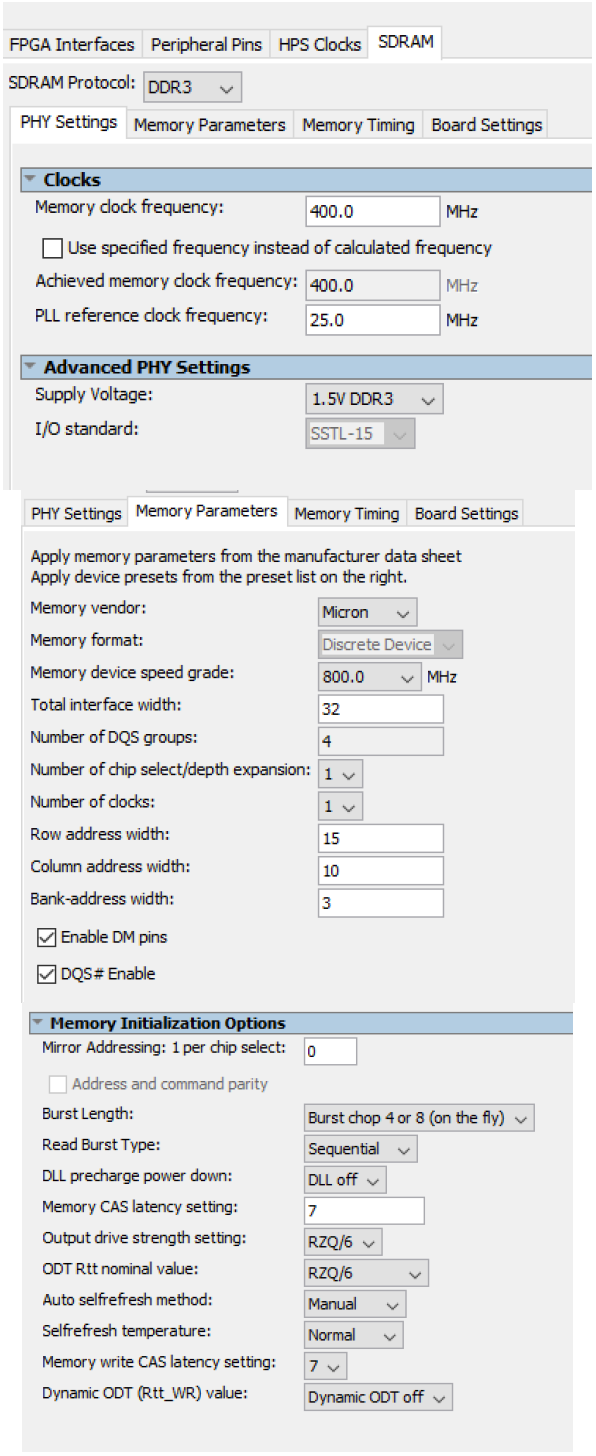
Next up is the SDRAM. If you have a preset file for this, you should add it to **quartus** (not the platform designer) project with Project->Add/remove files. Then close and open Platform designer again. You can now find the preset in platform designer by clicking view->presets.

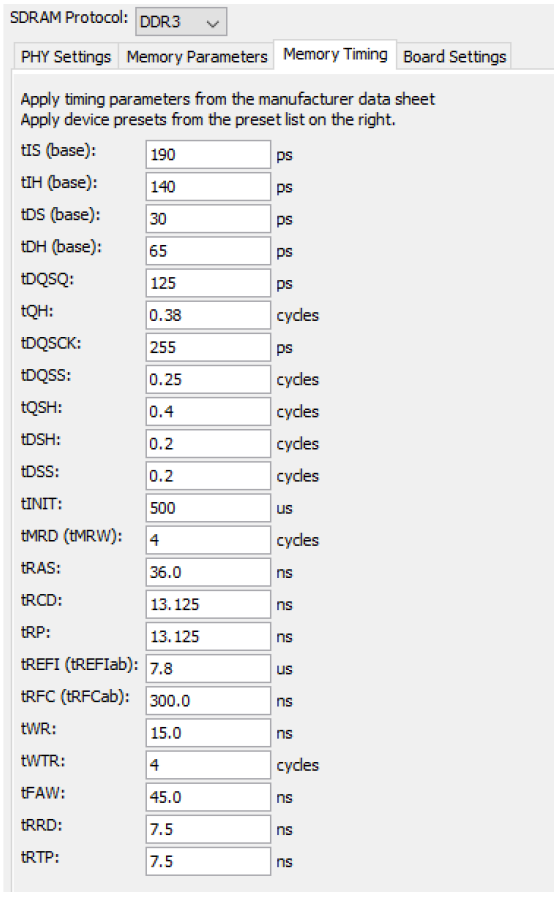


You can apply it by double clicking it. If you have no preset, you should copy the settings from the following images and save them as a preset by clicking new… in the presets window after entering the values:

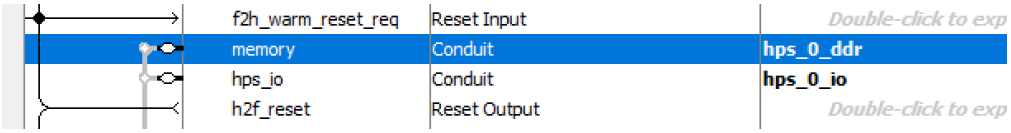


Here are the SDRAM settings:

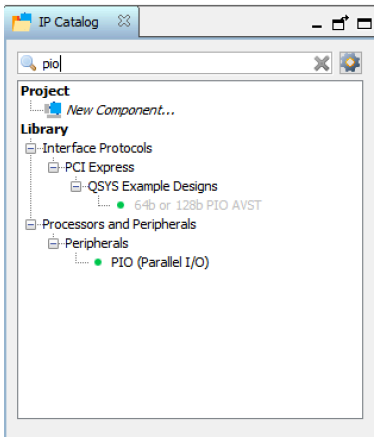

FPGA Interfaces
Peripheral Pins
HPS Clocks
SDRAM
SDRAM Protocol:
DDR3
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Clocks
Memory clock frequency:
400.0
MHz
Use specified frequency instead of calculated frequency
Achieved memory clock frequency:
400.0
MHz
PLL reference clock frequency:
25.0
MHz
Advanced PHY Settings
Supply Voltage:
1.5V DDR3
I/O standard:
SSTL-15
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Apply memory parameters from the manufacturer data sheet
Apply device presets from the preset list on the right.
Memory vendor:
Micron
Memory format:
Discrete Device
Memory device speed grade:
800.0
MHz
Total interface width:
32
Number of DQS groups:
4
Number of chip select/depth expansion:
1
Number of clocks:
1
Row address width:
15
Column address width:
10
Bank-address width:
3
Enable DM pins
DQS# Enable
Memory Initialization Options
Mirror Addressing: 1 per chip select:
0
Address and command parity
Burst Length:
Burst chop 4 or 8 (on the fly)
Read Burst Type:
Sequential
DLL precharge power down:
DLL off
Memory CAS latency setting:
7
Output drive strength setting:
RZQ/6
ODT Rtt nominal value:
RZQ/6
Auto selfrefresh method:
Manual
Selfrefresh temperature:
Normal
Memory write CAS latency setting:
7
Dynamic ODT (Rtt_WR) value:
Dynamic ODT off

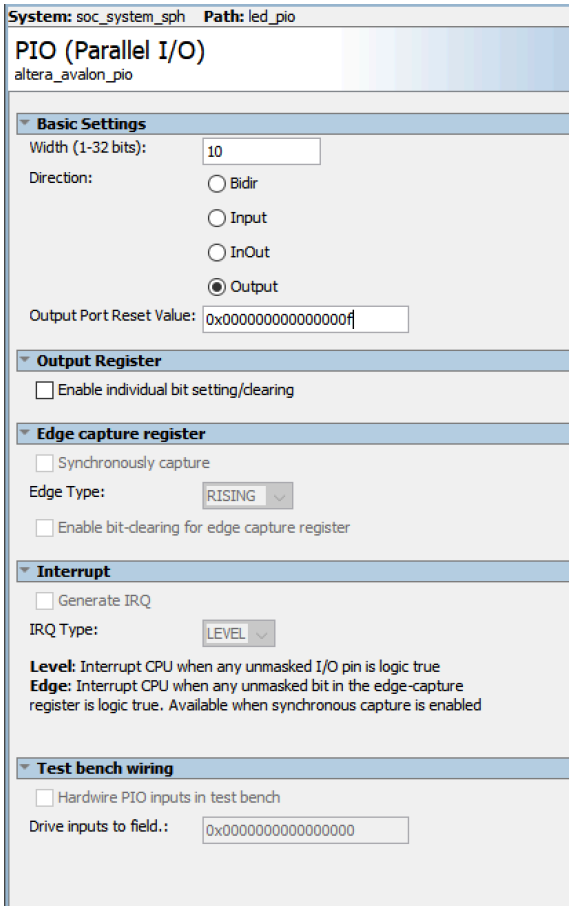


We export the memory conduit as hps_0_ddr:



For the board settings choose Altera's default settings.
Next, we will add a PIO module by double clicking it:

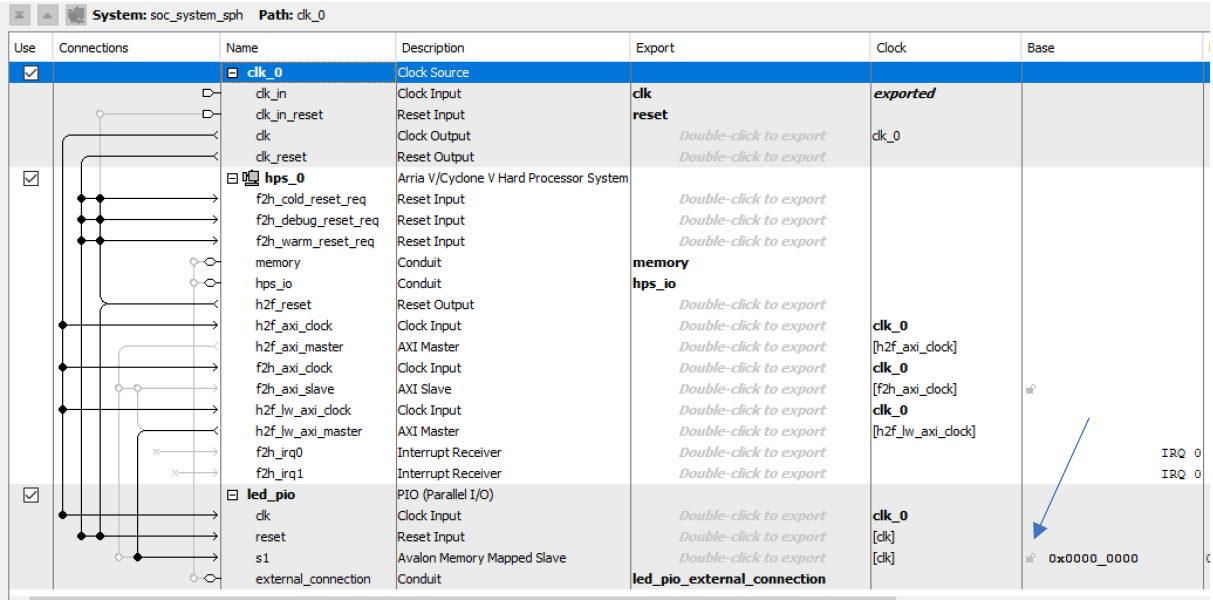




A reset value of 15 turns on 4 LEDs in case of an reset. This helps to ensure that everything is working as expected.

//TODO: add interrupt handler

We now connect everything as shown here:



Click on the lock besides the led_pio base address, to ensure that it does not get changed. Now click Generate->Generate HDL… select Verilog and keep the default settings. (You do not need to create a block diagram)

After the generation is done, we can close the Platform Designer.

Connecting the FPGA and the HPS

Back in Quartus we need to import the generated IP by selecting Project->Add/Remove Files and adding the qip file. It is found in a subfolder <system name>/synthesis/yourFile.qip

Next, we need to instantiate the system. The platform designer has already created a file with the instantiation of the component, but we still need to connect the signals. The file is called <your hps name>_inst.v and is found in the <your hps name> folder. We need to merge the contents of this file with the connections that are defined in the ghrd_top.v file provided by the GHRD from terasic. For every connection that is present in our instance, we need to replace the <connected-to-xxx> with the respective signal from the top-level module, whose signals are then finally connected to the hardware itself.

This is how the final file should look like for our current hps design:

```
module soc_system_sph_top_level(

///////// CLOCK /////////
input              CLOCK_50,

       ///////// CLOCK2 /////////
input              CLOCK2_50,

///////// CLOCK3 /////////
input              CLOCK3_50,

///////// CLOCK4 /////////
input              CLOCK4_50,

///////// DRAM /////////
output      [12:0] DRAM_ADDR,
output      [1:0]  DRAM_BA,
output             DRAM_CAS_N,
output             DRAM_CKE,
output             DRAM_CLK,
output             DRAM_CS_N,
inout       [15:0] DRAM_DQ,
output             DRAM_LDQM,
output             DRAM_RAS_N,
output             DRAM_UDQM,
output             DRAM_WE_N,
```

```
      ///////// GPIO /////////
      inout     [35:0]         GPIO_0,
      inout     [35:0]         GPIO_1,


      ///////// HPS /////////
      inout              HPS_CONV_USB_N,
      output      [14:0] HPS_DDR3_ADDR,
      output      [2:0]  HPS_DDR3_BA,
      output             HPS_DDR3_CAS_N,
      output             HPS_DDR3_CKE,
      output             HPS_DDR3_CK_N,
      output             HPS_DDR3_CK_P,
      output             HPS_DDR3_CS_N,
      output      [3:0]  HPS_DDR3_DM,
      inout       [31:0] HPS_DDR3_DQ,
      inout       [3:0]  HPS_DDR3_DQS_N,
      inout       [3:0]  HPS_DDR3_DQS_P,
      output             HPS_DDR3_ODT,
      output             HPS_DDR3_RAS_N,
      output             HPS_DDR3_RESET_N,
      input              HPS_DDR3_RZQ,
      output             HPS_DDR3_WE_N,
      output             HPS_ENET_GTX_CLK,
      inout              HPS_ENET_INT_N,
      output             HPS_ENET_MDC,
      inout              HPS_ENET_MDIO,
      input              HPS_ENET_RX_CLK,
      input       [3:0]  HPS_ENET_RX_DATA,
      input              HPS_ENET_RX_DV,
      output      [3:0]  HPS_ENET_TX_DATA,
      output             HPS_ENET_TX_EN,
      inout       [3:0]  HPS_FLASH_DATA,
      output             HPS_FLASH_DCLK,
      output             HPS_FLASH_NCSO,
      inout              HPS_GSENSOR_INT,
      inout              HPS_I2C1_SCLK,
      inout              HPS_I2C1_SDAT,
      inout              HPS_I2C2_SCLK,
      inout              HPS_I2C2_SDAT,
      inout              HPS_I2C_CONTROL,
      inout              HPS_KEY,
      inout              HPS_LED,
      inout              HPS_LTC_GPIO,
      output             HPS_SD_CLK,
      inout              HPS_SD_CMD,
      inout       [3:0]  HPS_SD_DATA,
      output             HPS_SPIM_CLK,
      input              HPS_SPIM_MISO,
      output             HPS_SPIM_MOSI,
      inout              HPS_SPIM_SS,
      input              HPS_UART_RX,
```

```
      output             HPS_UART_TX,
      input              HPS_USB_CLKOUT,
      inout       [7:0]  HPS_USB_DATA,
      input              HPS_USB_DIR,
      input              HPS_USB_NXT,
      output             HPS_USB_STP,


      ///////// KEY /////////
      input       [3:0]  KEY_N,

      ///////// LEDR /////////
      output      [9:0]  LEDR

);

        wire [9:0]  fpga_led_internal;

        assign LEDR = fpga_led_internal;


soc_system_sph u0 (
      .clk_clk                            (CLOCK_50),
//                        clk.clk
      .reset_reset_n                      (1'b1),                     //
reset.reset_n

      // ETHERNET

      .hps_0_io_hps_io_emac1_inst_TX_CLK ( HPS_ENET_GTX_CLK),       //
hps_0_io.hps_io_emac1_inst_TX_CLK
      .hps_0_io_hps_io_emac1_inst_TXD0   ( HPS_ENET_TX_DATA[0] ),   //
.hps_io_emac1_inst_TXD0
      .hps_0_io_hps_io_emac1_inst_TXD1   ( HPS_ENET_TX_DATA[1] ),   //
.hps_io_emac1_inst_TXD1
      .hps_0_io_hps_io_emac1_inst_TXD2   ( HPS_ENET_TX_DATA[2] ),   //
.hps_io_emac1_inst_TXD2
      .hps_0_io_hps_io_emac1_inst_TXD3   ( HPS_ENET_TX_DATA[3] ),   //
.hps_io_emac1_inst_TXD3
      .hps_0_io_hps_io_emac1_inst_RXD0   ( HPS_ENET_RX_DATA[0] ),   //
.hps_io_emac1_inst_RXD0
      .hps_0_io_hps_io_emac1_inst_MDIO   ( HPS_ENET_MDIO ),         //
.hps_io_emac1_inst_MDIO
      .hps_0_io_hps_io_emac1_inst_MDC    ( HPS_ENET_MDC  ),         //
.hps_io_emac1_inst_MDC
      .hps_0_io_hps_io_emac1_inst_RX_CTL ( HPS_ENET_RX_DV),         //
.hps_io_emac1_inst_RX_CTL
      .hps_0_io_hps_io_emac1_inst_TX_CTL ( HPS_ENET_TX_EN),         //
.hps_io_emac1_inst_TX_CTL
      .hps_0_io_hps_io_emac1_inst_RX_CLK ( HPS_ENET_RX_CLK),        //
.hps_io_emac1_inst_RX_CLK
```

```
      .hps_0_io_hps_io_emac1_inst_RXD1   ( HPS_ENET_RX_DATA[1] ),   //
.hps_io_emac1_inst_RXD1
      .hps_0_io_hps_io_emac1_inst_RXD2   ( HPS_ENET_RX_DATA[2] ),   //
.hps_io_emac1_inst_RXD2
      .hps_0_io_hps_io_emac1_inst_RXD3   ( HPS_ENET_RX_DATA[3] ),   //
.hps_io_emac1_inst_RXD3

      // QSPI

      .hps_0_io_hps_io_qspi_inst_IO0     ( HPS_FLASH_DATA[0]    ),     //
.hps_io_qspi_inst_IO0
      .hps_0_io_hps_io_qspi_inst_IO1     ( HPS_FLASH_DATA[1]    ),     //
.hps_io_qspi_inst_IO1
      .hps_0_io_hps_io_qspi_inst_IO2     ( HPS_FLASH_DATA[2]    ),     //
.hps_io_qspi_inst_IO2
      .hps_0_io_hps_io_qspi_inst_IO3     ( HPS_FLASH_DATA[3]    ),     //
.hps_io_qspi_inst_IO3
      .hps_0_io_hps_io_qspi_inst_SS0     ( HPS_FLASH_NCSO    ),        //
.hps_io_qspi_inst_SS0
      .hps_0_io_hps_io_qspi_inst_CLK     ( HPS_FLASH_DCLK    ),        //
.hps_io_qspi_inst_CLK

      // SD CARD

      .hps_0_io_hps_io_sdio_inst_CMD     ( HPS_SD_CMD    ),           //
.hps_io_sdio_inst_CMD
      .hps_0_io_hps_io_sdio_inst_D0      ( HPS_SD_DATA[0]     ),      //
.hps_io_sdio_inst_D0
      .hps_0_io_hps_io_sdio_inst_D1      ( HPS_SD_DATA[1]     ),      //
.hps_io_sdio_inst_D1
      .hps_0_io_hps_io_sdio_inst_CLK     ( HPS_SD_CLK   ),           //
.hps_io_sdio_inst_CLK
      .hps_0_io_hps_io_sdio_inst_D2      ( HPS_SD_DATA[2]     ),      //
.hps_io_sdio_inst_D2
      .hps_0_io_hps_io_sdio_inst_D3      ( HPS_SD_DATA[3]     ),      //
.hps_io_sdio_inst_D3

      //HPS USB

      .hps_0_io_hps_io_usb1_inst_D0      ( HPS_USB_DATA[0]    ),      //
.hps_io_usb1_inst_D0
      .hps_0_io_hps_io_usb1_inst_D1      ( HPS_USB_DATA[1]    ),      //
.hps_io_usb1_inst_D1
      .hps_0_io_hps_io_usb1_inst_D2      ( HPS_USB_DATA[2]    ),      //
.hps_io_usb1_inst_D2
      .hps_0_io_hps_io_usb1_inst_D3      ( HPS_USB_DATA[3]    ),      //
.hps_io_usb1_inst_D3
      .hps_0_io_hps_io_usb1_inst_D4      ( HPS_USB_DATA[4]    ),      //
.hps_io_usb1_inst_D4
      .hps_0_io_hps_io_usb1_inst_D5      ( HPS_USB_DATA[5]    ),      //
.hps_io_usb1_inst_D5
```

```
      .hps_0_io_hps_io_usb1_inst_D6      ( HPS_USB_DATA[6]    ),      //
.hps_io_usb1_inst_D6
      .hps_0_io_hps_io_usb1_inst_D7      ( HPS_USB_DATA[7]    ),      //
.hps_io_usb1_inst_D7
      .hps_0_io_hps_io_usb1_inst_CLK     ( HPS_USB_CLKOUT    ),       //
.hps_io_usb1_inst_CLK
      .hps_0_io_hps_io_usb1_inst_STP     ( HPS_USB_STP    ),          //
.hps_io_usb1_inst_STP
      .hps_0_io_hps_io_usb1_inst_DIR     ( HPS_USB_DIR    ),          //
.hps_io_usb1_inst_DIR
      .hps_0_io_hps_io_usb1_inst_NXT     ( HPS_USB_NXT    ),          //
.hps_io_usb1_inst_NXT

      //HPS UART
      .hps_0_io_hps_io_uart0_inst_RX     ( HPS_UART_RX    ),          //
.hps_io_uart0_inst_RX
      .hps_0_io_hps_io_uart0_inst_TX     ( HPS_UART_TX    ),          //
.hps_io_uart0_inst_TX

      //HPS GPIO
      .hps_0_io_hps_io_gpio_inst_GPIO53  ( HPS_LED),                 //
.hps_io_gpio_inst_GPIO53
      .hps_0_io_hps_io_gpio_inst_GPIO54  ( HPS_KEY),

      .led_pio_external_connection_export (fpga_led_internal), //
led_pio_external_connection.export


      //HPS DDR3
      .hps_0_ddr_mem_a                         ( HPS_DDR3_ADDR),
//                memory.mem_a
      .hps_0_ddr_mem_ba                        ( HPS_DDR3_BA),
//                .mem_ba
      .hps_0_ddr_mem_ck                        ( HPS_DDR3_CK_P),
//                .mem_ck
      .hps_0_ddr_mem_ck_n                      ( HPS_DDR3_CK_N),
//                .mem_ck_n
      .hps_0_ddr_mem_cke                       ( HPS_DDR3_CKE),
//                .mem_cke
      .hps_0_ddr_mem_cs_n                      ( HPS_DDR3_CS_N),
//                .mem_cs_n
      .hps_0_ddr_mem_ras_n                     ( HPS_DDR3_RAS_N),
//                .mem_ras_n
      .hps_0_ddr_mem_cas_n                     ( HPS_DDR3_CAS_N),
//                .mem_cas_n
      .hps_0_ddr_mem_we_n                      ( HPS_DDR3_WE_N),
//                .mem_we_n
      .hps_0_ddr_mem_reset_n                   ( HPS_DDR3_RESET_N),
//                .mem_reset_n
      .hps_0_ddr_mem_dq                        ( HPS_DDR3_DQ),
//                .mem_dq
```

```
      .hps_0_ddr_mem_dqs                        ( HPS_DDR3_DQS_P),
//                .mem_dqs
      .hps_0_ddr_mem_dqs_n                      ( HPS_DDR3_DQS_N),
//                .mem_dqs_n
      .hps_0_ddr_mem_odt                        ( HPS_DDR3_ODT),
//                .mem_odt
      .hps_0_ddr_mem_dm                         ( HPS_DDR3_DM),
//                .mem_dm
      .hps_0_ddr_oct_rzqin                      ( HPS_DDR3_RZQ)
//                .oct_rzqin

);

endmodule
```

This file should now be set as the top-level entity. Start Analysis and Synthesis to check the design for errors. If this compiles without errors, we can assign the Pins.

Pin Assignment

You can use the following .tcl script to do this automatically. Note that this script is only valid for the DE10 board. This script is

```
package require ::quartus::project

set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK_50
set_location_assignment PIN_AF14 -to CLOCK_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to KEY[3]
set_location_assignment PIN_AJ4 -to KEY[0]
set_location_assignment PIN_AK4 -to KEY[1]
set_location_assignment PIN_AA14 -to KEY[2]
set_location_assignment PIN_AA15 -to KEY[3]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[0]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[1]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[2]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[3]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[4]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[5]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[6]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[7]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[8]
set_instance_assignment -name IO_STANDARD "2.5 V" -to SW[9]
set_location_assignment PIN_AB30 -to SW[0]
set_location_assignment PIN_Y27 -to SW[1]
set_location_assignment PIN_AB28 -to SW[2]
set_location_assignment PIN_AC30 -to SW[3]
```

```
set_location_assignment PIN_W25 -to SW[4]
set_location_assignment PIN_V25 -to SW[5]
set_location_assignment PIN_AC28 -to SW[6]
set_location_assignment PIN_AD30 -to SW[7]
set_location_assignment PIN_AC29 -to SW[8]
set_location_assignment PIN_AA30 -to SW[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to LEDR[9]
set_location_assignment PIN_AA24 -to LEDR[0]
set_location_assignment PIN_AB23 -to LEDR[1]
set_location_assignment PIN_AC23 -to LEDR[2]
set_location_assignment PIN_AD24 -to LEDR[3]
set_location_assignment PIN_AG25 -to LEDR[4]
set_location_assignment PIN_AF25 -to LEDR[5]
set_location_assignment PIN_AE24 -to LEDR[6]
set_location_assignment PIN_AF24 -to LEDR[7]
set_location_assignment PIN_AB22 -to LEDR[8]
set_location_assignment PIN_AC22 -to LEDR[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX0[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX1[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX2[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[4]
```

```
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX3[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX4[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HEX5[6]
set_location_assignment PIN_W17 -to HEX0[0]
set_location_assignment PIN_V18 -to HEX0[1]
set_location_assignment PIN_AG17 -to HEX0[2]
set_location_assignment PIN_AG16 -to HEX0[3]
set_location_assignment PIN_AH17 -to HEX0[4]
set_location_assignment PIN_AG18 -to HEX0[5]
set_location_assignment PIN_AH18 -to HEX0[6]
set_location_assignment PIN_AF16 -to HEX1[0]
set_location_assignment PIN_V16 -to HEX1[1]
set_location_assignment PIN_AE16 -to HEX1[2]
set_location_assignment PIN_AD17 -to HEX1[3]
set_location_assignment PIN_AE18 -to HEX1[4]
set_location_assignment PIN_AE17 -to HEX1[5]
set_location_assignment PIN_V17 -to HEX1[6]
set_location_assignment PIN_AA21 -to HEX2[0]
set_location_assignment PIN_AB17 -to HEX2[1]
set_location_assignment PIN_AA18 -to HEX2[2]
set_location_assignment PIN_Y17 -to HEX2[3]
set_location_assignment PIN_Y18 -to HEX2[4]
set_location_assignment PIN_AF18 -to HEX2[5]
set_location_assignment PIN_W16 -to HEX2[6]
set_location_assignment PIN_Y19 -to HEX3[0]
set_location_assignment PIN_W19 -to HEX3[1]
set_location_assignment PIN_AD19 -to HEX3[2]
set_location_assignment PIN_AA20 -to HEX3[3]
set_location_assignment PIN_AC20 -to HEX3[4]
set_location_assignment PIN_AA19 -to HEX3[5]
set_location_assignment PIN_AD20 -to HEX3[6]
set_location_assignment PIN_AD21 -to HEX4[0]
set_location_assignment PIN_AG22 -to HEX4[1]
set_location_assignment PIN_AE22 -to HEX4[2]
set_location_assignment PIN_AE23 -to HEX4[3]
set_location_assignment PIN_AG23 -to HEX4[4]
set_location_assignment PIN_AF23 -to HEX4[5]
set_location_assignment PIN_AH22 -to HEX4[6]
set_location_assignment PIN_AF21 -to HEX5[0]
```

```
set_location_assignment PIN_AG21 -to HEX5[1]
set_location_assignment PIN_AF20 -to HEX5[2]
set_location_assignment PIN_AG20 -to HEX5[3]
set_location_assignment PIN_AE19 -to HEX5[4]
set_location_assignment PIN_AF19 -to HEX5[5]
set_location_assignment PIN_AB21 -to HEX5[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CKE
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_ADDR[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_BA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_BA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_DQ[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_LDQM
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_UDQM
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_WE_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_CAS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to DRAM_RAS_N
set_location_assignment PIN_AH12 -to DRAM_CLK
set_location_assignment PIN_AK13 -to DRAM_CKE
set_location_assignment PIN_AK14 -to DRAM_ADDR[0]
set_location_assignment PIN_AH14 -to DRAM_ADDR[1]
set_location_assignment PIN_AG15 -to DRAM_ADDR[2]
set_location_assignment PIN_AE14 -to DRAM_ADDR[3]
set_location_assignment PIN_AB15 -to DRAM_ADDR[4]
```

```
set_location_assignment PIN_AC14 -to DRAM_ADDR[5]
set_location_assignment PIN_AD14 -to DRAM_ADDR[6]
set_location_assignment PIN_AF15 -to DRAM_ADDR[7]
set_location_assignment PIN_AH15 -to DRAM_ADDR[8]
set_location_assignment PIN_AG13 -to DRAM_ADDR[9]
set_location_assignment PIN_AG12 -to DRAM_ADDR[10]
set_location_assignment PIN_AH13 -to DRAM_ADDR[11]
set_location_assignment PIN_AJ14 -to DRAM_ADDR[12]
set_location_assignment PIN_AF13 -to DRAM_BA[0]
set_location_assignment PIN_AJ12 -to DRAM_BA[1]
set_location_assignment PIN_AK6 -to DRAM_DQ[0]
set_location_assignment PIN_AJ7 -to DRAM_DQ[1]
set_location_assignment PIN_AK7 -to DRAM_DQ[2]
set_location_assignment PIN_AK8 -to DRAM_DQ[3]
set_location_assignment PIN_AK9 -to DRAM_DQ[4]
set_location_assignment PIN_AG10 -to DRAM_DQ[5]
set_location_assignment PIN_AK11 -to DRAM_DQ[6]
set_location_assignment PIN_AJ11 -to DRAM_DQ[7]
set_location_assignment PIN_AH10 -to DRAM_DQ[8]
set_location_assignment PIN_AJ10 -to DRAM_DQ[9]
set_location_assignment PIN_AJ9 -to DRAM_DQ[10]
set_location_assignment PIN_AH9 -to DRAM_DQ[11]
set_location_assignment PIN_AH8 -to DRAM_DQ[12]
set_location_assignment PIN_AH7 -to DRAM_DQ[13]
set_location_assignment PIN_AJ6 -to DRAM_DQ[14]
set_location_assignment PIN_AJ5 -to DRAM_DQ[15]
set_location_assignment PIN_AB13 -to DRAM_LDQM
set_location_assignment PIN_AK12 -to DRAM_UDQM
set_location_assignment PIN_AG11 -to DRAM_CS_N
set_location_assignment PIN_AA13 -to DRAM_WE_N
set_location_assignment PIN_AF11 -to DRAM_CAS_N
set_location_assignment PIN_AE13 -to DRAM_RAS_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_CLK27
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_HS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_VS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_DATA[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to TD_RESET_N
set_location_assignment PIN_AC18 -to TD_CLK27
set_location_assignment PIN_AH28 -to TD_HS
set_location_assignment PIN_AG28 -to TD_VS
set_location_assignment PIN_AG27 -to TD_DATA[0]
set_location_assignment PIN_AF28 -to TD_DATA[1]
set_location_assignment PIN_AE28 -to TD_DATA[2]
set_location_assignment PIN_AE27 -to TD_DATA[3]
set_location_assignment PIN_AE26 -to TD_DATA[4]
```

```
set_location_assignment PIN_AD27 -to TD_DATA[5]
set_location_assignment PIN_AD26 -to TD_DATA[6]
set_location_assignment PIN_AD25 -to TD_DATA[7]
set_location_assignment PIN_AC27 -to TD_RESET_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_HS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_VS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_R[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_G[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_B[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_BLANK_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to VGA_SYNC_N
set_location_assignment PIN_AK21 -to VGA_CLK
set_location_assignment PIN_AK19 -to VGA_HS
set_location_assignment PIN_AK18 -to VGA_VS
set_location_assignment PIN_AK29 -to VGA_R[0]
set_location_assignment PIN_AK28 -to VGA_R[1]
set_location_assignment PIN_AK27 -to VGA_R[2]
set_location_assignment PIN_AJ27 -to VGA_R[3]
set_location_assignment PIN_AH27 -to VGA_R[4]
set_location_assignment PIN_AF26 -to VGA_R[5]
set_location_assignment PIN_AG26 -to VGA_R[6]
set_location_assignment PIN_AJ26 -to VGA_R[7]
set_location_assignment PIN_AK26 -to VGA_G[0]
set_location_assignment PIN_AJ25 -to VGA_G[1]
set_location_assignment PIN_AH25 -to VGA_G[2]
set_location_assignment PIN_AK24 -to VGA_G[3]
set_location_assignment PIN_AJ24 -to VGA_G[4]
set_location_assignment PIN_AH24 -to VGA_G[5]
set_location_assignment PIN_AK23 -to VGA_G[6]
set_location_assignment PIN_AH23 -to VGA_G[7]
```

```
set_location_assignment PIN_AJ21 -to VGA_B[0]
set_location_assignment PIN_AJ20 -to VGA_B[1]
set_location_assignment PIN_AH20 -to VGA_B[2]
set_location_assignment PIN_AJ19 -to VGA_B[3]
set_location_assignment PIN_AH19 -to VGA_B[4]
set_location_assignment PIN_AJ17 -to VGA_B[5]
set_location_assignment PIN_AJ16 -to VGA_B[6]
set_location_assignment PIN_AK16 -to VGA_B[7]
set_location_assignment PIN_AK22 -to VGA_BLANK_N
set_location_assignment PIN_AJ22 -to VGA_SYNC_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_BCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_XCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_ADCLRCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_ADCDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_DACLRCK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to AUD_DACDAT
set_location_assignment PIN_AF30 -to AUD_BCLK
set_location_assignment PIN_AH30 -to AUD_XCK
set_location_assignment PIN_AH29 -to AUD_ADCLRCK
set_location_assignment PIN_AJ29 -to AUD_ADCDAT
set_location_assignment PIN_AG30 -to AUD_DACLRCK
set_location_assignment PIN_AF29 -to AUD_DACDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to IRDA_TXD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to IRDA_RXD
set_location_assignment PIN_W21 -to IRDA_TXD
set_location_assignment PIN_W20 -to IRDA_RXD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_CLK2
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_DAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to PS2_DAT2
set_location_assignment PIN_AB25 -to PS2_CLK
set_location_assignment PIN_AC25 -to PS2_CLK2
set_location_assignment PIN_AA25 -to PS2_DAT
set_location_assignment PIN_AB26 -to PS2_DAT2
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_DOUT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_DIN
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to ADC_CONVST
set_location_assignment PIN_W24 -to ADC_SCLK
set_location_assignment PIN_V23 -to ADC_DOUT
set_location_assignment PIN_W22 -to ADC_DIN
set_location_assignment PIN_Y21 -to ADC_CONVST
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to FPGA_I2C_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to FPGA_I2C_SDAT
set_location_assignment PIN_Y24 -to FPGA_I2C_SCLK
set_location_assignment PIN_Y23 -to FPGA_I2C_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[5]
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set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[8]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[9]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[10]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[11]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[12]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[13]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[14]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[15]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[16]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[17]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[18]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[19]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[20]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[21]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[22]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[23]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[24]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[25]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[26]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[27]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[28]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[29]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[30]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[31]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[32]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[33]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[34]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to GPIO[35]
set_location_assignment PIN_W15 -to GPIO[0]
set_location_assignment PIN_AK2 -to GPIO[1]
set_location_assignment PIN_Y16 -to GPIO[2]
set_location_assignment PIN_AK3 -to GPIO[3]
set_location_assignment PIN_AJ1 -to GPIO[4]
set_location_assignment PIN_AJ2 -to GPIO[5]
set_location_assignment PIN_AH2 -to GPIO[6]
set_location_assignment PIN_AH3 -to GPIO[7]
set_location_assignment PIN_AH4 -to GPIO[8]
set_location_assignment PIN_AH5 -to GPIO[9]
set_location_assignment PIN_AG1 -to GPIO[10]
set_location_assignment PIN_AG2 -to GPIO[11]
set_location_assignment PIN_AG3 -to GPIO[12]
set_location_assignment PIN_AG5 -to GPIO[13]
set_location_assignment PIN_AG6 -to GPIO[14]
set_location_assignment PIN_AG7 -to GPIO[15]
set_location_assignment PIN_AG8 -to GPIO[16]
set_location_assignment PIN_AF4 -to GPIO[17]
set_location_assignment PIN_AF5 -to GPIO[18]
set_location_assignment PIN_AF6 -to GPIO[19]
set_location_assignment PIN_AF8 -to GPIO[20]
set_location_assignment PIN_AF9 -to GPIO[21]
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set_location_assignment PIN_AF10 -to GPIO[22]
set_location_assignment PIN_AE7 -to GPIO[23]
set_location_assignment PIN_AE9 -to GPIO[24]
set_location_assignment PIN_AE11 -to GPIO[25]
set_location_assignment PIN_AE12 -to GPIO[26]
set_location_assignment PIN_AD7 -to GPIO[27]
set_location_assignment PIN_AD9 -to GPIO[28]
set_location_assignment PIN_AD10 -to GPIO[29]
set_location_assignment PIN_AD11 -to GPIO[30]
set_location_assignment PIN_AD12 -to GPIO[31]
set_location_assignment PIN_AC9 -to GPIO[32]
set_location_assignment PIN_AC12 -to GPIO[33]
set_location_assignment PIN_AB12 -to GPIO[34]
set_location_assignment PIN_AA12 -to GPIO[35]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKIN_P1
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKIN_N1
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKIN_P2
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKIN_N2
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKOUT_P1
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKOUT_N1
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKOUT_P2
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKOUT_N2
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[0]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[1]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[2]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[3]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[4]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[5]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[6]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[7]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[8]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[9]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[10]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[11]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[12]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[13]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[14]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[15]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_P[16]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[0]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[1]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[2]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[3]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[4]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[5]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[6]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[7]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[8]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[9]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[10]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[11]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[12]
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```
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[13]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[14]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[15]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_TX_D_N[16]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[0]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[1]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[2]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[3]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[4]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[5]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[6]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[7]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[8]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[9]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[10]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[11]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[12]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[13]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[14]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[15]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_P[16]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[0]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[1]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[2]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[3]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[4]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[5]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[6]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[7]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[8]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[9]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[10]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[11]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[12]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[13]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[14]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[15]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_RX_D_N[16]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKIN0
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_CLKOUT0
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_D[0]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_D[1]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_D[2]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_D[3]
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_SCL
set_instance_assignment -name IO_STANDARD "2.5 V" -to HSMC_SDA
set_location_assignment PIN_AA26 -to HSMC_CLKIN_P1
set_location_assignment PIN_AB27 -to HSMC_CLKIN_N1
set_location_assignment PIN_H15 -to HSMC_CLKIN_P2
set_location_assignment PIN_G15 -to HSMC_CLKIN_N2
set_location_assignment PIN_E7 -to HSMC_CLKOUT_P1
set_location_assignment PIN_E6 -to HSMC_CLKOUT_N1
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set_location_assignment PIN_A11 -to HSMC_CLKOUT_P2
set_location_assignment PIN_A10 -to HSMC_CLKOUT_N2
set_location_assignment PIN_A9 -to HSMC_TX_D_P[0]
set_location_assignment PIN_E8 -to HSMC_TX_D_P[1]
set_location_assignment PIN_G7 -to HSMC_TX_D_P[2]
set_location_assignment PIN_D6 -to HSMC_TX_D_P[3]
set_location_assignment PIN_D5 -to HSMC_TX_D_P[4]
set_location_assignment PIN_E3 -to HSMC_TX_D_P[5]
set_location_assignment PIN_E4 -to HSMC_TX_D_P[6]
set_location_assignment PIN_C3 -to HSMC_TX_D_P[7]
set_location_assignment PIN_E1 -to HSMC_TX_D_P[8]
set_location_assignment PIN_D2 -to HSMC_TX_D_P[9]
set_location_assignment PIN_B2 -to HSMC_TX_D_P[10]
set_location_assignment PIN_A4 -to HSMC_TX_D_P[11]
set_location_assignment PIN_A6 -to HSMC_TX_D_P[12]
set_location_assignment PIN_C7 -to HSMC_TX_D_P[13]
set_location_assignment PIN_C8 -to HSMC_TX_D_P[14]
set_location_assignment PIN_C12 -to HSMC_TX_D_P[15]
set_location_assignment PIN_B13 -to HSMC_TX_D_P[16]
set_location_assignment PIN_A8 -to HSMC_TX_D_N[0]
set_location_assignment PIN_D7 -to HSMC_TX_D_N[1]
set_location_assignment PIN_F6 -to HSMC_TX_D_N[2]
set_location_assignment PIN_C5 -to HSMC_TX_D_N[3]
set_location_assignment PIN_C4 -to HSMC_TX_D_N[4]
set_location_assignment PIN_E2 -to HSMC_TX_D_N[5]
set_location_assignment PIN_D4 -to HSMC_TX_D_N[6]
set_location_assignment PIN_B3 -to HSMC_TX_D_N[7]
set_location_assignment PIN_D1 -to HSMC_TX_D_N[8]
set_location_assignment PIN_C2 -to HSMC_TX_D_N[9]
set_location_assignment PIN_B1 -to HSMC_TX_D_N[10]
set_location_assignment PIN_A3 -to HSMC_TX_D_N[11]
set_location_assignment PIN_A5 -to HSMC_TX_D_N[12]
set_location_assignment PIN_B7 -to HSMC_TX_D_N[13]
set_location_assignment PIN_B8 -to HSMC_TX_D_N[14]
set_location_assignment PIN_B11 -to HSMC_TX_D_N[15]
set_location_assignment PIN_A13 -to HSMC_TX_D_N[16]
set_location_assignment PIN_G12 -to HSMC_RX_D_P[0]
set_location_assignment PIN_K12 -to HSMC_RX_D_P[1]
set_location_assignment PIN_G10 -to HSMC_RX_D_P[2]
set_location_assignment PIN_J10 -to HSMC_RX_D_P[3]
set_location_assignment PIN_K7 -to HSMC_RX_D_P[4]
set_location_assignment PIN_J7 -to HSMC_RX_D_P[5]
set_location_assignment PIN_H8 -to HSMC_RX_D_P[6]
set_location_assignment PIN_F9 -to HSMC_RX_D_P[7]
set_location_assignment PIN_F11 -to HSMC_RX_D_P[8]
set_location_assignment PIN_B6 -to HSMC_RX_D_P[9]
set_location_assignment PIN_E9 -to HSMC_RX_D_P[10]
set_location_assignment PIN_E12 -to HSMC_RX_D_P[11]
set_location_assignment PIN_D11 -to HSMC_RX_D_P[12]
set_location_assignment PIN_C13 -to HSMC_RX_D_P[13]
set_location_assignment PIN_F13 -to HSMC_RX_D_P[14]
set_location_assignment PIN_H14 -to HSMC_RX_D_P[15]
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set_location_assignment PIN_F15 -to HSMC_RX_D_P[16]
set_location_assignment PIN_G11 -to HSMC_RX_D_N[0]
set_location_assignment PIN_J12 -to HSMC_RX_D_N[1]
set_location_assignment PIN_F10 -to HSMC_RX_D_N[2]
set_location_assignment PIN_J9 -to HSMC_RX_D_N[3]
set_location_assignment PIN_K8 -to HSMC_RX_D_N[4]
set_location_assignment PIN_H7 -to HSMC_RX_D_N[5]
set_location_assignment PIN_G8 -to HSMC_RX_D_N[6]
set_location_assignment PIN_F8 -to HSMC_RX_D_N[7]
set_location_assignment PIN_E11 -to HSMC_RX_D_N[8]
set_location_assignment PIN_B5 -to HSMC_RX_D_N[9]
set_location_assignment PIN_D9 -to HSMC_RX_D_N[10]
set_location_assignment PIN_D12 -to HSMC_RX_D_N[11]
set_location_assignment PIN_D10 -to HSMC_RX_D_N[12]
set_location_assignment PIN_B12 -to HSMC_RX_D_N[13]
set_location_assignment PIN_E13 -to HSMC_RX_D_N[14]
set_location_assignment PIN_G13 -to HSMC_RX_D_N[15]
set_location_assignment PIN_F14 -to HSMC_RX_D_N[16]
set_location_assignment PIN_J14 -to HSMC_CLKIN0
set_location_assignment PIN_AD29 -to HSMC_CLKOUT0
set_location_assignment PIN_C10 -to HSMC_D[0]
set_location_assignment PIN_H13 -to HSMC_D[1]
set_location_assignment PIN_C9 -to HSMC_D[2]
set_location_assignment PIN_H12 -to HSMC_D[3]
set_location_assignment PIN_AA28 -to HSMC_SCL
set_location_assignment PIN_AE29 -to HSMC_SDA
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK2_50
set_location_assignment PIN_AA16 -to CLOCK2_50
set_instance_assignment -name IO_STANDARD "2.5 V" -to CLOCK3_50
set_location_assignment PIN_Y26 -to CLOCK3_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to CLOCK4_50
set_location_assignment PIN_K14 -to CLOCK4_50
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_CONV_USB_N
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[0]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[1]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[2]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[3]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[4]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[5]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[6]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[7]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[8]
-tag __hps_sdram_p0
```

```
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[9]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[10]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[11]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[12]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[13]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ADDR[14]
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_BA[0] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_BA[1] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_BA[2] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_CAS_N -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_CKE -tag
__hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_CK_N -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_CK_P -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_CS_N -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DM[0] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DM[1] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DM[2] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DM[3] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[0] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[1] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[2] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[3] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[4] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[5] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[6] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[7] -
tag __hps_sdram_p0
```

```
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[8] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[9] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[10] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[11] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[12] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[13] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[14] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[15] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[16] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[17] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[18] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[19] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[20] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[21] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[22] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[23] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[24] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[25] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[26] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[27] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[28] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[29] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[30] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_DQ[31] -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_N[0] -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_N[1] -tag __hps_sdram_p0
```

```
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_N[2] -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_N[3] -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_P[0] -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_P[1] -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_P[2] -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "DIFFERENTIAL 1.5-V SSTL CLASS I" -to
HPS_DDR3_DQS_P[3] -tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_ODT -tag
__hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_RAS_N -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_RESET_N
-tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_RZQ -tag
__hps_sdram_p0
set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to HPS_DDR3_WE_N -
tag __hps_sdram_p0
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_GTX_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_INT_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_MDC
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_MDIO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_RX_DV
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_ENET_TX_EN
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_DCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_FLASH_NCSO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_GSENSOR_INT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C1_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C1_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C2_SCLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C2_SDAT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_I2C_CONTROL
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_KEY
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LCM_BK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LCM_D_C
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set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LCM_RST_N
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LCM_SPIM_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LCM_SPIM_MOSI
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LCM_SPIM_SS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LCM_SPIM_MISO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LED
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_LTC_GPIO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_CMD
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SD_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_CLK
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_MISO
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_MOSI
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_SPIM_SS
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_UART_RX
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_UART_TX
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_CLKOUT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[0]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[1]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[2]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[3]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[4]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[5]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[6]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DATA[7]
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_DIR
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_NXT
set_instance_assignment -name IO_STANDARD "3.3-V LVTTL" -to HPS_USB_STP
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[0] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[0] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[1] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[1] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[2] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[2] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[3] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[3] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[4] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[4] -tag __hps_sdram_p0
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set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[5] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[5] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[6] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[6] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[7] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[7] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[8] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[8] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[9] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[9] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[10] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[10] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[11] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[11] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[12] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[12] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[13] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[13] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[14] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[14] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[15] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[15] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[16] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[16] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[17] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[17] -tag __hps_sdram_p0
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```
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[18] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[18] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[19] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[19] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[20] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[20] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[21] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[21] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[22] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[22] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[23] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[23] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[24] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[24] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[25] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[25] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[26] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[26] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[27] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[27] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[28] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[28] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[29] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[29] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[30] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[30] -tag __hps_sdram_p0
```

```
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQ[31] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQ[31] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_P[0] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_P[0] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_P[1] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_P[1] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_P[2] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_P[2] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_P[3] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_P[3] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_N[0] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_N[0] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_N[1] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_N[1] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_N[2] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_N[2] -tag __hps_sdram_p0
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH
CALIBRATION" -to HPS_DDR3_DQS_N[3] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DQS_N[3] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITHOUT
CALIBRATION" -to HPS_DDR3_CK_P -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITHOUT
CALIBRATION" -to HPS_DDR3_CK_N -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[0] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[10] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[11] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[12] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[13] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[14] -tag __hps_sdram_p0
```

```
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[1] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[2] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[3] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[4] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[5] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[6] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[7] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[8] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ADDR[9] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_BA[0] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_BA[1] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_BA[2] -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_CAS_N -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_CKE -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_CS_N -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_ODT -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_RAS_N -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_WE_N -tag __hps_sdram_p0
set_instance_assignment -name CURRENT_STRENGTH_NEW "MAXIMUM CURRENT" -to
HPS_DDR3_RESET_N -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DM[0] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DM[1] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DM[2] -tag __hps_sdram_p0
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION"
-to HPS_DDR3_DM[3] -tag __hps_sdram_p0
```

You might see, why you would use a .tcl script instead of doing this manually ;)

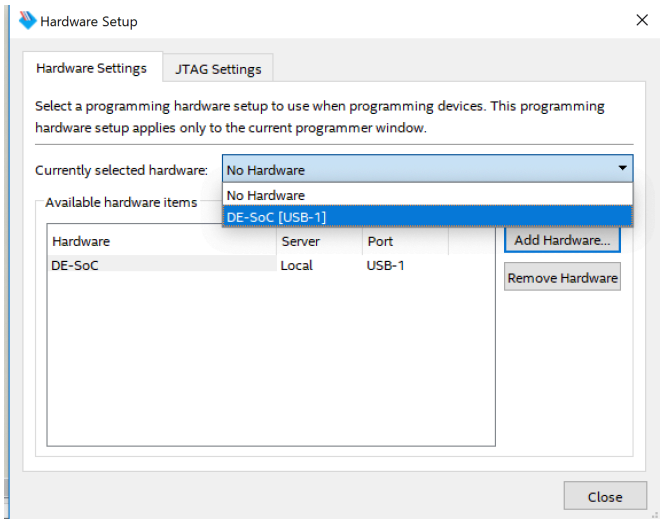
The script can be opened by selecting Tools->Tcl Scripts… Then add the .tcl script to the project and final click on Run. It might take a while and Quartus might become unresponsive, so have patience. This script should be saved for further projects, as we need to assign the pins again with every new project.

Now we can compile the System with Processing->Start Compilation.

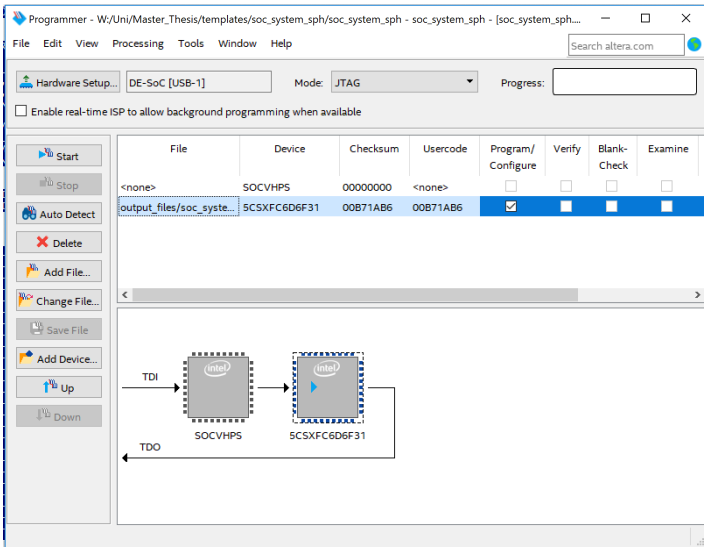
// TODO: create .rbf file to program FPGA from ARM Core

// TODO: create custom Linux

After the compilation has finished, we can program the FGPA with the .sof by clicking on Tools->Programmer and selecting the FPGA. If the FPGA is not shown, click on the Hardware Setup button in the top left corner and select the DE-SoC in the dropdown menu, then click on the DE-SoC in the list to use it. Click close to return to the programmer.



To program the FPGA double click on the File column and select the .sof file that was created in the output_files folder. Check the Program/Configure box and click Start.



Using ARM DS-5 to program ARM core

Launch the ARM DS-5 IDE by opening the Altera embedded shell, that is found under C:\altera\<version>\embedded (if you are using a newer version of the EDS, replace altera with intel).

execute the `eclipse` command to open ARM DS-5. If this command (or any following command) does not work, you need to add the respective folders to your path. You can do this with the following command:

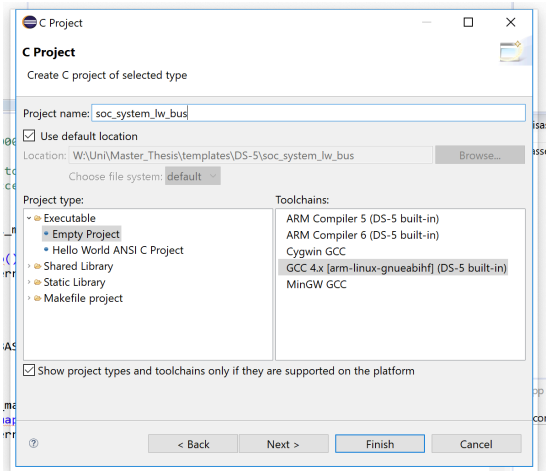
```
set PATH=%PATH%;C:\your\path\here\
```

The standard path to DS-5 is as follows: C:\Program Files\DS-5 v5.23.1\bin
(your version might vary)

Opening ARM DS-5 with the embedded command shell enables additional functionality.

Setting up the eclipse project

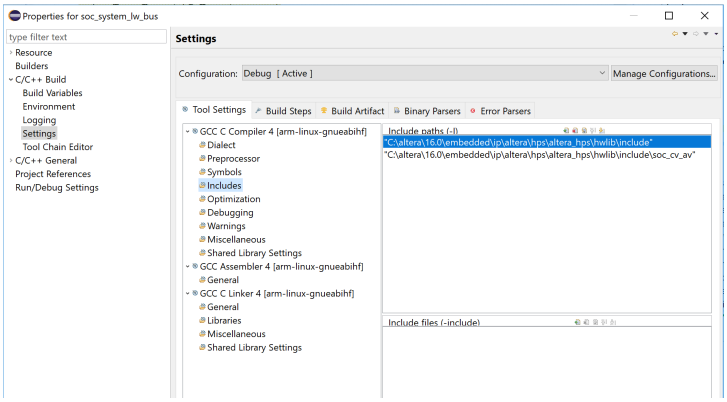
In DS-5 create a new project by selecting File->New-C Project.
Choose the GCC 4.x Toolchain and an empty project template and click Finish.



Right click your new project and select properties.
Under C/C++ Build->Settings->GCC C Compiler->Includes add the following two Include paths:

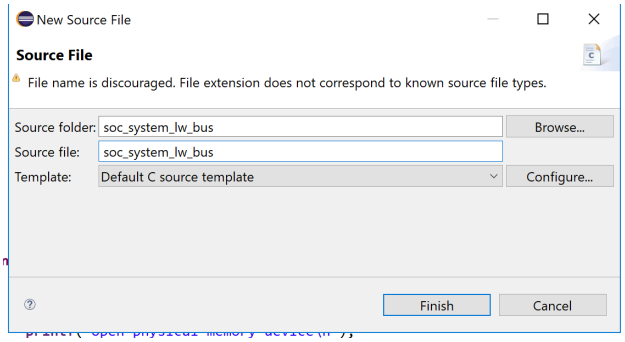
```
<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/include
```

```
<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/include/soc_cv_av
```



Click Apply, then OK.

We can now create the source files. Right-click on the project and select new source file.



Provide a name and click Finish. Add the following code to the file:

```
#include <assert.h>
#include <errno.h>
#include <fcntl.h>
#include <stdbool.h>
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <sys/mman.h>
#include <unistd.h>



#include "alt_generalpurpose_io.h"
#include "YOUR_CREATED_HEADER_FILE.h"
#include "hwlib.h"
#include "socal/alt_gpio.h"
#include "socal/hps.h"
#include "socal/socal.h"
#include "hps_soc_system.h"

// physical memory file descriptor
int fd_dev_mem = 0;
```

```
// memory-mapped peripherals
void   *hps_gpio     = NULL;
size_t hps_gpio_span = ALT_GPIO1_UB_ADDR - ALT_GPIO1_LB_ADDR + 1;
size_t hps_gpio_ofst = ALT_GPIO1_OFST;

void   *h2f_lw_axi_master     = NULL;
size_t h2f_lw_axi_master_span = ALT_LWFPGASLVS_UB_ADDR - ALT_LWFPGASLVS_LB_ADDR +
1;
size_t h2f_lw_axi_master_ofst = ALT_LWFPGASLVS_OFST;

void *fpga_leds = NULL;

void open_physical_memory_device() {
    fd_dev_mem = open("/dev/mem", O_RDWR | O_SYNC);
    if(fd_dev_mem  == -1) {
        printf("ERROR: could not open \"/dev/mem\".\n");
        printf("errno = %s\n", strerror(errno));
        exit(EXIT_FAILURE);
    }
}


void close_physical_memory_device() {
    close(fd_dev_mem);
}

void mmap_hps_peripherals() {
    hps_gpio = mmap(NULL, hps_gpio_span, PROT_READ | PROT_WRITE, MAP_SHARED,
fd_dev_mem, hps_gpio_ofst);
    if (hps_gpio == MAP_FAILED) {
        printf("Error: hps_gpio mmap() failed.\n");
        printf("    errno = %s\n", strerror(errno));
        close(fd_dev_mem);
        exit(EXIT_FAILURE);
    }
}

void munmap_hps_peripherals() {
    if (munmap(hps_gpio, hps_gpio_span) != 0) {
        printf("Error: hps_gpio munmap() failed\n");
        printf("    errno = %s\n", strerror(errno));
        close(fd_dev_mem);
        exit(EXIT_FAILURE);
    }

    hps_gpio = NULL;
}

void mmap_fpga_peripherals() {
    h2f_lw_axi_master = mmap(NULL, h2f_lw_axi_master_span, PROT_READ |
PROT_WRITE, MAP_SHARED, fd_dev_mem, h2f_lw_axi_master_ofst);
```

```
    if (h2f_lw_axi_master == MAP_FAILED) {
        printf("Error: h2f_lw_axi_master mmap() failed.\n");
        printf("    errno = %s\n", strerror(errno));
        close(fd_dev_mem);
        exit(EXIT_FAILURE);
    }

    fpga_leds = h2f_lw_axi_master + LED_PIO_BASE;
}

void munmap_fpga_peripherals() {
    if (munmap(h2f_lw_axi_master, h2f_lw_axi_master_span) != 0) {
        printf("Error: h2f_lw_axi_master munmap() failed\n");
        printf("    errno = %s\n", strerror(errno));
        close(fd_dev_mem);
        exit(EXIT_FAILURE);
    }

    h2f_lw_axi_master = NULL;
    fpga_leds         = NULL;
}

void mmap_peripherals() {
    mmap_hps_peripherals();
    mmap_fpga_peripherals();
}

void munmap_peripherals() {
    munmap_hps_peripherals();
    munmap_fpga_peripherals();
}


void handle_fpga_leds() {


    if(alt_read_word(fpga_leds)== NULL)
    {
        printf("Read from fpga_leds failed!");
    }
    else
    {
            uint32_t leds_mask = alt_read_word(fpga_leds);

        if (leds_mask != (0x01 << (LED_PIO_DATA_WIDTH - 1))) {
            // rotate leds
            leds_mask <<= 1;
        } else {
            // reset leds
            leds_mask = 0x1;
        }

        alt_write_word(fpga_leds, leds_mask);
```

```
    }
}


int main(void)
{
    printf("Program Started");

    printf("Open physical memory device\n");
    open_physical_memory_device();

    printf("memory map peripherals\n");
    mmap_peripherals();

    printf("set FPGA LEDs\n");
    while(true)
    {
        handle_fpga_leds();
        usleep(ALT_MICROSECS_IN_A_SEC/10);
    }

       munmap_peripherals();
       close_physical_memory_device();

    // everything is ok
    return 100;
}
```

Next, we need to include all the required header and source files. First we will create a board support header file using the embedded shell. Navigate to your quartus project folder in the embedded shell and execute the sopc-create-header-files command. If it is not working, add the following directory to your path:

`C:\intelFPGA_lite(or altera)\<version>\quartus\sopc_builder\bin`

This command will create the required header files. Copy the header files for your top-level entity into you eclipse project and include it in the code instead of `YOUR_CREATED_HEADER_FILE`.

Next, we need to copy the required HWLib files from the altera install directory. The files can be found in the following directory:

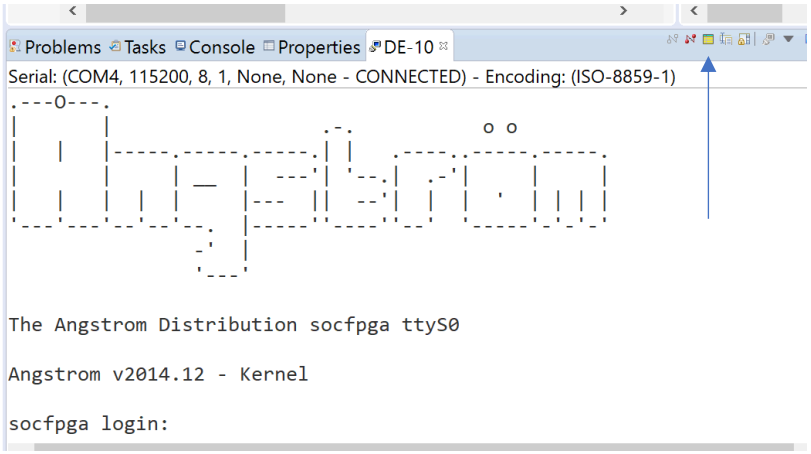
`<altera_install_directory>/<version>/embedded/ip/altera/hps/altera_hps/hwlib/src`

In this example we will only access a gpio register, so you just need to copy the `alt_generalpurpose_io.c` file to your project.

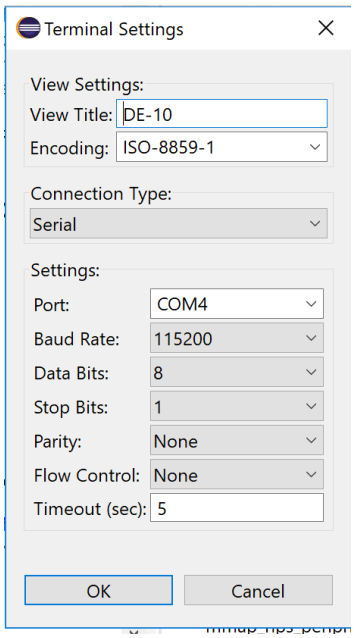
After adding this file, you can compile your project.

Creating a Remote Debug Connection to the board

If the board is connected, the MSEL jumpers are set to 01010, and a valid Linux installation is on the SD Card, we can connect to the Linux system via the UART interface as well as copy files onto the SD Card via SSH. First, we will configure the serial connection. By clicking on the small yellow box near the command line, you can configure the settings for the serial connection.



Use the following settings, and you should see a login prompt for the Linux system.

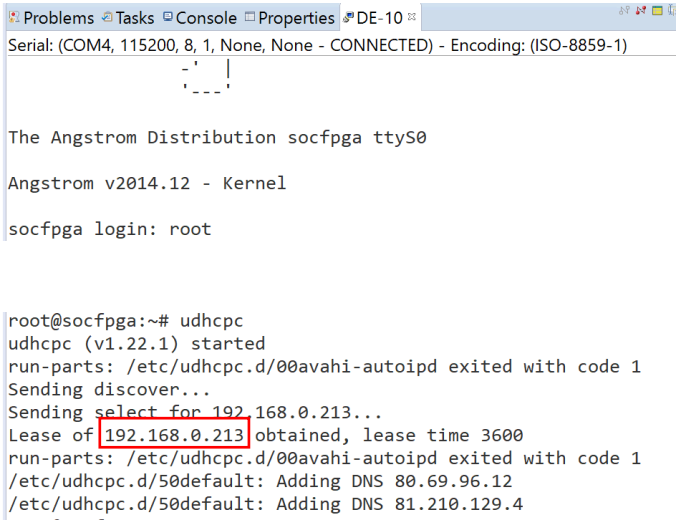


Note that you Com Port may vary, you can find out your Com Port e.g. through the windows device manager. The login username name is root and the password is empty, so simply hit enter. After this you need to make sure, that the DE10 board is connected to a router with an ethernet cable.

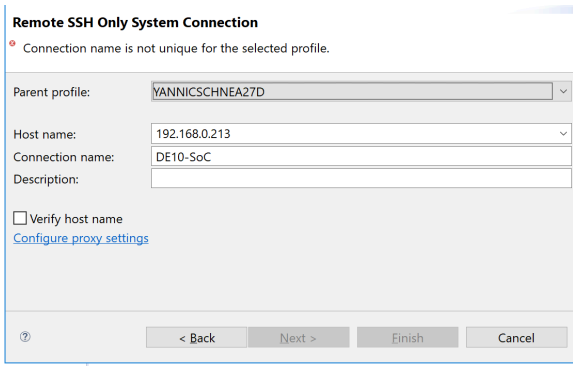
Now you can request an IP by entering the following command in the serial terminal.

udhcpc

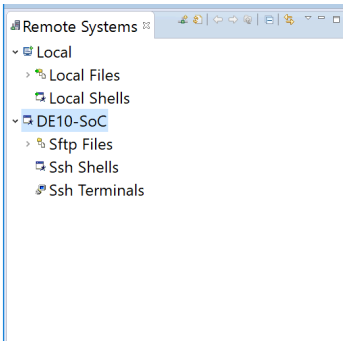
You can now see the IP of the board:



Now we can SSH into the system. For this select File->New->other…->Remote System Explorer->Connection
Select SSH Only
Enter the IP that you just obtained for the Host name and choose a name for this connection and click on Finish.

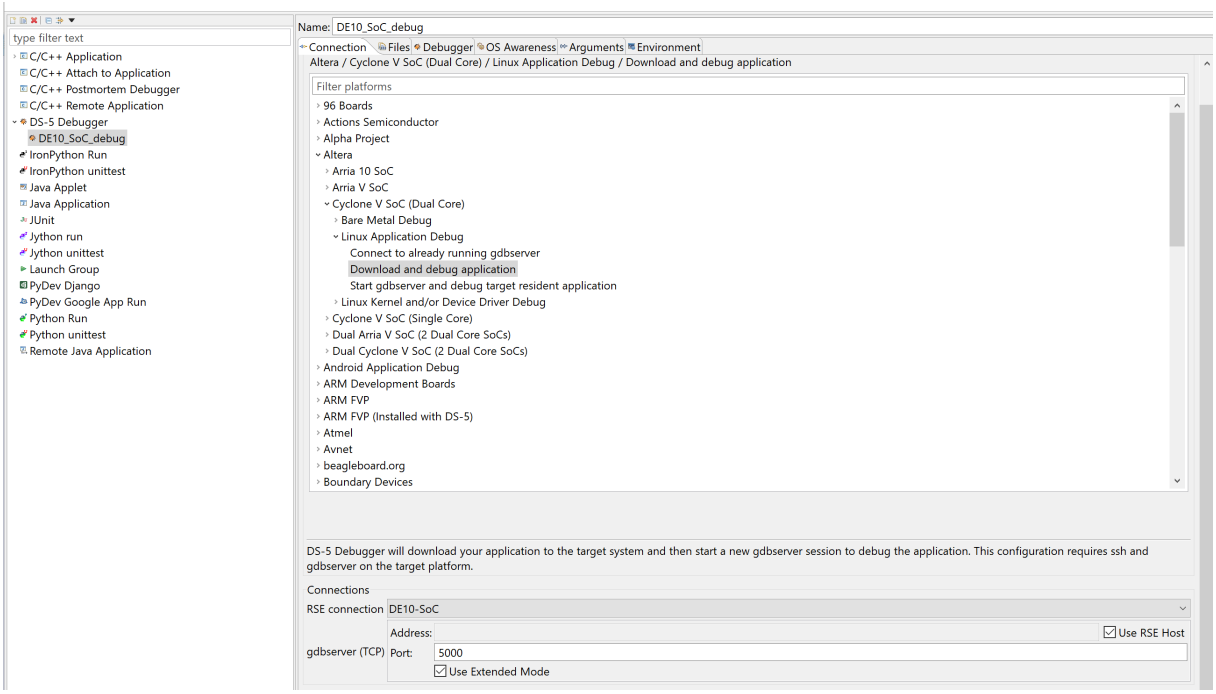


You can now open the Remote System Explorer by selecting Window->Open Perspective-> Other… -> Remote System Explorer.



Creating a debug configuration

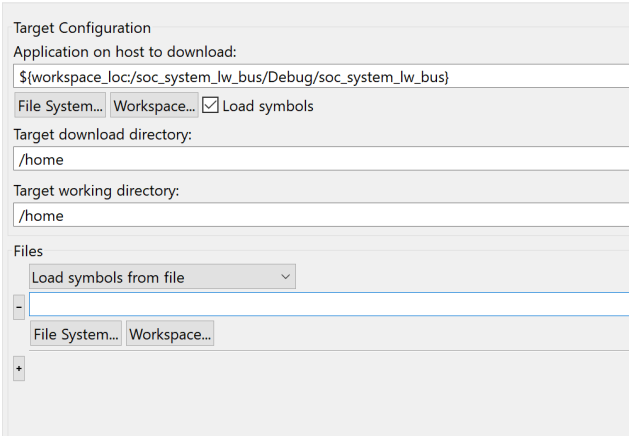
Right-click on your project and select Debug As->Debug Configurations…
Select DS-5 Debugger
Create a new configuration
For the connection select: Altera-> Cyclone V SoC (Dual Core)->Linux Application Debug-> Download and debug application.
Scroll down a bit and Select the DE10-SoC as RES connection.



In the files tab under Application on host to download:
Click on Workspace… and select the binary file.

It should like something like this:
`${workspace_loc:/soc_system_lw_bus/Debug/soc_system_lw_bus}`

Set the target download directory to /home

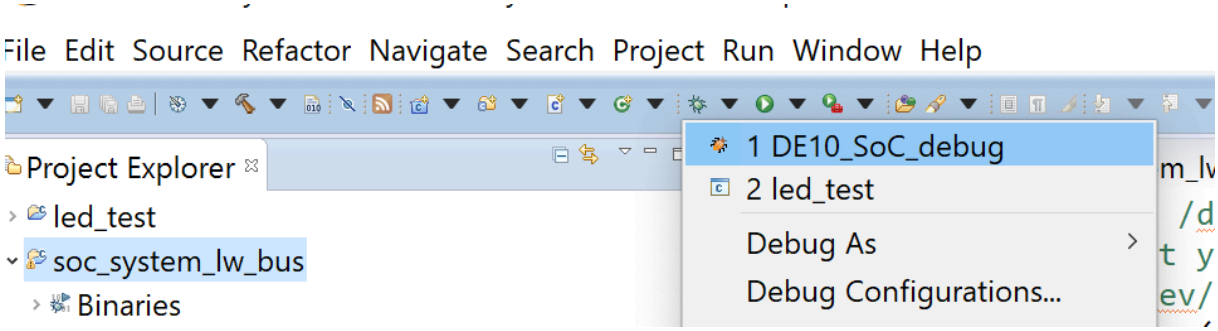


In the debugger tab select Debug from symbol -> main

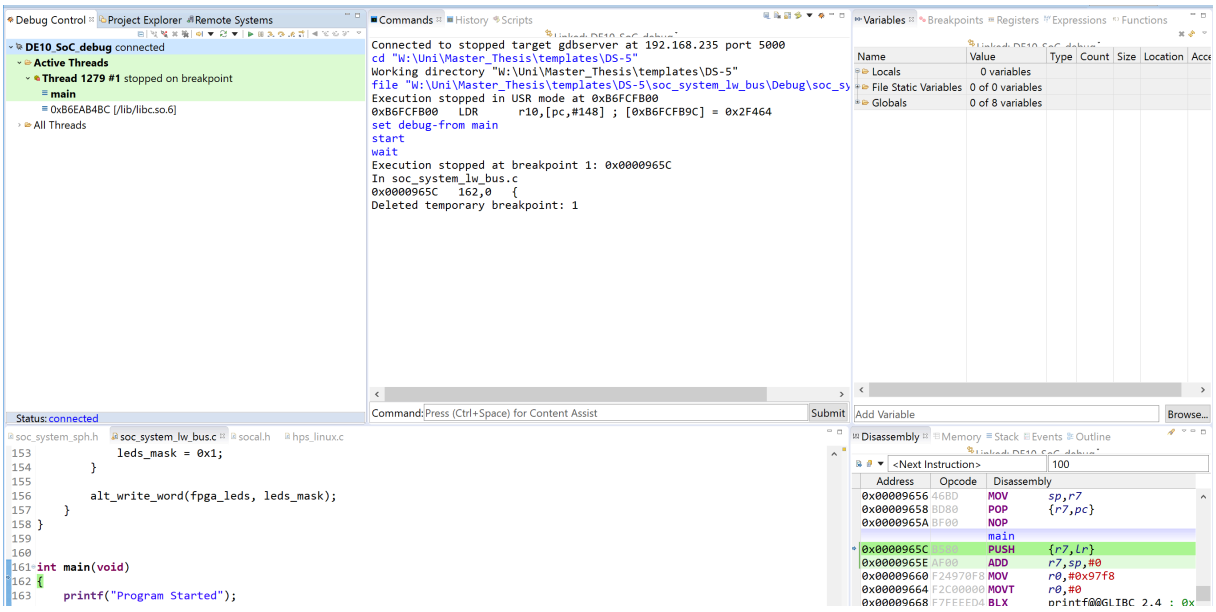
Click apply and close.

Launching the code in the debugger

You can now start the debugging process by selecting your debug configuration from the menu bar.



You are then prompted to insert the password again and accept the connection.



If everything worked out, you should see the perspective in the picture above. Remember that the FPGA needs to be programmed for this to work. This is the case if the first 4 LEDs are lighting up. If you press the green play button now, the LEDs start to blink one after another.

This concludes the setup of the basic system.