华南理工大学

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Intro to Computer Science and Software Engineering

Computer Organization

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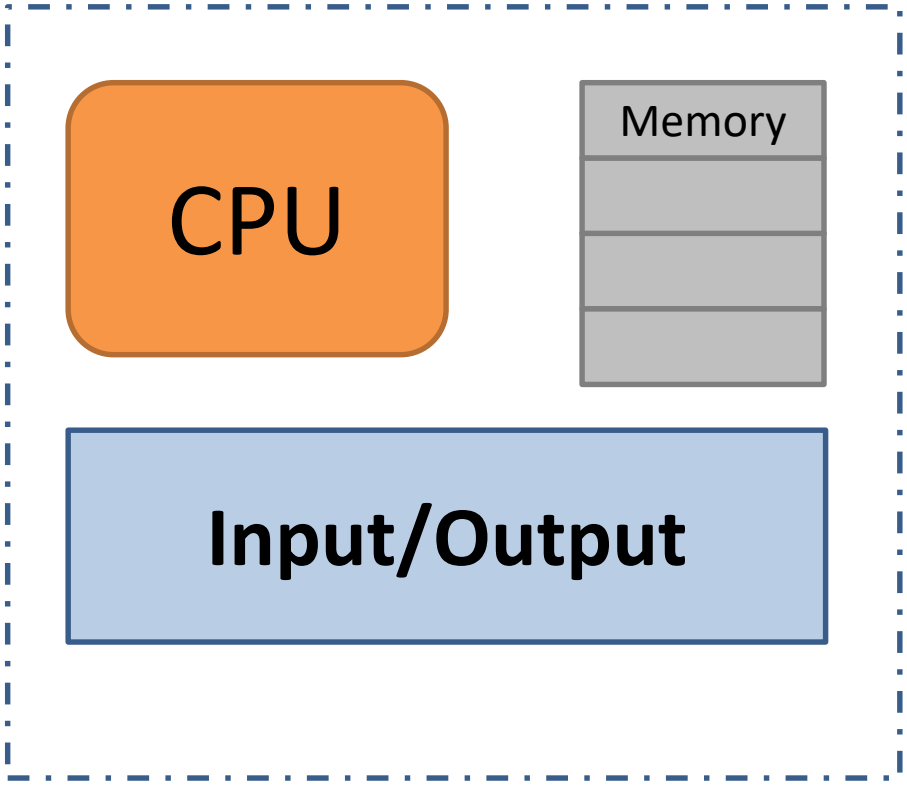
School of Software Engineering

Computer Organization

- Three subsystems
  - The CPU
  - The main Memory
  - The input/output



Central Processing Unit (CPU)

- Three parts
  - Arithmetic Logic Unit (ALU)
    - Performs arithmetic and logical operations
  - Registers
    - Data registers
    - Instruction registers
    - Program counter (also a register)
  - Control Unit

Main memory

- A collection of storage locations, each with a unique identifier called **address**
- Word: the number of bytes can one memory location store.
  - How many bits? Can be 8-bit/1-byte, 16-bit/2-byte, 32-bit/4-byte or 64-bits/8-byte?
- Word: number of bits transferred to and from memory per operation.
- Address: the identifier to access a word (value in a memory location)

Address space

- Address space: the total number of uniquely identifiable locations in memory
- Example:
  - How many bytes can the memory stored?
    - The capacity or size, e.g. 64kilobytes
  - The size of word
    - e.g. 1-byte
  - The address space: 0 ~ 65,535
  - That is 16-bit for each address (unsigned integer)!

Memory types

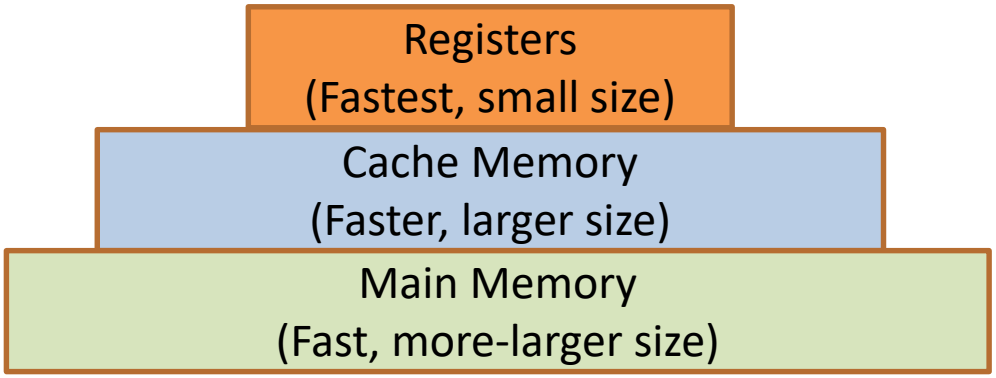
- Two types: RAM and ROM
- Random Access Memory (RAM)
  - Can be read and write (many times) by users
  - Volatile, data erased if the system is powered down.
  - Two categories:
    - Static RAM: using flip-flop gates; refresh no needed
    - Dynamic RAM: using capacitors; refresh needed;

Memory types

- Read-only memory (ROM)
  - Usually allowed to read but not write, e.g. the BIOS ROM
  - Nonvolatile
  - Variations
    - Programmed read-only memory (PROM)
    - Erasable programmed read-only memory (EPROM)
    - Electronically erasable programmed read-only memory (EEPROM)

Memory hierarchy

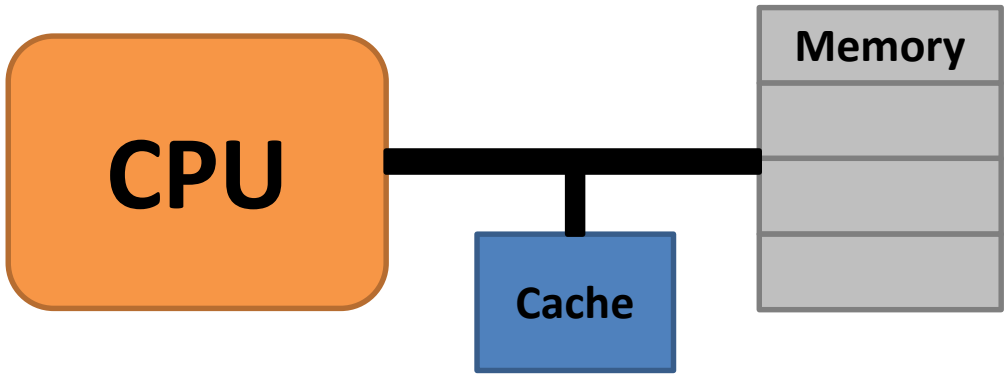
- Factors: speed, size and cost!



- Features
  - Speed： main memory < cache < registers
  - Size: main memory > cache > registers
  - Cost: main memory < cache < registers

Cache memory

- At any time contains a copy of a portion of main memory!!
  - Why? Why duplicate?
- 80-20 rule:
  - 80 percent time accessing only 20 percent of data



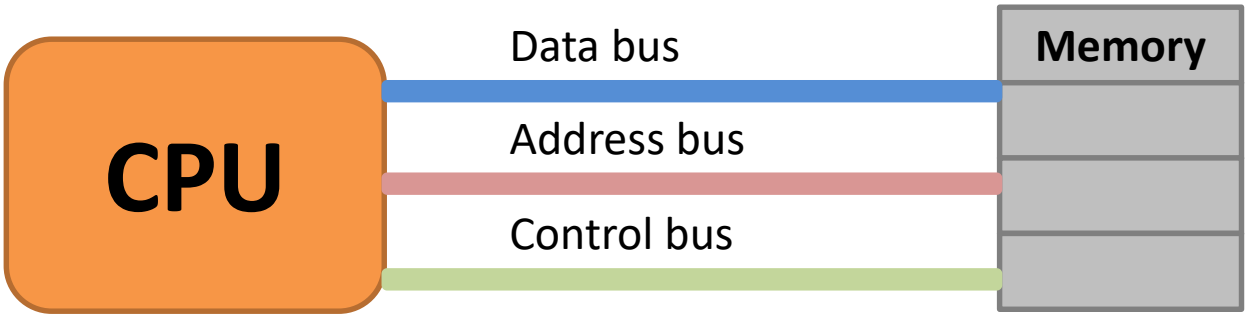
所有图片均来自网络

Input and Output

- Enable computer to
  - communicate with outside world
  - store programs and data even when the power is off
- Two categories
  - Non-storage: keyboard, monitor, printer … …
  - storage devices
    - Magnetic storage devices, optical storage devices

Connecting CPU and Memory

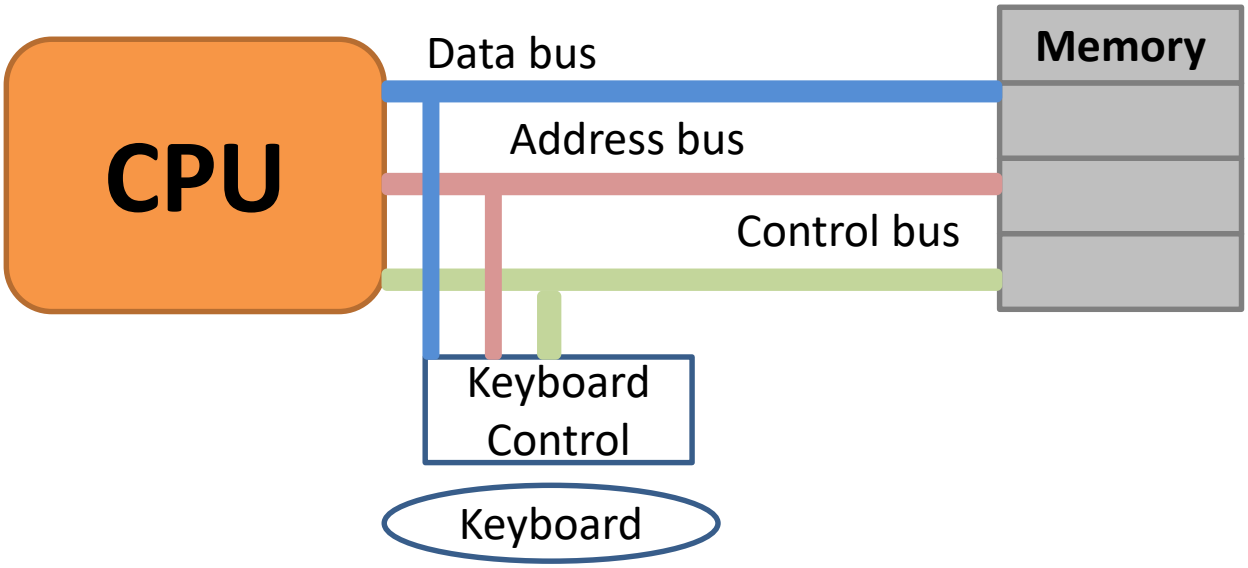
- Normally connected by three bus: data, address and control bus



- Bus are made of a set of wires.
  - For data bus, number of wires = the size of word;
  - For address bus, number of wires = number of bits of a address
  - For control bus, number of wires depends on the number of control instructions

Connecting I/O devices

- I/O devices are connected to bus through an intermediary called controller.
- Each kind of I/O device would have it's associated type of controller.

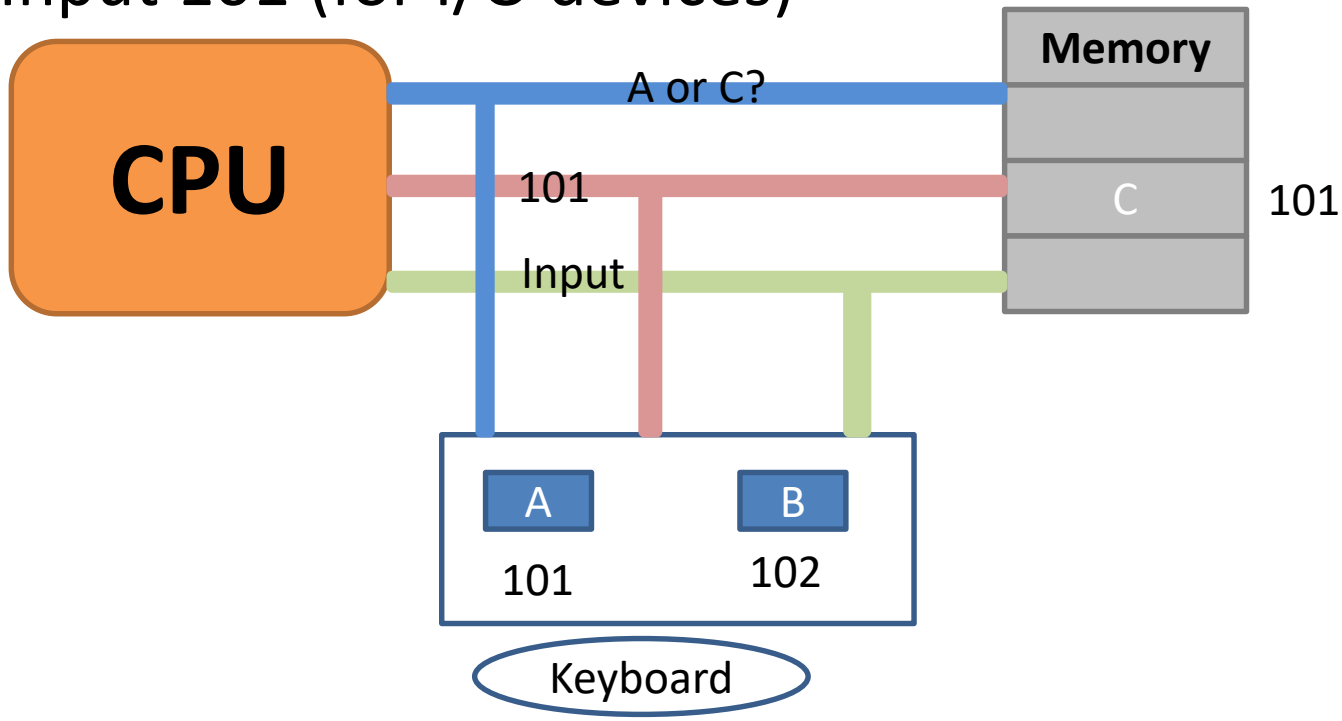


Addressing I/O devices

- The CPU usually uses the same bus to read data from or write data to main memory and the I/O device.
  - The only different must be the instructions
- Two methods:
  - Isolated I/O
  - Memory-mapped I/O

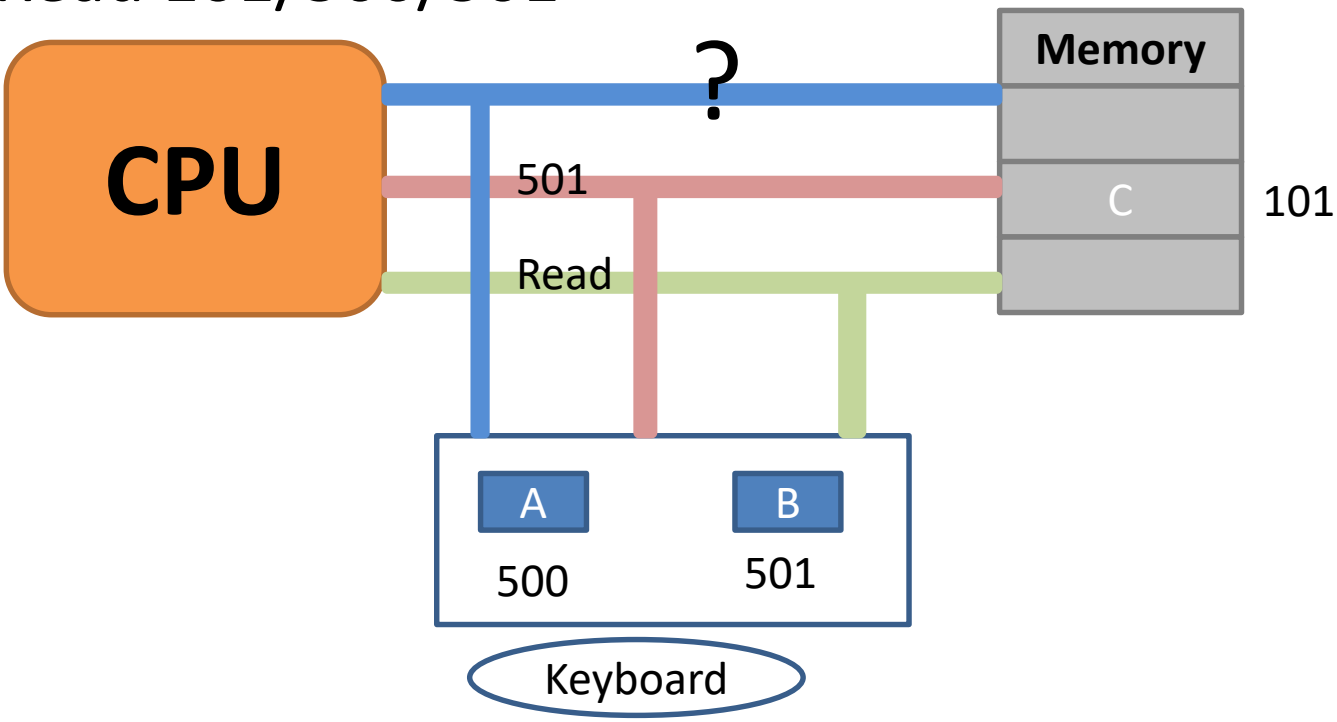
Isolated I/O

- Use different set of instruction to access I/O devices (from main memory)
  - Read 101 (for memory)
  - Input 101 (for I/O devices)



Memory-mapped I/O

- Use the same set of instructions, and treat each register in the I/O controller as a word in the memory.
  - Read 101/500/501

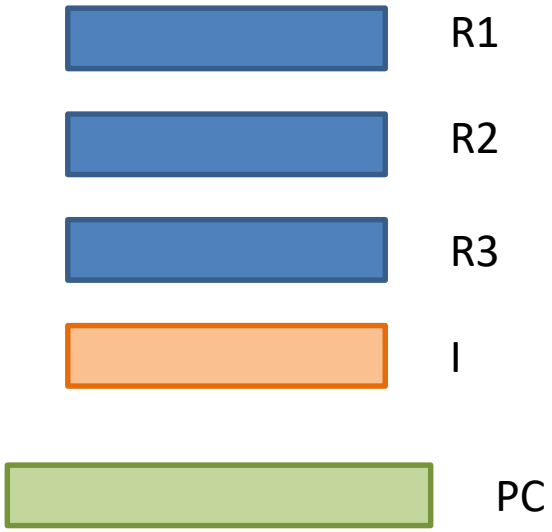


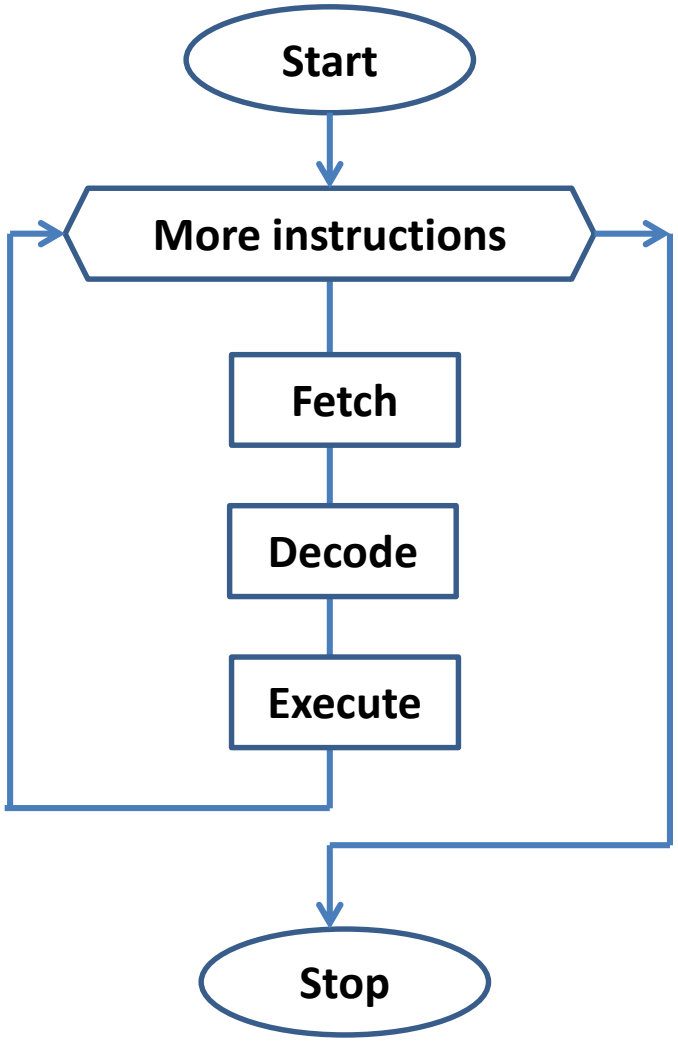
Program execution

- Programs: a sequence of instructions
- Programs: operates on input data, generates output data
- Machine Cycle
  - The CPU use repeating machine cycles to execute instructions in the program, one by one, from the beginning to end.

Machine cycle

- Instruction register
- Program Counter
- General Registers

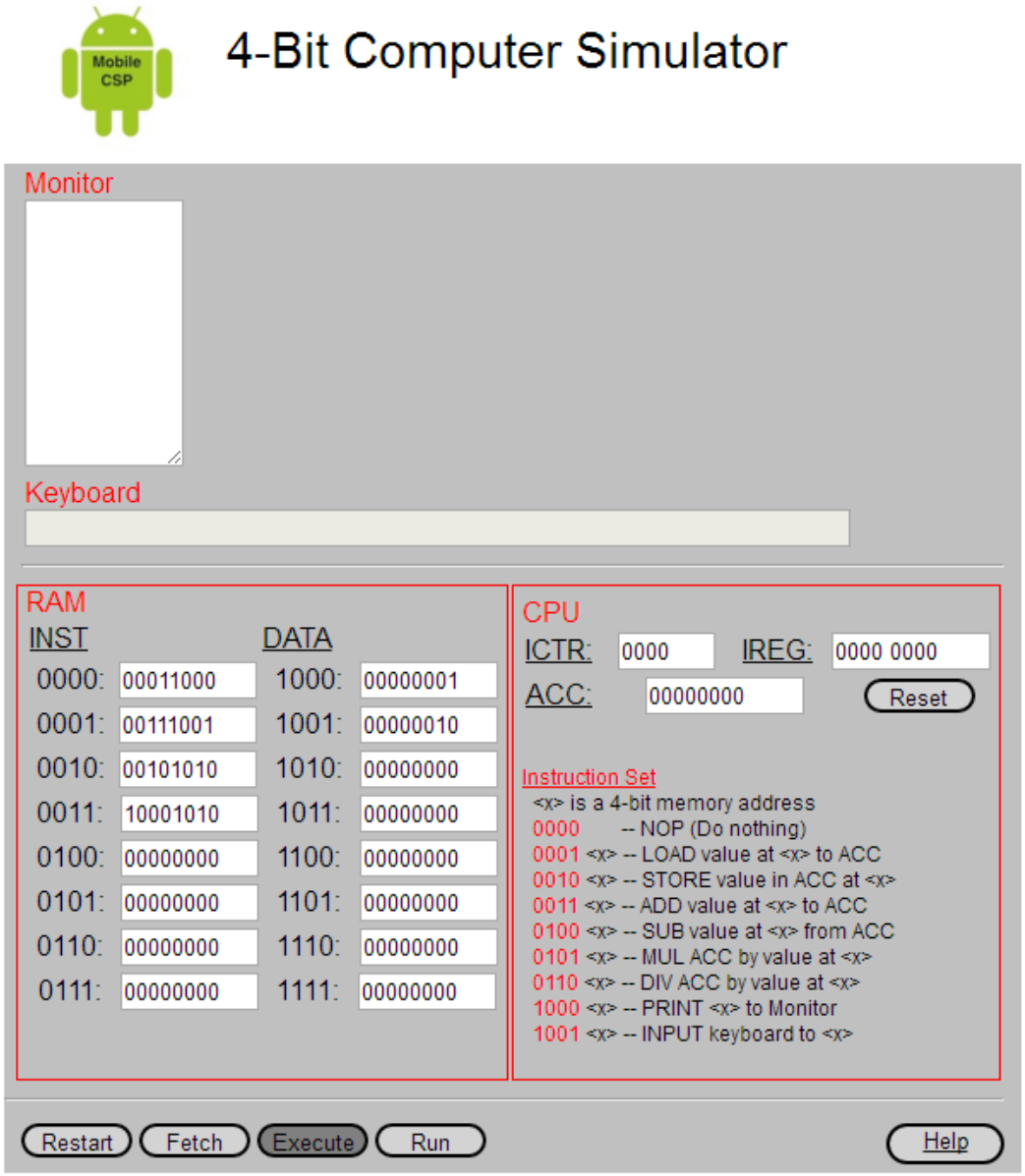




4-Bit Computer Simulator

冯.诺依曼体系结构

- **4-Bit Computer Simulator**
- http://appinventor.cs.trincoll.edu/csp/webapps/computer/add1.html

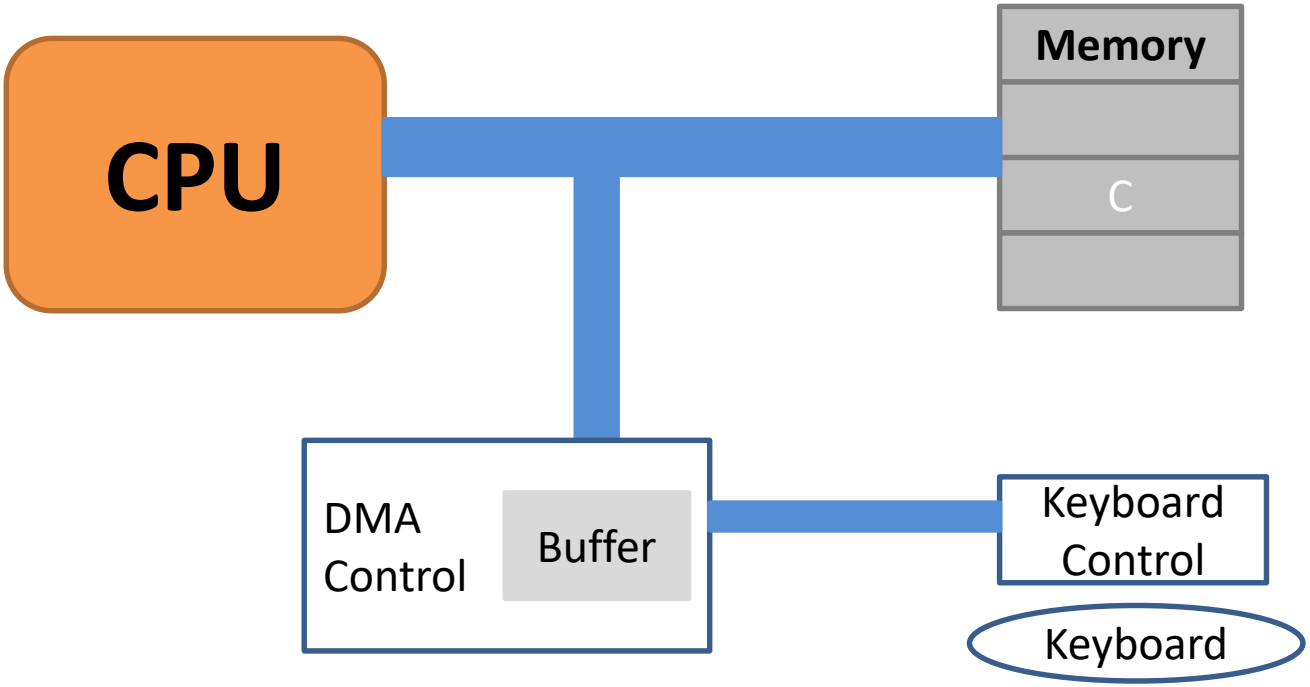


Input and output operations

- Programmed I/O
  - After command issue, CPU constantly checks the status of the device.
  - Waste of CPU cycles
- Interrupt-Driven I/O
  - The device must informs (interrupts) the CPU when it's ready
  - No waste of CPU cycles
- Data flow: I/O → CPU → Memory

Input and output operations

- Direct memory access (DMA)
  - Require a DMA controller
  - Data flow: : I/O → DMA → Memory



About Instructions

- Two different architectures
  - Complex Instruction Set Computer (CISC)
    - Pentium Series CPU@Intel

    缩小机器指令系统与高级语言语义差距，为高级语言提供更多的支持，是有效缓解“软件危机”的方法
  - Reduced Instruction Set Computer (RISC)

    减少指令平均执行的周期数